A STUDY OF RADIATION-TOLERANT VOLTAGE-CONTROLLED OSCILLATORS DESIGNS IN 65 NM BULK AND 28 NM FDSOI CMOS TECHNOLOGIES

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ABSTRACT

Phase-locked loop (PLL) systems are widely employed in integrated circuits for space analog devices and communications systems that operate in radiation environments, where significant perturbations, especially in terms of phase noise, can be generated due to radiation particles. Among all the blocks that form a PLL system, previous research suggests the voltage-controlled oscillator (VCO) is one of the most critical components in terms of radiation tolerance and electric performance. Ring oscillators (ROs) and LC-tank VCOs have been commonly employed in high-performance PLLs. Nevertheless, both structures have drawbacks including a limited tuning range, high sensitivity to phase noise, limited radiation tolerance, and large design areas. In order to fulfill these high-performance requirements, a current-model logic (CML) based RO-VCO is presented as a possible solution capable of reducing the limitations of the commonly used structures and exploiting their advantages. The proposed hybrid VCO model includes passive components in its design which are the key parameters that define oscillation frequency of this structure. This tunable oscillator has been designed and tested in 65nm Bulk and 28 nm Fully depleted silicon-on-insulator (FDSOI) CMOS technologies

The 65nm testchip was designed to compare the behavior of the proposed CML VCO with a current-starved RO and a radiation hardened by design (RHBD) LC-tank VCO in terms of tuning range, phase noise, Single event effect (SEE) sensitivity and design area. Simulations were carried out by applying a double exponential current pulse into different sensitive nodes of the three VCOs. In addition, SEE tests were conducted using pulsed laser experiments. Simulation and test results show that a CML VCO can effectively overcome the limitations presented by a RO-VCO and LC-tank VCO, achieving a wide range of tuning, and low sensitivity to noise and SEEs without the need for a large cross-section.

Further studies of the proposed CML VCO were done on 28nm FDSOI in order to reduce the leakage current and increase the switching speed. the same current-starved VCO and CML VCO were implemented on this testchip, and simulations were performed by injecting a double exponential current pulse energy into the previously defined sensitive nodes. The results show SEE sensitivity improvement without narrowing the tuning range or affecting the phase noise response.

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First, it is my desire to thank my family, who despite being far away have contributed infinite love, especially to my mother, thanks to whom I had the courage to dream beyond many barriers and thus undertake this new challenge. To my beloved Adriana, who with her occurrences, patience, understanding and deep love has been an essential basis for growing both academically and personally in this new stage in my life.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
BOX	Buried Oxide
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge-pump
DC	Direct Current
DUT	Device Under Test
FDSOI	Fully Depleted Silicon on insulator
IC	Integrated Circuit
LET	Linear Energy Transfer
MOS	Metal Oxide Semiconductor
NMOS	N-Channel Metal Oxide Semiconductor
PFD	Phase and Frequency Detector
PLL	Phase-locked Loop
PMOS	P-Channel Metal Oxide Semiconductor
RF	Radio Frequency
RHBD	Radiation-hardened by Design
RO	Ring Oscillator
SE	Single Event
SEE	Single Event Effect
SET	Single Event Transient
SEU	Single Event Upset
SoC	System on Chip

SPA	Single-Photon Absorption
SPICE	Simulation Program with Integrated Circuits Emphasis
SSSC	Saskatchewan Structural Sciences Centre
TCAD	Technology computer-aided design
TPA	Two-Photon Absorption
VCO	Voltage-Controlled Oscillator

1. INTRODUCTION

1.1 Research Background

Low-noise phase-locked loops (PLLs) recently have become more attractive in high-performance systems. They have emerged as a common component with increasing importance in analog electronics and high-speed wireless and wired communications systems where high-performance clock synthesizers, strong clock recovery systems, and local oscillators of high-stability and high-reliability are needed [1],[2]. However, the noise response is not the only important factor in terms of performance. In fact, PLLs may be subject to perturbations from single event effects (SEEs) that are generated by the strike of energetic particles. These effects are more common in high-altitude or space applications and even in some terrestrial devices' environments, where energetic particles such as heavy ions, alpha particles, protons, neutrons. or electrons are present. Depending on the, strength of the striking ions and affected nodes, an impact on the PLL can range from a temporary phase shift to the loss of PLL frequency lock [3],[4].

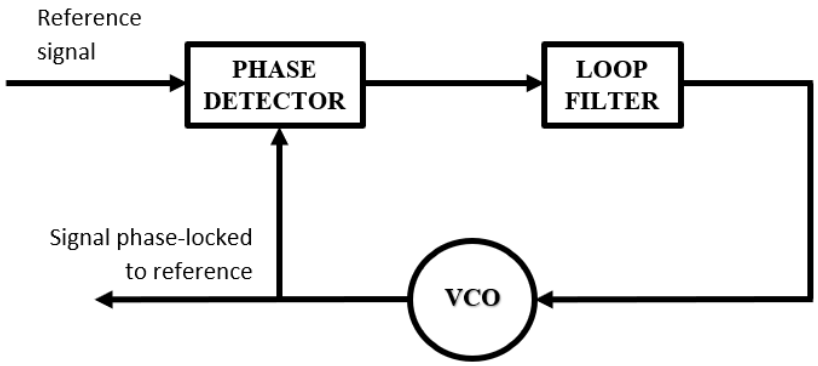


Figure 1.1 Block diagram of a basic PLL [1].

A PLL is a hybrid analog/digital system whose main function is to generate an oscillating output signal with constant frequency. A basic PLL structure, shown in Figure 1, is composed of a phase and frequency detector (PFD), which includes a charge-pump (CP), a loop filter, and a voltage-controlled oscillator [2].

Previous studies have identified the analog blocks of a PLL as the main sources of frequency deviation and output distortion. Charged particles striking on the charge-pump or the loop filter may produce variations in the control voltage which subsequently affect the VCO oscillation frequency, resulting in missing pulses and even causing oscillation interruption in some cases. Different hardening techniques have been employed to mitigate the SEE sensitivity in the charge-pump [3]-[6]. From the results it was proven that if the CP is hardened enough, the susceptibility of the VCO to SEE is increased, principally due to its large cross-section [7],[8].

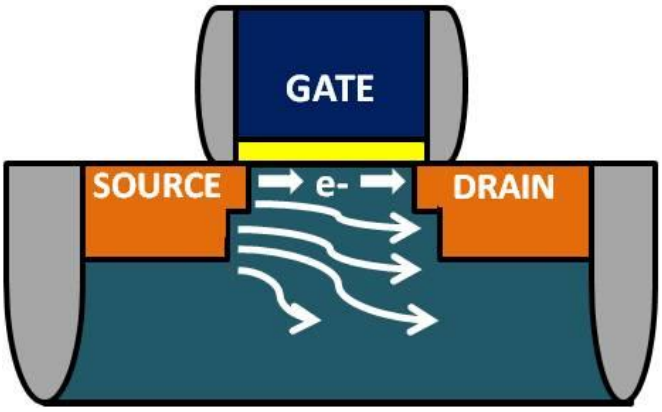
High performance VCOs are commonly implemented in Integrated Circuit designs as LC-tank oscillators or Ring oscillators. Compared to the RO-VCOs, the LC-tank VCOs present low-noise sensitivity. In terms of radiation tolerance, LC-tank VCOs show less sensitivity to SEEs compared to RO-VCOs [9],[10]. These characteristics are caused by the resonance frequency of this oscillator which is defined by the value of the passive elements that compose it, especially of the inductors that contribute to greater stability [11],[12]. For applications in which a good response to noise and high performance are required, LC-tank oscillators are optimal.

SEE tolerance has been studied in LC-tank VCOs. The initial approaches were developed on SiGe technologies without providing either a CMOS-related analysis or a mitigation technique [13]. Further studies related to CMOS bulk technologies have been conducted in order to analyze the SEEs of LC-tank structures. For this purpose, a fixed LC oscillator in 90nm bulk technology [14] and a radiation-hardened by design (RHBD) LC-tank VCO in 65nm bulk [15] were implemented. Results on both cases showed effective mitigation of the SEEs, but even when these approaches have fulfilled both noise and radiation tolerance requirements, the common limitations of LC-tank designs regarding a narrow tuning range and large design area have not been overcome.

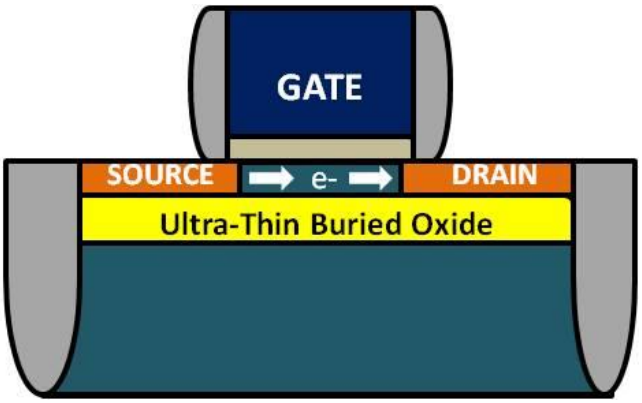
On the other hand, despite the low radiation tolerance and high phase noise, RO-VCO structures are able to provide a wide tuning range. In addition, since the oscillation frequency of this kind of oscillator is defined from the delay of the CMOS transistors, the required cross-section is relatively small compared to the LC-tank model, which allows large scalability at low cost. A common RO-VCO design contains a bias stage and a RO stage composed by an odd number of delay stages connected in a loop. SEE analysis shows that a charged particle strike occurs in the bias stage, an output signal modulation is produced due to the transient caused in the biasing nodes. This disturbance can be reduced by using redundant bias modules [7]. However, due to the larger

area, the RO stage presents more sensitivity to SEEs, producing odd harmonics when a charged particle injects energy into this loop [16]. The use of a fully differential delay stage in the RO stage partially reduces this vulnerability [17]. However, depending on the injected SEE energy, the output frequency modulation is still produced, causing missing pulses that lead in some cases to an oscillation interruption.

Other limitations have appeared, generated by these high-performance systems as a result of the hardening techniques used for both oscillators, which have been proposed mostly in bulk CMOS technologies. As the feature size of the technology is reduced, there have been increases in leakage currents and short channel effects like increased power consumption, and reductions in the switching speed [18]-[20].



(a)



(b)

Figure 1.2 Transistor cross-section in a) Bulk technology b) FDSOI technology [20] Copyright © 2018 IEEE.

Due to these limitations, various manufacturing companies have opted for fully depleted silicon-on-insulator (FDSOI) technologies. As shown in Figure 2, the main difference is the layer stack model used by FDSOI. This new technology uses an ultra-thin buried oxide (BOX) layer beneath the thin silicon layer that forms the channel. This ultra-thin BOX layer mitigates the current leakage by confining the channel. FDSOI has advantages over bulk technologies such as faster circuits and lower power consumption. Moreover, the layer stack model provides the advantage of controlling the body terminal by applying different reverse and forward body biasing levels, which allow for optimization of the design performance depending on the requirements. By controlling the body biasing voltage, the threshold level of the transistor can be modulated, and even lower threshold values can be employed. In addition, due to its layer stack structure, FDSOI technologies present an extremely small charge collection volume, which increase reliability in harsh radiation environments [21]. All these advantages make FDSOI potentially the best option for low-power designs [22]. However bulk technologies cannot be discarded and possible solutions for the previously mentioned drawbacks will be addressed in the following chapters of this thesis.

1.2 Motivation

Following an examination of the mitigation of the radiation effects on a PLL previous studies on hardening techniques for charge-pumps, this research focuses on the design of a radiation-tolerant voltage-controlled oscillator that is able to boost the positive features of a RO-VCO and a LC-tank VCO, including in these positive features the generation of a wide tuning range with low phase noise, and the reduction of power consumption.

The challenge is to design a hybrid VCO which will be a modified version of a RO-VCO. Its oscillation frequency will be defined by the propagation delay produced by an even number of stages connected in a loop, and it will employ passive components like the LC-tank VCO to tune this delay. From this principle, the goal is to obtain a wide tuning range and effectively increase the radiation tolerance. The proposed design will be implemented in 65nm bulk technology in order to compare the expected results with other common VCOs implemented using the same technology.

An additional motivation is the advantages of FDSOI technologies, which include reduction of power consumption and inherent radiation hardening. The advantages of this technology have not been explored fully in analog circuitry. The goal of this step is to implement the CML VCO design

and the previously employed RO structure, in order to verify by using a simulation where the proposed solution reflects improvements, thanks to the advantages of the technology

1.3 Objectives

Limitations have been identified in common VCO structures employed by a PLL system, both at the design and technology levels. Even though diverse hardening techniques have been applied, the proposed designs still have some critical failures that can generate catastrophic distributions in a high-performance PLL system. In this thesis, a radiation-tolerant VCO using two different CMOS technologies is presented. The scope of this thesis was determined from two main objectives:

1. Design a CML voltage-controlled oscillator in a 65nm bulk CMOS technology in order to evaluate its SEE sensitivity and phase noise performance compared to those of RO-VCOs and LC-tank VCOs.
2. Study the advantages of FDSOI CMOS technologies to analog circuits by analyzing the tuning range, phase noise, SEE tolerance and power consumption. The CML and RO-VCOs are to be implemented in a 28nm FDSOI technology in order to identify improvements compared with 65nm bulk designs.

All the studied VCO designs in 65nm bulk CMOS will be verified through SPICE simulations, beginning with a functional test of each VCO to determine tuning range and phase noise parameters. In addition, SEE simulations will be carried out by injecting a double exponential pulse with different peak amplitudes into sensitive nodes of each circuit. This simulation will provide information about the SEE tolerance of each VCO. All the obtained parameters will be used to compare both the electrical performance and the SEE response of the studied circuits and then to identify the improvements presented by the proposed CML VCO model. Following the functional verification at a simulation level, a testchip containing these VCO structures will be fabricated in 65nm bulk CMOS technology. This testchip will be used to carry out a functional test and an experimental SEE test using a two-photon absorption laser experiment. These experimental results will be analyzed in order to confirm the results obtained through simulation.

Furthermore, the VCO designs implemented in 28nm FDSOI CMOS technology will be verified through SPICE simulations. First the electrical performance will be verified in terms of phase noise, tuning range, and power consumption, and then the SEE response of the two structures will be tested by injecting a double exponential pulse with different peak amplitudes into the previously

identified sensitive nodes of the implemented designs. The obtained results will be used to determine the advantages of using FDSOI in analog designs.

1.4 Thesis Organization

This thesis is based on two author's manuscripts written during the current author's Master of Sciences studies, one previously published and other to be published the next year. All the simulation and experimental results presented in these manuscripts are organized to show the author's work in the study of high-performance radiation-tolerant voltage-controlled oscillators for phase-locked loop systems. Each chapter presents a brief summary that describes the relationship between the given chapter and the previous one. Conclusions are presented at the end of each chapter. The organization and main contents of this thesis are summarized below.

Chapter 1 gives a brief introduction to phase locked loop systems, sensitive nodes of PLL, and existing hardening techniques for the most common VCO designs implemented at the IC level, explaining the limitations in terms of electrical performance and radiation tolerance. Thus, this chapter presents the motivation for proposing a new radiation-tolerant VCO design in 65nm bulk technology in order to overcome the previously identified drawbacks and to explore the application of 28nm FDSOI technologies in a fault-tolerant VCO design. The chapter then outlines how a new radiation tolerant VCO will be simulated in both CMOS technologies and implemented in 65nm bulk technology for irradiation experiments.

Chapter 2 reviews the basic concepts of PLL structures, including a general description of its different blocks. A detailed explanation about ring oscillators and LC-tank oscillators is presented, showing basic schematic-level structures, governing equations and a detailed operation function, including the limitations of each model. A CML-based RO is outlined, paying special attention to different CML structures and their oscillation frequency equations. Also outlined are the basic mechanisms of SEE, including charge deposition and collection, and classifications of SEEs with an emphasis on transient errors in analog circuits. This chapter also includes the basic concepts related to SEE test methodologies, with special attention to the two-photon absorption (TPA) test. Finally, a brief description of FDSOI CMOS technology is summarized, including the main differences between this technology and bulk technologies, and its advantages in analog designs.

Chapter 3 presents the first manuscript in which a current-mode logic (CML) based RO-VCO is proposed as a solution to eliminate the limitations presented by commonly employed VCOs. The

proposed model is a hybrid structure that, like the RO uses the propagation delay as a key factor in defining the oscillation frequency, unlike the RO, the delay time of each buffer stage depends mostly on the value of passive components such as resistors and capacitors, rather than the transconductance of MOS transistors. This study includes simulations that were carried out to compare both electric performance and SEE sensitivity of the proposed design with a current-starved RO and a RHBD LC-tank VCO. The studied oscillators were designed and implemented in 65nm bulk CMOS technology. The fabricated testchip was tested using TPA laser experiments for SEE sensitivity analysis. The results demonstrated that the proposed structure requires a relatively small design area and presents low-SEE sensitivity, low phase noise and a wide tuning range.

Chapter 4 contains the second manuscript, in which the previously studied CML-based RO-VCO was designed and simulated in a 28nm CMOS FDSOI technology, the idea was to implement a radiation tolerant design and exploit the advantages of this new technology and exploit its inherent radiation-hardened behavior. The results demonstrate a noticeable enhancement in SEE sensitivity without narrowing the tuning range or affecting the phase noise response of the circuit. In addition, an increase in the switching speed and lower levels of power consumption were evidenced in the simulation information.

Finally, Chapter 5 summarizes this work, including detailed conclusions, and also outlines the contributions of this thesis and future directions for research.

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2. BACKGROUND

2.1 Phase-locked Loops

As introduced in the first chapter, a phase-locked loop is a control system whose main function is to generate an oscillating output signal that works at a specific fixed frequency. PLL structures employ a feedback connection to relate the frequency and phase of an output signal to the phase and frequency of an input reference signal [1]. A PLL is an elegant and efficient solution in numerous high-performance applications, including high-speed clocks, recovery systems, frequency synthesizers, correction systems, ADC converters, and power conversion systems, among others [2][3]. As shown in Figure 2.1, the building blocks of a conventional PLL structure are a phase and frequency detector (PFD), charge-pump (CP), loop filter, voltage-controlled oscillator (VCO), and frequency divider [4].

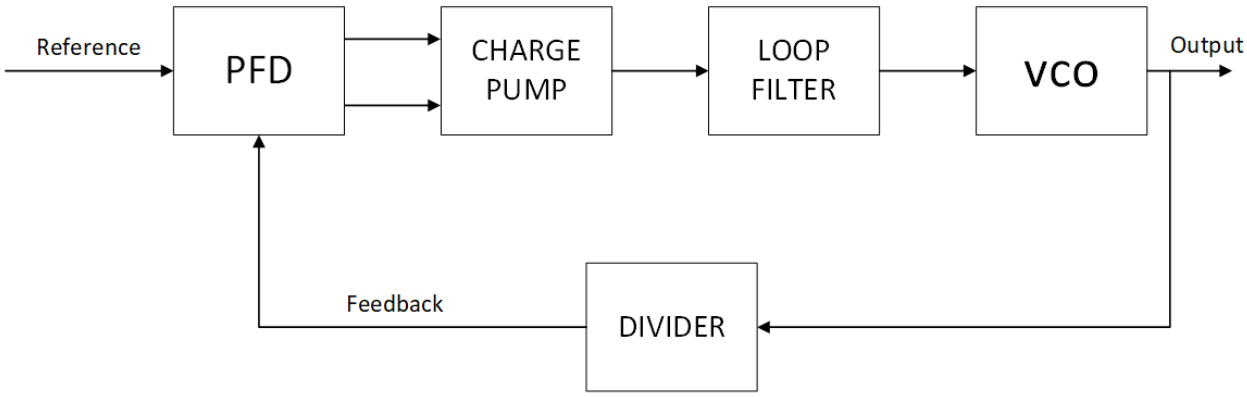


Figure 2.1 Building blocks of a conventional PLL structure.

The reference signal is usually generated by a crystal oscillator due to its low noise. The feedback signal is directly related to the VCO output. In the lock condition of a PLL, the output remains oscillating at a stable frequency. This condition is achieved because the feedback connection adjusts the control voltage of the VCO so that a constant phase and frequency difference between the two inputs is obtained. When an N factor frequency divider is employed, the PLL output frequency must be N times larger than the reference clock [5].

The lock condition of a PLL is limited by the output range, defined as the bandwidth limit within which the output signal can vary its frequency. If this condition is broken, the PLL will be able to recover its normal operation but the recovery time will considerably affect the performance of the system [6].

2.1.1 Phase and frequency detector

A phase and frequency detector is a sequential logic system used to detect the phase difference between two clock signals and to generate a signal sensitive to frequency. These two main functions assure the phase lock state of a given loop [7]. In a PLL system, the signals used to compare the phase and frequency difference are a reference clock, which is normally a crystal oscillator, and a feedback signal coming from the VCO output.

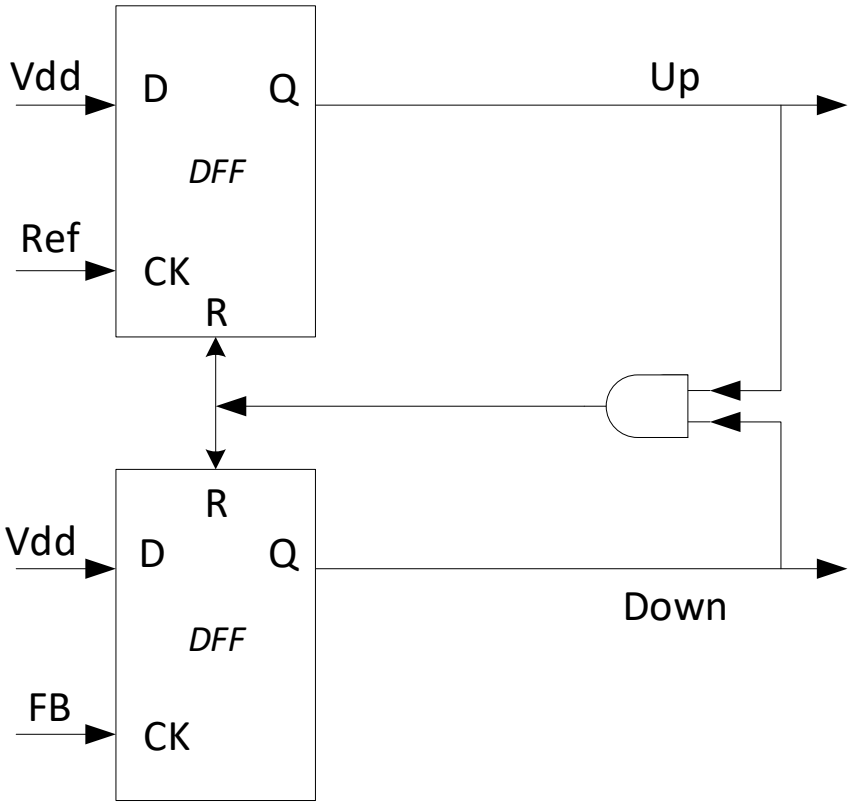


Figure 2.2 Conventional PFD

As shown in Figure 2.2, a PFD is a digital block with two outputs, UP and DOWN, that are dependent on the input clock signals and controlled by a reset connection [8]. These digital outputs are converted into an analog control voltage by using a charge-pump. The common PFD presents four logic states summarized in Table 2-1. In the first case, both UP and DOWN outputs are low,

which means the control voltage of the VCO will remain unaffected. When only the UP output is high, the control voltage will be increased in order to speed up the frequency of the VCO. In contrast, if only the DOWN output is high, the control voltage will be decreased in order to slow down the VCO frequency. Finally, if both outputs are high, the D flipflops employed as comparators will be reset through an AND gate.

Table 2.1 Logic States of a phase and frequency detector.

UP	DOWN	Effect on Control Voltage
0	0	No change
0	1	VCO frequency slow down
1	0	VCO frequency speed up
1	1	Reset activation

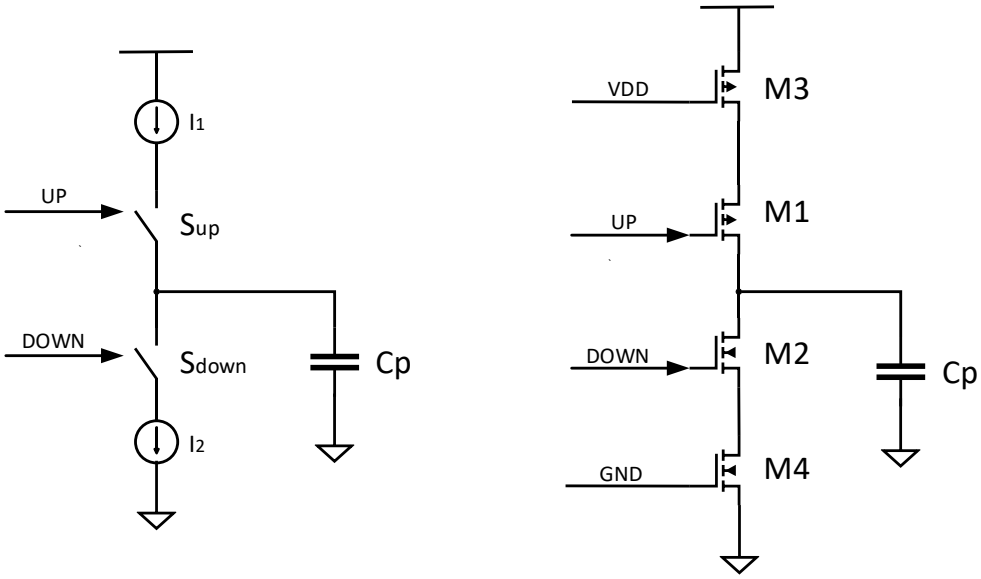
However, in some high-speed applications, a PLL is not able to respond to small phase errors, which is a main cause of crossover distortion, also known as the dead zone. The dead zone is produced when a mismatch occurs between the propagation delay of the reset path in the PFD and the switching time of the charge-pump. It is recommended that some buffer stages be added to increase the delay in the reset path of the PFD in order to avoid the dead zone [9].

2.1.2 Charge-pump and loop pass filter

The charge-pump is a key building block of a PLL that function as an interface circuit which converts the digital outputs from the PFD to an analog signal that will control the VCO. In other words, the output of the CP will be the VCO tuning voltage. When the PLL achieves the lock condition, the output of the CP will remain constant. This stability is a key factor in the design of a CP [10].

A conventional CP design, as shown in Figure 2.3(a) is composed of two symmetrical current sources, each connected in series to a switch. These switches are activated by the pulsating signals coming from the PFD outputs [11]. The upper current source I1 will inject a current when the UP output of the PFD is high, charging the capacitor CP, and therefore increasing the control voltage. On the other hand, the lower current source I2 will act as a current sink, discharging the capacitor CP which reduce the control voltage when the DOWN output of the PFD is high. When both UP

and DOWN signals are low, the control voltage remains the same. The amount of the increased or decreased charge is proportional to the PFD pulse widths. An ideal CP design will have equal UP and DOWN currents over the entire control range [4].



(a) (b)

Figure 2.3 Basic charge-pump (a) general schematic (b) transistor level schematic.

As shown in Figure 2.3(b), CMOS logic can be used to implement the CP. In this basic design, transistors M1 and M2 are acting as switches controlled by the PFD pulses, and transistors M3 and M4 are in saturation mode which means they are acting as current sources [4].

In general, PLL CPS employ more than one capacitor in the output. A loop filter usually is placed in the control voltage line to integrate and filter the error current or ripple generated by the CP. The most common loop filter is a low-pass filter composed of one resistor and two capacitors. The order of the filter is important in the stability of the PLL. Filters that present a high-quality factor will reduce the noise, resulting in easier PLL lock acquisition [1].

2.1.3 Feedback divider

A feedback divider is a digital block placed in the feedback line of a PLL. Its main function is to produce a feedback signal with a frequency N times smaller than the output frequency. Although this is an optional block, PLLs with a feedback divider are very attractive for some high frequency systems which require small and precise changes in frequency for frequency synthesis.

Programable designs commonly are employed in order to produce a wide range of frequency bands [1],[4].

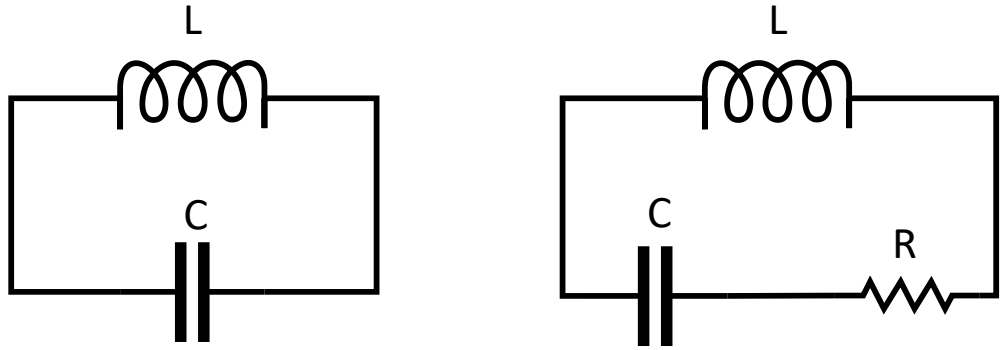
2.1.4 Voltage-controlled oscillator

An oscillator is a circuit that generates an alternate periodic output signal. A circuit can produce oscillation at a given frequency if it has a gain of at least 1 and a phase of 0 or a multiple of 2π. These minimum oscillation conditions are called the Barkhausen criterion. An optimal oscillator must present low phase noise and high stability [1].

Some applications require the oscillator to work at variable resonant frequencies. A tunable oscillator is one whose frequency varies depending on a control signal, which is generally a voltage signal, and can be built by making one of the parameters that define the resonance frequency of a given system variable. Some important factors of a VCO are central frequency, tuning range, tuning linearity, phase noise, and power dissipation. At the IC level, the most common oscillators are LC-tanks and ring oscillators [1],[4].

2.1.4.1 LC-tank VCO

An LC-tank oscillator is a common circuit employed in radio frequency applications. An ideal LC-tank resonator, shown in Figure 2.4(a), consists of a capacitor in parallel with an inductor in such a way that the impedances of these two components are equal and opposite. This results in an infinite impedance, and hence, an infinite quality factor. However, capacitors and inductors present resistive components which must be considered in the non-ideal resonator model, as shown in Figure 2.4(b) [1],[4].



(a) (b)

Figure 2.4 LC-tank resonator (a) ideal (b) non ideal.

The LC-tank oscillation frequency is defined by Equation 2.1. The value of the inductor L and capacitor C are the factors that define the oscillation frequency in the circuit. Therefore, a tunable LC-tank oscillator can be obtained by varying one of these parameters depending on the control signal [12].

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

Due to the complexity of changing the inductor value, the most common approach employs voltage-dependent capacitors in order to vary the oscillation frequency in the LC-tank structure, Figure 2.5 shows a conventional CMOS LC-tank VCO structure [1].

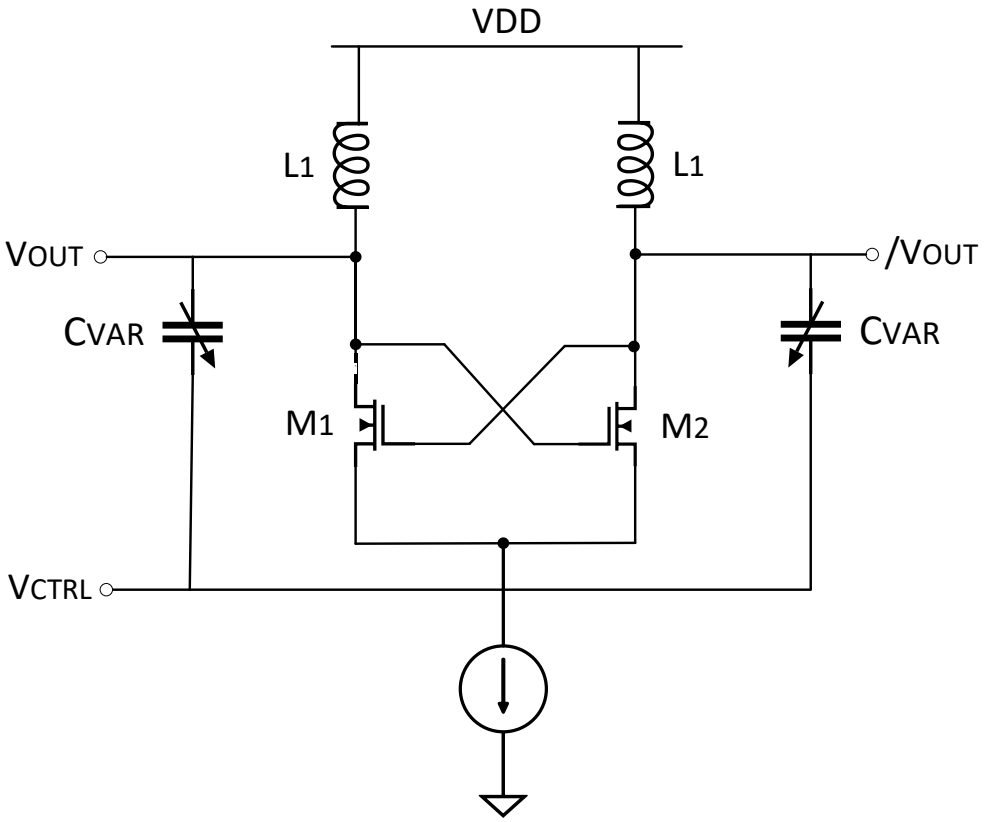


Figure 2.5 Conventional LC tank VCO.

The total capacitance of this VCO will consist of the value of the variable capacitors and the parasitic capacitance generated by the diffusion of NMOS transistors. LC-tank VCO structures are widely employed in high-performance applications principally because this tunable oscillator presents a high-quality factor and hence low jitter and phase noise, as well as high linearity and

low power consumption. However, this kind of circuit has some limitations, such as a narrow tuning range, and large design area due to the inductor. [1],[12]

2.1.4.2 Ring oscillator VCO

A ring oscillator is a common structure formed by an odd number of delay stages or CMOS inverters connected in a loop (see Figure 2.6). The number of delay stages must be chosen to satisfy different requirements such as oscillation frequency, switching speed, power consumption, and noise response. Generally, three to seven stages provide an optimal performance for most of the applications. [1],[13]

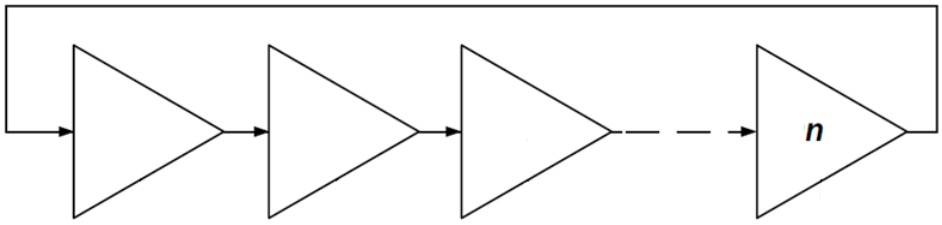


Figure 2.6 Basic Ring Oscillator design.

The oscillation frequency of the RO structure is defined by the total propagation delay T_d produced by each one of the N delay stages, as shown in Equation 2.2. In other words, a tunable oscillator can be built from a common ring oscillator by dynamically modifying either the number of delay stages in the loop or the delay produced by each stage. [13]

$$f_o = \frac{1}{2NT_d} \tag{2.2}$$

Since the dynamic variation of the number of stages represents a significant challenge that involves physical constraints, the most common RO-VCO is designed by modifying the delay of each stage through a biasing signal which controls the total current I_D that flows through each delay stage. In addition, as shown in Equation 2.3, the oscillation frequency of this VCO also considers the output capacitance C_T of each delay stage [13].

$$f_o = \frac{I_D}{2NC_T VDD} \tag{2.3}$$

Ring oscillators are commonly used due to their wide tuning range, large scalability, low cost and small design area. However, this kind of structure has serious drawbacks in terms of radiation tolerance and high phase noise [1],[13].

2.1.4.3 CML VCO

A current mode logic oscillator is a modified version of a ring oscillator. As shown in Figure 2.7, the CML-based RO employs differential inverters with a resistor load as delay stages. The output swing of this structure is determined by the value of a tail current rather than by voltage levels. A conventional CML oscillator uses an even number of stages connected in a loop with two feedback lines [13],[14].

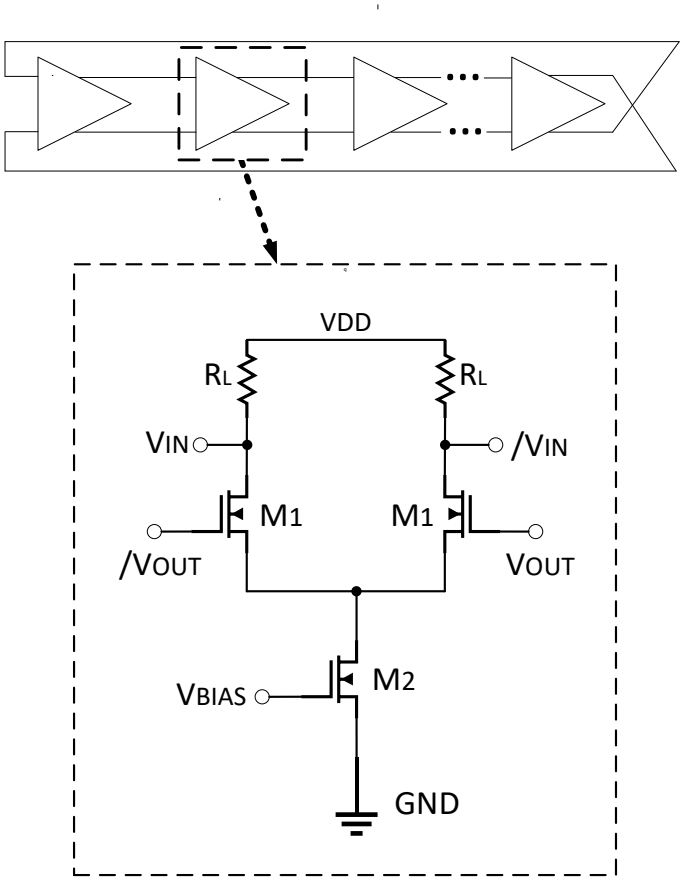


Figure 2.7 CML oscillator block diagram and differential delay stage schematic.

The oscillation frequency of a CML oscillator is given by Equation 2.4. From this equation, it can be seen that the key factors that define the resonant frequency of this system are the load resistor R_L and the output capacitance C_p at each delay stage. Therefore, a tunable oscillator can be made from a CML RO by using a variable load resistor value or a voltage-dependent capacitance value [1],[14].

$$f_o=\frac{1+g_{ds}R_L}{2NC_pR_L} \tag{2.4}$$

2.2 Single Event Effects

Single event effects (SEEs) are unexpected alterations of the normal operation of an integrated circuit produced when a sensitive node of an electronic circuit is hit by a highly energetic particle, such as proton, neutron, alpha particle, or heavy ion. The perturbations caused by the impact of these charged particles include temporary interruption of the normal operation, changes in logic levels, or permanent damage of an electronic device [15].

2.2.1 Charge deposition and collection

The basic mechanism of a SEE generation is independent from the energetic particle that produces it. Within the SEE generation procedure, the charge deposition and collection are important factors to consider [16]- [18]. When a charged particle passes through a semiconductor material, the particle generates extra electron-hole pairs along a cylindrical track while losing its energy as shown in Figure 2.8(a). Depending on the incident particle, the charges in the semiconductor material can be generated by direct or indirect ionization [19].

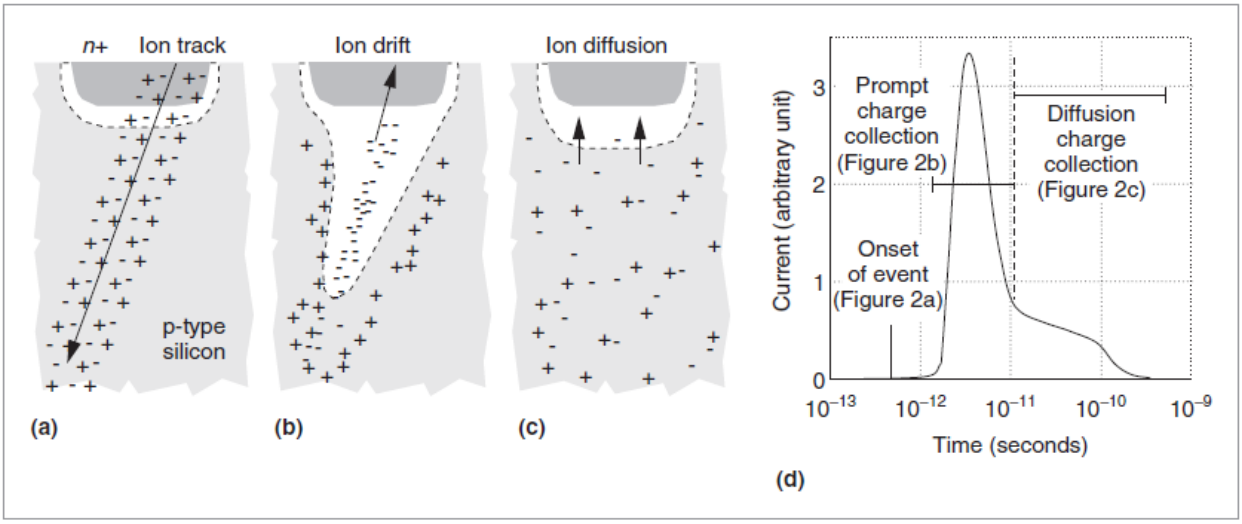


Figure 2.8 Charge deposition and collection in a reverse-biased junction (a) deposition, (b) collection, (c) drain off, (d) resultant current pulse [20] Copyright © 2005 IEEE.

In direct ionization, charged particles, such as heavy ions deposit energy into the semiconductor material, generating SEE automatically. In the case of a light particle without enough energy to generate a SEE, indirect ionization is produced since this kind of energetic particle can elastically or inelastically collide with a semiconductor nucleus. On the other hand,

indirect ionization occurs because of light particles that, despite not having enough energy to cause SEE, can cause a nuclear displacement by means of elastic or inelastic collisions with a semiconductor nucleus, generating secondary charged particles which are able to release electron-hole pairs along their tracks [15],[19].

If the ion track is located near a sensitive node, such as a p-n junction, which presents a high electric field, the released charge is easily collected through a drift process that extends the depletion region deep into the substrate, as shown in Figure 2.8(b), this produces a transient current at the junction contact. Once the diffusion takes control of the collection process, the collected charge is drained off the affected junction, as shown in Figure 2.8(c). The resultant current pulse generated by the charge deposition and collection process is shown in Figure 2.8(d) [20]. The resultant curve can be represented as a double exponential current impulse. The different parameters of this curve such as peak amplitude, rising time and pulse duration can be obtained by using the simulator TCAD, and will differ for different design technologies.

2.2.2 Single event transient

Single event transients (SETs) in analog circuits can be defined as temporary observable perturbations that occur as a result of the strike of a charged particle against a sensitive p-n junction or node in integrated circuits [22]. The effect of SETs in analog circuits will vary depending on the sensitivity of the affected system. The most common problems generated by SETs in analog circuits are phase shift, amplitude perturbations, and interruption of oscillating signals [23].

2.2.3 SEE testing

Since SEEs are unexpected events that affect the normal operation of a circuit, a radiation test to assure the correct performance of an IC is mandatory. Although the optimal testing method is to send electronic systems into space, the high cost required for this kind of evaluation has led to the development of several SEE experiments that effectively reproduce the radiation effect at ground-level.

2.2.3.1 Particle tests

Particle accelerators are facilities designed for the reproduction of radiation environments by using a wide variety of ions with different energetic levels and flux. Around the world there are many particle accelerators facilities dedicated to SEE testing procedures. The most widely used

particle accelerator facilities are Texas A&M, Berkeley lab, Indiana University Cyclotron Facility, and Canada's TRIUMF.

The most common particle test is carried out by using a proton beam. This test is recommended when an IC design present sensitivity to low-energy ions. Proton tests may need to be carried out if available heavy-ion experimental results show that the IC is sensitive to low-LET ions. In cases where energy of the applied beam is lower than 30 MeV, the IC must be prepared in advance through a de-packing procedure in which the lid of the IC package is removed in order to expose the die to the protons. In contrast, high-energy proton beam experiments do not require this extra preparation [24].

2.2.3.2 Pulsed laser test

Pulsed laser tests employ charge generation using photon effects[25]-[28]. Laser facilities are classified based on the type of laser used, those types being single photon absorption (SPA) lasers and two-photon absorption (TPA) laser experiment. A single photon absorption laser consists of a single photon with enough energy to exceed the semiconductor bandgap and generate an electron-hole pair. Previous studies have demonstrated that for an accurate SEE representation the pulse length of this kind of laser must be in the range of picoseconds [29]. In modern IC technologies that employ more and thicker overlayers, SPA lasers have a great limitation as they cannot penetrate deep enough into the substrate due to their relatively small wavelength.

A two-photon absorption laser experiment requires two simultaneous photons to generate an electron-hole pair as a single photon cannot produce enough energy to exceed the substrate bandgap [30]. This kind of laser appeared to be solution to the inherent limitation of SPA lasers, but this system requires high light intensity in order to simulate accurately the radiation effect.

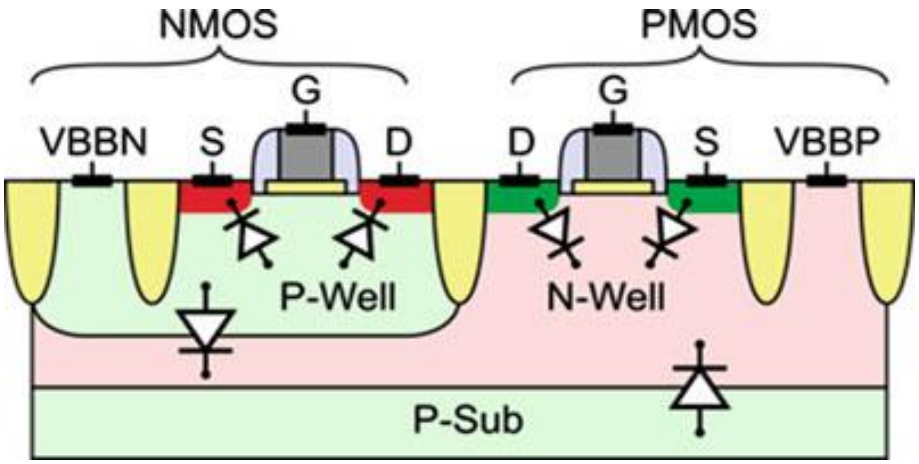
Pulse laser tests are very attractive for SEE research mainly due to their low cost, easy access, and simplicity. In a laser testing procedure, the laser pulse is focused on a device in order to scan it. The energy level is increased in order to determine the radiation tolerance of the device under test (DUT). Since the laser pulse presents a diameter of around 1μm, this kind of testing provides control in terms of pulse duration and location of the injected charge [27].

In spite of the great acceptance of laser tests, new packaging techniques, such as flip-chip generate new challenges for this type of experiments. For example, in this type of packaging, the laser pulse must be injected into the circuit of interest from the back of the package. This requires

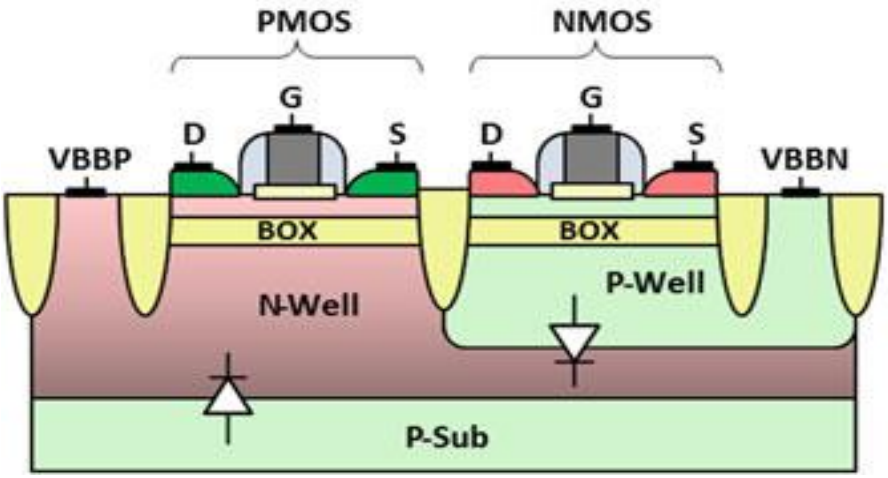
a previous preparation of the integrated circuit which must be opened at the back, and the substrate over the entire die must be thinned so that the laser penetrates enough to interact with the circuit tested [27].

2.3 FDSOI Technology

The scaling down of the transistor size due to Moore's law has increased the short-channel effect, causing some undesired drawbacks, such as higher leakage, higher power consumption, increasing difficulty in controlling the channel. FDSOI was developed as an extension of Moore's law without requiring elaborated designs.



(a)



(b)

Figure 2.9 Transistor cross-section with parasitic diodes (a) bulk (b) FDSOI [31] Copyright © 2017 IEEE.

This planar process takes advantage of existing manufacturing methods and improves them through key innovations, providing smaller design areas, performance improvements, a considerable reduction in power consumption, and a flat process that takes advantage of the methods of existing manufacturing to offer reduced silicon geometries [32].

Unlike standard CMOS technologies, FDSOI presents substantial changes in the layer stacking model. This new technology employs a very thin silicon layer to implement the channel, and places an ultra-thin isolator layer of thickness equal to 10 to 20 nm, called buried oxide, between the thin silicon channel and the substrate, which fully depletes the transistor so that no channel doping is required. Thanks to this extra oxide layer, FDSOI technologies can provide improved electrostatic characteristics, principally because the parasitic capacitances between the source and drain are eliminated. as shown in Figure 2.9 [32],[33].

Unlike bulk technology that has limited body biasing, the buried oxide layer in FDSOI technology provides control over the transistor not only through the gate voltage but by applying a different biasing voltage to the substrate. Through this backgate control the substrate is polarized, and hence, the threshold voltage of a transistor can be widely varied depending on the requirements in terms of switching speed and power consumption [32].

2.3.1 Advantages of FDSOI for common circuit design

The advantages of FDSOI obtained by the improved electrostatic performance of this technology can be appreciated in some common circuit blocks. In digital designs, the most important factors to consider are power consumption and switching speed. A FDSOI structure reduces the parasitic capacitance of a transistor, providing more efficient circuits with faster switching speed. In addition, the reduction of the parasitic capacitance provides a reduction of the leakage current, and hence, reduces static power dissipation, which can be a significant problem in large logic circuits [32].

On the other hand, the advantages of FDSOI in analog blocks have not been thoroughly studied. The fully isolated channel provided by FDSOI technologies reduces considerably the gate capacitance and leakage currents. This channel isolation makes FDSOI transistors immune to latch-up, which means smaller and even simple analog designs can be used without affecting the performance of a given system. Compared to bulk technologies, lower noise sensitivity and higher gains are possible by using FDSOI, thanks to the absence of channel doping and pocket implants

in a fully depleted transistor [32]. In terms of radiation tolerance, the level of charge collection presented by FDSOI technologies is considerably smaller than bulk technologies. This behavior shows that FDSOI has an inherent radiation tolerance, so it works well in environments with high levels of radiation [34].

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3. A RADIATION-TOLERANT CML VOLTAGE-CONTROLLED OSCILLATOR IN 65NM CMOS

Submitted as:

J. Cardenas, Z. Zhang, C. Gu, L. Chen, and R. Chen, "A Radiation-Tolerant CML Voltage-Controlled Oscillator in 65 nm CMOS," *IEEE Transactions on Nuclear Science,* 2019.

Basic knowledge related to phase-locked loops and the main building blocks of this kind of system, in addition to general information of single event effects and testing methods were presented in the previous chapter. Previous studies point to the voltage-controlled oscillator as one of the most radiation sensitive blocks in a PLL. However, the evidence also emphasizes the limitations presented by each of the commonly used VCO designs, especially in harsh radiation environments. Therefore, a new VCO alternative will be proposed and analyzed.

In this chapter, a radiation-tolerant CML VCO is presented as a suitable option for high-performance applications. Simulated and experimental analysis are employed to compare the proposed CML VCO with a current-starved RO-VCO and a LC-tank VCO in terms of electric performance and SEE response. The benefits of the proposed design are improved SEE tolerance and reduced phase noise compared to the RO-VCO, and a wider tuning range and smaller design area compared to the LC-tank VCO, which suggests significant mitigation of the previously identified drawbacks.

Contributions on this manuscript:

- Jaime Cardenas: Circuit design, electrical performance and SEE simulations, data obtention and analysis of SEE experimental results.
- Zhichao Zhang: Circuit design, simulations and experiment advisor
- Cheng Gu: TPA Laser experiment execution
- Li Chen: Idea developing advisor, and paper review
- Rui Chen: TPA Laser experiment execution, data analysis advisor

A Radiation-Tolerant CML Voltage-controlled Oscillator in 65 nm CMOS

Jaime S. Cardenas, Cheng Gu, Li Chen, Rui Chen, and Zhichao Zhang

Abstract

Ring oscillators and LC-tank structures have been widely chosen in high-performance PLLs. However, these common topologies present some drawbacks principally in terms of tuning range, phase noise, SEE sensitivity, and design area. In this paper, a current-mode logic (CML) based RO-VCO is proposed as a hybrid design able to overcome the limitations presented by the typically used voltage-controlled oscillators (VCOs). In the proposed structure, the delay time of each buffer stage is mainly determined by the value of passive components, such as resistors and capacitors, instead of the transconductance of MOS transistors. Simulations are carried out to compare the electric and radiation performance of the proposed design with a common current-starved RO and a RHBD LC-tank VCO. The three compared VCO are implemented in standard 65nm CMOS technology. Two-photon absorption laser experiments are conducted to test the SEE sensitivity. Simulation and experimental results suggest that the proposed VCO structure effectively mitigates the SEE effects and high phase noise sensitivity presented in the RO structure, and additionally, overcomes the limitations of the LC-tank VCO by providing a wide tuning range without requiring a large design area.

Index Terms

current mode logic (CML), single event effect (SEE), voltage-controlled oscillator (VCO), radiation-hardened by design (RHBD), two-photon absorption (TPA) laser experiment

3.1 Introduction

Phase lock loops (PLLs) have become a common IC component. This kind of block plays an important role in analog electronics and communications circuitry by acting as high-performance clock synthesizers, clock recovery circuits and local oscillator frequency generators. Its main function is to generate a highly accurate oscillating output signal at a specific frequency. However, PLLs may be subject to single event effects (SEEs) through the strike of charged particles, such as protons, and alpha particles, when exposed to a radiation environment. Depending on the energy and struck node, the SEE on a PLL can produce single event upset (SEU) or single event transient

(SET) pulses, impacting the performance of its blocks, causing phase and frequency shift, and potentially result in loss of PLL frequency lock.

A PLL is essentially a combination of digital and analog circuits. From previous studies, it has been found that charge-pumps (CP) are the most sensitive components to SETs in a PLL. This is because the main function of this block is to provide a multilevel DC voltage which controls the oscillation frequency of the VCO. Different hardening techniques for CPs have been proposed [1]-[2], showing that if the CPs are hardened enough, the VCO becomes the most sensitive part of the PLL. This is because the VCO has the largest cross-section, and as a result most of the SETs in a PLL are generated due to strikes in the VCO [3].

Commonly, VCOs are implemented by IC designs such as LC-tank oscillators or ring oscillators (RO). LC thank oscillators have outstanding performance in terms of phase noise, jitter, and are intrinsically more SET resistant than ROs [4]. This is due to the presence of inductors that present lower impedance compared with the impedance of a diode-connected transistor. SET tolerance of the LC-tank VCO has been tested in previous approaches based on SiGe technologies in [5] but without providing a deep analysis. Subsequent studies have been proposed employing a radiation hardened by design (RHBD) LC-tank oscillator using CMOS 90nm technology [6] and also a RHBD LC tank VCO in CMOS 65nm technology [7]. From the analysis, both designs proved to mitigate the SET effectively. However, both designs require larger silicon areas and present a limited tuning range requiring careful calibration.

Despite the high sensitivity to SETs, ROs are more attractive because of their wider tuning range, large scalability, low cost, and small die area. A RO-VCO basic structure is composed of the bias stage and the RO stage. Several proposed RO-VCO approaches effectively mitigated the SET effects, such as output frequency modulation due to input bias perturbations, generation of odd harmonics, and oscillation interruption [8]-[11]. Nevertheless, the previously proposed designs have not solved the strong output signal modulation when the SE strike is propagated through the delay stages, and which may lead to the presence of missing pulses.

To overcome the limitations presented by the LC-tank and RO-VCOs, a CML-based RO-VCO is proposed. This hybrid VCO is able to produce a tunable oscillation frequency based on the delay of buffer cells which is mainly determined by the value of passive components such as resistors

and capacitors, instead of the transconductance of MOS transistors, and which achieves a wide range of tuning and a significant reduction of sensitivity to SEEs. The circuit was designed and fabricated in 65nm CMOS bulk technology. Simulations were carried out to test both the electric performance and the SEE response. In addition, a two-photon absorption (TPA) laser experiment [12]-[15] was used to conduct an empirical SEE study on the fabricated chip. The simulation and experimental results suggest the SET effect was effectively mitigated.

3.2 Circuit Design

3.2.1 LC-Tank VCO

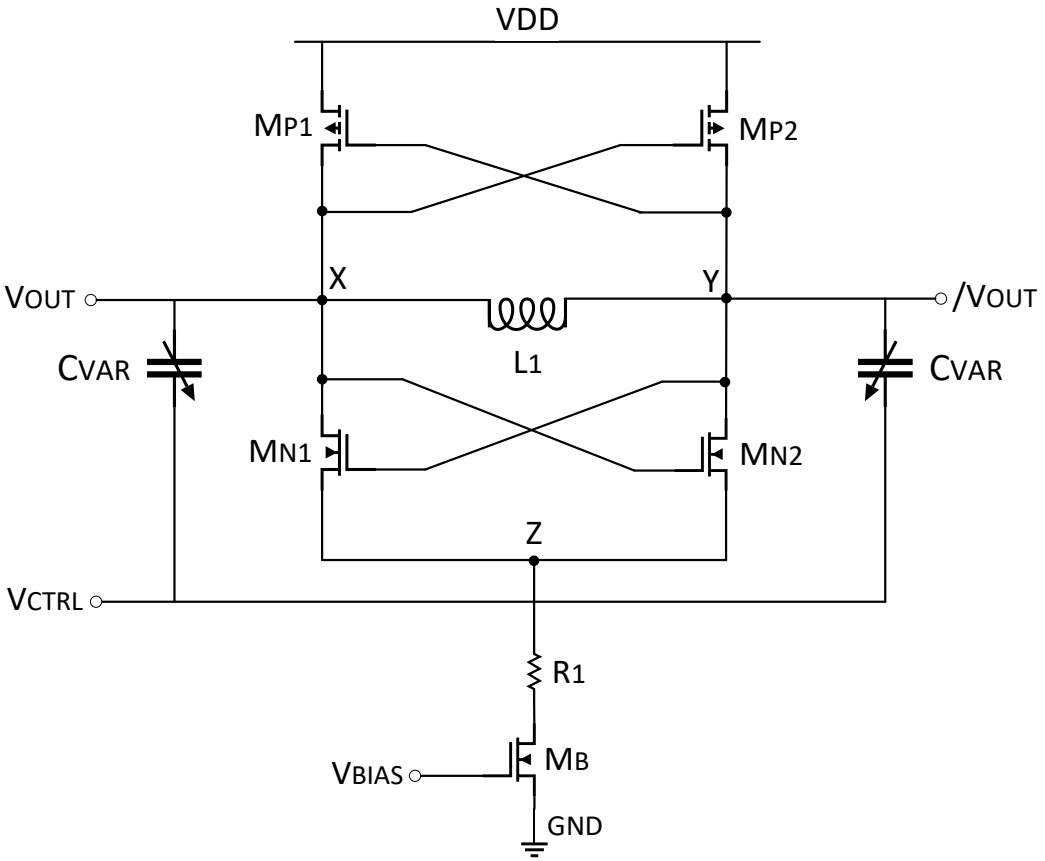


Figure 3.1 RHBD LC-Tank VCO with cross-coupled PMOS load and decoupling resistor.

The basic LC-tank structure is formed by an inductor L connected in parallel with a capacitor C, and the resonant frequency of this oscillator can be determined from Equation 3.1.

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.1}$$

This LC-tank circuit is a lossy resonator due to the resistive component R generated by capacitors and inductors, connecting the resonator block to an active circuit that provides a negative resistance value cancelling the losses.

The chosen LC-tank VCO is a low-noise differential VCO [16]-[18]. The structure showed in Figure 3.1 uses two cross-coupled NMOS transistors which have a transconductance large enough to cancel the resistive component produced by the tank. This topology also includes a tail bias transistor M_B hardened with a decoupling resistor R1 that reduces the perturbations in the bias node and consumes a large portion of the voltage drop caused by a SE. In addition, the design uses a cross-coupled PMOS load in order to increase the output swing and reduce the circuit susceptibility to SEEs. Finally, to achieve a wider tuning range, voltage-controlled varactor capacitors C_{VAR} were employed. The total capacitance in this RHBD LC-tank can be expressed as:

$$C_{total}=C_P+C_{VAR} \tag{3.2}$$

where C_P is the parasitic capacitance of the four cross-coupled MOS transistors and C_{VAR} is the capacitance of varactors, which is mainly determined by the control voltage V_{CTRL}. The central oscillation frequency of this VCO will be:

$$f_{VCO}=\frac{1}{2\pi\sqrt{LC_{total}}} \tag{3.3}$$

Although in theory this topology presents low sensitivity to noise and SEEs, the drawback of this kind of structure is the limited tuning range achieved.

3.2.2 Current-starved RO-VCO

A common current-starved ring oscillator shown in Figure 3.2 has two main stages: a ring oscillator stage consisting of an odd number of delay stages connected in series forming a loop, and an input bias stage based on current mirrors to control the current flow through each delay stage.

The oscillating frequency of this VCO can be tuned by varying the total amount of charge supplied to the delay cells using a control voltage. The oscillation frequency of this VCO can be calculated using Equation 3.4.

$$f_{osc}=\frac{1}{2N\tau}=\frac{I_D}{N.C_{total}.V_{DD}} \tag{3.4}$$

where I_D is the current flowing through each delay stage, N is the total number of delay cells, C_{total} is the total output capacitance at each delay stage and V_{DD} is the supply voltage. Even though this kind of VCO can generate a wide tuning range, its sensitivity to noise and SEEs is very high since its oscillation frequency depends on the transconductance of the transistors generated by the delay cells.

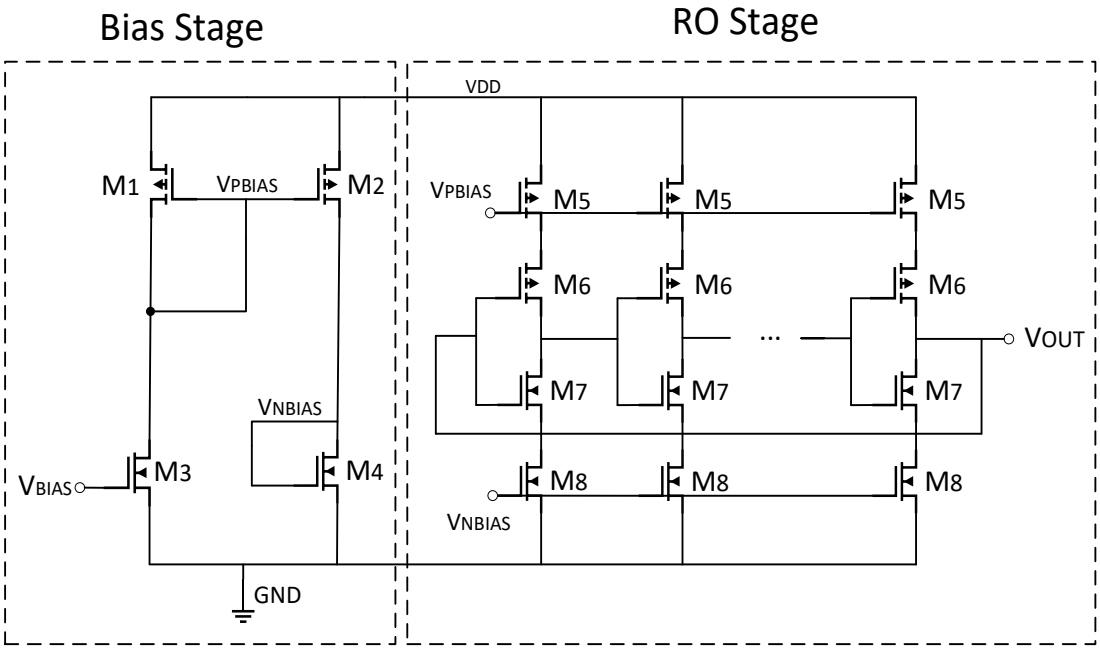


Figure 3.2 Current-starved Ring Oscillator VCO

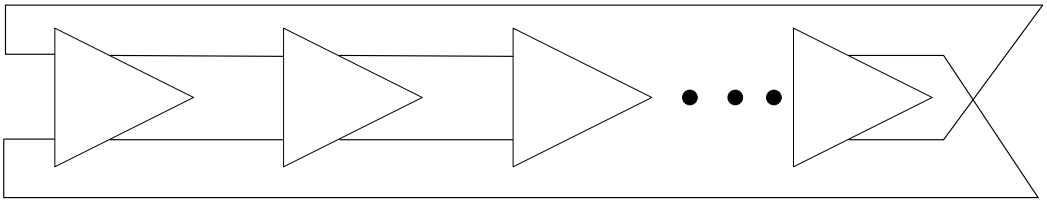
3.2.3 Proposed CML voltage-controlled oscillator

A differential CML-based VCO is proposed as a hybrid model of the previously mentioned designs. This structure is able to mitigate the SEE effectively and additionally to provide a relatively wide tuning range and low noise sensitivity. The basic CML oscillator [19]-[20] is formed by differential buffer (delay) cells connected in series as shown in |ure 3.3(a), and the CML buffer cell is commonly designed as shown in Figure 3.3(b). The delay of the buffer cell in a CML oscillator is determine using Equation 3.5:

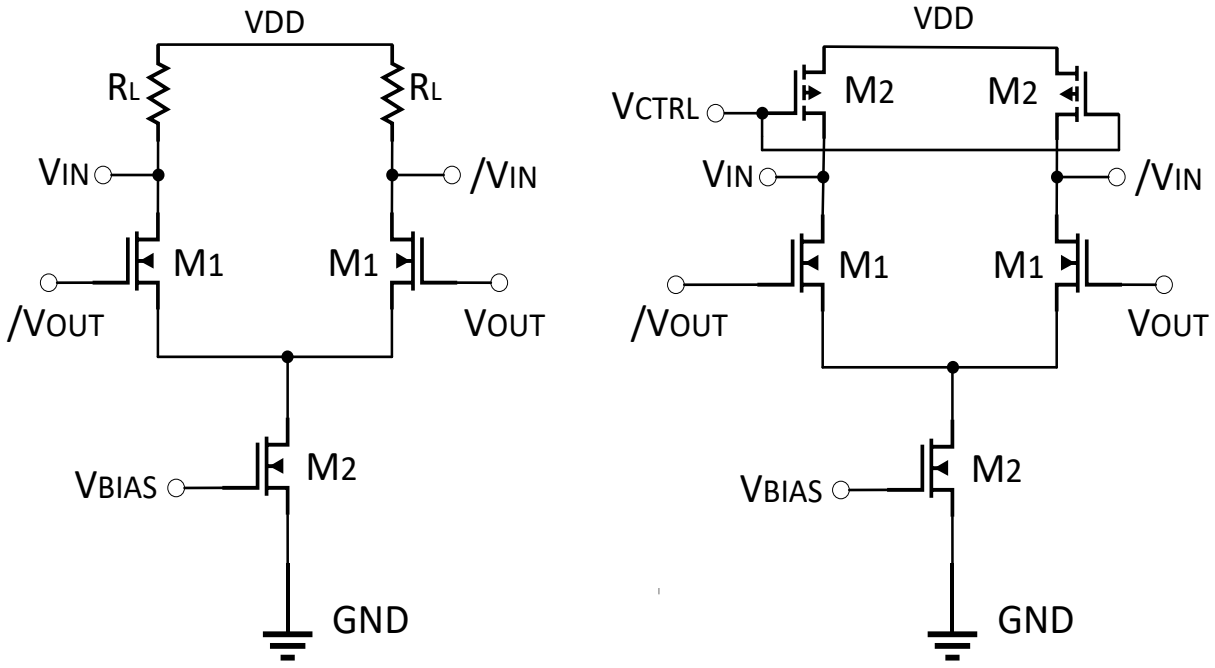
$$\tau=\frac{C_pR_L}{1+g_{ds}R_L} \tag{3.5}$$

In this Equation, C_p is the parasitic capacitance in the output node, R_L is the load resistance, and g_{ds} is the drain to source transconductance of the NMOS transistors. The oscillation frequency will be defined from the delay of an even number of buffer cells connected in series, and can be obtained as follows:

$$f_{osc}=\frac{1}{2N\tau}=\frac{1+g_{ds}R_L}{2NC_pR_L} \tag{3.6}$$



(a)



(b) (c)

Figure 3.3 (a) CML-based oscillator block diagram (b) CML buffer stage with resistive load (c) CML VCO buffer stage with PMOS load

From Equation 3.6, the oscillation frequency is mostly dependent on the total output capacitance and the load resistance. In order to make this oscillator tunable, a variable load resistor

can be used employing PMOS transistors operating in the triode region as shown in Figure 3(c), but this approach will increase the SEE sensitivity considerably.

An alternative to obtain a tunable oscillator and alleviate the SEE sensitivity is shown in Figure 3.4. In this approach, the parasitic capacitance is modified by adding two parallel varactor capacitors C_{VAR} to tune the frequency, and two parallel load C_L capacitors to compensate the frequency, considering these changes, the time delay of the buffer cell is:

$$\tau = \frac{(C_p + C_{VAR} + C_L)R_L}{1 + g_{ds}R_L} \tag{3.7}$$

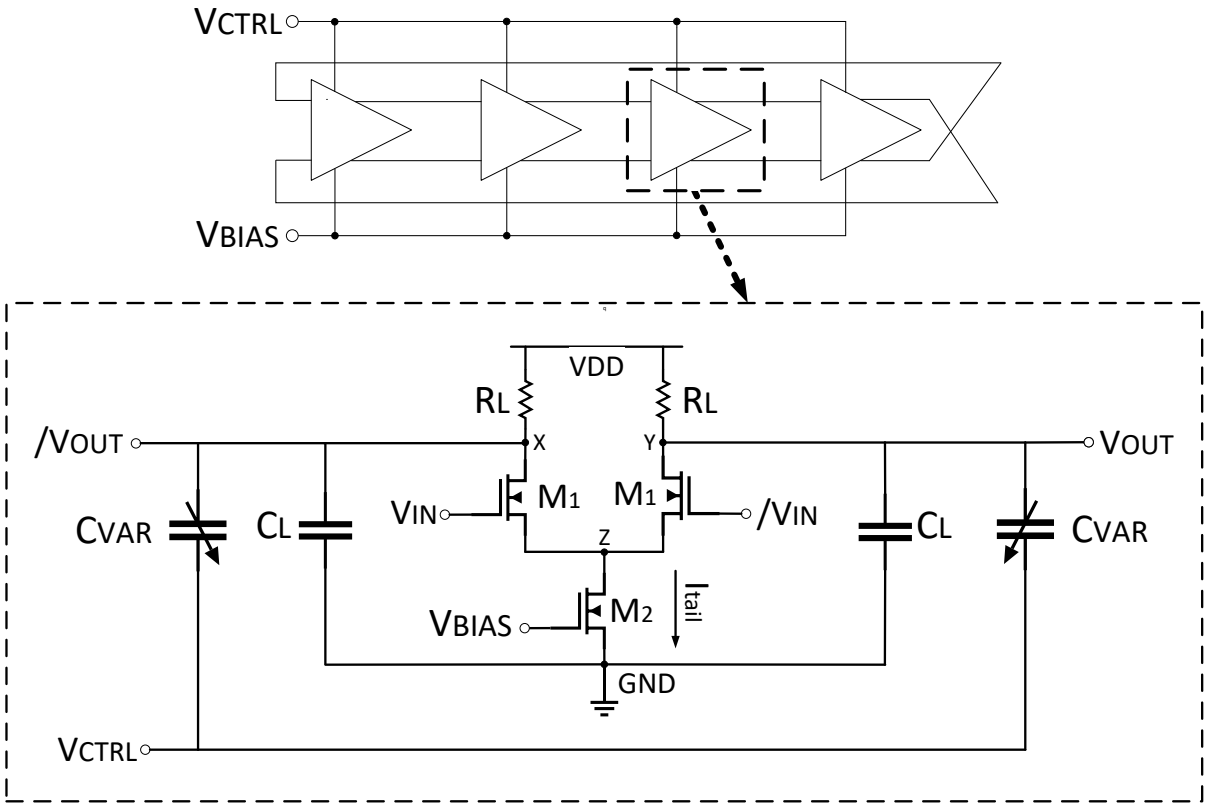


Figure 3.4 proposed CML VCO bloc diagram and CML delay stage schematic

The time delay of the buffer cell, and hence, the oscillation frequency can be regulated by using a variable control voltage that is applied to the varactor capacitors. As can be seen in Equation 3.7, the oscillation frequency of this VCO is defined mostly from passive components that have low SEE sensitivity. In contrast, the transistor transconductance g_{ds} may be affected by the tail transistor, which is sensitive to SEEs, but this weakness may be effectively mitigated since the value of g_{ds} is much smaller than the load resistor and capacitor value. The output swing of each

buffer stage will be defined as (I_{tail}*R_L).

3.3 Simulation Result Analysis

In order to compare electrical performance, an LC-tank VCO, a current-starved VCO and CML VCO were built in 65nm CMOS bulk technology, and simulations were carried out to determine the actual tuning range of the three oscillators. From the results shown in Figures 3.5, 3.6, and 3.7, it can be seen that the LC-tank structure has a limited tuning range from 1.08 to 2.1GHz.

The current-starved and CML VCO structures present similar tuning ranges, which are from 0.3 to 2.5GHz and from 0.8 to 3.2GHz, respectively. In terms of phase noise, a central frequency close to 1GHz was chosen to find the noise performance shown in Figures 3.8, 3.9, and 3.10. Results at 1MHz offset revealed the current-starved high sensitivity to noise, with a value equal to -67.52dBc/Hz, while the LC-tank and CML VCOs exhibited good noise performance with values of -116.8dBc/Hz and -92.15dBc/Hz, respectively.

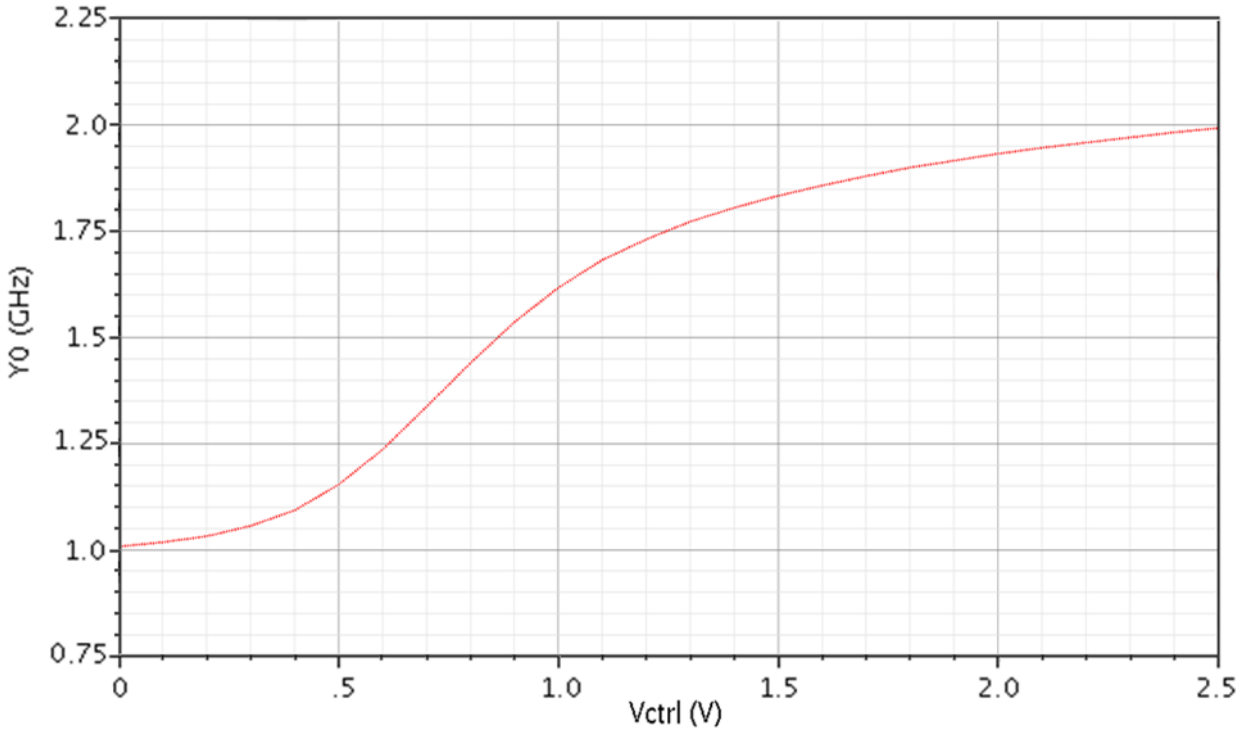


Figure 3.5 Output frequency vs control voltage for the LC-tank VCO.

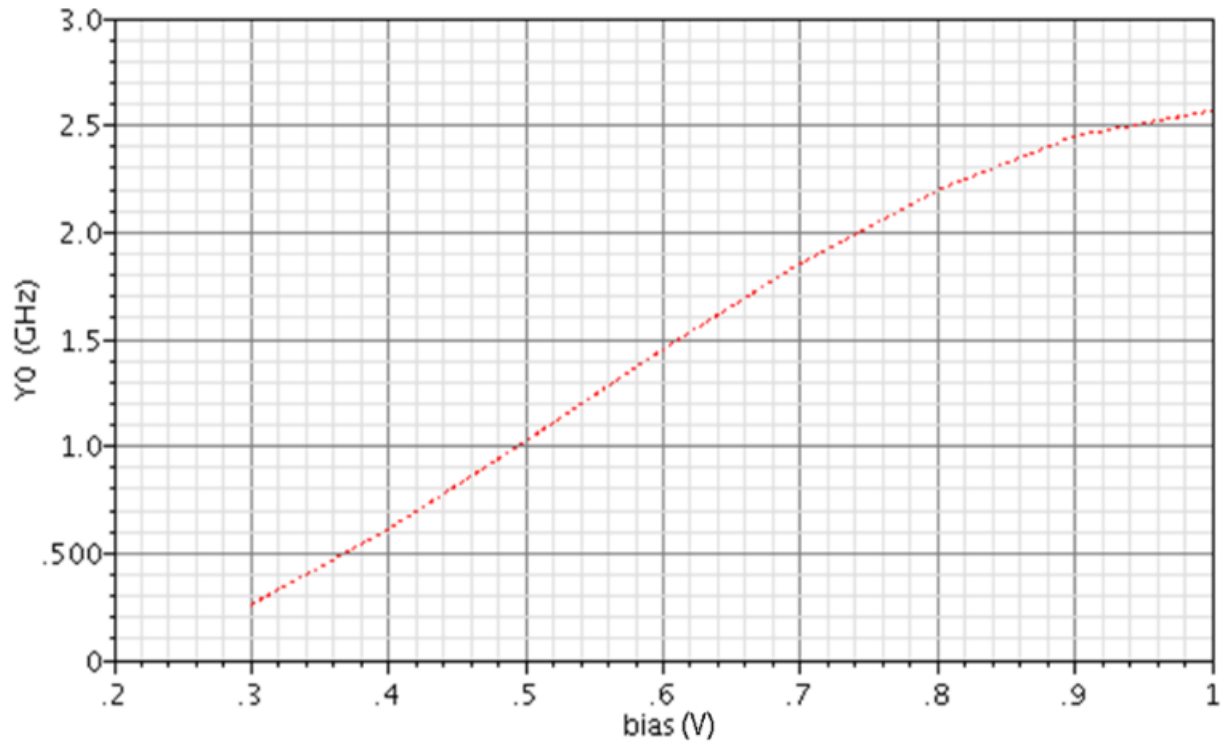


Figure 3.6 Output frequency vs control voltage for the current-starved ring VCO.

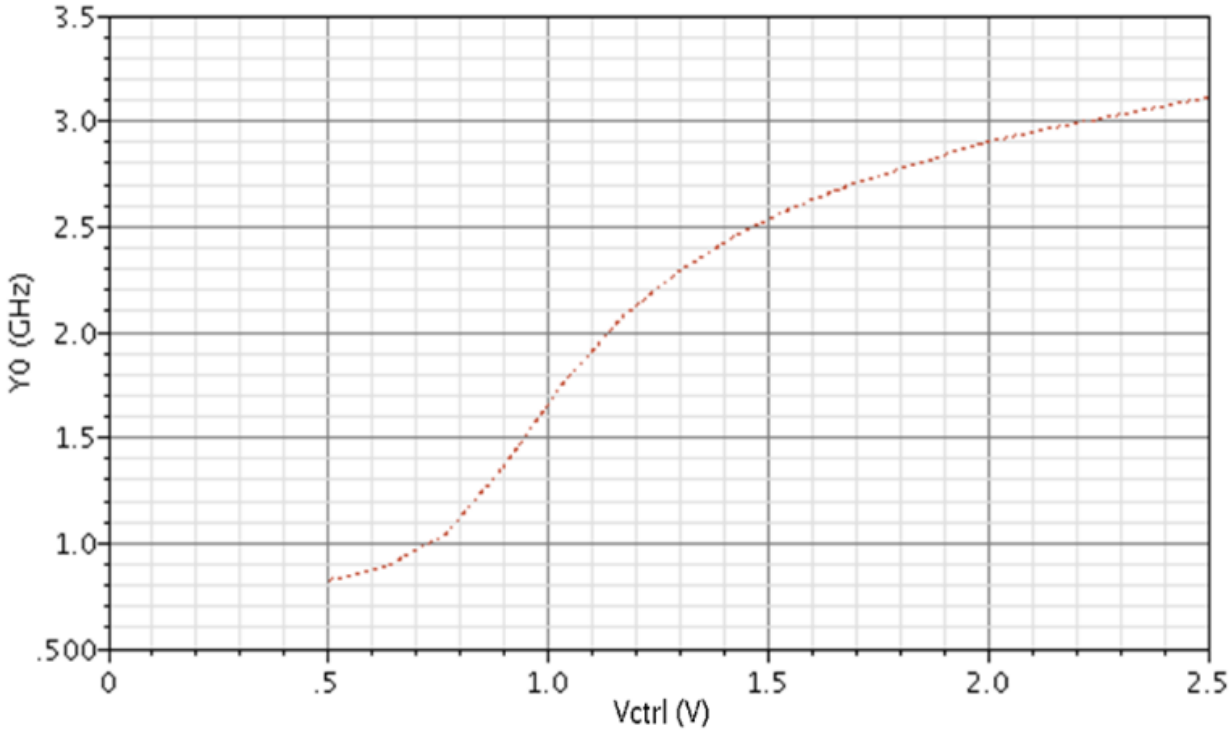


Figure 3.7 Output frequency vs control voltage for the proposed CML VCO.

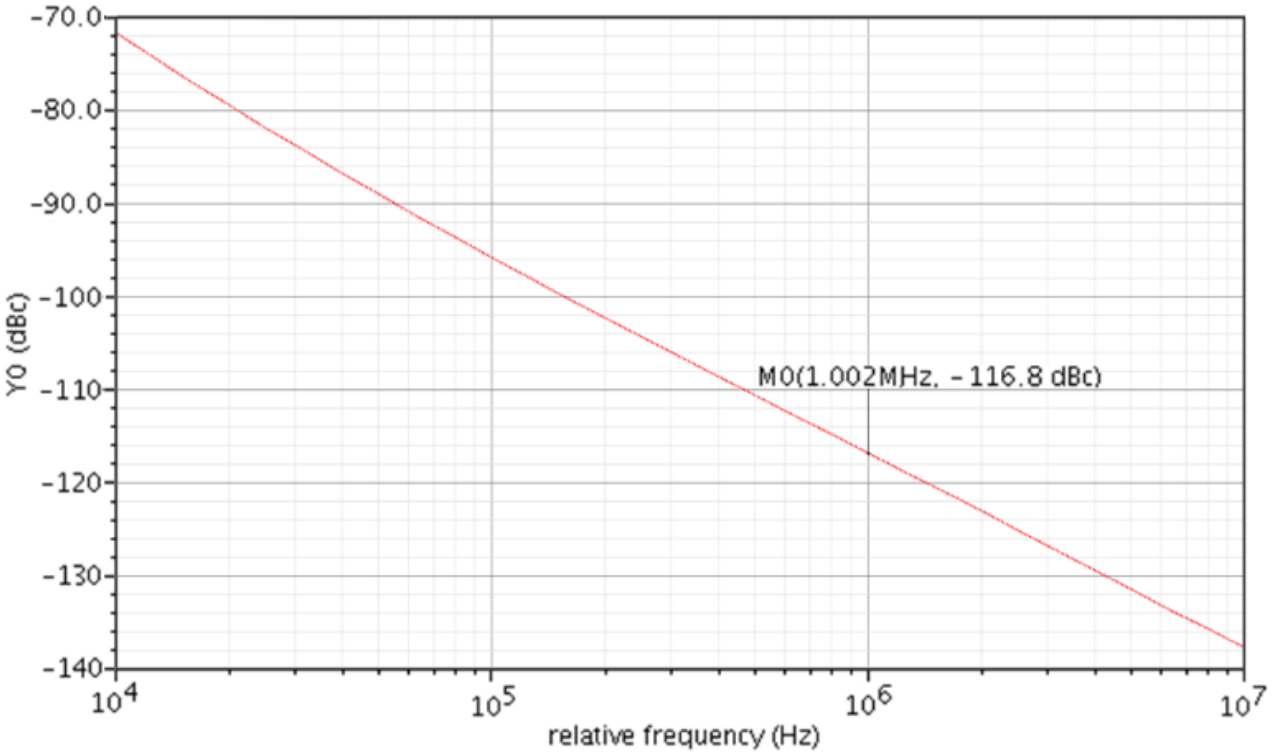


Figure 3.8 Output frequency vs control voltage for the LC-tank VCO

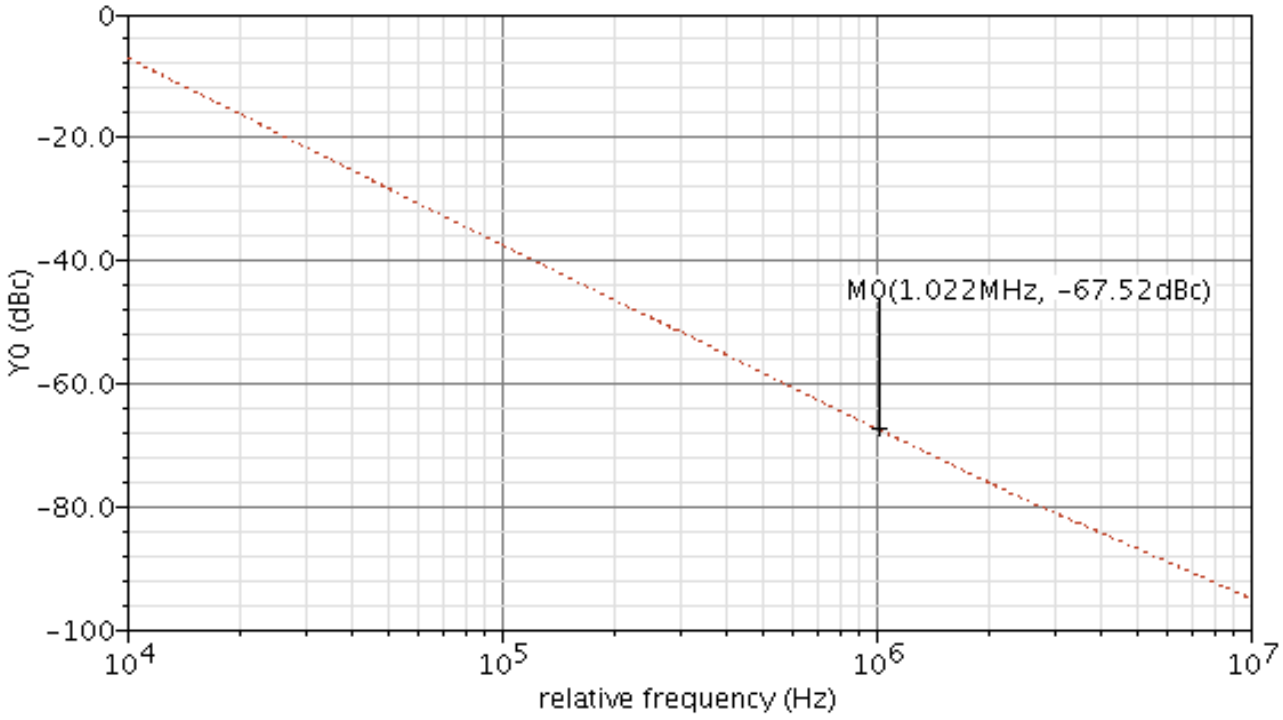


Figure 3.9 Output frequency vs control voltage for the current-starved ring VCO.

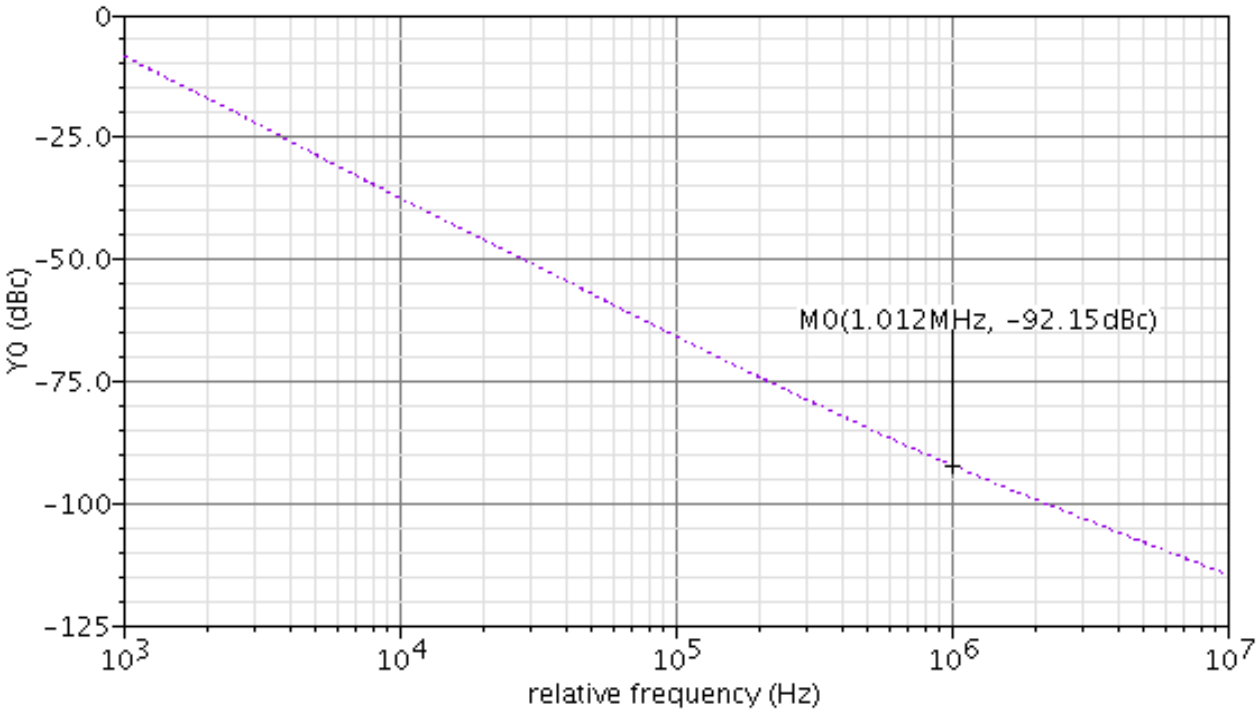
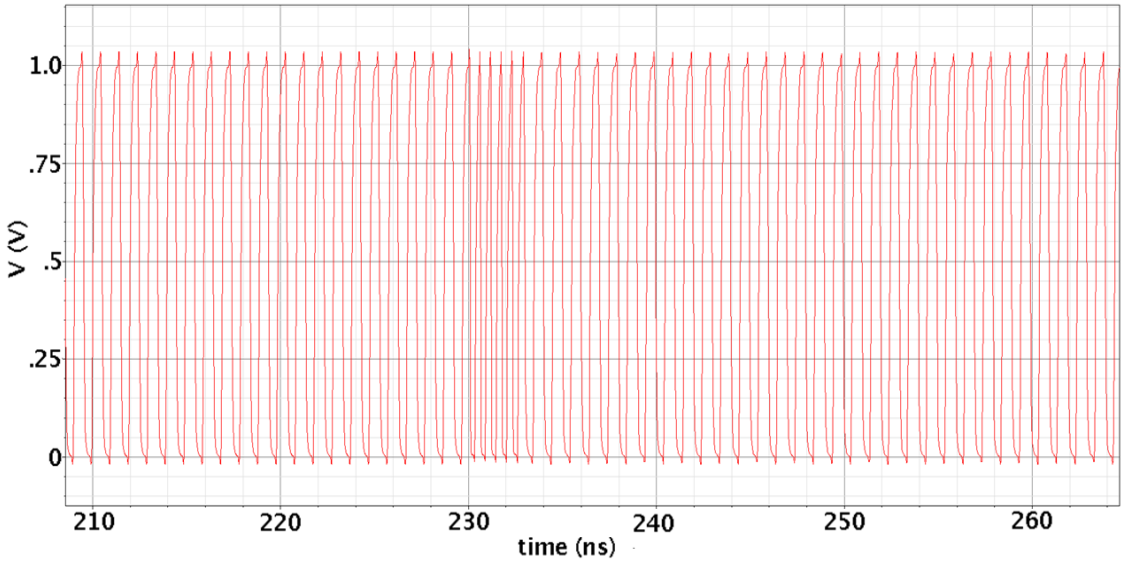


Figure 3.10 Output frequency vs control voltage for the proposed CML VCO.

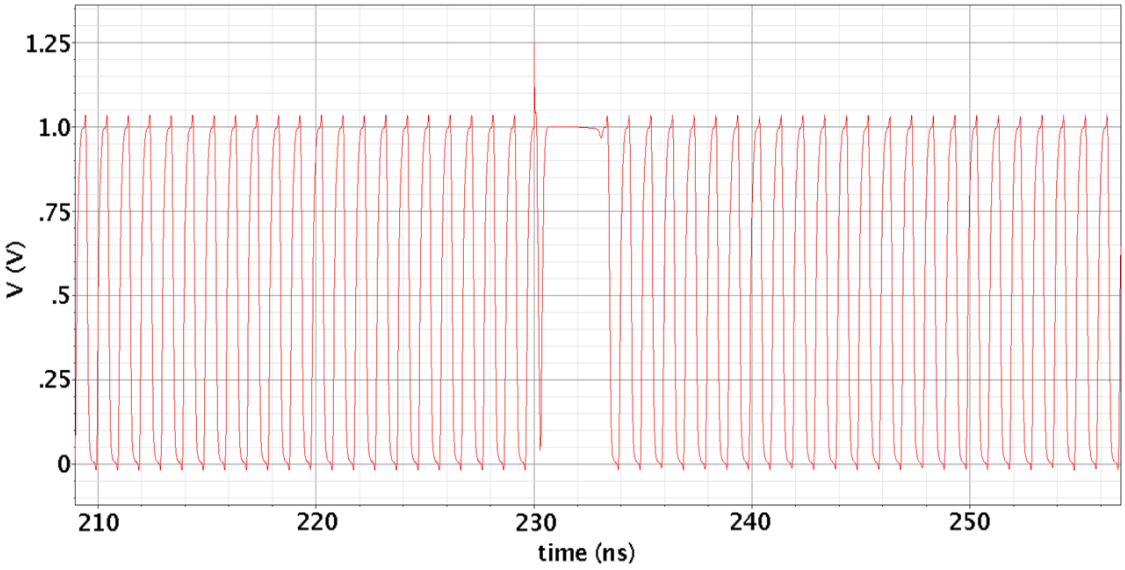
For the SEEs study, circuit level analysis and simulations were performed by injecting a double-exponential current pulse into different sensitive nodes of the previously described VCOs as defined in previous works. The employed pulse was setup with 10ps rising time, 1ns duration, and a peak magnitude ranging from 1µA to 2.5mA [7],[21].

The SE strike was simulated in the current-starved VCO presented in Figure 3.2. The injected pulse threshold peak amplitude energy for this VCO was found at 100µA. The period before the strike was equal to 1.04ns, when the SE hit the bias stage of this VCO, the bias voltage fluctuated and was propagated through the current mirrors, causing a temporary modulation effect in the output frequency, as shown in Figure 3.11(a). During the SEE the output period was 0.0728ns which represents a 30 % frequency shift.

When the strike occurred in the RO stage, the deposited charge was stored in the output nodes, causing missing pulses as shown in Figure 3.11(b). In both cases the perturbation was removed once the deposited charge was drained off the circuit.



(a)

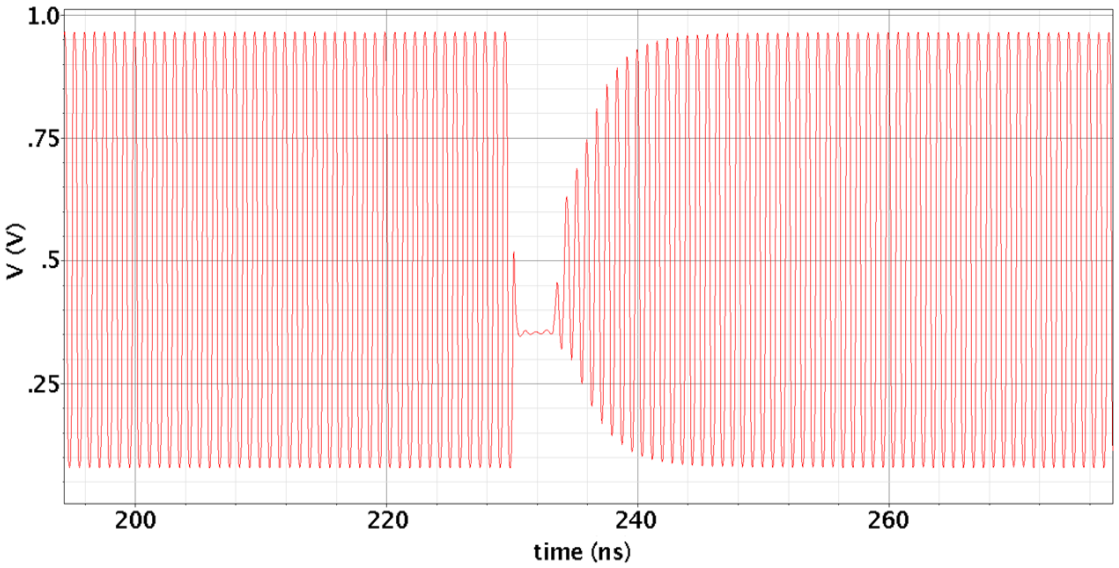


(b)

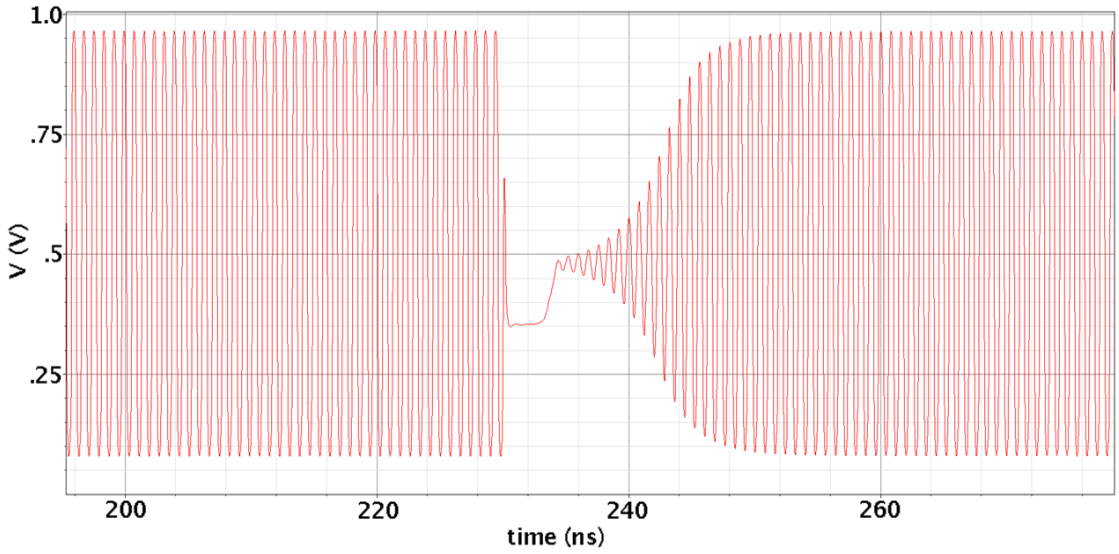
Figure 3.11 Current-starved VCO output signal during a SE at (a) bias stage (b) RO stage. The strike occurs at 230ns and stops at 233ns. with 100µA peak amplitude.

The next SEE simulations were carried out in the LC-tank VCO shown in Figure 3.11. For this circuit, the injected pulse has a threshold peak magnitude at 2.5mA. When the charge was injected into the output nodes, both frequency and amplitude were modulated as shown in Figure 3.12(a). A similar effect occurred when the SEE hit the bias transistor. However, as shown in Figure

3.12(b), the disturbance in the output amplitude is larger and a longer recovering time was needed for the LC-tank to recover back its normal oscillation. The output nodes were shown to be less susceptible to the SEEs. This response is due to the extra transconductance provided by the cross-coupled load PMOS pair.

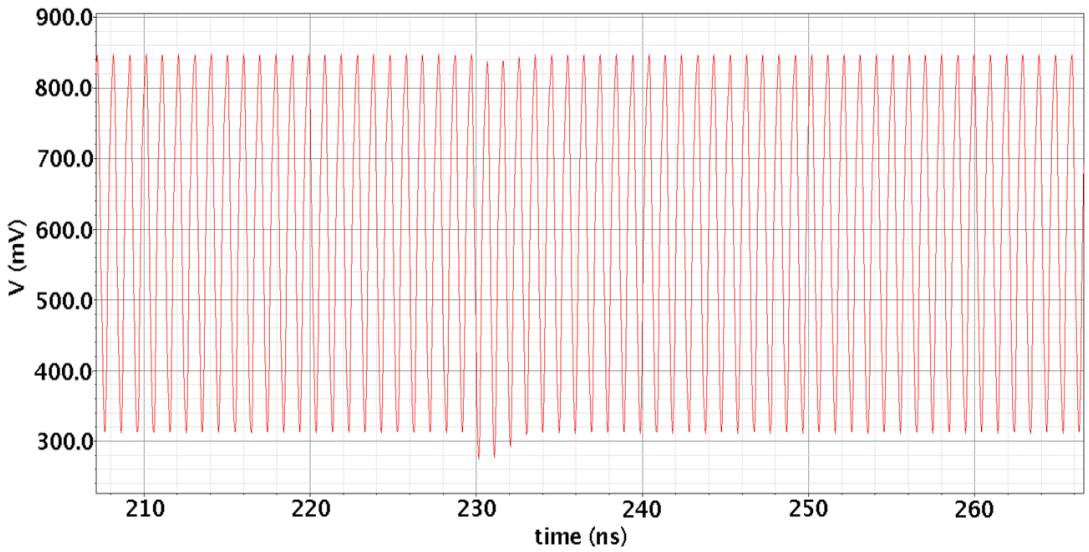


(a)

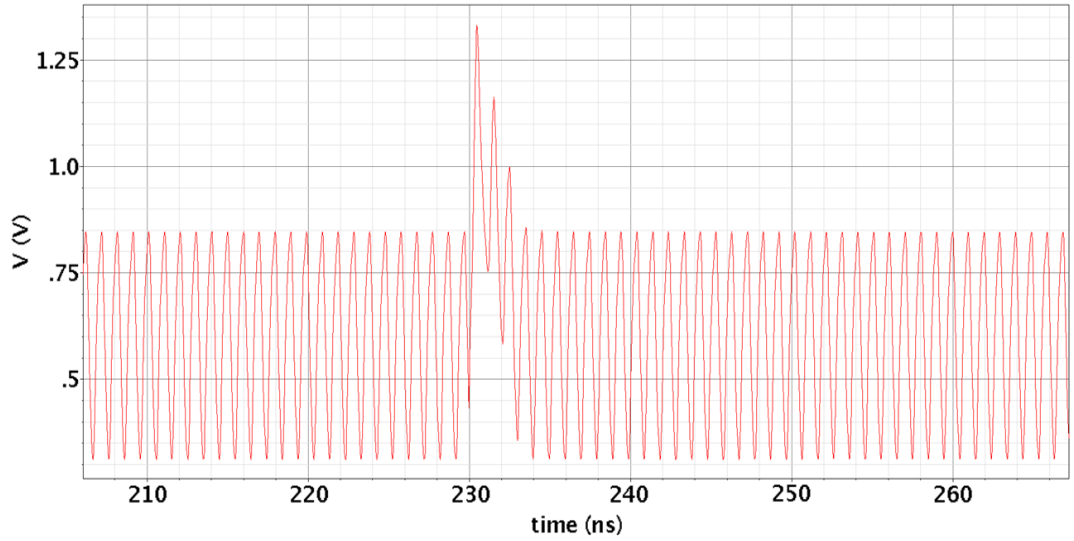


(b)

Figure 3.12 LC-tank VCO output signal during a SE at (a) output node X (b) bias transistor node Z. The strike occurs at 230ns and stops at 233ns, with 2.5mA peak amplitude.



(a)



(b)

Figure 3.13 CMLVCO output signal during a SE at (a) output node X (b) bias node Z. The strike occurs at 230ns and stops at 233ns, with 1.5mA peak amplitude

Finally, SEE simulations were performed in the proposed CML VCO. The threshold peak amplitude for the injected pulse was found at 1.5mA for this design. When the current pulse was injected into the output node X, the period and frequency changes were only around 0.4% from the normal oscillation condition. In terms of amplitude, there was also a temporary disturbance of the output signal, as shown in Figure 3.13(a). A similar effect occurred in terms of phase shift when

the SEE was applied to the bias transistor, but in contrast, when the charge was deposited on the node Z the amplitude disturbance was larger as shown in Figure 3.13(b). This effect shows the bias transistor is the most sensitive node in this design. Since both the amplitude and frequency perturbations caused by the SEE are limited, when this VCO is implemented within a PLL system, the induced transient distortion can be effectively mitigated by the close loop system.

3.4 Experimental Results Analysis

3.4.1 Circuit setup

The three oscillators were tested using a Spectrum Analyzer (Agilent N9030A PXA) to verify the simulated electrical performance. The phase noise experimental results shown in Figures 3.14, 3.15, and 3.16 are consistent with the simulated data. The results suggest that the proposed CML VCO presents low noise sensitivity, showing a similar noise response to the LC-tank VCO. Additionally, Figure 3.17 shows a zoomed layout view with the actual design dimensions of each VCO. From the marked design areas it can be seen that the CML VCO occupies an area smaller than the LC-tank VCO. For the SEE experimental study, the three oscillators were set to oscillate at a frequency around 1GHz.

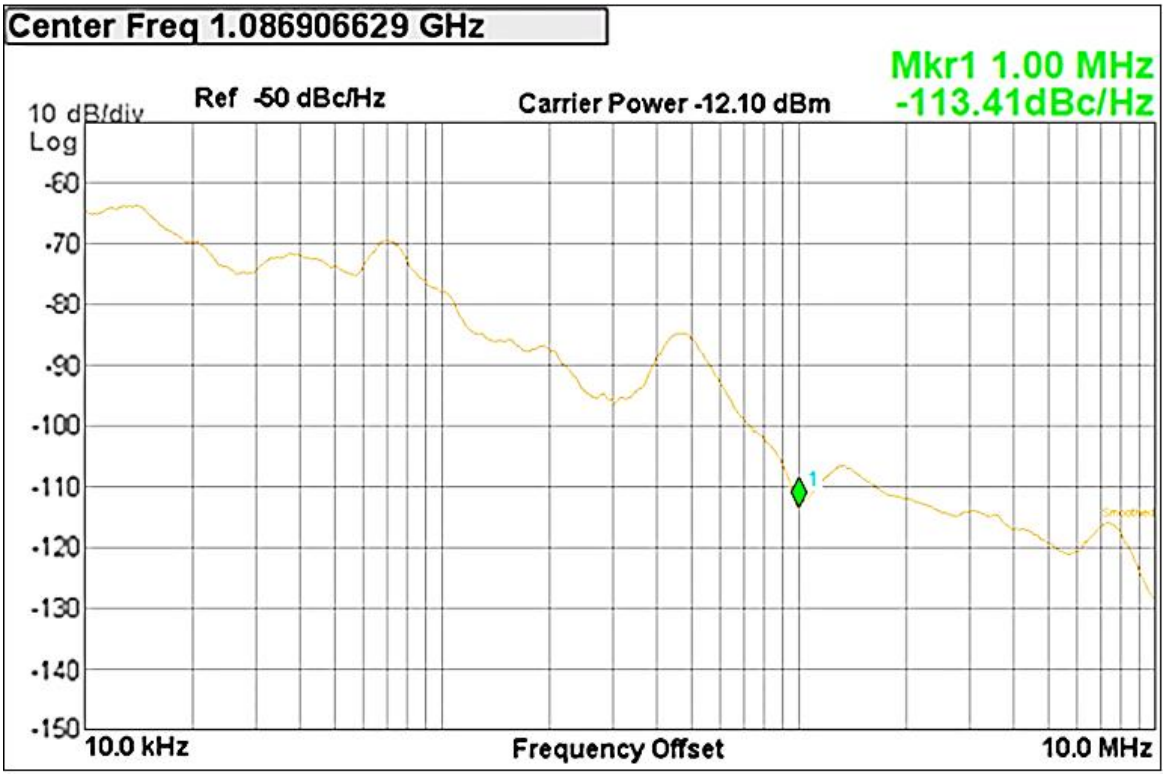


Figure 3.14 Phase noise plot of the LC-tank VCO, marker placed at 1MHz offset.

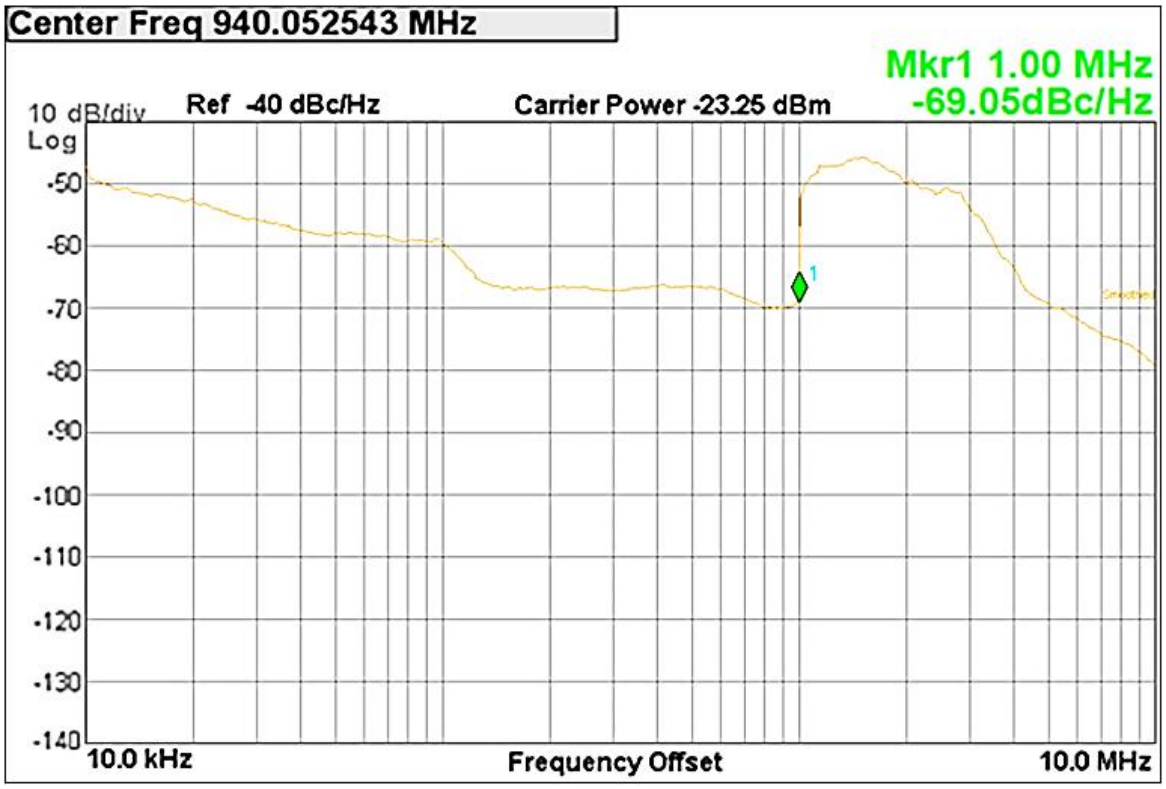


Figure 3.15 Phase noise plot of the current-starved ring VCO, marker placed at 1MHz offset.

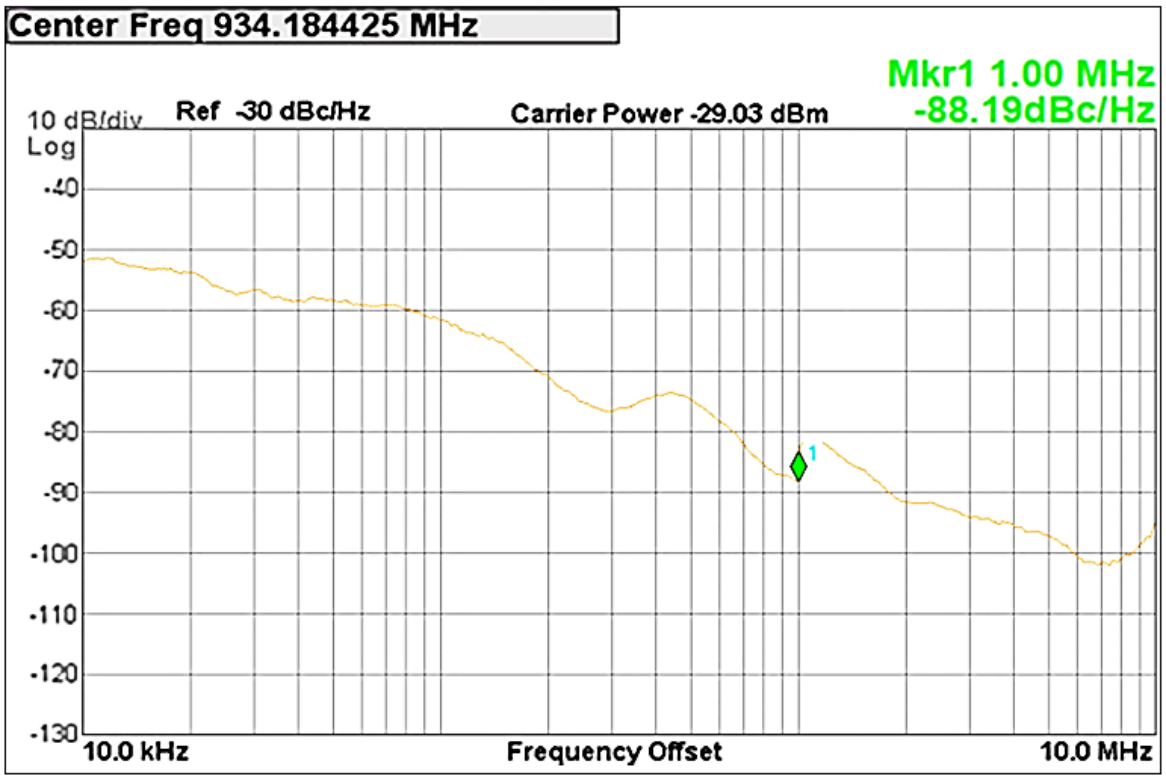


Figure 3.16 Phase noise plot of the CML VCO, marker placed at 1MHz offset.

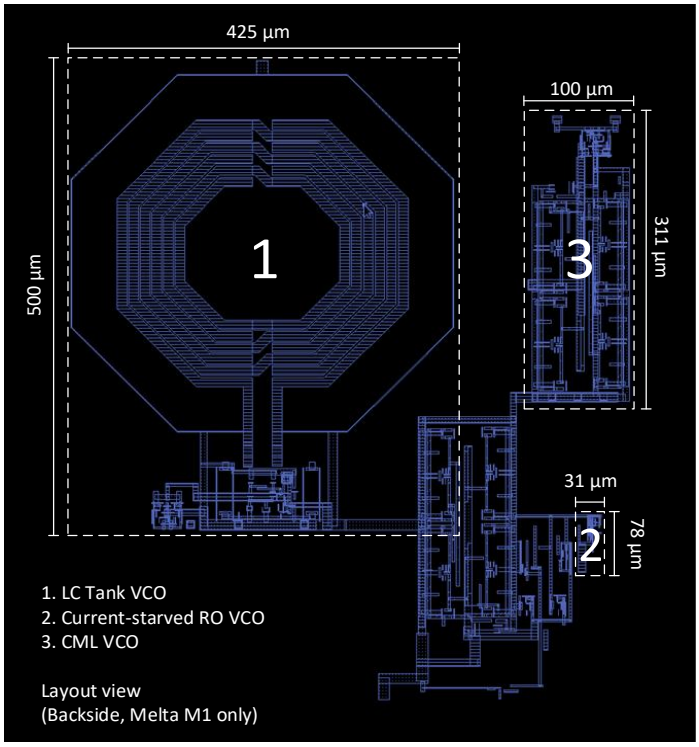


Figure 3.17 Partial layout of the DUT showing the size of the designed VCOs.

3.4.2 Laser setup

A pulsed laser was chosen as an effective tool to investigate SEEs. It is able to provide better spatial and temporal control abilities in a SEE testing in comparison to the traditional proton and heavy-ion testing [21]. In this study, a two-photon absorption (TPA) laser experiment was used. The laser system is located at the Saskatchewan Structural Sciences Centre (SSSC), which contains a seeding laser (a Verdi-pumped ultrafast mode-locked Vitesse laser, with Ti:Sapphire as a gain medium, fixed 80MHz repetition rate and 800nm wavelength); a pump laser (an Nd: Vanadate continuous Verdi laser , with 532nm wavelength and up to 18W of power); an amplifier (a RegA 9000) to combine the seeding laser and pump laser together, with a tunable repetition from 10KHz to 300KHz and fixed 800nm wavelength. Eventually, the output pulsed-laser from RegA 9000 has the power around 50mW, repetition of 10 KHz, wavelength of 800 nm, and pulse duration of less than 160fs. Subsequently, the wavelength of the pulsed laser will be extended up to 1250nm by another device, the OPA9800. All these devices came from Coherent, Inc. The basis of the laser scanning system is a ThorLabs MPM200-SGP microscope. The Coherent laser source, producing pulsed laser beams with 1250nm wavelength and 10kHz repetition rate was used in the experiments.

The device under test (DUT) was the 65nm SoC device in a flip-chip package. The silicon die was thinned from the backside and mirror-polished at the substrate to facilitate the laser testing. The TPA laser experiments focused on injecting laser pulses into the DUT from the backside so that the laser pulses could avoid the metal layers in the top of the package.The laser energy was injected across the areas with a step size of 5.4µm.

3.4.3 Laser scan results analysis

The output frequency spectrum of the three blocks under test was monitored by a Spectrum Analyzer (Agilent N9030A PXA). During the laser testing, rapid frequency shift, and temporary spurs in the frequency domain were observed.

These two factors were used to define a failure criterion in this study, in such a way that an event was considered to be a SEE whenever the frequency shift was larger than 1% of the center frequency and/or the level of the spur(s) was less than 30dB below the carrier power. A die photograph of the scanned areas is shown in Figure 3.18.

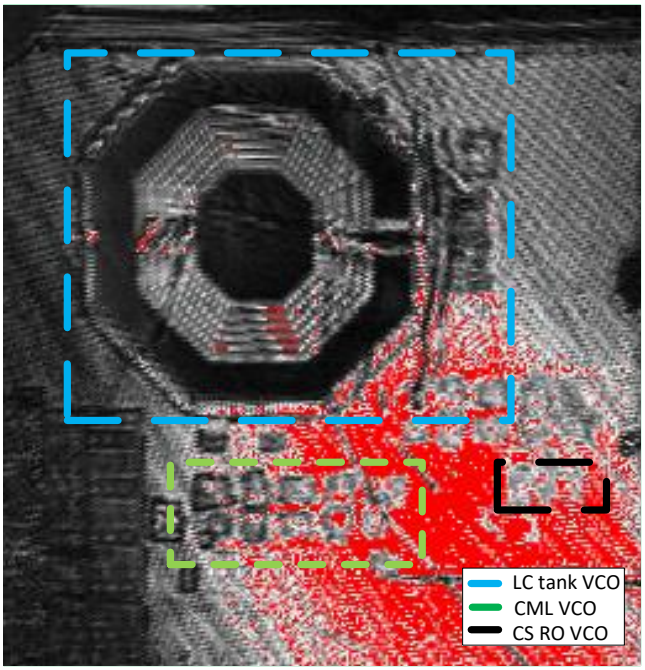
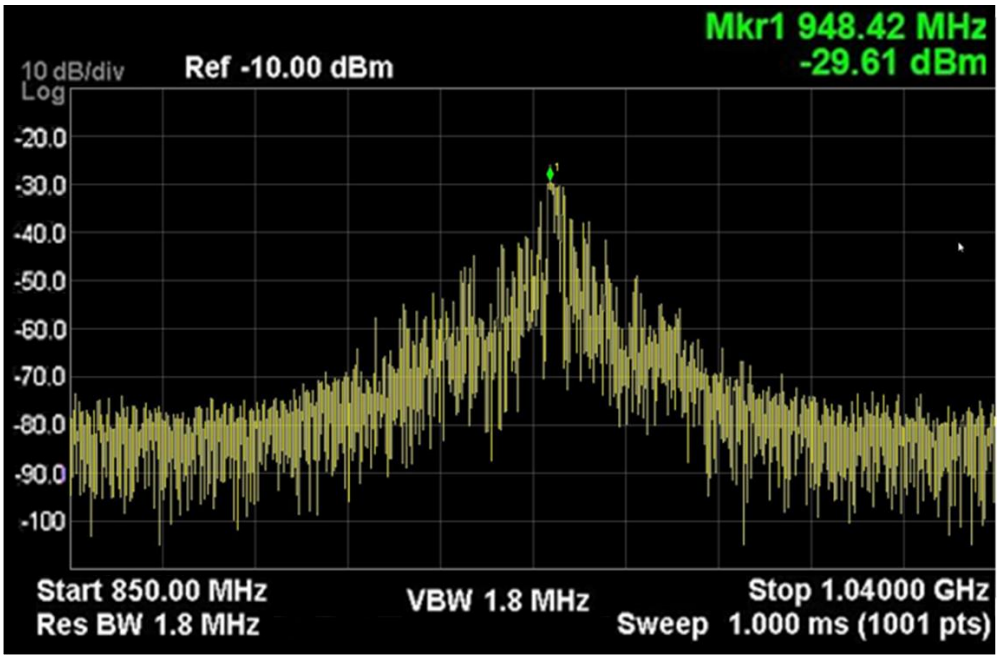


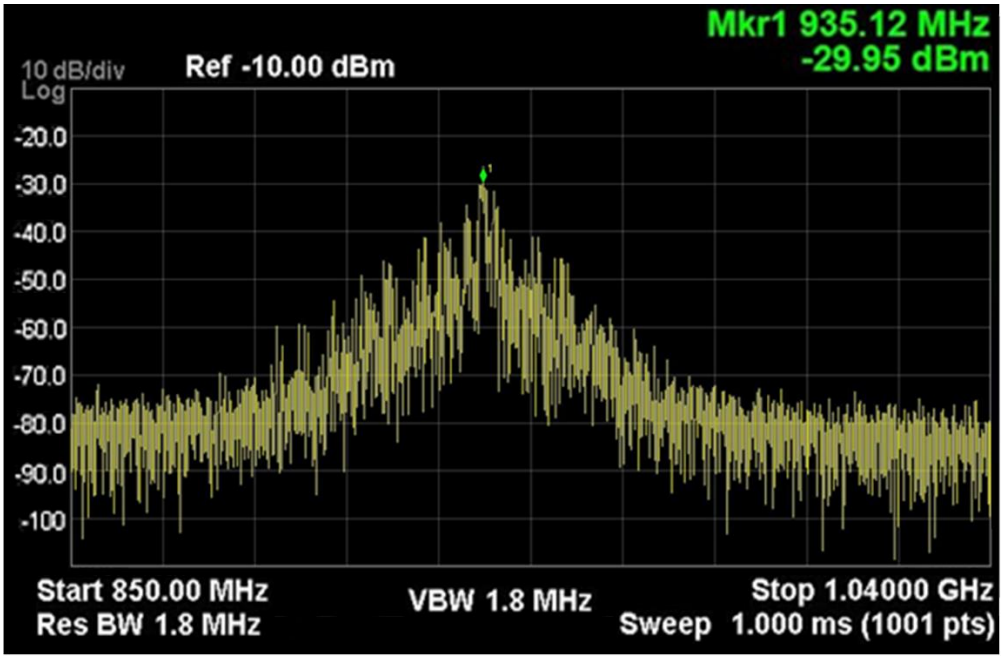
Figure 3.18 Die photograph of the scanned areas.

The current-starved RO-VCO was scanned first with the laser beam since this is theoretically the most sensitive design. The beam energy was increased in steps of 500 pJ up to 2.5nJ which was identified as the threshold energy of this VCO. Figure 3.19(a) is the spectrum of the current-starved

RO-VCO under normal oscillation operation. When a laser beam of 2.5nJ was applied, the output frequency was first shifted down and then recovered back quickly Figure 3.19(b) shows the spectrum before the normal oscillation has recovered.



(a)



(b)

Figure 3.19 Current-starved RO-VCO spectra: (a) no laser hit, (b) phase shift with SEE at 2.5nJ

The experiments were repeated on the LC-tank VCO. Figure 3.20 shows the spectrum of the LC-tank VCO when no laser energy is applied. As can be observed in Figure 3.21(a) when a laser beam at 2.5nJ is injected the output signal has no phase shift, which matches the simulation results. In order to verify the SEE response of the LC-tank VCO, the applied laser energy was increased to 3nJ. As shown in Figure 3.21(b), the output expected remain stable showing no phase shift.

The last laser experiment was performed on the CML VCO. The normal oscillation operation of the proposed VCO is shown in Figure 3.22(a). When a laser beam of 2.5nJ was injected, parasitic spurs around the central frequency were generated as shown in Figure 3.22(b); nonetheless the circuit kept oscillating with no significant phase shift. Figure 3.23 shows that when a higher beam of energy of 3nJ was injected, the spurious phase noise increased but the oscillation remained normal without showing a significant phase shift.

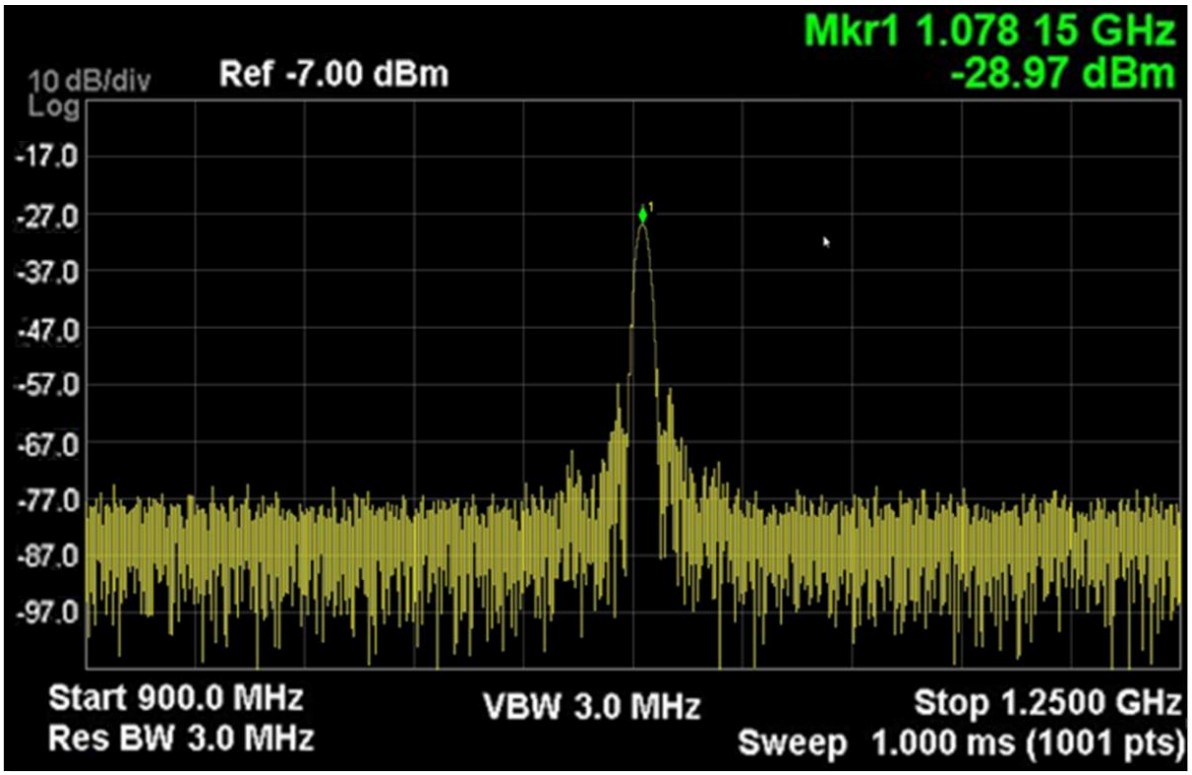
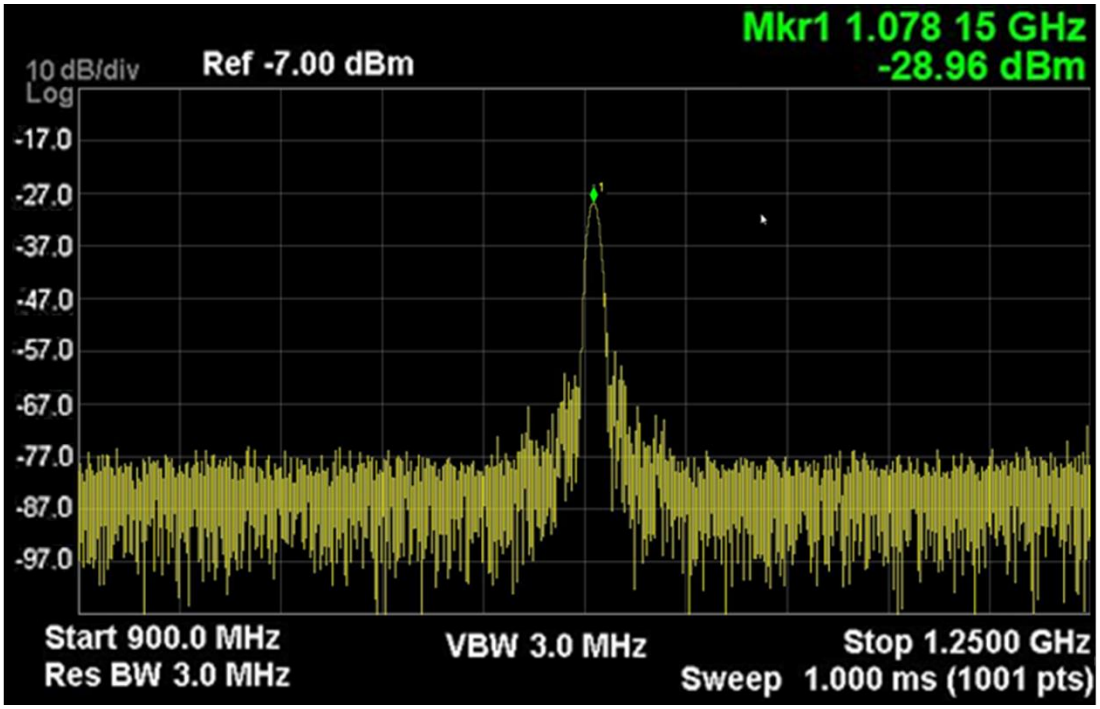
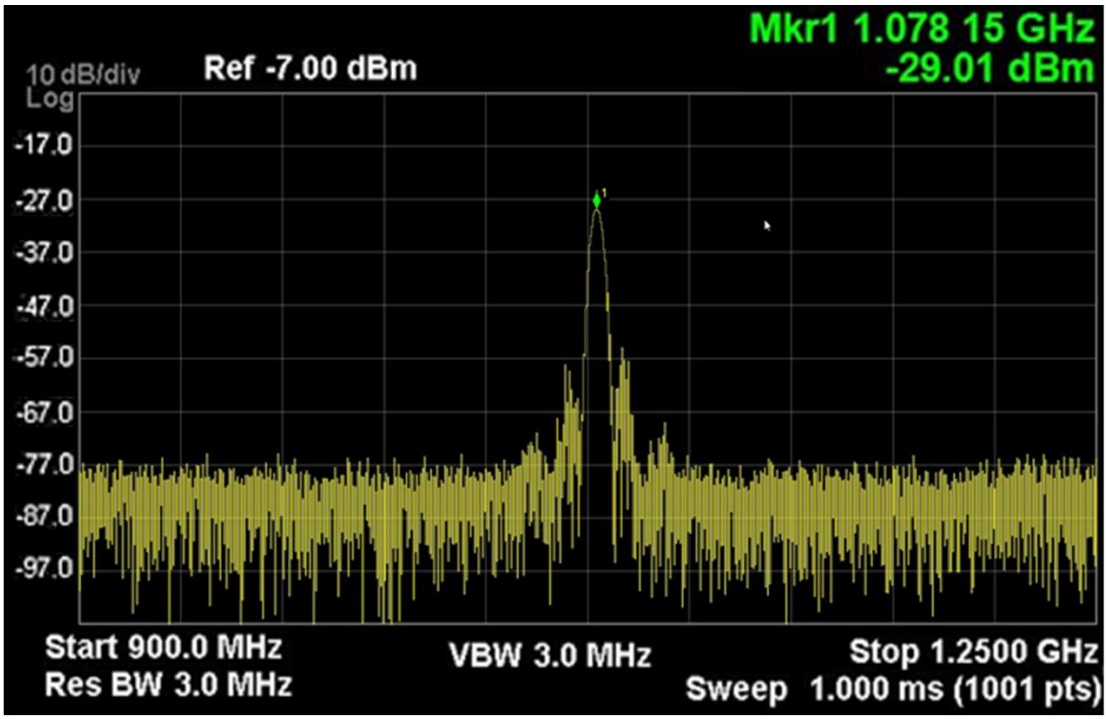


Figure 3.20 LC-tank VCO spectra: no laser hit.

According to the test results the CML VCO presents similarities to the LC-tank VCO in terms of sensitivity to noise and to a SEE. Both oscillators present low phase noise when operating under normal conditions and very high SEE tolerance.

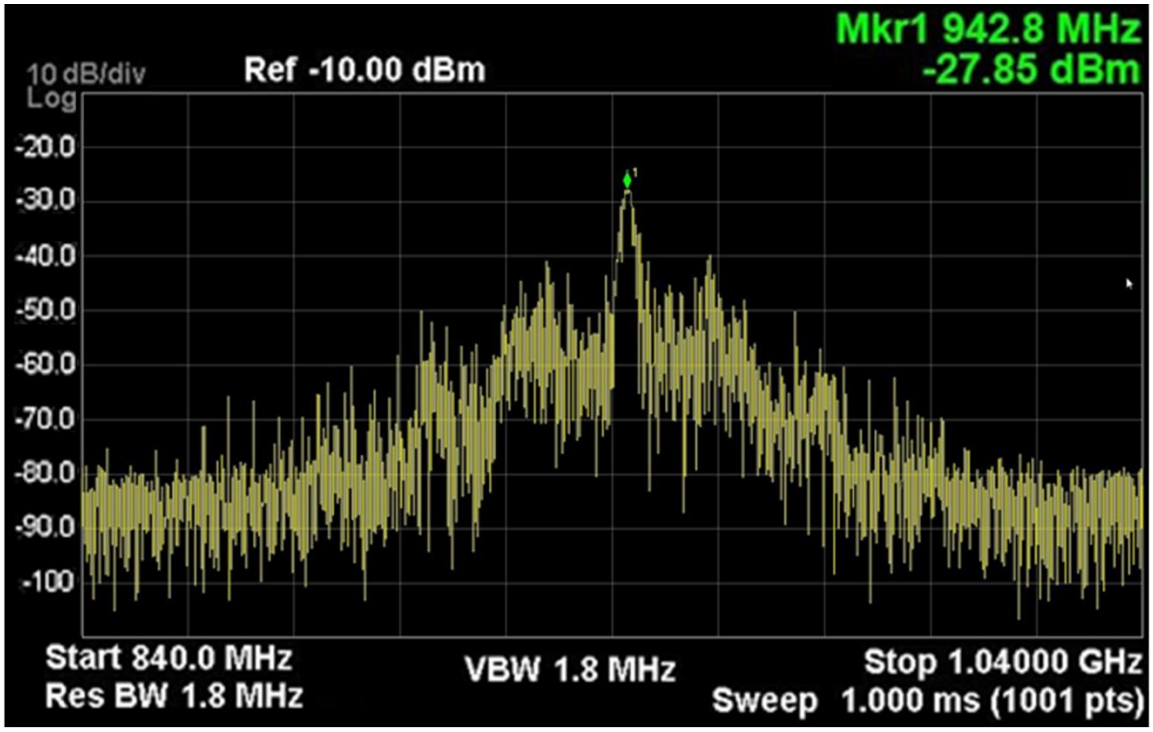


(b)

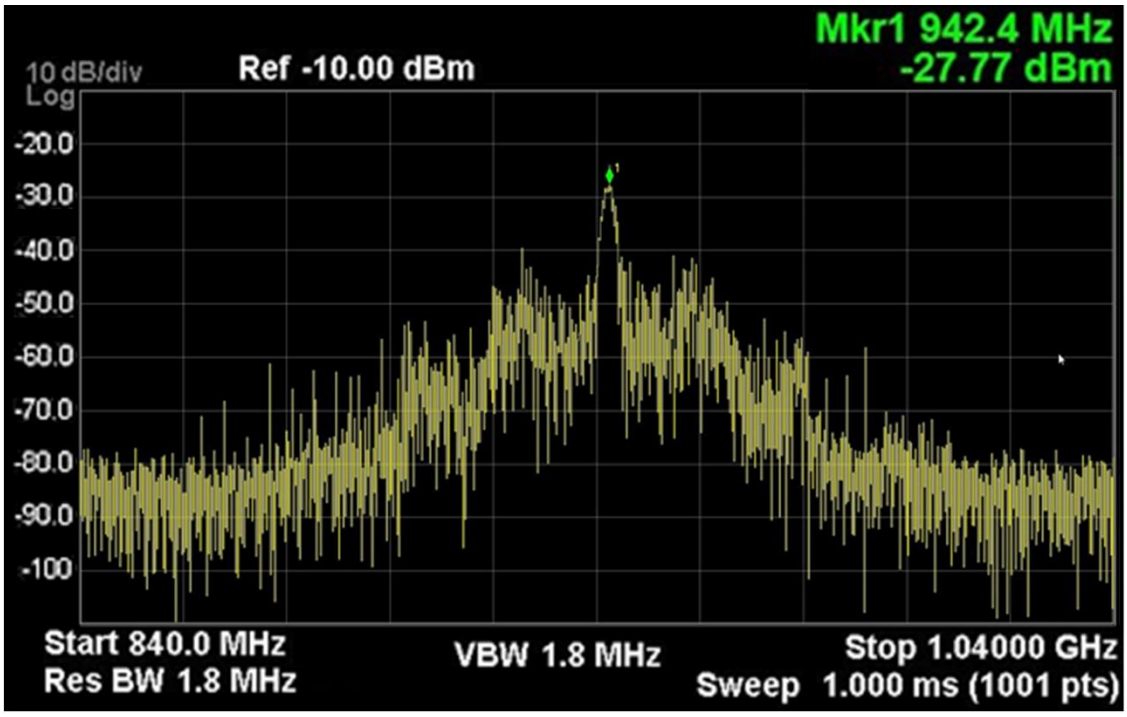


(c)

Figure 3.21 LC-tank VCO spectra: (a) with SEE at 2.5nJ (b) with SEE at 3nJ.



(a)



(b)

Figure 3.22 CML VCO spectra: (a) no laser hit, (b) with SEE at 2.5nJ.

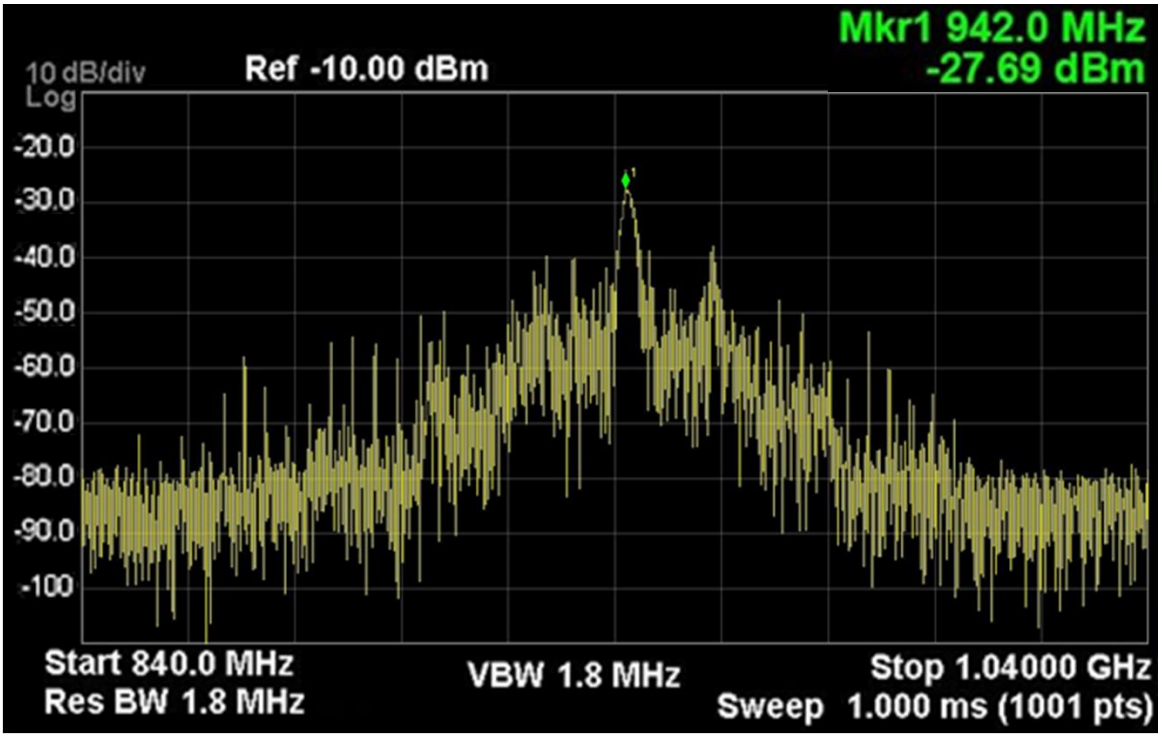


Figure 3.23 CML VCO spectra: with SEE at 3nJ.

In the case of the CML VCO, its low sensitivity was achieved due to the presence of the coupling capacitors CL and varactors CVAR, which were directly connected to the output of each buffer stage, and which helped to release the injected beam energy directly to ground, speeding up the recovery time. When a SEE strikes the CML VCO, the only drawback produced is the rise in the spurious noise. However, this factor does not affect the normal operation of this design since the duration of this side effect is not significant. Tables 3-1 and 3-2 contains a summary of all the obtained results of this study.

Table 3.1 Comparison of electrical performance and design area of the different VCO designs

VCO Design	Tuning range	Phase noise	Design Area
RO-VCO	1.08 - 2.1GHz	-116.8dBc/Hz	78x31µm
LC-tank	0.3 - 2.5GHz	-67.52dBc/Hz	452x500µm
CML-VCO	0.8 - 3.2GHz	-92.15-dBc/Hz	100x311µm

Table 3.2 TPA laser experiment conducted in the 65nm testchip

Beam energy	**Experimental Results**		
	RO-VCO	**LC-tank**	**CML-VCO**
2.5 nJ	• phase shift (1.4%) • No spurious noise • Amplitude attenuation (0.34dBm)	• No phase shifts • No spurious noise • Amplitude attenuation (0.01dBm)	• phase shift (0.04%) • No spurious noise • Amplitude rise (0.08dBm)
3 nJ	-	• No phase shifts • No spurious noise • Amplitude attenuation (0.04dBm)	• phase shift (1.4%) • Temporary spurious noise • Amplitude rise (0.16dBm)

3.5 Conclusion

A 65nm bulk CMOS CML-based RO-VCO was designed and analyzed in order to provide a high-performance and radiation-tolerant structure. From the simulated and experimental results, it can be concluded that the proposed CML VCO shares the advantages of the current-starved RO VCO and the LC-tank VCO and additionally overcomes their limitations by effectively mitigating the SEE effects. The proposed design shows a radiation tolerance similar to the LC-tank VCO without affecting the tuning range or increasing the phase noise. This behavior proved the CML VCO to be a good reliable option for high-performance PLLs, which does not require a large design area. The SEE experiments evidenced an increase in spurious noise around the central frequency of the CML VCO. However, this side effect did not affect the circuit performance since the load and variable capacitors employed in the buffer stages helped to speed up the recovery time of the circuit in case of a SE. As was expected, the current-starved RO-VCO was demonstrated to be the most sensitive structure to SEEs, while the limited tuning range of the LC-tank VCO was also proved.

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4. A RADIATION-TOLERANT CML VOLTAGE-CONTROLLED OSCILLATOR IN 28NM CMOS FDSOI

Published as:

J. Cardenas, A. Khan, L. Chen, Z. Zhang, and M. Khan, "A Radiation-tolerant CML voltage-controlled oscillator in 28nm CMOS FDSOI," *2019 IEEE Canadian Conference of Electrical and Computer Engineering (CCECE)*, Edmonton, AB, Canada, 2019, pp. 1-4.

In the previous chapter, a CML-based RO-VCO was implemented and fabricated in 65nm bulk technology. The proposed area-efficient design was proven to effectively improve the limited tuning range, high phase noise and high SEE sensitivity shown in common VCO designs, such as RO and LC-tank VCOs. However, power consumption was not a critical factor in this study, due to the short-channel effect presented and leakage currents that are present in bulk technologies. An alternative technology with improved characteristics must be studied for the implementation of analog circuits, paying special attention to radiation-tolerant VCOs.

In this chapter, 28nm FDSOI technology is employed for implementing the previously proposed radiation-tolerant CML VCO. Simulations are carried out to compare the performance and radiation response of the proposed design with a 28nm FDSOI RO-VCO and to demonstrate the improvements obtained by the use of this new technology in contrast with its 65nm counterpart. The benefits of FDSOI technologies applied to analog circuits are reduced power consumption, improved radiation tolerance, and reduced design area without affecting the high performance previously shown in bulk technologies.

Contributions on this manuscript:

- Jaime Cardenas: CML-VCO design, electrical performance and SEE simulations and analysis.
- Abdul Khan: RO VCO design, SEE simulations support
- Li Chen: Advisor for idea developing and paper review
- Zhichao Zhang: Advisor for design, simulation, and analysis
- Muhammad Khan: Advisor for problem solutions

A Radiation-tolerant CML Voltage-controlled Oscillator in 28nm CMOS FDSOI

Jaime Cardenas, Abdul Khan, Li Chen, Zhichao Zhang, and Muhammad Khan

Abstract

Ring oscillators have been one of the main choices for high-frequency electronic devices because they are able to generate a wide tuning range. However, they present a high sensitivity to single event effects in radiation environments. As a hardening technique, an improved ring-oscillator based on current mode logic was developed. In this circuit the delay of each stage of the oscillator, and subsequently, the oscillation frequency can be determined by the value of the passive elements (resistors and capacitors) rather than the properties of the active components. The oscillator was designed and simulated in a 28nm CMOS FDSOI technology. The simulation results reveal that an improvement in the sensitivity of the system to SEEs is obtained without affecting the tuning range or increasing the phase noise, and also show the increased switching speed and reduced leakage current.

Keywords

current mode logic (CML), voltage-controlled oscillator (VCO), single event effect (SEE), radiation-hardened by design (RHBD)

4.1 Introduction

Voltage-controlled oscillators (VCO) are the core of many RF circuits including phase locked loops (PLLs), high-performance clocks, frequency synthesizers, and data recovery systems [1]. However, when this kind of system works inside a radiation environment, the VCO becomes one of the most sensitive blocks to single event effects (SEEs) due to its large cross-section, which makes these blocks more susceptible to receiving the impact of a charged particle, such as alpha particles or heavy ions. The strike of these particles can cause single event transient (SET) pulses or a single event upset (SEU), depending on the energy and duration of the impact [2].The most common VCO designs implemented by IC design are LC-tank oscillators and ring oscillators (RO). The LC-tank oscillator has an excellent performance in terms of phase noise since its oscillation frequency depends only on the inductive and capacitive components in the oscillator. However, these passive components require a much greater die area plus a much more precise design that allows an increase in its limited tuning range. RO-VCOs are also commonly used because they

require a smaller die area, which represents a lower manufacturing cost, larger scalability, and a wider tuning range.

In contrast RO-VCOs are generally more sensitive to SEEs because the circuits are composed of a bias stage and a ring delay stage, which are more vulnerable when struck by a charged particle. An ion hit can cause a transient disturbance in the biasing voltage or a frequency modulation. The use of redundant bias was proposed in order to eliminate SETs in RO-VCO; however, this design requires a larger area in the delay stages and thus has a higher SET sensitivity in this portion of the circuit [3]. In order to mitigate this problem a fully differential delay cell was proposed [4], reducing the impact of a SET on the delay stages, however, the current between each delay stage showed strong fluctuations, causing serious frequency modulation with missing pulses. An alternative to reduce the current rejection performance for delay stages was proposed using a CML-based RO-VCO in standard 65nm CMOS technology [5]. This design achieves a complete mitigation of the frequency modulation effect by using redundant adjustment blocks, such as a biasing block and a 5-stage output buffer, but it also increases the cross-section of the design.

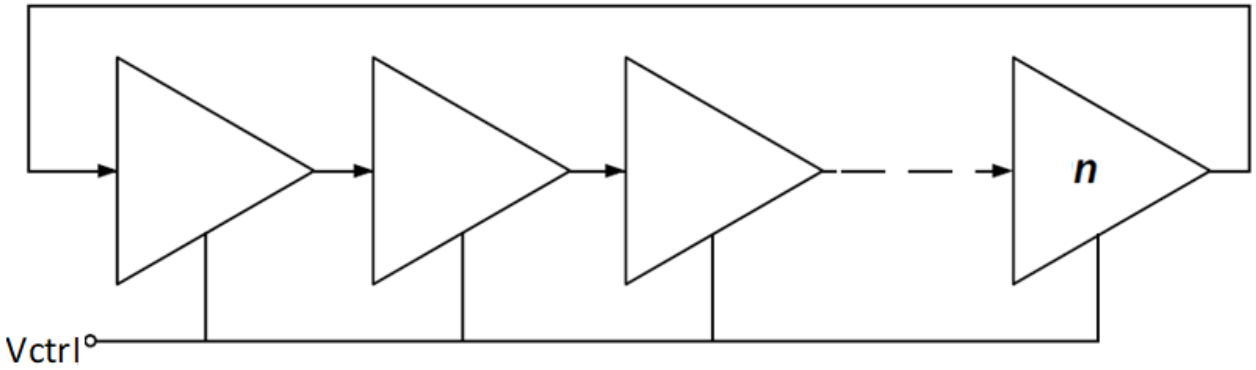


Figure 4.1 Voltage controlled ring oscillator block diagram.

A possible solution for this issue is a CML-based RO-VCO in 28nm CMOS FDSOI technology, which takes advantage of the inherent radiation-hardened features of this technology by the use of a confined channel configuration that reduces leakage and makes the design insensitive to soft error systems. In addition, it has an oscillation frequency obtained from the value of the passive components rather than from the transconductance of transistors, which provides low sensitivity to SEE. This paper is outlined as follows. A detailed design of the circuit is explained in Section 4.2, and the simulation results are shown in Section 4.3.

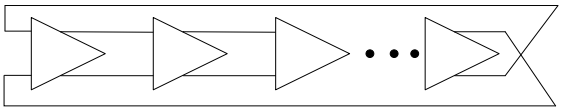
4.2 Circuit Design

4.2.1 Voltage-controlled ring oscillator

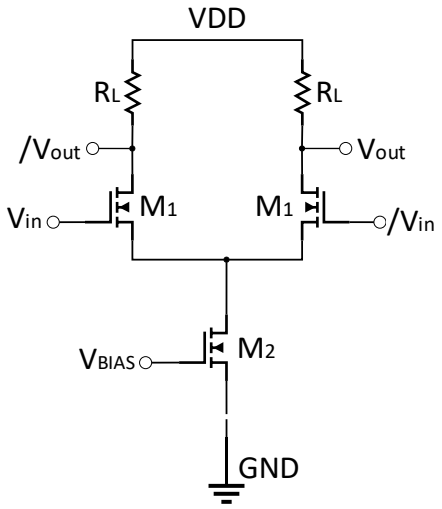
A ring oscillator is a system composed of an odd number of inverters or delay stages connected sequentially forming a ring so that the output of the last inverter is connected to the input of the first. This circuit is able to oscillate between two logic levels, 1 and 0. The oscillation frequency is determined from the sum of the delay contributed by each of the inverters as shown in Equation 4.1, where τ is the total propagation delay produced by an inverter, and N is the total number of inverters used.

$$f_{osc} = \frac{1}{2N\tau} \tag{4.1}$$

In this type of oscillator, the frequency can be tuned by varying the delay, either by changing the number of delay stages, which has a high degree of complexity, or more commonly by varying the amount of charge that is supplied to the stages of delay through the use of a variable biasing voltage, as shown in Figure 4.1.



(a)



(b)

Figure 4.2 (a) CML oscillator block diagram (b) CML buffer stage with resistive load.

This type of oscillator can provide a wide tuning range, but in contrast it is very sensitive to noise and SEEs because its oscillation frequency depends on the transconductance of the transistors that form the delay stage.

4.2.2 CML voltage-controlled oscillator

In order to reduce the sensitivity of the oscillator to noise and SEE, a differential CML-based ring oscillator is proposed. This oscillator uses an even number of sequentially connected delay stages in addition to two crossed feedback lines, as shown in Figure 4.2(a). Each delay stage or delay buffer has a pair of complementary outputs, as shown in Figure 4.2(b).

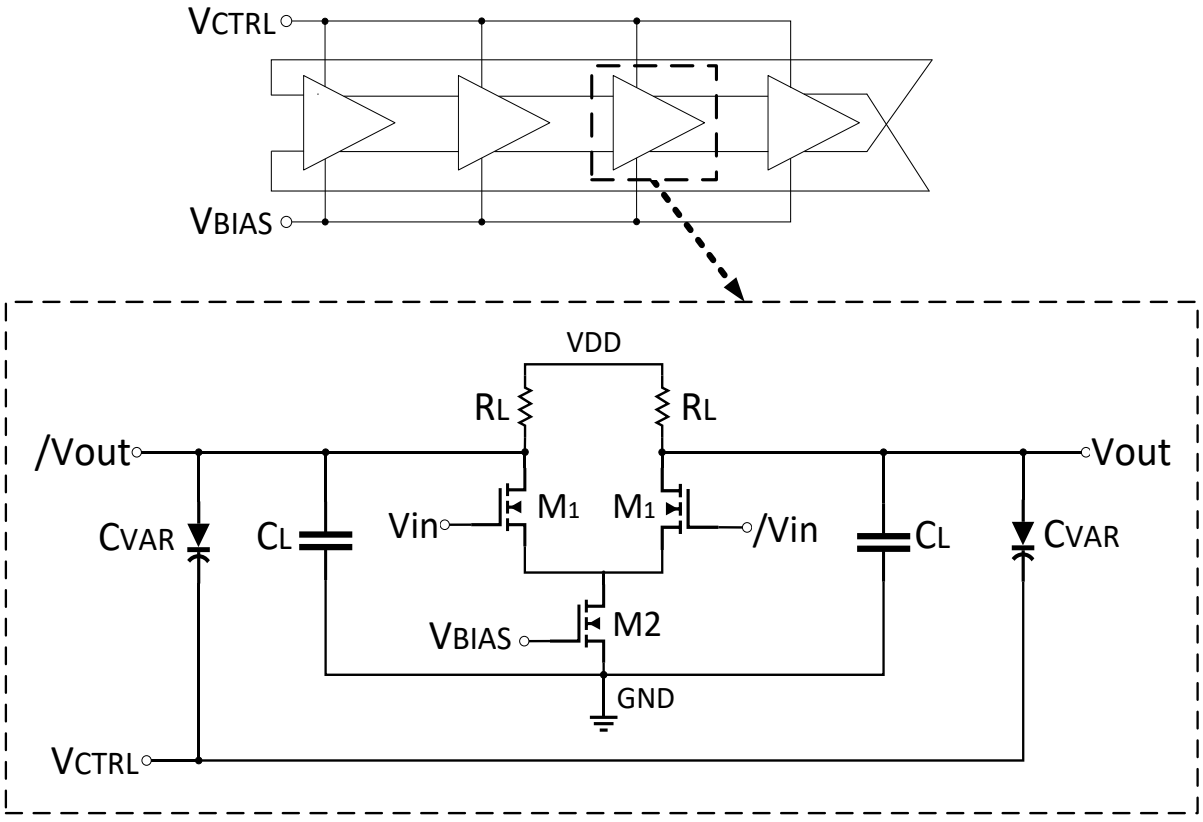


Figure 4.3 Schematic of the proposed VCO and the CML delay stage

The oscillation frequency will be determined from the delay, as in the ring oscillator, using Equation 4.1. However, in the CML based oscillator the total propagation delay of each stage is obtained using Equation 4.2, where C_p corresponds to the total capacitance at the output node, R_L is the load resistance connected to the output node and g_{ds} is the drain-to-source conductance on M1 [6].

$$\tau = \frac{C_p R_L}{1 + g_{ds} R_L} \tag{4.2}$$

This equation shows the total propagation delay on a CML oscillator depends mostly on the output parasitic capacitance and load resistance, which make this design less sensitive to a SEE. Thus, the oscillation frequency can be tuned by varying either the load resistance or the output capacitance. In the first case, R_L can be tuned by using a PMOS transistor operating in the triode region by applying a variable control voltage (Vctrl) but this considerably increases the sensitivity of the system to SEE. On the other hand, it is possible to vary the output capacitance by using MOS varactors in order to regulate the frequency. As it can be appreciated in Figure 4.3, additional load MOS capacitors were added in parallel to the varactors for frequency compensation, modifying the output capacitance, and therefore, the total propagation delay [7]. which is determined using Equation 4.3.

$$\tau = \frac{(C_{var} + C_L + C_p) R_L}{1 + g_{ds} R_L} \tag{4.3}$$

where C_{var} corresponds to the variable capacitance of the MOS varactors, C_L is the compensation MOS capacitors, and C_p represents the parasitic capacitance of the output node, which is considerably smaller than the added capacitance, and consequently, means a reduction in the SEE sensitivity.

Only the g_{ds} conductance may represent a weak point on this design because it can generate a tail current which is still sensitive to SEE. However, this value is smaller than the R_L and C_{var}, thus effectively mitigating the SEE in the bias block. The tuning oscillation frequency for the CML VCO is then given by Equation 4.4, using four stages for performance optimization.

$$f_{osc} = \frac{1 + g_{ds} R_L}{2N(C_{var} + C_L + C_p) R_L} \tag{4.4}$$

4.3 Results and Discussion

Analyzing the simulation results, Figure 4.4 shows that the stabilization time is about 3.5ns, which is very small compared with previous designs, after this time the proposed VCO can generate a stationary sinusoidal waveform indicating that this design can be used in systems that require reliable oscillators.

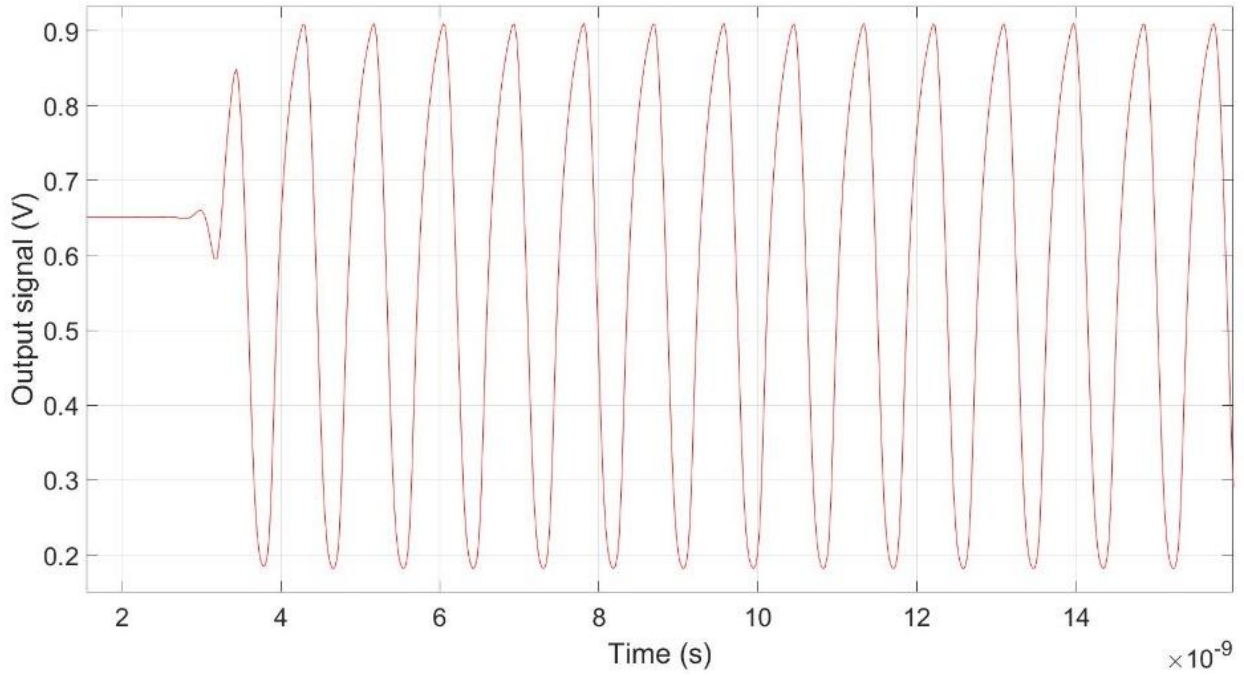


Figure 4.4 Output signal of the CML VCO.

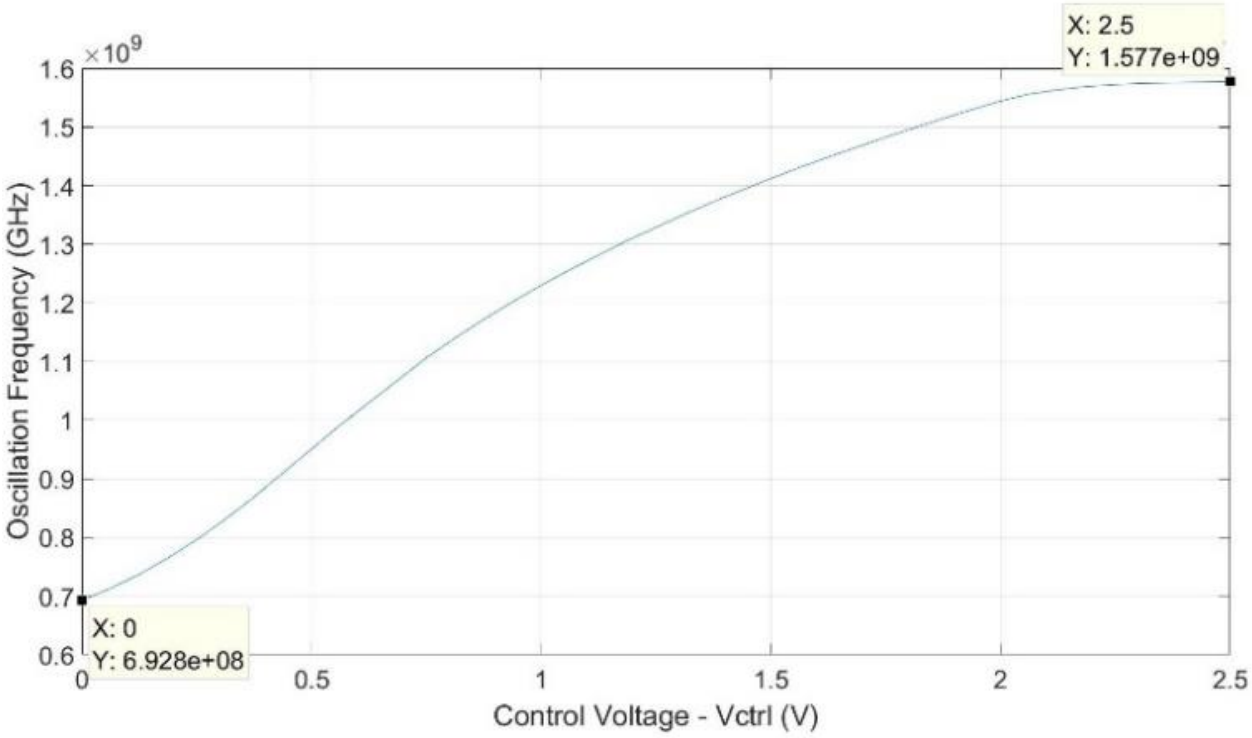


Figure 4.5 Oscillation frequency vs control voltage for CML VCO.

A larger disadvantage of this CML VCO is the limited tuning range generated especially because we are using a wide range control voltage. This is due to the large load resistance R_L. However, as shown in Figure 4.5, the tuning range obtained is about 1GHz (from 692MHz to 1.57GHz) which is quite useful for main telecommunication systems.

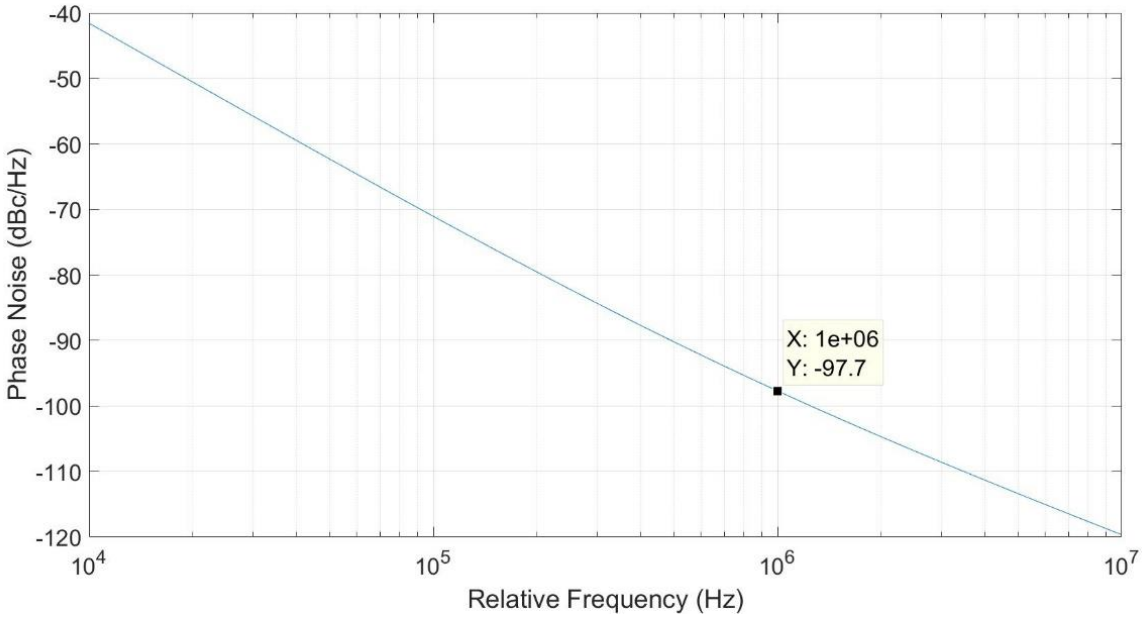


Figure 4.6 Phase noise of CML VCO, with marker at 1MHz offset.

For analyzing phase noise, simulations were carried out using a central frequency of 1.132 GHz, from Figure 4.6, an improvement compared to previous designs can be appreciated, achieving a phase noise of -97.7 dBc/Hz for a 1MHz offset is achieved without the need of additional buffers. The proposed oscillator also shows an improved behavior regarding power consumption, where its performance displays average consumed power of 0.9mW, this low-power design is achieved due to the mitigation of leakage that is provided by the FDSOI technology which uses a confined channel that eliminates the parasitic diffusion capacitance.

For the SEE analysis, simulations were performed by applying an exponential current pulse at 20ns with a peak amplitude of 100µA with a rise and fall time equal to 10ps, and a duration of 1ns. The current pulse was injected into different sensitive nodes of the CML VCO. First, the described current pulse was injected into the bias node. Before the strike, the signal had a period equal to 0.8834ns which gave a fixed frequency of 1.132GHz. Once the current pulse was applied, the oscillation frequency was slightly disturbed showing a period of 0.8836ns, corresponding to an oscillation frequency of 1.1317GHz, which results in a phase shift equal to 0.02%. Additionally,

as shown in Figure 4.7, the amplitude also suffers a small disturbance in the range of 2 or 3mV but without presenting missing pulses or oscillation failure. The perturbation is removed immediately once the injected charge is dissipated.

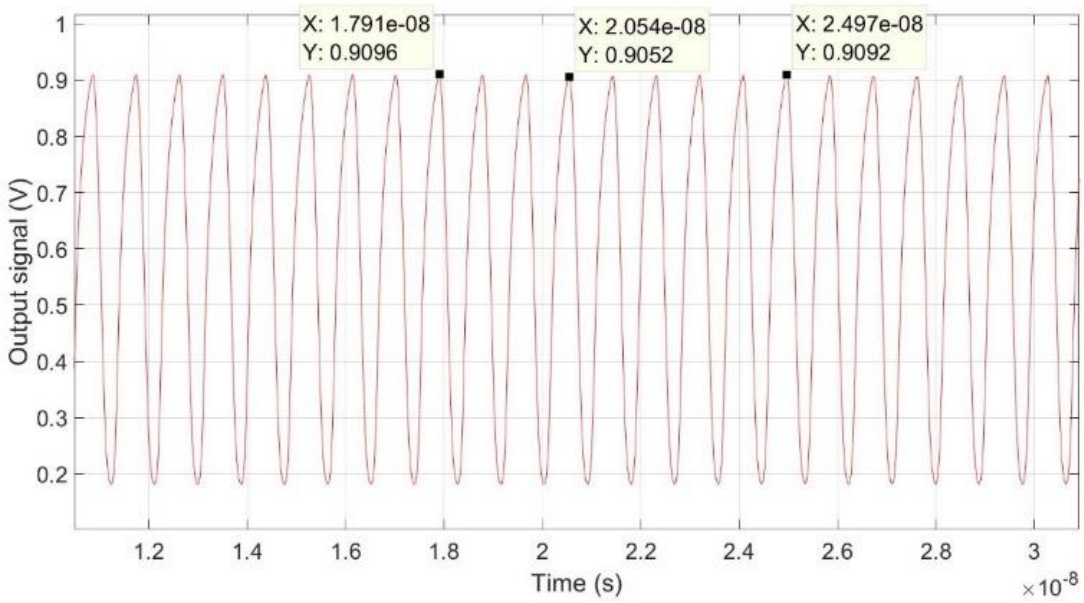


Figure 4.7 Output signal of the CML VCO during the SEE in the bias block, the strike occurs at 20ns and stops at 21ns

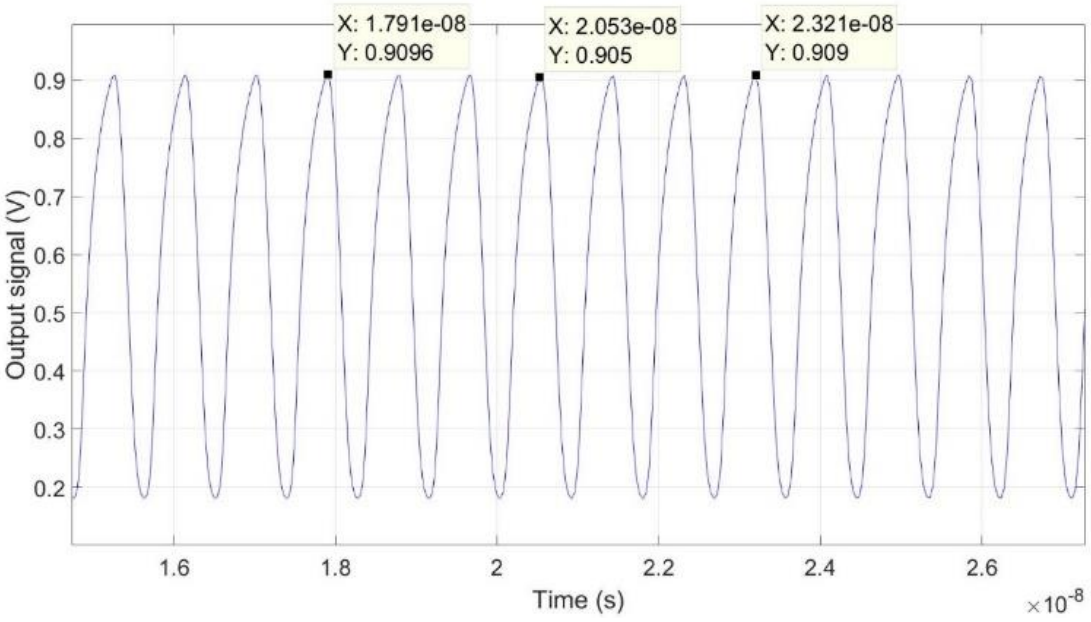


Figure 4.8 Output signal of the CML VCO during the SEE in the Vctrl block, the strike occurs at 20ns and stops at 21ns

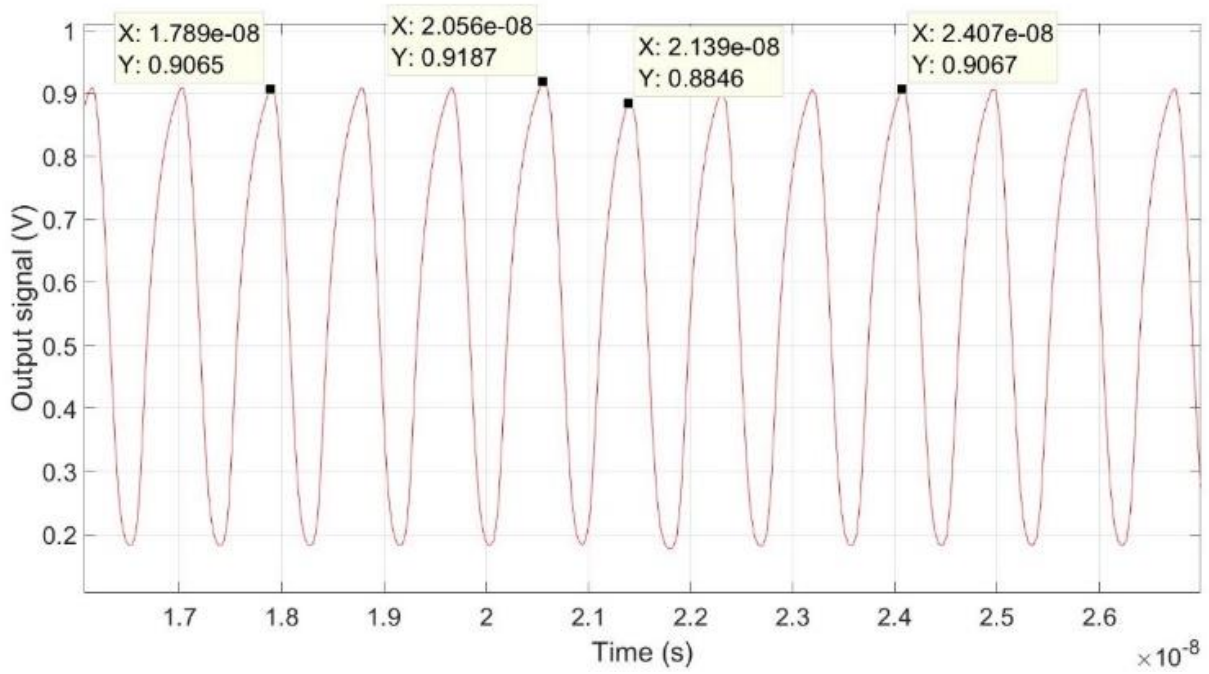


Figure 4.9 Output signal of the CML VCO during the SEE in the delay stage, the strike occurs at 20ns and stops at 21ns

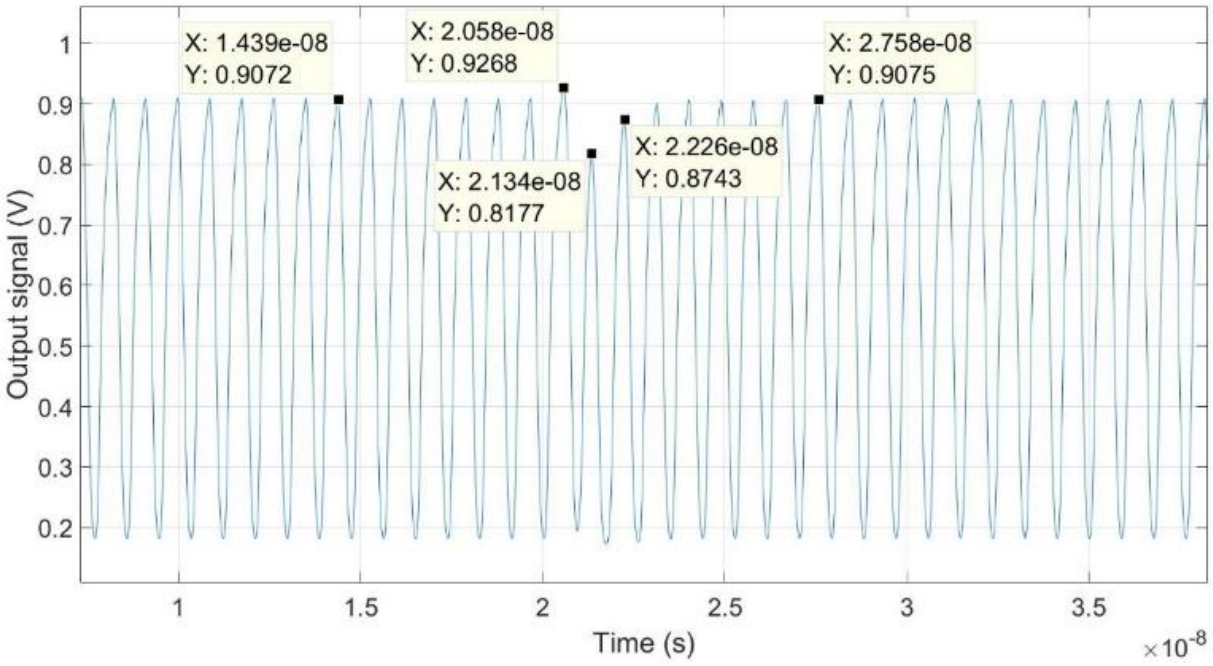


Figure 4.10 Output signal of the CML VCO during the SEE in the delay stage, the strike occurs at 20ns and stops at 21ns, pulse Amplitude of 350µA

The next node of interest is the control voltage of the VCO, the single event was simulated with the same current pulse, obtaining results similar to the obtained in the previous case. Again, before the strike, the period of the signal was 0.8834ns, and once the strike happened the phase was slightly affected, increasing the period to 0.8835ns, which represents a phase shift equal to 0.011%. As in the bias node, the amplitude was slightly attenuated in the range of 4 or mV without resulting in additional problems such as oscillation failure, as in the previous case, the perturbation is removed once the injected charge is dissipated as shown Figure 4.8.

The last SEE test was done by injecting the current pulse in the output of one of the delay buffers. In this case once the strike occurred the signal period was equal to 0.8836ns which resulted in a phase shift of 0.02. In terms of amplitude the disturbance is considerably more noticeable with an amplitude rise of around 20mV, which disappears immediately once the injected charge is dissipated, as can be seen in Figure 4.9. The radiation tolerance of the system was simulated by increasing the peak amplitude of the current pulse. For instance, as Figure 4.10 shows, when a current pulse equal to 350µA was injected, the signal period obtained was 0.88366ns which resulted in a phase shift of 0.029%. Additionally, in terms of amplitude, there is a more noticeable disturbance of around 15mV, but as in previous simulations disappears once the current pulse is dissipated.

The simulation results show the proposed CML oscillator has an improved performance compared with the previous design in 65nm standard CMOS. As shown in Table 4.1, the improvement was achieved not only in terms of power consumption and stability but also in terms of low sensitivity to a SEE.

Table 4.1 Comparison in terms of performance and SEE sensitivity

Process	**Tuning Range**	**Phase Noise**	**Power Consumption**	**Average Frequency shift (during SE)**
65 nm Bulk	800 MHz – 3.2 GHz	-92.15 dBc/Hz	1.2 mW	3%
28 nm FDSOI	692 MHz - 1.57GHz	-97.7 dBc/Hz	0.9 mW	0.015%

4.4 Conclusion

The standard ring oscillator presents a high sensitivity to a SEE and high-power consumption. In order to improve the performance a CML-based VCO was designed in 28nm CMOS FDSOI technology. In this design, the oscillation frequency was tuned by using MOS varactors which reduced the sensitivity to a SE. Simulations were performed by injecting current pulses into the bias node, control voltage node and delay buffer stage of the CML VCO. The simulation shows that the proposed design effectively reduces the sensitivity with an average frequency shift equal to 0.015% during the incidence of the current pulse with 100µA peak amplitude. In addition, the proposed system shows an improved performance regarding phase noise and power consumption with values equal to -97.7dBc/Hz and 0.9mW respectively, which was achieved due to the use of a fully depleted technology for the design.

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5. CONCLUSIONS, CONTRIBUTIONS AND FUTURE WORK

5.1 Conclusions

This work examines the use of a hybrid voltage-controlled oscillator as a possible solution to the limitations presented by the commonly employed VCO models. In order to determine the efficiency of the proposed design, a comparative study in terms of electrical performance and SEE tolerance was carried out. This analysis involved three different VCO structures implemented and fabricated in 65nm bulk technology. In addition, the advantages of FDSOI technologies were considered as a way to improve the proposed circuit. For this purpose, two oscillators were implemented in 28nm FDSOI technologies. From the results obtained in the present work, the following conclusions were found.

Regarding the proposed CML VCO implemented in 65nm bulk CMOS, simulation and experimental results revealed that the proposed structure effectively exploits the positive characteristics of the current-starved VCO and LC-tank VCO. Specifically, the results showed that proposed design can effectively provide a wide tuning range. In terms of SEE tolerance and noise sensitivity, the CML VCO showed a response similar to the L- tank VCO without requiring a large cross-section. Although spurious noise around the main carrier was registered during the laser testing, the proposed design showed a fast recovery time in case of a SEE. In addition, the expected limitations of the RO-VCO and LC-tank VCO were also probed through the simulation and experimental results. It can be concluded that the proposed CML VCO is an efficient option for high-performance PLLs in harsh radiation environments.

With reference to the use of FDSOI technologies, the simulation results demonstrated significant improvements in terms of SEE tolerance and power consumption without increasing the phase noise levels or excessive narrowing of the tuning range. In addition, there was an obvious reduction of the design area due to the feature size of the employed technology. The analysis described suggests that in effect, the FDSOI technology provides great advantages to the performance of analog circuits.

5.2 Contributions

The main contributions of this work are related to a new high-performance and radiation-tolerant VCO design and the use of new technologies for analog circuit implementation. This study demonstrates the limitation of commonly employed voltage-controlled oscillators and provides enough evidence to probe the efficiency of a rarely used CML VCO model in terms of radiation tolerance and electrostatic performance. Moreover, this work proves the advantages of FDSOI, which it should be emphasized have not been extensively explored in the implementation of analog circuits. The proposed studies have been divided into two manuscripts, one was presented at the IEEE Canadian Conference on Electrical and Computer Engineering (2019), and the other is under review by the *IEEE Transactions on Nuclear Science journal*.

5.3 Future Work

Although the results shown by the designs implemented in FDSOI are promising, it is necessary to manufacture the testchip in order to perform SEE experiments that verify the information obtained through simulation. In addition to this, it is advisable to conduct more studies on the use of the FDSOI technology in other analog circuits, paying special attention to the implementation of a complete PLL system.