STUDY OF RADIATION TOLERANT STORAGE CELLS FOR DIGITAL SYSTEMS

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Abstract

Single event upsets (SEUs) are a significant reliability issue in semiconductor devices. Fully Depleted Silicon-on-Insulator (FDSOI) technologies have been shown to exhibit better SEU performance compared to bulk technologies. This is attributed to the thin Silicon (Si) layer on top of a Buried Oxide (BOX) layer, which allows each transistor to function as an insulated Si island, thus reducing the threat of charge-sharing. Moreover, the small volume of the Si in FDSOI devices results in a reduction of the amount of charge induced by an ion strike.

The effects of Total Ionizing Dose (TID) on integrated circuits (ICs) can lead to changes in gate propagation delays, leakage currents, and device functionality. When IC circuits are exposed to ionizing radiation, positive charges accumulate in the gate oxide and field oxide layers, which results in reduced gate control and increased leakage current. TID effects in bulk technologies are usually simpler due to the presence of only one gate oxide layer, but FDSOI technologies have a more complex response to TID effects because of the additional BOX layer.

In this research, we aim to address the challenges of developing cost-effective electronics for space applications by bridging the gap between expensive space-qualified components and high-performance commercial technologies. Key research questions involve exploring various radiation-hardening-by-design (RHBD) techniques and their trade-offs, as well as investigating the feasibility of radiation-hardened microcontrollers.

The effectiveness of RHBD techniques in mitigating soft errors is well-established. In our study, a test chip was designed using the 22-nm FDSOI process, incorporating multiple RHBD Flip-Flop (FF) chains alongside a conventional FF chain. Three distinct types of ring oscillators (ROs) and a 256 kbit SRAM was also fabricated in the test chip. To evaluate the SEU and TID performance of these designs, we conducted multiple irradiation experiments with alpha particles, heavy ions, and gamma-rays. Alpha particle irradiation tests were carried out at the University of Saskatchewan using an Americium-241 alpha source. Heavy ion experiments were performed at the Texas A&M University Cyclotron Institute, utilizing Ne, Ar, Cu, and Ag in a 15 MeV/amu cocktail. Lastly, TID experiments were conducted using a Gammacell 220 Co-60 chamber at the University of Saskatchewan. By evaluating the performance of these designs under various

irradiation conditions, we strive to advance the development of cost-effective, high-performance electronics suitable for space applications, ultimately demonstrating the significance of this project.

When exposed to heavy ions, radiation-hardened FFs demonstrated varying levels of improvement in SEU performance, albeit with added power and timing penalties compared to conventional designs. Stacked-transistor DFF designs showed significant enhancement, while charge-cancelling and interleaving techniques further reduced upsets. Guard-gate (GG) based FF designs provided additional SEU protection, with the DFR-FF and GG-DICE FF designs showing zero upsets under all test conditions. Schmitt-trigger-based DFF designs exhibited improved SEU performance, making them attractive choices for hardening applications. The 22-nm FDSOI process proved more resilient to TID effects than the 28-nm process; however, TID effects remained prominent, with increased leakage current and SRAM block degradation at high doses. These findings offer valuable insights for designers aiming to meet performance and SER specifications for circuits in radiation environments, emphasizing the need for additional attention during the design phase for complex radiation-hardened circuits.

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First, I would like to express my deepest gratitude and love to my biggest supporter in life, whose unwavering love, encouragement, and belief in me have been the cornerstone of my success. Your understanding and patience during challenging times have been truly inspiring, and your constant motivation has pushed me to work harder.

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List of Abbreviations

ADC	Analog-to-Digital Converters
ASIC	Microprocessors and Application-Specific Integrated Circuit
BOX	Buried Oxide
CHB	Checkerboard
CMOS	Complementary Metal-Oxide-Semiconductor
CNRX	Continuous Active Diffusion
CO-59	Cobalt-59
CO-60	Cobalt-60
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DFR	Dual-Feedback-Recovery
DICE	Dual Interlocked Storage Cell
DSET	Digital Single Event Transient
DUT	Device Under Test
ECC	Error Correction Code
FBB	Forward Body Bias
FDSOI	Fully Depleted Silicon-on-Insulator
FF	Flip-Flop
GG	Guard Gate
HI	Heavy Ion
IC	Integrated Circuit

IGBT	Insulated Gate Bipolar Transistors
LEAP	Layout Error-Aware Transistor Positioning
LET	Linear Energy Transfer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistors
NI-60	Nickel-60
NSREC	Nuclear Science and Space Radiation Effects Conference
PDK	Process Design Kit
PLL	Phase-Locked Loop
PIF	Proton Irradiation Facility
RBB	Reverse Body Bias
RHBD	Radiation Hardened by Design
RO	Ring Oscillator
SE	Soft Error
SEB	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SI	Silicon
SIA	Semiconductor Industry Association

SOI	Silicon on Insulator
SRAM	Static Random-Access Memory
ST	Schmitt Trigger
STI	Shallow Trench Isolation
TAMU	Texas A & M University
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
VLSI	Very Large-Scale Integration

1 Introduction

1.1 Introduction

In recent years, advanced semiconductor technologies have gained increasing importance in space systems and high-performance computing, with the aim of enhancing performance, reducing power consumption, and minimizing system size and weight. However, the harsh radiation environment in space, as well as on Earth, poses significant challenges to the reliable operation of electronic systems. Single-event upsets (SEUs) and total ionizing dose (TID) effects are two critical factors that can lead to malfunctions or even permanent damage to electronic systems in these settings [1-3]. Consequently, radiation-hardening-by-design (RHBD) techniques

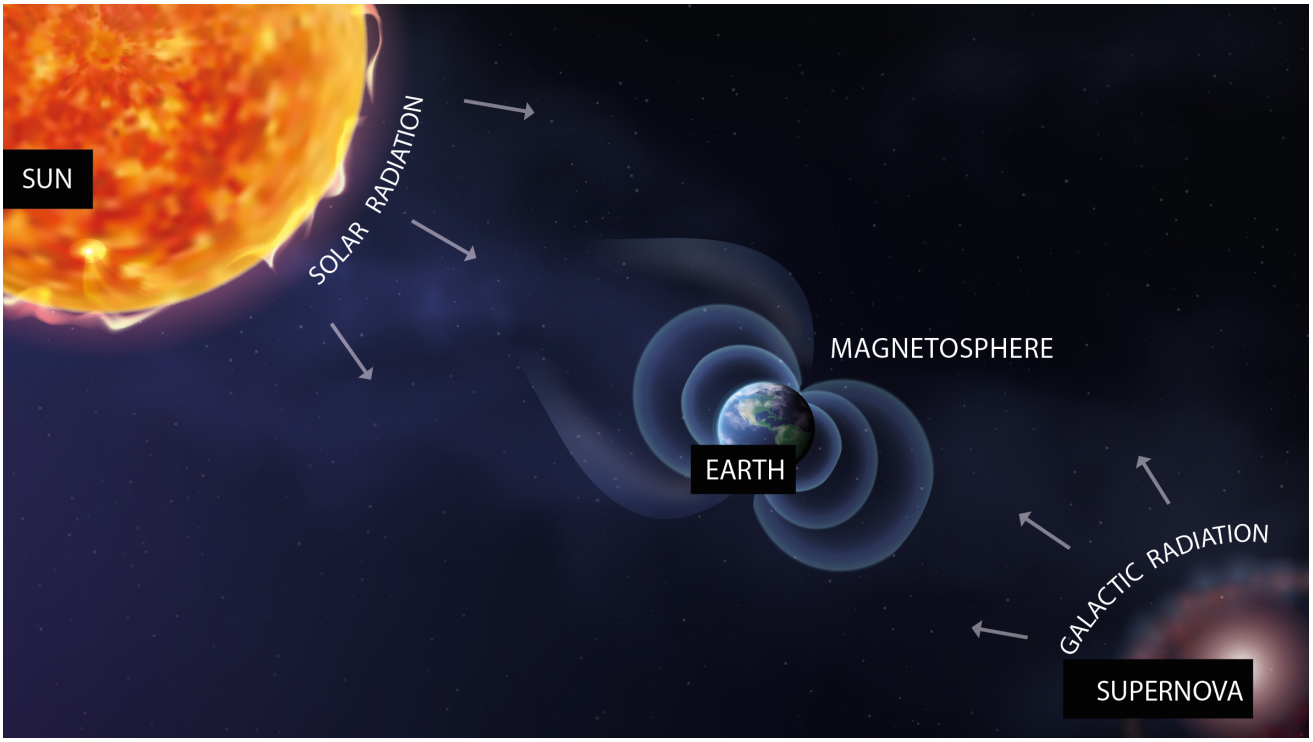

Figure 1.1 Cosmic radiation environment in space [4].

are essential for developing robust designs that can withstand ionizing radiation and maintain reliable performance in extreme environments.

SEUs, caused by radiation particles interacting with nanoscale technologies, are a major reliability issue for modern micro-electronic systems [5]. These events can affect various storage components, such as memory cell arrays, flip-flops (FFs), and Static Random-Access Memories (SRAMs), leading to bit flips and functionality issues. To address this, designers often implement RHBD techniques through layout, schematic, or system-level architectural manipulations, improving SEU resilience for components like FFs [6-8]. Additionally, error correction and detection methods are employed to further safeguard systems against radiation-induced errors.

On the other hand, TID effects in integrated circuits (ICs) can result in changes to gate propagation delays, leakage currents, and even loss of device functionality [9,10]. These effects are particularly concerning in long-term space missions, where devices can be exposed to constant sources of radiation for years. ICs in bulk technologies and Fully Depleted Silicon-on-Insulator (FDSOI) technologies exhibit different responses to TID effects, necessitating tailored radiation-hardening approaches [10,11]. Designers must carefully choose the appropriate technology and design techniques to achieve optimal radiation tolerance while balancing other factors like power consumption, performance, and cost.

As technology continues to scale down and supply voltage decreases, ensuring the reliability of electronic systems in radiation-rich environments becomes increasingly crucial. By employing RHBD techniques and understanding the impact of SEUs and TID effects on various semiconductor technologies, designers can develop more resilient systems for aerospace and high-performance computing applications. This requires continuous research and development in radiation-hardening techniques, material sciences, and device modeling to stay ahead of the ever-evolving challenges posed by radiation effects on semiconductor technologies. In turn, this will enable more advanced and reliable systems capable of withstanding the harsh conditions found in space, nuclear facilities, and other radiation-prone environments, ultimately contributing to the success and safety of missions and operations in these demanding contexts.

1.2 Motivation

As previously noted, the sensitivity of integrated circuits (ICs) to individual ions, such as alpha particles from packaging material, increases significantly as their feature size decreases. FDSOI technology nodes exhibit promising radiation-hardness characteristics compared to bulk technology nodes. However, as feature sizes reach the nanometer scale, single event upsets (SEUs) remain a concern, necessitating the development of innovative hardening techniques to ensure reliable electronic device performance in space. Additionally, understanding the comparative total ionizing dose (TID) resilience between different nodes is essential when choosing the most suitable technology for various space applications.

FDSOI technologies are attractive due to features such as high speed and low power consumption, making them good candidates for space applications. Unlike bulk technologies, FDSOI technologies utilize a thin Silicon (Si) layer on top of a Buried Oxide (BOX), providing superior gate control in the channel region and reduced nodal capacitances, as illustrated in Figure 1.2 [8,12,13]. The thin Si layer also limits charge collection after ion strikes due to the reduced active-Si volume [14]. FDSOI technologies largely avoid the charge-sharing issues experienced by bulk technologies, which occur when multiple transistors that are in close proximity to an impacted transistor collect simultaneous charges.

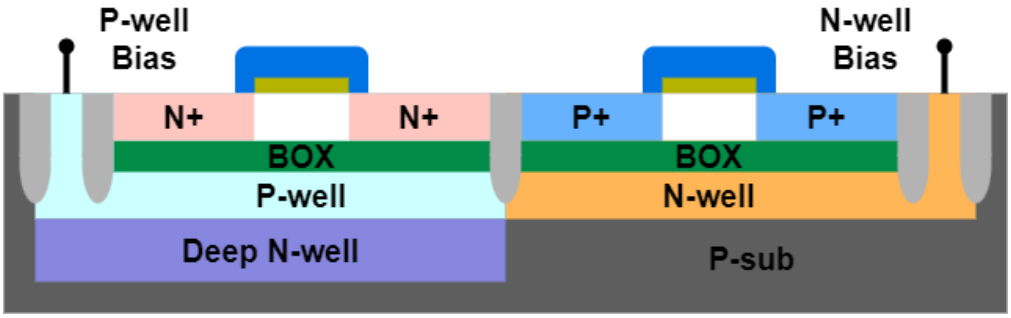

Figure 1.2 22-nm FD SOI transistor cross sections for a regular well configuration [8].

In addressing residual single event challenges, researchers often focus on circuit-level approaches that do not necessitate modifications at the process or technology level [6,7]. These methods involve alterations to the schematics or layouts of the target design. Due to the infeasibility of changing fabrication processes to enhance single-event (SE) performance, designers typically opt for RHBD techniques [6]. Some of the challenges in this research area

include the introduction of cost-effective mitigation solutions and the management of trade-offs between SEU performance, power, area, and other factors. Implementing SEU mitigation techniques often involves modifying layout, schematic, or system-level architectures, and striking the right balance among these parameters can be difficult [6,7]. By addressing these challenges, this study aims to contribute valuable insights to the development of radiation-hardened electronics for various applications.

In FDSOI technologies, TID effects are more complex compared to bulk devices due to the presence of an additional parasitic structure introduced by the Buried Oxide (BOX) layer [8,15 - 19]. This layer leads to a two-dimensional coupling effect between the front and back interfaces of the channel, significantly impacting the ionizing dose response of FDSOI devices. As a result, FDSOI technologies exhibit greater sensitivity to TID than bulk counterparts [10,20,21]. Despite their inherent resistance to particle-induced single event effects (SEEs) making FDSOI technologies appealing for space missions [6,10,11], previous research on the 28-nm FDSOI technology node [3,6] demonstrated substantial increases in TID-induced gate delay and leakage currents. These challenges present difficulties for space applications requiring high total absorbed dose tolerance, making it essential to investigate TID effects in the 22-nm FDSOI technology node as well.

1.3 Objectives

The overall goal of this thesis is to study the SEU and TID performance at the 22-nm FDSOI technology node, and develop cost-effective electronics for various space applications. To achieve this, a test chip was designed and fabricated using the 22-nm FDSOI process, incorporating multiple RHBD FF chains alongside a conventional FF chain, three distinct types of ROs, and a 256 kbit SRAM. Multiple irradiation experiments were conducted to assess the SEU and TID performance of these designs. The thesis is structured around three specific objectives:

Investigate the SEU performance of different RHBD FFs based on three fundamental hardening techniques: transistor-stacking, guard-gating, and Schmitt-triggers. This objective involves the development, testing, and analysis of various FF designs making use of these techniques, such as stacked FF, charge-canceling stacked FF, interleaved-stacked FF, GG FF, DFR

FF, GG-DICE FF, ST1 FF, ST2 FF, and ST-DFR FF. All design were fabricated using the same 22-nm FDSOI process. The designs were subjected to alpha particle and heavy ion irradiation for SEU characterization, and their SEU performance is thoroughly evaluated.

Compare the total ionizing dose effects in 22-nm and 28-nm FDSOI technologies using SRAM and ring oscillator designs. This objective aims to assess the TID performance of the 22-nm FDSOI technology by utilizing SRAM and various RO designs, such as inverter ROs, NAND ROs, and NOR ROs. The results are compared to those of the 28-nm FDSOI node to identify differences in radiation tolerance between the two technology nodes. The findings will highlight the necessity for careful consideration when designing complex circuits for radiation-hardened applications.

1.4 Thesis Overview

This thesis comprises the author's manuscripts published or currently under review during their master's studies. It focuses on the examination of single event effects on digital systems through simulation and experimental results. Each chapter begins with a concise summary, highlighting the connection between the current chapter and the preceding one, followed by a brief conclusion. The organization and primary content of this thesis are summarized below.

Chapter 1 offers a brief introduction to radiation effects and fundamental background information, as well as the motivation and objectives of this research.

Chapter 2 delves into more detailed background information, covering the radiation effects investigated in this research, radiation particles, experimental facilities, and radiation-hardening techniques used in the project.

Chapter 3 examines the design and experimental results of stacked-transistor-based hardened flip-flop designs in comparison to conventional designs at the 22-nm FDSOI node. It presents three stacked-transistor-based DFF designs and evaluates their SEU performance after exposure to alpha particle and heavy ion irradiation.

Chapter 4 explores multiple RHBD flip-flop designs using guard-gate circuits at the 22-nm FDSOI node and presents their irradiation results. The chapter evaluates the SEU performance

of several guard-gate (GG) structure-based FF designs after exposure to alpha particle and heavy ion irradiation and assesses the impact of the CnRx construct in the GG design.

Chapter 5 evaluates the single-event performance of Schmitt-trigger-based flip-flop designs compared to the conventional DFF design at the 22-nm FDSOI node. The study presents three Schmitt-trigger-based FF designs and assesses their SEU performance after exposure to alpha particle and heavy ion irradiation.

Chapter 6 presents a comparative study of total ionizing dose effects between the 22-nm and 28-nm FDSOI technology nodes, focusing on ring oscillators and memory elements. The study uses ring oscillators (ROs) and a 256 kbit SRAM block to assess the TID sensitivity of these devices, followed by Co-60 radiation tests to evaluate their TID performance.

Finally, Chapter 7 provides conclusions and recommendations for future work.

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2 Background

In this chapter, a comprehensive overview of the key single event effects (SEEs) relevant to electronic systems is provided. The discussion encompasses single event transients (SETs), single event upsets (SEUs), single event latch-ups (SELs), single event functional interrupts (SEFIs), and single event gate ruptures (SEGRs). Additionally, the concept of total ionizing dose (TID) is introduced, along with its implications for device performance and reliability.

Various irradiation sources utilized in this research are examined, including heavy ions, alpha particles, Co-60 gamma rays, protons, and lasers, as well as their impact on electronic components. Furthermore, error correction techniques are presented, such as error correction codes (ECC) and the principles of Hamming codes, which serve to safeguard SRAM blocks in radiation environments.

2.1 Single Event Effects

SEEs are radiation-induced phenomena that can lead to functional disruptions, performance degradation, or permanent damage in electronic devices and systems operating in high-energy particle environments, such as those encountered in space or high-altitude aviation applications [1]. These effects originate from the interaction of high-energy particles, including cosmic rays, protons, or heavy ions, with sensitive areas of integrated circuits (ICs) and semiconductor devices, resulting in transient or permanent errors in device operation [2][3].

SEEs encompass a broad spectrum of effects, such as SEUs, SELs, SEGRs, single event burnouts (SEBs), SEFIs, and SETs [4][5]. Each effect poses unique challenges and can significantly impact the reliability and performance of electronic systems in radiation-rich environments.

Numerous mitigation techniques have been developed over the years to address the various types of SEEs. These approaches include radiation-hardened technologies, circuit-level design techniques like redundancy, ECC, and radiation-hardening-by-design (RHBD), as well as system-level strategies such as fault-tolerant computing and radiation-aware software design [6]. Despite these efforts, SEEs continue to pose a significant challenge for modern electronic systems, especially as device scaling persists and technology nodes become smaller, heightening the sensitivity of devices to radiation-induced errors.

2.1.1 Single Event Transient

A SET is a single event effect in combinational-logic circuits of digital systems, contrasting with SEUs in sequential cells. SET soft error rates are influenced by factors like clock speed, with higher frequencies increasing the likelihood of capturing SETs and potentially limiting system speed [7].

SETs occur when ions strike a buffer or other combinational cell in a digital circuit, generating a transient pulse that may impact the entire system if captured by a flip-flop. An SET in the system clock tree can cause system failure by producing an extra clock edge and disrupting sequential logic.

Energetic particles, like heavy ions, create SETs by interacting with reverse-biased PN junctions in combinational logic transistors. They generate transient pulses through direct and secondary ionization processes. SETs can be categorized as Analog (ASET) or Digital (DSET) based on their presence in analog or digital circuits.

The focus here is on DSETs, which have become a growing concern due to technology scaling. DSETs can significantly affect the soft error rate (SER) in sub-100nm technologies, with even relatively low-energy alpha particles potentially increasing the SER [8,9]. Therefore, examining DSETs and their impact is vital for developing reliable digital technologies.

2.1.2 Single Event Upset

A Single Event Upset is a non-destructive, transient error that occurs in electronic systems due to the interaction of ionizing radiation with the sensitive regions of semiconductor devices [10]. SEUs can lead to the alteration of stored data or change in the logic state of the electronic device, potentially causing a malfunction or system failure [11]. With the increasing demand for high-performance electronics in various fields such as aerospace, defense, medical, and telecommunications, the impact of SEUs on the reliability and overall performance of electronic systems has become a critical concern [12].

The most common manifestation of an SEU is a bit flip, where a binary value (0 or 1) stored in a memory cell, or a flip-flop is changed to the opposite value. This can lead to data corruption, incorrect calculations, or system malfunctions. The susceptibility of electronic systems to SEUs depends on several factors, including device technology, circuit design, operating environment, and shielding techniques [13]. As technology nodes continue to shrink, the sensitivity of semiconductor devices to SEUs has increased due to the reduced charge collection volume, lower operating voltages, and higher integration densities [10]. Moreover, the use of advanced electronic systems in harsh radiation environments, such as space and high-altitude applications, further increases the likelihood of SEUs [14].

SEUs can significantly affect the reliability and performance of electronic systems, causing system crashes, data corruption, or unexpected behavior [15]. In safety-critical systems, such as avionics and nuclear power plant control systems, SEUs can pose severe risks to human life and the environment. Therefore, understanding the mechanisms of SEUs and their impact on electronic systems is essential for designing robust and reliable systems [16].

SEUs occur is all types of storage cells, including latch, SRAM cells, DRAM cells, and dynamic logic circuits. Figure 2.1 shows the schematic of a D latch, including two pass gates and a pair of inverters with a positive feedback loop.

Consider Image 2.1. When both CLK and input D are high, the latch enters the hold state. In this situation, the MN1 and the MP2 are turned off, making them sensitive to radiation strikes. If a particle impacts the drain of MN1, the resulting current may be significant enough to surpass

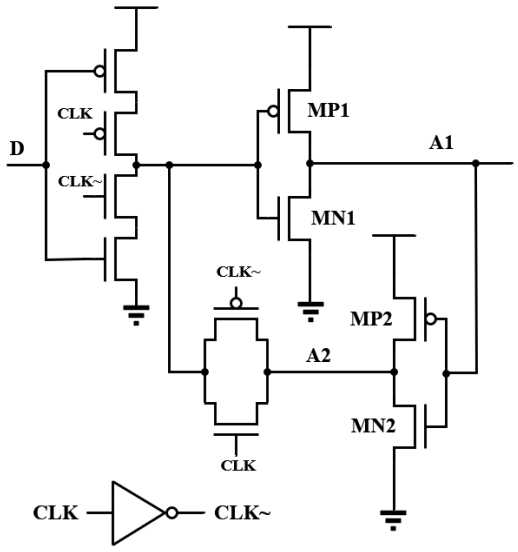

Figure 2.1 D-Latch design.

the restoring current provided by the MP1. This voltage perturbation at the affected node can then propagate to inverter in the feedback loop, potentially causing an unintended state change in the D latch, which is known as the SEU.

2.1.3 Single Event Latchup

A SEL is a radiation-induced phenomenon that can have severe consequences for ICs exposed to high-energy particle environments, such as those encountered in space or high-altitude aviation applications. The latch-up effect occurs when high-energy particles, like galactic cosmic rays or heavy ions, strike the sensitive regions of the IC, creating a parasitic thyristor structure that can induce a high current state and potentially result in permanent device damage or failure [17,18].

The SEL was first observed in the early 1970s, coinciding with the increasing integration of bipolar and complementary metal-oxide-semiconductor (CMOS) technologies in microelectronics [19]. Since then, it has emerged as a critical reliability concern for designers of electronic systems operating in radiation-rich environments.

Over the years, a variety of mitigation techniques have been developed to prevent or reduce the risk of SEL in ICs. These methods encompass radiation-hardened technologies and process modifications, as well as circuit-level design techniques and system-level approaches [20,21].

Despite these advancements, SELs remain a significant challenge for modern ICs, particularly as device scaling persists and technology nodes continue to shrink.

2.1.4 Single Event Functional Interrupts

SEFIs are radiation-induced events that can cause temporary functional disruptions or malfunctions in ICs operating in high-energy particle environments, such as those found in space or high-altitude aviation applications. SEFIs occur when high-energy particles, like galactic cosmic rays or heavy ions, interact with sensitive regions of the IC, resulting in erroneous outputs, state changes, or unintended operations without causing permanent damage [1,2].

SEFIs have been a topic of concern since the early days of space electronics, as they can significantly impact system reliability and mission success. They are particularly critical for complex digital systems, such as microprocessors and application-specific ICs (ASICs), where even a transient disturbance can have a cascading effect on overall system functionality [22].

Various mitigation techniques have been developed over the years to prevent or reduce the risk of SEFIs in ICs. These methods include radiation-hardened technologies, circuit-level design techniques, such as redundant architectures or ECC, and system-level approaches, like fault-tolerant computing and watchdog timers [5,6]. Despite these efforts, SEFIs remain a significant challenge for modern ICs, especially as device scaling continues and technology nodes shrink.

2.1.5 Single Event Gate Ruptures

SEGRs are radiation-induced events that can cause permanent damage or failure in power metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs) when exposed to high-energy particle environments, such as those encountered in space or high-altitude aviation applications. SEGRs transpire when high-energy particles, like cosmic rays or heavy ions, impact the gate oxide region of the transistor, resulting in a localized increase in the electric field, which can subsequently lead to gate oxide breakdown and device failure [23,24].

SEGRs were initially reported in the 1980s when researchers observed unanticipated failures in power MOSFETs and IGBTs operating in radiation-rich environments [25,26]. Since then, SEGRs have emerged as a critical reliability concern for designers of electronic systems that function in such conditions, particularly for high-voltage and high-power applications.

A variety of mitigation techniques have been developed to prevent or reduce the risk of SEGRs in power devices. These methods encompass radiation-hardened technologies, process modifications to enhance gate oxide robustness, and design techniques such as increasing the gate oxide thickness or incorporating gate field plates [26,27]. Despite these advancements, SEGRs continue to pose a significant challenge for modern power devices, especially as the demand for high-voltage and high-power systems persists.

2.2 Total Dose Effects

The TID effect refers to the degradation of devices caused by prolonged exposure to high-energy particles in radiation environments [28-35]. This degradation occurs when energetic particles generate charged electron-hole pairs in the SiO2 layer, which can become trapped at the Si-SiO2 interface and form an electric field. Over time, this leads to the deterioration of the device's electrical characteristics, increased gate delay, and higher transistor leakage current. In extreme cases, it can cause circuit malfunctions as well.

Modern technologies have reduced gate oxide layers to nanometer scales, effectively mitigating TID effects [36]. However, TID analysis in Silicon-On-Insulator (SOI) technologies is more complex due to the additional Buried Oxide isolation layer between the substrate and body, alongside the gate oxide and Shallow Trench Isolation (STI) [37].

2.3 Irradiation Sources

2.3.1 Heavy Ion Irradiation Source

Heavy ion accelerators generate high-energy ion beams with energies up to GeV levels and linear energy transfer (LET) values spanning the full LET range found in space, from less than 1

MeV-cm^2/mg to around 100 MeV-cm^2/mg [38]. These accelerators enable efficient evaluation of ICs' SEE performance and data collection for in-orbit error rate calculations. The detection of the first space-related soft error caused by heavy ions led to research on their effects and radiation-tolerant designs for space-based ICs [39].

Ground-based accelerators allow researchers to effectively simulate naturally occurring heavy ions, providing a cost-effective and controllable method for replicating the space environment. This technique enables repeated radiation-effect experiments and in-depth studies of radiation-hardened designs. In this study, heavy-ion experiments were carried out at TAMU. Figure 2.2 shows the heavy-ion control room and facility at TAMU.

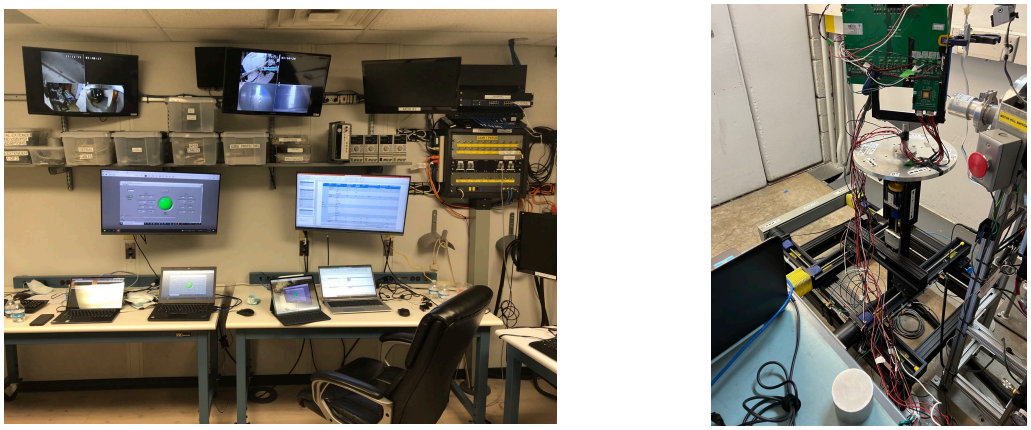

Figure 2.2 Heavy-ion facility at TAMU.

2.3.2 Alpha Particle Irradiation Source

Alpha particles, which are high-velocity helium nuclei with two protons and two neutrons, have a rest mass of 6.64 x 10-27 kg and an electric charge of 3.20 x 10-19 coulomb. Intel reported the first SEE on Earth caused by an alpha particle from radioactive-contaminated packaging material in ICs [40].

Alpha particles, primarily emitted through the decay of materials like Americium 241, have a dominant energy peak at 5.486 MeV, representing 85.2% of the particles. These particles can penetrate the 10-20 μm dead layer of ICs and access the sensitive layer due to their 27.9 μm range in silicon. The LET of a 5.486 MeV alpha particle is 0.5 MeV-cm^2/mg [41], though the LET range

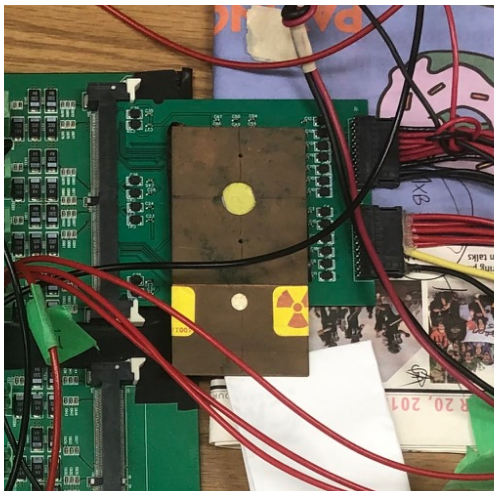

Figure 2.3 Alpha particle source on the top of the testing circuit.

of alpha particles exiting from an Am-241 source can range from approximately 0.1 LET to 2.6 LET.

Alpha sources offer the advantage of not requiring an accelerator and having no beam time limitations. The dose rate can be controlled by applying various concentrations of Americium 241 to a copper plate. The alpha source used in this work is shown in Figure 2.3.

2.3.3 Co-60 Irradiation Source

Co-60 is a widely used radioactive isotope in various industrial, medical, and research applications due to its gamma-ray emission properties. It is produced as a result of neutron activation of stable cobalt-59 (Co-59) in a nuclear reactor, which subsequently decays with a half-life of 5.27 years into nickel-60 (Ni-60) while emitting two gamma photons with energies of 1.17 MeV and 1.33 MeV [42].

The Co-60 irradiation source utilized for the TID experiments were conducted using a Gammacell 220 Co-60 chamber (Figure 2.4) at the University of Saskatchewan. This chamber is capable of providing an irradiation rate of 108.2 rad(Si) per minute. The designated container for the Device Under Test (DUT) measures approximately 15.2 cm x 20.6 cm. A cable bundle with a diameter of up to 3.5 cm can be accommodated, allowing for the biasing and readout of the electronics being irradiated using external test equipment. A cable length of approximately 1 meter is required for this setup.

Figure 2.4 Gammacell 220 Co-60 Irradiator.

2.3.4 Proton Irradiation Source

Proton beam irradiation sources are an advanced technology that employ accelerated protons to create a highly focused and precise beam of energy. Proton beams share a similarity with heavy ion beams in that they are both monoenergetic, making it convenient to examine the cross-section in relation to LET or energy [41]. The energy levels of proton beams can range from a few MeV to several hundred MeV, which is considerably lower than the highest energy of protons found in space. Nonetheless, for a majority of ICs, the cross-section reaches saturation at around 100 MeV [41]. In this study, experiments are conducted at TRIUMF's Proton Irradiation Facility (PIF) in Vancouver. A schematic representation of the laboratory can be seen in Figure 2.5.

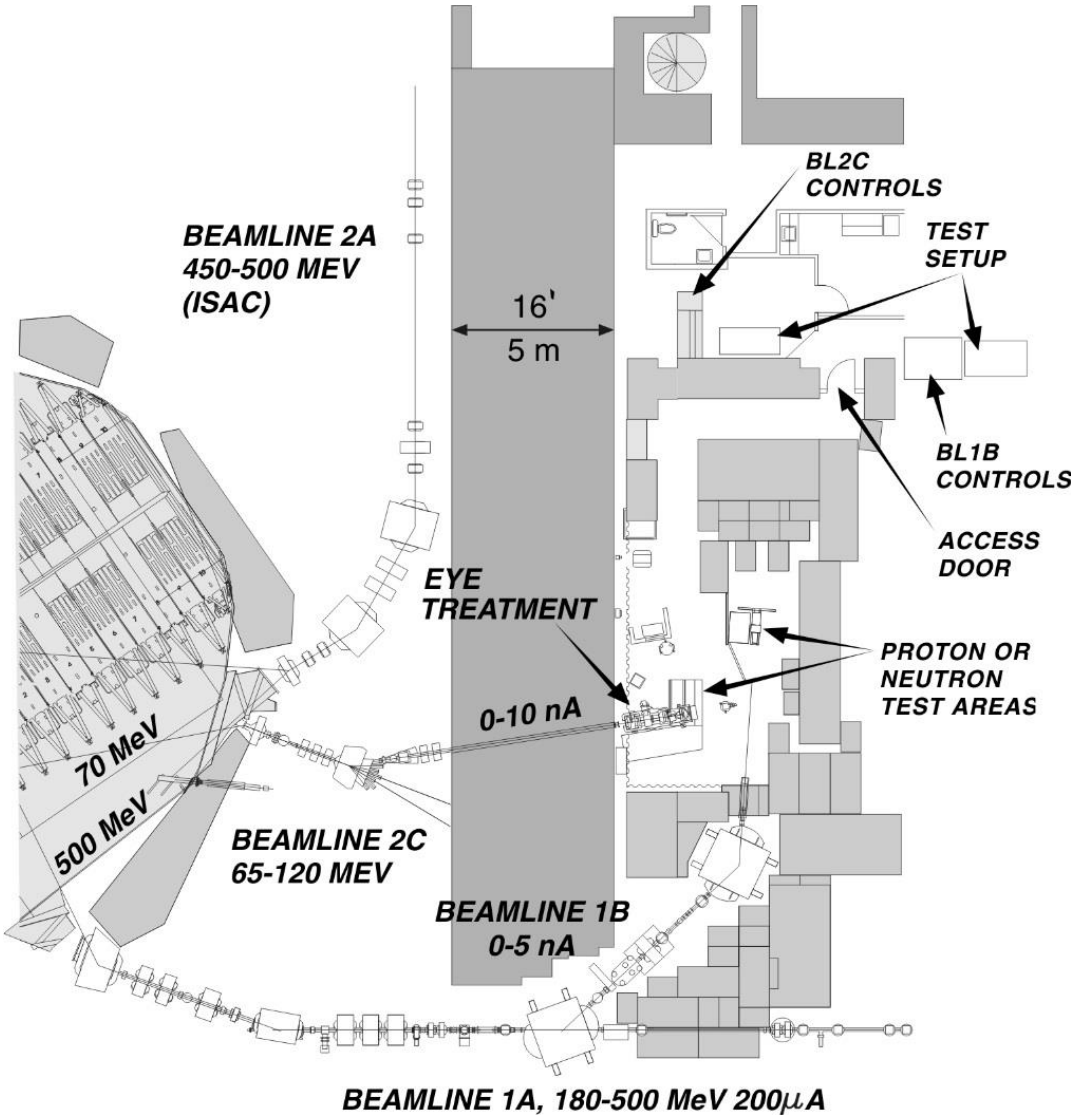

Figure 2.5 Floorplan of the PIF lab at TRIUMF [43].

2.3.5 Laser Irradiation Source

The laser testing mechanism involves the interaction of laser light with silicon, generating electron-hole pairs that produce SET pulses akin to those created by ion impacts. Laser irradiation sources are favored over alternative irradiation methods due to their increased precision and accuracy. They offer detailed spatial and temporal information, allowing for fine control over both time and location. Additionally, laser irradiation sources are a more cost-effective option compared to other methods. Figure 2.6 shows the SPA/TPA Laser System at the University of Saskatchewan.

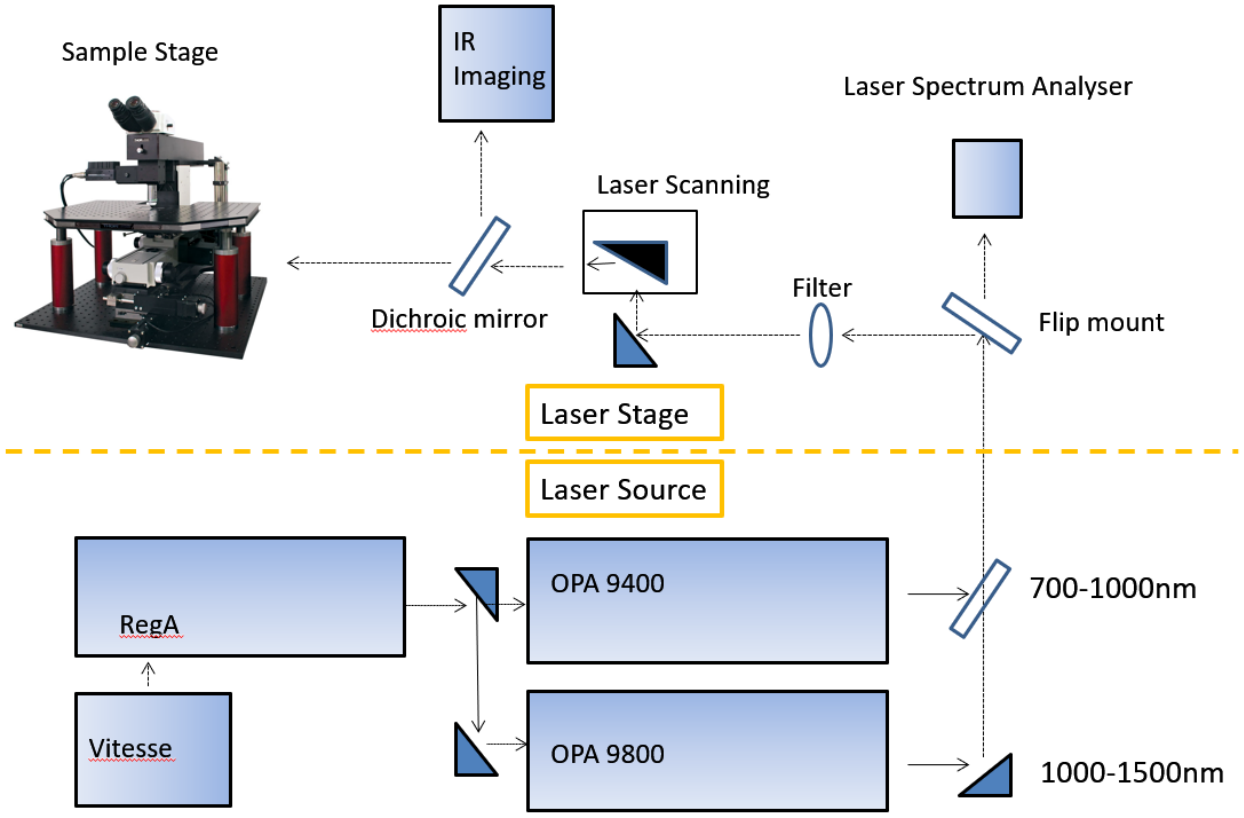

Figure 2.6 SPA/TPA Laser System at the University of Saskatchewan.

2.4 ECC and Hamming Code

ECC plays a crucial role in ensuring the reliable transmission of data through electrical circuits. Researchers have employed various error-detecting methods, such as parity bits and Cyclic Redundancy Checks (CRC) to address electrical error issues in IC design [44-48]. ECC allows for the automatic correction of errors in data transport by adding redundant bits to enhance reliability. Upon receiving the data, the receiver or detection device evaluates it based on the redundant bits. Data stored in memory is highly susceptible to SEEs, making error detection and correction particularly valuable for protecting memory circuits [49].

Hamming code is an error-correcting code that plays a crucial role in the field of digital communication and computer systems, which was introduced by Richard W. Hamming, who was an American mathematician and computer scientist [50]. The Hamming code works on the

principle of parity bits, which are extra bits added to the original data bits to facilitate error detection and correction. In the Hamming code, these parity bits are placed at specific positions, namely the power of 2 (e.g., 1, 2, 4, 8, etc.), within the encoded data [51]. The positioning of the parity bits allows the code to identify and correct single-bit errors that may occur during data transmission or storage [52].

When encoding a data sequence using the Hamming code, the parity bits are calculated based on the data bits in specific groups, which are determined by the position of the parity bit itself. For example, parity bit P1 is responsible for data bits in positions 1, 3, 5, 7, and so on, while parity bit P2 is responsible for data bits in positions 2, 3, 6, 7, and so on [53]. The parity bits are set to either 0 or 1 to ensure an even number of 1's in each group, which is known as even parity.

Upon receiving the encoded data, the receiver evaluates the parity bits for the received data sequence using the same method as the sender. If the calculated parity bits match the received parity bits, the data is assumed to be error-free. However, if there is a mismatch, the receiver can identify the position of the erroneous bit by adding the positions of the incorrect parity bits. Consequently, the receiver can correct the single-bit error and recover the original data.

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3 Efficacy of Transistor Stacking on Flip-Flop SEU Performance at 22-nm FDSOI Node

Contributions of the Author

The results described in this chapter have been published in the following peer-reviewed publication:

Z. Li, C. Elash, C. Jin, L. Chen, S. Wen, R. Fung, J. Xing, S. Shi, Z. Yang and B. Bhuva, "Efficacy of Transistor Stacking on Flip-Flop SEU Performance at 22-nm FDSOI Node," IEEE Transactions on Nuclear Science, vol. 70, no. 4, pp. 596-602, April 2023.

In this project, I contributed to the design of schematics and layouts for the stacked-transistor FFs presented, and took charge of the test chip design in 2020. Additionally, I conducted flip-flop chain simulations and verification. In 2021, Chris and I traveled to TAMU to conduct the heavy-ion experiment, during which we collected the data. Subsequently, I processed the data and collaborated with Dr. Chen and Chris on the analysis. I authored the initial draft of this manuscript and prepared all the figures featured in the published paper. The text and figures presented here were created by me. Furthermore, I presented this research as an oral presentation at the IEEE International Nuclear and Space Radiation Effects Conference (NSREC) held in Provo, UT, in July 2022.

Summary

The stacked-transistor structure is one of the most effective configurations for improving SEU performance in FDSOI technology. This is attributed to the unique design of FDSOI technology, where each transistor resembles an isolated silicon island surrounded by silicon oxide.

As a result, unlike traditional bulk technologies, the stacked-transistor structure in FDSOI technologies can further separate sensitive nodes, enhancing the overall SEU resilience.

This manuscript investigates the effectiveness of the stacked-transistor structure in mitigating Single-Event Upsets (SEUs) at the 22-nm Fully Depleted Silicon-on-Insulator (FDSOI) node through multiple radiation-hardening-by-design (RHBD) D-Flip Flop (DFF) designs. Three stacked-transistor-based DFF designs are presented, including a conventional stacked-transistor DFF design and two hardened stacked-transistor-based DFF designs using layout techniques.

The results show that stacked-transistor DFF designs offer significant improvement in SEU performance compared to conventional DFF designs. Experimental results from heavy-ion irradiations demonstrate a 10x reduction in SEU cross-sections for conventional stacked-transistor designs, and further reductions by using charge-cancelling and interleaving techniques in addition to the stacked-transistor technique. The interleaved-stacked design exhibited the best SE performance, showing zero upsets for all test conditions.

Efficacy of Transistor Stacking on Flip-Flop SEU Performance at 22-nm FDSOI Node

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Abstract

Fully depleted silicon-on-insulator (FDSOI) technology nodes offer better single-event performance compared with comparable bulk technologies. However, upsets are still possible at nanoscale feature sizes and additional hardening techniques need to be explored. Single-event upset (SEU) performance of multiple flip-flop designs using the stacked-transistor hardening technique at a 22-nm FDSOI technology node is presented in this paper. Irradiation results show significant reductions in SEU cross-sections for stacked-transistor-based hardened designs compared to a conventional design. Alpha particle exposures showed zero upsets for all D-Flip-Flop (DFF) designs tested. When exposed to heavy-ions, the stacked-transistor DFF design showed a 17X improvement over a conventional DFF design at an LET value of 47 MeV-cm^2/mg. The stacked-transistor design with the charge-cancelling technique showed upsets when particle LET exceeded 93.8 MeV-cm^2/mg and at a high angle of incidence. The stacked-transistor design with the interleaving technique showed zero upsets for all test conditions.

Index Terms

Flip-flop (FF), fully-depleted silicon-on-insulator (FDSOI), Heavy-Ion, radiation hardening by design, single event upset, soft-error rate, stacked structure.

3.1 Introduction

Radiation particles can produce Single-Event Upsets (SEUs) in nanoscale technologies, which are considered to be a significant reliability issue for modern micro-electronic systems [1 -

6]. Although SEUs are common in space, their presence on the ground has become a major reliability issue at advanced technology nodes [4]. To mitigate this threat, the use of radiation-hardening-by-design (RHBD) techniques is preferred by designers since changes in fabrication processes to improve single-event (SE) performance is not possible. These SEU mitigation techniques can be implemented through manipulating the layout, schematic, or system-level architecture [7,8].

Compared with bulk technologies, Fully-Depleted Silicon-on-Insulator (FDSOI) technologies use a thin Silicon (Si) layer on top of a Buried Oxide (BOX), resulting in excellent gate control over the channel region and reduced nodal capacitances, as shown in Figure 3.1 [9 - 11]. Another benefit of the thin Si layer is reducing the amount of charge collected after an ion strike due to the small active-Si volume [12]. The SE response of bulk technologies suffers from charge collected by multiple transistors in close proximity of a hit transistor, referred to as charge-sharing. For SOI technologies, the threat of charge-sharing through common well or substrate is mostly eliminated due to the isolation of each transistor. Prior work of a regular flip-flop (FF) design at the FDSOI 28-nm node has shown a more than an order of improvement of SEU cross-section over similar designs at a 28-nm bulk technology [1]. However, at nano-scale technologies, the distance between transistors is small enough that the charge cloud generated by a single ion may affect multiple transistors, especially when ions hit said transistors with a large incident angle. Such an enhancement of the charge-collection mechanism along with reductions in critical charge may increase the vulnerability of storage cells at the 22-nm FDSOI technology node [13].

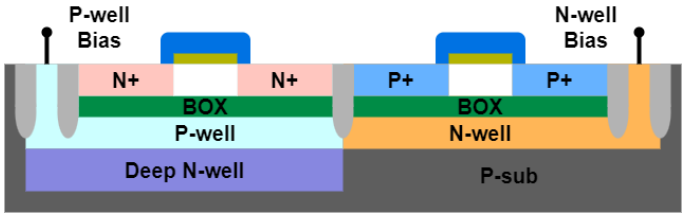

Figure 3.1 22-nm FD SOI transistor cross sections for a regular well configuration.

The stacked-transistor design is effective in reducing SE effects for SOI technologies, ranging from 150-nm to 28-nm nodes [1,12,14-17]. Experimental results from a 45-nm FDSOI technology node showed that the cross-section of a stacked-transistor DFF is more than an order of magnitude smaller than that of the conventional DFF design [14]. Research at a 32-nm FDSOI technology node showed that the stacked-transistor DFF design has better performance than many

other hardening techniques while incurring an area overhead of less than 50% compared to the conventional DFF designs [15]. At the 28-nm FDSOI technology node, the regular stacked-transistor DFF along with two variants utilizing Layout Error-Aware Transistor Positioning (LEAP) techniques were evaluated for SEU performance to show the effectiveness of stacked-transistor technique against SE effects [1]. All stacked-transistor-based DFFs showed zero errors with normal incidence tests up to 50 MeV-cm^2/mg, and had cross-sections at least one order of magnitude lower than the conventional design for angled tests [1]. As the feature size of transistors continues to shrink, the likelihood of SEUs is expected to increase because of the reduced critical charge requirements [18,19]. The performance of similar stacked-transistor designs and other possible techniques (such as interleaving to reduce charge-sharing and charge-cancelling techniques) at the 22-nm FDSOI technology node has not yet been fully evaluated.

This paper evaluates the efficacy of stacked-transistor structure in mitigating SE threats at the 22-nm FDSOI node through multiple RHBD DFF designs. Three stacked-transistor based DFF designs are presented, including a conventional stacked-transistor DFF design and two hardened stacked-transistor based DFF designs using layout techniques.

The first hardened design is a conventional stacked-transistor DFF design similar to what has been done at previous nodes. The second design relocates transistors to enhance charge-cancelling for PMOS and NMOS transistors in the feedback loops of the DFFs [1,20,21]. The third hardened design not only uses the charge-cancelling technique, but also further interleaves the stacked-transistors to avoid them from getting hit simultaneously by a steep incidence angle particle. Results from heavy-ion irradiations show a 10x reduction of SEU cross-section of conventional stacked-transistor designs, and further reductions by using charge-cancelling and interleaving techniques in addition to the stacked-transistor technique.

The rest of the paper is organized as follows: Section II introduces the proposed designs and Section III presents the test chip design and simulation results. Experimental results are presented and in Section IV. The results are analyzed and discussed in Section V before concluding remarks are given in Section VI.

3.2 Stacked-transistor Structure and Latch Designs

3.2.1 DFF

All presented DFF designs in this work used primary and secondary latches with clocked transmission gates, as shown in Figure 3.2 The conventional D-latch design uses inverters and pass gates, as shown in Figure 3.3 The storage node in this design is vulnerable to ion strikes. This conventional D-latch design has the lowest performance penalty and the highest SEU vulnerability.

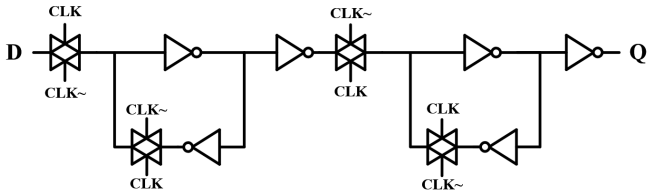

Figure 3.2 The simplified schematic of the primary-secondary DFF.

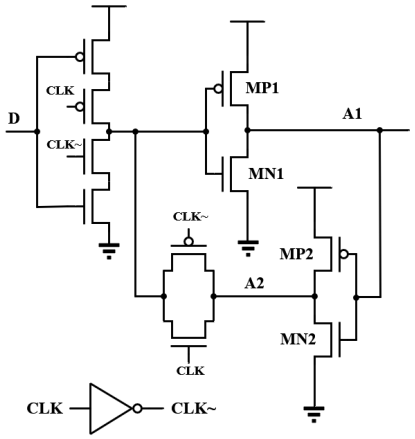

Figure 3.3 Conventional D-Latch design.

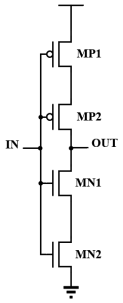

Figure 3.4 Stacked inverter.

3.2.2 Stacked-Transistor DFF

A stacked-transistor inverter splits the PMOS and NMOS transistors into two series-connected transistors, as shown in Figure 3.4. With the same input given to all transistors, either both PMOS or both NMOS transistors are ON or OFF. Assuming both PMOS transistors are OFF, an ion hit on the top transistor (MP1) only affects the intermediate node and will not affect the output node because transistor MP2 is OFF (the output node is isolated and is only controlled by the NMOS transistors). When the drain node of transistor MP2 is hit, the lack of a connection to supply voltage reduces the collected charge, thereby reducing the SE vulnerability. For such an inverter, the output node will experience a voltage perturbation only when both OFF transistors get hit by an ion at a steep incident angle or both transistors collect charge due to charge-sharing [14,15,22,23]. Replacing one or both inverters with stacked-transistor inverters in a conventional D-latch design, as shown in Figure 3.5, will enhance the SEU performance of the latch. Figure 3.6(a) shows the relative position of transistors for a conventional D-latch on a layout. Figure 3.6(b) shows the layout of the stacked-transistor version of the same latch design where each transistor is replaced by two series-connected transistors. The pass gates in all designs are not stacked, which would affect the checkerboard input results. However, the size of the pass transistors is relatively larger than the other transistors to mitigate the effect.

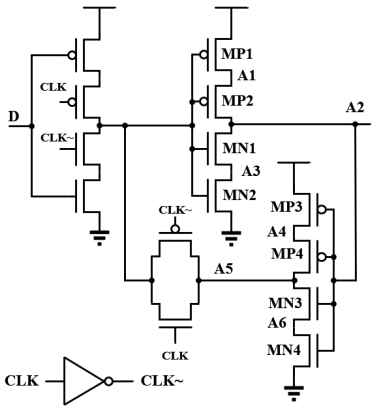

Figure 3.5 D-latch design with stacked inverters.

3.2.3 Charge-cancelling-stacked DFF

The first improvement to the stacked-transistor design is to enhance charge-cancelling (however slight it may be in SOI technologies) to allow both storage nodes to collect charge after an ion hit. When both the sensitive nodes collect charge, they will maintain the voltage differential and reduce the probability of an upset [1]. For instance, when storage node A2 is low and it gets hit by a particle, a positive pulse will be generated, and it will become a negative pulse at node A5 as it passes through the inverter. If these two nodes are placed adjacently, both the nodes will collect the charge and maintain the voltage differential. Figure 3.6(c) shows a layout that employs enhanced charge-cancelling on top of the stacked-transistor design by placing relevant transistors adjacently. Evaluation of SEU performance of these designs will allow designers to understand the extent of charge-sharing at this node. The stacked-transistor DFF designed with this charge-cancelling technique is called charge-cancelling-stacked DFF thereafter in this paper.

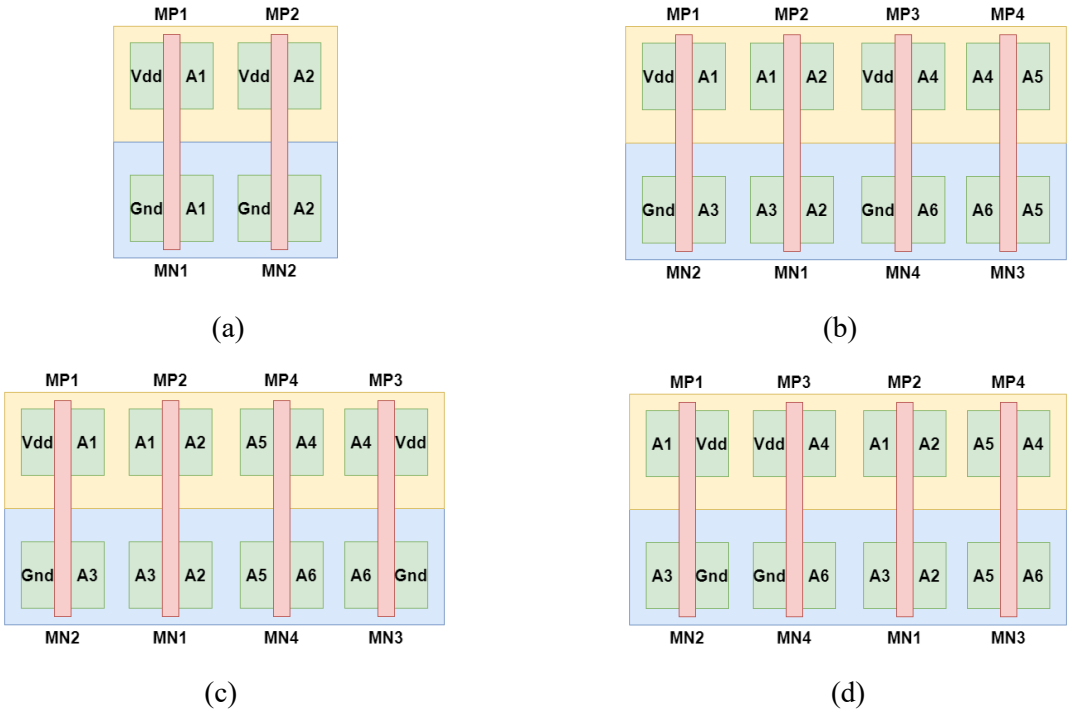

Figure 3.6 Multiple layout designs: (a) Conventional D-latch layout design. (b) Stacked D-latch layout design. (c) Enhanced charge-cancelling with stacked-transistor D-latch layout design. (d) Interleaved-stacked D-latch layout design.

3.2.4 Stacked-Transistor DFF with Interleaving

Despite the presence of the stack construct, its effectiveness will be compromised if the two stacked OFF transistors within an inverter are hit by an ion simultaneously. Therefore, stacked-transistor designs will be vulnerable to angular ion strikes. To mitigate such an effect, layout-based RHBD techniques may be used. For example, stacked-transistors in an inverter may be interleaved in the layout, as shown in Figure 3.6 (d). Such an approach separates the stacked-transistors that share the common input to different locations in the layout to ensure that both the transistors will be hit only if the angle of incidence is very high. The stacked-transistor DFF designed with this interleaving technique is called interleaved-stacked DFF thereafter in this paper. It should be noted that instead of using this interleaving technique itself, it implements both charge-cancelling and interleaving techniques in order to further improve the SEU performance.

3.3 Test Chip Design

A test chip was designed and fabricated in the 22-nm FD-SOI process. Figure 3.7 shows some of the details of the chip-level layout. Four DFF chains, conventional DFF, DFF with stacked-transistors, DFF with enhanced charge-cancelling on top of stacked-transistors, and DFF with interleaving on top of stacked-transistors, were designed with all four D-latch designs

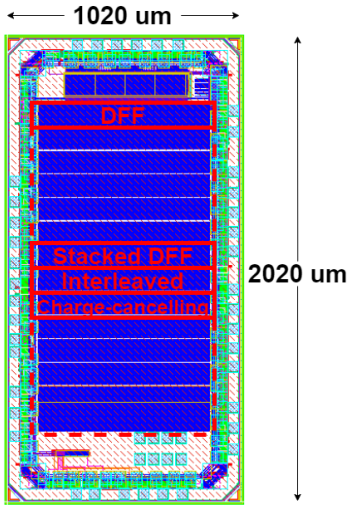

Figure 3.7 Test chip overall layout.

discussed above. The relative positions of each transistor in the layout for each of these designs are shown in Figure 3.6. These DFF circuits were used to design 12,000 stage shift registers with feed-forward data and feed-backward clock signals, as shown in Figure 3.8 [24]. Shift registers were clocked by an external clock signal. All shift registers shared a common input.

The nominal core logic supply voltage for this technology is 0.8 V, and the nominal IO voltage is 1.8 V. All four DFF designs were simulated with the foundry-supplied PDK. Table 3.1 shows the simulated relative performance of each DFF design in terms of power and clock-to-Q delays using the post-layout extracted circuit. The stacked-transistor DFF, charge-cancelling-stacked DFF and interleaved-stacked DFF have the same area as they have the same schematic design and number of transistors. They have about 1.5 times the area of the conventional DFF design because the number of transistors in the inverter in the latch is double due to the stack structure. Compared with the conventional DFF, all stacked-transistor based DFFs have larger power consumption and Clock-to-Q delay. This is because of the parasitic capacitances associated with stacking (increased number of transistors) and separating sensitive transistors (longer interconnects). The placement of the transistors was modified, so the routing became more complicated, which would further increase the power consumption. As the schematic designs for

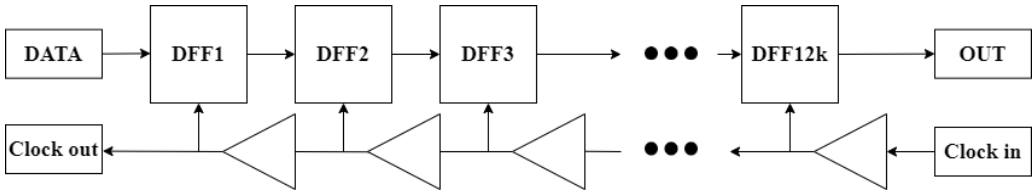

Figure 3.8 Flip-flop chain and the clock data flow for the shift register design.

Table 3.1 Electrical Performance Characteristics for the FF Chains

FF	Average Power (n.u.)	Clk-Q Delay (n.u.)	Overall Area (n.u.)
DFF	1	1	1
Stacked DFF	1.1	1.4	1.5
Charge-cancelling-stacked DFF	1.3	1.5	1.5
Interleaved-stacked DFF	1.4	1.5	1.5

RHBD DFFs are identical, differences in power and Clock-to-Q parameters are due to the different routing interconnects and layout floorplan.

3.4 Experimental Results

3.4.1 Alpha Particle Experiments

Alpha particle irradiation experiments were conducted at the University of Saskatchewan using a disk source including an Americium-241 alpha source with 2.5 μCi activity and 4.61×10^7 a/cm^2/h emissivity. The alpha source was placed above the die of the chip and the distance between the alpha source and the die was less than 8 mm. The testing was conducted with a 1 MHz clock and a core voltage of 0.8 V and 0.6 V with the input to the shift registers at logic 0. Each case was tested for 400 hours. No errors were observed for nominal supply voltages indicating excellent SE performance against low-LET particles of this node.

3.4.2 Heavy Ion Experiments

Heavy ion experiments were conducted at the Texas A&M University (TAMU) Cyclotron Institute using Ne, Ar, Cu, and Ag in 15 MeV/amu cocktail. The experiment setup is shown in Figure 3.9 [10,11]. These particles have the linear energy transfer (LET) values of 2.74, 8.45, 19.7

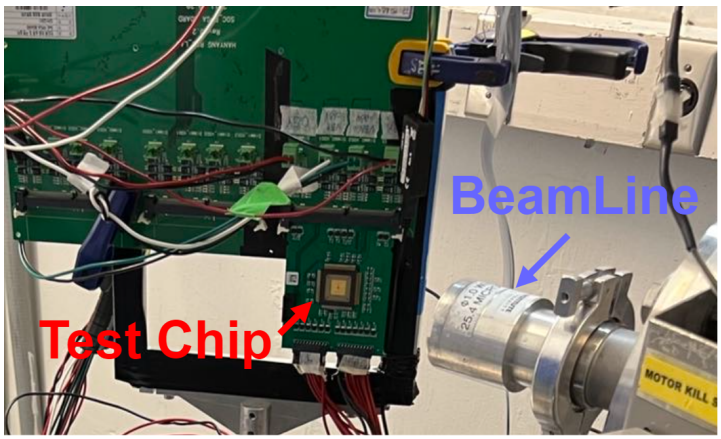

Figure 3.9 Heavy ion experimental setup at Texas A&M University.

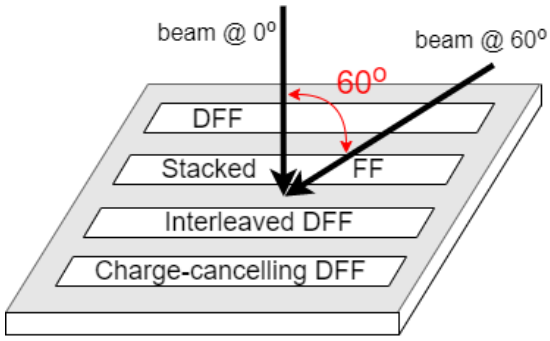

Figure 3.10 Tilt angle used during testing showing the angle of incidence with respect to power lines on the IC. Power lines run left-to-right in the IC.

and 46.9 MeV-cm^2/mg, respectively. Tests were also conducted for a tilt angle of 60˚ from normal. The tilt angle was measured along the east-west axis, as shown in Figure 3.10. All tests were conducted at core voltages of 0.8 V and 0.6 V. The shift registers were clocked at 1 MHz frequency with an input of logic 0. Table 3.2 provides information on the ions used, including the effective LET values for the 60º angle test and the range of ions in the silicon. No vacuum was used during the test and the chip was de-lidded.

The SEU cross-section values of the conventional DFF and the stacked-based hardened DFFs were calculated based on the collected data. The SEU cross section is calculated as:

$$Cross\ Section = \frac{n}{Fluence \times Storage} \tag{3.1}$$

Where n is the total number of SEU, *Fluence* is the effective fluence in the unit of ions/cm^2, and *Storage* is total number of the DFFs in the shift register. The error bar calculation is based on 95% confidence intervals when the number of the events is fewer than 50 [25,26]; when the cross-sections are based on events more than 50, the standard deviation can be calculated with the Normal distribution [27,28]:

Table 3.2 Ions Used in Heavy Ion Experiments

Ion	Effective LET for tilt 0˚ (MeV-cm^2/mg)	Effective LET for tilt 60˚ (MeV-cm^2/mg)	Range (um)
Ne	2.7	5.5	292
Ar	9.5	16.9	212
Cu	19.7	39.4	155
Ag	46.9	93.8	130

$$\frac{2*\sqrt{Events}}{Fluence} \tag{3.2}$$

When there is no SEU, the error number will be assumed to be 1, and the limiting SEU cross section will be calculated as:

$$Cross\ Section = \frac{1}{Fluence \times Storage} \tag{3.3}$$

Figure 3.11 shows the SEU cross-sections of all four designs as a function of particle LET and supply voltage at normal incidence. Results indicate that for low LET particles (< 20 MeV-cm^2/mg), the stacked-transistor DFF cross-section is around 3 orders of magnitude smaller than that of the conventional DFF at nominal VDD (0.8 V). For high LET particles (> 20 MeV-cm^2/mg), its cross-section is about 2 orders of magnitude lower than the conventional DFF. Threshold LET values for the two designs at nominal VDD are approximately 8 and 18 MeV-cm^2/mg, respectively. Reducing the supply voltage to 0.6 V decreases the LET thresholds to 3 and 7 MeV-cm^2/mg, respectively. It should be noted that the saturated SEU cross-section of the conventional DFF is close to the active area of the DFF layout. Compared to the conventional DFF design, the stacked-transistor DFF design showed more than an order of magnitude improvement in saturated SEU cross-section, and more than 2X improvement in LET threshold. Enhanced-charge-cancelling-stacked and stacked-interleaved designs showed zero upsets for normal incidence for both VDD values across the particle LET values tested, indicating superior SE performance.

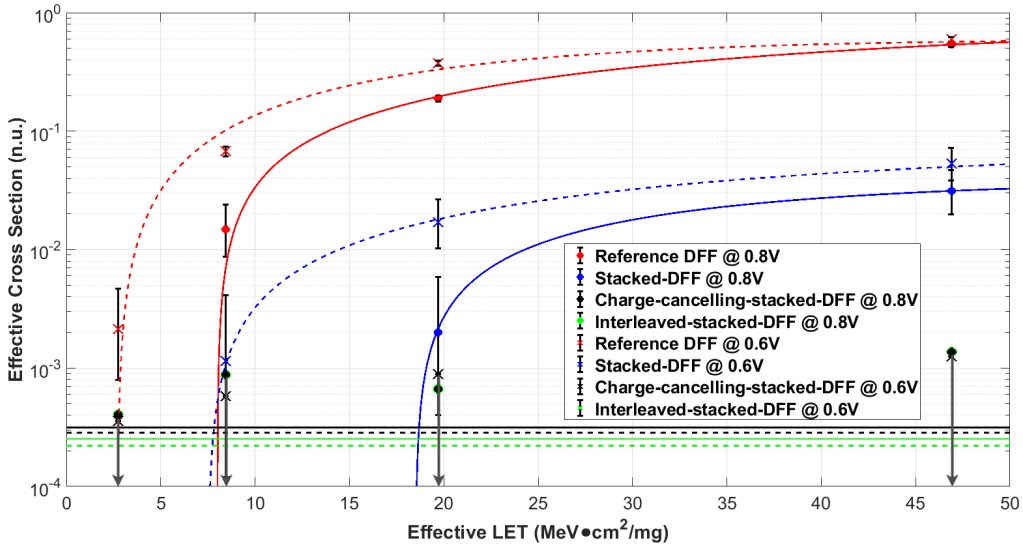

Figure 3.11 FFs' SEU cross-section as a function of LET and voltage at normal incidence.

Results for angular incidence for these designs are shown in Figure 3.12(a), 3.12(b), 3.12(c), and 3.12(d) for conventional DFF design, stacked-transistor design, charge-cancelling-stacked design, and interleaved-stacked design, respectively. The LET value is the effective LET for the cases when the incidence angle is 60˚. The conventional DFF shows a 20% increase in SEU cross-section when angle incidence was varied from normal incidence to 60˚ tilt. The stacked-transistor design showed a 40% increase, indicating increased vulnerability when multiple transistors collect charge after an ion strike at a steep incidence angle. The charge-cancelling-stacked design showed a significant number of upsets, indicating the vulnerability of this technique when the angle of incidence exceeds a threshold value. It should be noted that the charge-cancelling-stacked design showed upsets only for the highest LET particle (47 MeV-cm^2/mg)

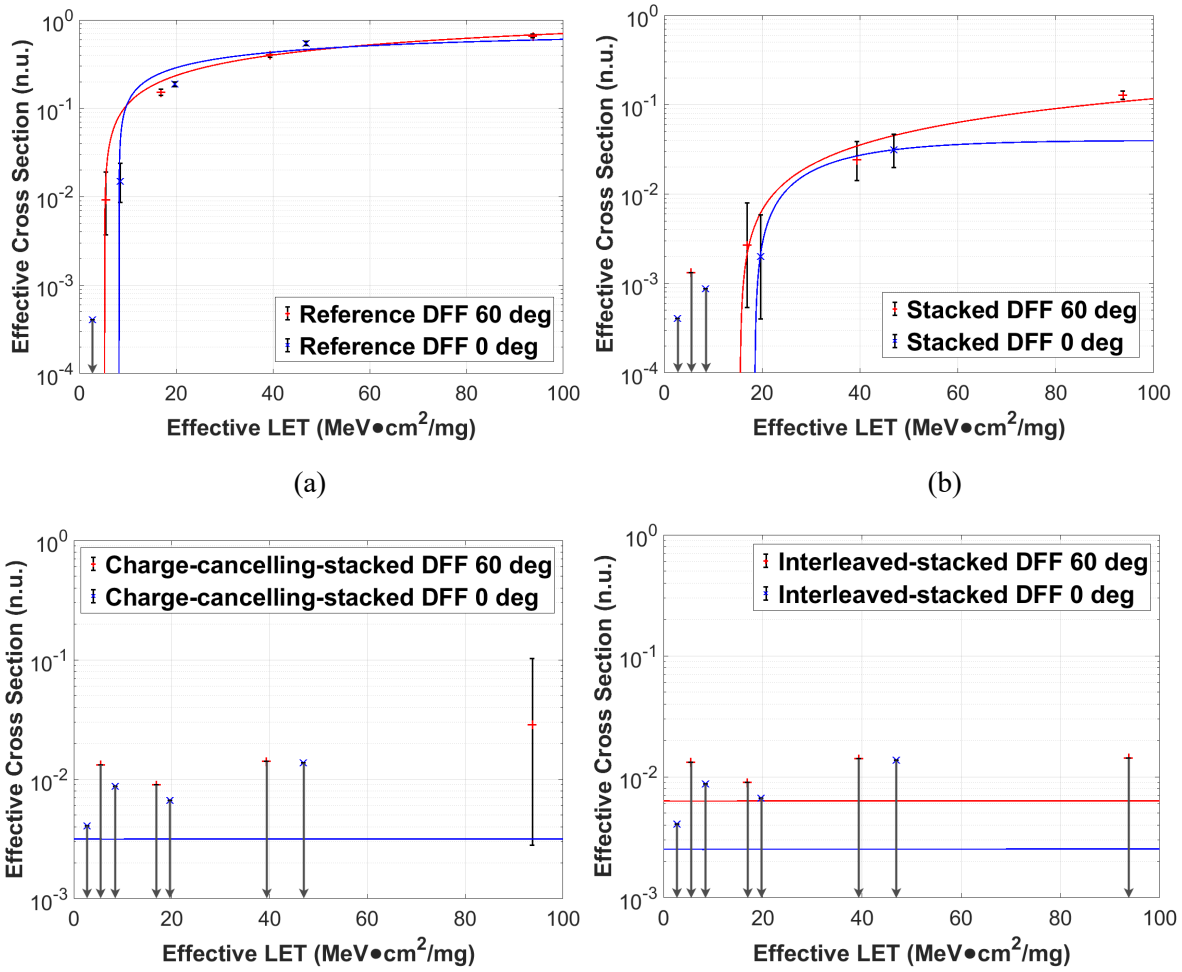

Figure 3.12 SEU Cross-section at normal and 60 ° angle for 0.8 V VDD for (a) conventional DFF, (b) Stacked-transistor DFF, (c) Enhanced-charge-cancelling-stacked DFF, and (d) Interleaved-stacked DFF.

tested at 60˚ tilt incidence. The interleaved-stacked design showed zero upsets for all test conditions presented in this paper, showing excellent performance.

3.5 Discussions

The results show that at the advanced 22-nm FDSOI technology node, the conventional DFF design is vulnerable to SEU even though the collected charge is very small. The reduction in the collected charge due to the thin diffusion layer resulted in a decrease in sensitivity. However, the loop delay was also decreased simultaneously. If the SET pulse is longer than the loop delay, conventional flip-flops can still experience upset. The stacked-transistor DFF shows a significant decrease in SEU cross-section by a factor of ten compared to the conventional DFF design. This improvement is primarily due to the stacking of transistors, as the only difference between the stacked-transistor DFF design and the conventional design is this stacked-transistor structure. This structure prevents the direct path from output to power rails when one transistor is affected by an ion, thus reduces the sensitive areas. While no upset has been observed in the interleaved-stacked DFF design, it has been observed in the regular stacked-transistor design, which suggests that some charge collection by multiple transistors is in close proximity at this node, and it would be the main reason that causes the regular stacked-transistor DFF to have upsets. While at the same time, precautions in the layout design should be made to ensure that there are no other adjacent paths from the output to power rails.

The charge-cancelling-stacked design does further improve the SEU cross-section, but is vulnerable at steep angles with high LET particles, indicating failure of this technique to maintain the voltage differential when collected charge exceeds a certain threshold, and/or charge collection by transistors located in different Si islands (similar to what was observed for stacked-DFF design). The interleaved-stacked design performed the best amongst these four designs, showing zero upsets under all test conditions. For spatially-redundant designs, such as a DICE FF, which requires charge collection by multiple transistors to cause an upset, placing sensitive transistors in a single Si island (for reduced area penalty) may result in charge-sharing and should be avoided. For such designs, interleaving sensitive transistors seems to be the most effective approach for hardening.

Figure 3.13 compares the cross-section curves of the conventional DFF fabricated in different technology nodes, including 22-nm FDSOI technology together with the 65-nm FDSOI [29], 28-nm bulk planar, 20-nm bulk planar [30], and 16-nm bulk FinFET [31]. The SEU cross-section of the 65-nm FDSOI is an order of magnitude higher than that for the 22-nm FDSOI technology. The 22-nm FDSOI design shows around one order of magnitude smaller SEU cross-section than 28-nm bulk planar technology, and around half an order of magnitude smaller SEU cross-section than 20-nm bulk planar and 16-nm bulk FinFET technologies.

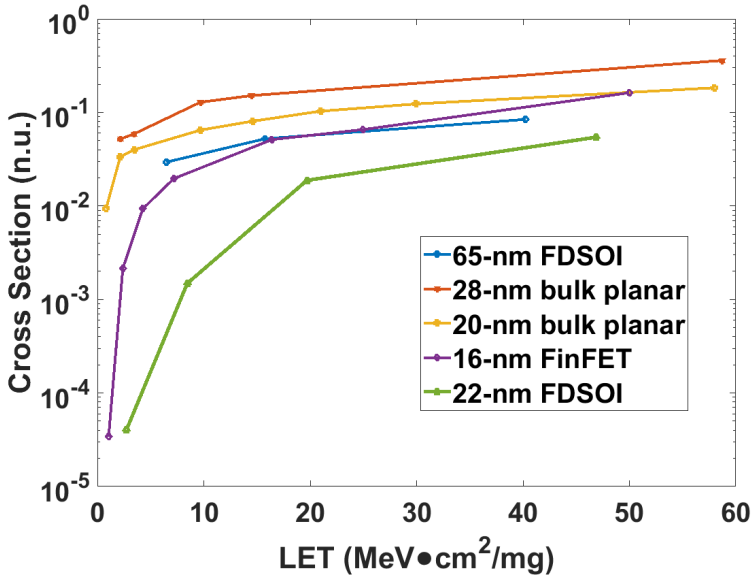

Figure 3.13 SEU cross section comparison among five different technology nodes (28-nm FDSOI, 20-nm bulk CMOS, 28-nm bulk CMOS, 16-nm FinFET, 22-nm FDSOI)

3.6 Conclusions

A conventional D-flip-flop, stacked-transistor flip-flop, charge-cancelling-stacked flip-flop, and interleaved-stacked flip-flop designs have been fabricated at the 22-nm FDSOI technology node and irradiated with alpha particles and heavy-ions for SEU characterization. Results show excellent SEU resilience of the FDSOI process compared to comparable bulk processes. Amongst the four designs presented, the charge-cancelling-stacked design showed upsets only at high LET values and at a high angle of incidence, and the interleaved-stacked design showed zero upsets for all test conditions. The stacked-transistor design shows more than one order improvement in SEU cross-sections over that of the conventional DFF design. These results show

the effectiveness of stacked-transistor designs for FDSOI technology nodes and will help designers apply stacked-transistor techniques to harden customized DFF and logic circuits.

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4 SEU Performance of RHBD Flip-Flops Using Guard-Gates at 22-nm FDSOI Technology Node

Contributions of the Author

The results described in this chapter have been accepted as the following peer-reviewed publication:

Z. Li, C. Elash, C. Jin, L. Chen, S. Wen, R. Fung, J. Xing, S. Shi, Z. Yang and B. Bhuva, "SEU Performance of RHBD Flip-Flops Using Guard-Gates at 22-nm FDSOI Technology Node," IEEE Transactions on Nuclear Science, Accepted on Jun. 07, 2023.

Throughout this project, I participated in designing schematics and layouts for the GG-based FFs and took charge of the test chip design. Additionally, I conducted simulations and verification for flip-flop chains. In 2021, Chris and I visited TAMU to carry out a heavy-ion experiment and gather data. Following this, I processed the data and worked in collaboration with Dr. Chen and Chris on the analysis. I composed the initial draft of the manuscript and created all the figures included in the published paper. Furthermore, I presented this research as an oral presentation at the European Conference on Radiation and its Effects on Components and Systems (RADECS) held in Venice, Italy, in October 2022.

Summary

The guard-gate structure inherently incorporates a stacked-transistor design, which is believed to effectively enhance SEU performance. However, the stacked-transistor structure can only prevent upsets when transistors are individually struck by lower LET particles. By placing a delay element between the two inputs of the stacked-transistor structure, transients with pulse

widths longer than the delay can be filtered out. This configuration, known as the guard-gate structure, offers improved protection against SEUs.

This manuscript investigates the single-event upset (SEU) resilience of flip-flop (FF) designs in 22-nm Fully Depleted Silicon-On-Insulator (FDSOI) technology, focusing on radiation-harden-by-design (RHBD) techniques. The study presents the SE response of several guard-gate (GG) structure-based FF designs, including conventional FF, GG FF with a delay unit, GG-based dual-feedback-recovery (DFR) FF, and GG-based DICE FF. Heavy-ion irradiations demonstrate that GG-FF offers better performance than conventional FF due to the additional delay unit, while DFR and DICE FF designs show no errors up to 92 LET MeV-cm^2/mg with reduced supply voltage and angular incidence.

The findings reveal that FDSOI technology has excellent SEU resilience, and GG-based FF designs provide additional protection against SEUs. The DFR-FF and GG-DICE FF designs exhibit superior SE performance, with no upsets detected at 0.8 V VDD for both incidence angle conditions across various particle LET values tested. TCAD simulations were used to analyze CnRx construct in the GG and DFR designs. Careful layout design in relation to the CnRx construct was found to be crucial for enhancing SE performance, as it can unintentionally create a direct path for charge collection. The proposed changes to the GG-FF layout significantly reduced charge collection at sensitive nodes, resulting in improved SEU resilience.

SEU Performance of RHBD Flip-Flops Using Guard-Gates at 22-nm FDSOI Technology Node

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Abstract

Because of the isolation of transistors, fully-depleted silicon-on-insulator (FDSOI) technology nodes have shown better single-event upset (SEU) resilience compared with bulk technology nodes. Additional radiation-hardening-by-design (RHBD) techniques can further improve the SEU performance. In this paper, SEU performance of multiple RHBD flip-flop (FF) designs using the guard-gate circuit at a 22-nm FDSOI technology is presented, including a conventional FF, a guard-gate (GG) FF, a dual-feedback-recovery (DFR) FF, and a GG-Dual-Interconnected Storage Cell (DICE) FF. Irradiation results showed significant reductions in SEU cross-sections for hardened designs compared to the conventional design. Specifically, the conventional GG design demonstrates more than 100X improvement over a conventional FF design, while DFR and GG-DICE designs showed no upsets for all test conditions. Further analysis was carried out to explain the SEU performance difference between the GG and DFR FF designs, and it is noted that proper layout arrangement is critical for achieving ideal SEU mitigation in this FDSOI technology node.

Index Terms

Flip-flop (FF), fully depleted silicon on insulator (FDSOI), guard-gate structure, radiation hardening by design, single event upset, soft-error rate.

4.1 Introduction

As technology scales down and supply voltage decreases, single-event upsets (SEUs) has been recognized as a significant reliability concern for CMOS technologies [1 - 3]. Some storage

components, such as memory cell arrays, can be protected with error detector codes (ECC) combined with interleaved cell schemes. However, since thousands to millions of flip-flops (FFs) are typically used in very large-scale integration (VLSI) circuit designs, measures must be taken to improve the SEU resilience of FFs. As a result, designers tend to use radiation-harden-by-design (RHBD) techniques to mitigate the SEU threat [4,5].

The SE response of bulk technologies suffers from charge collected by transistors in close proximity of the transistor being hit, which is referred to as charge sharing. In contrast to bulk technologies, Fully-Depleted Silicon-On-Insulator (FDSOI) technologies use a thin Silicon (Si) layer on top of a Buried Oxide (BOX), where each transistor is essentially an insulated thin Si island surrounded by silicon oxide, as shown in Figure 4.1 [6 - 8]. As a result, the threat of charge-sharing is significantly reduced due to the isolation of each transistor. FDSOI technologies also exhibit excellent gate control over the channel region and reduced nodal capacitances [6,9]. Another benefit of the thin Si layer is the reduced amount of charge collected after an ion strike due to the small active-Si volume [4]. Experimental results showed that the SEU performance of a conventional FF design at 28-nm FDSOI node is more than an order of magnitude better than a similar design at 28-nm bulk technology [9]. In addition to these inherent advantages, stacked-transistor design in SOI technologies has shown to be very effective in reducing SE effects at recent technologies, from 150-nm to 28-nm nodes [9 - 14]. Research at 45-nm FDSOI technology showed the cross-section of a stacked-transistor FF is more than an order of magnitude smaller than that of the conventional FF design [11]. However, at nano-scale technologies, the charge cloud generated by a single incident ion may affect multiple transistors due to the small distance between transistors. This enhancement of the charge sharing mechanism and the reduction of the critical charge may increase the vulnerability of designs using stacked-transistors at 22-nm FDSOI technology. As a result, it is important to investigate designs to further improve the stacked-transistor structure at this technology node. Guard-gate (GG) is another common method to mitigate single-event transient (SET) effects in logic circuits, which has two inputs and four transistors to implement the gate [15]. GG-based FF designs essentially use stacked-transistor structure when the two inputs are the same; therefore, it should provide additional protection over SEUs with SOI technologies. Prior work at 65-nm FDSOI technology node has shown multiple GG-based FFs and all of them has different level of SEU improvement compared with the regular FF design [15]. Another design, dual-feedback-recovery (DFR) FF, is based on the GG structure,

but using the primary and secondary latches as the delay elements, which is supposed to further improve the SEU performance [16]. The Dual-Interconnected Storage Cell (DICE) structure has been shown to have excellent SEU performance in many recent technologies [17], so it would also be interesting to evaluate the GG-based DICE structure implemented with FDSOI technology node.

This paper presents SE response of multiple RHBD FFs designed with GG structure at the 22-nm FDSOI technology node. The FF designs include conventional FF, GG FF with a delay unit, GG-based DFR FF, and GG-based DICE FF. Results from heavy-ion irradiations show that the SEU cross-section of GG-FF has superior performance than the conventional FF due to the additional delay unit. DFR and DICE FF designs did not show any errors up to 92 LET MeV-cm^2/mg with reduced supply voltage and angular incidence.

The organization of the rest of this paper is as follows: In Section II, the proposed designs are introduced. In Section III, the test chip design and simulation results are presented. Experimental results are presented in Section IV, and results are discussed in Section V. Finally, conclusions are drawn in Section VI.

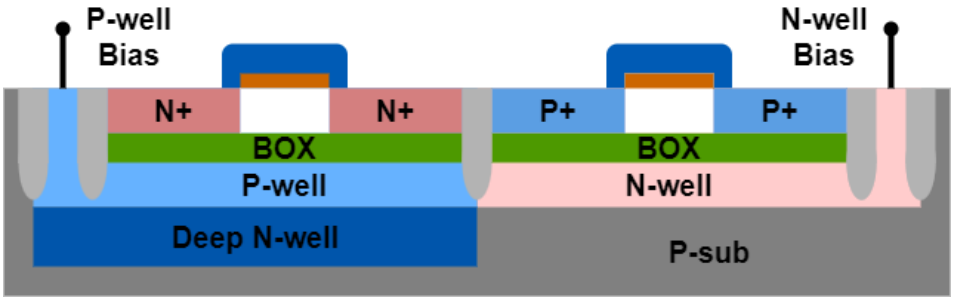


Figure 4.1 22-nm FDSOI transistor cross sections for a regular well configuration.

4.2 GG Structure and FF Designs

A stacked-transistor inverter, shown in Figure 4.2, replaces the PMOS (NMOS) transistor with two series-connected PMOS (NMOS) transistors with gate terminals tied together. In case of an ion hit on an OFF transistor, the connection between the storage node and supply rails does not exist, limiting the amount of charge collected. The reduced charge collection improves the SE performance of designs employing stacked transistors in SOI technologies. For such an inverter,

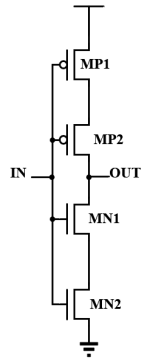


Figure 4.2 Stacked inverter.

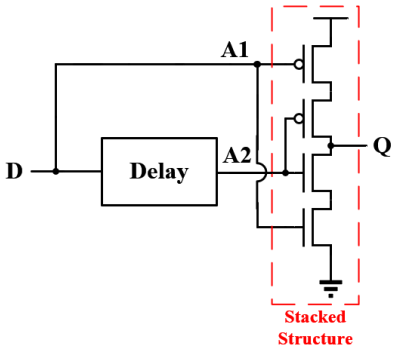


Figure 4.3 GG structure with a delay unit.

the output node will experience significant charge collection only when both OFF transistors get hit by an ion at a steep incident angle, or both transistors collect charge due to charge-sharing [10 - 12,18].

However, the stacked-transistor inverter can only prevent the upsets when the transistors are directly hit by the particles. The use of the stacked transistor cell with gate terminals of PMOS (NMOS) not shorted together has been used to compare two digital signals [19,20]. Such a gate, also referred to as Guard-gate, Mueller gate, TAG, or C-element, has been widely used to harden FF designs by requiring both inputs to match to switch the output of the gate; otherwise, the output will be floating [19]. The GG structure with a delay unit shown in Figure 4.3 can be used to filter out the transient pulses occurs at the input of the stacked-transistor inverter. Depends on the delay being used, certain length of the transient pulses would be eliminated. In this case, the GG structure will further improve the SEU resilience.

4.2.1 Conventional FF

The conventional FF design uses inverters and pass gates, as shown in Figure 4.4. Both the storage nodes in this design are vulnerable to ion strikes. This conventional D-latch design is expected to have the lowest performance penalty and highest SE vulnerability.

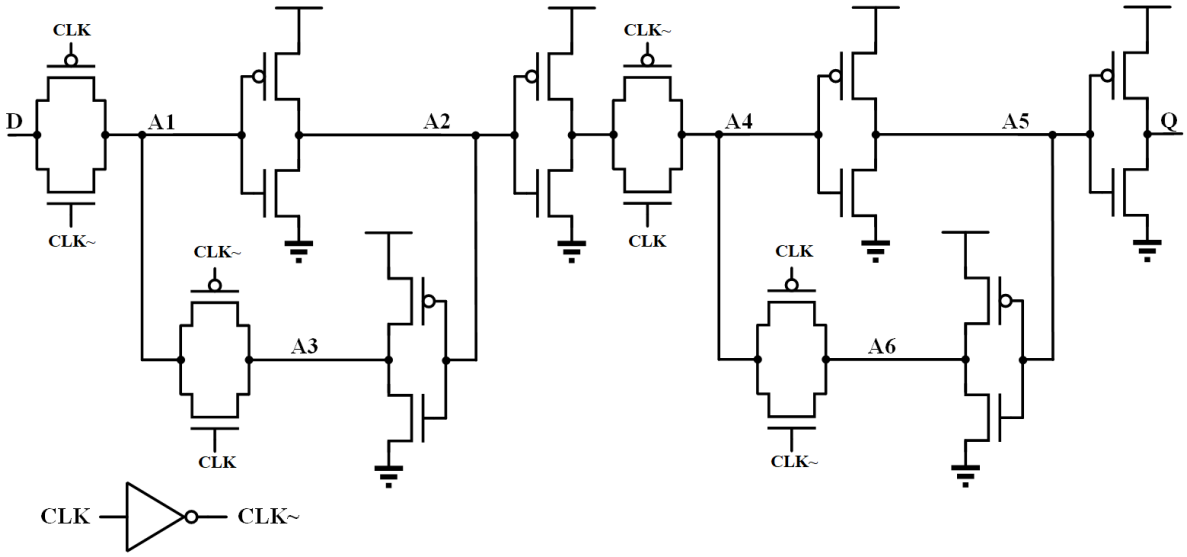


Figure 4.4 Conventional FF design.

4.2.2 GG FF

Figure 4.5 shows the GG-based FF design, where a delay element is used between two inputs of a stacked inverter [20]. For this design, SET pulses will be eliminated if the SET pulse is shorter than the delay element. When the value on node A1 is changed by a SET pulse, the value on node A2 is delayed by two inverter delays. As a result, the guard-gate will keep the previous value if the SET pulse width is shorter than the two-inverter delay. In previous studies at 65-nm FDSOI technology node [15], GG FF design showed excellent SE performance for low-LET particles but became less effective against high-LET particles when SET pulses became longer than the delay.

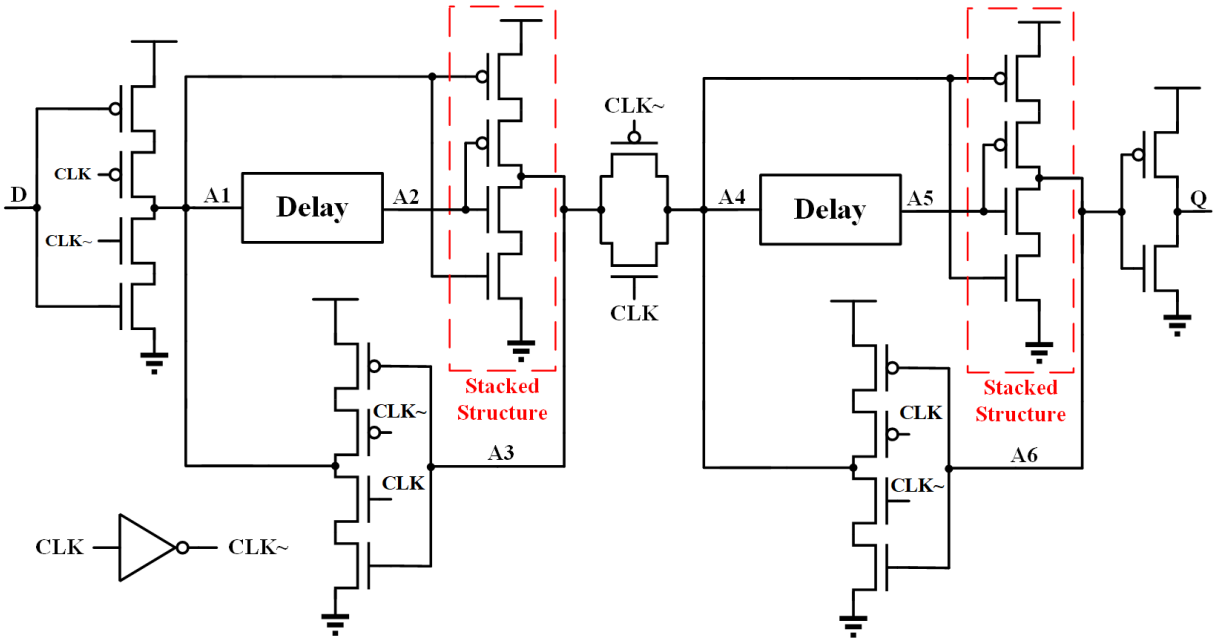


Figure 4.5 GG FF design.

4.2.3 DFR FF

Figure 4.6 shows a GG design based on the DFR technique [16]. A DFR-FF uses GGs and the delay path from the primary and secondary latch without introducing additional delay elements to protect the stored values. There are two guard-gates in the DFR-FF. When CLK = 1, the

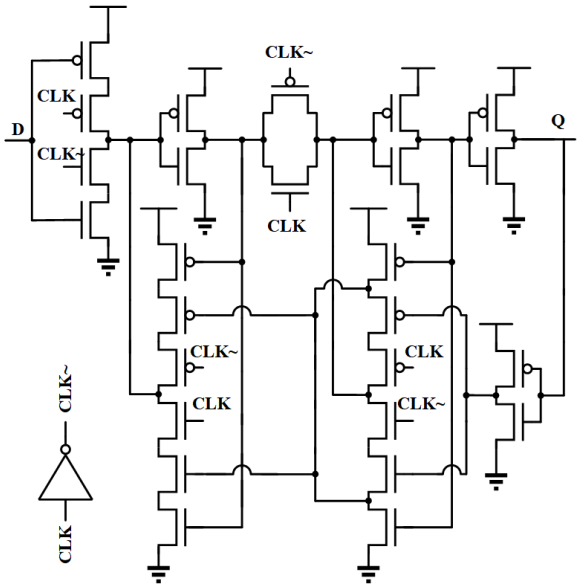


Figure 4.6 DFR FF design.

secondary latch works as a delay element; When CLK = 0, the output and feedback inverters work as a delay element [16]. Previous studies have shown a decrease of 3-5X for DFR-FF over conventional FF for heavy-ion exposures at 65-nm thin BOX FDSOI technology [15, 21]. For this FF layout, stacked transistors were spaced apart by 0.3 um. This distance will effectively prevent these transistors from getting hit by the same particle even with a large incident angle due to the very thin Si regions.

4.2.4 GG-DICE FF

The conventional DICE latch design uses four inverters that are interconnected to store data, as shown in Figure 4.7. The inverters are arranged in such a way that feedback loops within the latch to have a single node upset immunity [21]. However, with the nanometer scale feature sizes in the advanced silicon technologies, the likelihood of charge sharing among sensitive nodes increases, which reduces the effectiveness of the DICE designs [22]. The DICE implemented in the 22-nm FDSOI technology node was designed by replacing each inverter with a stacked-transistor, and is referred to as GG-based DICE FF [20], as shown in Figure 4.8. The two series-connected transistors do not share the same input but are connected to two separate storage nodes storing the same data. This technique can help further prevent a SET pulse from affecting two series-connected transistors simultaneously, since a pulse on one node will only affect one of the transistors in the stacked inverter [23,24].

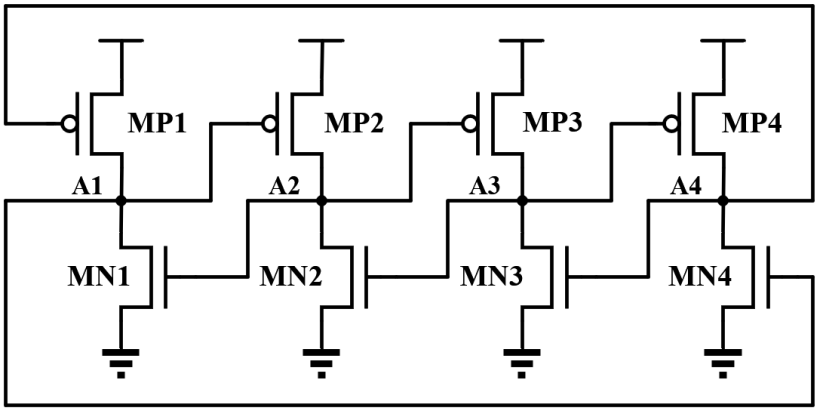


Figure 4.7 Conventional DICE latch design.

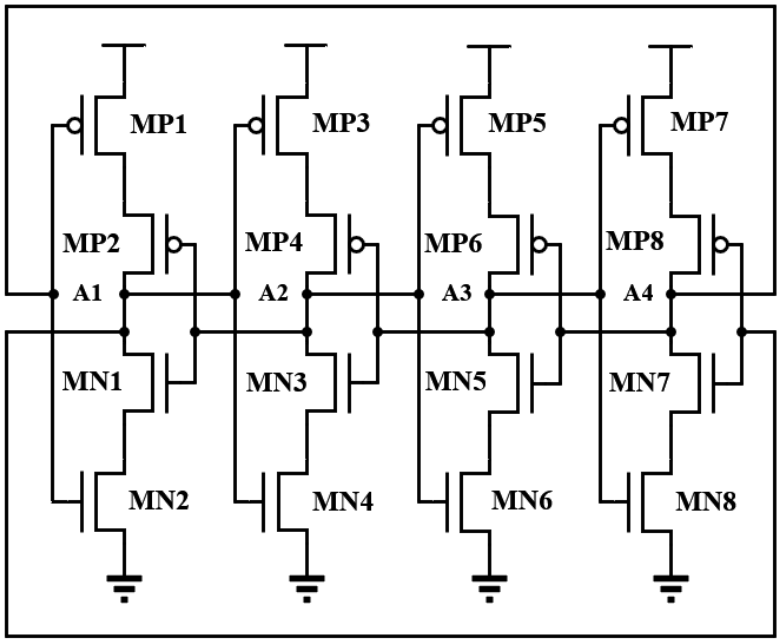


Figure 4.8 GG based DICE latch design.

4.3 Test Chip Design

A test IC containing above FF designs, namely the reference FF, the guard-gate FF (GG FF), dual-feedback-recovery FF (DFR FF), and guard-gate based DICE FF (GG-DICE FF) was fabricated in a commercial 22-nm FDSOI technology with some of the layout details shown in Figure 4.9. The delay circuit for the GG-FF was implemented with a two-inverter chain. The FF

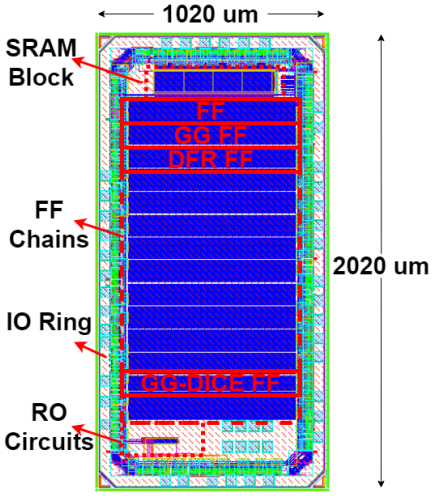


Figure 4.9 Test chip overall layout.

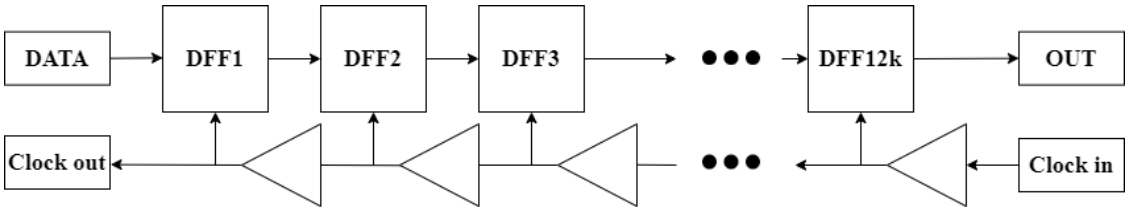


Figure 4.10 Flip-flop chain and the clock data flow for the shift register design.

designs were connected as shift register chains with 12,000 stages. The shift registers are clocked through an external clock signal. A reversed clock scheme is used to provide clock signals to the FFs to avoid hold violations, as shown in Figure 4.10 [25]. All FF chains share the same data input. The outputs of the FF chains are connected to the IO pads for external error detection. The nominal core logic supply voltage for this technology is 0.8 V, and the IO voltage is 1.8 V. Functional verification testing was carried out on the fabricated FF chains with all 0's, 1's and Checker-board (CHB) inputs. Functional tests were carried out before and after each test.

All four FF designs were simulated with the foundry-supplied PDK. Table 4.1 summarizes the overall area, average power, Clk-to-Q delay, and setup time of the aforementioned FF designs. These results were obtained by simulating the post-layout extracted circuits. It must be noted that the timing and power characteristics were not optimized during layout generation. All designs have hold times below zero, so they are not shown in the table. The GG FF design has understandably longer Clk-Q delay and setup time due to the delay unit in the propagation path. The GG designs have better SEU resilience, but with the expense of the timing penalty. Due to the reduced number of transistors used in the DFR FF design, the power consumption of the DFR FF is also reduced compared with the GG FF design. Meanwhile, because the GG structure is moved to the feedback loop, and no additional circuitry is added to implement the structure, the Clk-Q is also greatly reduced for the DFR FF design. As for the DICE-GG FF design, the interconnected structure

Table 4.1 Electrical Performance Characteristics for the FF Chains

FF	Overall Area (n.u.)	Average Power (n.u.)	Clk-Q Delay (n.u.)	Setup Time (n.u.)	Clk Capacitance (n.u.)
Reference FF	1	1	1	1	1
GG-FF	1.7	1.2	2.5	4.2	1.0
DFR-FF	1.3	1.1	1.2	4.7	1.0
GG-DICE FF	1.9	2.5	1.7	2.2	2.0

makes it possible without significant Clk-Q delay penalty. The use of four pass transistors between the primary and secondary latches improve the setup time and Clk-Q delay compared to other designs, but it also results in increased Clk load. Since this DICE-GG FF design has the most transistors, its power consumption is much higher compared to other radiation hardened designs.

4.4 Experimental Details and Results

4.4.1 Alpha Particle Experiments

Alpha particle irradiation experiments were performed at the University of Saskatchewan using a disk source containing Americium-241 alpha source with an activity of 2.5 μCi and an emissivity of 4.61×10^7 a/cm^2/h. The alpha source was placed above the die of the chip with a distance less than 8 mm between the alpha source and the die. The tests were performed with a 1 MHz clock and core voltages of 0.8 V and 0.6 V. Based on 400 hours of testing per chain, no errors were observed in any of the chains, verifying the robustness of the 22-nm FDSOI technology to alpha particles.

4.4.2 Heavy Ion Experiments

Heavy ion experiments were performed at the Texas A&M University (TAMU) Cyclotron Institute using Ne, Ar, Cu, and Ag in 15 MeV/amu cocktail with Linear Energy Transfer (LET) values of 2.74, 8.45, 19.7 and 46.9 MeV-cm^2/mg, respectively. Th e experimental setup is shown

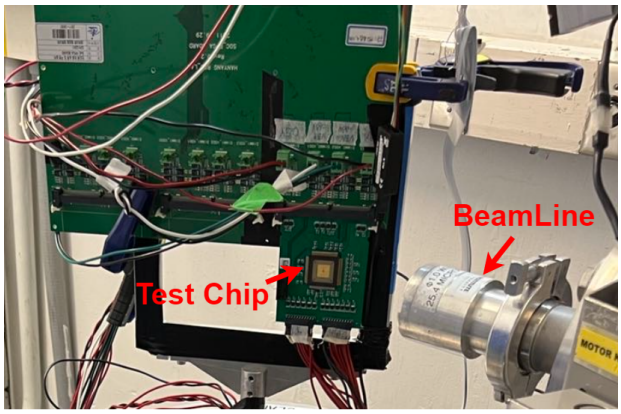


Figure 4.11 Heavy ion experimental setup at Texas A&M University.

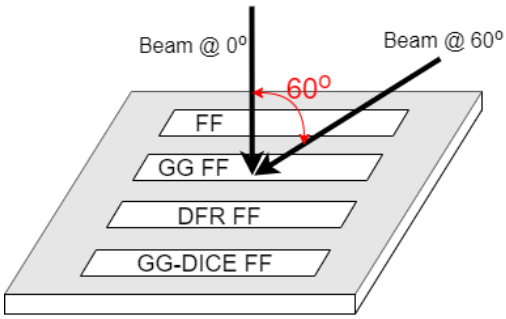


Figure 4.12 Tilt angle used during testing showing the angle of incidence with respect to power lines on the IC. Power lines run left-to-right in the IC.

Table 4.2 Ions Used in Heavy Ion Experiments

Ion	Effective LET for tilt 0˚ (MeV-cm^2/mg)	Effective LET for tilt 60˚ (MeV-cm^2/mg)	Range (um)
Ne	2.7	5.5	292
Ar	9.5	16.9	212
Cu	19.7	39.4	155
Ag	46.9	93.8	130

in Figure 4.11 [7,8]. Tests were also conducted for a tilt angle of 60˚ from normal. The tilt angle was measured along the east-west axis, as shown in Figure 4.12. All tests were conducted at core voltages of 0.8 V and 0.6 V. The shift registers were clocked at 1 MHz frequency with an input of logic 0. Table 4.2 provides information on the ions used, including the effective LET values for the 60º angle test and the range of ions in the silicon. No vacuum was used during the test and the chip was de-lidded.

The SEU cross-section values of the conventional FF and the hardened FFs were calculated based on the collected data. The SEU cross section is calculated as:

$$Cross\ Section = \frac{n}{Fluence \times Storage} \tag{4.1}$$

Where *n* is the total number of SEU, *Fluence* is the effective fluence in the unit of ions/cm^2, and *Storage* is total number of the FFs in the shift register. The error bar calculation is based on 95% confidence intervals when the number of the events is fewer than 50 [26]; when the cross-sections are based on events more than 50, the normal distribution will be used [27]:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}(\frac{x-\mu}{\sigma})^2} \tag{4.2}$$

Where *f(x)* is the probability density function, σ is the standard deviation, and μ is the mean. As a result, the standard deviation can be calculated with the normal distribution [27,28]:

$$\frac{2*\sqrt{Events}}{Fluence} \tag{4.3}$$

When there is no SEU, the error number will be assumed to be 1, and the limiting SEU cross section will be calculated as:

$$Cross\ Section = \frac{1}{Fluence \times Storage} \tag{4.4}$$

Figure 4.13 (a) shows the SEU cross-sections as a function of LET at the normal angle and 0.8 V supply voltage, and Figure 4.13 (b) shows the SEU cross-sections as a function of LET at 60˚ angle and 0.8 V supply voltage. The conventional FF design showed the highest SE cross-section, followed by the conventional GG-FF. At the nominal supply voltage, the GG-FF designs showed around 100X to 400X improvement over conventional FF design. It should be noted that the saturated cross-section of the conventional FF has already reached its maximum value, which is close to the active area of the FF layout. The DFR-FF design and the GG-DICE FF design showed zero upsets for 0.8 V VDD for both incidence angle conditions across the particle LET values tested, indicating superior SE performance.

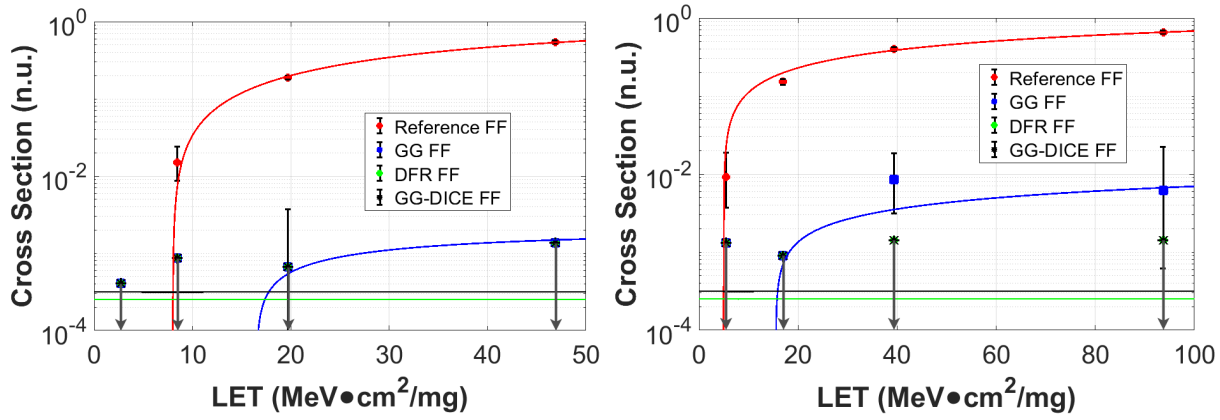


Figure 4.13 (a) SEU Cross-sections at normal angle and 0.8 V VDD. (b) SEU Cross-sections at 60˚ angle and 0.8 V VDD.

Figure 4.14 (a) and (b) show the SEU cross-sections as a function of LET with 0.6 V supply voltage at the normal angle and 60˚ angle, respectively. The overall trends for the 0.6 V results are similar to the 0.8 V results. The conventional FF design still showed the highest SEU cross-section.

At the 0.6 V supply voltage, the GG-FF designs showed around 80X to 150X improvement over the conventional FF design. There was little change in the saturated SE cross-section of FF when the supply voltage was reduced. As the FF SEU cross-section changed little when supply voltage was reduced, the improvement of RHBD designs over FF decreased when supply voltage was reduced. The DFR-FF design and the GG-DICE FF design still showed zero errors.

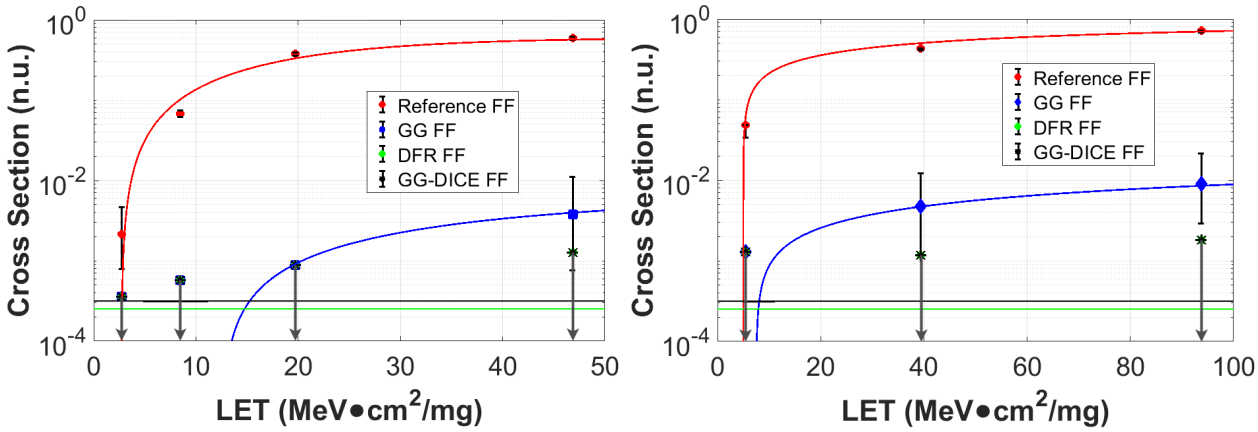


Figure 4.14 (a) SEU Cross-sections at normal angle and 0.6 V VDD. (b) SEU Cross-sections at 60˚ angle and 0.6 V VDD.

4.5 Discussions

4.5.1 SEU Cross-Section Discussions

As the stacked-transistor structure is embedded in the GG structure, the combination of DICE latches and guard gates in the DICE-GG FF results in exceptional SEU performance. This is because the GG structure prevents any upsets in one sensitive node in the DICE structure from propagating to the other sensitive nodes [20]. This structure is especially effective in FDSOI technologies, as transistors are isolated from each other, and guard gates also act as a stacked structure to prevent charge sharing between transistors. As a trade-off, this design involves extra transistors, resulting in large area and power penalties. In practical applications, DICE-GG FF can be used when a high-level tolerance to SEUs is the primary goal, while power and area are less critical.

The GG-FF design showed better SEU performance than the reference FF design, as GG-FF has an additional guard-gate circuit that eliminates SET pulses shorter than the delay (which in this design is equal to the delay of a two-inverter chain). The DFR-FF has a delay element similar to that of the GG-FF design. When CLK = 1, the secondary latch is the delay element, which is composed of two inverters and a transmission gate; when CLK = 0, the output and feedback inverters form the delay element, which has two inverters connected in series. However, DRR-FF exhibited no upset up to 92 LET MeV-cm^2/mg. Further analysis needs to be carried out to explain this phenomenon.

The GG-FF cells were simulated using the TCAD simulator Accuro from Robust Chip Inc. Heavy-ions were used as the particles for simulation, and the LET values were consistent with those in heavy-ion experiments. The schematic of a latch in the GG-FF is redrawn in Figure 4.15 with labeled transistors and nodes. The TCAD simulation heat map revealed that the sensitive areas of upsets occurred between the transistors MP4 and MP5. A portion of the GG-FF layout, and the heat map showing the transistors MP4 and MP5, is shown in Figure 4.16. (a). As shown in the layout, MP4 and MP5 are not two separate diffusion islands; instead, these two PMOS transistors are physically placed in one diffusion block and are electrically separated by a poly connected to VDD. This is due to the new Continuous Active Diffusion (CnRx) layout construct,

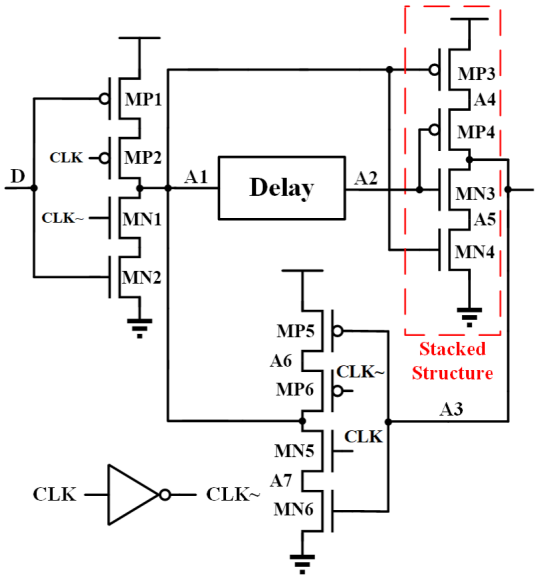
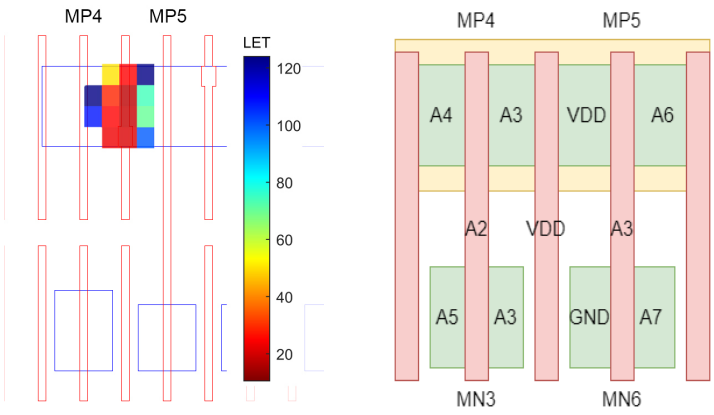


Figure 4.15 GG latch schematic design.



(a) (b)

Figure 4.16 (a) GG design heat map and (b) GG design layout.

which is incorporated into this FDSOI technology node. With the CnRx construct, the active diffusion regions of PEFTs can be implemented continuously within a cell design to improve electrical performance [29, 30]. As previously mentioned, the purpose of the stacked-transistor structure is to separate the direct path from VDD to the output node by using two transistors in series connection. However, due to the CnRx structure, transistors MP4 and MP5 were placed adjacently in the layout with the source of MP5 connected to VDD. Consequently, even with the implementation of the stacked-transistors structure where MP3 and MP4 were positioned together, the source of MP5 provided another direct path for MP4 to VDD.

To address this issue, one solution is to swap the source and drain of MP5 to separate MP4 from VDD, while another is to separate the two transistors, MP4 and MP5, with two silicon islands instead of one using the CnRx construct. A new layout was designed where the two transistors,

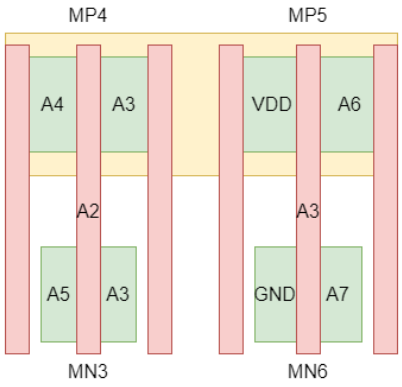


Figure 4.17 New GG design layout with MP4 and MP5 separated.

MP4 and MP5, are placed in two separate diffusion areas, as shown in Figure 4.17. In this case, the TCAD simulation showed that this location is not as sensitive as before.

Another TCAD simulation was carried out to further compare the charge collection at the Drain (A3) of the transistor MP4. Figure 4.18 displays the charge collected at node A3 before and after the layout modification, respectively. It clearly demonstrates that the SET current pulse in the original GG-FF layout design is significantly larger in both magnitude and width. This should be mainly due to the Drain node of MP4 being directly adjacent to the VDD source as discussed previously. The parasitic bipolar effect can significantly increase the charge collection in this case. In addition, the carriers' mobility is significantly increased within the strained PMOS channels due to the CnRx structure. Consequently, at these strained-channel regions, a higher amount of charge could be collected from ion strikes [30].

The layout of DFR-FF was also carefully examined; it is found that the stacked PMOS transistors in the guard gates were placed in different diffusion islands. There is no scenario where the output node of the guard gate is adjacent to VDD or GND. The experimental results also support the conclusions from simulations. It indicates that the guard gate design with the FDSOI technology node could achieve better SEU reduction with careful layout design.

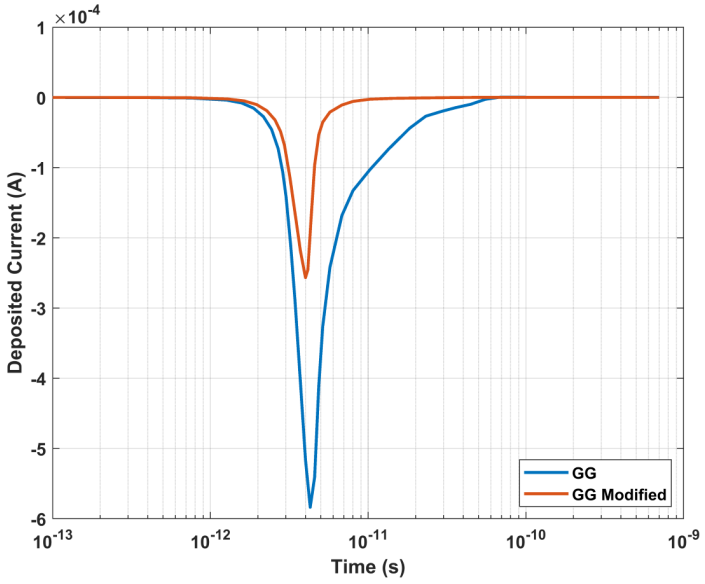


Figure 4.18 Charge collected at the node A3 before and after the modification for a 64 LET ion strike.

4.5.2 Comparing SEU Performance of GG-FF Designs across the Latest Technologies

Figure 4.19 shows the comparison of the conventional FF and GG-FF at three different technologies including 22-nm FDSOI, 16-nm FinFET, and 7-nm FinFET [19]. It should be noted that the 16-nm and 7-nm GG- FF designs also used two inverters as delay elements. The SEU cross-section of the conventional FF at the 22-nm FDSOI technology shows a less than one order of magnitude difference than that of the conventional FF at the 16-nm FinFET technology node. The SEU cross-section of the conventional FF at the 22-nm FDSOI technology is close to that of 7-nm FinFET technology node. However, the GG-FF at the 22-nm FDSOI technology shows much better SEU performance compared with those at the 16-nm and 7-nm FinFET technology nodes. The cross-section of the GG-FF at the 22-nm FDSOI node is around three orders of magnitude less than that at the 16-nm FinFET node, and two orders of magnitude less than that at the 7-nm FinFET node. The stacking transistors in the guard-gate, implemented with the FDSOI technology, certainly play important roles for this difference.

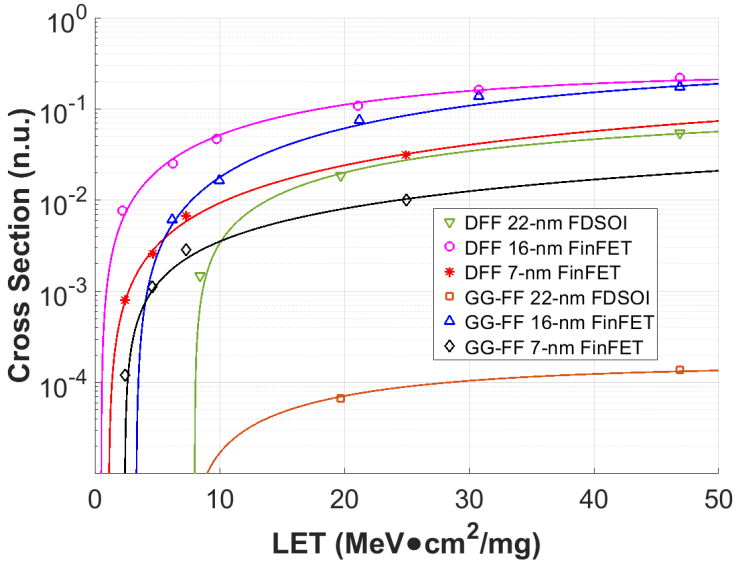


Figure 4.19 SEU cross section comparison of flip flops designed with guard-gate between three different technology nodes (22-nm FDSOI, 16-nm FinFET and 7-nm FinFET).

4.6 Conclusion

A conventional FF, GG-FF, DFR-FF, and GG-based DICE FF designs have been fabricated in the 22-nm FDSOI technology and irradiated with alpha particles and heavy ions for SE characterization. Results showed excellent SE resilience of the FDSOI process. Amongst the five designs presented, the dual-feedback-recovery and GG-based DICE designs showed zero upsets for all test conditions. The conventional GG design demonstrates more than 100X improvement over a conventional FF design at the nominal supply voltage. These results show the effectiveness of the stacked-transistor and GG constructs for FDSOI technology nodes and will help designers apply this design technique to harden customized FF and logic circuits. TCAD simulations were utilized to analyze the GG and DFR layout, revealing an issue in the GG design where one of the stacked-transistors still maintains a path to VDD due to the CnRx layout construct. A critical aspect of improving SE performance was identified to be the careful layout design in the context of the CnRx construct, which can inadvertently create a direct path for charge collection. The proposed modifications to the layout of the GG-FF design demonstrated a significant reduction in charge collection at the sensitive nodes, leading to improved SEU resilience.

Acknowledgment

The authors would like to thank GlobalFoundries for providing silicon fabrication through the 22FDX university program. They would also like to thank the Natural Science and Engineering Research Council of Canada and CMC Microsystems for their support.

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5 SEU Performance of Schmitt-Trigger-based Flip-Flops at the 22-nm FD SOI Technology Node

Contributions of the Author

The results described in this chapter have been published as the following peer-reviewed publication:

Z. Li, C. Elash, C. Jin, L. Chen, S. Wen, R. Fung, J. Xing, S. Shi, Z. Yang and B. Bhuva, "SEU Performance of Schmitt-Trigger-based Flip-Flops at the 22-nm FD SOI Technology Node," Microelectronics Reliability, Volume 146, July 2023, 115033.

Throughout this project, I was involved in designing schematics and layouts for Schmitt-trigger based FFs and took charge of the test chip design. Additionally, I conducted simulations and verification for flip-flop chains. In 2021, Chris and I visited TAMU to carry out a heavy-ion experiment and collect data. Subsequently, I processed the data and collaborated with Dr. Chen and Chris on the analysis. I authored the initial draft of the manuscript and prepared all the figures featured in the published paper. Furthermore, I presented a poster showcasing this research at the IEEE International Nuclear and Space Radiation Effects Conference (NSREC) held in Provo, UT, in July 2022.

Summary

The Schmitt-trigger has two important voltage levels: the upper threshold voltage and the lower threshold voltage. When the input voltage rises above upper threshold voltage, the output switches to a high state. Conversely, when the input voltage falls below the lower threshold voltage, the output switches to a low state. The difference between upper and lower threshold voltage is

called the hysteresis voltage, and it ensures that the output remains stable even if the input signal is noisy or has slow transitions.

With the Schmitt-trigger implemented in a FF, the feedback-loop delay will increase which will prevent SEUs when the transient pulse width is shorter than the feedback loop delay. This would effectively improve the SEU performance.

This manuscript evaluates the SEU performance of three Schmitt-trigger-based DFF designs compared to a conventional DFF design in a 22-nm FD SOI technology. Experimental results, including alpha particle and heavy-ion irradiation tests, show that the Schmitt-trigger-based DFF designs exhibit improved SEU performance compared to the conventional DFF designs. Schmitt-trigger-based FFs have demonstrated SEU cross-section improvements ranging from 2X to 200X over various LET values and supply voltages. Using Schmitt-trigger gates can notably enhance SE performance of DFFs at the 22-nm FD SOI technology node. The ST2 DFF exhibits the best SEU tolerance among the tested designs. These findings will aid designers in achieving performance and SER specifications for circuits intended for radiation environments using this technology node.

SEU Performance of Schmitt-Trigger-based Flip-Flops at the 22-nm FD SOI Technology Node

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Abstract

Compared with bulk technologies, Fully-depleted silicon-on-insulator (FD SOI) technology nodes show better resistance to single-event upsets. However, additional hardening techniques should be investigated to mitigate upsets at this technology node. Single-event (SE) performance of multiple hardened flip-flop (FF) designs based on Schmitt-trigger circuits along with a conventional DFF design in a 22-nm FD SOI process is presented. FF designs were tested using alpha particles and heavy-ions. Results show significant reductions in SEU cross-sections compared with the conventional design. Alpha particle exposures showed zero upsets for all FF designs tested. Schmitt-trigger-based FF designs showed from 2X to 200X improvement in heavy-ion SEU cross-sections compared with the conventional DFF design.

Index Terms

Flip-flop (FF), fully depleted silicon on insulator (FD SOI), Heavy-Ion, radiation hardening by design, single event upset, soft-error rate, Schmitt-trigger.

5.1 INTRODUCTION

Radiation-induced soft errors have become a significant reliability issue for aerospace and high-performance super computers [1]. An incident ion traversing a semiconductor region has the potential to generate a single-event transient (SET) pulse at the output node of a logic gate. This SET pulse can lead to a single-event upset (SEU) [2]. An SEU may occur if the SET takes place within a storage cell or if a logic circuit produces an SET that is subsequently followed by a register or another storage element, as the latter may capture the SET as an SEU error. SEUs result from

bit value flips in storage elements, such as flip-flops (FFs) or Static Random Access Memories (SRAMs), when they are impacted by ionizing particles [2].

Transistors in the latest Fully-Depleted Silicon-on-Insulator (FD SOI) technologies are fabricated on a very thin silicon (Si) layer over a buried oxide layer, as shown in Figure 5.1 [3 - 5]. With each transistor fabricated on a Si island (isolated from other transistors by insulators), the volume of active Si is very small for each transistor. This allows for superior gate control over the channel region while reducing nodal capacitances, yielding faster logic gate switching times over those for bulk technologies [6]. A side benefit of this technology is that the charge collection volumes after an ion strike are very small due to ultra-thin diffusion regions, making single-event transient (SET) pulses generated due to an ion strike very short. Usually, shorter SET pulses will improve the single-event (SE) performance of FF circuits [7,8]. However, for a latch design, to a first degree, an upset will occur when the SET pulse width is longer than the feedback-loop delay. With reduced nodal capacitances, FD SOI technology yields shorter logic gate delays than bulk technologies, resulting in shorter feedback-loop delays for storage cells. As a result, DFF designs at FD SOI technologies do experience upsets even though the collected charge is significantly reduced compared to bulk technologies. For critical applications requiring extremely low SEU error rates, Radiation Hardened by Design (RHBD) methodologies must be used to further improve the radiation tolerance of FF designs fabricated at this technology node to meet the design specifications.

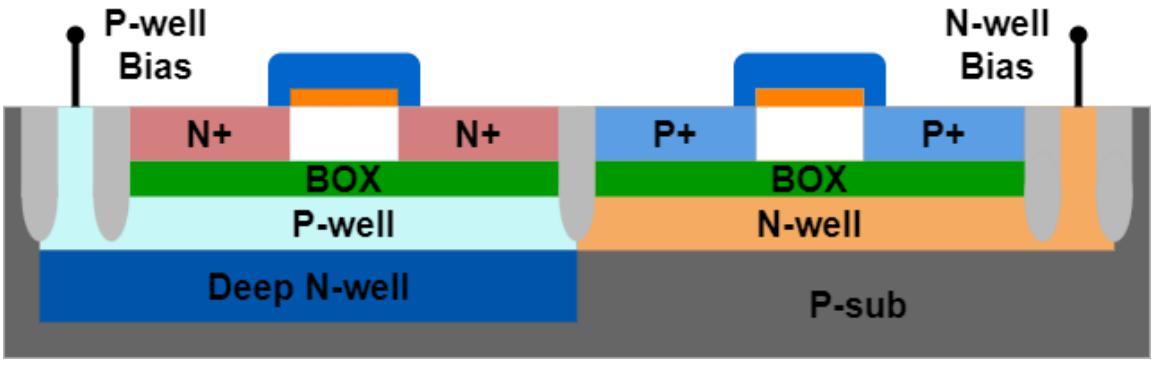


Figure 5.1 22-nm FD SOI transistor cross-sections for a regular well configuration.

Since SET pulse width is a strong function of fabrication process parameters, designers need to increase the feedback-loop delay to improve the SE performance of DFF designs. Designers can shorten the SET pulse width by increasing the transistor sizes. However, the

associated power penalty limits the use of this technique, leaving designers with increasing the feedback-loop delay as the major RHBD option for improving the SE performance of FF cells. Designers have a multitude of ways to increase the logic gate delay, each with an associated performance penalty. One of the techniques for increasing the feedback-loop delay is to replace inverters in a conventional DFF design with Schmitt-trigger gates. The Schmitt-trigger logic gate only switches the output when the input voltage changes beyond a threshold value [9]. As a result, Schmitt-trigger is commonly used to eliminate the noise in signals [10]. When Schmitt-trigger logic gates are used to make a latch, the requirement that the input must pass a threshold value to affect the output essentially increases the feedback-loop delay of the latch (or requires a larger voltage swing at the input to initiate a transition on the output node). This improves the SE performance of the latch with an acceptable performance penalty, making it one of the most attractive techniques for hardening DFF designs.

There are already some experimental results showing exceptional SEU performance for the Schmitt-trigger-based DFF designs. Experimental results for the 65-nm CMOS technology showed the SEU cross-section of a Schmitt-trigger-based DFF around an order of magnitude lower than the conventional DFF [11]. Experimental results for the 16-nm Bulk FinFET CMOS technology showed that SEU cross-section for heavy-ion exposures had an improvement of up to ~30× for Schmitt-trigger-based DFF over a conventional DFF at nominal supply voltage and room temperature [12].

This paper evaluates the SE performance of three Schmitt-trigger-based DFF designs along with a conventional DFF fabricated in a 22-nm FD SOI technology. Alpha particles and heavy-ion irradiation experiments were conducted to evaluate the SEU performance of all the designs. Results clearly show the improved performance of Schmitt-trigger-based DFF designs over conventional DFF designs in terms of SEU rates.

The organization of the rest of this paper is as follows: In Section II, the proposed designs are introduced. In Section III, the test chip design and simulation results are presented. Experimental results are presented in Section IV, and results are analyzed and discussed in Section V. Finally, conclusions are drawn in Section VI.

5.2 Schmitt-Trigger DFF Designs

5.2.1 DFF Design

As shown in Figure 5.2, all FF designs presented in this work use primary and secondary latches with clocked transmission gates. Inverters and pass gates are used in the conventional D-latch design, as shown in Figure 5.3. The storage nodes in this design are vulnerable to ion strikes due to very low critical charge. This conventional D-latch design has the lowest performance penalty and the highest SE vulnerability.

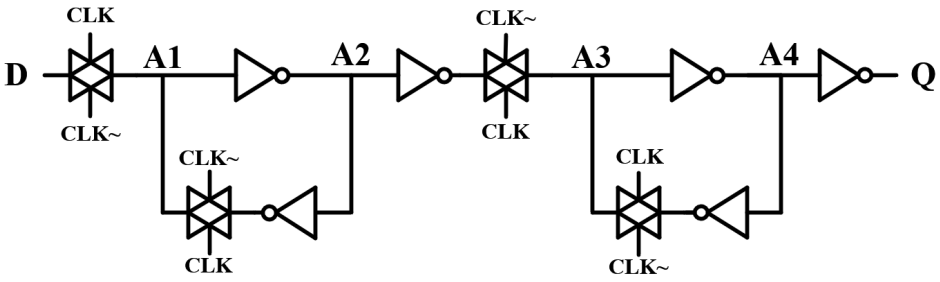


Figure 5.2 The simplified schematic of the primary-secondary DFF.

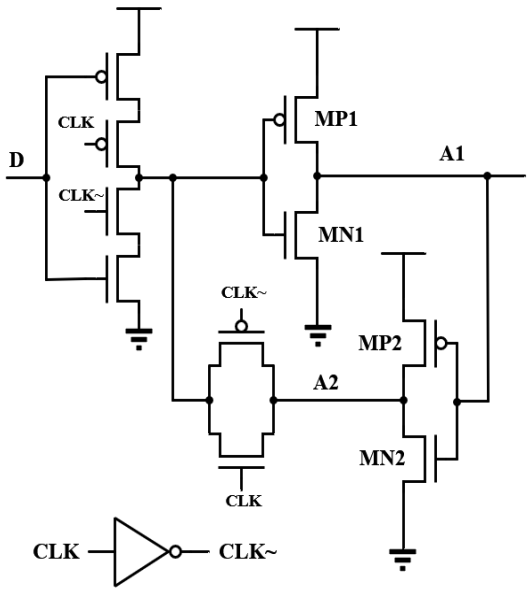


Figure 5.3 Conventional D Latch design.

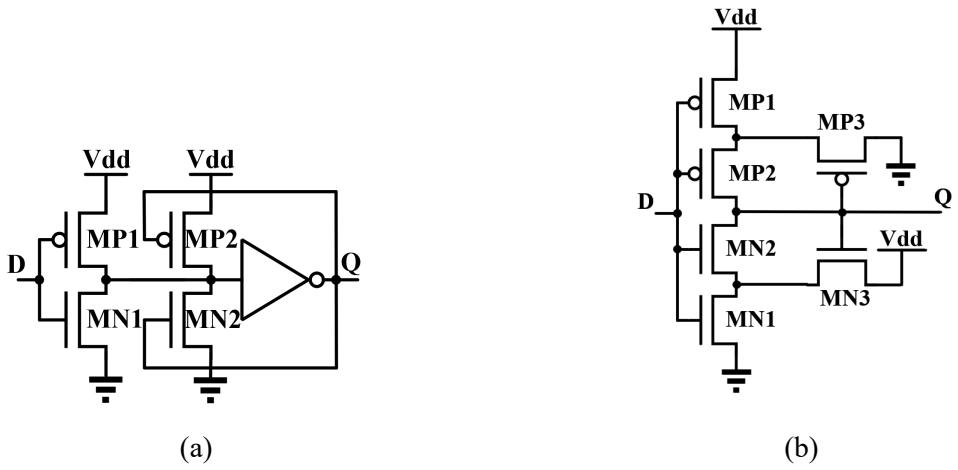
5.2.2 Schmitt-Trigger Designs

There are two conventional Schmitt-trigger designs used by designers, as shown in Figure 5.4 [13, 14]. For the design shown in Figure 5.4(a), the pull-up (MP2) and pull-down (MN2) transistors oppose the currents from MN1 and MP1, respectively, to increase the switching threshold. The switching thresholds are determined by $k_{MN1}/(k_{MP1}+k_{MP2})$ and $(k_{MN1}+k_{MN2})/k_{MP1}$, respectively, where k is the gain factor, which is proportional to the transistor width [13]. The second Schmitt-trigger gate design is shown in Figure 5.4(b) [14]. For this circuit, transistor MP3 (or MN3) opposes the switching currents passing through MP1 and MP2 (or MN1 and MN2) to resist Low-to-High (or High-to-Low) transition. The switching thresholds are determined by the sizing ratio between transistor MN1 and MN3, or MP1 and MP3, and the exact low-to-high threshold, V_{Th01}, and high-to-low threshold, V_{Th10}, can be calculated by equations (1) and (2).

$$V_{Th01} = \frac{V_{DD}+V_{ThN}\sqrt{\frac{k_{MN1}}{k_{MN3}}}}{1+\sqrt{\frac{k_{MN1}}{k_{MN3}}}}, \tag{5.1}$$

$$V_{Th10} = \frac{V_{DD}-|V_{ThP}|\sqrt{\frac{k_{MP1}}{k_{MP3}}}}{1+\sqrt{\frac{k_{MP1}}{k_{MP3}}}}, \tag{5.2}$$

$$k_i = \frac{1}{2}\mu C_{ox}\frac{W_i}{L_i}, \tag{5.3}$$



(a) (b)

Figure 5.4 (a) The first type of the Schmitt-trigger design. (b) The second type of the Schmitt-trigger design.

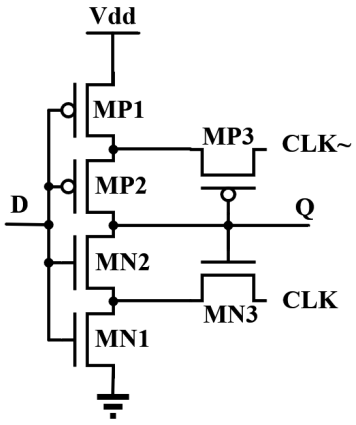


Figure 5.5 A variation of the second Schmitt-trigger.

Here k_i is the gain factor, which is a factor proportional to transistor width [15]. V_{ThN} and V_{ThP} represent NMOS and PMOS threshold voltages, respectively [14].

A variation of the second Schmitt-trigger circuit is shown in Figure 5.5, where transistors MP3 and MN3 are connected to CLK_bar and CLK signals, respectively, instead of Ground and supply voltage (VDD) [11]. Such a design provides better performance by disengaging the transistors associated with the Schmitt-trigger function during the write operation and pre-charging the intermediate nodes for faster response time. These circuits have been successfully used in many applications for increasing the switching threshold to remove noise from digital and analog signals [10]. Increasing the switching threshold has the undesirable side effect of larger gate delays for noise-removal applications, however increasing the gate delay will increase the feedback-loop delay of a latch designed with Schmitt-trigger gates, thereby improving the SE performance.

5.2.3 ST1 Schmitt-Trigger-Based DFF

Figure 5.6 shows a DFF design (termed as ST1) where the conventional DFF latch inverters are replaced by the first Schmitt-trigger gate. Replacing both the inverters with the Schmitt-trigger gate increases the feedback-loop delay further with associated improvement in SE response (and increases in performance penalty).

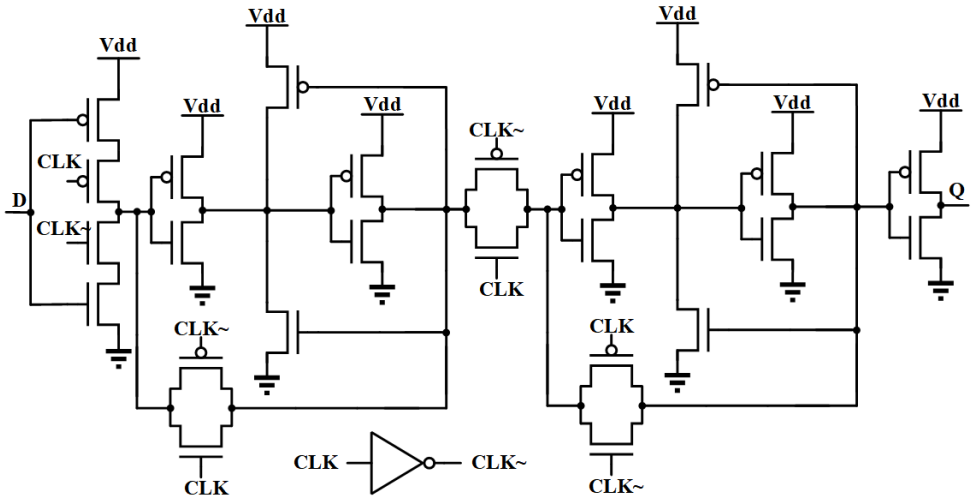


Figure 5.6 ST1 DFF schematic based on the first type of the Schmitt-trigger design where only one inverter is replaced by a Schmitt-trigger.

5.2.4 ST2 Schmitt-Trigger-Based DFF

Figure 5.7 shows a DFF design (termed as ST2) using the variation of the second Schmitt-trigger design. As mentioned before, during the write mode, no current will pass through MP3 and MN3. This structure disengages the direct path of the Schmitt-trigger in write mode and restricts the delay penalty as a result of the off-centered threshold voltage [11]. During the hold operation, the critical charge can be increased by pulling up the sources of MN3 and MN6 and pulling down

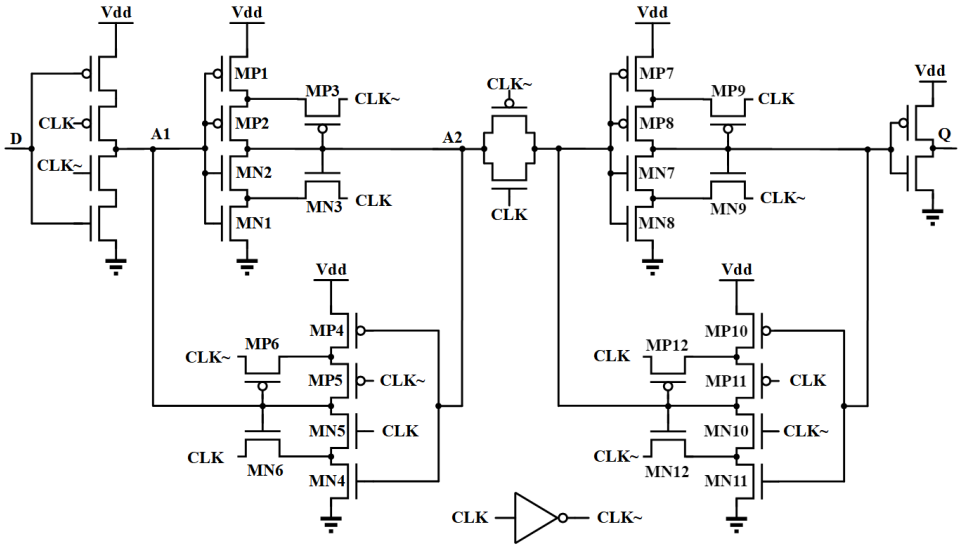


Figure 5.7 ST2 DFF schematic based on the variation of the second type of the Schmitt-trigger design.

the sources of MP3 and MP6. In addition, when the positive or negative transient is generated on node A2, the corresponding MN4 or MP4 transistor will be switched on [11]. This will pull down the CLK signal or pull up the CLK~ signal, which can turn off the transistor MN5 and MP5, respectively, and avoid a potential upset. It has been proven that this architecture has 3X improvement in SER compared to a conventional DFF design at a 65-nm bulk CMOS technology [11].

5.2.5 Schmitt-Trigger-Based DFR DFF

Additional feedback-loop delay can be added when using the guard-gate (or C-element) in the feedback-loop, which can be beneficial to combine it together with Schmitt-trigger. Guard-gate is a logic gate where each transistor in an inverter is split into two serially connected transistors with the input to one PMOS and NMOS pair delayed, as shown in Figure 5.8 [16,17]. In the presence of a SET pulse shorter than the delay, the output will not change until both inputs match. In essence, such a gate eliminates SET pulses shorter than the delay element shown in

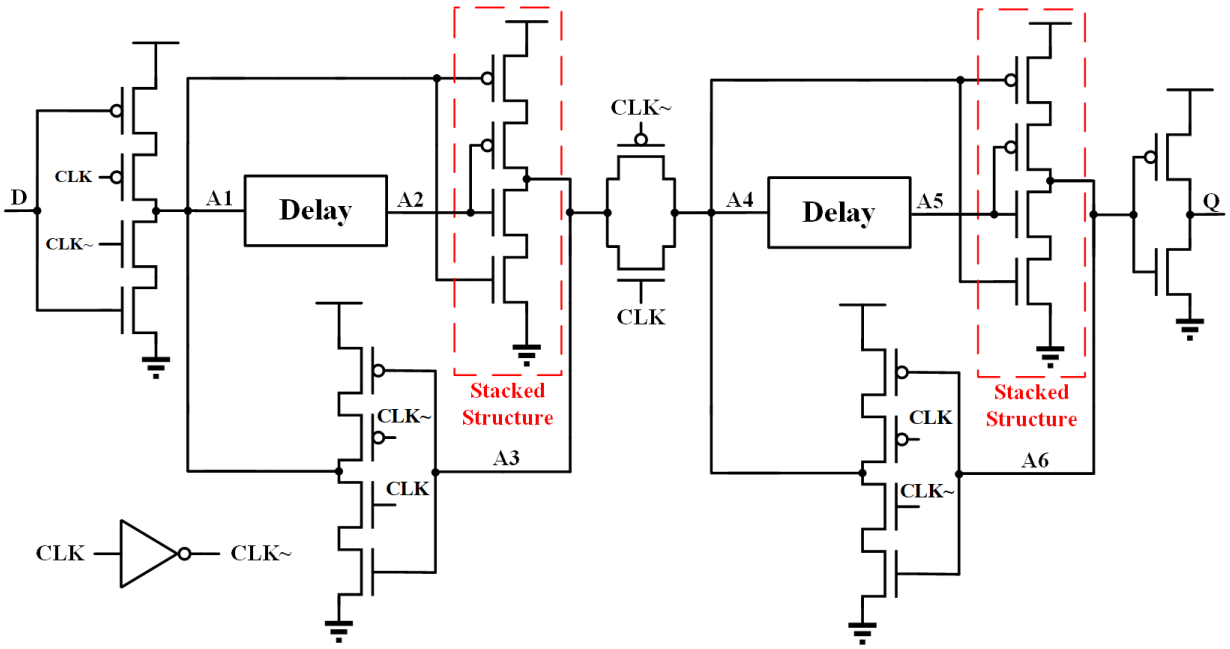


Figure 5.8 Guard-gate-based latch design where an inverter is replaced by a guard-gate along with the delay circuit.

Figure 5.8. A dual feedback recovery (DFR) based DFF uses guard-gates and the delay path from the primary and secondary latches without introducing additional delay elements to protect the stored values [18], as shown in Figure 5.9. There are two guard gates in the DFR-FF. When CLK

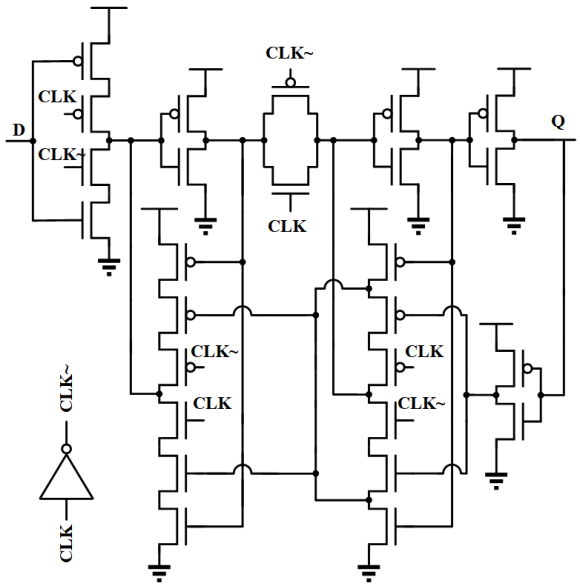


Figure 5.9 DFR-FF design.

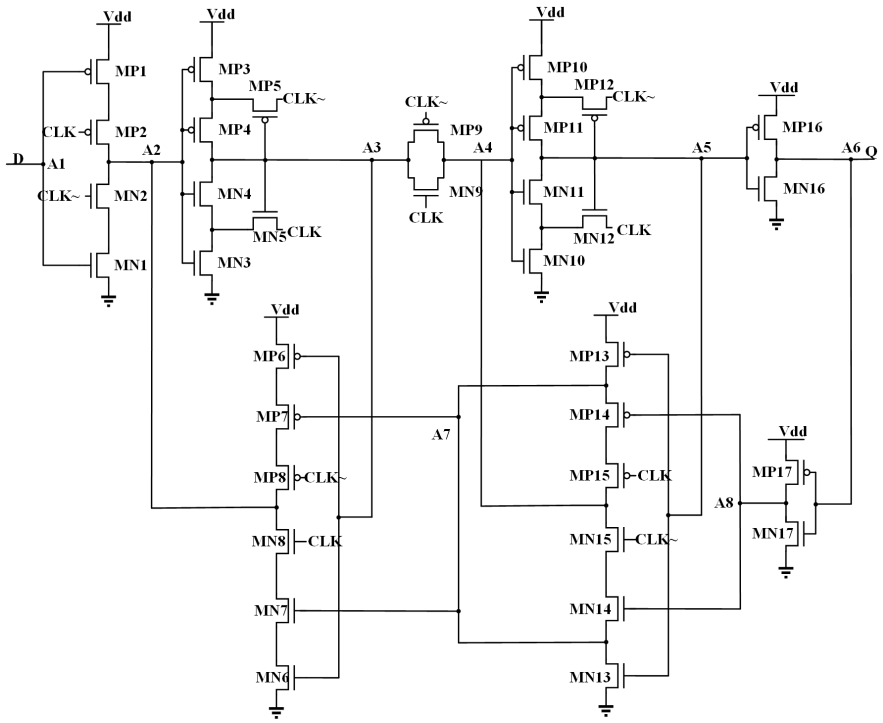


Figure 5.10 ST-DFR DFF schematic based on the variation of the second type of the Schmitt-trigger design and the DFR structure.

= 1, the secondary latch works as a delay element; When CLK = 0, the output and feedback inverters work as a delay element [18]. Previous studies have shown a decrease of 3-5X for DFR-FF over conventional DFF for heavy-ion exposures at the 65-nm thin BOX FDSOI technology [19,20], and no single-event upsets were observed up to a LET of 93.80 MeV-cm^2/mg at the 22-nm FD SOI technology [21]. The Schmitt-trigger-based DFR (ST-DFR) DFF is using the second type of the Schmitt-trigger design to replace the inverters in the DFR-FF, as shown in Figure 5.10. The Schmitt-triggers are placed in the forward path and the DFR structure is implemented in the feedback loops.

5.3 Test Chip Design

A test IC containing multiple Schmitt-trigger-based DFF cells was designed in a commercial 22-nm FD SOI technology, with some of the layout details shown in Figure 5.11 . It should be noted that the test chip also includes some other testing circuits (SRAM and Ring Oscillators), but this paper only focuses on the highlighted FF chains. The DFF designs were connected as shift register chains wit h 12,000 stages. The shift registers are clocked through an external clock signal with 1 MHz. A reversed clock scheme is used to provide clock signals to the DFFs to avoid hold time violations, as shown in Figure 5.12 [22]. All DFF chains share the same data input (Logic 0). The outputs of the DFF chains are connected to the IO pads for external error

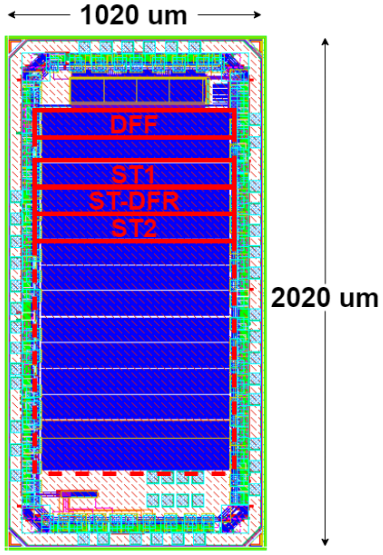


Figure 5.11 Test chip overall layout (includes some other testing circuits).

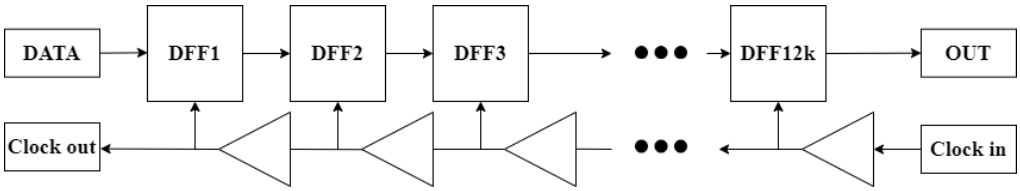


Figure 5.12 Flip-flop chain and the clock data flow for the shift register design.

detection. The nominal core logic supply voltage for this technology is 0.8 V, and the IO voltage is 1.8 V.

Four different DFF cells were designed for this work. The first design was a conventional DFF with inverters and pass gates shown in Figure 5.3. The second DFF design replaced both of the latch inverters in a conventional DFF with a Schmitt-trigger gate shown in Figure 5.4(a). This design is referred to ST1 DFF design, as shown in Figure 5.6. The third design replaced both the inverters in a conventional DFF with the modified Schmitt-trigger gates as shown in Figure 5.5, yielding the ST2 DFF design shown in Figure 5.7. The last design is the Schmitt-trigger based DFR DFF design shown is Figure 5.10, termed as ST-DFR DFF.

Table 5.1 summarizes the overall area, critical charge, average power, Clk-to-Q delay, setup time, feedback-loop delay, and CLK capacitance of the aforementioned DFF designs. These results were obtained by simulating the post-layout extracted circuit. For the critical charge simulation, double exponential current pulses were placed on the nodes at the input and output of the primary and secondary latches, for example, nodes A1, A2, A3, and A4 in Fig 2. The width and peak of the pulse were selected in relation to previous pulse results for this technology. The maximum integration of the current pulse resulted in the shown critical charge. Please note that the ST-DFR DFF design has the highest feedback-loop delay and smallest clock-to-Q delay among

Table 5.1 Electrical Performance Characteristics for the FF Chains

FF	Overall Area (n.u.)	Critical Charge (n.u.)	Average Power (n.u.)	Clk-Q Delay (n.u.)	Setup Time (n.u.)	Feedback-loop Delay (n.u.)	CLK Capacitance (n.u.)
DFF	1	1	1	1	1	1	1
ST1	1.2	1.3	2.2	2.4	2.1	2.1	1.0
ST2	1.7	1.4	1.4	2.2	1.1	2.2	2.0
ST-DFR	1.7	1.4	1.5	2.1	2.4	3.4	1.5

the three designs. It also must be noted that the timing and power characteristics were not optimized during layout generation.

5.4 Experimental Results

Alpha particle irradiation experiments were conducted at the University of Saskatchewan using a disk source containing Americium-241 alpha source with 2.5 μCi activity and 4.61×10^7 a/cm^2/h emissivity. The alpha source was placed above the die of the chip and the distance between the alpha source and the die was less than 8 mm. The testing was conducted with a 1 MHz clock and core voltages of 0.8 V and 0.6 V. No errors were observed on any chain based on a 400-hour test for each chain, validating the robustness of the 22-nm FD SOI technology against alpha particles.

Heavy ion experiments were conducted at the Texas A&M University (TAMU) Cyclotron Institute using Ne, Ar, Cu, and Ag in 15 MeV/amu cocktail. The experimental setup is shown in Figure 5.13. These particles have linear energy transfer (LET) values of 2.74, 8.45, 19.7 and 46.9 MeV-cm^2/mg, respectively. Tests were conducted at core voltages of 0.8 V and 0.6 V with normal and 60˚ tilt angle incidences. As shown in Figure 5.14, the tilted angle is along the east-west direction so that multiple transistors of the same type are along the track. Functional testing before each exposure revealed that the ST1 chain did not function at 0.6 V. Since the ST1 chain has the

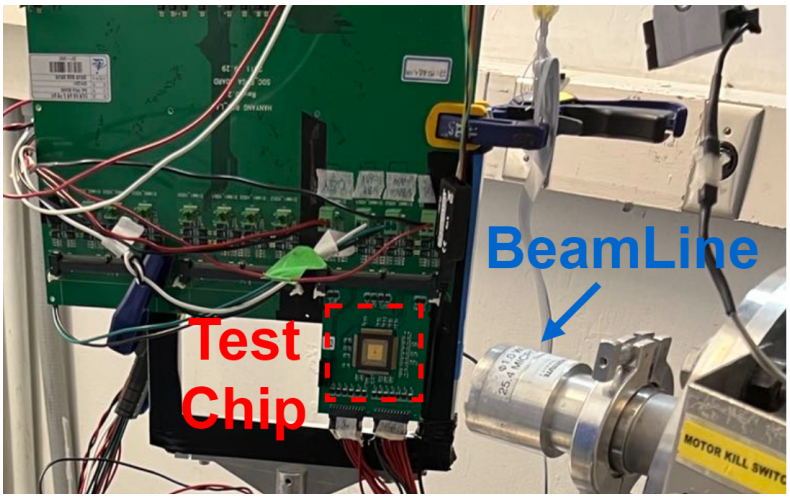


Figure 5.13 Heavy ion experimental setup at Texas A&M University.

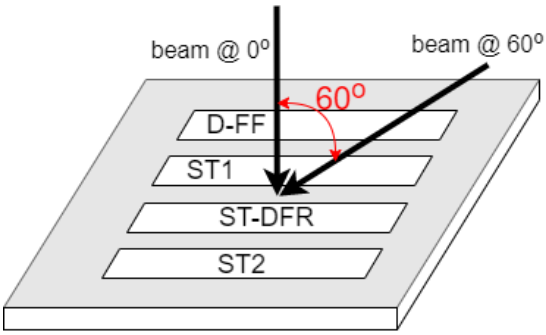


Figure 5.14 Tilt angle used during testing showing the angle of incidence with respect to power lines on the IC. Power lines run left-to-right in the IC.

Table 5.2 Ions Used in Heavy Ion Experiments

Ion	Effective LET for tilt 0˚ (MeV-cm²/mg)	Effective LET for tilt 60˚ (MeV-cm²/mg)	Range (um)
Ne	2.7	5.5	292
Ar	9.5	16.9	212
Cu	19.7	39.4	155
Ag	46.9	93.8	130

largest feedback loop delay, and the reversed clocking scheme was used, it is expected that the lower supply voltage slowed the writing operation of the flip-flop enough such that the reverse clocking signal resulted in setup-time violations within the chain. Table 5.2 provides information on the ions used, including the effective LET values for the 60º angle test and the range of ions in the silicon. No vacuum was used during the test and the chip was de-lidded.

The SEU cross-sectional values of the conventional DFF and the hardened DFFs were calculated based on the collected data. The cross-section is calculated as:

$$Cross\ Section = \frac{n}{Fluence \times Storage}, \tag{5.4}$$

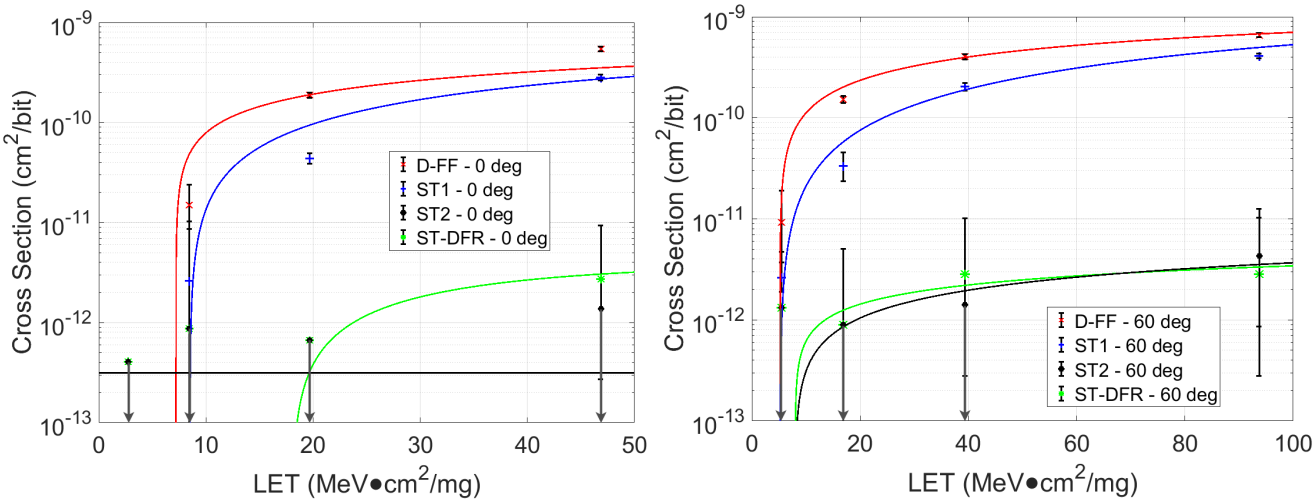
Where *n* is the total number of SEU, *Fluence* is the effective fluence in the unit of ions/cm², and *Storage* is the total number of the DFFs in the shift register. The error bar calculation is based on 95% confidence intervals when the number of events is fewer than 50 [23]; when the cross-sections are based on events more than 50, the standard deviation can be calculated with the Normal distribution [24,25]:

$$\frac{2*\sqrt{Events}}{Fluence}, \tag{5.5}$$

When there is no SEU, the error number will be assumed to be 1, and the cross-section will be calculated as:

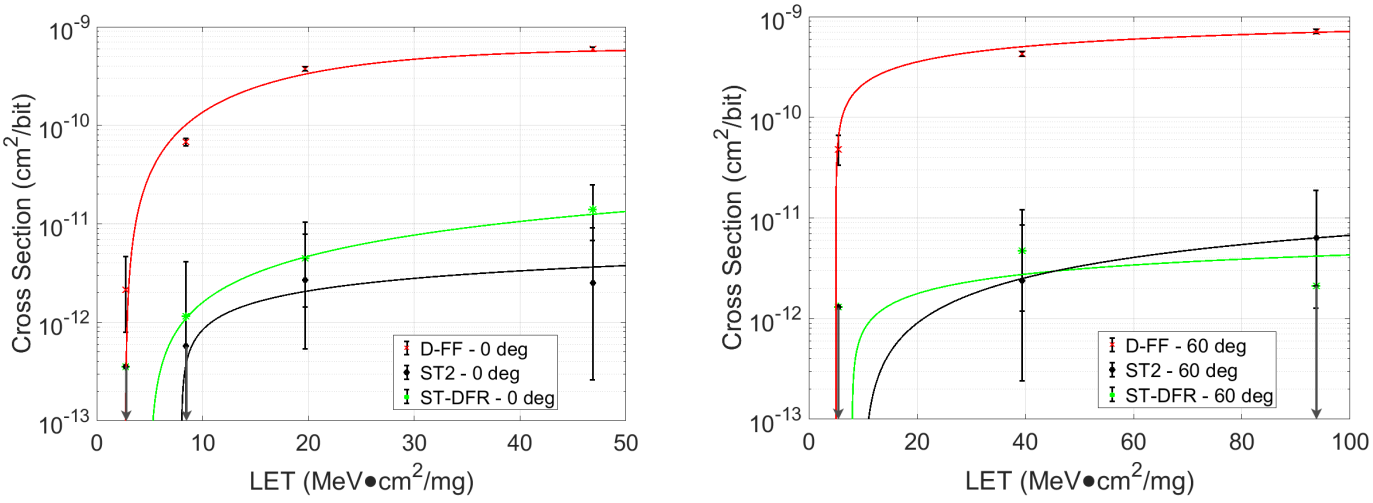
$$Cross\ Section = \frac{1}{Fluence \times Storage}, \tag{5.6}$$

Figure 5.15 (a) and (b) show the SEU cross-sectional results of the 0.8 V tests for normal and 60˚ tilt angle incidences. All three designs showed SEU cross-sections related to feedback-loop delay for each FF design at the normal incidence. Conventional DFF showed the highest SEU cross-section, followed by ST1 and ST-DFR designs. ST2 design showed the best SEU performance among those designs. It must be noted that the DFF design at this technology node shows significantly improved SE performance over comparable bulk designs. At the nominal supply voltage, the Schmitt-trigger-based designs showed 2X to 200X improvement over the conventional DFF design. ST1 design has a 5X smaller SEU cross-section compared to the reference DFF. At the 60˚ titled angle tests the SEU cross-section of the ST1 DFF increases and approaches the saturated value of the reference DFF. It should be noted that the saturated cross-section of the conventional DFF is close to the active area of the DFF layout at the 60˚ incidence angle tests. On the other hand, the SEU cross-section of the ST2 design maintains two orders of magnitude improvement over the ST1 design and the reference DFF design. The SEU cross-section of the ST-DFR design is very close to the ST2 design, despite it showing a few more errors



(a) (b)

Figure 5.15 (a) SEU Cross-section at normal angle and 0.8 V V_{DD} for the conventional DFF, ST1, ST2 and ST-DFR. (b) SEU Cross-section at 60˚ angle and 0.8 V VDD for the conventional DFF, ST1, ST2 and ST-DFR.



(a) (b)

Figure 5.16 (a) SEU Cross-section at normal angle and 0.6 V V_{DD} for the conventional DFF, ST2 and ST-DFR. (b) SEU Cross-section at 60˚ angle and 0.6 V VDD for the conventional DFF, ST2 and ST-DFR.

when the LET was increased beyond 40 MeV-cm^2/mg value. Figure 5.16 (a) and (b) show a similar cross-sectional trend for the reference and the hardened DFF at 0.6 V for normal and 60˚ tilt angle incidences. As mentioned previously, the ST1 design did not function at this low voltage testing condition. The ST-DFR design still shows a few more errors than the ST2 design. The ST2 design still exhibits the best SEU performance at this testing condition.

5.5 Discussions

The experimental results show the ST2 design has a much better SEU performance than the ST1 design and the conventional DFF in this 22-nm FD SOI technology node. It has been observed that a DFF design similar to ST2 implemented with a 65-nm bulk CMOS technology has only around 3X SEU improvement over the conventional DFF when irradiated with neutrons [11], and up to 30 X improvement in 16-nm FinFET CMOS bulk technology when irradiated with heavy-ions [12]. Those results are less appealing than its performance in the 22-nm FD SOI technology. The reason could be that this type of Schmitt-trigger structure used in the feedback loops has two transistors connected in series for both NMOS and PMOS transistors, which naturally formed the stacked-transistor structure. The stacked transistors further reduce SEU sensitivity due to isolated transistors in FD SOI technologies [26,27]. In this case, it provides

additional protection besides just the Schmitt trigger gate. Therefore, the ST2 DFF design performs much better in FD SOI technologies than the bulk technologies.

The reason that the ST2 design shows a slightly better SEU performance than the ST-DFR design is that there are four Schmitt triggers in the ST2 design, but just two in the ST-DFR design. With the help of the DFR structure, the ST-DFR design has a longer loop delay. With only two Schmitt-trigger gates it makes it less robust compared to the ST2 design which contains four Schmitt-trigger gates.

Figure 5.17 shows the comparison of the conventional DFF and ST2 design at the 22-nm FD SOI node and the 16-nm Bulk FinFET technology node [12]. These two ST2 designs have the same Schematic, and the nominal operating voltage for the 16-nm FinFET technology is 0.8 V. The SEU cross-section of the conventional DFF at the 22-nm FD SOI technology shows a less than one order magnitude difference from that of the conventional DFF at the 16-nm FinFET technology node. However, compared with the 16-nm FinFET ST2, the ST2 at the 22-nm FD SOI technology shows better SEU performance. No errors were observed for the 22-nm FD SOI ST2 during the normal incidence tests at nominal supply voltage.

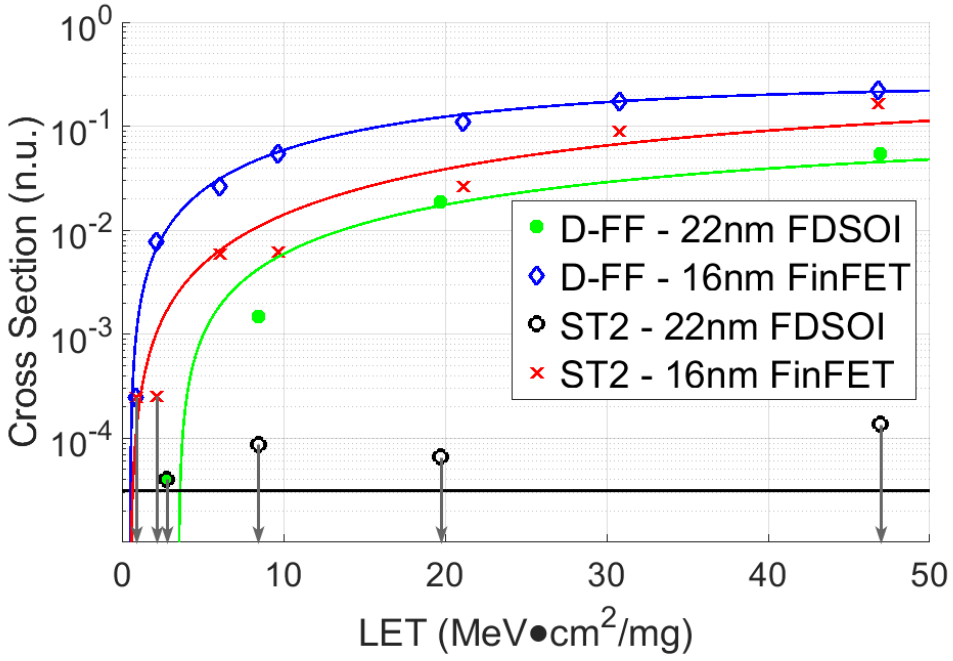


Figure 5.17 SEU cross-section comparison between two different technology nodes (22-nm FDSOI and 16-nm FinFET).

5.6 Conclusions

Multiple Schmitt-trigger-based DFF designs are designed and tested with alpha particles and heavy ions for SE performance. Alpha particle exposure showed zero upsets for all DFF designs tested including the conventional DFF design. The Schmitt-trigger-based FFs have shown improvements in SEU cross-sections varying from 2X to 200X over the tested range of LET values and supply voltages. Results show that the use of Schmitt-trigger gates can significantly improve the SE performance of DFFs at the 22-nm FD SOI technology node. The ST2 DFF has the best performance in terms of SEU tolerance. These results will help designers meet performance and SER specifications using this technology node for fabricating circuits bound for radiation environments.

Acknowledgment

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6 Comparison of Total Ionizing Dose Effects in 22-nm and 28-nm FD SOI Technologies

Contributions of the Author

The results described in this chapter have been published as the following peer-reviewed publication:

Z. Li, C. Elash, C. Jin, L. Chen, J. Xing, Z. Yang and S. Shi, "Comparison of Total Ionizing Dose Effects in 22-nm and 28-nm FD SOI Technologies," Electronics, vol. 11, no. 11, p. 1757, June 2022.

Throughout this project, I participated in the test chip design and assumed responsibility for simulations and verification. I designed the schematics and layouts of the FFs used for the TID test, while Jaime designed the ring oscillators. I also compiled and connected the SRAM block. The TID testing was conducted by Shuting, Zhi Wu, and me using the Co-60 facility at the University of Saskatchewan. I processed the data and collaborated with Dr. Chen and Chris on the analysis. I authored the initial draft of the manuscript and created all the figures included in the published paper.

Summary

TID is a measure of the accumulated ionizing radiation dose absorbed by a material or electronic device over a period of exposure. It is typically expressed in units of radiation absorbed dose, such as Grays (Gy) or rads. TID is a significant consideration in the design and evaluation of electronic systems that operate in radiation-rich environments, such as space, nuclear facilities, or medical equipment involving radiation.

Ionizing radiation can cause various detrimental effects on electronic devices, including changes in device parameters, increased leakage currents, and threshold voltage shifts in transistors. These effects can lead to performance degradation, increased power consumption, or even complete failure of the electronic system. To ensure the reliability and longevity of electronic devices in radiation environments, engineers employ various radiation-hardening techniques to mitigate the effects of TID.

This manuscript investigates Total Ionizing Dose (TID) effects on the 22-nm Fully Depleted Silicon-On-Insulator (FD SOI) technology node and compares the results with those from the 28-nm FD SOI technology node. The study uses ring oscillators (ROs) and a 256 kbit SRAM block to assess the TID sensitivity of these devices. Experimental results show that the ROs built using NAND2, NOR2, and inverter gates are impacted differently by TID effects. The NOR2 ROs are the most affected, while the NAND2 ROs are the least affected.

Comparing the 22-nm and 28-nm technology nodes, the frequency degradation in the 22-nm inverter-based RO is significantly improved, indicating that the PMOS driving current is less affected by TID effects in the 22-nm node. The 22-nm process has a 25% thinner BOX layer than the 28-nm process, which results in better resilience to TID effects. However, TID effects are still prominent in the 22-nm FD SOI node, with an increase in leakage current showing a linear trend from low to high doses. The SRAM block lost functionality at 332 krad(Si) of total dosage.

Comparison of Total Ionizing Dose Effects in 22-nm and 28-nm FD SOI Technologies

Zongru Li *, Christopher Jarrett Elash, Chen Jin, Li Chen, Jiesi Xing, Zhiwu Yang and Shuting Shi

Abstract

Total ionizing dose (TID) effects from Co-60 gamma ray and heavy ion irradiation were studied at the 22-nm FD SOI technology node and compared with the testing results from the 28-nm FD SOI technology. Ring oscillators (RO) designed with inverters, NAND2, and NOR2 gates were used to observe the output frequency drift and current draw. Experimental results show a noticeable increased device current draw and decreases in RO frequencies where NOR2 ROs have the most degradation. As well, the functionality of a 256 kb SRAM block and shift-register chains were evaluated during Co-60 irradiation. SRAM functionality deteriorated at 325 krad(Si) of the total dosage, while the FF chains remained fully functional up to 300 krad(Si). Overall, the 22-nm FD SOI results show better resilience to TID effects compared to the 28-nm FD SOI technology node.

Keywords

22-nm FD SOI; 28-nm FD SOI; Co-60; flip-flop (FF); heavy ion; radiation effects; ring oscillator (RO); static random-access memory (SRAM); total ionizing dose (TID)

6.1 Introduction

Integrated circuits (ICs) can experience various functionality issues when subjected to prolonged doses of radiation. These effects are often a reliability concern in long-term space missions where devices can spend years exposed to constant sources of radiation. Total ionizing dose (TID) effects in ICs can result in changes to gate propagation delays, leakage currents, and even loss of device functionality [1]. When ICs are exposed to ionizing radiation, positive charges are accumulated within the gate oxide and field oxide layers, thus resulting in less gate control of the device and an increased leakage current [2]. For PMOS transistors, the result of these charges

can result in the device failing to turn on, whereas NMOS transistors become difficult to turn off [1,2]. The mechanisms of TID effects in bulk technologies are often simpler due to the inclusion of only one gate oxide layer; however, fully depleted silicon on insulator (FD SOI) technologies feature a more complex response to TID effects [3].

Transistors in the latest FD SOI technologies are fabricated on a very thin silicon (Si) layer over a buried oxide layer (BOX). With each transistor fabricated on a Si Island and isolated from other transistors by the BOX layer, the volume of active Si is minimal for each transistor. This allows for superior gate control over the channel region while reducing nodal capacitances, which yields faster logic gate switching times over those for bulk technologies. However, because FD SOI technologies have an additional parasitic structure due to the BOX layer, effects due to TID are more complex than bulk devices [4–9]. The BOX layer introduces a two-dimensional coupling effect between the front and back interfaces of the channel. This doubled coupling becomes a critical contribution to the ionizing dose response of FD SOI devices. In this case, FD SOI technologies tend to be more sensitive to TID than their bulk counterparts [10,11]. This is important to note due to the attractiveness of FD SOI technologies for use in space missions because of the technologies' inherent resilience to particle-induced single event effects (SEEs) [3,9]. There are already some experimental results from previous research on TID effects in the 28-nm FD SOI technology node [2,9]. These results show that a TID-induced gate delay increased significantly in that technology node, as well as leakage currents which impose barriers for it to be used for some space applications where tolerance to high total absorbed dose levels is required. Therefore, it is essential to investigate TID effects in the 22-nm FD SOI technology node and compare them with the results from the 28-nm FD SOI technology node.

To evaluate TID effects, a 22-nm FD SOI test chip was designed and fabricated. Ring oscillators (ROs), flip-flop (FF) chains, and a static random access memory (SRAM) block were chosen as the testing vehicles for evaluating the technology's susceptibility to TID effects; including both Co-60 and heavy ions irradiation sources [12]. RO circuits can offer insights into gate delays due to changes in the frequency of the circuits, as well as changes in power consumption as dosage increases. The FF chains and the SRAM block can be used to offer a broad perspective on device functionality. A similar test chip with 28-nm FD SOI technology was also

fabricated previously, and the results from that test chip will be used in this paper for comparison purposes between the two technologies [9].

The organization of the rest of this paper is as follows. In Section 2, details of the test circuits are introduced. In Section 3, details of the test chip design and experimental setup are described. In Section 4, the experimental results will be presented and discussed. Lastly, conclusions are drawn in Section 5.

6.2 Description of Test Circuits

6.2.1 Ring Oscillators

Individual transistors are the ideal test vehicles for evaluating TID effects; however, there are many challenges regarding fabrication and testing. Additional design procedures are necessary to avoid the antenna effects during fabrication, leading to additional measurement errors. As explained by [13], measuring the change in the delay of a single transistor is difficult in practice, and can severely skew the results if the transistor has large variations in fabrication. Instead, ring oscillator (RO) circuits use the average parameter values of all transistors in the circuit, and as such, are well suited for the TID characterization of circuit-level parameters such as gate delay and power usage [8,14,15]. The use of averaged measurements allows for averaging statistical variations between individual gate parameters, thus ensuring that statistical variations between individual transistors in the RO circuit are incorporated into the overall RO characteristics [8]. Additionally, since ROs are often used for clock generation sources, it is important to understand how their performance can change as the dosage of ionizing radiation increases.

RO circuits are designed using an odd number of logic gates connected in a loop, which results in an unstable circuit oscillating at a fixed frequency. The oscillating frequency depends on the number of stages in the loop. The RO frequency is determined by the following equation:

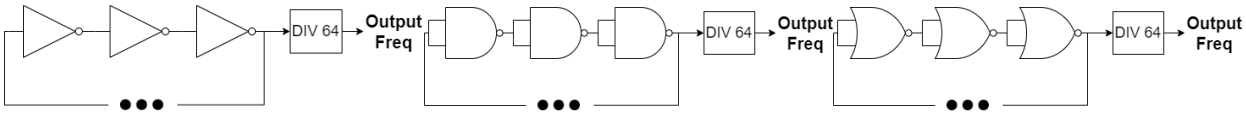
$$f = \frac{1}{2 \times n \times t} \tag{6.1}$$

where f is the RO frequency, n is the number of stages in the RO loop, and t is the average delay of each RO stage. The equation for a single inverter delay is given below:

$$Delay_{inv} = \frac{C_L \times V_{DD}}{\frac{W}{L} \times \mu \times C_{ox} \times (V_{DD} - V_{th})^2} \quad (6.2)$$

where C_L is the load capacitance, V_{DD} is the supply voltage, W and L are the width and length of the gate, μ is the carrier mobility, C_{ox} is the capacitance of the oxide layer, and V_{th} is the gate threshold voltage [16]. TID effects will alter both the mobility and the threshold of the device, which will thus result in a measurable difference in the delay of the gate, and therefore the frequency of the oscillator.

A variety of different ROs were constructed with 2-input NAND (NAND2) gates, 2-input NOR (NOR2) gates, and inverters, as shown in Figure 6.1. For each type of gate, multiple ROs were designed, each with a different number of gates to achieve different oscillating frequencies. It should be noted that they were designed based on the cells from the standard cell library without any special layout design techniques. The inverter ROs included four different frequency options,



(a) (b) (c)

Figure 6.1 Three different RO designs: (a) Inverter-based RO design; (b) NAND2-based RO design; (c) NOR2-based RO design.

Table 6.1 Inverter-based programmable RO simulation results.

Delay Block	Number of Delay Stages	Output Frequency (n.u.)
S0	21	1.00
S1	29	0.77
S2	45	0.57
S3	69	0.36

Table 6.2 NAND-based programmable RO simulation results.

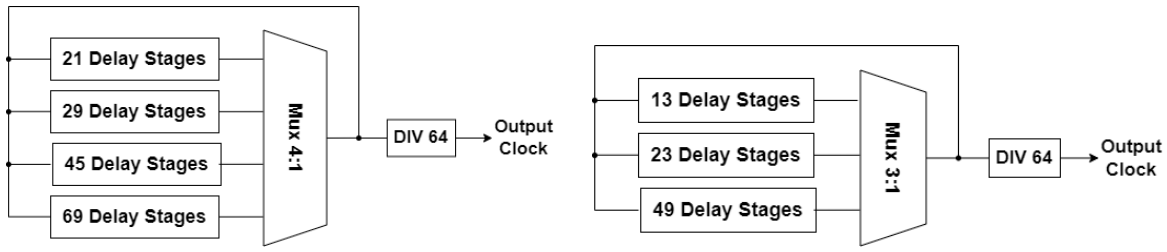
Delay Block	Number of Delay Stages	Output Frequency (n.u.)
S0	13	1.00
S1	23	0.68
S2	49	0.39

Table 6.3 NOR-based programmable RO simulation results.

Delay Block	Number of Delay Stages	Output Frequency (n.u.)
S0	13	1.00
S1	23	0.68
S2	49	0.38

and the NAND2 ROs and NOR2 ROs both had three different frequency options. Tables 6.1–6.3 show the ROs' expected oscillation frequencies normalized to their respective fastest oscillation frequency as measured by post-layout simulations from the foundry supplied process design kit (PDK).

The output of oscillators for each respective gate was connected to a multiplexer and a frequency divider circuit, as shown in Figure 6.2. The inclusion of the divider was needed as the high frequencies of the oscillators were not able to be directly captured by the chip's IO pads, which are limited to 50 MHz. A reference RO used for comparison purposes was previously fabricated in the 28-nm FD SOI technology node. It was constructed with 44-stage inverters and a nominal oscillating frequency of 1 GHz.



(a) (b)

Figure 6.2 Schematic designs of different gate-based ROs: (a) Inverter-based RO schematic design; (b) NAND2 or NOR2-gate-based RO schematic design.

6.2.2 Flip-Flop Chains

The designed FF block included 14 different FF chains, which were comprised of a conventional master-slave transmission gate FF and 13 different radiation-hardened FF designs. The FFs were connected as shift register chains with 12,000 stages in each chain. The shift registers were clocked through an external clock signal and received input data via an IO pad. The reversed

clock scheme was used to help avoid hold-time violations, as shown in Figure 6.3. While the power draw of each FF chain is slightly different due to the inherent design differences, together they offer an appropriate testing platform for determining changes in IC power usage as the dose rate increases, as well as changes in device functionality.

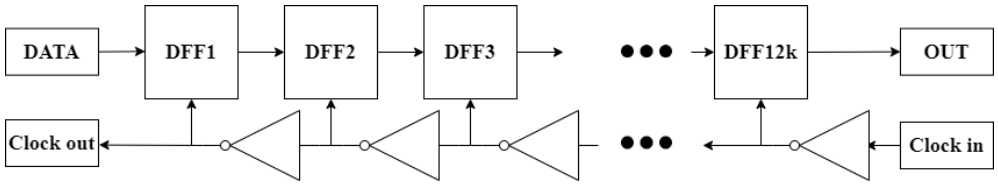
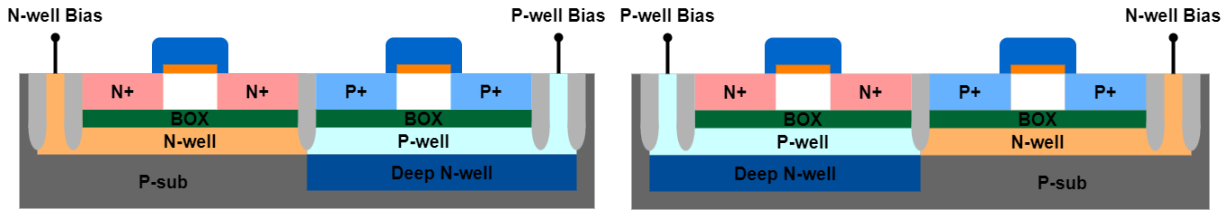


Figure 6.3 Flip-flop chain and the clock data flow for the shift register design.

6.2.3 SRAM Block

A forward body bias (FBB) transistor configuration was chosen for the SRAM array, as shown in Figure 6.4a. The FBB transistor configuration allows for higher drive and lower threshold voltages, whereas the conventional reverse body bias (RBB) configuration, shown in Figure 6.4b, can limit leakage currents by increasing the threshold voltage of the device. Traditionally, SOI technologies were prone to TID-induced leakage currents causing operational failures [17]. However, recent FD SOI technologies, such as 28-nm and 22-nm, have shown a significantly higher tolerance for TID exposures with limited increases in leakage currents, especially when the total absorbed dose is within 100 krad(Si) [18]. In this case, the usage of the RBB configuration to limit the operational performance of ICs was not as appealing as before. Instead, the usage of the FBB configuration to improve the performance of an IC design has become more valuable than the traditional RBB configuration. To investigate TID effects on an SRAM with FBB configuration, a 256 kbit SRAM block was designed with a memory compiler. The SRAM block



(a) (b)

Figure 6.4 (a) Flipped well configuration (FBB); (b) regular well configuration (RBB).

featured a 15-bit address line, an 8-bit data line, as well as a read/write enable and clock input. It was a single-port SRAM configured as 32 K × 8 memory with 256-cells on a bit-line. It included additional features such as bit-line redundancy, a pipeline mode, and power-gating. Inside of the SRAM design, it included cell arrays and various peripheral circuits such as row/column decoders, self-timing generators, sense amplifiers, and buffers. As SRAMs are commonly used in circuit designs, it is important to evaluate their performance under TID effects.

6.3 Test Chip Design

A test chip consisting of the three types of circuits previously discussed was developed and fabricated in a commercial 22-nm FD SOI technology, as shown in Figure 6.5. All FF chains shared the same data input. The outputs of the SRAM block and FF chains were connected to the IO pads for external error detection, and the outputs of the RO circuits were connected to the IO pads for the frequency measurements. The nominal core logic supply voltage for this technology was 0.8 V, and the IO voltage was 1.8 V. Functional verification testing was carried out on the fabricated SRAM and FF chains with all 0s, 1s, and checker-board input patterns before irradiation.

A testing system consisting of power supplies, an FPGA board, and a microcontroller used during testing. The test chip was soldered onto a custom-made daughter board and was connected to the FPGA via a DIMM connection. During testing, the FFs, SRAM, and ROs were powered at

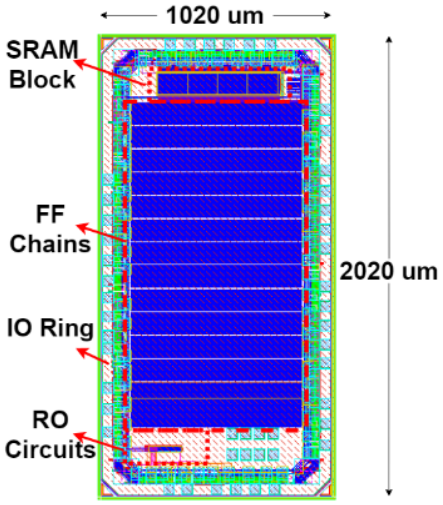


Figure 6.5 Test chip overall layout.

their nominal voltage of 0.8 V. The FF chains were clocked at 1 MHz with the ‘all 0’ data input pattern, and current readings were taken from the power supplies every minute. The SRAM block was also clocked at 1 MHz, and a checker-board data pattern was used. At the beginning of testing, all addresses in the SRAM were written with the test data. Then, the content of the SRAM was continually read out to check if the data were still appropriately stored. If there was a mismatch in data, the system would record the event and attempt to repair the address with the correct test data, and the process would continue. If the address data could not be repaired, then that address location was considered non-functional and recorded.

During testing, the ROs were also powered at their nominal voltage of 0.8 V. The output pins of the ROs were connected to counters inside the FPGA and monitored the number of oscillations of each RO within a 0.1 s period. By knowing the number of oscillations for a given period, the frequency of each RO was able to be determined. During testing, all collected data on the FPGA were transferred to a microcontroller via a serial connection, where the data were logged and recorded so that testing personnel could evaluate the experimental data in real-time.

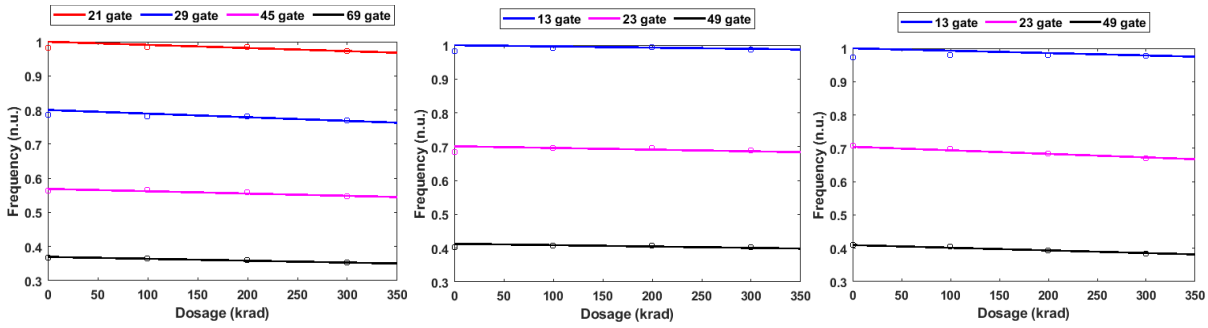
6.4 TID Experimental Results and Discussions

The TID experiments were performed by using a Gammacell 220 Co-60 chamber (Figure 6.6) at the University of Saskatchewan, Saskatoon, SK, Canada. The Gammacell 220 chamber can

Figure 6.6 Gammacell 220 Co-60 Irradiator.

provide an irradiation rate of 108.2 rad(Si) per minute. The total absorbed dose during the experiments was around 300 krad(Si).

The frequencies of the ROs were recorded during the TID testing and plotted in Figure 6.7. It should be noted that the observed experimental data are a linear trend, so a first-order polynomial curve fitting was implemented to understand this trend better. It is interesting to note that the ROs with the same gate type experienced the same decreasing rate in their output frequency during testing. This can simply be attributed to the same gate delay degradation during TID testing.



(a) (b) (c)

Figure 6.7 RO frequencies vs. total absorbed dose during Co-60 test: (a) Inverter-based ROs; (b) NAND2-based ROs; (c) NOR2-based ROs.

The relative change in frequency was calculated from the ROs designed with inverters, NAND2, and NOR2 gates and listed in Table 6.4. For the inverter-based RO, the relative decrease in frequency was the average of the drops in four different stage options; for the NAND2 and NOR2-based ROs, the average value of the drops in three different stage options was used to calculate the relative decrease in frequency. From the results, a trend emerged showing that ROs built using different gates were impacted by TID effects at differing rates.

Table 6.4 shows that the frequencies of the NAND2 ROs were least affected by the TID, whereas the NOR2 ROs were most affected. It is noted that the NAND2 gates have two NMOS

Table 6.4 RO frequency differences from 0 krad(Si) of exposure to 300 krad(Si) during Co-60 test.

RO Type	Relative Decrease in Frequency
Inverter	−3.7%
NAND2	−2.1%
NOR2	−4.3%

transistors in series and two PMOS in parallel, whereas the NOR2 gates have two PMOS transistors in series and two NMOS in parallel. The sizing of the NMOS and PMOS network of the NAND2 and NOR2 gates used in the ROs was designed such that the rising and falling time were roughly equal. In general, the positive charge trapped in the BOX under the transistors due to TID irradiation results in a negative shift of the threshold voltage, which leads to an increased driving current of the NMOS transistor and reduced driving current for the PMOS transistors in the gates. Findings in [2] show that the PMOS driving current is significantly reduced compared to the increase in the NMOS driving current in 28-nm FD SOI technology, which leads to the monotonic decrease in the frequency with the irradiation dose. The experimental results in this paper also show the same trends. The results of the NAND2 and NOR2 ROs further validate this since NOR2 has two PMOS transistors in series, which further degrades the delay of the gate, and hence reduces the frequency of the ROs.

TID testing with heavy ion irradiation was conducted at the Texas A&M University (TAMU) Cyclotron Institute. An irradiation rate of 60.9 rad(Si) per second was provided. Figure 6.8 shows the change of the frequencies as the increase in the heavy ions TID exposure for the inverter-based RO (45 stages), NAND2-based RO (23 stages), and NOR2-based RO (23 stages). The results still show that the NOR2 RO has the largest frequency degradation, while the NAND2

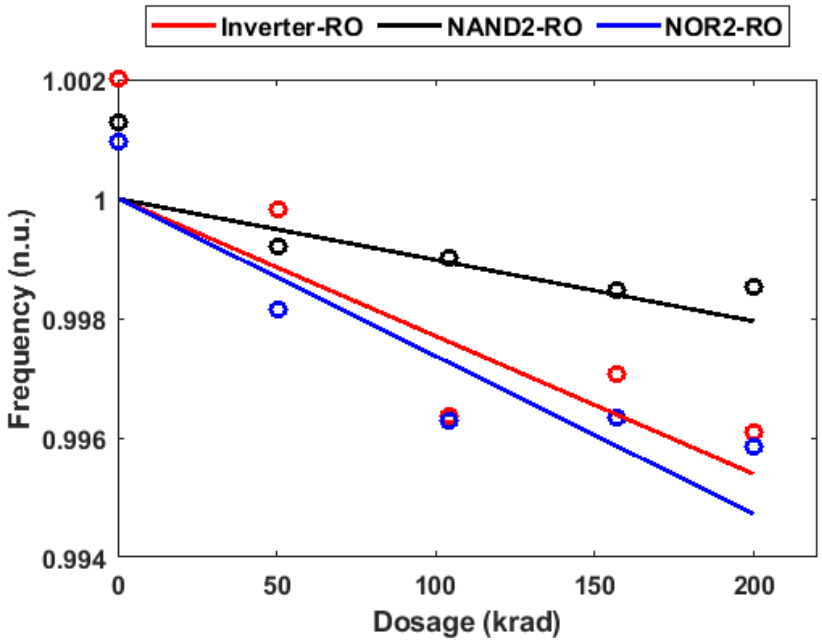


Figure 6.8 RO frequencies vs. total absorbed dose during heavy ion test.

RO has the least, which was demonstrated from the previous analysis. In addition, it can be observed that the degradation of the RO frequency from the Co-60 test is much more than the heavy ion test. Despite the use of the High-K dielectric gates in advanced technologies, which can help to reduce the radiation-induced voltage shift in the gate insulator, the radiation-induced charge in SOI buried oxides and shallow trench isolation oxide (STI) can cause degradation or failures as well [19]. Electron-hole pairs are generated in the oxide layers when applying high-energy ionizing radiation, but most holes and electrons can immediately recombine. For high LET particles, such as heavy ions, they generate high-density charge pairs, making the initial recombination rate significantly large. The charge pair line density is relatively small for the low LET particles, such as Co-60, which reduces the initial recombination rate. Compared to the heavy ions, the Co-60 has a better ability and efficiency to create the trapped charges in oxide layers [9], as reported in [20,21], respectively.

Another inverter-based RO in 28-nm technology was used for comparison. There are 45 stages in the 28-nm RO, and 44 of them are also used as delay stages contributing to other designs. A multiplexer was used to switch between these two modes, as shown in Figure 6.9. When the select input is high, the design will work as an RO. The 28-nm RO was also based on the conventional inverter without any layout optimizing techniques, which is the same as the 22-nm design, making these two designs fully comparable. The frequency versus total dose for two inverter-based ROs (45 stages and 69 stages, respectively) in the 28-nm and 22-nm FD SOI technologies are plotted in Figure 6.10. These results show that during the Co-60 test at 300 krad(Si) of dosage, the 28-nm RO had a frequency decrease of over 11.8% from the initial, compared to the 3.7% decrease in 22-nm RO. During the heavy ion test, at 200 krad(Si) of dosage, the 28-nm

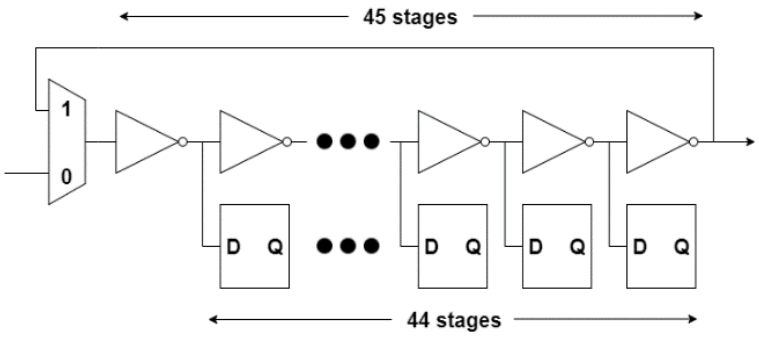
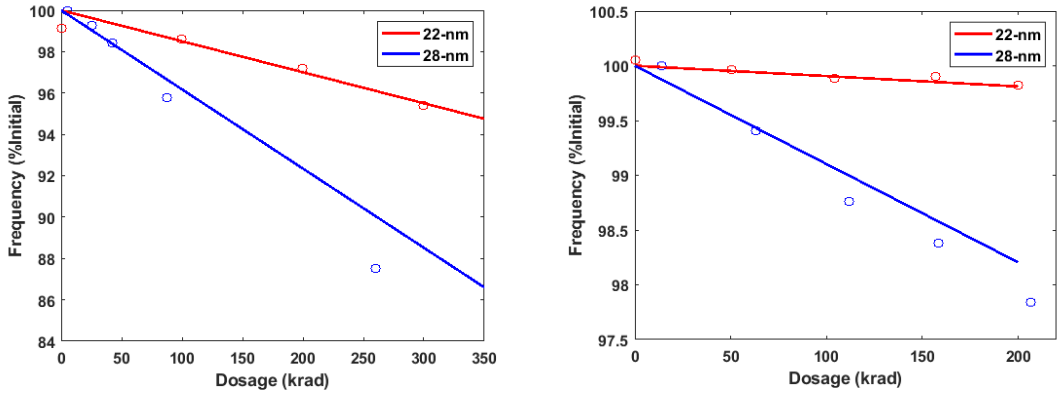


Figure 6.9 Schematic of the 28-nm RO design.



(a) (b)

Figure 6.10 RO frequencies from 22-nm and 28-nm test for (a) Co-60 test; (b) heavy ion test.

RO had a frequency decrease of around 1.8% from the initial, compared to a less than 0.5% decrease in the 22-nm RO. These results show that the degradation in frequency for the 22-nm inverter-based RO has significantly improved. This indicates that the PMOS driving current is less affected by the TID effects for the 22-nm technology node, which could be due to manufacturing improvements. It is known that a thinner SiO2 BOX layer can lead to a milder TID effect [18,22]. The thicknesses of the BOX and the SOI body of the 28-nm FD SOI technology are 25-nm and 7-nm [23], and those are 20-nm and 6-nm in the 22-nm FD SOI technology node, respectively [24]. The BOX of the 22-nm process is 25% thinner than that of the 28-nm process, so a less positive charge will be deposited in the BOX of the 22-nm process during irradiation. This will cause less interference with the threshold voltage of the 22-nm process, eventually leading to better resilience to TID effects.

Figure 6.11 shows the change in power supply current as the TID exposure increased for both 22-nm and 28-nm test circuits for Co-60 irradiation. Both of the plots are normalized. The current of 22-nm influenced by cumulative TID exposure is very similar to that of the 28-nm test. However, the current of the 22-nm test increased by approximately 8 times after 300 krad(Si) dosage compared to the initial starting current, while the 28-nm showed a 4 times increase. The increase in driving and leakage currents in the transistors can explain this increase in the current draw as the dose rate increases. These data show that TID effects are still prominent in the 22-nm FD SOI node. In addition, in the 22-nm technology node, the increase in the leakage current shows a linear trend from low doses to high doses.

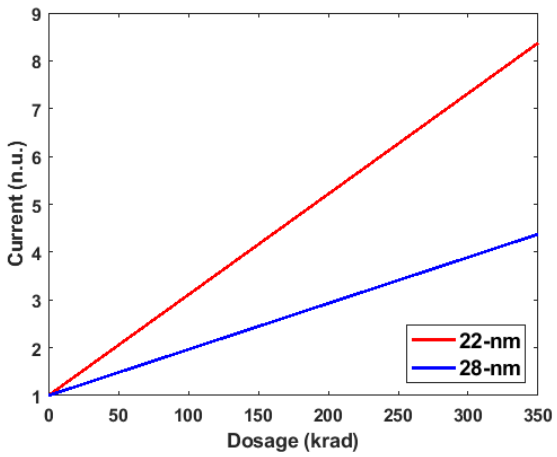


Figure 6.11 Current from 22-nm and 28-nm tests during Co-60 test.

The SRAM operated normally during testing until its functionality deteriorated at 325 krad(Si) of the total dosage. At this point, the number of recorded errors increased drastically, and every address showed a loss in functionality by 332 krad(Si) of the total dosage. A series of troubleshooting tests were performed to try and return functionality back to the SRAM block. These included resetting the test program, power cycling the SRAM, and clocking the SRAM at a slower rate of 100 kHz. None of these methods yielded any results, and the SRAM block was presumed dead. The FFs were still functional after the 300 krad(Si) total absorbed dose, and no error was observed on any of the FF chains. To compare with the SRAM, the FFs were subjected to additional testing up to 350 krad(Si) while retaining their functionality. In this case, it is believed that the SRAM storage cells themselves did not fail at 325 krad(Si), but instead, some part of the peripheral circuitry became damaged. For example, the internal operation of the SRAM block is controlled by a self-timing, asynchronous circuit, which could fail due to the increased delay, and this would explain why the entirety of the SRAM block failed at the same time instead of a more gradual loss in functionality. In this case, this timing issue caused by TID should be taken into account when designing the memory. For example, the self-timing circuit in the SRAM should be designed to be tolerant of the additional delay induced by the TID. Another method is to apply the back-gate voltage to the peripheral circuitry. When applying the back-gate voltage to circuits in the flipped well configuration, the drive current will be enhanced, and the delay will be reduced, which should effectively mitigate the TID effect in the peripheral circuitry.

6.5 Conclusions

Three types of RO circuits were designed and fabricated to evaluate the effects of frequency and leakage currents while exposed to gamma radiation. Results were compared with the previous 28-nm FD SOI node, and they show that the 22-nm FD SOI node had less frequency degradation compared to the 28-nm node. Among the three types of ROs, all showed degradations due to the TID, but the NOR ROs yielded a worse performance than that of the inverter ROs and NAND ROs due to the significantly reduced driving current in PMOS transistors during TID testing. The reduction rate of the RO frequency during the Co-60 was much higher than that of the HI test. The power supply current increased as the dosage increased similarly to that of the 28-nm node. The SRAM failed when the cumulated dose reached 325 krad(Si), but the FF chains were still functional through the test up to 300 krad(Si). These results indicate that additional attention must be paid when designing complex circuits for radiation-hardened applications.

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7 SUMMARY, CONTRIBUTIONS AND FUTURE WORK

7.1 Summary

This study examines the effects of various radiation types on the 22-nm FDSOI technology node. Multiple radiation-hardened-by-design flip-flop (FF) configurations were investigated, utilizing three fundamental hardening techniques: transistor-stacking, guard-gating, and Schmitt-triggers. Drawing from these foundational methods, several FF designs were developed and tested, including the stacked FF, charge-canceling stacked FF, interleaved-stacked FF, GG FF, DFR FF, GG-DICE FF, ST1 FF, ST2 FF, and ST-DFR FF. All FF designs were fabricated using the 22-nm FDSOI process and subjected to alpha particle and heavy ion irradiation for SE characterization. The SEU performance of these FFs was thoroughly evaluated, and subsequent analysis of the designs was conducted based on the results obtained. Each design demonstrated varying degrees of SEU performance enhancement. Among the various designs, the charge-cancelling-stacked FF experienced upsets only at high LET values and high angles of incidence, while the interleaved-stacked design and DFR-DICE FF designs showed zero upsets for all test conditions. Stacked-transistor and Schmitt-trigger-based designs displayed significant improvements in SEU cross-sections over conventional DFF designs, with the latter showing improvements ranging from 2X to 200X over the tested range of LET values and supply voltages. TCAD simulations were employed to analyze the layout of GG and DFR designs, revealing an issue in the GG design where one of the stacked transistors maintained a path to VDD due to the CnRx layout construct. Careful layout design was identified as a critical aspect in improving SE performance, as the CnRx construct could inadvertently create a direct path for charge collection. Proposed modifications to the GG-FF layout led to a significant reduction in charge collection at sensitive nodes, resulting in improved SEU resilience. This comprehensive investigation aims to provide valuable insights for improving the radiation tolerance of 22-nm FDSOI technology nodes in future applications.

The TID performance of the 22-nm FDSOI technology was assessed using a SRAM and various RO designs, and the results were compared to those of the 28-nm FDSOI node. In order to assess the impact of gamma radiation exposure on functionality and leakage currents, three different types of RO circuits were designed and fabricated. When compared to the previous 28-nm FDSOI node, the 22-nm FDSOI node demonstrated less frequency degradation. During TID testing, all three types of ROs encountered degradation. However, the NOR ROs displayed poorer performance compared to the inverter ROs and NAND ROs. This can be attributed to the substantial reduction in driving current observed in PMOS transistors during TID testing. The reduction rate of RO frequency during the Co-60 test was considerably higher than that of the HI test. As the radiation dosage increased, the power supply current rose similarly to that of the 28-nm node. The SRAM failed when the cumulative dose reached 325 krad(Si), while the FF chains remained functional up to 300 krad(Si) throughout the testing. These findings suggest that careful consideration is necessary when designing complex circuits for radiation-hardened applications.

7.2 Contributions

In this thesis, several studies exploring the radiation tolerance of various digital circuit designs and a RISC-V microprocessor, specifically for high-reliability applications, are presented. The contributions of this thesis are as follows:

Transistor stacking improves flip-flop SEU performance at the 22-nm FDSOI node, with stacked-transistor DFF designs showing significant improvement over conventional designs. Charge-cancelling and interleaving techniques further reduce upsets, with the interleaved-stacked design showing zero upsets for all test conditions. The charge-cancelling-stacked design only showed upsets at high LET values and high incidence angles. The stacked-transistor design has more than one order improvement in SEU cross-sections compared to conventional designs, making it an effective technique for hardening customized DFF and logic circuits.

Radiation-hardened-by-design flip-flops using guard-gates were evaluated at the 22-nm FDSOI technology node, with GG-based FF designs providing additional protection against SEUs. The DFR-FF and GG-DICE FF designs showed zero upsets for all test conditions, while the conventional GG design showed more than 100X improvement over conventional FF designs at

nominal supply voltage. These results highlight the effectiveness of stacked-transistor and GG constructs for hardening customized FF and logic circuits.

Schmitt-trigger-based DFF designs were found to exhibit improved SEU performance over conventional designs at the 22-nm FDSOI technology node, with improvements varying from 2X to 200X over the tested range of LET values and supply voltages. The ST2 DFF has the best SEU tolerance performance, making it an attractive choice for hardening applications. These results provide valuable information for designers seeking to meet performance and SER specifications for circuits bound for radiation environments.

The 22-nm FDSOI process is more resilient to TID effects than the 28-nm process due to its thinner BOX layer. However, TID effects are still prominent, with an increase in leakage current and the SRAM block losing functionality at high doses. All types of ROs showed degradations due to TID, with NOR ROs yielding worse performance than inverter and NAND ROs. The power supply current increased as the dosage increased, similar to the 28-nm node. Complex circuits for radiation-hardened applications require additional attention during the design phase.

These contributions advance the understanding of radiation tolerance in digital circuits and microprocessors, providing valuable insights and techniques for designing radiation-hardened systems for aerospace, high-performance supercomputers, and other high-reliability applications.

7.3 Current Work

The rising demand for high-performance computing in extreme environments, such as space, nuclear, and defense applications, has underscored the need for radiation-hardened microprocessors. To address this need, researchers are developing a radiation-hardened RISC-V microprocessor, combining the open-source, flexible, and modular RISC-V architecture with radiation resilience. The project's primary goal is to create a robust and efficient computing platform capable of reliable operation under radiation exposure, thereby enhancing the performance and longevity of systems in space exploration, nuclear research, and defense sectors.

RISC-V is an open standard instruction set architecture available under free and non-restrictive licenses. It has strong industry support, particularly from chip and device manufacturers,

and is designed for unrestricted extensibility and customization to meet market demands. In this project, a 32-bit fault-tolerant RISC-V microprocessor is being developed for high-reliability applications. The design is based on the CV32E40P core from OpenHW Group, a mature and efficient 32-bit RISC-V core with a 4-stage pipeline. The core implements the RV32IMC instruction set architecture, and the Xpulp custom extensions enhance code density, performance, and energy efficiency.

Various fault-tolerant techniques are applied to the design. First, regular flip-flops in the datapath design are replaced with fault-tolerant flip-flops. Second, clock/reset trees and other combinational circuits are replaced with fault-tolerant techniques to minimize errors in the system. This involves identifying sensitive buffers in the clock and reset trees and replacing them with fault-tolerant ones based on their sensitivity levels. Third, combinational logic circuits are protected using approximate logic approaches, which identify and safeguard the most sensitive nodes. Finally, on-chip memories are designed with error-detecting and correcting codes to protect against single-bit errors.

An on-chip ring oscillator provides the clock for the microprocessors, with a frequency range from 200 MHz to 1 GHz. A serial configuration interface is used to control the clock frequency, SRAM tuning parameters, and processor and debug circuitry. The microprocessor and control circuits are placed in a test chip, fabricated using 22-nm FDSOI technology. After functional testing, the chips are to be tested with pulsed lasers, heavy ions, and proton particles to evaluate their radiation tolerance performance. The project is ongoing, and the test chip will be taped out by the end of June 2023.

7.4 Future Work

The results obtained from this thesis provide a strong foundation for further research and development in radiation-hardened designs for digital systems. The following are potential directions for future work:

Explore advanced radiation-hardening techniques: Investigate novel radiation-hardening techniques that can be applied to the flip-flop designs and combinational logic circuits to further

enhance their tolerance to radiation-induced soft errors. Emerging techniques such as selective hardening, adaptive voltage scaling, and error detection and correction could be explored.

Analyze the impact of technology scaling: As technology nodes continue to scale down, the effects of radiation-induced soft errors may become more significant. Future work could analyze how these effects change with different technology nodes and investigate the suitability of the proposed radiation-hardening techniques for smaller technology nodes.

Multi-core RISC-V microprocessor: Extend the radiation-tolerant RISC-V microprocessor design to incorporate multiple cores, thereby increasing computational power and enhancing the system's overall fault tolerance. Investigating the impact of radiation on interconnects and cache coherence mechanisms in a multi-core setup will also be valuable.

Benchmarking and comparison with other architectures: Conduct a comprehensive performance evaluation of the radiation-tolerant RISC-V microprocessor, comparing it to other radiation-hardened microprocessor designs based on different architectures, such as ARM, MIPS, and x86. This comparison will help validate the effectiveness of the radiation-hardening techniques employed in the RISC-V design.

Radiation-aware power management: Investigate the development of radiation-aware power management techniques that can be integrated into the radiation-tolerant RISC-V microprocessor. These techniques could dynamically adjust the supply voltage, clock frequency, or other system parameters to minimize radiation-induced soft errors while maintaining optimal performance and energy efficiency.

Investigate the impact of radiation on analog and mixed-signal components: While this thesis primarily focuses on digital components, radiation effects on analog and mixed-signal components are also crucial for system-level reliability. Future work could explore radiation-hardening techniques for these components, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and phase-locked loops (PLLs).

Real-world application and system-level analysis: Apply the radiation-hardened RISC-V microprocessor to real-world applications, such as satellite systems, space exploration, and high-performance computing in radiation-rich environments. This would involve developing system-

level analysis and simulation tools to evaluate the overall reliability and performance of these systems in the presence of radiation.