Single Event Effect Hardening Designs in 65nm CMOS Bulk Technology

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ABSTRACT

Radiation from terrestrial and space environments is a great danger to integrated circuits (ICs). A single particle from a radiation environment strikes semiconductor materials resulting in voltage and current perturbation, where errors are induced. This phenomenon is termed a Single Event Effect (SEE). With the shrinking of transistor size, charge sharing between adjacent devices leads to less effectiveness of current radiation hardening methods. Improving fault-tolerance of storage cells and logic gates in advanced technologies becomes urgent and important.

A new Single Event Upset (SEU) tolerant latch is proposed based on a previous hardened Quatro design. Soft error analysis tools are used and results show that the critical charge of the proposed design is approximately 2 times higher than that of the reference design with negligible penalty in area, delay, and power consumption. A test chip containing the proposed flip-flop chains was designed and exposed to alpha particles as well as heavy ions. Radiation experimental results indicate that the soft error rates of the proposed design are greatly reduced when Linear Energy Transfer (LET) is lower than 4, which makes it a suitable candidate for ground-level high reliability applications.

To improve radiation tolerance of combinational circuits, two combinational logic gates are proposed. One is a layout-based hardening Cascode Voltage Switch Logic (CVSL) and the other is a fault-tolerant differential dynamic logic. Results from a SEE simulation tool indicate that the proposed CVSL has a higher critical charge, less cross section, and shorter Single Event Transient (SET) pulses when compared with reference designs. Simulation results also reveal that the proposed differential dynamic logic significantly reduces the SEU rate compared to traditional dynamic logic, and has a higher critical charge and shorter SET pulses than reference hardened design.

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My appreciation also extends to my laboratory colleagues, Haibin Wang and Yuanqing Li. We worked together to finish the test chip from design to sign off and they supported me greatly and gave me a lot of technical suggestions. Thanks also go to Trevor Zintel, who was our support engineer and helped us a lot with license and software problems.

Lastly and most of all, I would like to thank my parents, whose value to me only grows with age. It is their love and encouragement that helped me to survive all the stress from these years; they never let me give up. I am so proud to be their daughter.

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LIST OF ABBREVIATIONS

3D	Three-Dimension
BPSG	Borophosphosilicate Glass
CIAE	China Institute of Atomic Energy
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CQFP80	80-pin Surface Mount Ceramic Quad Flat Package
CVSL	Cascode Voltage Switch Logic
DFF	D-type Flip Flop
DICE	Dual Interlocked Storage Cell
DIMM	Dual In-line Memory Module
DUT	Device Under Test
ECC	Error Correcting Codes
ESD	Electrostatic Discharge
FF	Flip-flop
FIT	Failure-In-Time
FPGA	Field Programmable Gate Array
IBM	International Business Machines
IC	Integrated Circuit
I/O	Input/Output
LEAP	Layout Design Through Error-Aware Transistor Positioning
LET	Linear Energy Transfer
MCU	Multiple Cells Upset

MFF	Mega Flip-flops
NMOS	Negative-Channel Metal Oxide Semiconductor
PCB	Printed Circuit Board
PMOS	Positive-Channel Metal Oxide Semiconductor
Quatro	Quad-node Ten Transistor Cell
RC	Resistor-Capacitor
SBU	Single Bit Upset
SE	Soft Error
SEE	Single Event Effect
SEL	Single Event Latch-up
SEMU	Single Event Multiple Nodes Upset
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SNM	Static Noise Margin
SOI	Silicon-On-Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
TCAD	Technology Computer Aided Design
TMR	Triple Modular Redundancy
TSMC	Taiwan Semiconductor Manufacturing Company
VDD	Voltage Drain Drain
VSS	Voltage Source Source

CHAPTER 1: INTRODUCTION

1.1 Background and Motivation

Particles from space and terrestrial radiation environments pose great dangers to integrated circuits (ICs). In the 1970s, Binder et al. were first to report upsets in a communication satellite caused by cosmic rays [1]. Before long, engineers at Intel discovered that alpha particles could cause nonrecurring errors in terrestrial memory devices [2], and they proposed the term "soft errors" for the first time to define random and recoverable faults caused by particle irradiation [3]. When a single energetic particle in a radiation environment strikes a microelectronic device, electron and hole pairs are generated along the path of the particle in semiconductor materials. The charge is collected by reverse-biased p-n junctions or diffusion regions, and causes voltage transients at the associated nodes. If the transient occurs in a combinational logic circuit, it is referred as a Single Event Transient (SET) [4]. If the SET occurs inside or is latched into a storage cell, it is called a Single Event Upset (SEU) [5]. The data errors caused from SETs and SEUs cannot damage the circuit itself, so they are often referred to as soft errors, which are defined as the random errors generated from particle striking. The generated charges may also trigger a parasitic thyristor structure and a direct and short current path between the power and the ground in Complementary Metal-Oxide Semiconductor (CMOS) Bulk technologies, which is referred as a Single Event Latch-up (SEL). A SEL can only be recovered by power recycling, which induces a significant reliability hazard for space instrumentation. These phenomena are generally termed Single Event Effects (SEEs) in microelectronics [6].

Besides charged particles like heavy ions, protons, and alpha particles, non-charged particles such as neutrons can also induce soft errors [5]. Unlike heavy ions and alpha particles which directly ionize semiconductor materials and generate electron-hole pairs, neutrons can cause soft

errors via indirect ionization, meaning that they react with silicon nuclei and generate secondary charged particles [6]. Heavy ions, alphas, protons, and neutrons comprise the major radiation sources. In a space environment, the abundant existence of protons and heavy ions is the main threat to space instrumentation. As to the electronics at ground level, SEEs are caused by alpha particles emitted from packaging materials and neutrons generated from cosmic rays reacting with the upper atmosphere of the earth.

In well-designed ICs, SEEs appear to be the most troublesome in a space environment or in high-altitude terrestrial environments. SEEs have been reported to be found in microprocessors, memories, network switches, routers, configuration bits in Field Programmable Gate Arrays (FPGA), and even in implantable medical devices (e.g., cardiac defibrillators) in terrestrial electronic systems [6]. The error rate can be as much as 50,000 FIT (Failure-In-Time: 1 failure per 10^9 hours of device operation), while the typical hard failure (e.g., gate oxide breakdown, metal electromigration, latch-up) rates in ICs add up to only 5-200 FIT [2]. For example, in 1999-2000, Sun Systems' flagship servers, which had a selling price of $500,000 to $1 million USD dollars, encountered an unacceptably high system failure rate due to SEEs found in the memory cards. It took engineers a year to fully understand and solve the problems. This cost Sun Systems tens of millions of dollars and an enormous number of man-hours in technical debugging and in debriefings with customers. Furthermore, Sun's brand image was damaged and the company was criticized for the poor treatment of their customers.

During the last forty years, scaling of silicon technologies has greatly improved the performance of ICs in terms of power, speed, and integration. However, the continuous scaling means more transistors per unit area, smaller power supply voltage, higher clock frequency, less node capacitance, and more complexity of circuits, all of which make the circuits more vulnerable to SEEs. For example, the strike of a particle usually causes only a Single Bit Upset (SBU) in

Static Random Access Memories (SRAM) manufactured in less advanced technologies. However, it can cause Multiple Cells Upset (MCU) in advanced technologies. Figure 1.1 shows the trend of SBU and MCU ratios with the scaling of technology nodes in SRAMs [7], illustrating that SEEs can have worse impacts on circuits in modern technologies.

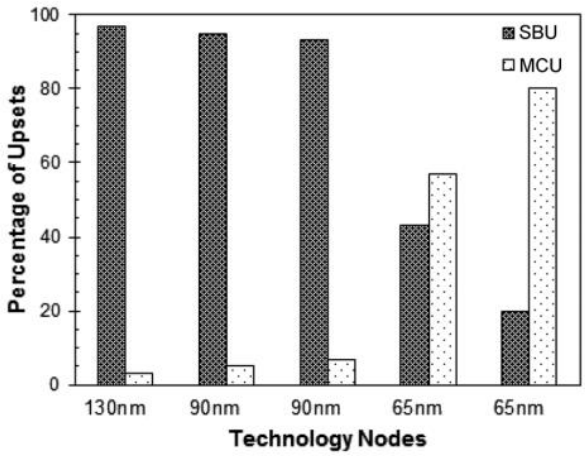

Figure 1.1 Percentage of upsets with the shrinking of technology nodes [7]

Researchers and engineers have been continuously studying the radiation effects in microelectronics and exploring radiation hardening techniques in circuits and systems. Generally, mitigation techniques of SEEs can be classified into three categories: system-level, circuit-level, and fabrication-level [5]. A typical example of system-level approaches is Error-Correcting Codes (ECC), which add extra parity bits to correct erroneous bits in memories [8]. In general, the ECC method is more effective in memory applications. Fabrication-level methods are based on fabrication, which can greatly improve the tolerance of SEEs by changing fabrication processes. Triple-well [9] or quadruple-well structures [10] and Silicon-On-Insulator (SOI) substrates [11] are widely used. Circuit-level designs, which are the focus of this thesis, contain schematic and layout hardening methods. Circuit-level methods have high flexibility and are independent of fabrication processes, since they can be applied to basic cells or blocks, or to whole circuits. Through spatial or temporal redundancy of sensitive nodes or devices, the single event tolerance can be improved

from a schematic perspective. For example, a Dual Interlocked Storage Cell (DICE) was introduced to achieve SEU tolerance by storing two pairs of complementary values instead of one pair [12]. A Quad-node ten transistor cell (Quatro) is another SEU-tolerant storage design, which reduces soft error rate (SER) by 98% compared to its regular counterpart in a 90nm CMOS technology [13]. In the layout-level, node separation and guard rings are broadly used to mitigate SEE [14]. Layout Design Through Error-Aware Transistor Positioning (LEAP) is one of the newest approaches in layout-level, showing 5 times the improvement over the regular layout method in a 180nm CMOS technology [15].

Many methods listed above were proposed to improve the SEU resistance of storage cells in sequential circuits. SET glitches in combinational logic circuits do not necessarily cause failures because of various masking effects [2]. However, studies show that soft errors caused by the SETs in combinational logics can contribute significantly to the overall errors when clock frequencies are in gigahertz range or higher [16]. The traditional methods include, but are not limited to, increasing the transistor size, using guard drains in layout, and using spatial or temporal redundancy. However, the complexity of logic circuits increases the difficulty of finding a universal hardening method. Taking into account the factor of high operating clock frequencies, it is necessary to improve the radiation tolerance of combinational circuits.

1.2 Objectives

The overall objective of this thesis is to propose radiation hardening designs at the circuit-level to reduce soft errors induced by SEEs. Schematic methods and layout methods will be used to improve the radiation tolerance of sequential circuit cells and combinational logic circuits. The approach taken is as follows:

1. Develop a latch that is immune to alpha particles with minimum overhead.

Radiation at ground level may bring soft errors to electronic devices and cannot be ignored. The effectiveness against a particle strike will be evaluated using sophisticated Technology Computer Aided Design (TCAD) simulation tools. A flip-flop chain containing the proposed design will be implemented in a 65nm CMOS Bulk technology test chip. Alpha-particle and heavy-ion exposures will be performed to verify its capability against ground-level and space-level radiation.

2. Design radiation hardening logic gates based on Cascode Voltage Switch Logic (CVSL) and dynamic logic gates.

Combinational logic circuits are more prone to SETs with high clock frequencies. With the development of high speed processors and devices, reducing or shortening SETs in logic gates is more important than ever. To evaluate the effectiveness of radiation resistance, simulations will be carried out to analyze SET characteristics of reference and proposed designs. The performance of area, power, and delay will also be measured in the 65nm CMOS Bulk technology.

The steps below are followed to accomplish the objectives:

1. Study the background of SEEs, including the mechanism of particle radiation, the main sources, and their impacts on sequential and combinational circuits.

2. Summarize the current various SEE resilient designs from schematic-level to layout-level.

3. Propose a radiation hardening latch and two fault-tolerant logic gates, and analyze their SEE resistance.

4. Perform particle incidence simulations by soft error simulators on proposed and previous hardening designs to evaluate their effectiveness of SEU/SET mitigation.

5. Build test benches for proposed designs and their counterparts and do simulations using Spectre to compare their area, delay, and power dissipation.

6. Design and fabricate a test chip which contains the proposed flip-flop chain. Since charge sharing is more obvious in advanced Bulk technologies, resulting in a lower upset threshold, 65nm Bulk technology is chosen as the fabrication process.

7. Implement a test system and carry out alpha and heavy-ion experiments to evaluate the SEU-tolerant performance of the proposed design and its counterpart.

1.3 Thesis Organization

Chapter 1 of this study gives the background of radiation and explains the motivation of this thesis. Objectives are also presented in this chapter. Chapter 2 introduces the background of radiation effects and Single Event Effects. Chapter 3 provides a review of the current radiation tolerant designs on sequential and combinational circuits. Chapter 4 presents the proposed hardening latch design and Single Event Upset (SEU) simulations. Chapter 5 introduces the two proposed combinational logic gates and analyzes their radiation hardening performance by using TCAD simulations. Chapter 6 describes the test chip in 65nm CMOS technology and the test system for alpha and heavy-ion experiments. Radiation test results are also analyzed in this chapter. Chapter 7 is the summary and conclusions of the thesis.

CHAPTER 2: RADIATION EFFECTS BACKGROUND

2.1 SEE Basic Mechanism

As mentioned in chapter 1, Single Event Effects (SEEs) come from an energetic particle strike on an integrated circuit (IC). When striking the semiconductor material, the energetic particle loses energy quickly. Based on Energy Band theory, this energy makes electrons jump from the valence band to the conduction band, so that there are electrons in the conduction band and holes in the valence band. During this process, electron-hole pairs are generated. These generated electrons and holes will be recombined eventually if there is no electric field. However, if this happens in a reverse-biased junction where a high field exists, the depletion layer can help collect carriers through the drift process. Thus, a reverse-biased junction is the most sensitive area of a circuit.

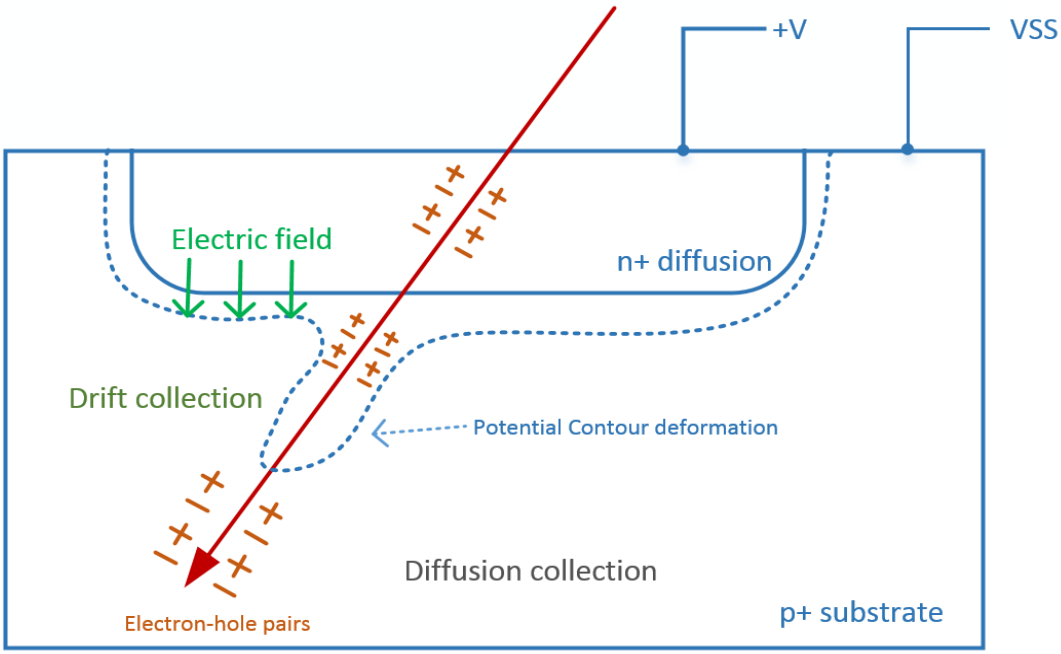

Figure 2.1 Basic mechanism of a strike in a reverse-biased junction

Figure 2.1 details the basic mechanism when a strike happens in a reverse-biased junction[17]. As shown, when the N diffusion connects to Voltage Drain Drain (VDD) and the P substrate connects to Voltage Source Source (VSS), the reverse-biased junction is formed. The high electric field present in the depletion part is from the N diffusion to the P substrate. According to Baumann's study, at the beginning of the particle striking, a cylindrical trajectory exists whose radius is less than one micron [17]. This cylindrical trajectory is full of electrons and holes. These concentrated electrons and holes neutralize those in the depletion region around the trajectory, and, at the same time, the high electric field helps collect electrons into the N diffusion and holes into the P substrate. Thus, electrostatic potential changes, and potential contour deforms, as shown in Figure 2.1. This funnel-shaped depletion area (termed "field funnel") can also raise the charge collection in return because it extends deeply into the P substrate [18]. After tens of picoseconds, drift collection caused by the electric field is finished, resulting in electrons concentrating in the N diffusion and holes concentrating in the P substrate. From the perspective of the circuit, a current pulse is shown on the node struck. A voltage perturbation can be captured [19], which may change the logic state of this node and cause a soft error. Following the drift process described above, diffusion collection dominates the event. This diffusion process assists the recombination and diffusion of carriers from this area. Nanoseconds after the strike, all carriers are removed and disappear. During the whole process, a current pulse is formed in the struck node.

The incident particle lost its energy when penetrating the silicon material and generating electron-hole pairs. To quantify the damage strength in a semiconductor material from the injection of a charged particle, the terminology LET (Linear Energy Transfer) is used broadly [20]. The definition of LET is the deposited energy per unit length of an incident particle. Due to the differences in injected materials, LET is normalized with the density of the target material. Its unit is $MeV \cdot cm^2/mg$.

$$LET = \frac{1}{\rho}\frac{dE}{dL} \tag{2.1}$$

In equation (2.1), E represents Energy with the unit MeV, L is Length with the unit cm^2, and ρ is density with the unit mg/cm^3 [21].

In silicon, 3.6eV is needed to generate an electron-hole pair. With the charge of one electron $1.6*10^{-19}$C and the density of Si $2.33g/cm^3$, Naseer et al. showed how to transfer the unit $MeV \cdot cm^2/mg$ to pC/μm [22], which is also generally used to express the magnitude of LET.

When LET = 1pC/μm, it means that 1pC charge is deposited per unit length (μm), so the deposited electron-hole pairs per μm is $\frac{1pC/\mu m}{1.6*10^{-19}C}$. The energy per μm is $\frac{1pC/\mu m}{1.6*10^{-19}C} \times 3.6eV$. LET can be obtained after normalized by the density of silicon, $\frac{1pC/\mu m}{1.6*10^{-19}C} \times 3.6eV \div 2.33g/cm^3$.

$$\frac{1pC}{\mu m} \Leftrightarrow \frac{\frac{1pC}{\mu m}}{1.6*10^{-19}C} \times 3.6eV \div \frac{2.33g}{cm^3} = 96.57MeV \cdot cm^2/mg \tag{2.2}$$

According to equation (2.2), 97 $MeV \cdot cm^2/mg$ LET value can be expressed as 1pC/μm. In general, an approximation of 1pC/μm = 100 $MeV \cdot cm^2/mg$ is used for convenience. From the definition of LET, we know that LET is related to the energy and mass of incident particles, and the materials struck by the particles [6].

2.2 Sources of Radiation

There are three radiation sources for SEE in space: particles in the earth's radiation belts called Van Allen Belts, particles from solar activities, and particles from galactic cosmic rays. On earth, the neutron particles in the atmosphere and alpha particles in packaging materials can also induce soft errors via indirect or direct ionization [23]. Alpha particles, heavy ions, neutrons, and protons will be introduced in the following sections.

2.2.1 Alpha Particles

The first soft errors of SEE discovered on earth were caused by alpha particles in packaging materials of chips. These soft errors had a negative impact on the function of circuits [24].

Alpha is a doubly ionized helium atom (He^2), which is the product emitted by the emissive decay of radioactive materials. An alpha particle consists of two neutrons and two protons, so that it carries a charge of +2, and its mass is 4 times that of a hydrogen atom. In a package of integrated circuits, there are small amounts of radioactive isotopes, such as uranium and thorium. When they decay, high energetic alpha particles are generated with the energy varying from 3.95 to over 9 MeV [24]. It has already been verified that alpha particles with 5 MeV or less can pass through silicon and cause upsets in dynamic memories. Alpha particles cannot travel far and a piece of paper can stop them easily. For example, polyimide can block alpha particles, so it is often used in fabrication processes.

For this thesis, alpha-particle radiation experiments were carried out at the University of Saskatchewan. An americium-241 5.5MeV alpha source was placed on top of a chip whose top lid was removed before the experiments. This alpha source has 2.5uCi activity and $4.61*10^7 a/cm^2/h$ emissivity.

2.2.2 Heavy Ions

Heavy ions are those charged particles heavier than protons and their atomic numbers are higher than 1, including charged helium, carbon, and neon ions. They have more than one unit of electric charge, for example, carbon-12, neon-22, calcium-45, iron-56, uranium-238, and krypton 84. Through direct ionization, a heavy ion strikes circuit devices, generating abundant electron-hole pairs along with the ionic track. The Linear Energy Transfer of heavy ions is from 1 $MeV \cdot cm^2/mg$ to 100 $MeV \cdot cm^2/mg$ [25].

The very first observation of soft errors in space was from the radiation of heavy ions [26], opening the door to the study of space radiation effects and radiation hardening technologies for space semiconductors. After that, for convenience, heavy ions were generated by accelerators, which could simulate space radiation environments and be used for radiation experiments on earth. Accelerators allow various types of ions, from Ar to U, to generate different LET beams of heavy ions. These accelerators speed up charged ions to high-level velocity, almost near the speed of light. Using accelerators for radiation experiments on earth helps to control the radiation environment, and to choose the types, energy, and intensity of ions. Repeated experiments and a large number of trials become possible via this method, which advances the study of radiation hardening.

For this thesis, we did heavy-ion experiments at the HI-13 Tandem accelerator, China Institute of Atomic Energy (CIAE), Beijing, China.

2.2.3 Neutrons

Neutrons are the product of nuclear fusion, nuclear fission, radioactive decay, or other reactions. Neutrons and protons, which will be introduced in the next section, constitute the nuclei of atoms. A neutron has the same mass as a proton, but it has no charge. Since they are not blocked by the coulomb barrier, neutrons can react with most nuclei. At sea level, about 95% of cosmic rays are neutrons [27]. Neutrons in the atmosphere are the end-products when the atmosphere interacts with cosmic rays [25]. The intensity varies with altitude, position in the geomagnetic field, and solar magnetic activities [28].

Neutrons cause soft errors in electrical devices through indirect ionization. One type of neutron radiation damage occurs when high-energy neutrons (10MeV-1GeV) in space react with the nuclei of silicon and generate ions, which can then produce electron-hole pairs via direct ionization. Another type is low-energy or thermal neutrons in space which react with boron (^{10}B)

in packaging materials, generating a lithium ion and an alpha particle [23]. Boron is presented in doped polysilicon, doped wafers, and borophosphosilicate glass (BPSG). When struck by neutrons, boron becomes unstable and loses energy through fission.

2.2.4 Protons

A proton is a subatomic particle with a positive charge of $1.6*10^{-19}$C. There are abundant protons existing in space environments. Protons make up 87% of galactic cosmic rays. The energy of these protons is usually around 1GeV but sometimes is as great as 10^{12} MeV. In addition, particles generated during solar activities include many highly energetic protons. The energy of protons trapped in the Van Allen Radiation Belts varies from several keV to several hundreds of MeV [25].

Protons can affect electronic circuits by direct and indirect ionization. When proton energy is lower than 10 MeV, protons can directly ionize the silicon materials, generating electron and hole pairs, in the same manner as alpha particles and heavy ions [29]. When energy is higher than 20 MeV, protons act like neutrons via indirect ionization by generating secondary charged particles to induce soft errors [30].

2.3 SEU (Single Event Upset)

Digital logic circuits can be divided into two categories depending on the logic function: sequential circuits and combinational circuits. Sequential circuits have memory, which means that not only current inputs but also previous inputs can affect the current outputs. However, in combinational circuits, outputs at any time depend only on the present inputs. Single Event Effects behave differently in these two kinds of circuits. The main components in sequential logic circuits are storage cells, such as flip-flops (FFs) and latches, which can store the data. If an energetic

charged particle strikes a latch, the sensitive node may collect enough charge and upset its state, causing a SEU to occur. For combinational logic circuits, there are no memory-like structures. The collected charge will cause a transient change of current and voltage in the nodes, which we define as a SET in the circuits.

When a charged particle strikes a sensitive node, a current pulse will be generated and may flip the state of the node. We quantify this behavior using critical charge (Q_{crit}). Critical charge is defined as the minimum quantity of charge required to upset a circuit node.

$$Q_{crit} = V_{DD} \times C_{node} \quad (2.3)$$

Equation (2.3) expresses critical charge after first-order approximation. Critical charge depends on the voltage and capacitance of the node. Based on analysis, critical charge is a contributing factor in determining the SER of a circuit. Higher restoring strength and a larger load help increase critical charge and improve radiation resistance [31]. It is easy to conclude that reduced node capacitance and lower power supply voltages in advanced technologies lower the critical charge and introduce more challenges for mitigating the SEEs.

The following is an example showing the mechanism of how a SEU occurs in a D-type Flip Flop (DFF) storage cell.

In Figure 2.2, a DFF consists of two transmission gates and two latches. A back-to-back inverter pair (INV1 & INV2 or INV3 & INV4) is the basic storage element of the latch. The transmission gate contains one Positive-Channel Metal Oxide Semiconductor (PMOS) and one Negative-Channel Metal Oxide Semiconductor (NMOS). When the clock is logic low, the first transmission gate opens, and input data is written into the first latch, and stored in the first back-to-back inverter pair. During this time, the second transmission gate is closed, and the second back-to-back inverter pair keeps the previous data. After a short time, the rising edge of the clock triggers the DFF to output the current data. The first transmission gate closes and the second one opens

when the clock changes from logic low to logic high. At this moment, data in the first latch will be passed to the second latch and be available at the node OUT. Consequently, after the rising edge of the clock, the DFF completes a reading cycle and exports data.

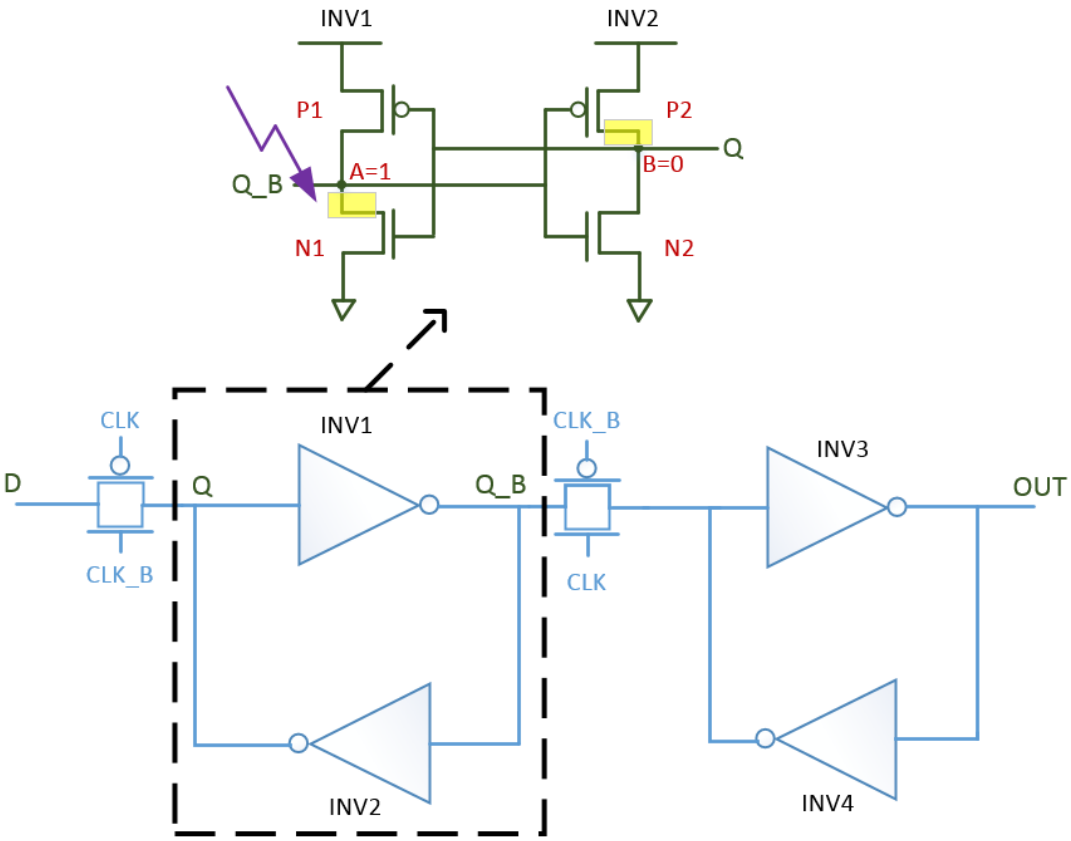

Figure 2.2 DFF and SEU analysis

A SEU occurs in a latch at the hold state, when the clock transition is not considered. For example, the first back-to-back inverter pair is analyzed in the state A=1 and B=0. In this state, Q=0 and Q_B=1, transistors P1 and N2 are open, and P2 and N1 are closed. A reverse-biased P-N junction is the sensitive region for a SEE, so the Drains of N1 and P2 are the most sensitive areas of this latch (marked with yellow). If a strike happens in one of these two Drains (assume the Drain of NMOS), a current pulse will occur. Electrons concentrate in the Drain of N1 and generate a negative pulse in node A. The open transistor P1 drives node A to power VDD by offering a

restoring strength. In the left illustration in Figure 2.3, the purple solid line represents the voltage in node A, and the black dashed line shows the voltage in node B. When the restoring transistor (P1) is strong enough, state 1 in node A can be recovered and will not change the data stored in the latch. If the restoring current from P1 fails to balance the current generated by the strike, which means the collected charge exceeds the critical charge of node A, the state of node A will change from 1 to 0 (the right illustration in Figure 2.3). Because of the feedback structure in the latch, logic low in node A will close N2 and open P2, resulting in node B changing from 0 to 1. Thus, an upset happens in this latch. This is the basic mechanism of a SEU in memory cells.

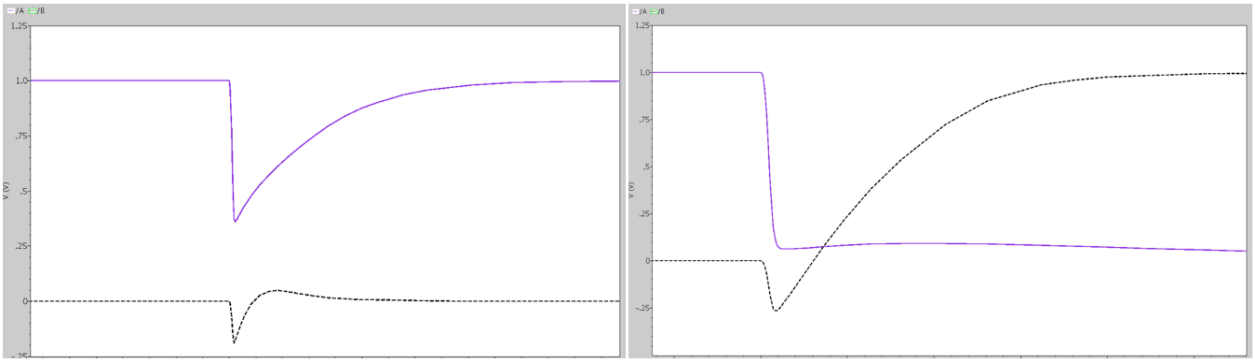

Figure 2.3 Voltage waves with time of storage nodes A and B in low and high collected charges

In general, the possibility for SEUs in memories is called “cross section.” The cross section is the result of the total error numbers of a circuit divided by the fluence of incident ions. Fluence is the total particle numbers passing through a unit area. Cross section also refers to a sensitive area and is expressed in cm^2. Thus, in many papers, the cross section versus LET curve depicts the device’s failure rate at various radiation conditions. Another term, Failure-In-Time (FIT), is used to show the failure rate of devices, which is the number of errors per one billion hours.

2.4 SET (Single Event Transient)

Unlike sequential circuits, there are no feedback structures in combinational circuits. The current pulse caused by charge collection can generate a voltage glitch and propagate along the critical path in a combinational circuit. Only when the glitch is captured by a storage element, such as a register, can a SET generate a soft error, which is a SEU in this case.

In fact, a SET in a circuit will not necessarily cause a failure because of various masking mechanisms, namely logical masking, temporal masking, and electrical masking [2].

Logical masking happens when there is no existing path for the SET to spread, and the fault will be masked. We can take a two-input NOR gate in a combinational path as an example, where if the two inputs are all logic high, the output will be logic low. When a particle strikes one of the inputs changing its value from high to low, the output of this NOR gate will remain logic low, which means that the SET is eliminated by logic masking. Only when particles strike both inputs simultaneously and change their values to logic low, will the output change from logic low to high.

Temporal masking means that a SET in a combinational path will not induce a functional fault to the whole circuit, if the register following this path does not sample this SET. For a positive-edge-triggered flip-flop, data must be stable for some time before the rising edge of the clock. This time is called setup time. If the input changes during the setup time, incorrect data will be captured and cause a setup violation. The time after the rising edge of the clock during which data must remain unchanged is called hold time. A hold violation happens when incorrect data is latched during this time. If a SET propagates along a combinational path and reaches a register during the setup time, or a SET happens in logics inside registers, this SET will cause a SEU [32]. In deep sub-micron processes, the SET pulse width in digital logics can be hundreds of picoseconds, while the clock speed rises steadily from megahertz to gigahertz. Thus, it is relatively easier for SET pulses to be captured by registers.

If a SET pulse in an input is shorter than the delay of the logic gate, it will be masked and cannot cause any soft error. This occurrence is called electrical masking. The allowable noise voltage on the input of a gate is determined by noise margin. A higher noise margin means larger noise is allowed by the logic gate, and thus, the logic gate has better noise resistance. For example, if the output of the first level of a combinational logic path is struck by an energetic charged particle, voltage perturbation caused by charge collection will appear, and this voltage perturbation is the input of the second level of this logic path. Next, consider the output of the second-level gate. If the voltage perturbation is lower than its noise margin, the SET will be masked through an electrical masking mechanism. With CMOS technology scaling, gate delay becomes shorter, so narrower SETs can propagate through combinational paths, which poses a challenge in mitigating soft errors in advanced technologies. In addition, Massengill et al. report that SETs in combinational chains can result in pulse broadening, depending on specific circuit configurations and technologies [33]. The research on SETs in combinational circuits attracts much attention due to the challenging factors.

This chapter details the basic mechanism of SEEs when a charged particle strikes semiconductor materials. A brief introduction of radiation sources is included. Following that, SEUs in sequential circuits and SETs in combinational circuits are explained using typical examples. In the next chapter, SEE mitigation techniques will be reviewed and some typical radiation hardening designs will be presented.

CHAPTER 3: CURRENT SEE TOLERANT DESIGNS

Currently Bulk and SOI are the two main silicon CMOS technologies. Figure 3.1 is a simplified diagram showing the difference between Bulk NMOS and SOI NMOS transistors. Silicon-On-Insulator (SOI) adds a layer of insulation oxide under the transistor's Source and Drain regions. Through reducing the sensitive volume, SOI technologies can effectively reduce the charge collection, and hence, has higher radiation resistance than Bulk technologies [5][11]. In addition, SOI technologies have reduced parasitic node capacitances, which shortens parasitic delay and lowers dynamic power consumption. Most importantly, transistors with SOI technologies are free from latch-up due to the complete isolation from device to device. All these advantages make SOI technologies an attractive option for the silicon industry to reduce SERs in electronic circuits.

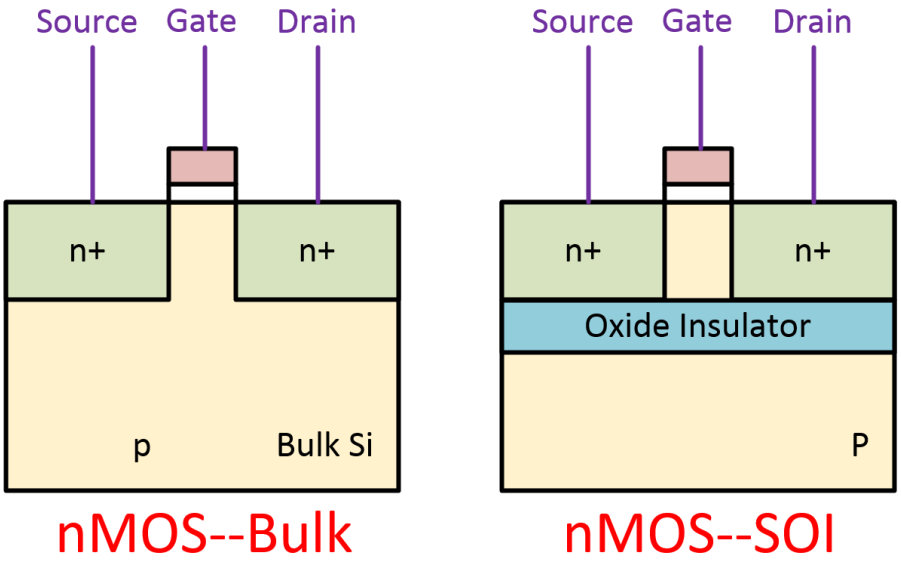

Figure 3.1 Bulk NMOS and SOI NMOS

With the continuing study of radiation effect mechanisms in Bulk and SOI technologies, mitigation methods have been developed not only at the circuit-level but also at the layout-level.

Section 3.1 provides a brief introduction of basic SEE-tolerant designs. Section 3.2 details the current circuit-based hardening designs, including Triple Modular Redundancy (TMR), Guard-Gate, DICE, and Quatro. Section 3.3 discusses layout-based mitigation theories (e.g., charge sharing and pulse quenching) and corresponding radiation hardening layout designs.

3.1 Basic Mitigation Approaches

Initially, researchers focused on SEU-tolerant designs for storage cells because clock frequencies were not very fast and SETs in combinational circuits were not significant with lower operating frequency. Generally, two back-to-back inverters are the storage elements in most of the storage cells, as shown in Figure 3.2. The occurrence of a SEU depends on two factors: the recovery time of the struck node voltage and the propagation time for the SET pulse to propagate through the feedback loop. For example, if a strike happens in the Drain of an "OFF" NMOS, there will be a current transient in the struck node, which will cause a negative voltage pulse. The "ON" PMOS of this node will eventually balance the voltage pulse and drive the node back to logic 1. At the same time, the voltage pulse will propagate to the other node through the feedback structure and upset the state if the pulse width is long enough. The time of this propagation is called cell feedback time. In cross-coupled inverters, cell feedback time can be simplified as Resistor-Capacitor (RC) delay. The competition between a SET's recovery time and cell feedback time determines whether a SEU happens [5]. The shorter RC delay a memory cell has, the more susceptible to SEUs it will be.

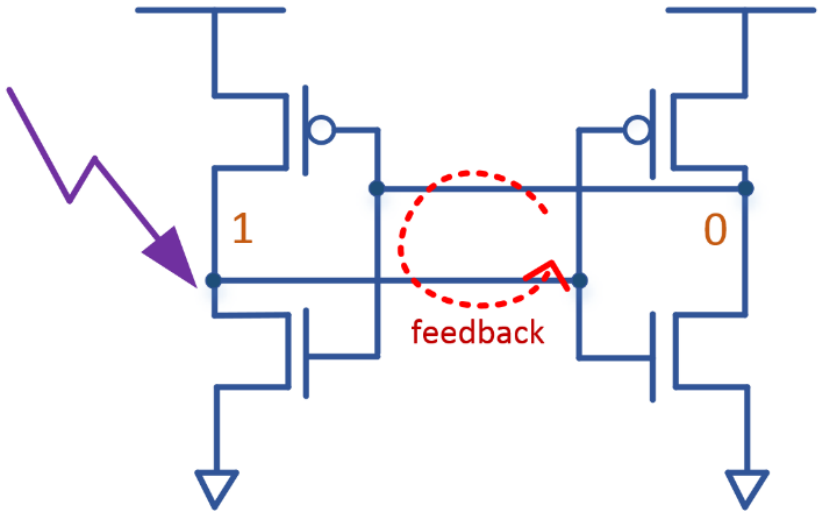

Figure 3.2 Feedback structure in a back-to-back inverter pair

Early mitigation methods focused on these two parameters by either decreasing the SET recovery time or increasing the cell feedback time. Decreasing the SET recovery time can be realized by increasing the size of transistors in the inverters, where larger transistors can provide a larger driving current to recover the struck node. However, using this method causes extra area and power consumption. To increase the cell feedback time, resistance or capacitance can be added into the feedback loop, as shown in Figure 3.2 [34]. Adding capacitance at critical nodes can also increase the critical charge. Resistors, diodes, transistors, or capacitors are used in different places of the feedback path to increase SEU resistance[35][36][37]. The cell feedback time method reduces SEUs in memory cells at the price of larger area, more power consumption, and slower operating speed. With the need for high speed circuits, new approaches and elegant designs are required.

3.2 Redundancy-based Mitigation Methods

More complex mitigation methods involve the redundancy of information instead of simply increasing the critical charge of storage nodes. For example, reproducing data spatially or

temporally can help reduce the probability of SEEs. Multiple copies of inputs or outputs and differential inputs or outputs are also used to implement this concept. The next three sections will introduce four advanced designs which fully take advantage of this concept.

3.2.1 TMR

Triple Modular Redundancy (TMR) has a straightforward structure and is widely used in commercial and space applications. Lyons et al. were first to apply the TMR method in radiation hardened equipment [38]. Figure 3.3 shows the basic form of the TMR method, where a majority voter is added to vote on the outputs from three identical modules.

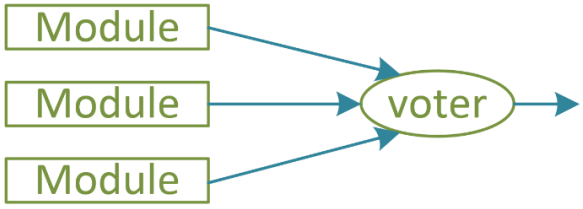

Figure 3.3 Illustration of the TMR principle

In sequential circuits, the module can be an unhardened latch or a regular DFF. All latches or flip-flops share the same clock and input data. If a strike hits one of the latches or flip-flops and causes a SEU, the majority voter can filter this SEU and output the correct data from the other two unaffected modules. The majority voter can be built by using combinational logics, so TMR is SEU-free and susceptible to SETs. The disadvantages of the TMR approach are the large area and power consumption, which can be 3~4 times greater than a single module.

3.2.2 Guard-Gate

A guard-gate is also called a Muller C-element. Figure 3.4 shows the basic structure of a guard-gate. When input A equals input B, the guard-gate behaves the same as an inverter. When

input A differs from input B, the output of the guard-gate is in a high impedance state and maintains its previous value [39].

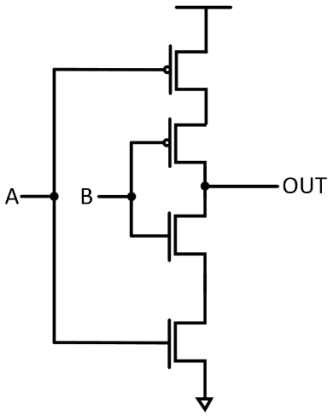

Figure 3.4 Schematic of a guard-gate [40]

The application of guard-gates in combinational circuits is illustrated in Figure 3.5. With inputs A and B replaced by the normal and delayed outputs of a combinational circuit, the guard-gate can remove the SET pulses in this combinational circuit if the SET pulse width is shorter than the delay unit, and output correct data to the following flip-flop. In other words, the guard-gate can mask the SET pulses whose width is shorter than Δt delay [40].

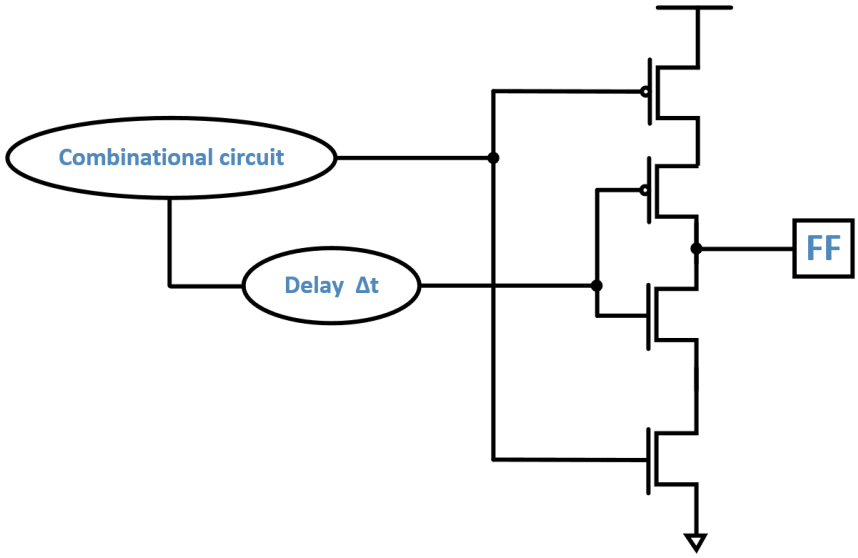

Figure 3.5 Guard-gate used in a combinational circuit

3.2.3 DICE

A Dual Interlocked Storage Cell (DICE) is a spatial redundant design, which has been used broadly since it was first proposed in 1996 [12]. Figure 3.6 shows the structure of a DICE cell. It has 4 storage nodes (A, B, C, and D) instead of 2 for redundancy purposes. In these four nodes, B and D have the complementary value of A and C. For example, assume nodes A and C are logic low (0), and B and D are logic high (1). Then, transistors N1, P2, N3, and P4 are "ON," whereas P1, N2, P3, and N4 are "OFF." The Drain of the P1 transistor is sensitive to a SET. If a particle strikes node A, a positive voltage pulse will occur at this node. The "ON" transistor N1 will drive node A to suppress this positive pulse, which may turn off P2 and turn on N4. Node B will be floating and retain its value when P2 and N2 are OFF. If N4 is ON, there will be a competition between P4 and N4 to determine the voltage level on node D. Even if N4 dominates, which drives the voltage on node D from high to low and turns N3 off, node C will retain its value and be floating in this worst case. Finally, once the positive SET pulse disappears, all the storage nodes in the DICE cell will restore their values. In conclusion, the DICE structure is immune to a SEU if only a single node is affected.

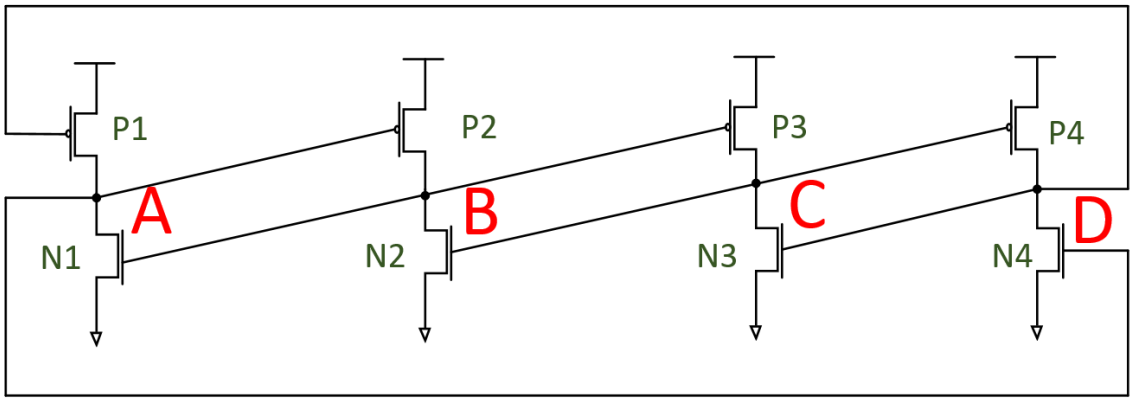

Figure 3.6 Dual Interlocked Storage Cell (DICE) [12]

In order to write into the DICE, at least two nodes need to be accessed simultaneously to achieve a successful write operation. Compared to the TMR structure, a DICE has smaller area and power dissipation. It has no static current path between power and ground during static mode. Another advantage of the DICE is that the transistors do not have to be specifically sized. Based on these benefits, the DICE structure is commonly used as a SEU-tolerant storage element. However, there are also some drawbacks for this design. The most obvious disadvantage is the occurrence of a SEU when two of the nodes are struck simultaneously. Researchers have made efforts to solve this problem. One example is the combination of the DICE structure and the guard-gate, as shown in Figure 3.7, which is also called a 4-TAG latch. Radiation experiments have shown that no error occurred even at 175 MeV·cm^2/mg LET value in the AMI 0.5μm process [41].

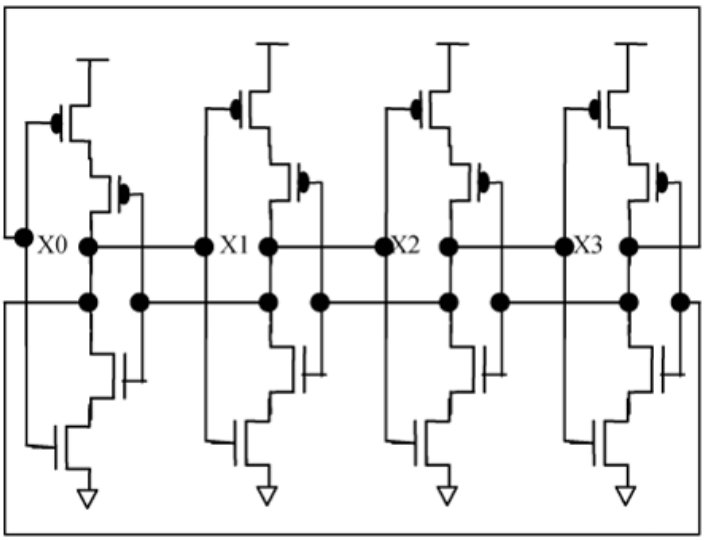

Figure 3.7 DICE latch with 4 guard-gates [41]

3.2.4 Quatro

The Quad-node ten transistor cell (Quatro or Quatro-10T) is another popular SEU-tolerant storage cell design [13]. This Quatro-10T cell was proposed firstly as a hardened memory cell of

SRAM. It can also be used as a latch cell in sequential circuits. Figure 3.8 shows the structure of a Quatro-10T cell.

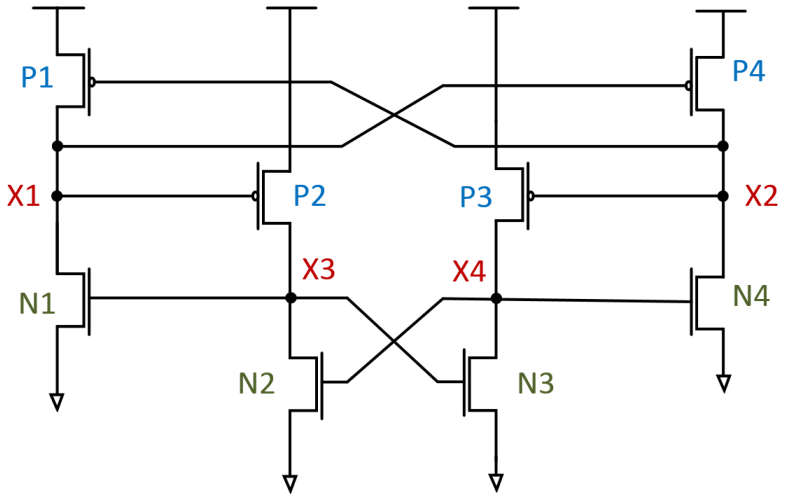

Figure 3.8 Quatro-10T cell [13]

With the symmetrical structure, the Quatro cell stores differential data in 4 nodes (X1, X2, X3, and X4). X1 and X4 have the same value, as do X2 and X3. This Quatro-10T cell is immune to a positive pulse in node X1 or X2, and immune to a negative pulse in node X3 or X4. For example, assume X1 is logic low (0) and X2 is logic high (1). If a positive pulse occurs in X1, the "ON" transistors P2 and P4 will be turned off, resulting in nodes X3 and X2 floating and unchanged. If node X3 has a negative SET pulse, the "ON" transistors N1 and N3 will be turned "OFF," resulting in X1 and X4 floating and maintaining their values. However, a negative pulse in node X1 or X2 and a positive pulse in node X3 or X4 may cause SEUs. For example, the negative SET pulse in node X2 will turn on both P1 and P3, causing competitions in nodes X1 and X4. If the SET pulse is large enough, the competitions will flip the Quatro cell and a SEU will occur. Appropriate size of transistors can reduce the competitions and help the Quatro cell improve its robustness.

It is reported that the Quatro-10T cell has a larger noise margin and lower leakage current than a DICE cell, and the SER of a Quatro-10T cell SRAM is reduced by 98% compared to the unhardened standard 6T cell, as shown in Figure 3.9 [13].

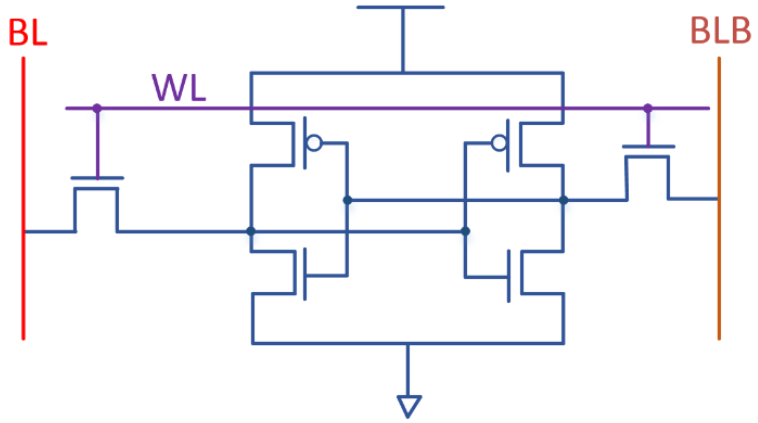

Figure 3.9 Regular 6T cell

3.3 Layout-based Mitigation Methods

With technologies scaling, shrinking of transistors results in a higher probability of Single Event Multiple Nodes Upset (SEMU). A SEMU caused by a single particle strike was observed firstly in SRAMs [42]. Charge sharing theory is proposed to explain this phenomenon. Researchers have made great efforts to reduce charge sharing, and hence, SEMUs as well as SERs. However, it becomes more challenging in the most advanced technologies, such as 40nm and 28nm technologies. On the other hand, some researchers started to use the mechanism of charge sharing to mitigate the single event effects, which led to layout-based hardening design techniques in addition to circuit-based mitigation approaches. In the next section, the mechanisms of charge sharing and pulse quenching will be detailed first, and then, several layout-based mitigation methods will be introduced, including node separation, guard rings, and Layout Design Through Error-Aware Transistor Positioning (LEAP).

3.3.1 Charge Sharing and Pulse Quenching

Besides diffusion and drift process, parasitic bipolar effect plays a significant role during charge collection. Figure 3.10 shows the cross section of both PMOS and NMOS transistors. If an energetic charged particle strikes the n-well when the Source of the PMOS is logic high and the Drain is logic low, electron-hole pairs will be generated, and electrons will be concentrated around the n-well because of the electric field between the n-well and p substrate. These collected electrons will decrease the potential of the n-well. The P-N junction between the Source and the n-well will be forward biased, and the P-N junction between the Drain and the n-well will be reverse biased. The lateral parasitic bipolar in the n-well will be turned on. For this bipolar transistor, the Drain is acting as the Collector, the n-well is the Base, and the Source is the Emitter. The amplification of this bipolar transistor will increase the Drain voltage, resulting in a positive pulse. In the NMOS device, the mechanism is the same as in the PMOS device. However, because the voltage perturbation of the P substrate is not so obvious as that of the n-well, the parasitic bipolar effect in the NMOS is not as significant as in the PMOS. With the shrinking of the feature size of transistors, the shorter the gate length, the larger the bipolar current gain [43].

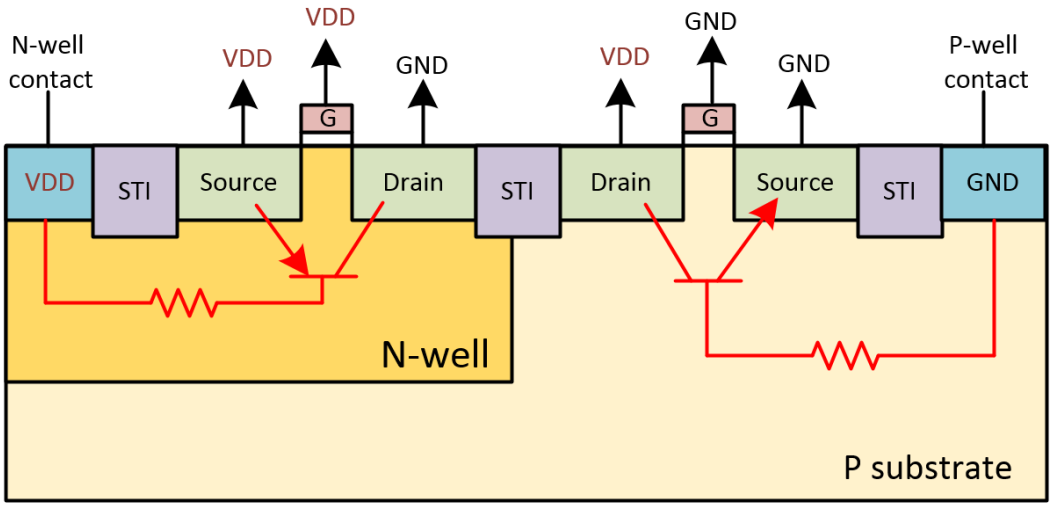

Figure 3.10 The cross section of CMOS transistors and the illustration of the parasitic bipolar transistors

When the distance between a hit device and neighbouring devices is large, such as in the less advanced technologies, generated carriers only concentrate on the vicinity of the hit device. However, technologies scaling results in less charge needed to represent a logic state, and generated carriers can affect adjacent devices due to the diffusion process. Amusan et al. studied the charge sharing between an active node and the passive node of adjacent MOS devices in the same well, as shown in Figure 3.11 [14].

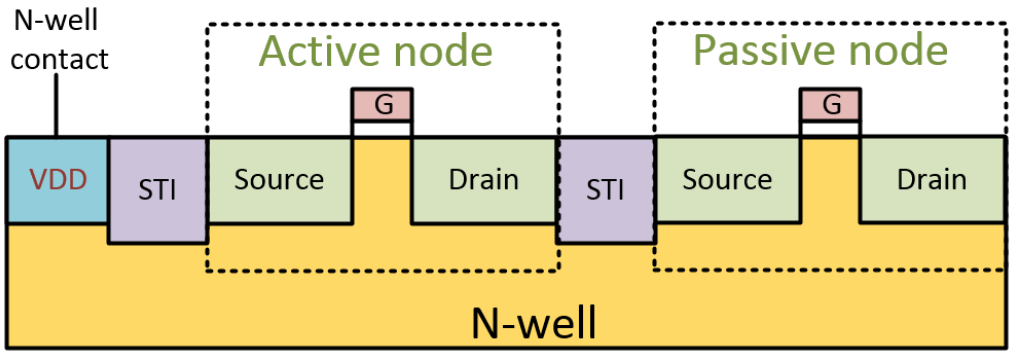

Figure 3.11 Diagram of an active node and passive node affected by charge sharing

Because of the diffusion process and parasitic bipolar mechanism in the n-well caused by a charged particle, the parasitic bipolar transistor of the passive PMOS can be turned on. In PMOS devices, the parasitic bipolar effect in the passive node is dominant over the diffusion process. The existence of the bipolar transistor will increase the total collected charge in both the active and passive nodes. If there is only a single node collecting these carriers, some generated carriers will be recombined in the end. However, because of the absence of a well-like structure and relatively stable voltage of the p substrate, diffusion is still the main mechanism of charge sharing in NMOS devices. In both PMOS and NMOS transistors, increasing the distance between the active and passive nodes can help to reduce charge sharing and the effect on adjacent transistors. Transistors in separated n-wells have a lower possibility of charge sharing [14]. The existence of the electric

field between an n-well and a p substrate can isolate them, and thus, charge sharing is not prominent in the separated wells.

As to SETs in combinational circuits, pulse quenching is referred to as the effect of charge sharing on SET pulse width. The pulse quenching effect was introduced to describe the phenomenon that SET pulse widths become shortened in certain cases at high LET values [44].

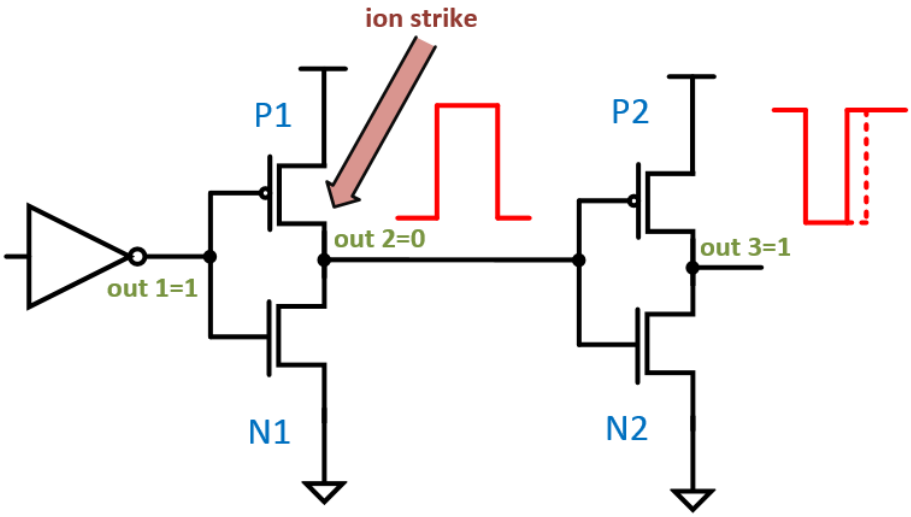

Figure 3.12 Illustration of the pulse quenching effect in a chain of inverters

In Figure 3.12, there is an inverter chain including three inverters. Assume that out1 is logic high, out2 is low, and out3 is high. Transistors P1 and N2 are "OFF," whereas N1 and P2 are "ON." Because of the reverse-biased junction in the Drain of P1, this node is sensitive to SETs. When an ion strikes the Drain of P1, there will be a positive voltage pulse in out2. This pulse will propagate downstream and generate a negative pulse in node out3. Ahlbin et al. observed the interesting phenomenon that the pulse width at out3 is shorter than that at out2 [44]. Through simulations, they found that it is caused by the charge sharing between P1 and P2. At the node out3, there are two voltage transitions. One is a high to low transition from the propagation of the SET at out2. The other is a low to high transition due to charge sharing. When the positive SET pulse generated at out2 propagates to out3, it will turn off transistor P2 and turn on N2. Then the "OFF" transistor

P2 is prone to charge collection. Especially when P1 and P2 are placed closely, the generated charge will be shared between transistors P1 and P2. Carriers diffuse from P1 to P2 and cause a low to high transition at the node out3. This low to high transition reduces the pulse width from out2 to out3 and pulse quenching occurs. Two requirements determine the occurrence of pulse quenching. The first one is the possibility of charge sharing. In less advanced technologies, the distance between transistors is relatively large, so pulse quenching is not as significant as that in advanced technologies. The second one is that the time of charge sharing from the hit device to the adjacent device must be close to the time of a SET propagating from the previous gate to the current gate. If the propagation delay of a SET from one gate to another is much larger than the charge sharing period, pulse quenching will not occur. In conclusion, it is "delayed charge sharing collection" that causes the quenched SETs.

Based on the mechanism of charge sharing and the description of the pulse quenching mechanism, the following layout-based mitigation methods are introduced to reduce charge collection and to improve the radiation tolerance of circuits.

3.3.2 Node Separation

To reduce the SER of circuits, the most direct method at the layout-level is increasing the node distance between two sensitive transistors, which can decrease the possibility of charge sharing. However, this method becomes less attractive with the scaling of transistors because of the large area overhead. A study using a 90nm Bulk CMOS technology shows that charge sharing may occur among multiple PMOS transistors by an angular particle strike because of the n-well potential variation, which means that node separation to 2μm is not enough to suppress SEMU and to decrease SER [45].

An alternative of node separation is interdigitating transistors, which is to place the less-affected nodes between two sensitive nodes [14]. As shown in Figure 3.13, the less-passive transistor is located between an active node and a passive node, so the distance between the active node and passive node can be enlarged. Since the less-passive node is not that sensitive to collected carriers, this node has less chance to experience upset. This method can diminish the SER without using too much area. It is more effective for NMOS transistors than PMOS transistors, because charge sharing caused by the parasitic bipolar effect is not obvious in NMOS transistors, and interdigitation enlarges the distance resulting in mitigation of the diffusion effect.

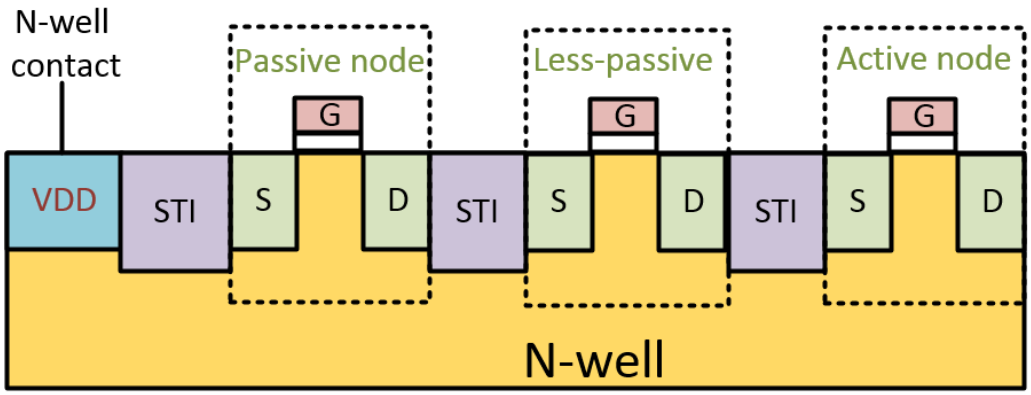

Figure 3.13 Interdigitating of transistors

3.3.3 Well Contact and Guard Ring

As discussed above, in PMOS devices, the main mechanism of charge sharing is the parasitic bipolar effect. Maintaining the voltage of the n-well is an effective method to reduce charge sharing and soft errors. Figure 3.14 is the layout diagram of an inverter with well contacts. A well contact is a high doping diffusion area that maintains well potential. Reducing the distance of a well contact and the struck node can diminish the resistance of the parasitic bipolar transistor, resulting in decreasing the time of potential drop and speeding up the recovery of the well voltage. A guard band is another type of well contact located among PMOS devices to extend horizontal well

contacts. It can also prevent potential perturbation. Simulations in a 130nm technology proved that guard bands could reduce soft errors by 97% in PMOS transistors and by 35% in NMOS transistors at a LET of 40 MeV·cm^2/mg [14]. The mitigation effect is different in PMOS and NMOS transistors because the well contacts and guard bands are used to decrease the contribution of the parasitic bipolar effect, which is not dominant in NMOS devices. Heavy-ion experiment results show that guard bands and high-density well contacts can remove 70% of SETs which are longer than 1ns [46].

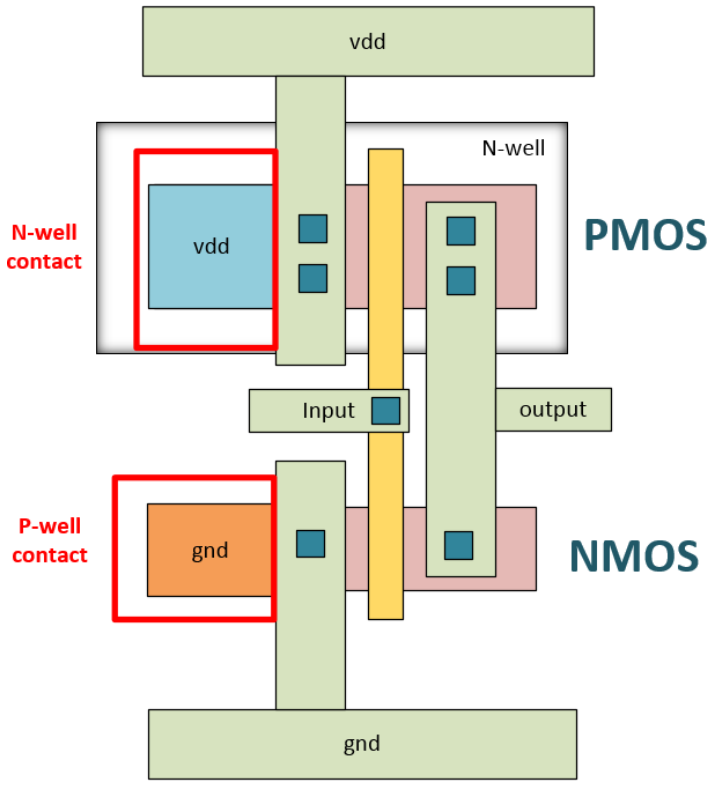

Figure 3.14 Well contacts in PMOS and NMOS transistors

Another design more effective than a guard band is a guard ring. Figure 3.15 shows a transistor surrounded by a guard ring. Besides preventing well potential from collapse, a guard ring can prevent a Single Event Latch-up (SEL). A SEL can enable a direct current path between power and ground rails due to a particle strike. Heavy ion experiment results indicated that the guard ring

structure did not show any improvement over SEUs in DICE circuits, but it was more effective in decreasing the collected charge in passive PMOS transistors than in NMOS transistors with normal and 60˚ strikes [45]. Compared to redundancy methods, area overhead for guard rings or guard bands is not too high. Well contacts and guard rings are still effective methods to improve radiation tolerance, especially for PMOS devices.

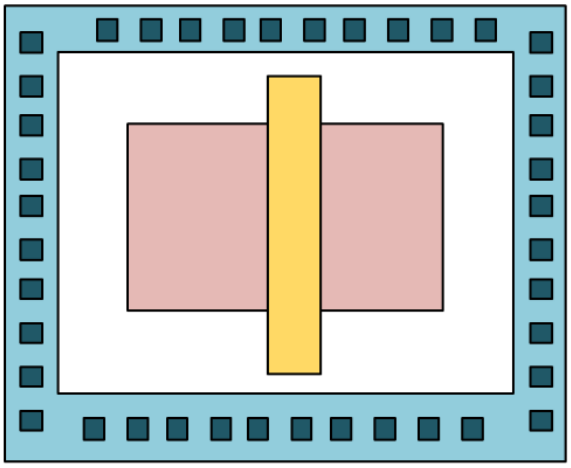

Figure 3.15 Diagram of a guard ring outside of a transistor [45]

3.3.4 Layout Design Through Error-Aware Transistor Positioning

Kelin et al. proposed Layout Design Through Error-Aware Transistor Positioning (LEAP) in 2010 [15]. It is a creative layout-based radiation hardening design, differing from traditional layout mitigation technologies, such as guard bands or guard rings. The basic principle of LEAP is charge cancellation via the layout method to reduce the possibility of multiple node upsets.

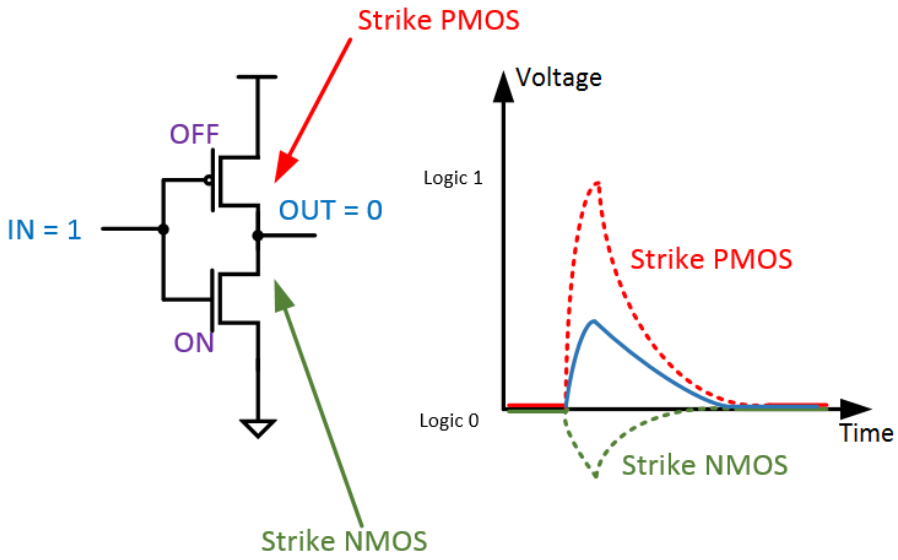

Figure 3.16 Charge cancellation when striking both Drains of the PMOS and NMOS in an inverter

Take a CMOS inverter as the example in Figure 3.16. Because of the existence of an electric field at a P-N junction, electrons will concentrate in N diffusion if an ion hits the Drain of the NMOS, resulting in a voltage drop. Holes will concentrate in the P diffusion if an ion hits the Drain of the PMOS, resulting in a voltage rise. When the input of this inverter is logic high, the output will be logic low. The red dashed line shows that there is a positive voltage pulse in node OUT when an ion strikes the PMOS. The green dashed line indicates that there is a negative voltage pulse in the node OUT when an ion strikes the NMOS. Because the Drain of the PMOS is reverse-biased and the Drain of the NMOS is forward-biased, this PMOS is more sensitive for a particle strike than the NMOS. Thus, the amplitude of the positive voltage pulse is larger than that of the negative pulse. If a particle strikes both the PMOS and NMOS simultaneously, these positive and negative pulses can cancel each other and reduce the pulse at the node OUT (the blue solid line). The principle of the LEAP layout design is to place the Drains of the PMOS and NMOS close to each other, which have opposite effects for a particle strike, as shown in Figure 3.17. The purple

line indicates the horizon which is the protected strike direction, because striking both Drains of the PMOS and NMOS can reduce the SET pulse magnitude of the node.

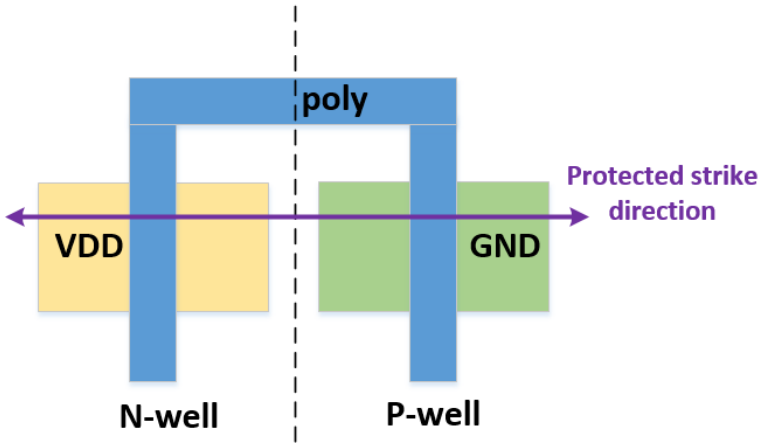

Figure 3.17 Layout of an inverter using LEAP principle

Kelin et al. chose the DICE cell to implement the LEAP technique because the DICE is a reliable design for SEUs but is vulnerable to SEMUs [15]. Figure 3.18 shows the schematic and layout diagram of a DICE cell using the LEAP layout hardening technology. If the states of A, B, C, D are 1, 0, 1, 0, respectively, P1, N2, P3, N4 are "ON," and N1, P2, N3, P4 are "OFF." Node A will drop if an ion strikes the Drain of N1. This negative pulse will turn off N4 and turn on P2, resulting in contention between P2 and N2. This contention will reduce the current of P3, leaving node C weakly driven by P3. Node D will be floating. After a short time, node A will recover because of P1's driving and the recombination of carriers. Thus, the DICE cell is immune to a SEU. However, if the ion strikes in the direction of the orange line, N1 and P2 will be hit simultaneously. In addition, the voltage of node B will change from low to high instead of the intermediate competition state caused by an N1 hit. The state change of both nodes A and B can cause this DICE cell to upset.

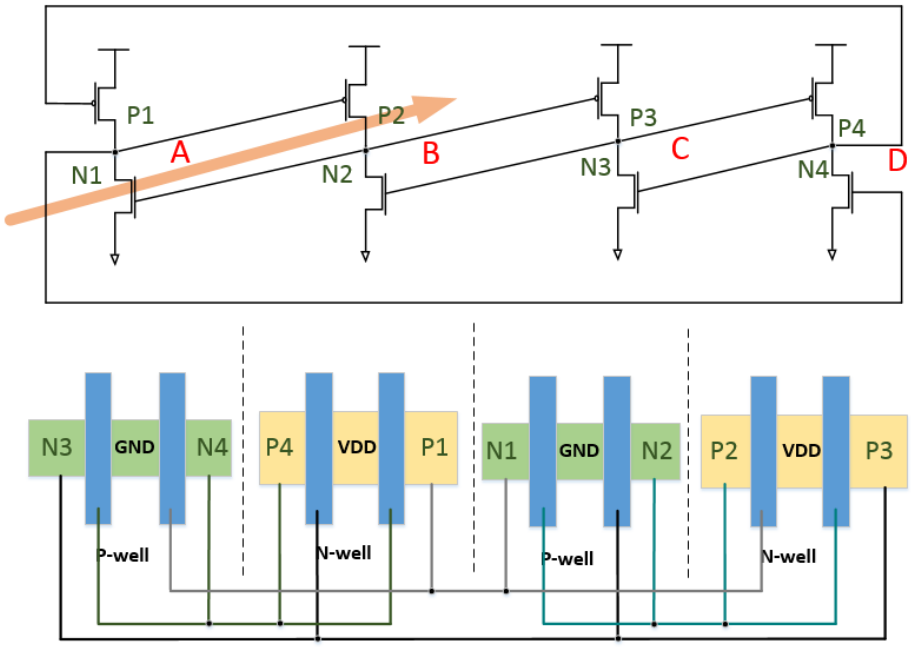

Figure 3.18 LEAP-DICE schematic and layout diagram [15]

Since the DICE cell is not immune to multiple node upsets, a LEAP layout design is proposed to solve this problem. In Figure 3.18, all 8 transistors in a DICE cell are aligned horizontally. For example, placing N2 between N1 and P2 separates these nodes from each other, and cancels the total effect of multiple node upsets. If N2 and P2 are hit simultaneously, the magnitude of the voltage pulse at node B is reduced, which is the same result shown in the inverter, as described in Figure 3.16. Different from the mechanism of N2 and P2, which is called "direct SET suppression," "indirect SET suppression" occurs when N1 and N2 are struck together [15]. The negative pulse created in node A by a particle strike can turn on P2, and then, cause a contention in node B, which may increase the voltage of B. At the same time, striking N2 can generate a negative pulse in node B. This negative pulse will suppress the increasing voltage above and drive B back to its original state. In this way, striking N1 and N2 together is beneficial for the DICE because of charge cancellation. For that reason, N2 is placed between N1 and P2. The other transistors are placed in

a similar way to reduce the overall effect of a SEMU. Besides the horizontal direction, all the other angled directions can be protected from a SEMU. In addition, the structure of P-N-P-N wells is better than P-P-N-N wells because the former structure provides additional isolation to reduce charge sharing. By using the LEAP layout design, the DICE cell is not only immune to SEUs, but also has a lower probability of single event multiple node upsets.

In an 180nm CMOS technology, the SER of the LEAP-DICE improves 2000 times compared to a regular DFF and 5 times compared to the regular DICE [15]. This LEAP-DICE consumes 40% more area and 54% more power than its regular counterpart. The fivefold improvement in SER is not from the extra 40% area, which can only improve SER by 1.75 times, according to the assumption of "2X node separation equals to 10X fewer soft errors" [47]. Lilja et al. implemented LEAP layout designs in a 28nm CMOS technology on DICE cells and D flip-flops [47]. Alpha and neutron experiment results showed that the LEAP-DICE in the 28nm CMOS has no error. According to the heavy ion experiment results, the improvement of the LEAP-DICE compared to the traditional DICE in the 28nm CMOS technology is considerably better than that in the 180nm technology, which means the LEAP layout method is more effective in advanced technologies. The experiment results also show that the LEAP layout technology can help to reduce the DFFs' SERs by 75%.

CHAPTER 4: A RADIATION HARDENING DESIGN IN SEQUENTIAL CIRCUITS

In this chapter, a new Quatro-based SEU-resilient latch design which adds two more transistors is presented. Section 4.1 describes the basic operation of this proposed design and analyzes its SEU tolerance compared to a regular Quatro cell. Section 4.2 compares the SEU performances of the proposed design and the traditional Quatro cell through simulation validation. Section 4.3 compares the power, delay, and area of these two designs.

4.1 Proposed Fault-tolerant Design and SEU Analysis

4.1.1 Proposed Quatro-based Flip-flop Design and Basic Operation

Inspired by the Quatro-10T SRAM bit-cell design [13], a new flip-flop design based on the Quatro structure is proposed in this section.

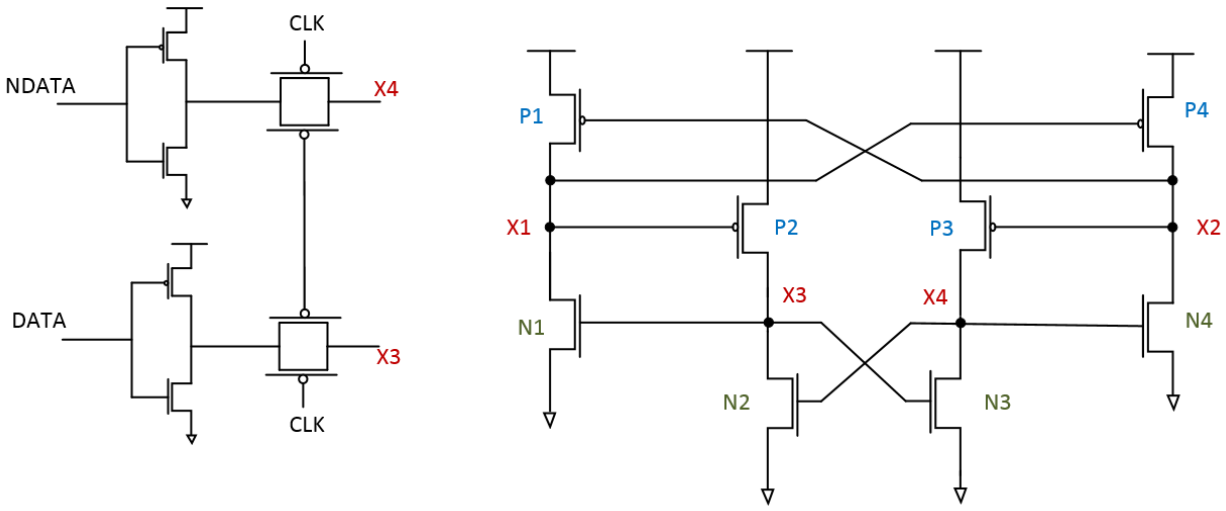

Figure 4.1 Diagram of the regular Quatro latch [13]

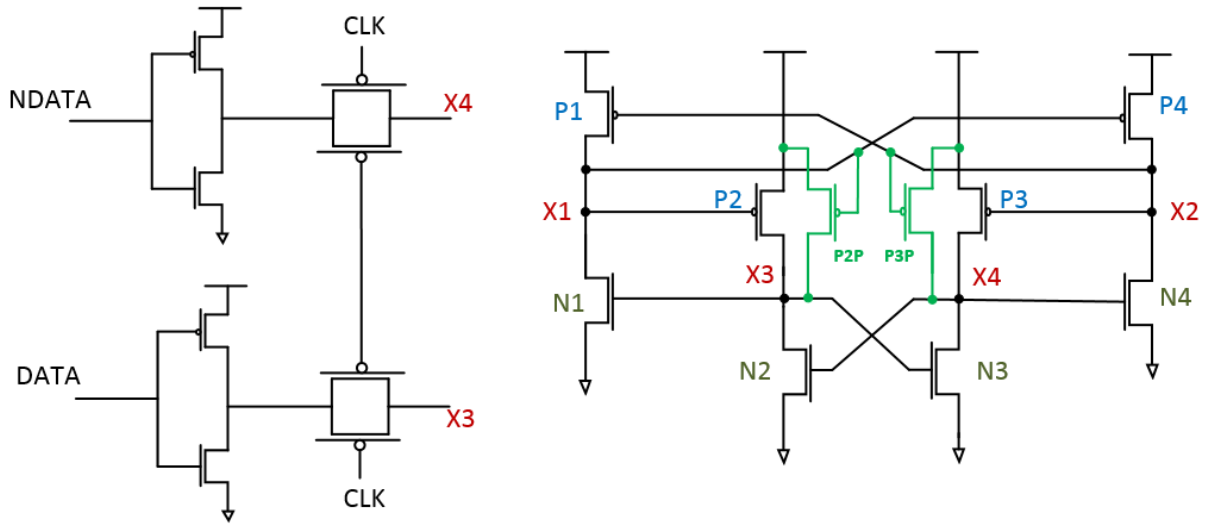

Figure 4.2 Proposed Quatro-based latch

Figure 4.1 shows the basic diagram of the regular Quatro structure. Eight transistors are used to store two pairs of complementary values. Differential data can be written into the cell. The logic state of X1 is the same as that of X4 and the logic state of X2 is the same as that of X3. With symmetrical structure, the Quatro cell reduces soft errors by 98% compared to a regular unhardened 6T SRAM cell [13]. Figure 4.2 is the schematic of the proposed Quatro-based latch. Two more PMOS transistors in each latch are added. P2P and P3P are connected in parallel to P2 and P3, respectively.

A flip-flop consists of a master latch, a slave latch, and transmission gates, which are used to connect inputs/outputs and storage latches. As shown in Figure 4.3, DATA and its complementary counterpart (NDATA) are written into the FF through inverters and transmission gates (each transmission gate has two PMOS transistors controlled by a CLK signal). The transmission gates between the master latch and the slave latch are similar to those in Figure 4.3, using NMOS transistors controlled by the CLK instead of PMOS transistors. When the CLK is low, the DATA and NDATA are written into the master latch and the data of the previous clock cycle are stored in

the slave latch as the outputs. At the rising edge of the CLK, the data in the master latch are transmitted to outputs through the slave latch. The transmission gates between the master latch and the input data are closed to cut off the connection. The layout of the transmission gates is shown in Figure 4.4. X3 and X4 are placed close to each other to reduce the overall SEE of the transmission gates. Transmission gates P1, P2, P3, and P4 are all located in the N-well to increase charge sharing effects. Because X3 and X4 have complementary values and the charge sharing between them can help to reduce the collected charge, X3 and X4 are placed close to each other.

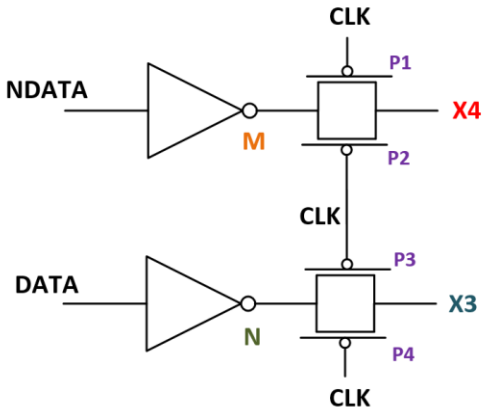

Figure 4.3 Schematic diagram of transmission gates

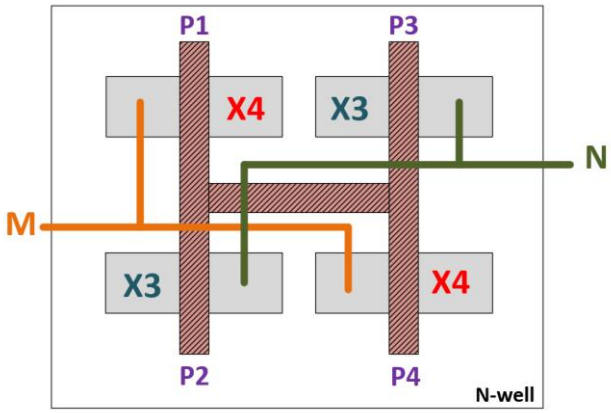

Figure 4.4 Layout sketch of two transmission gates

4.1.2 SEU Resistance Analysis

For the regular Quatro latch cell, Table 4.1 shows the SEU immunity to positive and negative pulses of four storage nodes, X1, X2, X3, and X4. Because of the symmetrical structure, SEU resistances of X1 and X2 are identical, as are the resistances of X3 and X4. Therefore, 4 different cases will be analyzed, including a positive pulse in X1 (case 1), a negative pulse in X2 (case 2), a positive pulse in X3 (case 3), and a negative pulse in X4 (case 4).

Table 4.1 SEU immunity of four nodes to positive and negative pulses in the Quatro cell

Storage node	**Positive pulse**	**Negative pulse**
X1	Immunity	SEU possibility
X2	Immunity	SEU possibility
X3	SEU possibility	Immunity
X4	SEU possibility	Immunity

Case 1 (a positive pulse in X1 or X2) ----- immune to a SEU:

With X1=X4=0 and X2=X3=1, if a charged particle strikes the Drain of P1, which is reverse-biased, a positive pulse will occur in node X1. The logic state of X1 will change from 0 to 1, turning off P2 and P4. Thus, nodes X3 and X2 will be floating. Node X4 will not be affected because of the “OFF” transistors P2, P4, N2, and N4. After a short time, the voltage level of node X1 will recover to its original level, since the generated carriers will be removed. The state of this Quatro cell will remain. Both the Quatro cell and the proposed design are immune to a SEU in this case.

Case 2 (a negative pulse in X1 or X2) ----- a SEU possibility:

Assume X1 and X4 are logic 1, and X2 and X3 are logic 0. If an energetic particle hits the Drain of N1, a negative pulse will occur in node X1. This negative pulse can turn on P2 and P4, resulting in contentions in nodes X3 and X2. For the regular Quatro cell, the logic state of X3 (X2) depends on the drive capacity of P2 and N2 (P4 and N4). The upset of X3 may turn on N3 and change the state of X4. Thus, the regular Quatro cell has the possibility of a SEU in this condition.

In the regular Quatro latch and the proposed Quatro-based latch, all transistors, including PMOS transistors (P1, P2, P3, and P4) and NMOS transistors (N1, N2, N3, and N4), are 150nm wide and 60nm long in a 65nm CMOS Bulk technology. According to semiconductor physics, free carriers are the holes in a PMOS and the electrons in a NMOS. The mobility of holes is less than that of electrons. If a PMOS transistor has the same size as a NMOS transistor, the drive capability of the PMOS transistor will be weaker than that of the NMOS transistor. With the same transistor size, the NMOS transistor will overpower the PMOS transistor if there is a competition between them. As a result in this case, upset will not happen in the regular Quatro cell, because the competition between P2 (P4) and N2 (N4) cannot flip the state of X3 (X2).

Case 3 (a positive pulse in X3 or X4) ----- a SEU possibility:

A positive pulse occurs in X3, when X1=X4=1, X2=X3=0, and a particle hits the Drain of P2. As in case 2 in the regular Quatro design, this positive pulse can cause competitions in nodes X1 and X4. It is possible for the whole cell to flip its state. This possibility depends on the transistor size of the PMOS and NMOS.

For the regular Quatro design, in which all PMOS and NMOS have the same size, the positive pulse in X3 will turn on N3 and N1. Because a NMOS transistor has a stronger drive capability, N3 and N1 will win the competition and flip the states of X4 and X1.

To verify the analysis above, a SEU injection is simulated by Spectre using the method in [48][49]. A precharged capacitor is connected with node X3 by a voltage-controlled switch, as shown in Figure 4.5. The capacitance depends on equation (4.1). Supply voltage "V" is 1V. Set the capacitance at 5fF. Therefore, 5fC positive charge will be injected into node X3.

$$Q = V \times C \tag{4.1}$$

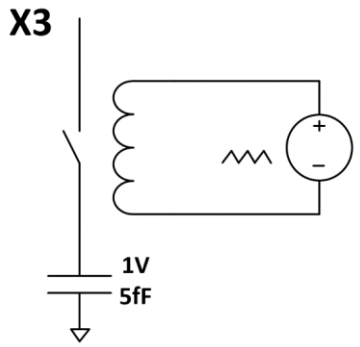

Figure 4.5 A capacitor controlled by a switch is used to simulate particle injection

Figure 4.6 shows the waveforms of X1, X2, X3, and X4 when a 5fC positive charge is injected into the regular Quatro cell. The waveforms show that the state of the regular Quatro cell flips when a positive pulse occurs in X3. This case is the worst scenario for the regular Quatro design to a SEU.

As to the proposed design, the existence of P2P and P3P can increase the capacitance of nodes X3 and X4, so the critical charge of these two nodes will be increased, resulting in X3 and X4 having higher critical charge threshold than the regular Quatro structure.

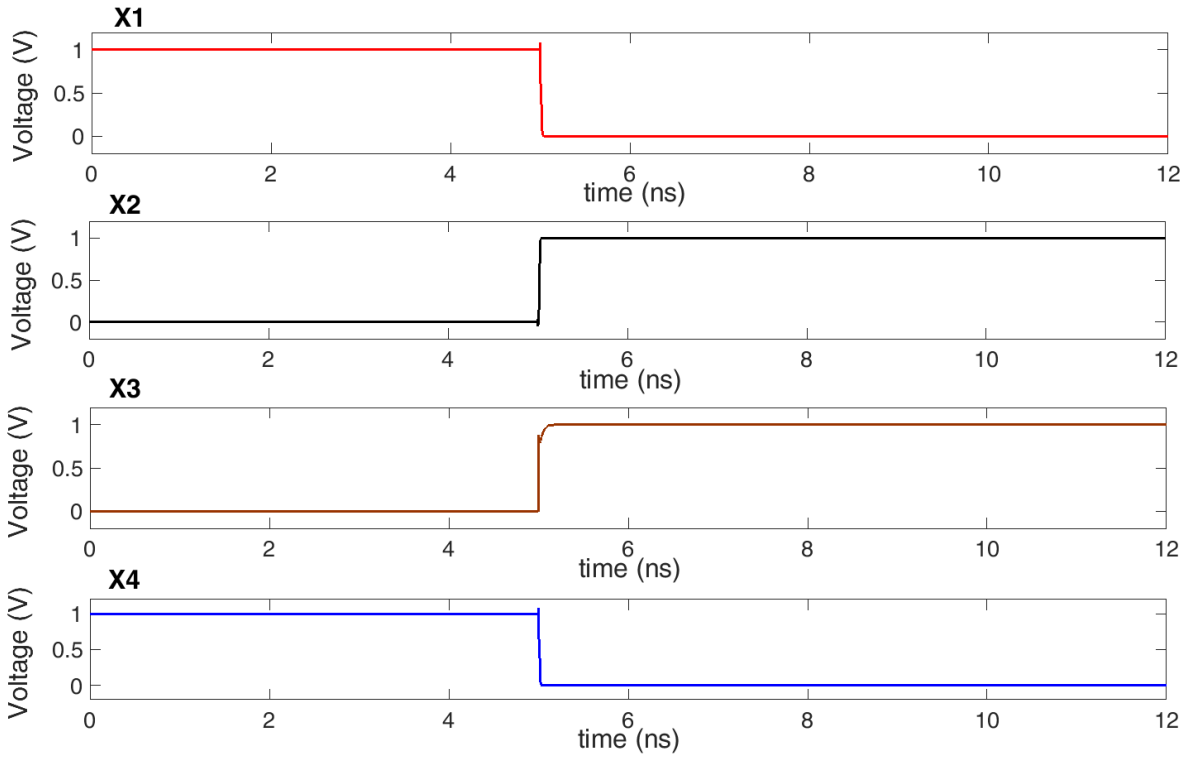

Figure 4.6 Waveforms of four nodes in the Quatro design: when a 5fC positive charge is injected into X3, the cell upsets in this case

On the other hand, the positive pulse in X3 tries to turn on N3, causing a competition between N3 and P3, and tries to induce a negative pulse in X4. P3P helps P3 increase the drive capability of the PMOS network, which can offer a larger recovery current than N3. This recovery current prevents an upset in node X4 and protects the value of the proposed cell. The same particle injection method is used in the proposed Quatro-based cell. Figure 4.7 shows the waveforms of X1, X2, X3, and X4 when a 5fC positive charge is injected into the proposed cell. The waveforms show that only SETs occur, which disappear after a short time. The results of the Spectre simulations prove that the proposed design has higher critical charge than the Quatro design, because it does not flip when 5fC is injected, whereas the Quatro does.

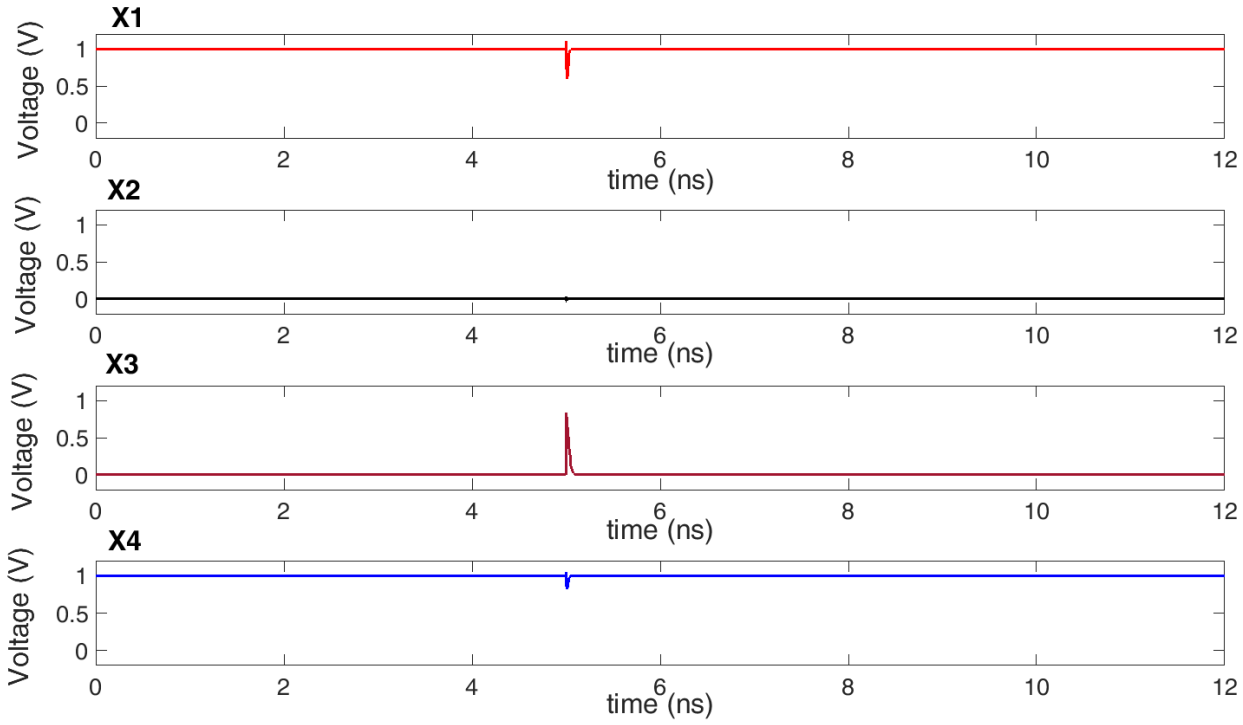

Figure 4.7 Waveforms of four nodes in the proposed design: when a 5fC positive charge is injected into X3, the cell does not upset in this case

Case 4 (a negative pulse in X3 or X4) ----- immune to a SEU:

As in case 1, a negative pulse in X3 can turn off transistors N1 and N3 with X1=X4=0 and X2=X3=1, leaving nodes X1 and X4 floating. When generated carriers are removed, the states of the Quatro and proposed cell will maintain their values and be without SEUs.

Different from the method in the proposed design which adds same-size transistors in parallel, doubling the transistor size was applied to achieve more radiation tolerance [13]. The Quatro cell was designed initially as a SRAM bit-cell, so the ratio of PMOS and NMOS transistors is restricted within a narrow range to guarantee its read and write operations and large enough Static Noise Margin (SNM). The width ratio of N2 and P2 should be around 1.5 to 1.7, and that of P1 and N1 should be 0.75 or less. Jahinuzzaman et al. suggested that the size of N2 and N3 could be enlarged

to improve the fault tolerance of the whole cell [13]. They simulated this method in a 90nm technology. The critical charge needed to flip the whole cell is improved as a result.

The method of doubling the transistor size is also simulated in this 65nm CMOS technology as a reference for the proposed design. The critical charge is determined through gradually increasing the deposited charge until SEUs occur in these cells. The same charge injection method is used as above. Two more designs are simulated. One doubles the width of N2 and N3 and keeps the other transistors the same as the regular Quatro design. The other doubles the width of P2 and P3 and keeps the other transistors the same as the regular Quatro. Table 4.2 shows the critical charge of these four Quatro-based designs. We can see that the proposed design has the highest critical charge, which increases by 2.23 times, 1.97 times, and 1.3 times compared to the regular Quatro, the Quatro with doubled size of N2 and N3, and the Quatro with doubled size of P2 and P3, respectively.

Table 4.2 Critical charge of Quatro designs with different transistor sizes

Design Options	Critical charge (fC)
Regular Quatro	4
Quatro with the double size of N2 and N3	4.5
Quatro with the double size of P2 and P3	6.8
Proposed Quatro-based design	8.9

4.2 Single Event Simulations

4.2.1 TFIT Soft Error Simulation Setup

SEUs in the regular Quatro and proposed latches are simulated by using the TFIT simulator from iROC Technologies Inc. TFIT is a SEE simulation tool at the transistor-level, which is used

to predict the SER performance of designs at the circuit and layout level [50][51][52]. Figure 4.8 is the TFIT block diagram and workflow. With faster speed than traditional Three-Dimension (3D) Technology Computer Aided Design (TCAD) simulators, TFIT can calculate the impact of particles on a transistor or a cell using Simulation Program with Integrated Circuit Emphasis (SPICE) simulators. Layouts of designs can also be read into the tool, so the charge sharing effect can be analyzed. Beyond the layouts of cells, the inputs of TFIT contain TCAD response models and simulation types. The outputs of TFIT are cross section, SEU/SET FIT, Multiple Cell Upset (MCU) FIT, SET waveforms, and sensitivity maps.

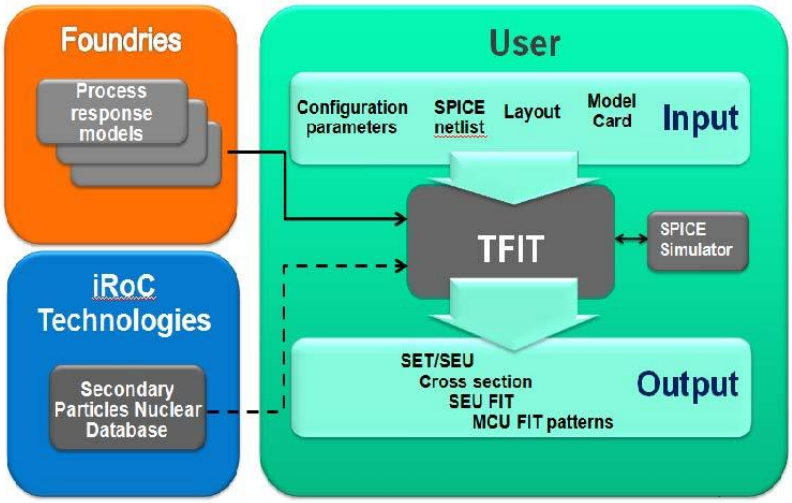

Figure 4.8 TFIT block diagram and workflow [50]

TFIT can perform critical charge computations, cross section computations, angular heavy-ion impact simulations, neutron SEU/SET FIT computations, alpha particles accelerated testing simulations, neutron MCU FIT, patterns computations, and thermal neutron SEU/SET computations.

For this thesis, sensitivity maps of the designs are generated by TFIT, which show the sensitive area with different LET values when the supply voltage is 1V. The cross section and LET

threshold of each transistor in different states can be displayed in sensitivity maps. The LET values we set are 1.3, 1.8, 2, 4.4, 5, 9, 13.9, 16, 25, and 30 MeV-cm^2/mg.

4.2.2 Simulation Results and Analysis

The SEU performances of the Quatro and proposed FFs are analyzed by using TFIT. Sensitivity map simulation results are generated. Figure 4.9 and Figure 4.10 are the sensitivity maps of the Quatro and proposed FFs with LET= 2 MeV·cm^2/mg when CLK is 0 and input is All-0. In this case, the proposed FF has no sensitive area and is immune to SEUs, which proves that it has a higher LET threshold than the Quatro FF.

Figure 4.11 and Figure 4.12 are the sensitivity maps of the Quatro and proposed FFs with LET from 1.3 to 30 MeV·cm^2/mg (1.3, 1.8, 2, 4.4, 5, 9, 13.9, 16, 25, and 30) when CLK is 0 and input is All-0. Figure 4.13 and Figure 4.14 are the sensitivity maps when CLK is 1 and input is All-0. Figure 4.15 and Figure 4.16 are the sensitivity maps when CLK is 0 and input is All-1. Figure 4.17 and Figure 4.18 are the sensitivity maps when CLK is 1 and input is All-1. As shown in these figures, the proposed FF has a larger sensitive area than the regular one with high LET values. The reason is that the Drains of P2P and P3P are sensitive in these conditions and they enlarge the possibility of SEUs.

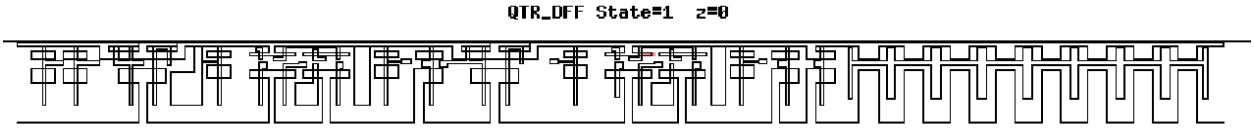

Figure 4.9 Sensitivity map of Quatro (CLK=0 All-0) when LET is 2 MeV·cm^2/mg

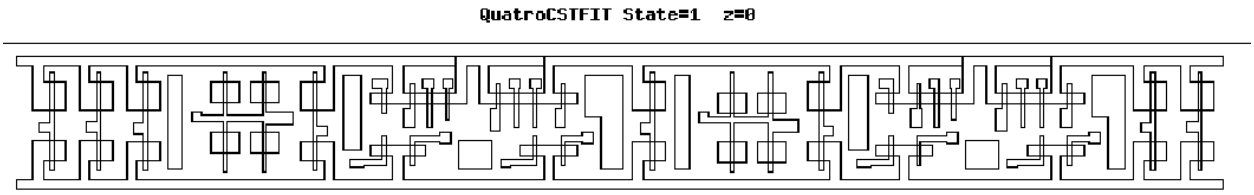

Figure 4.10 Sensitivity map of Proposed FF (CLK=0 All-0) when LET is 2 MeV·cm^2/mg

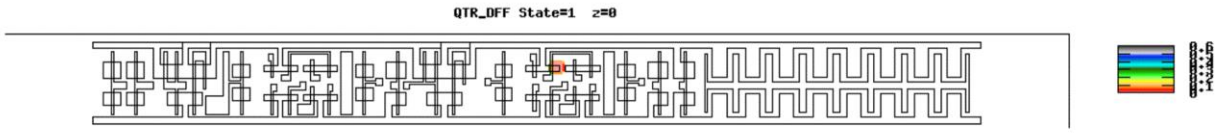

Figure 4.11 Sensitivity map of Quatro (CLK=0 All-0) LET from 1.3 to 30 MeV·cm^2/mg

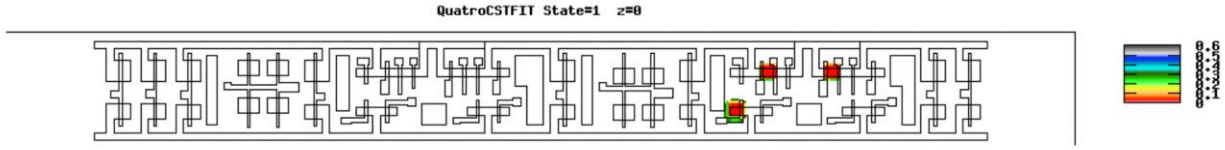

Figure 4.12 Sensitivity map of Proposed FF (CLK=0 All-0) LET from 1.3 to 30 MeV·cm^2/mg

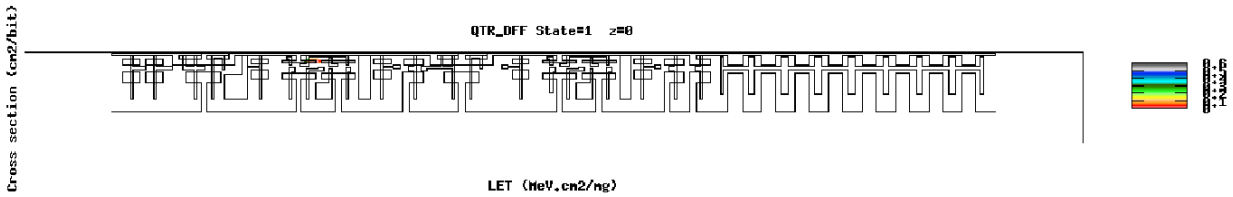

Figure 4.13 Sensitivity map of Quatro (CLK=1 All-0) LET from 1.3 to 30 MeV·cm^2/mg

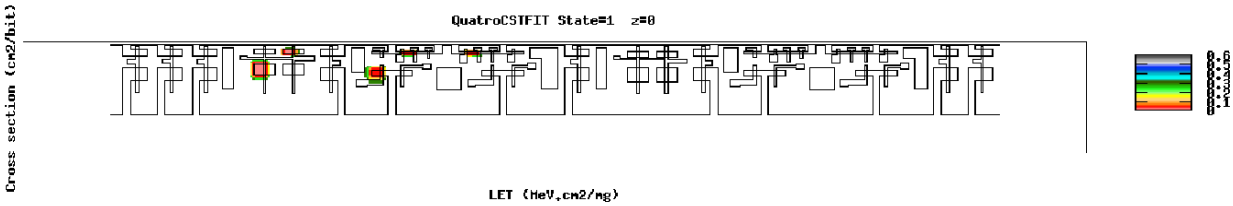

Figure 4.14 Sensitivity map of Proposed FF (CLK=1 All-0) LET from 1.3 to 30 MeV·cm^2/mg

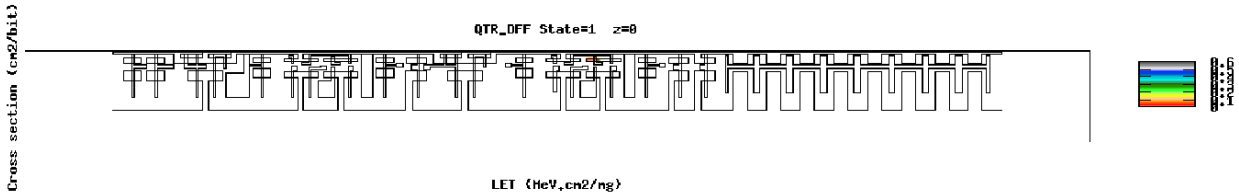

Figure 4.15 Sensitivity map of Quatro (CLK=0 All-1) LET from 1.3 to 30 MeV·cm^2/mg

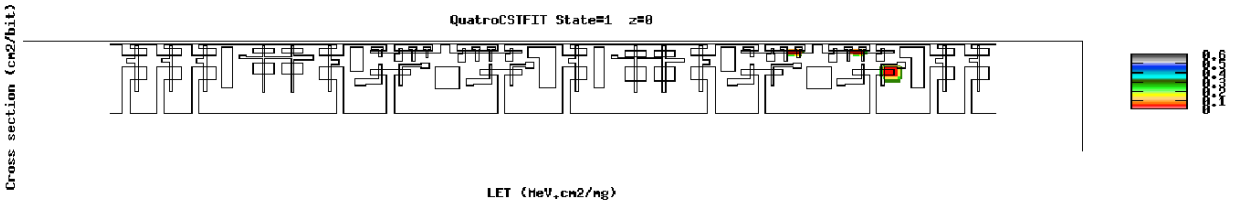

Figure 4.16 Sensitivity map of Proposed FF (CLK=0 All-1) LET from 1.3 to 30 MeV·cm^2/mg

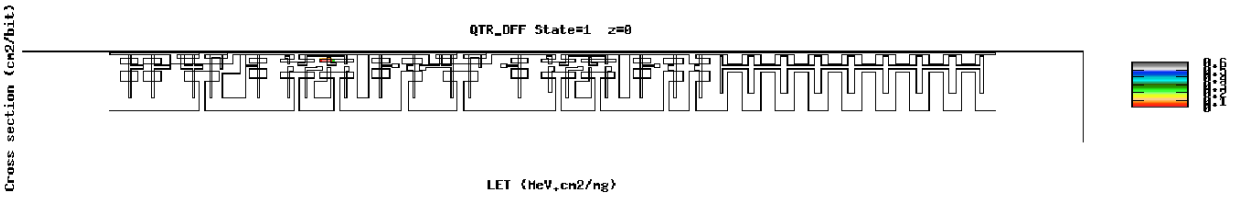

Figure 4.17 Sensitivity map of Quatro (CLK=1 All-1) LET from 1.3 to 30 MeV·cm^2/mg

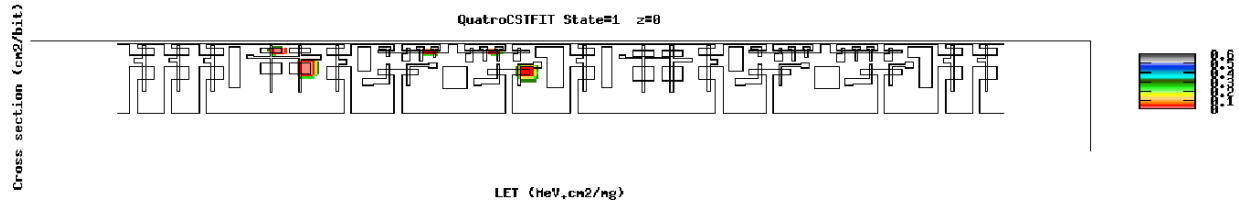

Figure 4.18 Sensitivity map of Proposed FF (CLK=1 All-1) LET from 1.3 to 30 MeV·cm^2/mg

Based on the Spectre and TFIT simulations on critical charge and sensitivity maps, we can predict that the proposed FF has a higher LET threshold than the Quatro FF, which means it has better performance against radiation from terrestrial environments. For higher LET values, the Quatro structure has better performance, because it has a smaller sensitive area.

4.3 Performance Comparison

Besides the SEU performance, overhead evaluations on area, delay, and power are described in this section. These evaluations are also based on the 65nm Bulk CMOS technology.

As to area consumption, with the same cell height 1.8μm, the proposed FF has a 17.6μm width, while the Quatro FF has a 14μm width.

C-to-Q delay is the delay from the rising edge of a clock signal to the output of a FF cell. C-to-Q delay is calculated by Spectre in a typical process corner, 27°C and supply voltage 1V. As shown in Table 4.3, the proposed FF cell increases the delay by around 1.135 times.

Table 4.3 C-to-Q delay of Quatro and Proposed FFs

C-to-Q delay (ps)	Quatro FF	Proposed FF	Ratio (Proposed/ Quatro)
Low → High	175.939	199.622	1.135
High → Low	190.0976	216.027	1.136

Power dissipation is simulated by Spectre in a typical process corner, 27°C and supply voltage 1V with different data activities. The data activity is the period ratio of the clock signal and the data signal. For example, 1/3 data activity means data changes its value every three clock cycles. In other word, if the period of the CLK is 8ns, the period of the data will be 48ns.

Table 4.4 is the power consumption of these two FF cells with different data activities. With the increase of data activities, power consumption rises, because the frequency of the data written into cells becomes faster. The proposed design consumes 1.61 times more power than the regular Quatro design.

Table 4.4 Power dissipation of Quatro and Proposed FFs with different data activities

Data activity	Quatro FF (uW)	Proposed FF (uW)	Ratio (Proposed/ Quatro)
1/3	2.919	4.727	1.619
1/2	3.575	5.781	1.617
1/1	5.543	8.941	1.613

In summary, the proposed design presents acceptable penalties of about 20% area, 15% delay, and 60% power dissipation with two more transistors added in each latch. For radiation tolerance, the Spectre simulations show that the proposed design has about 2 times the critical charge compared to the regular Quatro structure. The TFIT simulation results indicate that the proposed design is immune to low LET values and has a higher LET threshold than the traditional Quatro. The new design is a better candidate for terrestrial radiation environments. However, its performance with high LET values is not as good as the regular one, because it has a larger sensitive area.

CHAPTER 5: RADIATION HARDENING DESIGNS IN COMBINATION CIRCUITS

In this chapter, two proposed logic hardening designs are presented. One uses a layout-level hardening method based on the Cascode Voltage Switch Logic (CVSL). The other design is a differential dynamic logic gate. Section 5.1 presents the static logic radiation-tolerant design and its simulation results compared to the regular one. Section 5.2 introduces a SEU-immune design based on dynamic logic, and SEU simulations are analyzed in this section. Section 5.3 describes the performance comparisons of area, delay, and power.

5.1 Static Logic Hardening

5.1.1 Static CMOS Logic and CVSL

Besides sequential circuits, such as registers, latches, and flip-flops, combinational circuits are the other necessary components in integrated circuits. As introduced in chapter 2, the outputs of combinational circuits only depend on their current inputs. Combinational logic circuits can be divided into static logic circuits and dynamic logic circuits. Static logic circuits use stable input signals to turn transistors ON or OFF, so they have stable outputs. Dynamic logic circuits maintain their values using the storage function of parasitic capacitors embedded in the transistors. This section presents static logic hardening designs. Dynamic logic hardening methods will be explained in the next section.

Static CMOS logic is the most commonly used logic style in combinational circuit families. As shown in Figure 5.1 (a), a logic gate is built with a NMOS pull-down network and a PMOS pull-up network [2]. Figure 5.1 (b) is another example, a static CMOS logic 2-input NAND gate. Only when the inputs A and B are both logic 1, will the output Y be logic 0. In other cases, the

output Y is logic 1. The advantages of static CMOS logics are high noise margin, low power, and robustness [2]. The main drawback is that they need both NMOS and PMOS networks, which result in a relatively larger circuit size and slower speed compared to some of the other logic families.

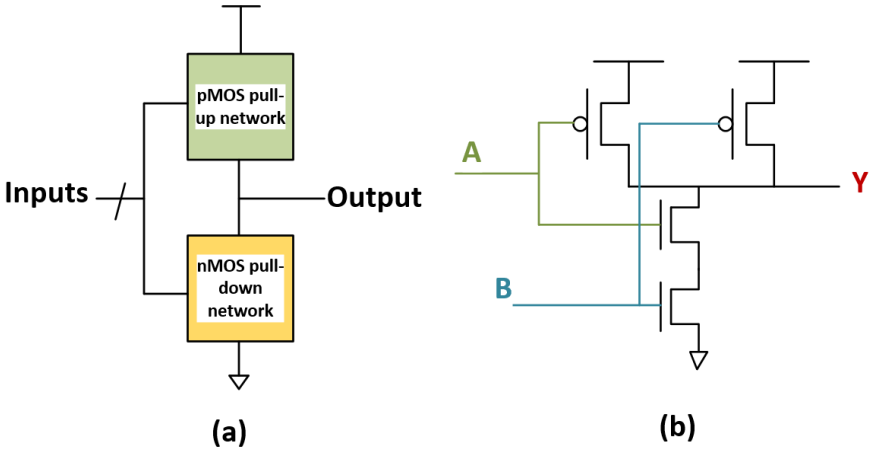

Figure 5.1 (a) general static CMOS logics; (b) 2-input static NAND gate

An alternative of static CMOS logics is Cascode Voltage Switch Logic (CVSL). Figure 5.2 shows the basic structure of a CVSL gate. Compared with a static CMOS gate, the inputs of the CVSL are only connected to the NMOS network. Differential outputs are generated from differential inputs. In the PMOS network, only two cross-coupled PMOS transistors are used, so the delay of this CVSL is only determined by the pull-down NMOS networks.

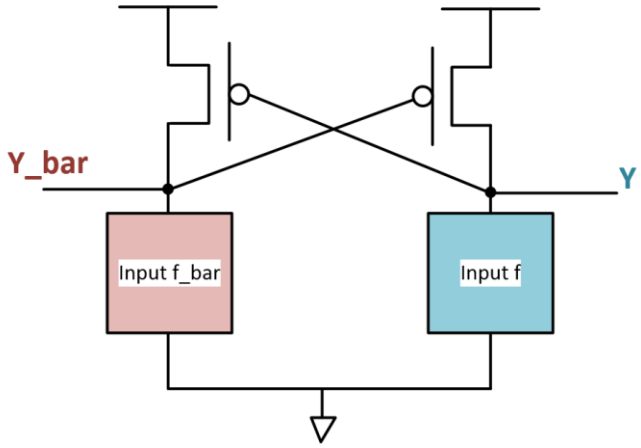

Figure 5.2 General CVSL gate

Compared with static CMOS logic gates, the simplified PMOS network can reduce the input capacitance of a CVSL gate. On the other hand, the feedback structure in PMOS networks can increase the delay of the CVSL and make it slower than static logic gates. In addition, the contention of the current in the back-to-back PMOS consumes more power.

The main advantage of the CVSL is its SET tolerance to radiation effects. Traditional hardening methods for static CMOS logic circuits are TMR or temporal sampling technologies. But these methods have large power and area overhead. Casey et al. evaluated the SET-tolerance of the CVSL gates and found that SETs could be terminated after a few stages [53]. Two factors can explain this phenomenon. One is that the differential inputs and outputs can help to improve radiation tolerance because data are stored in more than one node. The other is charge sharing happens between the two output nodes and cancels out each other in these two nodes. Simulations in the Taiwan Semiconductor Manufacturing Company (TSMC) 180nm and the International Business Machines (IBM) 130nm technologies show SETs cannot propagate beyond two-level CVSLs [55]. The CVSL logic was used in latch designs and the CVSL-DICE structure was proven to be immune to multiple node upsets [54].

5.1.2 Proposed Layout-based Hardening Design

Inspired by the CVSL immunity study above, a new layout-hardening CVSL design is proposed. Figure 5.3 shows two-level CVSL AND-NAND gates. Using the AND-NAND scheme in this design is more representative than the CVSL inverter structure. Different from the traditional layout design, Figure 5.4 is the layout diagram of two-level CVSL gates. The first stage of the CVSL gates is placed on the top and the second stage is located on the bottom. Similar to the LEAP layout mitigation technology, two nodes which have opposite pulses are placed close to each other. For example, among the four nodes A1, B1, C1, and D1, if there is a negative pulse in B1 caused

by a single particle strike, it will turn on P2 and result in a positive pulse in C1. Charge sharing between B1 and C1 will increase this positive pulse and a larger SET will be shown in node out_b'. The same mechanism is applied to A1 and D1. To reduce charge sharing between the sensitive pairs, B1 and C1 are placed far from each other and in different wells in the new layout design, as are A1 and D1. C1 and D1 are placed close to each other to cancel the total charge sharing effect and to reduce the SET pulses. The same applied to A1 and B1. These four nodes are placed horizontally to limit the sensitive direction to a narrow range.

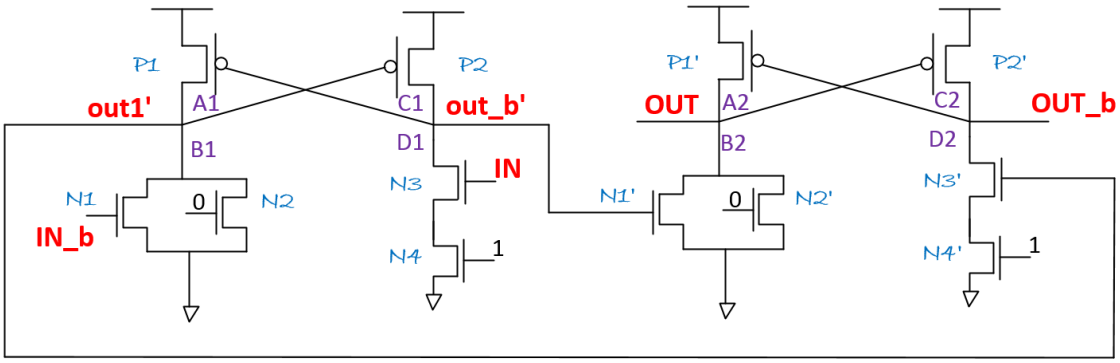

Figure 5.3 Schematic of two-level CVSL AND-NAND gates

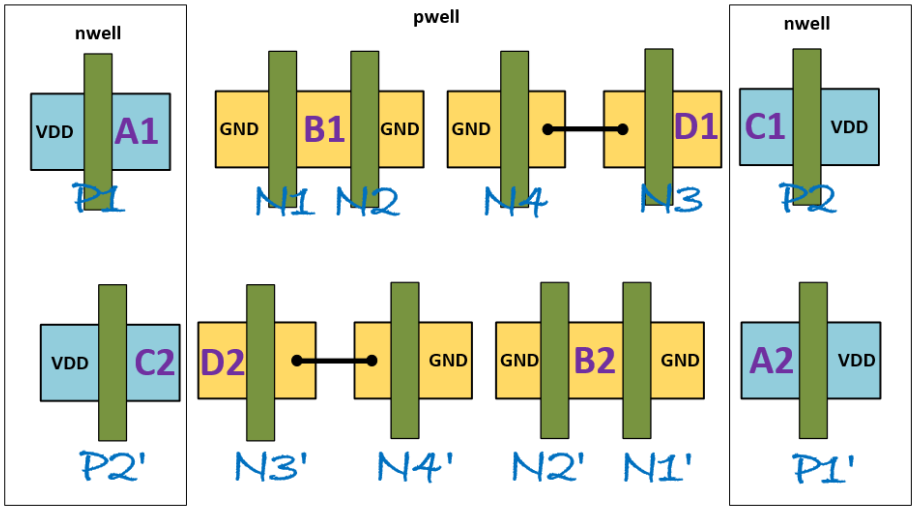

Figure 5.4 Layout diagram of two-level CVSL gates

As the reference of the proposed design, a static CMOS AND gate, is shown in Figure 5.5, with the same transistor number as the proposed CVSL (6 transistors). One input is fixed to logic 1, so the output will be the same as the other input. Because of the differential inputs and charge sharing layout structure, the proposed two-level CVSL design is predicted to be more tolerant against SETs than two-level static AND gates.

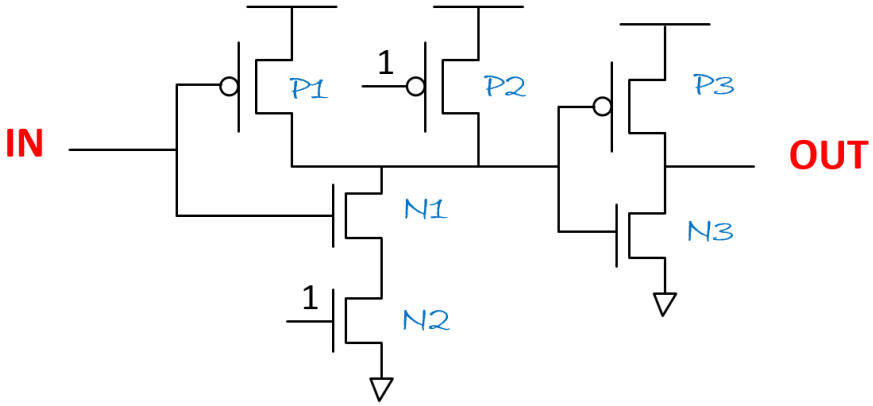

Figure 5.5 Schematic of reference static CMOS AND gate

Table 5.1 shows the size of transistors in the proposed design and the reference gate, which are implemented in the TSMC 65nm CMOS technology. The static AND gate uses the conventional layout structure.

Table 5.1 Transistor size of CVSL and reference static designs

Ref_AND gate	P1	P2	P3	N1	N2	N3
Transistor size (nm)	120/60	120/60	150/60	400/60	400/60	120/60
CVSL gate	P1	P2	N1	N2	N3	N4
Transistor size (nm)	120/60	120/60	400/60	400/60	400/60	400/60

5.1.3 SET Simulation Results and Analysis

Besides the analysis of SEU performance of flip-flops in chapter 4, the TFIT simulator can simulate SETs in combinational cells and export critical charge, cross section, and sensitivity maps. In the TFIT SET simulations in this chapter, voltage pulses longer than 5ps are defined as SETs, because the minimum delay of inverters in the 65nm CMOS technology is longer than 5ps. SETs shorter than 5ps are not considered since they will be filtered out when propagating through the logic gates. To analyze the performance of the layout-based CVSL design, a regular CVSL design using traditional layout is included. This regular CVSL design has the same schematic as the proposed CVSL, which means both have the same transistor number and size.

Table 5.2 lists the critical charge of the static AND gate, the regular-layout CVSL, and the proposed CVSL design at 0.9V, 1.0V, and 1.1V, obtained by the TFIT simulator. Compared with the reference static AND gate, the proposed CVSL design is 3 times better in critical charge when input is 0. When input=1, the improvement is not so obvious, only about 1.7 times. The reason is that the CVSLs use the PMOS feedback structure to increase their radiation resistance. Compared to the regular CVSL structure, the layout-based hardening design shows little improvement when input is 0, and around 20% improvement when input is 1. The reason is that the critical charge depends on the voltage as well as the capacitance of a node. These two structures have the same schematic, so the capacitance of the nodes is relatively equal. The charge cancellation via layout structure can raise the critical charge to some degree, but the enhancement to the regular layout structure is not so obvious as that to the static logic.

Critical charge of input 0 and input 1 is different. This is because in different states, the sensitive transistors are different. Figure 5.6 is the sensitivity map of the reference static AND gate when input is 0. In this state, N1 and P3 are the reverse-biased Drains in Figure 5.5. However, when input is 1, P1, P2, and N3 are the sensitive transistors. The size of the PMOS and NMOS is

different, so the critical charge in different states is not same. Figure 5.7 is the sensitivity map of the regular CVSL when input is 0. Figure 5.8 is the sensitivity map of the proposed design when input is 0. It is obvious that the sensitive area of a CVSL is much smaller than that of a static gate. The sensitive area of the proposed CVSL is smaller than that of the regular CVSL.

Table 5.2 Critical charge of static AND gate, regular CVSL, and proposed CVSL design

Logics	Inputs	VDD = 0.9V	VDD = 1.0V	VDD = 1.1V
Static ref	0	1.63 (fC)	1.97 (fC)	2.32 (fC)
	1	1.35 (fC)	1.60 (fC)	1.85 (fC)
Regular CVSL	0	4.89 (fC)	5.29 (fC)	5.67 (fC)
	1	1.92 (fC)	2.24 (fC)	2.53 (fC)
Proposed CVSL	0	5.04 (fC)	5.36 (fC)	5.68 (fC)
	1	2.29 (fC)	2.63 (fC)	2.98 (fC)

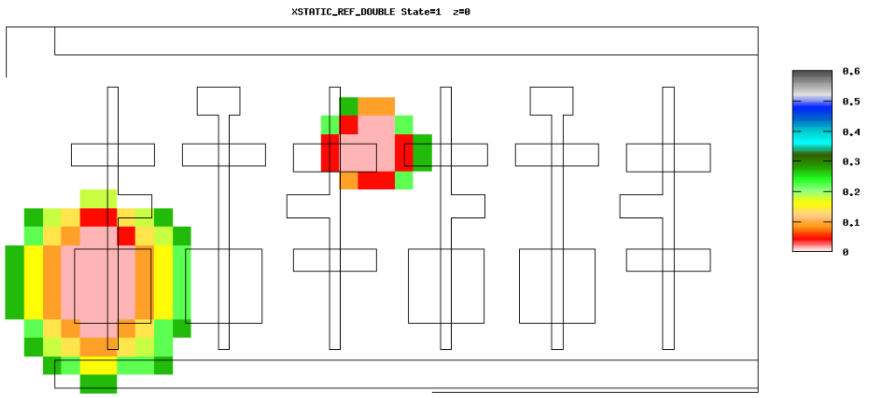

Figure 5.6 Sensitivity map of reference static AND gate when input is 0

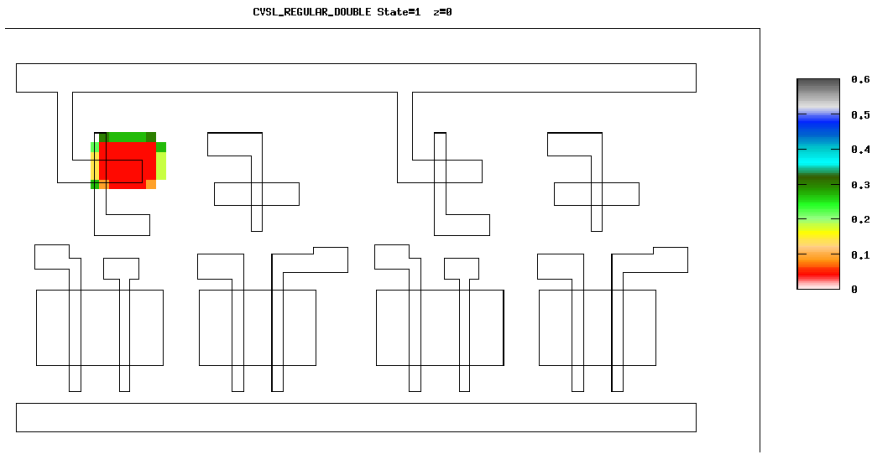

Figure 5.7 Sensitivity map of regular CVSL when input is 0

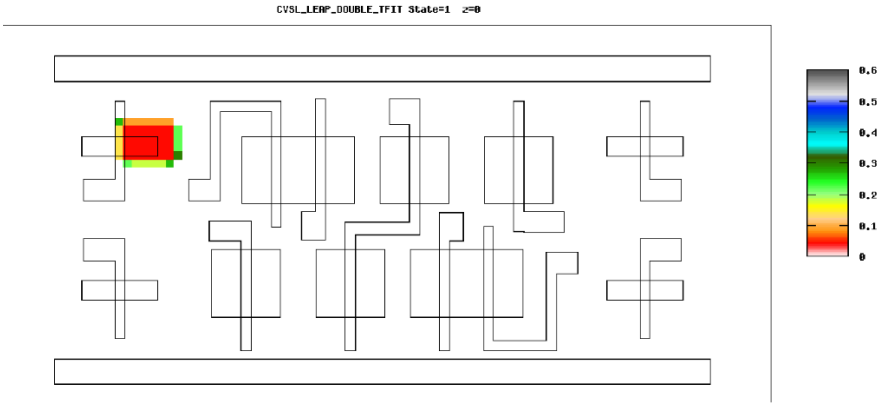

Figure 5.8 Sensitivity map of proposed CVSL when input is 0

Table 5.3 Cross section (cm^2) of three logics with different LET values when input is 0

LET ($MeV \cdot cm^2/mg$)	1.3	4.4	9
Ref_static	1.97×10^{-10}	3.02×10^{-9}	3.77×10^{-9}
Regular_CVSL	0	7×10^{-10}	8.25×10^{-10}
Proposed_CVSL	0	6×10^{-10}	7.5×10^{-10}

Table 5.3 is the cross section of the reference static logic, regular CVSL, and proposed CVSL design with three LET values. The CVSL structure is immune to SETs when LET is 1.3 $MeV \cdot cm^2/mg$. For higher LET values, the proposed CVSL improves ~5 times compared to the reference static gate. When LET is 4.4, the proposed CVSL design has reduced SET soft errors by

around 15% compared to the regular CVSL. This improvement comes from the reduced total collected charge through the layout hardening structure. In fact, charge cancellation via layout can reduce the total charge, but when LET becomes higher, this reduction plays a minor role. The reason is that when the energy of a particle is high, the amount of generated charge is large enough to cause upsets at stuck and passive nodes, where charge sharing is no longer effective.

TFIT simulations with different pulse widths are conducted to analyze the characteristics of SETs generated from the reference static logic, regular CVSL, and proposed CVSL, when LET is 4.4 MeV·cm^2/mg and input is 0. Figure 5.9 shows the cross section of these three designs with SET pulse widths within 5-25ps, 25-45ps, and larger than 45ps. Almost all SETs in the reference static logic gate are larger than 45ps. As to CVSL designs, all the SET pulses are within the region of 5ps-25ps. In the 5-25ps region, the cross section of the regular CVSL is 1.16 times larger than that of the proposed CVSL.

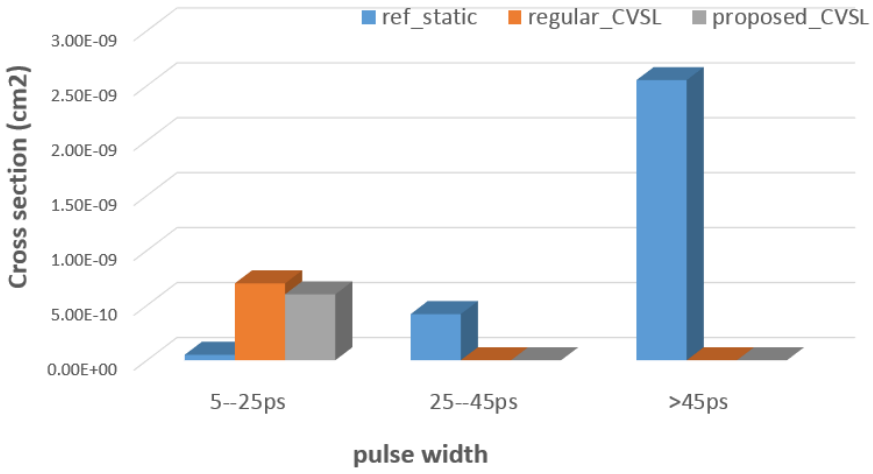

Figure 5.9 Cross section changes with pulse widths of three static designs when input is 0 at 4.4 MeV·cm^2/mg

5.2 Dynamic Logic Hardening

5.2.1 Single Event Effect Analysis on Dynamic Logic

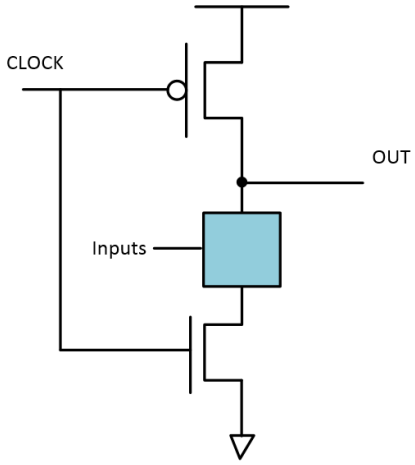

Figure 5.10 A general dynamic logic gate

Figure 5.10 shows the general structure of a dynamic logic gate. The clock signal and inputs control the output. Compared to the static logic, dynamic logic circuits have smaller area and faster speed, as only one PMOS transistor is used in the pull-up network. Dynamic logic circuits are widely used in Central Processing Units (CPUs) and digital signal processors for high-speed modules [55].

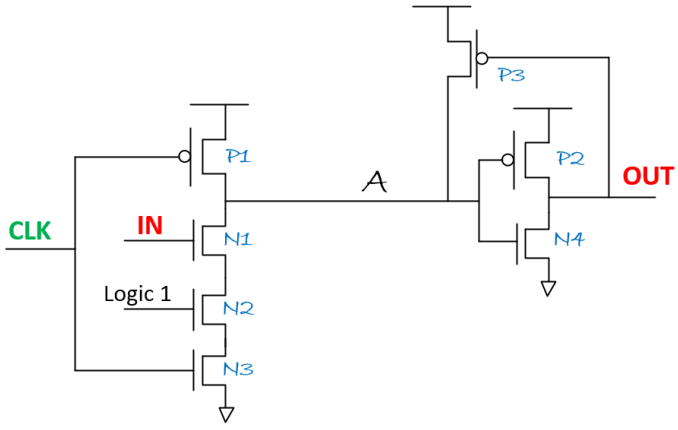

Figure 5.11 A regular dynamic AND gate

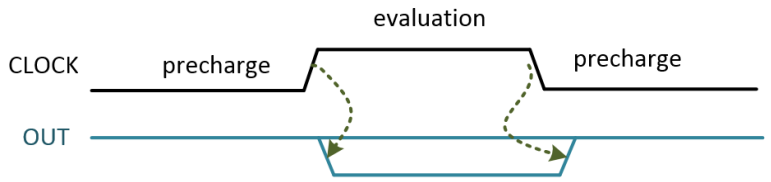

Figure 5.12 Precharge and evaluation stages of a dynamic logic

Take a regular dynamic AND gate as an example (Figure 5.11) to analyze its SEE performance. As shown in Figure 5.12, there are two phases in a dynamic logic operation, namely precharge and evaluation, depending on the clock signal. When the clock is low, P1 is ON and N3 is OFF. Node A is logic 1 and the output is 0. P3 is a keeper to maintain the state of node A. In this case, node A is driven by P1 and P3, so SETs may occur. However, when the clock is high, it is in the evaluation phase. The output is only controlled by input signals, because P1 is OFF and N3 is ON. With N2 ON, if the input of N1 is logic 1, node A driven by N1, N2, and N3 will be connected to GND and the output is 1. SETs may occur at nodes A and pulses can be shown at output. If the input is logic 0, N1 will be OFF. Node A will be floating and maintain logic 1. This state is immune to upsets. If a SET occur at node A, changing it from logic 1 to 0, the output OUT will change from 0 to 1 and turn off the keeper P3. Node A will stay at logic 0 during the evaluation phase until the next precharge phase. Since node A cannot change its value by itself without the update of the clock signal, this upset is similar with the SEUs in storage cells, in which SETs are trapped in the cells. The upsets in dynamic logic are regarded as SEUs. In summary, a SEU will occur when the input is 0 in the evaluation phase.

5.2.2 Proposed Design

Figure 5.13 is the proposed differential dynamic logic design. To make this structure more representative, a differential dynamic AND gate is chosen instead of an inverter. The proposed

structure combines two regular dynamic AND gates by adding two more PMOS transistors, PP1 and PP2. Inputs of the proposed design are complementary signals, IN and IN_b.

When the CLK is 0, these two dynamic logic gates are in the precharge stage, and nodes A and B are both logic 1. PP1 and PP2 are OFF, and the outputs, OUT and OUT_b, are both logic 0. In this case, only SETs occur, because PMOS transistors and keepers drive nodes A and B. It is immune to SEUs, which is similar to a regular dynamic logic.

When the CLK is 1, because of the symmetrical structure, the state of IN=1 and IN_b=0 is the same as that of IN=0 and IN_b=1. Assume that IN is 0 and IN_b is 1. Node A is logic 1 and B is logic 0. PP1 is ON and PP2 is OFF. Node B is driven by the NMOS transistors of the bottom dynamic logic gate, so this node is immune to SEUs. As to node A, because of the ON transistor PP1, A is connected to OUT_b, and P2 of the bottom dynamic logic gate drives this node. Besides P2, the keeper P3 of the top dynamic logic drives node A to logic 1. In this case, SEUs also will not occur because A is no longer floating.

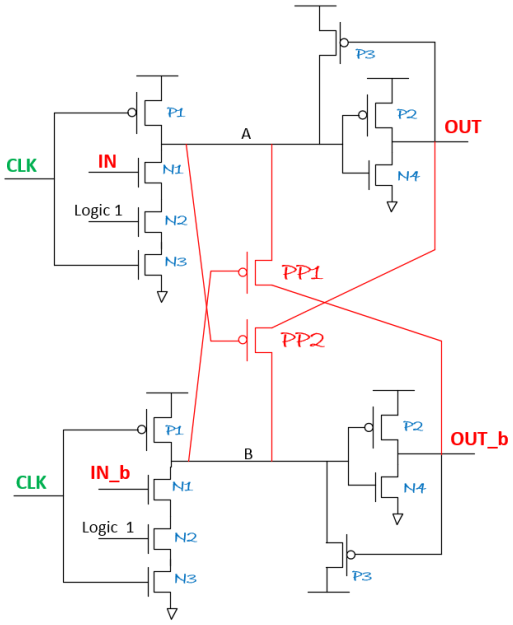

Figure 5.13 Proposed differential dynamic logic gate

The same method in chapter 4 is used to simulate charge injection on the proposed and regular designs by Spectre. A capacitor and a switch controlled by a voltage source are used to inject a positive or negative pulse. Table 5.4 is the transistor size of the reference and proposed designs. The length of all transistors is kept at 60nm.

Figure 5.14 shows the waveforms of the reference dynamic logic when input is 0 and 5fC is injected into node A. One can see that a SEU occurs after a 5fC charge is inserted. Only when the next precharge phase comes, can the state of node OUT be precharged again and return to logic low.

Table 5.4 Transistor size of reference and proposed dynamic logic gates

Transistor size (nm)	P1	P2	P3	N1	N2	N3	N4	PP1	PP2
Ref_dynamic_logic	120	150	120	400	400	400	120	\	\
Proposed_dynamic_logic	120	150	120	400	400	400	120	120	120

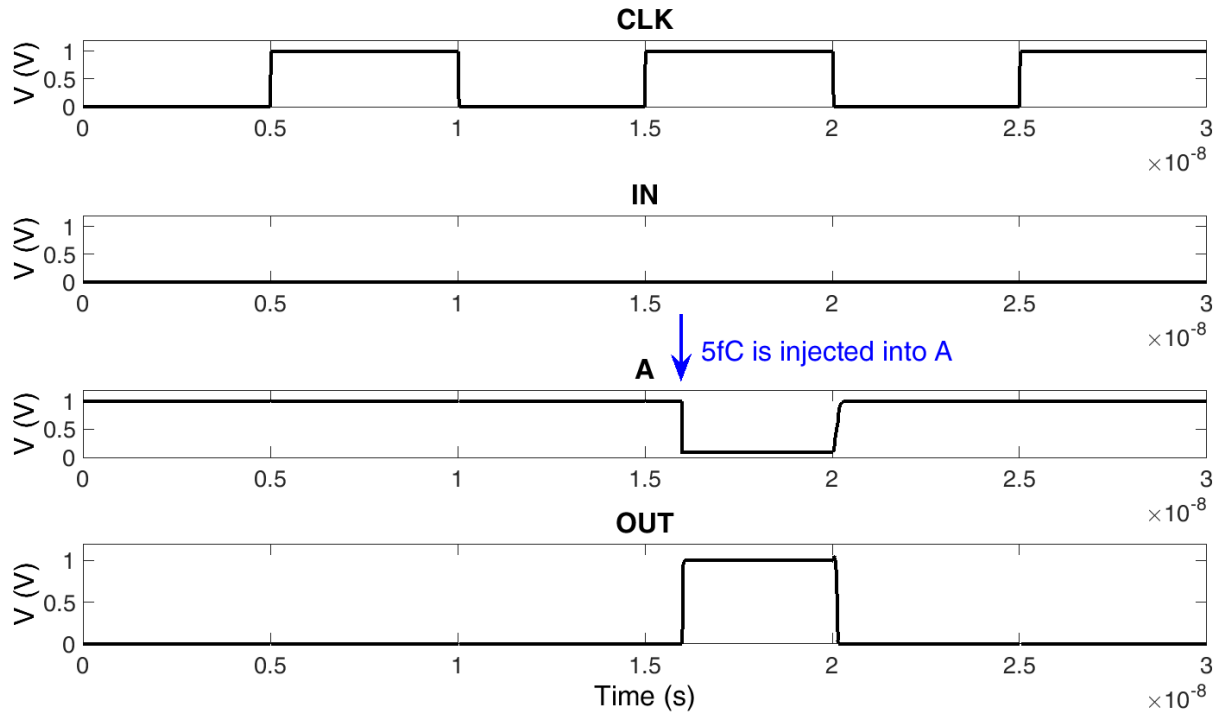

Figure 5.14 Waveforms of reference design when 5fC charge is injected into node A

Figure 5.15 and Figure 5.16 show the waveforms of the proposed design when 5fC and 50fC are injected into node A with inputs IN=0 and IN_b=1, respectively. After 5fC is injected, only a small pulse is shown at node A. The pulse shown in OUT after inserting 50fC is larger but the node can still recover by itself during the evaluation stage, indicating that a SET occurs instead of a SEU. According to the simulation results by Spectre, we can say that the proposed dynamic logic can help remove SEUs and increase the radiation tolerance.

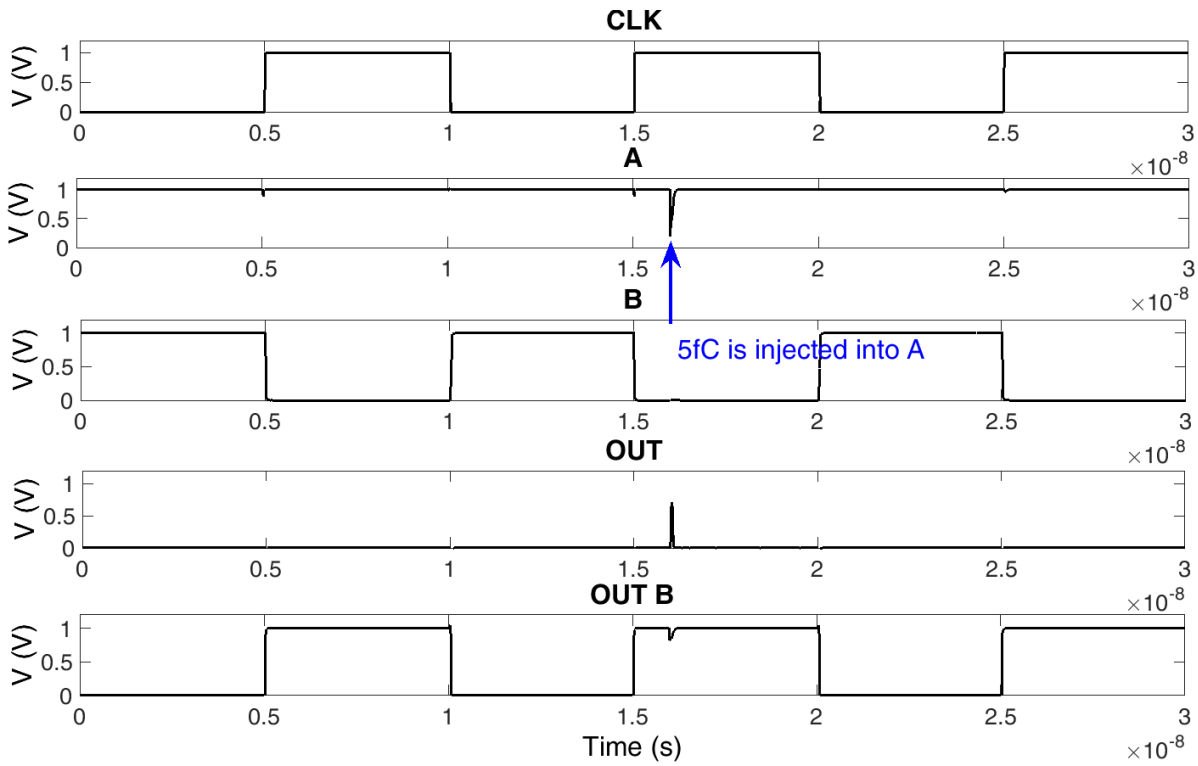

Figure 5.15 Waveforms of proposed design when 5fC charge is injected into node A

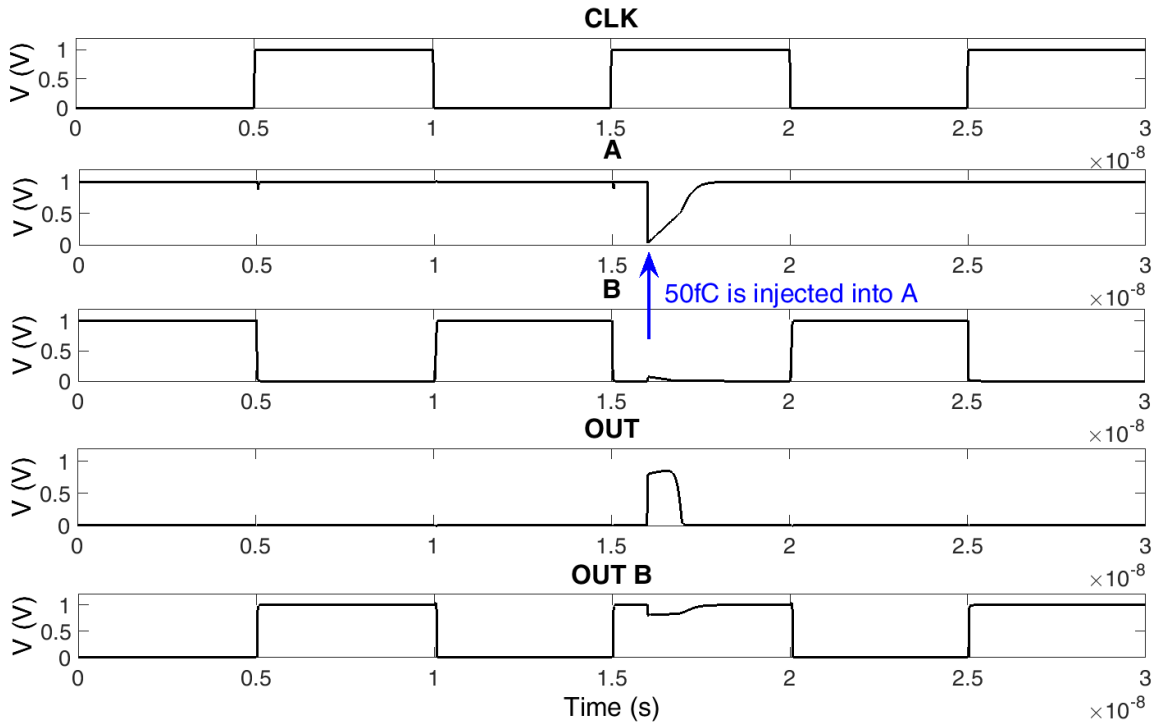

Figure 5.16 Waveforms of proposed design when 50fC charge is injected into node A

5.2.3 TFIT Simulation Results

To evaluate the radiation tolerance and SET characteristics of the proposed design, another hardened dynamic logic with differential keepers [55] is also included, and all three designs are simulated using the TFIT soft error simulator. Figure 5.17 is the differential dynamic logic design using differential keepers to remove the SEUs in the evaluation phase [55].

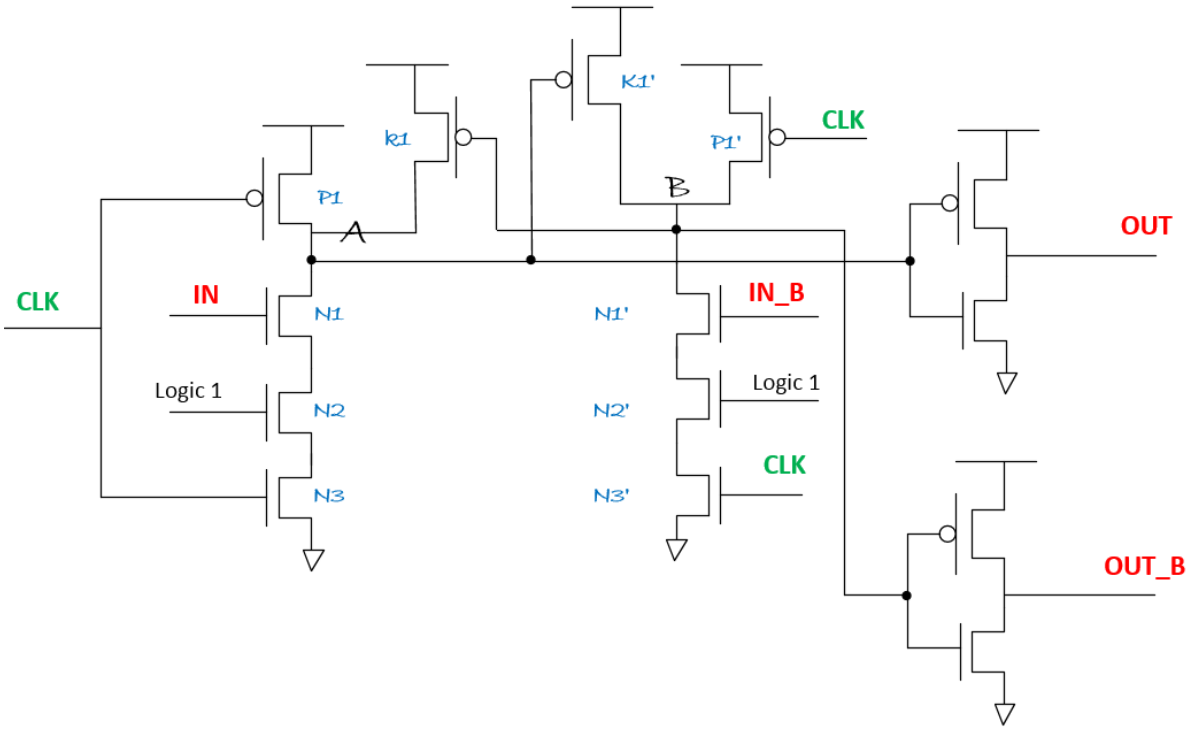

Figure 5.17 Schematic of the dynamic logic with differential keepers [55]

Table 5.5 shows the SEU cross section of the reference dynamic logic, the dynamic logic with differential keepers, and the proposed differential dynamic logic, when LET values range from 1.3 to 30 MeV·cm^2/mg. This SEU cross section is simulated with input=0 and clock=1, because in this condition, the reference dynamic is sensitive to SEUs and no transistors drive node A in Figure 5.11. From the data in Table 5.5, we can see that the proposed differential dynamic AND/NAND gate is immune to SEUs and there is no cross section with LET from 1.3 to 30 MeV·cm^2/mg. The reason is there is no floating state for the inner nodes A and B in Figure 5.13. The differential keepers design has the same results. However, for the regular dynamic logic gate, it is possible for SEUs to occur in this state. With the increase of LET, the sensitive area of this gate becomes larger.

Table 5.5 SEU cross section of reference and proposed dynamic logic gates

	LET (MeV·cm^2/mg)								
Logic	**1.3**	**4.4**	**9**	**13.9**	**16**	**18.72**	**22**	**27**	**30**
Ref_dynamic (10^{-9}cm2)	1.50	2.25	2.90	4.05	4.65	5.25	6.25	7.40	7.95
Dynamic with differential keepers	0	0	0	0	0	0	0	0	0
Proposed_dynamic	0	0	0	0	0	0	0	0	0

Table 5.6 lists the critical charge of these three designs when supply voltage is 1.0V. Inputs 0 and 1 in the precharge phase (CLK=0) and inputs 0 and 1 in the evaluation phase (CLK=1) are used in the simulations.

In the precharge stage, the outputs are independent from inputs. The output of the reference design is 0 and the outputs OUT and OUT_b of the proposed design are 0, meaning that the sensitive transistors are not changed. As a result, the critical charge of the precharge phase remains the same when the inputs are 0 and 1. Compared to the regular design, the new differential design improves critical charge by about 26%. The reason is that two more transistors, PP1 and PP2 in Figure 5.13, increase the capacitance of nodes OUT and OUT_b, and thus, they increase the critical charge of the outputs.

In the evaluation stage, when input is 0, the improvement of the proposed design is around 25%. When input is 1, the improvement rises to about 52%. The reason is that the observed node of TFIT is node OUT. In Figure 5.18, the green and red marks indicate the sensitive locations in the proposed design with input 0 and input 1, respectively. Node OUT in (A) has a larger sensitive area compared to this node in (B), because PP2 is sensitive in (A). In addition, the size of P2 in (A) is smaller than that of N4 in (B). That is the reason that the regular dynamic logic has different critical charges when inputs are 0 and 1. The transistor size is the same as that in the proposed

design. Node OUT at input=1 has the same results with node OUT_b at input=0 because of the symmetrical structure.

Compared to the differential keepers design, the proposed differential design has a 30% higher critical charge at input=0, and around 50% higher at input=1 in the evaluation stage. The reason is that PP1 and PP2 of the proposed design increase the capacitance of the output nodes, whereas the outputs of the logic design with differential keepers are only the outputs of inverters with regular capacitance.

Table 5.6 Critical charge (fC) of three dynamic logic gates

Design	CLK0IN0	CLK0IN1	CLK1IN0	CLK1IN1
Regular dynamic logic	2.74	2.74	2.82	2.33
Dynamic with differential keepers	2.64	2.64	2.68	2.28
Proposed dynamic design	3.46	3.46	3.52	3.54

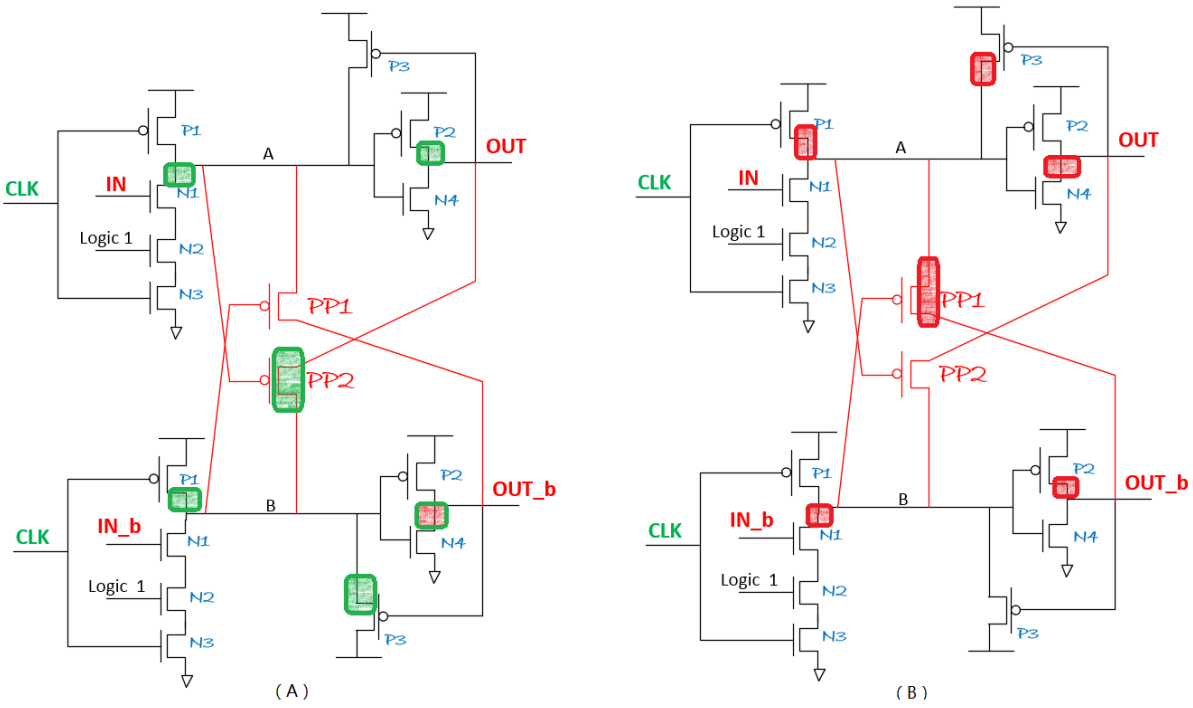

Figure 5.18 Sensitive Drains of proposed design in evaluation phase when input is 0 (A) and 1 (B)

SET characteristics are also analyzed by using the TFIT simulator and changing the setting of the SET pulse width. In the precharge stage, all of the dynamic cell outputs are precharged to high, and SETs during this stage can be ignored. The outputs during the evaluation stage are important because they will be sampled by the registers in the logic path. When LET is 1.3 MeV·cm^2/mg and input is 1, the cross section of SETs larger than 5ps is 5.75*10^{-10}cm^2 in the reference dynamic logic, 5.75*10^{-10}cm^2 in the dynamic logic with differential keepers, and 3.75*10^{-10}cm^2 in the proposed design. The proposed design reduces the sensitive area by around 35% compared to the other two designs. Figure 5.19 shows the cross section of these three dynamic logic gates with the pulse width of 5-25ps, 25-45ps, and larger than 45ps. One can see that the dynamic gate with differential keepers eliminates the SETs longer than 45ps compared to the reference dynamic logic, whose SETs are mostly longer than 45ps. The proposed design has the best performance because it shrinks the pulses below 25ps. Shorter SETs have less chance to be captured by registers, so the proposed design should have better performance in high speed circuits in terms of reducing SERs.

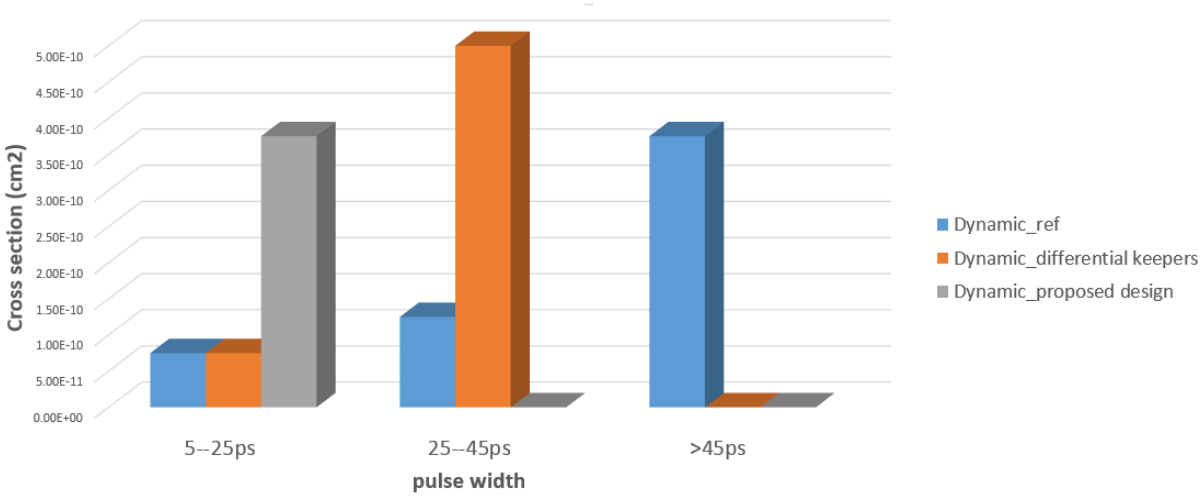

Figure 5.19 Cross section of pulse width in the three dynamic designs when LET is 1.3 MeV·cm^2/mg and input is 1 for evaluation phase

5.3 Delay, Power, and Area Comparison

Table 5.7 shows the delay of the static AND gate, the CVSL with regular layout structure, the proposed CVSL with hardening layout structure, the regular dynamic AND gate, the dynamic logic with differential keepers, and the proposed differential dynamic logic. This delay is post-layout delay simulated by Spectre in the 65nm CMOS Bulk technology with the conditions of 27°C, 1V, and a typical process corner.

The proposed CVSL design has almost the same delay as the regular layout CVSL, and it induces about 2.6 times more rising delay and around 4.7 times less falling delay than that of the regular static CMOS AND gate. The CVSL gate has a different rising and falling delay because of the different size of PMOS and NMOS transistors. It has a faster falling delay because of the fast switching of the two small cross-coupled PMOS transistors.

Table 5.7 Rising and falling delay of the six logic gates

Design	Rising delay (ps)	Falling delay (ps)
Static AND gate	16.553	32.301
CVSL with regular layout	59.714	5.676
CVSL with new layout	61.136	4.538
Regular dynamic AND gate	42.794	\
Dynamic logic with differential keepers	50.842	72.85
Differential dynamic logic	56.89	89.48

We can see that the regular dynamic AND gate has no falling delay because of its monotonicity. It cannot change from 1 to 0 during the evaluation phase, because node A will change from 0 to floating when the input changes from 1 to 0. That is the shortcoming of regular dynamic

logic circuits and the reason they are sensitive to SEUs. The differential dynamic logic removes the monotonicity and can switch from 1 to 0 or 0 to 1, with the cost of a 33% increase in the rising delay because of the additional transistors.

Table 5.8 Power consumption of the six logic gates

Design	Power consumption (uW)
Static AND gate	0.442
CVSL with regular layout	1.56
CVSL with new layout	1.43
Regular dynamic AND gate	0.592
Dynamic logic with differential keepers	2.07
Differential dynamic logic	3.06

Table 5.8 shows the power dissipation of these six logic gates simulated by Spectre in the 65nm CMOS Bulk technology with the conditions of 27°C, 1V, and a typical process corner. The CVSL with the new layout saves 10% power compared to the regular layout CVSL. The differential dynamic logic uses 5 times more power than the regular dynamic AND gate and 40% more power than the differential keeper design. This is it doubles the transistor number compared to the regular dynamic gate, and has two more transistors compared to the differential keeper design.

Table 5.9 Area of the six logic gates

Design	Area (μm^2)
Static AND gate	3.6
CVSL with regular layout	4.32
CVSL with new layout	3.51
Regular dynamic AND gate	3.96
Dynamic logic with differential keepers	8.1
Differential dynamic logic	9.36

Table 5.9 lists the area of these six logic gates. Compared to the regular CVSL, the proposed CVSL design reduces the area by 20%. The differential dynamic logic doubles the area of the regular dynamic logic, and it uses 15% more area than the differential keepers design.

In summary, the proposed layout-based CVSL design reduces critical charge by 3 times and cross section by 5 times compared to the regular static CMOS gate. It also reduces SET soft errors by 15% compared to the regular layout CVSL structure, and saves 10% in power and 20% in area. In addition, the proposed CVSL design reduces the width of SETs, so it is a better choice for high speed circuits.

The proposed differential dynamic logic eliminates SEUs compared to the regular dynamic logic. It enhances critical charge by a maximum of 52% at the cost of delay, power consumption, and area. Compared to the dynamic logic with differential keepers, the proposed design has a maximum of 50% higher critical charge and shorter SETs.

CHAPTER 6: TEST CHIP DESIGN AND EXPERIMENTAL RESULTS

A test chip including the proposed Quatro-based flip-flop chain was implemented in the TSMC 65nm CMOS Bulk technology. The test chip design is introduced in section 6.1. A test system was set up to carry out the radiation experiments, which is described in section 6.2. The results of alpha and heavy-ion tests are shown in sections 6.3 and 6.4, respectively.

6.1 Test Chip Design

6.1.1 Flip-flop Chains

Figure 6.1 shows the diagram of a flip-flop chain. As explained above, each flip-flop consists of two latches and transmission gates. When the clock is 0, the data is stored in the first latch. It will be written into the second latch as the outputs after the rising edge of the clock. In this chip, a FF chain including 600 proposed FFs was implemented. Table 6.1 lists the transistor size of the proposed FF. The names of all transistors are the same as those in Figure 4.2.

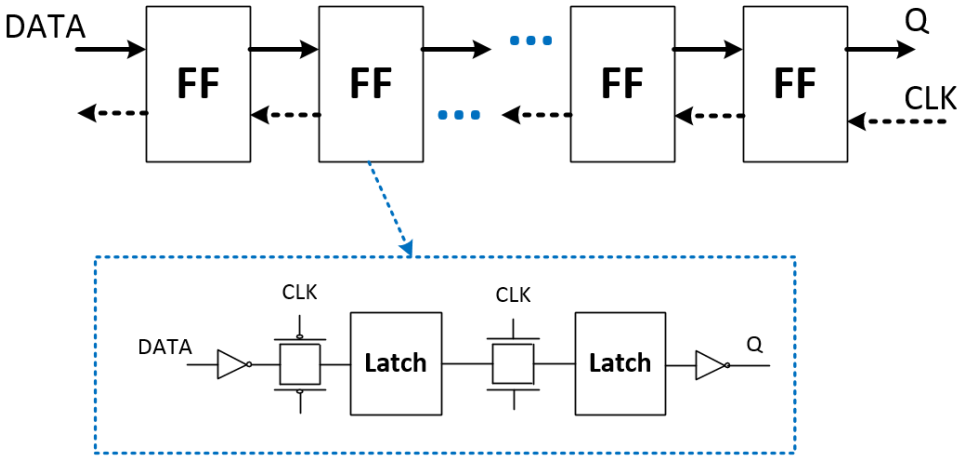

Figure 6.1 Diagram of a flip-flop chain

Table 6.1 Transistor size of the proposed FF design

Transistors	Width (nm)	Length (nm)
P1 / P2 / P3 / P4 / P2P / P3P	150	60
N1 / N2 / N3 / N4	150	60
Transmission gates (PMOS and NMOS)	300	60
Inverters (PMOS)	400	60
Inverters (NMOS)	290	60
Clock buffers (PMOS)	400	60
Clock buffers (NMOS)	300	60

6.1.2 Clock Network and Power Grid

For the clock network, a reverse clock scheme is used in the proposed FF chain. Different from the input data, which passes from the very first FF to the last one, the clock signal transfers from the very last FF back to the first one. A buffer is added between the clock signals of every two FFs, as depicted in Figure 6.2.

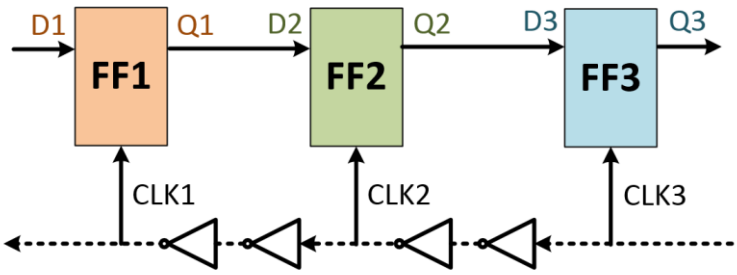

Figure 6.2 Diagram of reverse clock

The reverse clock can help to remove the hold time violation of every second stage FF. The mechanism is explained as follows.

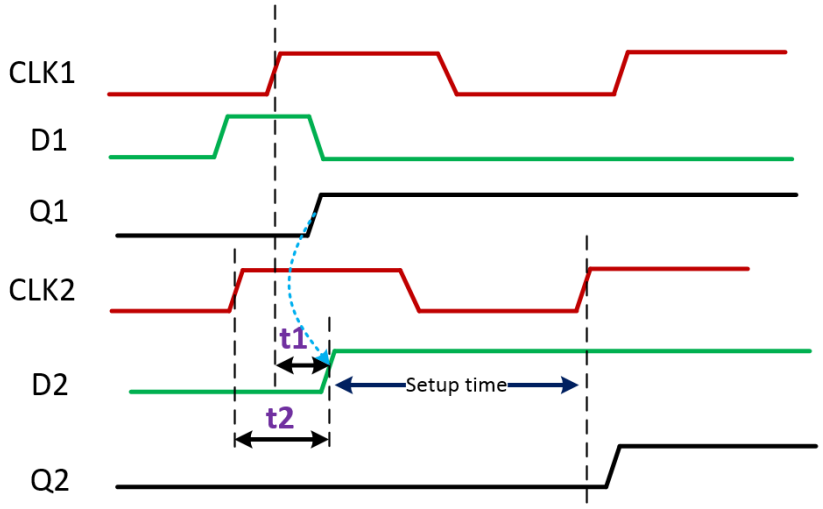

Figure 6.3 Timing analysis of the reverse clock between two adjacent FF cells

Because of the buffer between CLK1 and CLK2, the rising edge of CLK2 arrives earlier than CLK1, as shown in Figure 6.3. As explained in chapter 2, the setup time means that data must be stable before the rising edge of the clock. D2 must retain its value during the setup time before the rising edge of CLK2. D2 is the signal after a certain wire delay of Q1, as shown in Figure 6.2. As the timing analysis diagram shows in Figure 6.3, the time from D2 to the rising edge of CLK2 is large enough, so each FF, except the very first one, will not have a setup time violation. Precaution should be taken to ensure the first FF also does not have setup violations.

The hold time means that data should also be stable for a certain time after the rising edge of the clock. If inputs change too fast after the rising edge of the clock, the outputs may change. In Figure 6.3, if CLK2 and CLK1 are same, t1 will be the hold time of the second FF. In this cycle, logic 0 (D2) is written into FF2 and will be read out in the next cycle. If D2 changes from 0 to 1 too quickly, the output of this cycle will be logic 1, instead of 0. This is a hold time violation. Since

the reverse clock is used by adding buffers between every two clock signals of the FFs, the previous CLK (CLK1) always has a short delay relative to the following CLK (CLK2). As a result, the hold time stretches from t1 to t2. This can effectively remove the hold time violation in FF chains.

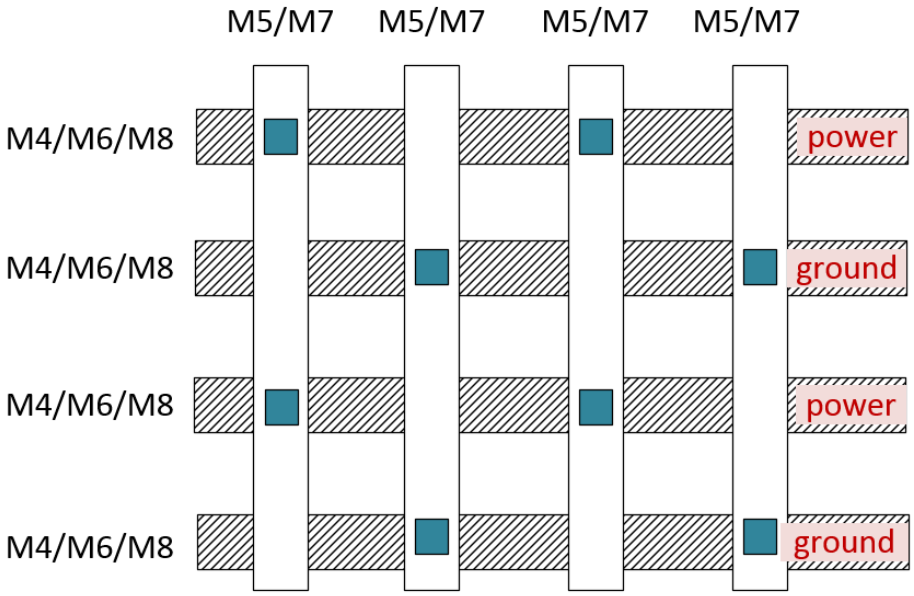

Figure 6.4 Power grid of the test chip

Another consideration during the design of FF chains is IR drop. IR drop is the power supply voltage variations between the power and ground networks. With the development of semiconductor technologies, the metal lines in metal layers, which are used as wires, become narrower, and the increased resistance contributes to the voltage drop. To prevent IR drop, the power grid structure in Figure 6.4 is applied. For example, if a FF cell uses metal layers 1, 2, and 3, then metal layers 4 to 8 can be used as the power and ground connections. The power and ground metal layers are placed in parallel or pass across each other, which can reduce the total resistance and offer a robust power supply for every FF cells.

6.1.3 Overall Chip and Verification

Figure 6.5 is the screenshot of the overall test chip designed in the 65nm CMOS Bulk technology. Bonding pads are placed on the top and bottom of the chip, which are used to connect the pins on a package and the design circuits on a die. An 80-pin Surface Mount Ceramic Quad Flat Package (CQFP80) is used as the package. The Input/Output (I/O) subsystem is responsible for communicating data between the chip and the external world. PVDD1DGZ and PVDD2DGZ are the two types of standard library IO cells used to provide the power supply for core and IO circuits, respectively. PVSS1DGZ and PVSS2DGZ are the ground I/O cells for the ground supply of core circuits and I/O cells, respectively. Another cell, named PVDD2POC, is applied as the power-on control power pad to provide I/O power supply. The ESD structures in the I/O cells can protect the test chip from damage by Electrostatic Discharge (ESD).

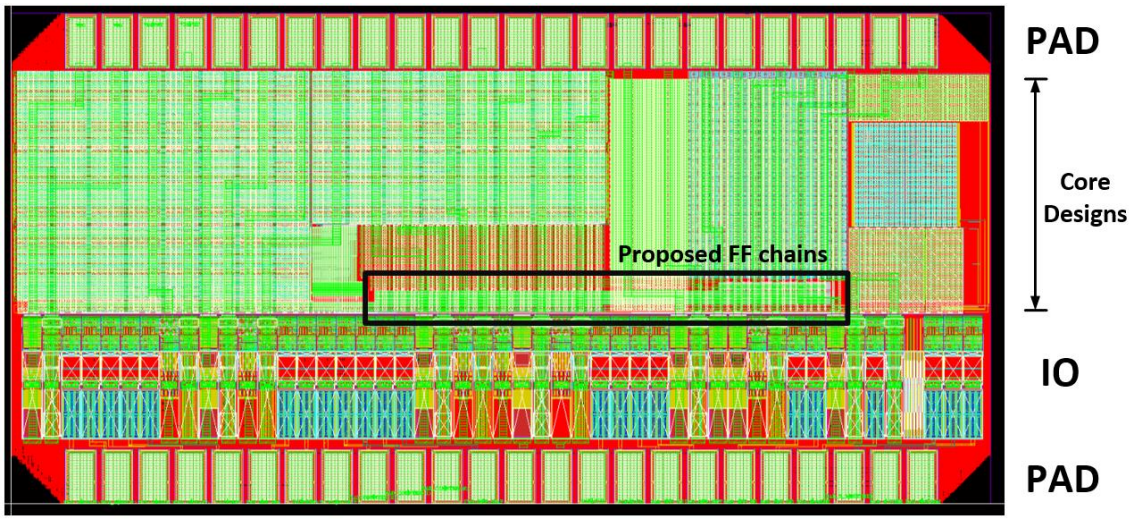

Figure 6.5 Overall chip design

Since it takes a relatively long time and large memory to perform the post-layout simulation on each FF chain (with 600 FFs), Verilog netlist was extracted by using the NC-Verilog and imported into the Modelsim to conduct functional tests. A pulse was injected as the input, and it was observed at the output of the FF chain after 600 cycles, which proved the design was working

properly. A 6-level FF chain was setup to conduct post-layout simulations with different temperatures, supply voltages, and process corners, as listed in Table 6.2. The “TT corner” indicates that NMOS transistors are typical and PMOS transistors are typical; the “FF corner” indicates that NMOS transistors are fast and PMOS transistors are fast. Figure 6.6 shows the waveforms of the clock, data input, and output in the SS process corner (in the worst case, NMOS transistors are slow and PMOS transistors are slow). All the simulations show that the data can pass through the FF chain correctly.

Table 6.2 Post-layout simulation conditions

Process corner	TT	FF	FS	SF	FF
Temperature	0˚C	25˚C	50˚C	75˚C	\
Supply voltage	0.8 V	0.9 V	1.0 V	1.1 V	1.2 V

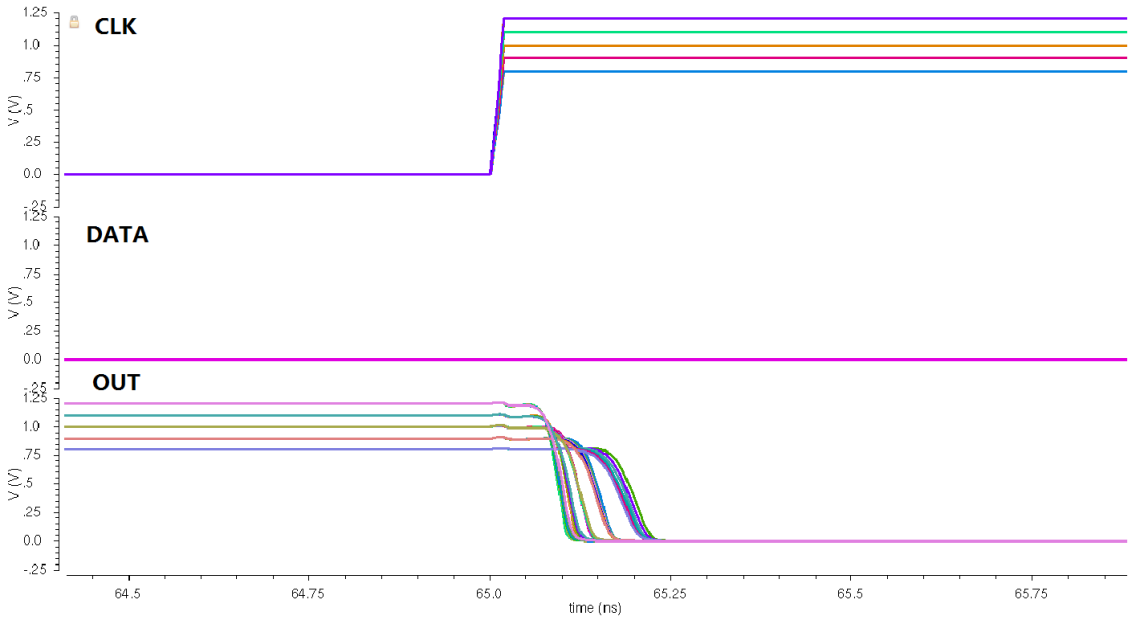

Figure 6.6 Post-layout simulation waveforms

6.2 PCB Design and Test System Setup

The test chip was mounted on a custom-designed Printed Circuit Board (PCB). The four-layer PCB board with a 244-pin mini dual in-line memory module (DIMM) interface was designed using the Altium Designer. Figure 6.7 shows the layout of the PCB, and Figure 6.8 is the picture of the real PCB board soldered with two test chips with the lids open.

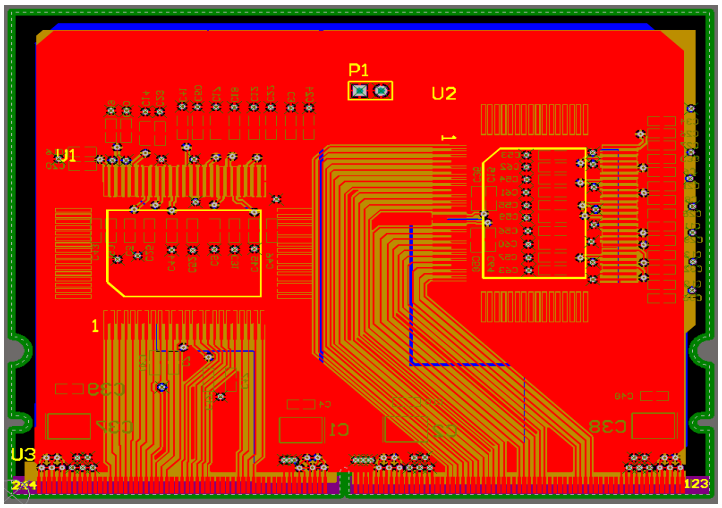

Figure 6.7 Designed PCB by Altium Designer

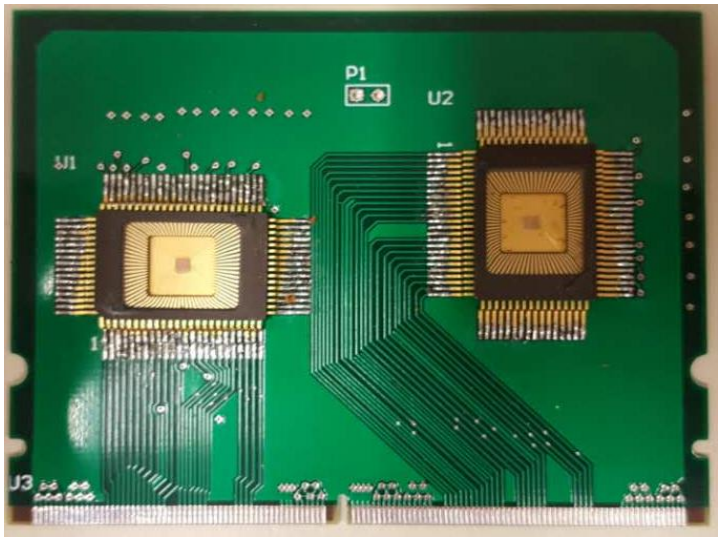

Figure 6.8 PCB and test chips

The testing system includes a configurable power, a daughterboard embedded with the test chip, a Xilinx Virtex-5 Field Programmable Gate Array (FPGA) motherboard, and a Raspberry Pi, as shown in Figure 6.9. The configurable power is used to offer different power supplies to the test chip (1V for core circuits and 2.5V for I/O circuits) and the FPGA. The FPGA is used to generate data patterns (All-0, All-1, and checkerboard), to compare the outputs of the test chip with its inputs, and to calculate the number of errors. Receiving the commands from the Raspberry Pi, the FPGA sends All-0, All-1, or checkerboard data pattern into the DUT (Device Under Test). It also accepts the outputs of the DUT, and then, compares the outputs with its inputs. Counting the errors through an accumulator, the FPGA passes the error number to the Raspberry Pi. The number is displayed on the monitor of the Raspberry Pi.

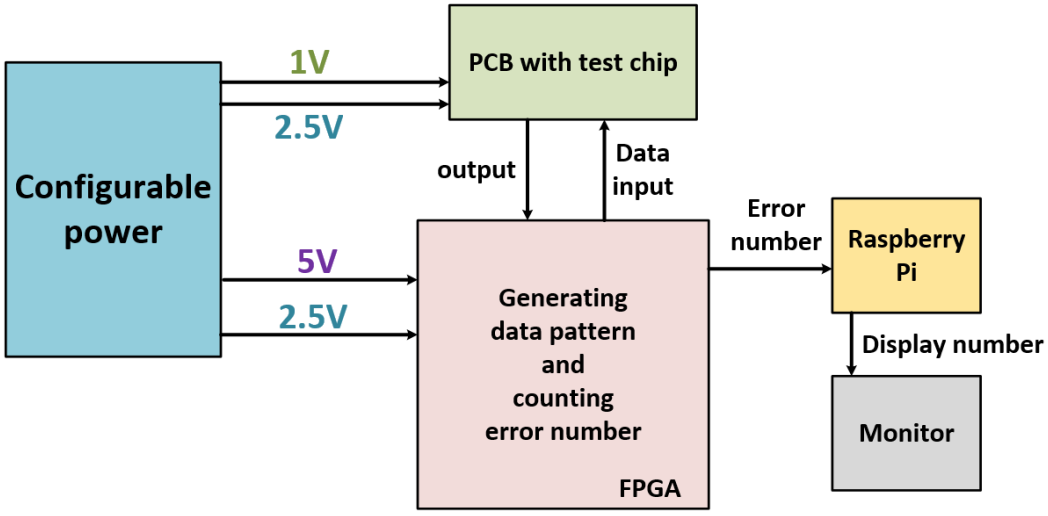

Figure 6.9 Diagram of the test system

The functional tests include four cases. The output of the All-0 pattern should be All-0. The output of the All-1 pattern should be All-1. The output of the checkerboard pattern should be …101010…. For these three cases, no error should be recorded. The last case is the pulse pattern input (one pulse cycle and 100 All-0 cycles). The output should be the same as the input after

delayed 600 cycles and the errors are twice the number of the pulses. The proposed FF chain passed all the functional tests with 1V/ 100 kHz and 1V/ 1MHz. Therefore, we can say that the proposed design works correctly.

6.3 Alpha Test Results and Analysis

An alpha test was conducted at the University of Saskatchewan. An Americium-241 5.5 MeV alpha source with 2.5uCi activity and 4.61×10^{7} a/cm^2/h emissivity was placed on top of the designed circuits whose top lid was removed before the experiments [56].

Figure 6.10 shows the setup environment of the alpha experiment. A Quatro FF chain designed previously by another student in the group was used as the reference design. The size of the transistors in these two FFs is same. Alpha experiment parameters and results are listed in Table 6.3. FIT/MFF (Failure-In-Time/Mega Flip-flops) is the number of errors of devices per 1M bits and per one billion hours.

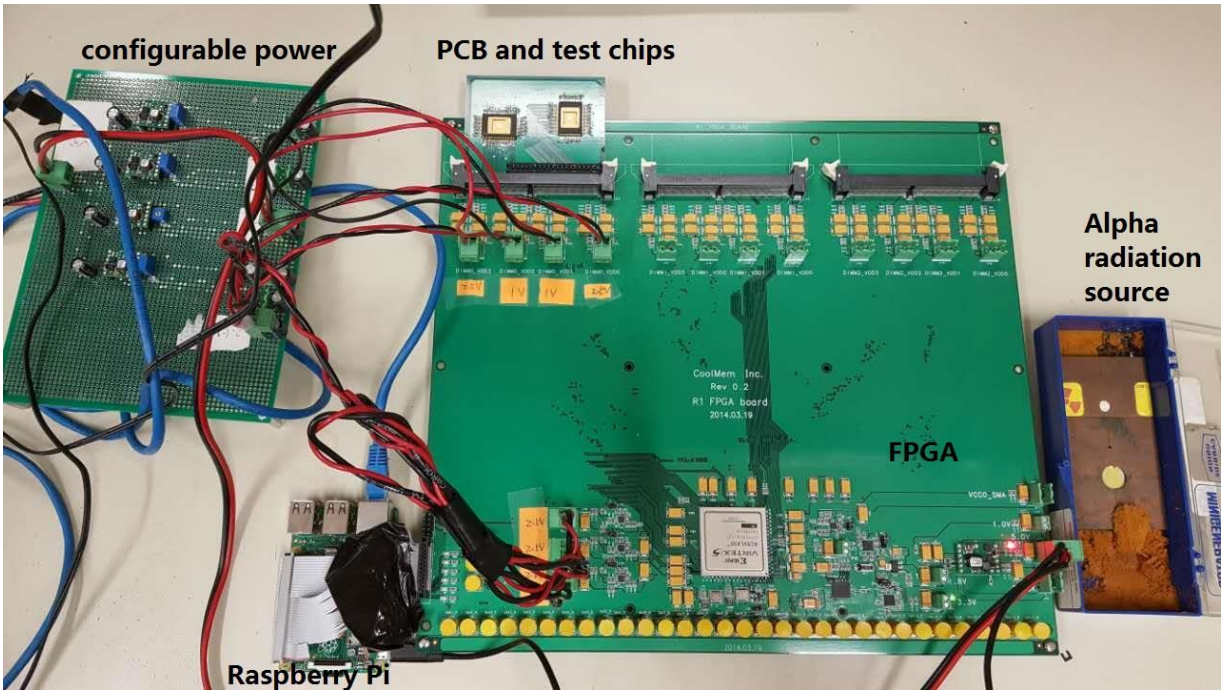

Figure 6.10 Alpha test setup

Table 6.3 Alpha test results of reference Quatro FF and proposed FF

	Reference Quatro FF	Proposed FF
Data pattern	Checkerboard	Checkerboard
Radiation duration (hour)	52	52
Supply voltage	1V	1V
Cell number	1005	600
Error number	366	0
FIT /MFF	152	0

The alpha radiation results in Table 6.3 were tested with operating frequency 100kHz. The alpha experiments on the reference Quatro design and proposed design were repeated for 6-7 times in different chips. The proposed Quatro-based FF shows no error every time when exposed to the alpha radiation source. However, the average FIT/MFF of the regular Quatro FF is 152 with the checkerboard input pattern. The reason is that the two additional PMOS transistors in each proposed latch improve the critical charge of nodes X3 and X4, which are the most sensitive storage nodes of the regular Quatro FF. As analyzed in chapter 4, P2P and P3P also improve the recovery current of PMOS networks in nodes X3 and X4, which increases the SEU tolerance of the proposed design.

The SEU simulation results by Spectre exhibit that the proposed design has 2 times the critical charge of the regular Quatro FF, which means the proposed FF has higher a LET threshold than the reference one. This new design shows no error in the alpha experiment, but the reference one shows more than 300 errors. The proposed FF is immune to SEUs from alpha radiation. Sensitivity maps from TFIT simulations in chapter 4 show that the new design has no sensitive area when LET is 2 MeV-cm^2/mg, whereas the regular Quatro FF shows a sensitive region with the same radiation exposure. A conclusion can be drawn that the Spectre and TFIT simulation results match the alpha experiment outcomes. Since alpha particles from packaging materials are one of the main radiation

sources in terrestrial environments, the proposed design can effectively reduce the SERs of ICs in ground level applications.

6.4 Heavy-Ion Test Results and Analysis

Heavy-ion tests were performed at the HI-13 Tandem Accelerator, China Institute of Atomic Energy (CIAE), Beijing, China. The FPGA and the daughterboard with the test chip were exposed to radiation particles with 1V supply voltage in Figure 6.11. Table 6.4 shows the parameters of heavy ions for these experiments.

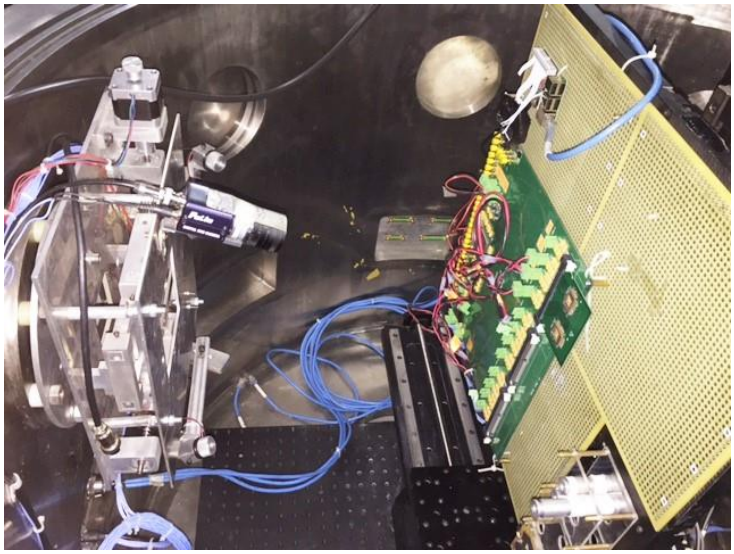

Figure 6.11 Heavy-ion test setup

Table 6.4 Parameters of heavy ions

particles	LET (MeV-cm^2/mg)	Energy (MeV)	Fluence (/cm^2)
C	1.82	75	3.00E+07
F	4.43	100	3.00E+07
Cl	13.9	155	5.00E+07
Ge	37	210	5.00E+07

Heavy-ion experiments were also conducted at 100kHz clock frequency. The cross section curve with LETs expresses the radiation tolerance level. The cross section can be obtained by equation (6.1). Fluence is the number of particles passing through a unit area. A larger cross section means weaker radiation tolerance.

$$\text{Error cross section} = \frac{Number\ of\ total\ errors}{number\ of\ FF\ cells \times Fluence} \tag{6.1}$$

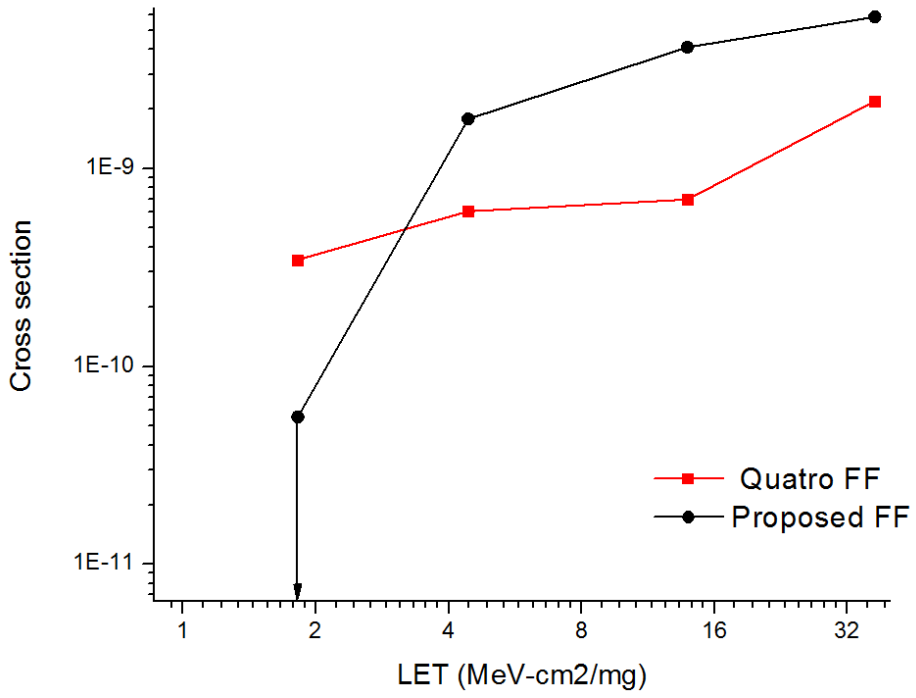

Figure 6.12 Heavy-ion cross section of the reference and proposed FFs

Figure 6.12 depicts the heavy-ion experiment results of the proposed and Quatro designs with the All-0 input pattern. When LET is 1.82 MeV·cm^2/mg, the proposed FF has no error, but the cross section of the reference FF is 3.46810^{-10} cm^2. We can conclude that the LET threshold of the proposed design is higher than 1.82 MeV·cm^2/mg, and that of the Quatro FF is lower than 1.82 MeV·cm^2/mg. The proposed design is immune to radiation particles with low LET values. This conclusion agrees with the alpha experiment results and TFIT simulation results.

However, the cross section of the proposed design is $5.83*10^{-9}$ cm^2 with 37 MeV-cm^2/mg LET value, and that of the reference design is $2.19*10^{-9}$ cm^2 at the same LET value. The proposed FF shows a SER around 2 times greater than that of the reference Quatro design. This can be explained by the sensitivity maps from the TFIT simulations. When the LET is higher than the LET threshold, the sensitive area of the proposed design is larger than that of the regular design. The larger sensitive region is from the Drains of the two additional transistors in each of the two latches, P2P and P3P. One of the two Drains is reverse-biased and creates a sensitive region in the storage node X3 or X4.

In summary, alpha particles as well as heavy-ion exposures have been performed and the radiation experimental results indicate that the proposed design with two more PMOS transistors in each latch is immune to alpha particles, and has a higher LET threshold than the traditional Quatro design. The overhead of the proposed design is an increase of 20% in area, 15% in delay, and 60% in power dissipation. Conclusions from the irradiation experiments match the TFIT simulation results.

CHAPTER 7: SUMMARY AND FUTURE WORK

7.1 Summary

With the development of semiconductor technologies, integrated circuits have more transistors in a unit area and a lower supply voltage as well as higher operating speeds. However, the scaling of silicon technologies also increases the SERs in integrated circuits induced by SEEs. Increasing the radiation tolerance of devices becomes a continuous challenge for researchers in this community.

This thesis detailed the mechanism of SEEs and introduced the main radiation particle sources, namely alpha particles, heavy ions, neutrons, and protons. SEEs take different forms in sequential circuits and combinational circuits. SEUs in sequential circuits and SETs in combinational circuits were analyzed based on the different circuit structures.

After introducing the radiation effect background, the thesis reviewed current radiation hardening designs from schematic-level to layout-level. As typical representatives of the schematic-level, TMR, guard-gate, DICE, and Quatro perform well when exposed to a SEE, but their overhead of delay, area, and power cannot be ignored. By examining the mechanisms of charge sharing and pulse quenching, the last section introduced the advantages and disadvantages of layout mitigation methods, including node separation, guard rings, and LEAP.

The study of hardened sequential cells focused on the Quatro flip-flop design. A proposed Quatro-based latch aiming to be immune to alpha particles with minimum overhead was introduced and compared with the regular Quatro design, through soft error simulators. A 65nm CMOS technology test chip including the proposed FF chain was designed and exposed to alpha particles and heavy-ion radiation. Radiation experimental results were analyzed.

Besides sequential circuit cells, two combinational logic gates were proposed in this thesis. A proposed CVSL using a layout hardening method and a proposed differential dynamic logic gate were simulated and compared with their reference designs. Other performances related to area, delay, and power were analyzed and compared.

7.2 Conclusions

Because the original Quatro latch design is sensitive to alpha particles, which can be found in packaging materials even in ground-level applications and threaten the high-reliability circuits, a new SEE hardened latch was proposed by adding two more transistors. Results from soft error simulation tools indicate that the proposed design has 2 times the critical charge and a higher LET threshold compared to the regular Quatro design. A 65nm CMOS Bulk technology test chip including the proposed design was implemented, and a test system was set up to carry out irradiation experiments. The proposed design is immune to alpha particles and heavy ions with low LET values. The increased SEU tolerance also brings some insignificant penalties of 20% area, 15% delay, and 60% power consumption compared to its reference counterpart. A conclusion is drawn that the proposed latch is SEU-free from alpha particles and heavy ions with low LET values and is a suitable candidate for ground-level high reliability applications.

A CVSL using a layout hardening method was designed in the 65nm technology. TCAD simulation shows that the proposed design has at a maximum 3 times the critical charge and a 1/5 cross section compared with the regular static logic gate. By saving 10% power and 20% area, the proposed CVSL has 15% less cross section than the regular layout CVSL. TFIT simulations also show that the CVSL structure can shrink a SET pulse width to less than 25ps when LET is 4.4 $MeV \cdot cm^2/mg$.

Regular dynamic logic gates have poor performance to SETs and are sensitive to SEUs. To solve this problem, a differential dynamic logic gate was proposed. A soft error simulator was used to evaluate the radiation tolerance of the proposed and reference designs. The proposed design removes SEUs in the evaluation phase. Compared to the regular dynamic logic and differential keepers dynamic gate, the proposed differential dynamic logic increases the critical charge by 50% with a cost of 30% additional delay. The results of SET characteristics analysis show that the proposed differential dynamic gate has shorter SET pulses than the other two designs, making it more suitable for high-speed circuits.

7.3 Future Work

The flip-flop chains in the test chip has 600 stages, which can be increased to 1000~2000 stages for more accurate radiation results and performance evaluation. This proposed design in 28nm or more advanced technologies can be explored in the future to evaluate its immunity to alpha particles and low LET heavy ions with advanced technologies. Overhead of area, delay, and power can be optimized by changing the layout of the proposed design and transistor size.

Besides TCAD simulations, the two proposed logic designs can be implemented in 65nm or more advanced technologies and be operated at higher clock frequencies to test their radiation hardening performances.

These three designs can be developed into standard cells with different drive capacitance which can be widely used into space applications and terrestrial designs. The methods in these three designs can be explored in other FF structures and combinational logic gates, and they also can be integrated into one design to obtain a high-performance radiation-tolerant circuit. The combination of schematic hardening method and layout-based hardening design is a promising work to improve the robustness of circuits.

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