Study of Single-Event Transient Effects on Analog Circuits

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by

Tao Wang

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ABSTRACT

Radiation in space is potentially hazardous to microelectronic circuits and systems such as spacecraft electronics. Transient effects on circuits and systems from high energetic particles can interrupt electronics operation or crash the systems. This phenomenon is particularly serious in complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) since most of modern ICs are implemented with CMOS technologies. The problem is getting worse with the technology scaling down. Radiation-hardening-by-design (RHBD) is a popular method to build CMOS devices and systems meeting performance criteria in radiation environment.

Single-event transient (SET) effects in digital circuits have been studied extensively in the radiation effect community. In recent years analog RHBD has been received increasing attention since analog circuits start showing the vulnerability to the SETs due to the dramatic process scaling. Analog RHBD is still in the research stage. This study is to further study the effects of SET on analog CMOS circuits and introduces cost-effective RHBD approaches to mitigate these effects.

The analog circuits concerned in this study include operational amplifiers (op amps), comparators, voltage-controlled oscillators (VCOs), and phase-locked loops (PLLs). Op amp is used to study SET effects on signal amplitude while the comparator, the VCO, and the PLL are used to study SET effects on signal state during transition time. In this work, approaches based on multi-level from transistor, circuit, to system are presented to mitigate the SET effects on the aforementioned circuits. Specifically, RHBD approach based on the circuit level, such as the op amp, adapts the auto-zeroing

cancellation technique. The RHBD comparator implemented with dual-well and triple-well is studied and compared at the transistor level. SET effects are mitigated in a LC-tank oscillator by inserting a decoupling resistor. The RHBD PLL is implemented on the system level using triple modular redundancy (TMR) approach. It demonstrates that RHBD at multi-level can be cost-effective to mitigate the SEEs in analog circuits. In addition, SETs detection approaches are provided in this dissertation so that various mitigation approaches can be implemented more effectively. Performances and effectiveness of the proposed RHBD are validated through SPICE simulations on the schematic and pulsed-laser experiments on the fabricated circuits. The proposed and tested RHBD techniques can be applied to other relevant analog circuits in the industry to achieve radiation-tolerance.

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List of Abbreviations

ADC	Analog-To-Digital Converter
AGC	Automatic Gain Controller
AOS	Auxiliary Offset Storage
BICS	Bulk Built-In Current Sensor
CCD	Charge-Coupled Device
CDR	Clock and Data Recovery
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pump
CUT	Circuit Under Test
DFF	D Flip-Flop
DICE	Dual Interlocked Storage Cell
DSP	Digital Signal Processing
DUT	Device Under Test
EDA	Electronic Design Automation
FIT	Failures-In-Time
FPGA	Field Programmable Gate Array
GCR	Galactic Cosmic Rays

IC	Integrated Circuit
IP	Intellectual Property
IOS	Input Offset Storage
ISI	Inter Symbol Interference
LET	Linear Energy Transfer
LO	Local Oscillator
LPF	Low Pass Filter
LUT	Look-Up Table
MBU	Multiple Bit Upset
MIM	Metal Insulator Metal
Op Amp	Operational Amplifier
OOS	Output Offset Storage
PDK	Process Design Kit
PFD	Phase Frequency Detector
PCB	Printed Circuit Board
PLLs	Phase-Locked Loops
RADs	Radiation Absorbed Dose
RHBD	Radiation-Hardening-by-Design
RF	Radio Frequency

RO	Ring Oscillator
SE	Single Event
SEL	Single-Event Latch-up
SER	Soft Error Rate
SET	Single-Event Transient
SEE	Single-Event Effects
SEU	Single-Event Upset
SNR	Signal To Noise Ratio
SPICE	Simulation Program With Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SSSC	Saskatchewan Structural Sciences Centre
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TSMC	Taiwan Semiconductor Manufacturing Company
VCO	Voltage-Controlled Oscillator

1. Introduction

1.1 Motivation

In space, one of the important sources of high energy particles are from far away in the galaxy referred as galactic cosmic rays (GCR) [1]. Even the origin of the GCR is still an open question in the field of astrophysics and astronomy, some of the characteristics of GCR were discovered by scientists. GCR travel at nearly the speed of light and strike the earth from all directions [2]. The GCR typically consists of 85% protons, 14% nucleus of helium atom, which is called alpha particles, and 1% electrons and other high energy heavy ions [3]. Most GCR have energies between 100MeV[1] corresponding to a velocity for protons of 43% of the speed of light and 10GeV corresponding to 99.6% of the speed of light [4], where eV (electron volt) is a unit with energy gained when an electron is accelerated through a potential difference of 1 volt. The other source of the cosmic rays can be associated with solar flares, a sudden brightening observed over the sun surface. Sun flares and other energetic solar events emit a large amount of low energy particles into space, and these high energetic particles' energy range is from several hundred MeV to several GeV [4]. When these particles are passing planets in space, they are accelerated by the magnetic fields that are around these celestial objects due to their negative or positive charges. As the results, these particles achieve high energy. An equation for the energy of a particle in the magnetic field is given by [5].

[1] MeV means million electron volt. $1\text{MeV} \approx 1.602 \times 10^{-13}$ Joules.

$$E = \frac{(QBR)^2}{2M} \tag{1.1}$$

where E is the energy of a particle in Joules, Q is the charge of a particle in Coulomb, B is the strength of magnetic field in Tesla, M is the mass of a particle in Kilogram, and R is the radius of particle circular path in Meter. As these high energetic particles pass through the atmosphere, they collide with the nucleus of the air atoms leading to secondary particles that shower down to the earth surface through the atmosphere. Secondary cosmic rays include neutrons, gamma rays, electrons, and protons [3] [6] [7]. Both primary cosmic rays and secondary cosmic rays contribute to the space radiation environment.

The space radiation environment is potentially hazardous to microelectronic circuits and systems which are used in the aerospace. Energetic particles such as heavy ions, neutrons, and protons can strike sensitive nodes in the circuits, causing temporary effects which are called single-event effects (SEEs) [8]. Permanent failure may occur when the circuits are under total dose effects from continuous exposure in radiation environments [9]. In the 1970's, the first single event (SE) happened in the semiconductor circuits due to cosmic rays and alpha particles was reported in [1] [10] [11] [12]. Another example of SEEs is the SOHO (Solar and Heliospheric Observatory) satellite has experienced four power supply switch-off events since its launch in December 1995. These four events were believed to originate from space radiation in one or more integrated circuits (ICs) [13]. Recently in November 2000, it was reported that the SUN servers were having problems with bit flips in the static random access memory (SRAM) used for the L2 cache memory which were caused by cosmic rays or alpha particles. Geostationary and GPS-satellites are more prone to radiation and inherit

component failures due to SEEs [14]. Memory failures, charge-coupled device (CCD) damage are also examples of the impact of high energy particles on space circuits and systems [15] [16]. As the dimensions and operating voltages of electronic devices that are used in aerospace are reduced to satisfy requirements of functionality, portability, and lower power; their radiation sensitivity such as SEEs, dramatically increases [17].

Radiation effects on CMOS microelectronic circuits can be divided into two categories: the instantaneous effects of the collision of a single energetic particle on the sensitive locations in the circuits, and the cumulative effects caused primarily by the abundant energetic particles over a long period of time. In general, CMOS scaling has improved the cumulative effects tolerance, however reducing the instantaneous effects has become more challenging.

Some lightweight shielding materials can be used to prevent electronic circuits and systems from accumulated radiation damages to a certain degree, however the shielding cannot stop the high energy particles from reaching the electronics. Therefore, in the radiation effects research and development community, the major goal is to study how the energetic particles interact with electronic circuits and to provide radiation-hardened devices, robust circuits and systems that can function as intended over the mission lifetime in the harsh radiation environment. Radiation-hardening can be implemented at the process level by foundries to meet specified radiation performance criteria. While this approach can provide reliable hardened devices but it requires expensive manufacturing processes. Radiation-hardening can also be achieved by designs at transistor, circuit, or system level to meet specified radiation performance criteria without any modification of the existing process or violation of design and layout rules. This particular approach is called radiation-hardening-by-design (RHBD) [18]. The

RHBD approach satisfies IC development trend and relationship between circuits and systems design, and semiconductor fabrication. IC design companies and design houses tape out their designs and their intellectual property (IP) cores to external foundries for fabrication, whereas the RHBD circuits and systems are fabricated with standard commercial processes.

In the past, researchers have focused on the RHBD designs such as single-event transients (SETs)-tolerant in digital circuits. Authors in [19–23] have introduced SET error analysis in combinational logic and sequential logic circuits. There have been special RHBD digital designs such as the radiation-hardened latch [24], and single-event upset (SEU)-hardened memory [25], etc. Successful SEU-hardened designs have operated reliably in popular digital RHBD circuits such as the dual interlocked storage cells (DICE) in hardened memory cells [25], and the triple modular redundancy (TMR) in hardened latches [24]. Unlike a single feedback topology in traditional latches, the DICE implements a dual feedback topology to store a bit. With this approach, at least two critical nodes must be hit simultaneously under SEEs to lead to a SEU. TMR is a popular radiation-hardening approach applied in digital circuits. The major drawback of this method is the penalty in area and power consumption.

In the past, digital circuits were studied more in hardened design than analog circuits because digital circuits are usually implemented with the minimum transistor size while the transistors in analog circuits are much larger. However, in recent years, with the device scaling down, analog RHBD design has received increased attention. In 2000, Addel, et al. [26] performed SET analysis on the analog circuit of an op amp. A radiation-hardened design was applied in one of the important stages in the op amp, the operational transconductance amplifier (OTA) [27]. A mathematical modeling for

radiation-hardened transistors has been presented in details [28]. Hogue, et al. [29] have intended to put the radiation-hardened transistor as a pcell into the standard library for a CMOS process technology. Generally speaking, RHBD design techniques for analog circuits are highly demanded, and should be studied more in the future.

In general, radiation effects such as SET-induced error responses in analog circuits are categorized into two groups. The first group is the signal amplitude variations. Specifically, SEEs in analog circuits are temporary effects in the time domain. The signal amplitude variation can lead to signal distortion and signal to noise ratio (SNR) degradation. This phenomenon becomes considerably worse in the sample and hold (S/H) circuits in op amps, comparators, and analog-to-digital converters (ADCs). The second group of error responses in analog circuits is the signal transition state effect. For example, the output signal of the dynamic comparator is sensitive to SEEs when the sampling clock is active [30]. Other examples are oscillation circuits such as voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs). Signal frequency and phase variations under radiation effects result in loosing lock in the PLLs [31–33].

This dissertation presents the study of SEEs on analog CMOS circuits and their mitigation approaches. Op amps, dynamic comparators, LC-tank oscillators, and PLLs were selected in this study for investigation. The study is of importance due to the following reasons:

First, the signal amplitude of an op amp, the transition time of a dynamic comparator, and the oscillation frequency and phase of a LC-tank oscillator/PLL are critical parameters and important performance indicators in real world applications. All of them are vulnerable to the radiation effects. Second, all of these circuits are widely used not only in aerospace industry but also in consumer electronic products. Op amps

and dynamic comparators are necessary for the interface between analog and digital circuits. Oscillators and PLLs are two critical sub-blocks in the applications of frequency synthesizers, wireless communications, and high-speed data links. Third, op amps and comparators are the fundamental sub-blocks of ADCs design while PLLs are critical sub-blocks of radio frequency (RF) front-end design and clock and data recovery (CDR) design.

All of these circuits were designed in EDA tool (Cadence) with the advanced CMOS process design kits (PDKs). After successfully investigated by schematic simulation, the typical analog IC design flows such as circuit design, layout, and tape out were carried out for the dynamic comparator, the LC-tank oscillator, and the PLL. Normally, RHBD circuits and non-RHBD circuits were taped out in the same chip in order to compare the SET vulnerability between the two. The experiment test including function test and laser validation was followed on the fabricated chips. Experimental results are used to compare the simulation results and to validate the effectiveness of the RHBD approaches.

1.2 Research Objectives

Based on previous discussion, objectives of this thesis work are set as follows:

1. SET effects leading to erroneous signal amplitude and phase sudden change during the transition time will be studied based on some typical analog circuits such as op amps, comparators, oscillators, and PLLs.
2. Depending on the analysis of SET effects in analog circuits, RHBD approaches will be proposed, designed, and implemented on the

aforementioned circuits based on the multi-level approach, namely transistor, circuit and system levels.

- A transistor level based RHBD design will be studied and implemented in a dynamic comparator. nMOS transistors in the comparator will be implemented using dual-well or triple-well technology.
- Circuit level based RHBD design will be studied and applied in an op amp and a LC-tank oscillator.
- System level based RHBD design will be studied and adopted in a PLL. Triple modular redundancy strategy is to be used in the RHBD PLL to obtain a stable oscillation signal under SET effects.

3. An effective SETs detection circuit will be designed and implemented. If the occurrence of a SET event in an IC can be detected in real time, then various SET mitigation approaches would be used at the system level.
4. The performances and effectiveness of SET mitigation approaches are to be investigated and validated by the schematic simulations and pulsed-laser experiments on fabricated circuits.

1.3 Thesis Organization

This thesis is organized as follows: Chapter 2 overviews radiation effects and discusses theory and mechanism of the SET effects on MOS transistors. This chapter also illustrates how SETs affect circuits and systems based on transistor and circuit level analysis. The pulsed-laser used to test the effect of heavy ions on the fabricated circuits is described in this chapter. The background of the analog circuits of op amps, comparators,

LC-tank oscillators, and PLLs are also introduced. Chapter 3 describes a RHBD op amp design to mitigate SET effects using three types of auto-zeroing techniques: input offset storage (IOS), output offset storage (OOS), and auxiliary offset storage (AOS). Chapter 4 introduces different implementation techniques to mitigate SET effects on a dynamic comparator. The hardened dynamic comparator design was verified based on the circuit simulations and experimental results. Chapter 5 presents a SET-tolerant LC-tank oscillator. Both of the circuit simulations and experimental results demonstrated the effectiveness of the proposed mitigation approach. Chapter 6 introduces PLL concepts and topologies. This chapter also provides performance analysis and describes the design of a SET-tolerant PLL. Chapter 7 introduces a design for SET detection which has potential applications in the SET-tolerant digital ICs. Chapter 8 concludes the dissertation and describes research direction for future explorations.

2. Radiation Effects Overview, Background of the Selected Analog Circuits, and Pulsed-Laser Testing

Radiation has both instantaneous and long-term effects on CMOS microelectronic circuits. The instantaneous effects of the collision of a single energetic particle on the sensitive locations in the circuits are called SEEs. The cumulative effects caused primarily by abundant energetic particles over a long period of time are called total ionization dose (TID) effects [34]. In general, CMOS scaling has improved TID tolerance but SEEs still have strong effects on the circuits. Reducing SEEs in advanced CMOS circuits and systems remains a challenge.

2.1 Total Ionization Dose (TID) Effects

Total ionization dose effects have a capability of damaging electronic circuits by ionizing semiconductor material over a certain period of time in aerospace applications [35]. When energetic particles pass through silicon dioxide (SiO_2) layer of a CMOS transistor, they deposit enough energy to break certain atomic bonds in the device that results in forming of electron-hole pairs (i.e., causing ionization). The amount of ionization is related to the total dose absorbed in the silicon dioxide layer and is usually given in units of rads (1rad = 100ergs/gm, while 1erg = 100nJ) [15]. In the regime of TID effects on MOS devices, the main concern from this energy deposition is the trapping of either or both the electrons and holes created in silicon dioxide. These electron-hole pairs can gradually degrade the performance or change functionality of MOS devices. Fig. 2.1 illustrates a simple model of TID generation and trapping of charges in the silicon

dioxide of a MOS device with a positive bias applied to the gate. Fig. 2.1(a) shows a MOS device before the ionizing radiation.

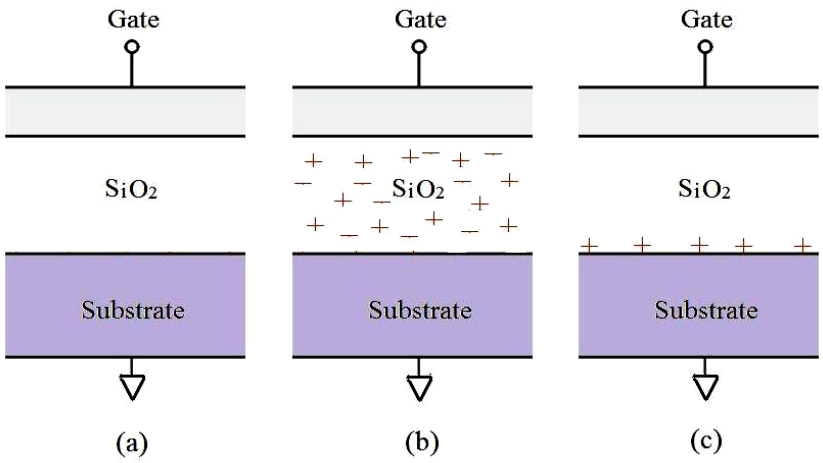


Figure 2.1 Total dose effects on a MOS transistor.

Electron-hole pairs are generated when ionizing radiation passes through the device as shown in Fig. 2.1(b). Before transporting through the oxide layer, most of the carriers recombine within the oxide layer. Higher mobility electrons quickly drift out of the oxide through the gate (in time of the order of picoseconds [36]) while the lower mobility holes are trapped in the silicon dioxide. Under the influence of the internal electric field, a small fraction of holes are trapped near the Si/SiO_2 interface as shown in Fig. 2.1(c). As the total dose in the device accumulates over a certain period of time, the amount of trapped positive charges increases. Eventually, these accumulated charges impact the MOS device properties by resulting in a decreased threshold voltage (V_{thn}) and an increased leakage current between the source and the drain of nMOS transistors. For pMOS transistors, the accumulated charges increase the threshold voltage (V_{thp}). The worst case for nMOS transistors is that positive charges trapping in the gate oxide can cause large leakage current to flow while nMOS transistors are in the off state. For pMOS

transistors, the worst case is that transistors remain off permanently. This effect will not only result in an increase in the static power consumption but also change the logic state, and thus causes permanent failure to CMOS circuits and systems.

To develop a TID-hardened design, state-of-the-art processes with nanometer-thick gate oxide layers have been shown as the effective solution for TID hardening [37]. Due to the scaling rules, the gate oxide thickness must be decreased at each process technology. As a result, the gate oxide thickness of the most advanced process technology is within 1-2nm, which is only a few atoms thick. In this way, the gate oxide traps less positive charges. Therefore, CMOS transistors are naturally becoming more TID tolerant. A published data has been reported at the Boeing Radiation Effects Laboratory with 45nm process shows negligible change in transistor threshold shift and off-state leakage with TID irradiation [34].

The other TID effect occurring in the transistor edge oxide is shown in Fig. 2.2(a). Instead of flowing right below the gate from the drain to the source, the leakage flows along the edge of the active region from the drain to the source of a transistor. These current paths are eliminated by special layout techniques such as enclosed-gate MOSFETs, shown in Fig. 2.2(b) [38]. In this way, current flows from the center to the outside of the device, making it immune to edge leakage current. However, this approach requires a larger area for each transistor, and also introduces a large source/drain capacitance. The most influence for this implementation is the difficulty in building a device model to perform circuit simulations.

In summary, with the scaling-down process, the TID effects becomes insignificant compared to SEEs. This thesis work concentrates on the other effect to CMOS circuits and systems, the SEEs.

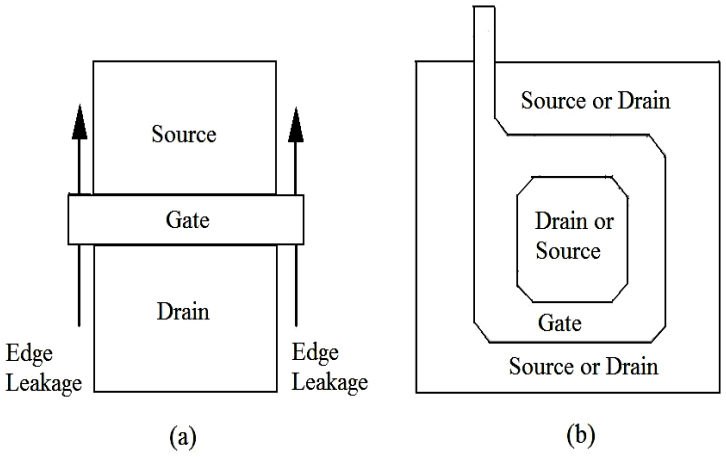


Figure 2.2 (a) TID-induced edge leakage. (b) Enclosed-gate transistor shape [38].

2.2 Single-Event Effects (SEEs)

SEEs are another type of radiation effects coming from a single energetic particle such as heavy ions penetrating a semiconductor material [39, 40]. Heavy particle impacts are random and can happen at any node in the electronic circuits. The heavy particle strikes the lattice structure of the semiconductor, transfers energy to the lattice, and leaves a number of free electron-hole pairs. These electron-hole pairs will recombine without introducing effects if the heavy ion passes through the bulk. However, the most sensitive part to SEEs in semiconductor device structure is the reverse-biased junctions such as n^+/p junction of the drain to substrate in nMOS transistor and p^+/n junction of the drain to substrate in pMOS transistor. One of the reasons for this phenomenon is that the electron-hole pairs will be separated by the electric field before recombination. The electric field comes from the reverse-biased p/n junction voltage potential causing

electrons to be swept to n-diffusion region while holes to be swept to bulk contact regarding nMOS transistors. This drift motion is called charge collection.

The other reason is that the drains of nMOS or pMOS transistors are usually driven by the supply rail through transistors so that the charge collection caused by SEEs cannot be compensated by the supply voltage directly. SEE-induced electron-hole pairs around the reverse-biased junction of the drain nodes of nMOS and pMOS transistors lead to a transient current across device junctions. This may change the voltage level or logic state on the sensitive nodes in analog or digital circuits. SEEs may cause system failures in this situation.

The example shown in Fig. 2.3 illustrates an nMOS transistor under the strike of a particle. Fig. 2.3(a) shows an energetic particle passing through the drain of an nMOS transistor in a few picoseconds while leaving behind a column of ionized material containing a number of electrons and holes. The total numbers of charges are proportional to the linear energy transfer (LET) of the incoming particle as well as the silicon density. LET is the amount of energy deposited per unit of distance as the particle traverses the silicon material. It is usually expressed in MeV-cm^2/mg. These charges are absorbed by the potential of the drain node and bulk node of the nMOS transistor shown in Fig. 2.3(b) before they are dissipated by recombination. When this happens, a transient current pulse is generated flowing from the drain to the bulk in the nMOS transistor as shown in Fig. 2.3(c). In the circuits, this transient current pulse charges or discharges the potential on some critical nodes, and thus pulling up or pushing down the logic level of these nodes.

An example of an inverter is shown in Fig. 2.4. The initial state in this example of input logic is low and the output logic is high. When an ion strikes the drain of the nMOS

transistor, a large number of electron-hole pairs are produced. Electrons will be collected by the node of the drain of nMOS transistor and voltage in this node will drop. A diagram of Fig. 2.5 shows the shape of the transient current pulse. Table 2-1 lists the quantification of the transient current pulse and induced voltage pulse in the 0.25μm CMOS technology [41] [42] [43].

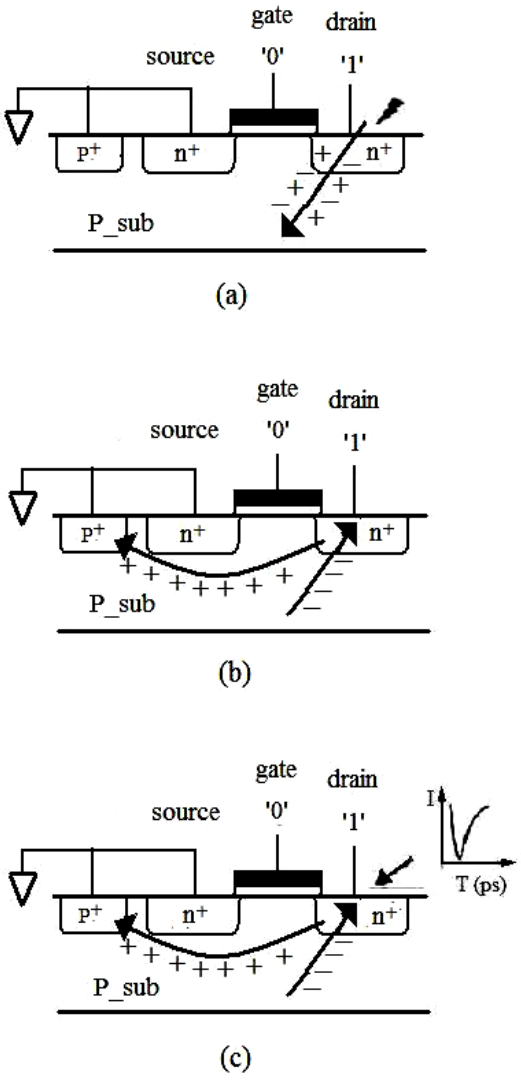


Figure 2.3 Illustration of charge generation, collection and circuit response for a drain node in a nMOS transistor. (a) Charge generation. (b) Charge collection. (c) Circuit response.

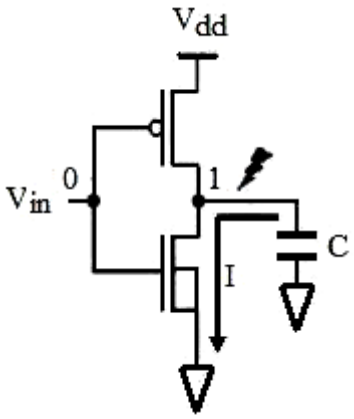


Figure 2.4 Transient error under SEE based on an inverter.

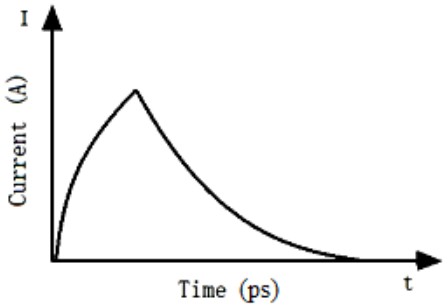


Figure 2.5 The shape of transient current pulse.

Table 2-1 Quantification of the current pulse and the voltage pulse. Both of them are tested under an ion interruption with an energy of 80 MeV-cm^2/mg in 0.25μm CMOS technology.

	Peak amplitude	**Rise time**	**Fall time**
Current pulse	≈6.5mA	≈4ps	≈50ps
Voltage pulse	≈1.2V	≈20ps	≈0.45ns

Unlike the total dose radiation which causes gradual degradation of the device parameters, a single-event interaction is an instantaneous effect in the circuits. As this event typically does not cause permanent damage to the circuits, it is referred as a soft error [34]. Statistics of soft errors in radiation environments are represented by soft error rate (SER), which is defined as the probability of a device having an error or failure which is given in unit of failure in time (FIT) or Failures/10^9 hours [34]. Some types of single-event errors in CMOS circuits include:

A- Single-event upset (SEU) [8]: When digital circuits such as flip-flops, SRAM-cells, and latches are hit by a high energy particle, an upset of internal logic state can happen. An example of this type of error is a state change of a memory bit as shown in Fig. 2.6. The standard 6T SRAM cell is composed of two pMOS transistors and two nMOS transistors forming a positive feedback loop [44] (switch transistors between the cell and word-line are not shown in the figure). This feedback loop maintains the data state of the cell. When an ion strikes at the output of the left side of the inverter where the logic is high, a large number of electron-hole pairs are produced along the particles trajectory and a large portion of these are separated by the electrical field. In this case, electrons will be collected by the node of the drain of nMOS transistor and the voltage in this node will drop. However, the supply rail tries to hold the high logic of this node through the pMOS transistor. As the node voltage drops, a current flowing from the supply voltage starts to charge this node to compensate for the dropped voltage. If the compensation current through the pMOS transistor is not strong enough to compensate for the current induced by SEEs, the voltage at the drain of nMOS transistor drops. If this voltage drops below the threshold voltage of the inverter on the other side of the cell, the SRAM bit flips with positive feedback loop. In this case, an upset of the state occurs [34].

This situation becomes more serious in the low power SRAM design because noise margin decreases with lower power supply and most of transistors are working in the sub-threshold region.

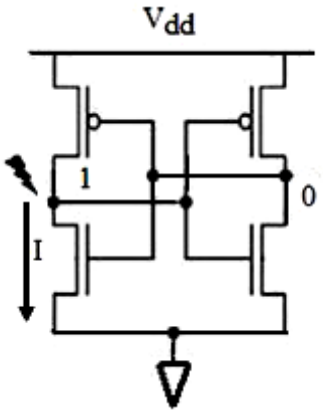


Figure 2.6 SEU in memory cell due to a heavy ion strike.

B- Multiple bits upset (MBU) [45] [46]: Rather than affecting a single bit in memory, an ion could affect several bits. The distance between circuit elements decreases in the down-scaled CMOS processes. If the ion beam incident angle increases, the particles trajectory across multiple devices. In this way, SEE-induced charges are collected by multiple nodes from different devices. More than one bits in the SRAM cells are upset at the same time. The effect of MBU is typically alleviated by a combination of error-correcting code that works on a word-by-word basis. Also layout rules can be defined to prevent physically-adjacent bits from belonging to the same word of memory.

C- Single-event transient (SET) [15]: Once a temporary spike or short signal pulse caused by a heavy ion is generated, it will propagate through logic gates until it reaches a latch or a flip-flop as shown in Fig. 2.7. If the timing of the SET pulse meets the setup and hold times of the latch or flip-flop which is shown in Fig. 2.8, an incorrect

logic will be stored in the latch or flip-flop and thus causes system malfunction. The increasing clock rate leads to increasing SET vulnerability in advanced CMOS technologies, since the clock period has the same order of the width to that of the SETs.

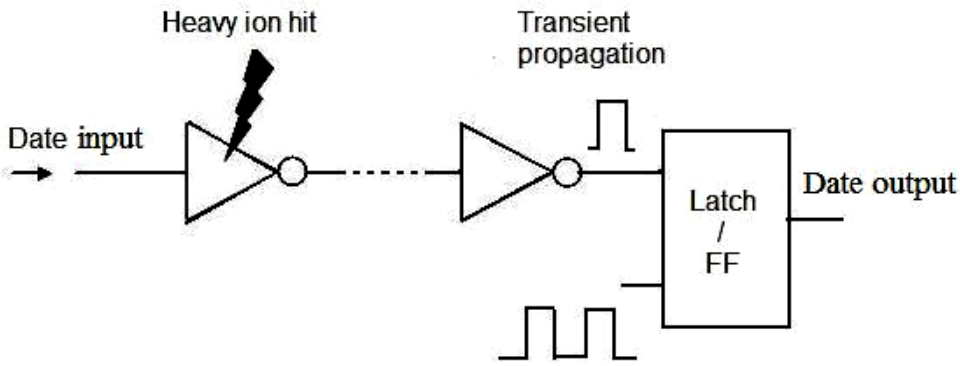


Figure 2.7 SET propagates in a logic circuit.

D- Single-event latch-up (SEL) [47] [48]: In most of the advanced CMOS processes, nMOS transistors and pMOS transistors share the same p-type substrate while pMOS transistors are fabricated in an n-well. In this way, CMOS inherits parasitic bipolar transistors with positive feedback topology in its well structure that can cause latch-up as shown in Fig. 2.9 [44]. For this CMOS structure, a parasitic npn transistor is formed by the n+ (emitter), p-substrate (base), and n-well (collector). Similarly, a parasitic pnp transistor is formed by the p+ (emitter), n-well (base), and p-substrate (collector). This structure forms a positive feedback loop between the two transistors [49].

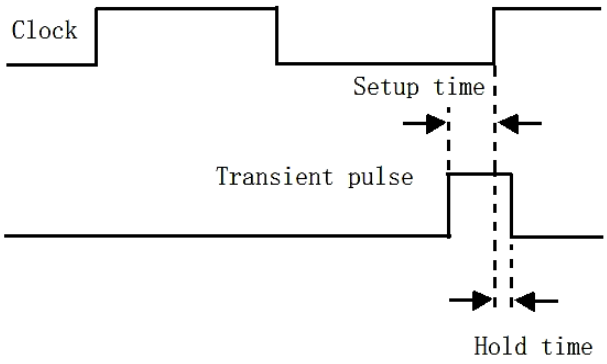


Figure 2.8 Timing of a SET pulse meets the setup and hold time of the latch or flip-flop.

If a heavy ion-induced current flows through the equivalent substrate resistance of R_{sub} to turn on the npn transistor, a current will flow through the equivalent n-well resistor, R_{well}. The voltage drop across R_{well} can be high enough to turn on the pnp transistor. As a result, a direct path from power supply to ground causes serious latch-up. This problem cannot be corrected until the power is removed and put back on again.

The SEL can cause permanent damages to the circuits since there is a short path between power supply and ground. SEL protection can be implemented by layout strategy. Depending on the process layout rule of the space between the p+ and n+, the p+ contact can be moved closer to the n+ diffusion region in the p-substrate while the n+ contact can be moved closer to the p+ diffusion region in the n-well. In this way, the resistances of R_{sub} and R_{well} can be so small that the voltage drop across it cannot turn on these two parasitic bipolar transistors.

The other SEL protection approach in the layout is to reduce the gain product of the two parasitic bipolar transistors by moving the n-well away from the n+ source/drain. The gain product of the two parasitic bipolar transistors is a prerequisite condition for latch-up. In theory, if the gain product of two parasitic bipolar transistors is less than one,

then latch-up can be avoided. The width of the base of the npn transistor increases in this way and leads to a gain reduction.

Some of other SEL protection approaches such as high substrate doping and high well doping, putting guard ring round the pMOS and nMOS devices separately as shown in Fig. 2.10 are also introduced [34]. The purpose of these approaches is intended to decrease the resistances of R_{sub} and R_{well} shown in Fig. 2.9.

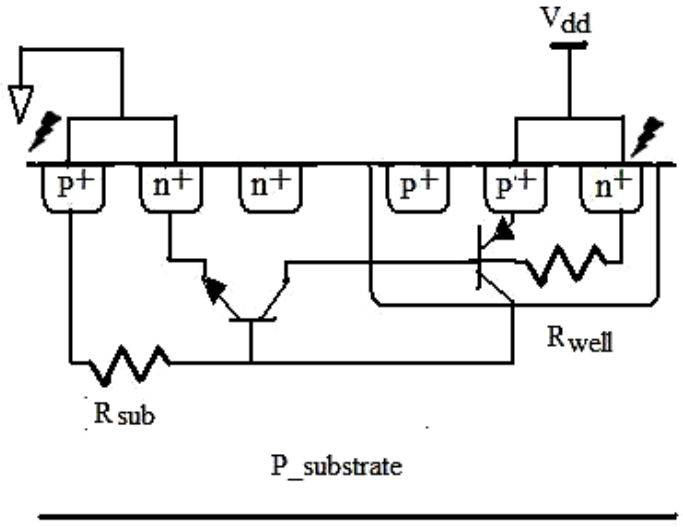


Figure 2.9 Diagram of the parasitic latch-up structure in a CMOS inverter.

In contrary to TID, SEEs on ICs become more significant for advanced CMOS technologies, especially SETs and SEUs. Soft error rate (SER) in nanometer circuits and systems increases due to three main reasons. First, the current drivability decreases because of the use of lower power supply voltage and the smaller transistor size. Second, the capacitances including parasitic capacitors and load capacitors at the SEE-sensitive nodes reduce. Third, for high-speed application using the nanometer technology, the circuits and systems are more vulnerable to SETs as the clock rate increases.

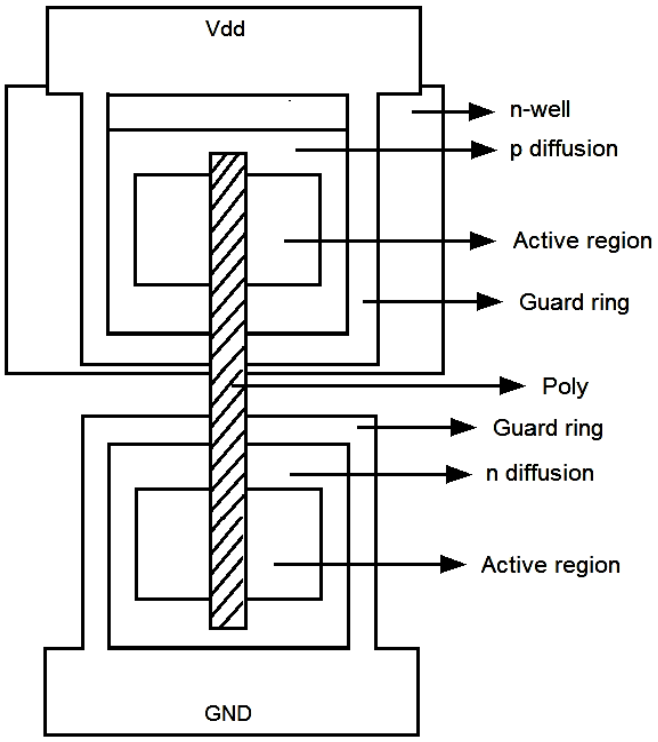


Figure 2.10 A CMOS device with guard ring.

2.3 General SEU/SET Mitigation Approaches

To develop digital SEE-hardened designs, a transistor with a large width can be implemented to improve the current drivability and increase the capacitance at the sensitive nodes. This hardening approach can be implemented in the latches, flip flops, and SRAM cells. Obviously, there is a tradeoff between SEU hardness and circuit speed and area. Large transistor size is preferred for the SET propagation path since the low pass nature of digital circuit may shorten the pulse at each stage until it disappears [34]. However, this hardening approach is not practical because a SEU can happen at any node while a SET can propagate through any path. In addition, it is impossible to enlarge all of

the transistors to mitigate SEEs. Even a timing-critical path is analyzed satisfactory by electronic design automation (EDA) tools, large transistors can slow down the signal propagation in this path. Low pass filter such as a simple RC circuit as shown in Fig. 2.11 can be inserted into the sensitive nodes to filter out the high frequency SET pulses. However, this approach is still subjected to the tradeoff between SET hardening and circuit speed and area. As a result, special approaches to mitigate both SETs and SEUs are essential in modern CMOS technologies used in the applications for radiation environments.

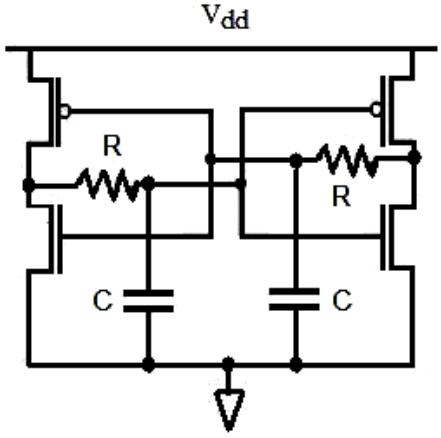


Figure 2.11 A SEU-hardened approach with RC filters in a SRAM cell.

Pulse width filtering with inserted delay [34]: Normally the width of the SET pulse is shorter than the propagation signal width. A delay unit with an inverter chain can be designed to make the delay time longer than the SET pulse width but must be shorter than the signal width. In this case, as shown in Fig. 2.12, the SET pulse can be filtered out while the normal signal is allowed to pass. The disadvantage of this method is that

there is a tradeoff between speed and SET hardening because an additional delay is introduced into the signal path.

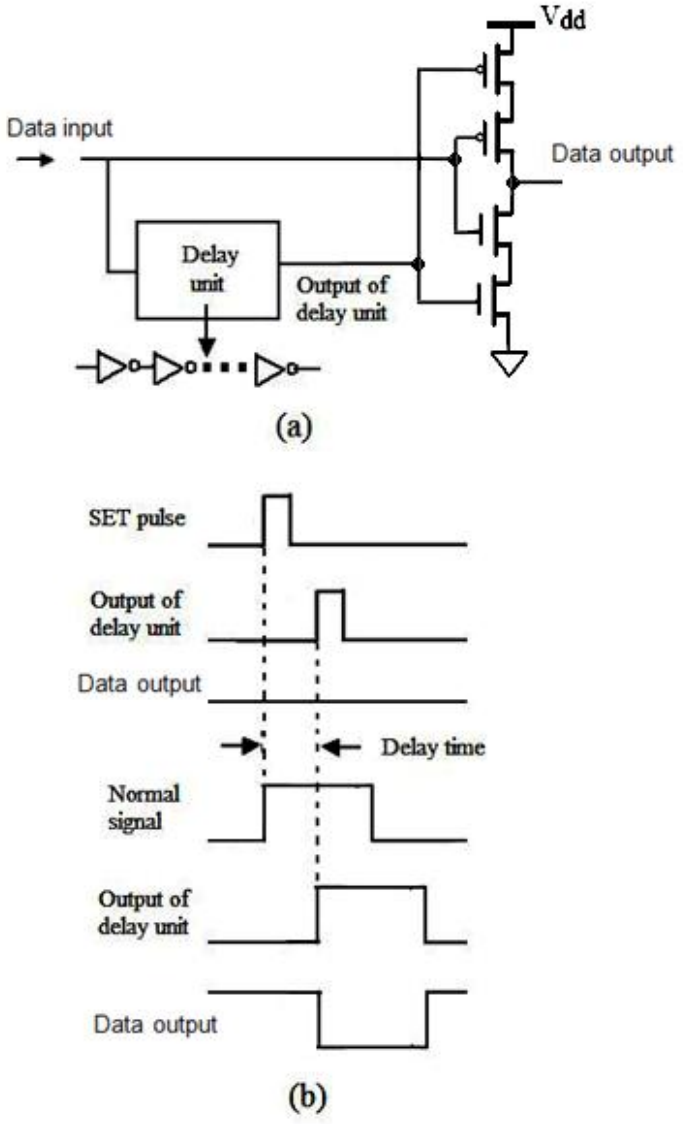


Figure 2.12 (a) Architecture of a pulse width filtering with inserted delay. (b) Waveforms of pulse width filtering with inserted delay [34].

Triple modular redundancy: TMR is a popular SET mitigation solution in the digital radiation-hardened design [24]. Fig. 2.13 illustrates the technique. Circuits and

systems are triplicated in parallel following by a voter to produce a single output. If SETs happen in any one of the three circuits or systems while the other two functions correctly, the correct logic value can be produced at the output with majority voting function. Even TMR is the most common SET mitigation method, there are some disadvantages with this solution. First, it is obvious that these three identical parallel blocks should not be placed closely in physical layout in case the charge share happens between any of the two blocks. This constraint requires more effort in the automatic placing and routing. Second, the voter does not protect itself if a SET strikes upon it. The whole system fails if the voter fails. Third, TMR method can work very well in the low frequency circuits and systems. However, glitch-induced error can happen in the high frequency circuits and systems as described in Chapter 6. Fourth, TMR approach has high power/area penalties.

Dual interlocked storage cells: DICE circuit is usually implemented in the latch which is called DICE latch [25]. Instead of a single feedback topology in the traditional latch, DICE implements a dual feedback topology to store a bit to improve SEU immunity. As shown in Fig. 2.14, at the rising edge of the clock, complementary data are stored in the drains of M_2 and M_4, respectively. Their redundant partners are also stored in the drain of M_6 and M_8, respectively. If a SEU happens at the drain of M_4 changing the logic of this node from 1 to 0, this abrupt change turns on the M_5 and makes logic competition between M_5 and M_6. Because both of M_5 and M_6 are turned on, the logic of output depends on the drivability of M_5 and M_6. The worst situation is that the logic of the drain of M_6 charges from 0 to 1. However, the logic change at the nodes of the drains of M_4 and M_6 will not affect the logic at the drain of M_2 and M_8 since both of these nodes are in the floating state. This mitigation approach introduces the area and speed penalty while improves SEU immunity.

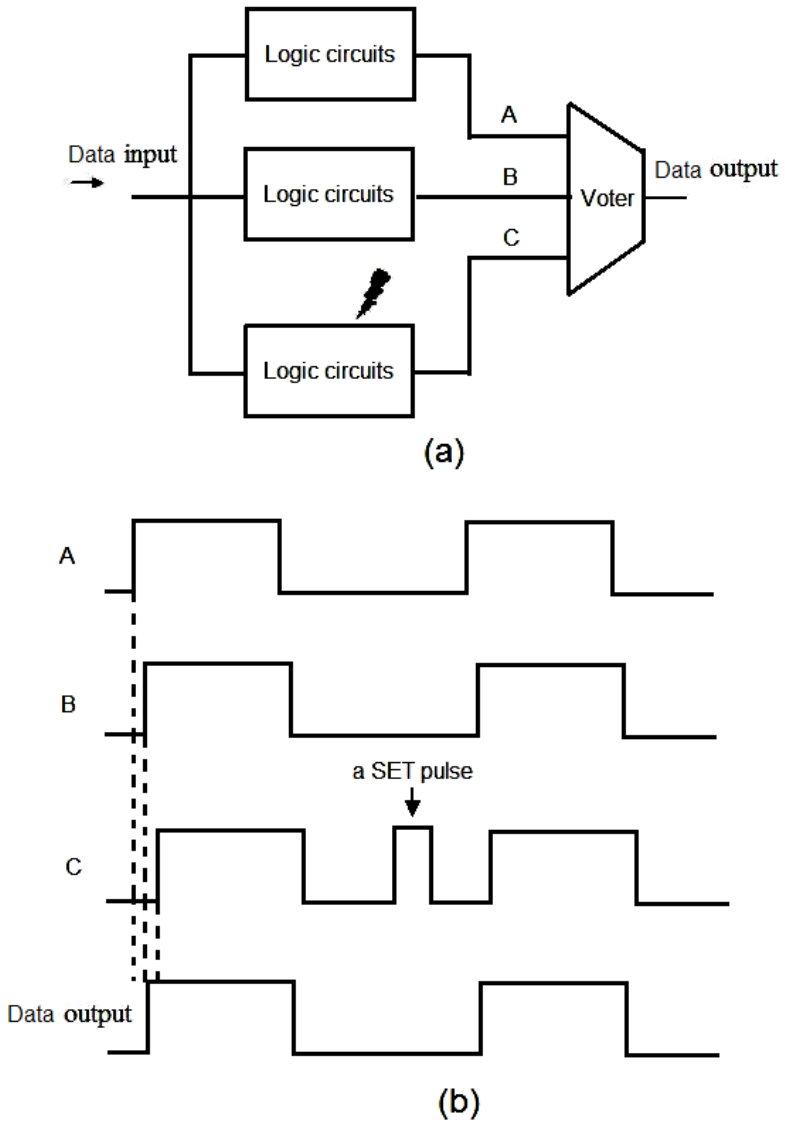


Figure 2.13 (a) Diagram of the TMR technique. (b) Waveforms of the TMR under a SET pulse propagation.

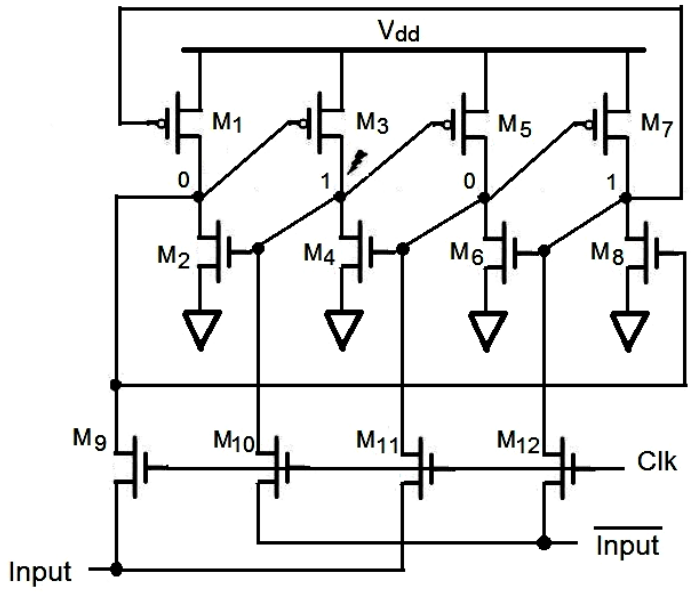


Figure 2.14 Schematic of DICE latch circuit [25].

2.4 SETs on CMOS Analog Circuits

With the development of semiconductor technologies and EDA tools, more circuit and system functions can be efficiently implemented in the silicon in digital domain. In the modern digital ICs design, millions and billions transistors are integrated on the same substrate to execute complicated functions and operations such as memory and data processing. However, analog circuits are still playing an important and indispensable role in today's ICs design. Almost all of interface circuits are composed by analog and mixed signal circuits. The reasons are presented in the following:

First, signals are eventually processed by computational system such as digital signal processing (DSP). However, the amplitudes of most nature signals are too small which can be a few microvolts to be digitized directly. In this way, amplifiers or automatic gain controllers (AGCs) are required to amplify these signals before processed

by the ADCs. Also, in order to get a “cleaned” digitized signal, filters are introduced to get rid of the out-of-band undesired signals. Furthermore, ADCs themselves are also typical analog circuit. Fig. 2.15 shows this front-end block.

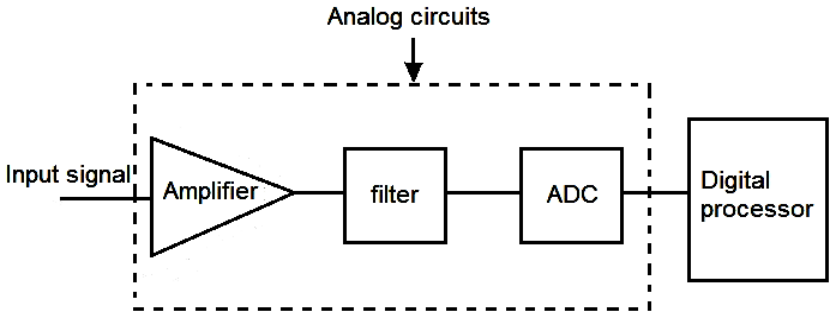


Figure 2.15 An architecture of signal digitization.

Second, analog circuits are extensively used in the front-end design in high speed data link applications as shown in Fig. 2.16. The channel is typically a cable or a printed circuit board (PCB) trace through which signals propagate from the transmitter to the receiver. The channel is the origin of many voltage noise and timing noise sources which impose a challenging design constraint in high speed circuit design. Voltage noise directly reduces voltage margins. To simplify the analysis, a transmission line can be modeled as a simple RC low-pass filter as shown in Fig. 2.17 (a). For a periodic square wave, a low-pass filter attenuates the high-frequency components, yielding finite rise and fall times, shown in Fig. 2.17 (b). But for a random digital signal, as illustrated in Fig. 2.17 (c), for a single one followed by a zero, the output does not come close to V_o. In this way, the output voltage level corresponding to ones and zeros varies with time, making it difficult to define a decision threshold. This phenomenon is due to the inter symbol

interference (ISI). The narrower the bandwidth, the larger the value of R and C, the longer the signal tails and the greater the ISI.

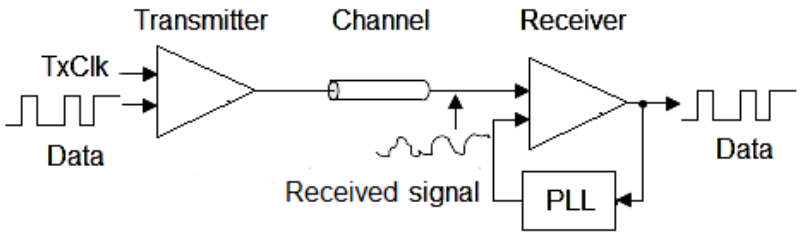


Figure 2.16 Diagram of a data link.

Other voltage noise sources come from the signal reflection, cross-talk, etc. Timing errors shift the transition edges of the received signals relative to the transition edges of the clock and reduce the timing margin. Fig. 2.18 (a) shows an ideal data sampling case in which the sampling point is right in the middle of a bit time. The timing margin is half of the bit time. However, in reality, as shown in Fig. 2.18 (b), the timing margin is reduced because jitter is introduced in the transmitted signal as well as the clock. With these effects, the input signals at the receiver are distorted in such a way that the transmitted data cannot be restored at the receiver side. So how to correct these problems is the heart of analog circuit design in the high speed data link applications. Normally, the analog blocks of the impedance matching, the signal driver, the pre-emphasizer, the post-equalizer, the PLL, the VCO, the CDR, and the sample and hold circuit are necessary functional blocks in the front-end of high speed data link designs. Quality of these analog circuits directly affects system performance. Analog circuits are

also extensively used in frequency synthesizer, front-end of the RF transceiver, power management, etc.

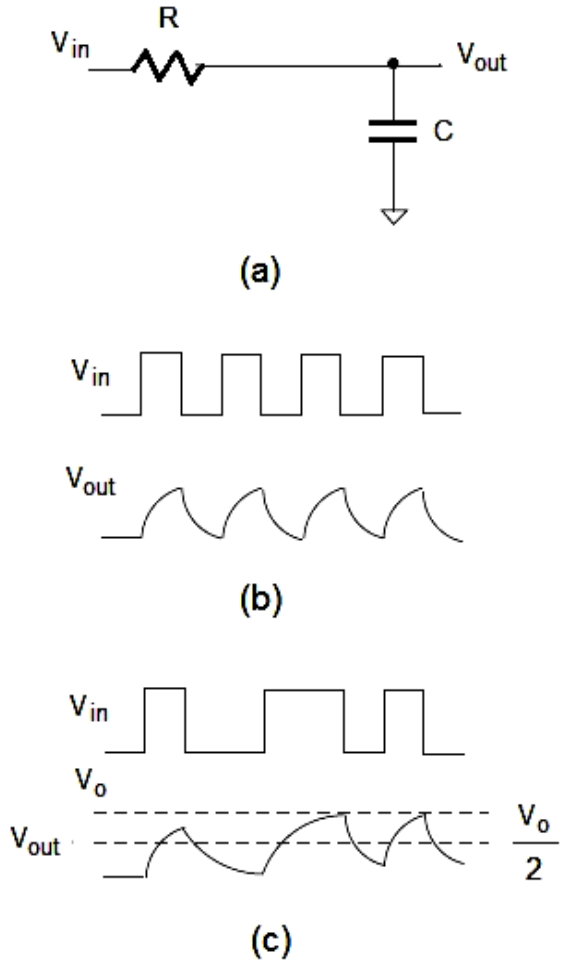


Figure 2.17 (a) RC model of transmission lines. (b) Periodic data response. (c) Random data response.

In analog circuits, SET is the most troublesome SEE that needs to be mitigated [34]. Unlike SETs in digital circuits in which SET-induced pulses need to surpass the gate threshold to propagate, a small SET-induced pulse can cause significant circuit degradation in analog circuits. A typical analog circuit is the current-mirror shown in

Fig .2.19. The current-mirror is a simple but very popular circuit to generate a bias current independent of voltage variations in analog circuits. Normally, an accurate bias current is critical for analog circuits because it directly affects many important performances such as voltage gain, bandwidth, voltage swing, and noise. In Fig. 2.19, the output current, I_{out}, is given by

$$I_{out} = \frac{W_2}{W_1} * I_{in} \tag{2.1}$$

where W_1 and W_2 is width of M_1 and M_2, respectively, I_{in} is the current flowing through M_1.

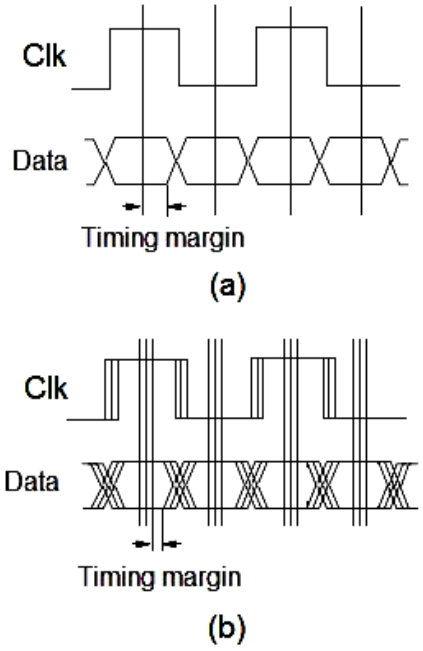


Figure 2.18 Phase noise and timing jitter. (a) Ideal case. (b) Practical case.

Channel length modulation is neglected in this equation. Normally, the lengths of two transistors are the same so as to minimize errors due to the side-diffusion of the source and drain areas. In the radiation environments, the current through M_1 changes

when a high energy ion strikes the sensitive node of M_1 and results in a change of I_{out} by the multiplication ratio. Usually, the multiplication ratio is from 3 to 10 in order to decrease the current variation [34]. In this case, the change of I_{out} degrades circuit performances such as gain, voltage swing, noise, common-mode rejection ratio, etc.

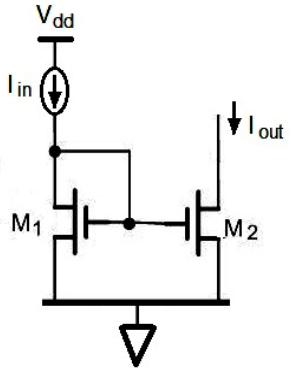


Figure 2.19 An nMOS-based current-mirror.

The other example is a differential pair amplifier. Differential architecture is extensively used in analog circuit design for the benefits of noise rejection, high linearity, and high voltage swing. As shown in Fig. 2.20, $M_{1,2}$ are the two input transistors. With a certain bias gate voltage, M_3 provides bias current determining the static operation point for $M_{1,2}$. $M_{4,5}$ work as an active load to transfer the current to output voltage. In the normal operation, the output voltage is given by

$$V_{o1} - V_{o2} = -g_{m1,2} * (r_{1,2} // r_{4,5}) * (V_{in1} - V_{in2}) \qquad (2.2)$$

where $g_{m1,2}$ are the transconductances of $M_{1,2}$, $r_{1,2}$ and $r_{4,5}$ are output resistances of $M_{1,2}$ and $M_{4,5}$, respectively. If a high energy ion strikes the sensitive node, such as the drain of M_1 or M_2, the output voltage is

$$V_{o1} - V_{o2} = -g_{m1,2} * (r_{1,2} // r_{4,5}) * (V_{in1} - V_{in2}) \pm \Delta V \qquad (2.3)$$

where ΔV is the SET-induced voltage drop at the output. "±" depends on the high energy ion striking at the drain of M_1 or M_2. If the high energy ion strikes at the drain of M_3, ideally, due to the characteristic of common-mode rejection of differential pair, the currents flow through the M_1 and M_2 are kept constant. So does the output voltage. However, the output resistance of M_3 cannot be ignored due to the short channel modulation effect. In this way, the SET-induced voltage drop at the drain of M_3 will affect the circuit performance. The gain of amplifier is changed which is given by

$$A_V = -\frac{r_{4,5} / 2}{1 / 2g_{m1,2} + r_3} \qquad (2.4)$$

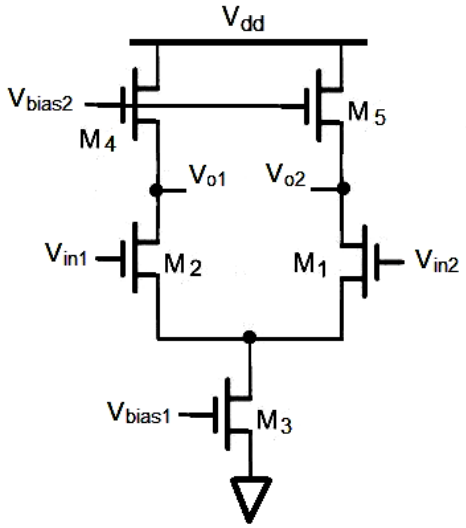


Figure 2.20 A differential pair amplifier.

Other effects on the differential pair amplifier include shift of the static operating point, degradation of the output voltage swing, and disturbance of the following stage.

The analog circuits studied in this dissertation are op amps, dynamic comparators, LC-tank oscillators, and PLLs. The motivation of the selection was discussed in Chapter 1. The detailed analyses of circuit operations and SET effects on these circuits are presented in the following chapters. Brief introductions of these circuits are described in the following:

Operational amplifier: The op amp is a versatile functional block used in almost every analog and mixed signal systems. It can be used to construct a simple application such as instrumentation amplifier, voltage regulator or relative large circuits and systems such as active high-order filter, switch capacitor circuits, and band gap reference circuits. Op amp amplifies the differential input signals with the voltage gain up to 10^5 while a general single stage amplifier has only tens of voltage gain. Because this huge voltage gain drives the op amp into a nonlinear region even with a small input signal voltage, op amp is usually employed in a feedback system. In this case, its high voltage gain only decides the precision and linearity of the closed-loop circuit.

Comparator: Similar to op amps, comparators take a tiny differential input voltage and generate a logic level output. However, the comparators usually work synchronously with a clock signal. At the rising edge or falling edge of the clock signal, logic signal can be generated at the output. Comparators are generally used in ADC and front-end of the receiver in high-speed data link applications.

Voltage-controlled oscillator: Oscillators are necessary in almost all of analog circuits and systems. For example, signals need to be sampled by the clock to perform analog to digital conversion. Also in data communications, all of the transmitted and received signals are synchronized by the clocks. However, most applications require a tunable oscillation frequency such as in a RF transceiver. Normally, the output frequency

is a function of input control voltage in the VCOs. Using a control voltage, variable output frequency of an oscillator can be generated.

Phase-locked loop: In the VCOs, many factors such as noise, temperature, power supply fluctuation, and ground bouncing can introduce jitter in the oscillation signals, therefore they will cause the shift of the frequency and phase of the oscillation signals. A mechanism must be introduced to generate an accurate output frequency and also correct the frequency shift automatically. PLL is a particular system which can perform this function. With a low frequency reference signal, PLLs can synchronize their output signals with this reference signal in frequency as well as in phase by a negative feedback topology. In this way, the frequency variation cannot be accumulated and a "clean" oscillation signal can be generated.

2.5 Pulsed-Laser Testing

In order to validate radiation-hardening techniques for mitigating the radiation effects on ICs, it is typically done by exposing the ICs to high energy particles from a particle accelerator [51]. This method can simulate the space radiation environment well with the high cost of equipment and time. In order to satisfy the requirement of a cost-effective test solution, aerospace industry utilizes pulsed-laser to simulate the effects of energetic particles on microelectronic circuits. The first published report in using a pulsed-laser to simulate the effects of the cosmic ray induced radiation on microelectronic devices can be traced back to 1965 [52]. By the mid-1980s, researchers from a number of different laboratories such as Naval Weapons Center, Naval Research Laboratory, and the Jet Propulsion Laboratory have begun to investigate the potential of

the pulsed-laser for simulating SEs in microelectronic devices. Pulsed-laser has been proven to be an effective method to simulate the transient effects of energetic particles striking microelectronic devices [53] [54]. These reports show excellent agreement between SET pulse shapes generated by the laser beam and by the heavy ions. Today, laser-based testing of ICs for SETs has gained widespread acceptance in the radiation effects research community as a useful testing method.

In the pulsed-laser testing, the energy of a photon depends on the wavelength of the laser. If the energy of a photon is larger than the bandgap[1] of the semiconductor material such as silicon, electron-hole pairs will be generated. The interaction of both heavy ions and pulsed-laser can generate electron-hole pairs inside the semiconductor material while both of the interaction times are much shorter than the response time of the device under test (DUT). However, the heavy ions test is suitable used in the system level radiation test rather than transistor level [51]. One reason is the particle accelerator irradiate heavy ions on the whole chip area. It only shows whether an upset is generated or not and only indicates which chip suffers from an upset. The precise position or sensitive nodes in the transistor level cannot be located in this type of test. The second reason is that the experiment with particle accelerator is very expensive and is not easy to access. The third reason is that heavy ions are randomly generated by particle accelerators. In this testing approach, temporal information is lost. On the other hand, testing with a pulsed-laser provides several advantages in the transistor level which are not offered by heavy ions testing. The smaller testing area is achievable with a laser since the laser can be precisely positioned on the DUT. In addition, the cost of laser-based

[1] Bandgap is an energy difference between the valence band and the conduction band in insulators and semiconductors.

testing is much cheaper than that of heavy ions testing so that it is suitable for transistor level testing. Lastly, the repetition rate of the laser pulse can be set to synchronize with the clock signal of the DUT to obtain temporal information in the SETs study. This characteristic of the laser is very important for the study of SETs on dynamic comparators in Chapter 4.

One of the limitations of laser testing in ICs is that the laser cannot penetrate metal layers covering DUT. One solution is to prevent all dummy metal layers from filling on top of the DUT in the fabrication process so that the laser beam can be focused on the interested transistors. Since design rule requires a certain percentage of dummy metal coverage for each of layers, this solution is only useful for the analog chips. For digital chips, the other solution is that laser can be emitted from the back side of DUT rather than from the front. However, this solution requires that the laser beam penetrates the whole substrate before it arrives at the p/n junction region.

Fig. 2.21 shows a block diagram of a typical pulsed-laser testing setup [55]. In general, this experiment requires a pulsed-laser source where the pulse repetition rate can be controlled from a single shot to over 1MHz. The pulse duration time should be on the order of a few picoseconds, a time that is longer than the time it takes for an ion to generate charges and shorter than the response time of the DUT. Normally, the LET of the laser traverses the silicon material can be adjusted by changing either the laser wavelength or the laser pulse energy. In order to produce ionization in semiconductor materials, the wavelength of the laser must be selected to guarantee the laser beam has a certain depth of the penetration path. In the silicon structure, a few microns charge depth can generate enough electron-hole pairs for SEU due to the shallow p/n junction in advanced processes [55]. The laser wavelength is available from 400nm, the visible

spectrum, to 1000nm which close to the infrared spectrum. A laser wavelength of 800nm is used to measure laser-induced SETs at the SSSC laboratory. This wavelength has a penetration depth of about 15μm in silicon (deeper than the depth of P/N junction in advanced CMOS process) and is, therefore, well suited for simulating the effects of energetic heavy ions [55]. Also the laser wavelength and the distance between the microscope lens and the DUT determine the beam spot size and thus accurately determine SEU sensitivity locations.

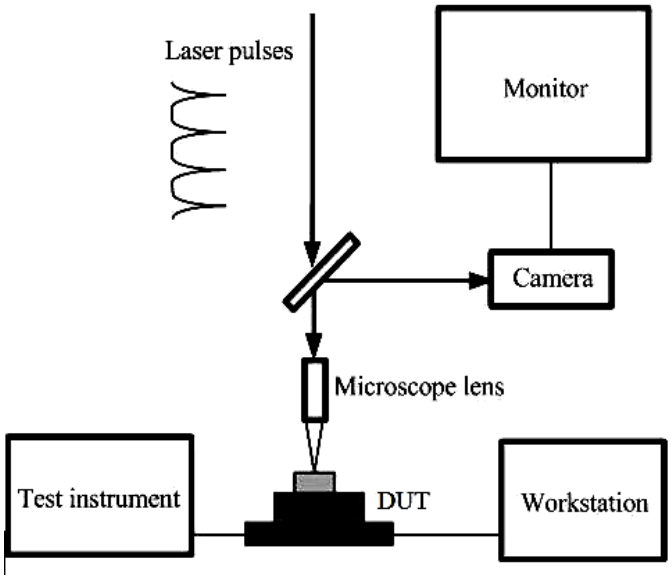


Figure 2.21 Diagram of pulsed-laser testing setup [55].

In the laser test facility, the DUT is mounted on a computer-controlled, two dimensional positioning system under a microscope. DUT can be moved with a step size of 0.1μm. The laser beam is focused on the surface of the device with the aid of a microscope. A CCD camera attached to the microscope allows investigators to observe the exact location of the laser beam on the circuit. The DUT is moved underneath the

laser beam to locate the sensitive nodes. A high-speed digital oscilloscope and spectrum analyzer are used to observe the output signals of the DUT. Fig. 2.22 shows the equipment setup for pulsed-laser testing in the SSSC. The laser pulse width is 1ps, with repetition rate of 4.75MHz. The working distance between the microscope lens and the DUT is 3mm. The testing process generally begins by scanning DUT over a large area with a maximum laser energy to identify sensitive regions. Once the laser-induced upset is captured by the measurement equipment, tightly focused small areas are scanned with the same laser energy in order to get the sensitive nodes of the circuit. Then the energy level is gradually reduced until it reaches the threshold, which is defined as the threshold laser energy to generate incorrect signal captured by the measurement equipment.

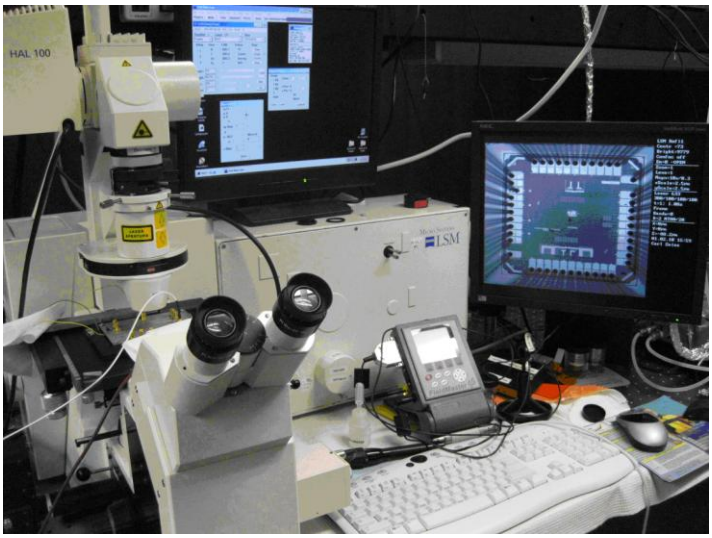


Figure 2.22 Laser and microscope setup.

3. Single-Event Transients-Tolerant Operational Amplifiers [1]

SET effects can be viewed as a random transient offset signal appearing at the input stage of an op amp due to their random and temporary natures. Therefore, offset cancellation techniques [50] can be applied in the RHBD op amp design. An important technique of offset cancellation, auto-zeroing will be introduced and applied to mitigate SETs in this chapter [50] [56] [57] [58].

3.1 Introduction to Offset and Auto-Zeroing Cancellation Technique

During the manufacturing process, none of any two transistors have identical properties such as threshold voltage (V_{th}), transistor dimension, and transistor conductively even they are assumed to have the same properties in the schematic simulation. This phenomenon is called mismatch which exists in all analog circuits, especially in differential input pair circuits such as differential amplifier, comparator, and op amp. An example is shown in Fig. 3.1 which is a typical differential amplifier [50]. Ideally, with the same input voltage, V_{in}, there should be no voltage difference at the output, V_{o1} and V_{o2}. However, due to mismatch between the two input transistors M_1 and M_2, the differential output voltage is not zero and is given by [50].

[1] The major results of this chapter were published in the IEEE 1st Microsystems and Nanoelectronics Research Conference, MNRC 2008, Oct. 2008.

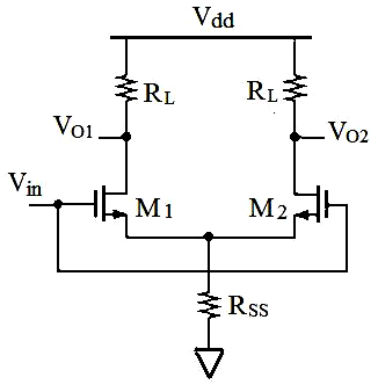


Figure 3.1 Differential pair sensing common mode input [50].

$$V_{o1} - V_{o2} = \frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2}) * R_{ss} + 1} * R_L * V_{in} \tag{3.1}$$

where g_{m1} and g_{m2} are the transconductance of the transistors M_1 and M_2, respectively, R_{ss} is the resistance of the tail current transistor, and R_L is the load resistance. In practice, it is more meaningful to specify the input-referred offset voltage, $V_{OS,in}$, which forces the output voltage to be zero as shown in Fig. 3.2 [50]. Usually, the offset limitation in multi-stage amplifiers is making the latter stages nonlinear. The other important effect of the offset in comparators and op amps is the reduction in comparative precision. For these reasons, the design of op amps, high-precision comparators, and high resolution ADCs requires offset cancellation. An important technique of the offset cancellation is auto-zeroing [50] [56] [57] [58].

The basic idea of the auto-zeroing is to sample an unwanted signal and periodically store the sampling voltage in a capacitor, and then subtract the voltage from the instantaneous value of the contaminated signal [59]. In the op amp applications, implementation with the auto-zeroing technique consists of a folded-cascode preamplifier and switched-capacitor circuits [50] [60]. An extra signal is required to make the circuit

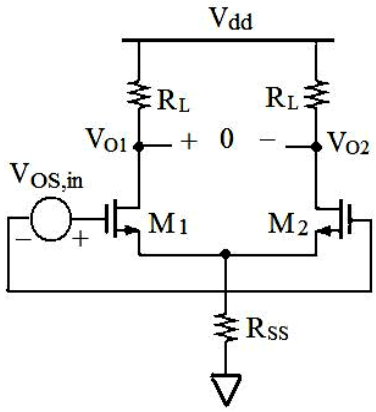


Figure 3.2 Differential pair with offset referred to the input [50].

operating in two phases: cancellation period and signal tracking period. Depending on specific application, the capacitor can be implemented either at the input, output or at the intermediate nodes between input and output of an op amp [56]. These techniques are called IOS, OOS, and AOS. With these offset cancellation techniques, the output signal is "clean" without the effect of offset. The method of the auto-zeroing technique for mitigating SETs in an op amp was provided in [61], where one of the approaches of auto-zeroing, IOS, was implemented in an op amp in order to compare with a general folded-cascode op amp in term of SET tolerance.

For the auto-zeroing op amp, two capacitors were implemented at the differential inputs to store the SET interference with negative feedback loop in the cancellation period. During the tracking period, the negative feedback loop is open and the op amp senses the difference of the input signals and generates the output signals. In this way, the SET-induced offset can be limited to one clock period. However this auto-zeroing op amp was implemented with an inverter followed by a sense amplifier, therefore the whole

design architecture was not based on the folded-cascode op amp which was used as a reference. In this chapter, three auto-zeroing architectures are to be introduced, IOS, OOS, and AOS, based on folded-cascode op amp approach. The architectures are then compared with the general folded-cascode op amp, in term of SET tolerance and other features. Only the pre-amplifier is studied in this design, the SET interaction from the rest of stages of the op amp is not included.

3.2 SET on the Folded-Cascode Op Amp

Compared to a single transistor amplifier, the cascode configuration improves amplification gain by increasing its output impedance. The cascode transistor also shields the input from the output voltage variations. These properties make cascode circuit popular in CMOS circuit design. The traditional CMOS cascode op amp is shown in Fig. 3.3. In Fig. 3.3(a), the input transistors of $M_{1,2}$ and the cascode transistors of $M_{3,4}$ are the same type which is called telescopic cascode pre-amplifier in the op amp design [50]. In Fig. 3.3(b), the input transistors of $M_{1,2}$ are pMOS and the cascode transistors of $M_{3,4}$ are nMOS which is called folded-cascode preamplifier. For both circuits, $M_{1,2}$ are differential signal input transistors which convert the input voltage to a current and apply the result to a common-gate stage of $M_{3,4}$.

A differential pair with the active current mirror $M_{7,8}$ converts a differential input to a single-ended output. It is obvious that the folded-cascode pre-amplifier need two current sources: $M_{11,12}$ combine together to be a current bias for the input stage $M_{1,2}$, and $M_{5,6}$ provide an additional current bias for the cascode stage $M_{3,4}$ while telescopic cascode pre-amplifier requires only one current source. As a result, the folded-cascode pre-

amplifier consumes more power than that of the telescopic cascode partner. On the other hand, the telescopic cascode pre-amplifier exhibits a higher gain than that of the folded-cascode pre-amplifier due to the nMOS input transistor (having higher mobility of charge carrier than that of the pMOS). Also, the folded-cascode pre-amplifier presents a smaller bandwidth compared with the telescopic cascode counterpart because of a folded pole is introduced. Even with these shortcomings, the folded-cascode pre-amplifier is more popular due to its high voltage swing and large common mode input range [50]. This study targets RHBD design on the folded-cascode pre-amplifier due to its popularity.

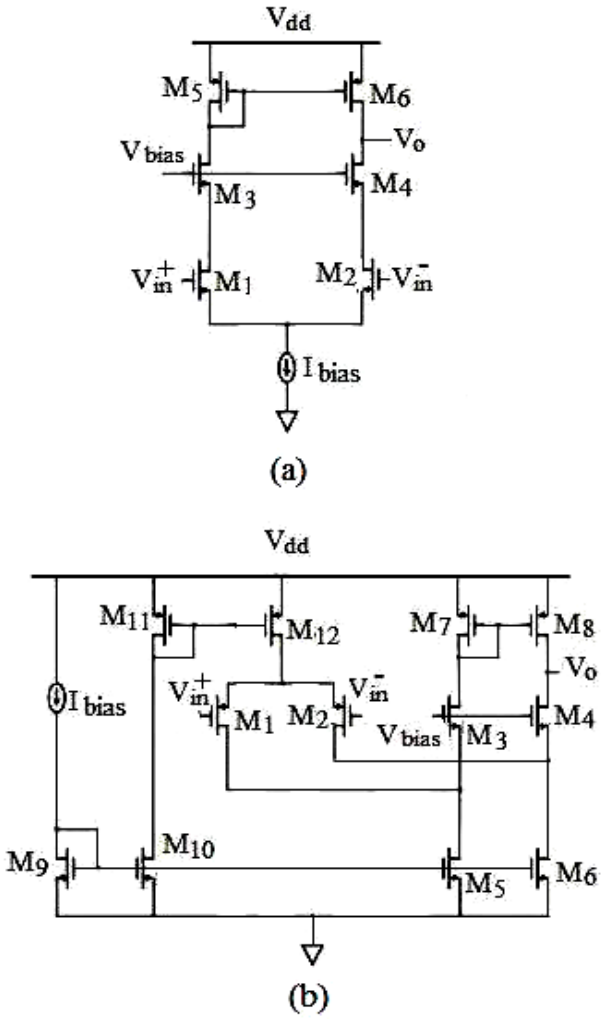


Figure 3.3 (a) A telescopic cascode op amp. (b) A folded-cascode op amp.

SET disturbances on any critical node on the circuits of folded-cascode preamplifier have a significant impact on the output voltage. This is demonstrated in Fig. 3.4, a positive current pulse with 5ns duration, 500μA magnitude, and 250ps fall/rise times is stimulated at the sources of $M_{1,2}$. Even these characteristics of this current pulse are not reasonable parameters in real SET-induced pulse, these parameter are quoted in [61] for comparison purposes only since they are not close to the real SET-induced pulse. As shown in the diagram, a significant error happens at the output when the pulse strikes on the differential input transistors.

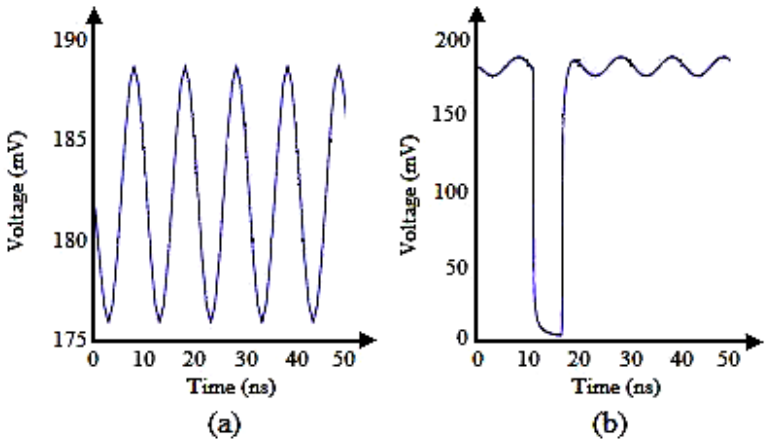


Figure 3.4 (a) Simulated output voltage of the folded-cascode pre-amplifier without SET interaction. (b) Simulated output voltage of the folded-cascode pre-amplifier with SET interaction.

3.3 Folded-Cascode Op Amp RHBD Design with Input Offset Storage

The designed circuit of the folded-cascode op amp with IOS is shown in Fig. 3.5. Transistors M_{1-8} form a folded-cascode pre-amplifier. Voltage source of V_{bias1} provides

the voltage bias for $M_{1,2}$ via two large resistors of $R_{1,2}$ which isolate the voltage source from the signal path. The auto-zeroing process requires two phases using a non-overlap clock signal to control the switches SW_{1-6}. During the cancellation period, the amplifier is disconnected from the signal path by turning $SW_{1,4}$ off, and the inputs are set to a common-mode voltage of V_{CM}. With $SW_{2,3}$ and $SW_{5,6}$ on, a unity-gain feedback loop is established.

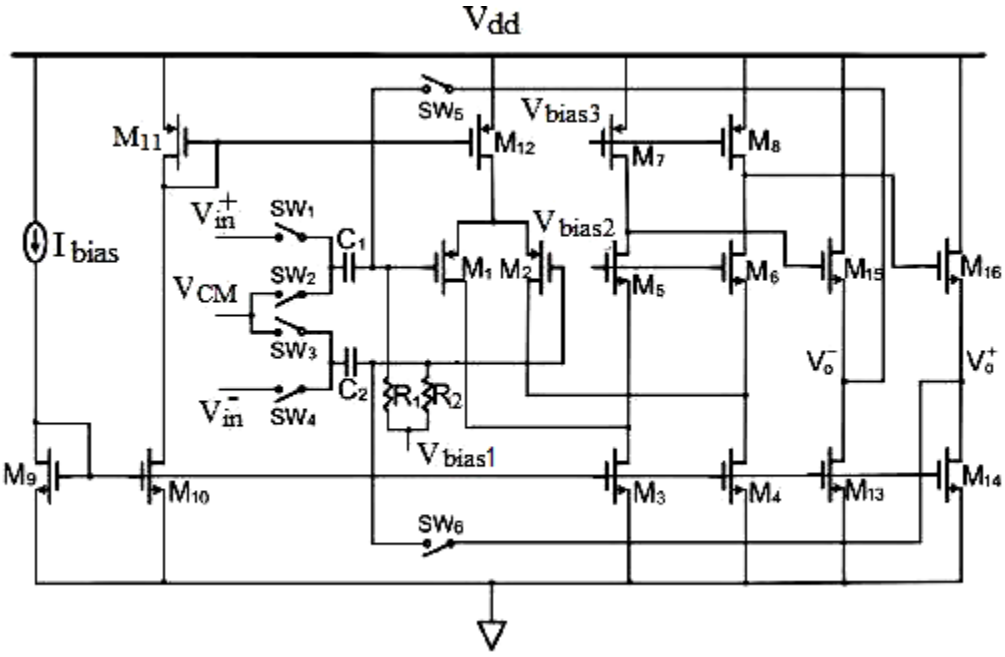


Figure 3.5 An input offset storage folded-cascode op amp.

The differential source follower consists of M_{13-16}. Since there is a feedback loop with switches $SW_{5,6}$, the common-mode voltage of the output can be tuned by the size of $M_{13,14}$ to get a common-mode voltage as the same as the V_{bias1} at the inputs. If the SET interaction happens during this time, with unity-gain feedback, the residual error voltage at the output will be

$$V_{o.error} = \frac{V_{in.error} * A}{1 + A} \tag{3.2}$$

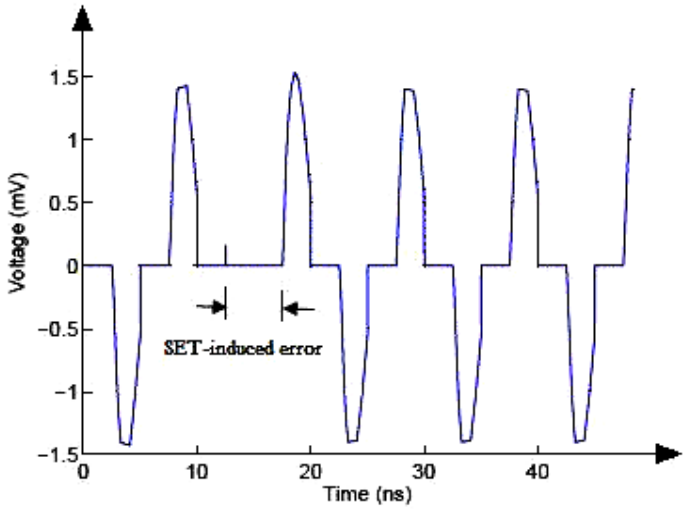


Figure 3.6 Differential output voltage with input offset storage folded-cascode op amp under a SET interaction.

where $V_{o.error}$ is the error voltage during the cancellation period, which is stored in capacitors $C_{1,2}$, $V_{in.error}$ is the input error voltage, and A is the gain of the pre-amplifier. Therefore, with SET cancellation, the pre-amplifier output is approximately equal to $V_{in.error}$, otherwise, the pre-amplifier output is A × $V_{in.error}$. During the tracking period, $SW_{2–3}$ and $SW_{5–6}$ are off, while $SW_{1,4}$ are on. The feedback loop is open. At this time, this error output remains the same and will be cancelled by subtracting it from the amplified input signal which contains the $V_{in.error}$ according to:

$$V_{out} = (\Delta V_{in} + \frac{A * V_{in.error}}{1 + A} - V_{in.error}) * (-A) \tag{3.3}$$

$$V_{out} \approx -\Delta V_{in} * A \tag{3.4}$$

It shows that the SET-induced input error voltage does not affect the output voltage during the tracking period. To test the SET tolerance of this circuit, the current impulse with the same amplitude and duration stated in the last section is added at the sources of $M_{1,2}$. The simulation result of the differential output of the preamplifier using this technique is shown in Fig. 3.6. During the cancellation period, the output is approximately to zero, and the SET-induced error will not affect the output signal during the followed tracking period.

3.4 Folded-Cascode Op Amp RHBD Design with Output Offset Storage

The technique of OOS stores the output error voltage in the capacitors $C_{1,2}$ which are in series with the pre-amplifier output as shown in Fig. 3.7. During the cancellation period, switches $SW_{2,3,5,6}$ are on, and $SW_{1,4}$ are off. The SET interaction happens in this time is amplified and stored in $C_{1,2}$. Voltage of $A \times V_{in.error}$ is stored in the equivalent series capacitance of C_1 and C_2 during this period. In the tracking period, $SW_{1,4}$ are on, and $SW_{2,3,5,6}$ are off. The pre-amplifier senses and amplifies the input difference and generates a voltage at the output which is given by

$$V_{out} = \Delta V_{in} + \frac{A*V_{in.error}}{2} - \frac{A*V_{in.error}}{2} = \Delta V_{in} \tag{3.5}$$

Two capacitors are assumed exactly the same in the OOS implementation. The difference between IOS and OOS is that they are applied in the different gain environments. For example, since the pre-amplifiers with OOS are open loop, it is typically used in low gain pre-amplifiers.

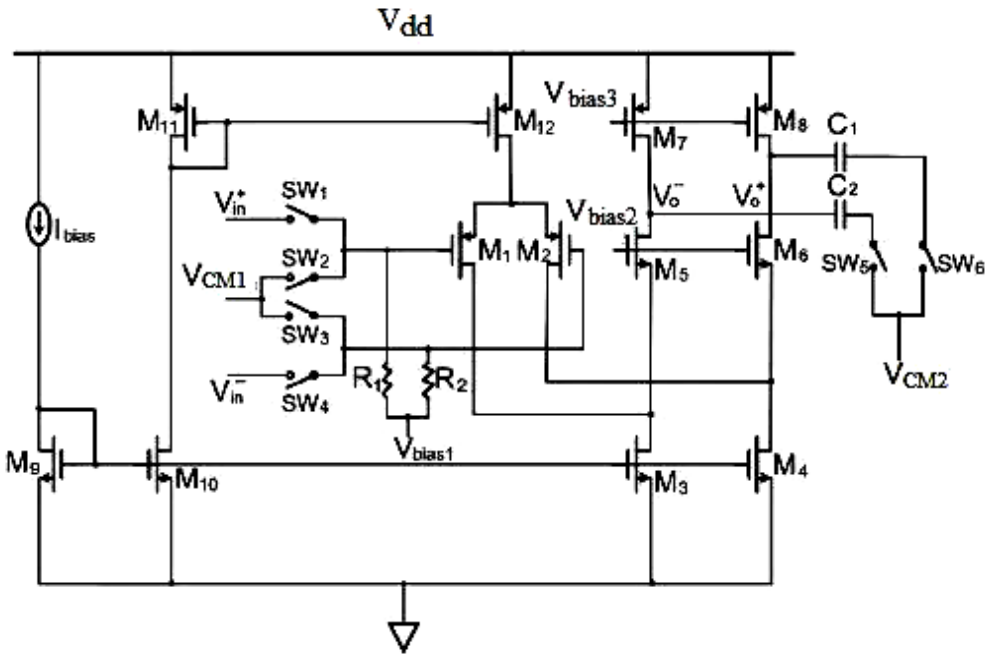


Figure 3.7 An output offset storage folded-cascode op amp.

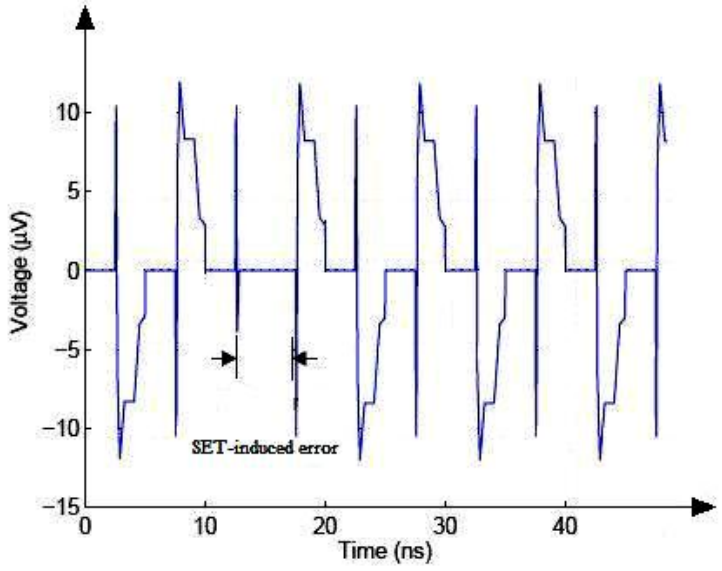


Figure 3.8 Differential output voltage with output offset storage folded-cascode op amp under a SET interaction.

The simulation result of differential output of the pre-amplifier with this technique is shown in Fig. 3.8. Similar to the case of IOS, the duration of SET effects at the output are shorter than the cancellation period. The voltage swing at the output is smaller than that of IOS due to the lower gain of the pre-amplifier in the OOS technique than that of the IOS.

3.5 Folded-Cascode Op Amp RHBD Design with Auxiliary Offset Storage

The general drawback of the two approaches above is that the introduction of capacitors in the signal path, signal speed and bandwidth, particularly serious issues in op amps and feedback systems will be affected [50] [58]. To resolve this problem, a cancellation scheme isolates the capacitors from the signal path through the use of an auxiliary amplifier is shown in Fig. 3.9. An auxiliary amplifier consists of M_{13-15} is added in the feedback loop. During the cancellation period, the SET interruption at the input of the pre-amplifier is amplified by A_1, the gain of the pre-amplifier, and stored in $C_{1,2}$. The $V_{o.error}$ drops by a factor approximately equal to the loop gain which is

$$V_{o.error} = \frac{V_{in.error} * A_1}{A_{aux}} \tag{3.6}$$

Simulation result of the differential output of the pre-amplifier using this technique is shown in Fig. 3.10. The duration of SET effects at the output are also shorter than the cancellation period. The bandwidth of this circuit is obviously larger than that of the IOS and the OOS.

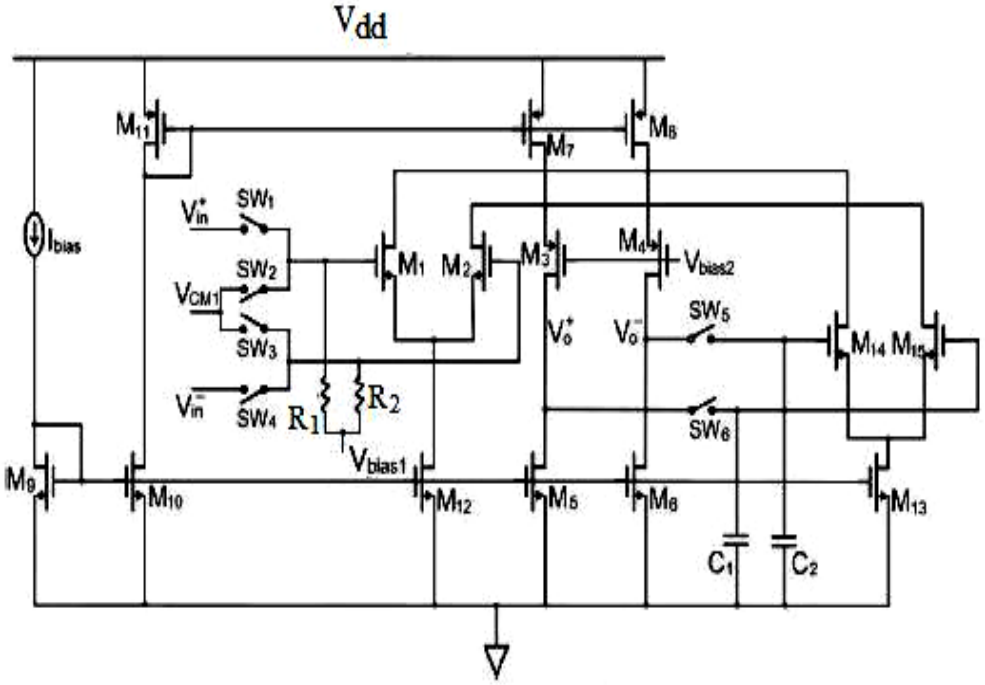


Figure 3.9 An auxiliary offset storage folded-cascode op amp.

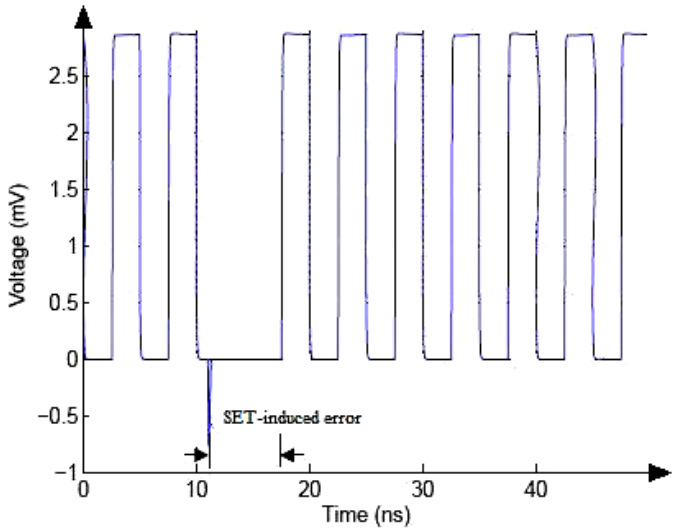


Figure 3.10 Differential output voltage with auxiliary offset storage folded-cascode op amp under a SET interaction.

3.6 Summary

Three approaches of the SET auto-zeroing cancellation techniques are presented and implemented in the op amp. Simulation results with a current pulse striking at critical circuit nodes indicates that the duration of SET effects is not longer than the cancellation period. The techniques can also be extended to ADCs to mitigate SET-induced errors.

4. Single-Event Transients Effects on Dynamic Comparators in the 90nm CMOS Triple-Well and Dual-Well Technology [1]

Comparators are commonly used in sampling circuits such as ADCs and interfacing circuits as shown in Fig. 4.1 [57]. Dynamic comparators are usually not used in aerospace and military applications. However due to their fast speed and low power consumption, dynamic comparators can be considered for space and military applications if its performance criteria can be met by using RHBD approaches. Studies have been done to evaluate their performances under SET effects and mitigation techniques have been introduced [61] [62]. Traditionally, circuits in triple-well process technology are more SET tolerant than those are in dual-well. However this may not be the case for the advanced nanometer CMOS technologies. In this chapter, comparators are designed and fabricated with dual-well and triple-well technologies using a CMOS 90nm process, respectively, to investigate their SET performances.

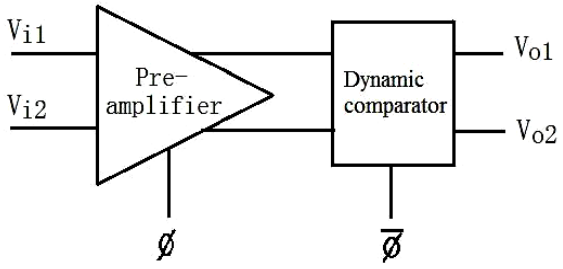


Figure 4.1 A simple comparator architecture.

[1] The major results of this chapter were published in the IEEE Transactions on Nuclear Science, vol. 56, Dec. 2009.

4.1 Dual–Well and Triple–Well Process Technology

For the dual-well technology, all the nMOS transistors are placed in the p-type substrate. For the triple-well technology, all the nMOS transistors are placed in the isolated p-well inside the deep n-well, with the cross-section view shown in Fig. 4.2. The process and mask flow for this fabrication process is described in [63]. For the advanced CMOS processes used for manufacturing space and military electronic circuits, the use of triple-well technology electrically isolates the nMOS transistors from the p-type substrate. Additionally, the presence of the triple-well mitigates substrate-noise coupling in analog RF and mixed signal circuits. The additional junction capacitances in triple-well structures have been used to obtain lower drain bulk series capacitance than dual-well structures in low noise amplifiers [64]. Triple-well technology also allows reverse-biasing of p-well to reduce the leakage currents (I_{off}) induced by TID effects [65]. This approach has been used effectively in limiting up to 1-2Mrad total dose exposure for SRAM designs in 130nm and 90nm CMOS technologies [66].

The use of triple-well technology may alleviate the above mentioned issues, but its effect on single-event vulnerability is still unclear. Triple-well technology was reported to be beneficial to mitigating SET effects [67]. However recent reports indicated that triple-well technologies in the advanced CMOS processes could increase SET effects: larger FIT rate for alpha testing in the 150nm CMOS technology [63] and increased SER for alpha and neutron testing on 65nm SRAMs [68]. A 3-D TCAD simulation study [42] showed that triple-well devices may collect more charges during a single-event strike compared to dual-well devices in 90nm CMOS technology, and therefore increase the single-event pulse width. Previous work in this regard has always been performed using

simulations or data from either dual-well or triple-well technology, but not from both. In this chapter, for the first time, both of the circuit simulations and laser experiments on a fabricated integrated circuit on a single die using triple-well and dual-well structures in a 90nm CMOS process are presented.

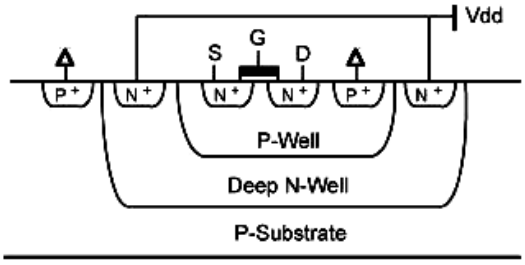


Figure 4.2 Cross-section view of a nMOS transistor implemented with triple-well CMOS technology.

4.2 Dynamic Comparator Circuit

Comparator topologies have been classified as static latched comparators, class AB latched comparators, and dynamic comparators, as reviewed in [69]. Of these topologies, dynamic comparators are considered in this work. Dynamic comparators are usually not considered for space and military applications due to the presence of floating nodes sometime during the clock cycle. However, dynamic comparator is faster and consumes less power as compared to its static counterpart and needs to be evaluated for SE performance. Such designs may be favored for future space and military applications if the performance criteria can be met by using RHBD approaches. Schematic diagram of the designed dynamic comparator is shown in Fig. 4.3. The basic mechanism is that when the clock is at the rising edge, the comparator senses the voltage differences between the two inputs and sets the outputs to low and high respectively. The input voltage difference

can be very small depending on the input offset voltage introducing by the mismatch issue. However, the output voltage should be a full swing voltage. Specifically, when the clock is low, the outputs v_o^+, v_o^-, and the nodes N_1 and N_2 are pulled high by the pMOS transistors M_{8-11}. At this time M_3 is off and the comparator is in the idle state. During the regeneration in the evaluation period (the clock is high), M_{8-11} are switched off, and M_3 is switched on. Depending on the differences in the input voltages, one branch of the cross-couple inverters M_{4-7} allows more current flow than that of the other side. With positive feedback, the final output state is determined. When the regeneration finishes, one of the output voltages is high while the other is low. The power efficiency is maximized since at this time, no current flows through either branches of the cross-couple inverter. If v_o^+ is high while v_o^- is low, $M_{4,7}$ are switched on while $M_{5,6}$ are switched off, and vice versa. M_3 is forced into the deep triode region and no current flow through it.

For the dual-well technology, all the nMOS transistors are placed in the p-type substrate. For the triple-well technology, all the nMOS transistors are placed in the isolated p-well inside the deep n-well, with the cross-section view as shown in Fig. 4.2. Enclosed-geometry layout has been well-known for total dose mitigation [38]. Therefore, all the transistors were designed using closed-geometry layout as shown in Fig. 4.4. The W/L ratio of the basic transistor used was 4μm/0.19μm. The transistor is surrounded by a guard ring. For the transistors requiring larger width, multiple transistors are connected in parallel. The sizes of the transistors used in the circuit are listed in Table 4-1. Fig. 4.5 shows the basic layout used for dual-well and triple-well designs, while Fig. 4.6 shows the actual photo of the die under a microscope. Additional layout considerations were carried out to avoid placement of the metal fill over the transistors so as to facilitate laser testing from the top of the die.

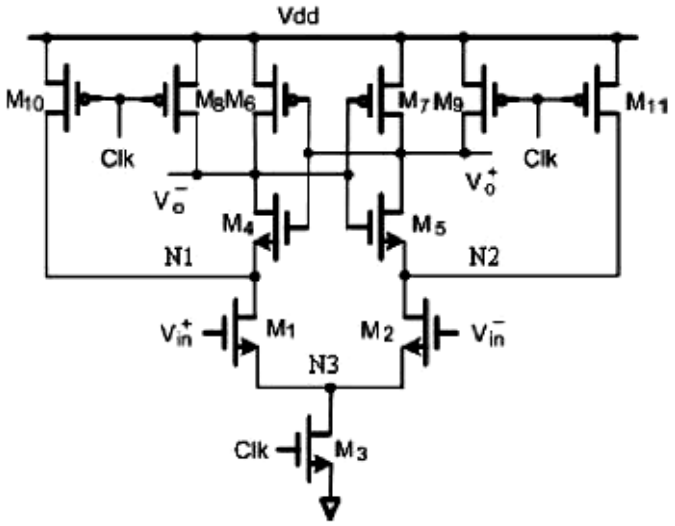


Figure 4.3 Schematic diagram of a dynamic comparator.

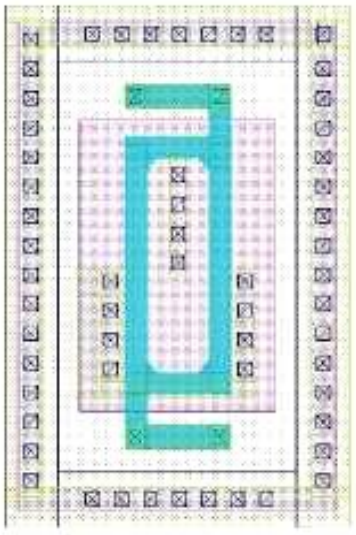


Figure 4.4 A basic transistor implemented with closed-geometry.

Table 4-1 Transistors size of the comparator.

Transistors	Width (µm)	Length (µm)
$M_{1,2}$	16	0.19
M_3	8	0.19
$M_{4,5}$	16	0.19
$M_{6,7}$	16	0.19
$M_{8,10}$	4	0.19
$M_{9,11}$	4	0.19

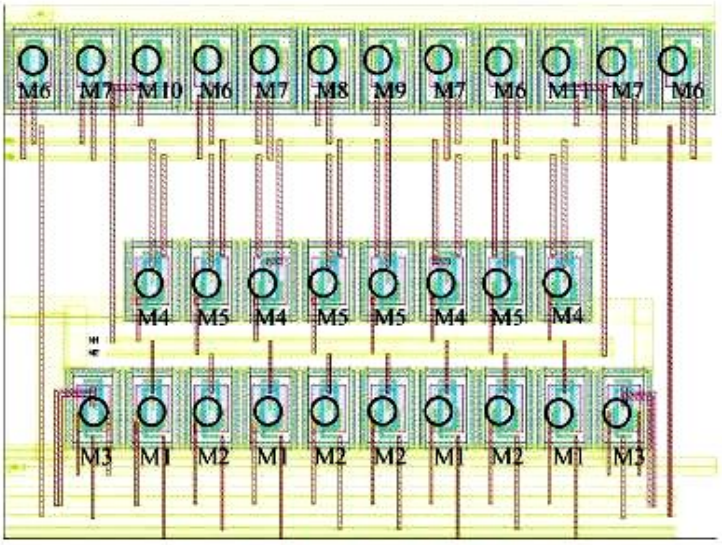


Figure 4.5 Layout of the dynamic comparator. Transistors in the first row from the top are pMOS transistors, the second and third rows are nMOS transistors. The circles on the transistors are laser hit locations.

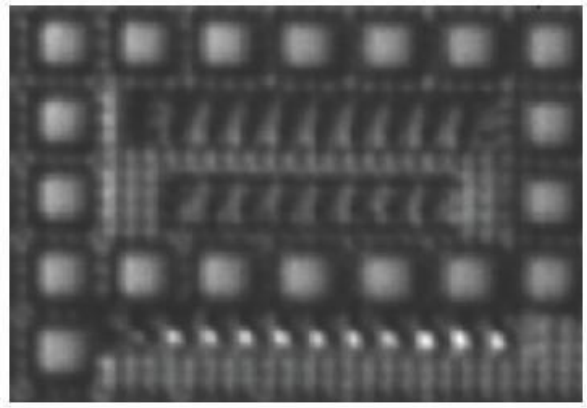


Figure 4.6 Photograph of the comparators. The large bright square blocks around the comparator are the filling tile layers from Poly to Metal 7. There is no filling layer on top of the comparator.

4.3 Experimental Results

The comparators were designed using Cadence and Mentor Graphics tools with device models obtained from STMicroelectronics (STM) CMOS 90nm design kit. The design was fabricated by Circuits Multi-Projects, France (CMP). The fabricated chip was verified with bench tests and the results showed a fully functioned comparator circuit operation. The chip package has a window on the top of the die, which is covered by a removable lid. It was removed when the laser experiments were performed. During the laser experiments, one input signal was a fixed DC reference voltage while the other was a continuous sinusoidal signal. The outputs of the comparators were connected to the probes of a high speed oscilloscope through an on-chip buffer to observe the SET pulses. Fig. 4.7 shows SET pulses generated by the pulsed-laser beam on the screen of a DSA90254A Digital Signal Analyzer which has 2.5GHz bandwidth and 20GSa/s.

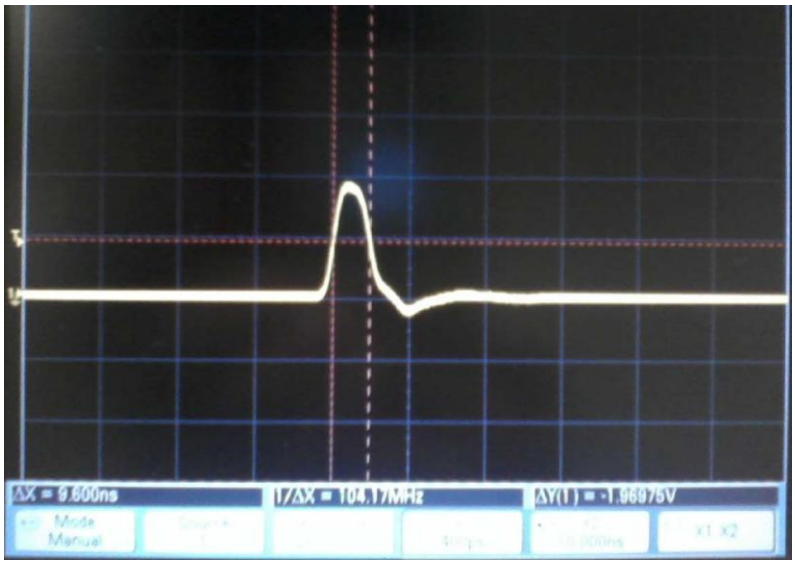


Figure 4.7 Photograph of the SET pulse at the output of the dual-well comparator. The grid for x-axis is 1ns, for y-axis is 0.5V.

The pulsed-laser beams were targeted on the drain of various transistors as marked in Fig. 4.5. First, the maximum laser energy was used to generate the SET pulses at the outputs. Then the energy level was gradually reduced until it reached a threshold which is defined as the lowest laser energy to generate incorrect voltage at the comparator output. The comparator output is latched at each clock cycle so as to clearly define the upset. The energy level was recorded as the threshold of energy required to generate the upset. The transistors hit by the laser beams were M_1, M_2, M_4, M_5, M_6, M_7, and M_3 for the two comparators which were fabricated with dual-well process and triple-well process, respectively. The SET pulses at the output pads of the comparator chip were observed on a high-speed oscilloscope. Table 4-2 lists the minimum laser pulse energy needed for the selected transistors of both comparators to generate upset at the output. The transistor pairs $M_{1,2}$, $M_{4,5}$, $M_{6,7}$ showed the same energy threshold.

Table 4-2 Threshold laser pulse energy of the transistors for the dual-well and triple-well comparators. Lower energy implies higher vulnerability.

	$M_{6,7}$ (nJ)	$M_{4,5}$ (nJ)	$M_{1,2}$ (nJ)	M_3 (nJ)
Dual-well comparator	145	59	59	168 (maximum energy)
Triple-well comparator	97	52	75	168 (maximum energy)

4.4 Discussions

Table 4-2 shows a SE hits on transistor M_3 did not generate SETs even at the maximum laser energy. This is easily explained by the fact that the pulse current induced by the laser beams results in the same voltage change in both branches of comparator. As the comparator only amplifies the differences of the two branches, any such increase in common voltage will not introduce any perturbation in the comparator output voltages. pMOS transistors M_6 and M_7 are built using the same structure and size for the dual-well and triple-well designs. But the threshold laser energy to cause an upset for these pMOS transistors are different (145nJ vs. 97nJ) for the two designs as shown in Table 4-2. Results showed that the dual-well design required 40% more laser energy to generate SET pulses than that for triple-well. This can be explained by the electron mobility differences of the nMOS transistors in the dual-well and triple-well designs. As the transistor physical structures (pMOS transistors are fabricated within the n-well and this physical structure is identical for dual-well and triple-well designs) and the circuit topology are identical, the charge collected is identical in both cases. However, because

of the triple-well structure for the nMOS transistors, the electron mobility for nMOS transistors is less than that for dual-well designs. This is confirmed by the experimental measurements. For identical V_{GS} and V_{DS} values, nMOS transistors for dual-well show 33% higher current than that for triple-well. As a result, the restoring current available for a p-hit is different in this case, resulting in different SET pulse characteristics, and different threshold values for laser energy for an incorrect result at the comparator output. Thus for all hits on pMOS transistors, where nMOS transistors provide the restoring current, the triple-well circuits will always be more vulnerable than the dual-well circuits for identical circuit topologies.

This can be further verified by the single-event schematic SPICE simulation performed on the dual-well and triple-well designs using Cadence Virtuoso Spectre Circuit Simulator. The simulations were carried out to identify the most vulnerable nodes using double-exponential current sources connected to the hit nodes. Even though for CMOS 90nm technology, double-exponential current pulses do not accurately represent the hit current, the simulation results can be used to compare the SE sensitivity of the nodes. The sensitivity of a node to SETs (or the critical charge for each node) is estimated as the minimum amount of charge needed to flip the outputs of the comparator in the simulated SET event. The current pulses were applied at the rising edge of the clock when the comparator was most vulnerable to SETs.

Fig. 4.8(a) shows the signal waveforms for the dual-well comparator when the current pulse was applied at the output node (v_o^+ or v_o^-), which was used to simulate the hits on the pMOS transistors, M_6 and M_7, in the laser experiments. It was shown that the output is flipped when the impulse current is increased to around 140μA. The critical charge for this node to flip is 22.4fC.

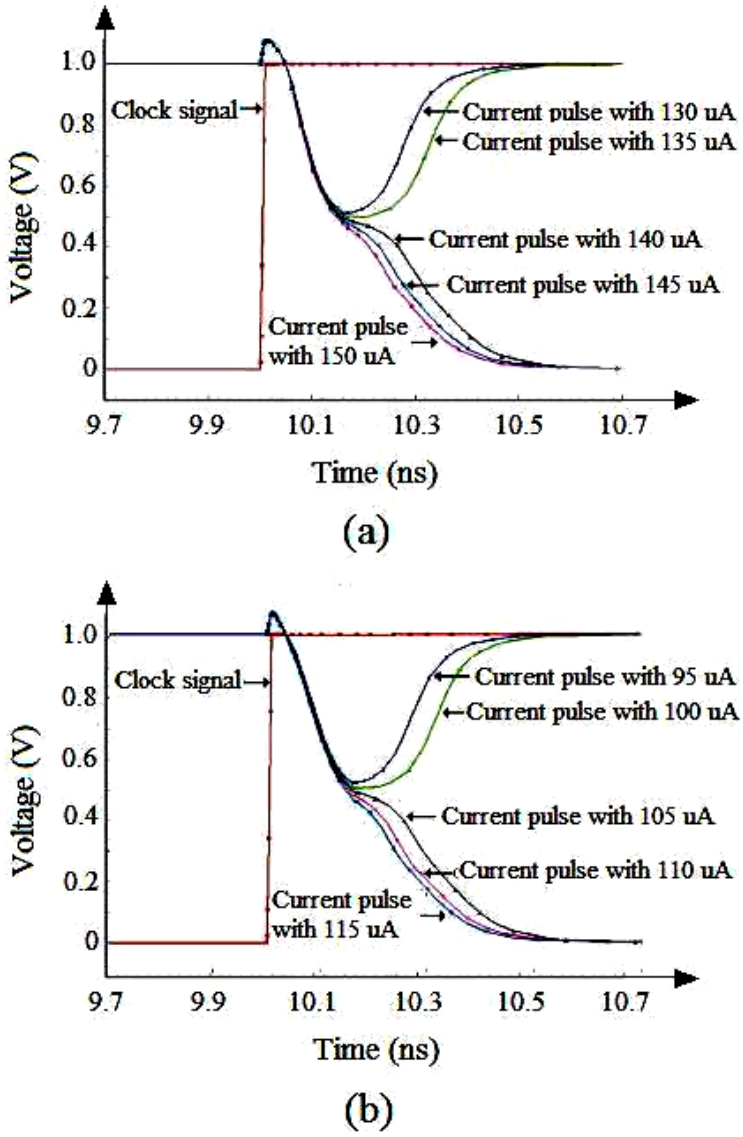


Figure 4.8 (a) Dual-well comparator output waveforms with SET current pulses from 130μA to 150μA. It shows that the SET current pulse with magnitude of 140μA generate the upset at the outputs. (b) Triple-well comparator output waveforms with SET current pulses from 95μA to 115μA. The electron mobility of nMOS transistors is 33% less than that of the dual-well transistors. It shows that SET current pulse with magnitude of 105μA generates the upset at the outputs, which is less than that of the dual-well design.

For the triple-well comparator, the electron mobility was modified purposely that the nMOS transistors in triple-well have 33% less current than that for dual-well. The same simulation procedure was followed to obtain the critical charges for the output nodes in the design. The output waveforms are shown in Fig. 4.8(b). The critical charge for this node is 16.8fC. The results are also listed in Table 4-3 for comparison. It is obvious that the triple-well design needs less energy to upset the output node when the pMOS devices are hit, which agrees well with the laser experimental results.

Table 4-3 Critical charges for the output node between dual-well and triple-well designs.

Nodes	**V_o^+, V_o^-**
Dual-well (fC)	22.4
Triple-well (fC)	16.8

Previously, it has been reported that the confinement of holes in the p-well due to a n-hit will result in higher charge collection and lower laser energy requirements [67]. Therefore triple-well designs will result in higher charge collection for n-hits. In general, triple-well should require less energy to cause a SET. This scenario is shown by the hits on transistors M_4 and M_5 listed in Table 4-2.

When the hits are on transistors M_1 and M_2, the situation is different. As the input v_{in}^+ is higher than v_{in}^-, node N_1 gradually goes low at the rising edge of the clock. The data is then latched by the back-to-back connected inverters made from M_4, M_5, M_6, and M_7. These four transistors act like a SRAM cell after the data is latched. At the clock

edge, if there is a hit on M_2, node N_2 will go low quicker than node N_1. Transistors of M_5 and M_4 essentially transfer this voltage to the output nodes. The amount of current sinked by the transistor $M_{4,5}$ will determine the quickness and consequently the SE vulnerability for transistors M_1 and M_2 with which the incorrect data is transferred to the output nodes and subsequently get latched. Thus, higher current through M_5 implies quicker sinking of charges, which will result higher vulnerability to SE current pulses. Fig. 4.9 shows the drain current of M_5 for both dual-well and triple-well designs. It clearly shows that dual-well design has higher current than triple-well to accelerate the SET effects. Therefore dual-well comparator is more vulnerable than triple-well one when the SE-hit is on M_1 or M_2. As a result, in this scenario, the circuit topology determines the relative laser threshold energy for an upset in both comparators.

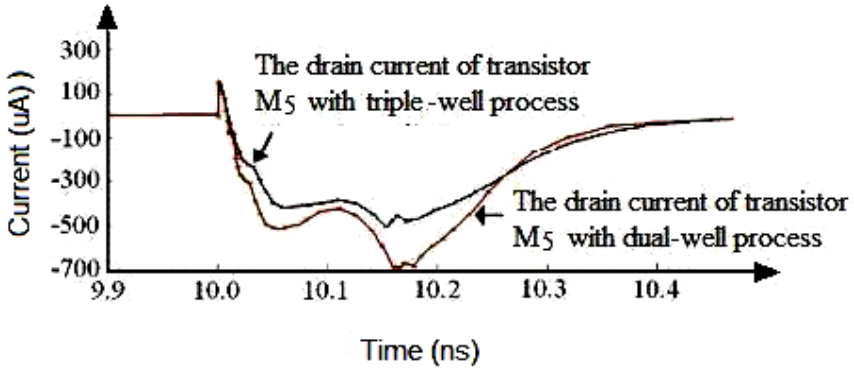


Figure 4.9 Dual-well and triple-well comparators output voltage waveforms and M5 drain current waveforms with SET current pulses of 200μA.

4.5 Summary

Two dynamic comparators were designed and fabricated using a 90nm CMOS technology. One was implemented with the standard n-well CMOS approach using dual-

well technology, another one was designed using an isolated p-well (triple-well technology). Pulsed-laser experiments were used to evaluate the performances of the two comparators under SET effects. The results show that the upset laser energy threshold is a strong function of circuit topology. Additionally, lower electron mobility for triple-well results in higher vulnerability for p-hits and lower charge collection for n-hits in triple-well results in lower vulnerability for n-hits.

5. A RHBD LC-Tank Oscillator-Tolerant to Single-Event Transients [1]

Chapter 3 and Chapter 4 study SET effects on the signal amplitude and transition time. From this chapter, the other two important parameters in analog circuits under SET effects, signal frequency and phase are to be addressed.

5.1 VCO Introduction

PLL is the heart of the commercial and space-deployed electronics systems as it is used to generate on-chip high-frequency clock signals based on an external low frequency reference clock signal. As PLL circuits have been identified as single-event soft point in space and military electronics systems, their reliable operation is critical for system operating in radiation environments [31] [70]. Within a PLL, one of the most critical sub-circuits is the VCO. One popular VCO topology applied in frequency synthesizers in digital systems is the ring oscillator which is shown in Fig. 5.1. Either inverter shown in Fig. 5.1(a) or differential amplifier shown in Fig. 5.1(b) can be implemented as a delay cell in the ring oscillator. Oscillation mechanism of the ring oscillator is that the noise component disturbs each node voltage, yields a growing waveform, and eventually exhibits full swings [50]. The advantages of ring oscillator are simple architecture, low power consumption, wide tuning range, and high integration.

[1] The major results of this chapter were published in the IEEE Transactions on Nuclear Science, vol. 57, Dec. 2010.

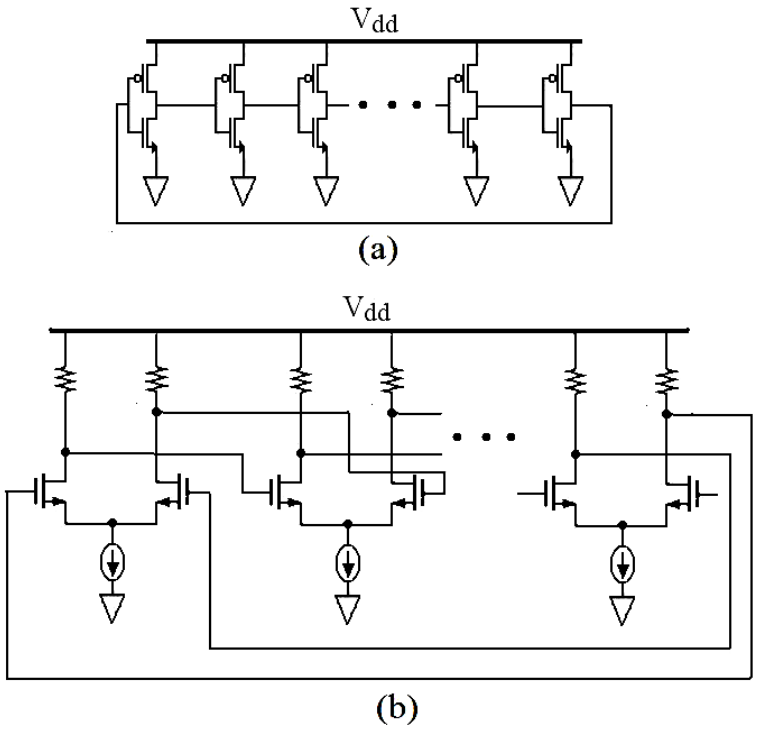


Figure 5.1 An inverter-based ring oscillator. (b) A differential amplifier-based ring oscillator.

However the total number of stages of the inverter-based ring oscillator must be odd while the number of stages of the differential amplifier-based ring oscillator could be an even number. In order to tune the output frequency, control voltages can be introduced to control the bias current or adjust the equivalent load resistance.

The other popular VCO topology usually applied in wireless communication is the LC-tank oscillator shown in Fig. 5.2. Two common-source amplifiers with the LC-tank load provide positive feedback topology. The frequency selective tank is composed of an inductor L in parallel with a capacitor C. The LC-tank circuit causes oscillation by charging and discharging the capacitor through the inductor. The equivalent resistor $R_{1,2}$

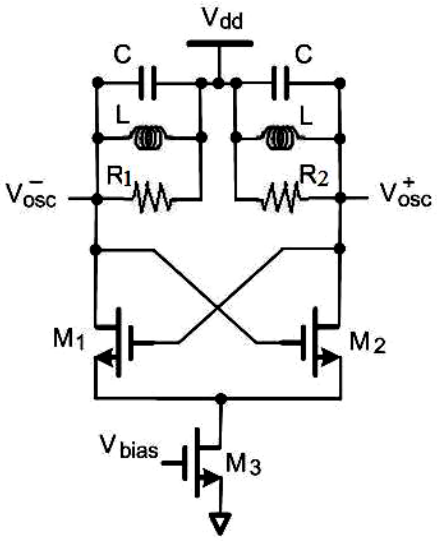


Figure 5.2 Schematic of a LC-tank VCO.

in parallel with LC-tank comes from the inductor series resistance. Resistor $R_{1,2}$ are used for simulation only [50]. The frequency tuning is usually carried out by varying the capacitance value of the tank. At resonance, the frequency-dependent phase shift around the loop is zero because the effect of inductance and capacitance cancel each other at this particular frequency. So the total phase shift around the loop is zero because the common-source stage exhibits a phase shift of 180° at low frequency. Based on the Barkhausen Criteria [50], the oscillation condition requires the transconductance of each transistor satisfying the equation

$$g_m > \frac{R*C}{L} \tag{5.1}$$

where R is the equivalent resistance parallels with the inductance and the capacitance. The sinusoidal waveform from the LC-tank circuit is transformed into a digital waveform through a differential pair. The amplitude of the oscillation is controlled by the tail

transistor M_3 through the controlled voltage V_{bias}. For low bias currents, the amplitude of the output waveform is proportional to the bias current. However, beyond a threshold value of the bias current, the output waveform reaches the supply rails and remains independent of the bias current. The low-bias current operation is termed as current-limited and the high-bias current operation is termed as voltage-limited [71]. In order to tune the output frequency, those capacitors usually implemented by varactors as shown in Fig. 5.3. The varactor is usually working in the weak inversion region. The junction capacitance between the channel and substrate changes by the gate voltage variation.

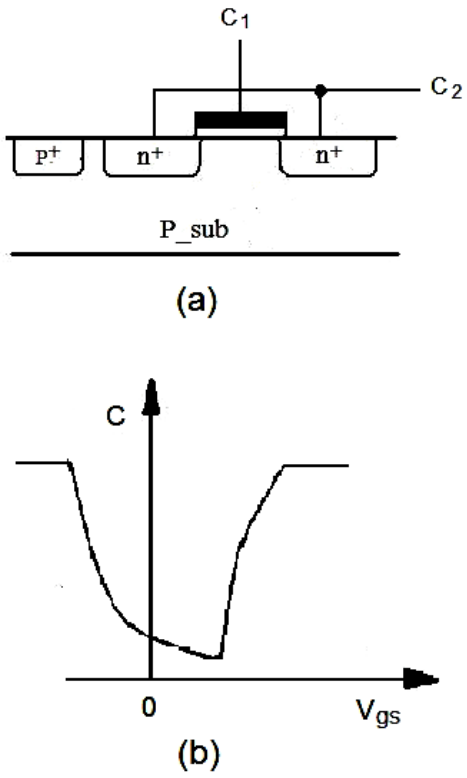


Figure 5.3 (a) A varactor implementation by nMOS transistor. (b) Capacitance characteristic with voltage variation.

Compared to a ring oscillator, the LC-tank oscillator requires more silicon area and consumes more power but it has outstanding phase noise and jitter performance even at very high frequencies [72,73]. LC-tank oscillators are preferred when a tunable precision frequency source is necessary, such as in communication systems. For space and military applications, where outstanding noise and jitter performance are required, LC-tank-based VCO is preferred, especially for RF applications [74].

5.2 SET Effects on the LC-Tank Oscillator

Recent studies have analyzed ring oscillator performance for SETs and have proposed design techniques to improve the PLL single-event performance [75–78]. Chen, et. al. [53] evaluated single-event performance of LC-tank oscillators on SiGe and CMOS technologies. However, mitigation techniques and analysis of such techniques for LC-tank oscillators have not been carried out for more advanced CMOS technologies. In this work, a LC-tank oscillator was designed for an operation at 300MHz. The circuit was simulated using Analog Artist in Cadence tool suite with device models obtained from STMicroelectronics (STM) for the 90nm CMOS design kit. Standard threshold voltage transistors were used in the design. The power supply voltage was 1.0V. The oscillator worked properly at the frequency of 300MHz. The only vulnerable nodes in this circuit are the drain regions of the transistors since the rest of the elements are passive. The capacitors of the LC-tank are implemented with MIM (metal insulator metal). The MIM capacitor is usually built using the top metal layer which is less SETs sensitive.

Single-event simulations were performed to study SET effects on the output oscillating signals. 3-D TCAD simulations using Synopsys Sentaurus software were

conducted for the 90nm CMOS technology. Particles incident with varying LET were used to generate current pulses in the circuit-level simulations. The results shown here are for a particle with a LET value of 120fC ≡ 80MeV-cm^2/mg. The transient current pulse has 10ps of rising time and 3ns of falling time, with around 300μA in magnitude. This 120fC current pulse was used to deposit charges to the drains of the each transistor M_1, M_2 and M_3 to simulate a single-event hit. The SET pulse not only generates an output-signal amplitude variation, but also causes an oscillation-signal phase shift. The perturbations in the amplitude and phase-shift are a strong function of the temporal location of the single-event hit. The two extreme examples (at the zero-crossing and at the peak) are shown in Fig. 5.4 and Fig. 5.5, respectively. First, a single-event hit at the zero-crossing point generates the largest possible phase shift as shown in Fig. 5.4. The voltage shift due to the single-event current injection changes the instantaneous oscillation voltage. After that, the instantaneous voltage is pulled back to zero within one half of a cycle because of the nonlinear oscillator characteristics. This results in a phase shift during this recovery period. On the other hand, as shown in Fig. 5.5, if the current pulse is injected at the peaks of the oscillation waveform, only the amplitude is changed but the phase remains the same [74]. The simulation results shown in Fig. 5.4 and Fig. 5.5 were obtained with the bias current of 0.45mA. The exact amplitude and phase shift are different for other bias current values.

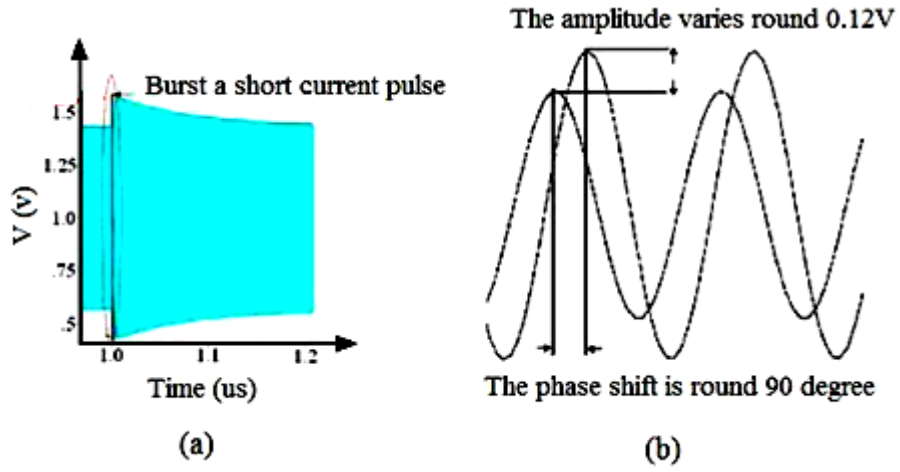


Figure 5.4 (a) Simulation result for the LC-tank oscillator as a SET is injected at the drain of transistor M_3 when a SET happens at the zero-crossing point. (b) Zoomed-in oscillating signal shows both signal amplitude and phase changes when a SET happens at the zero-cross point.

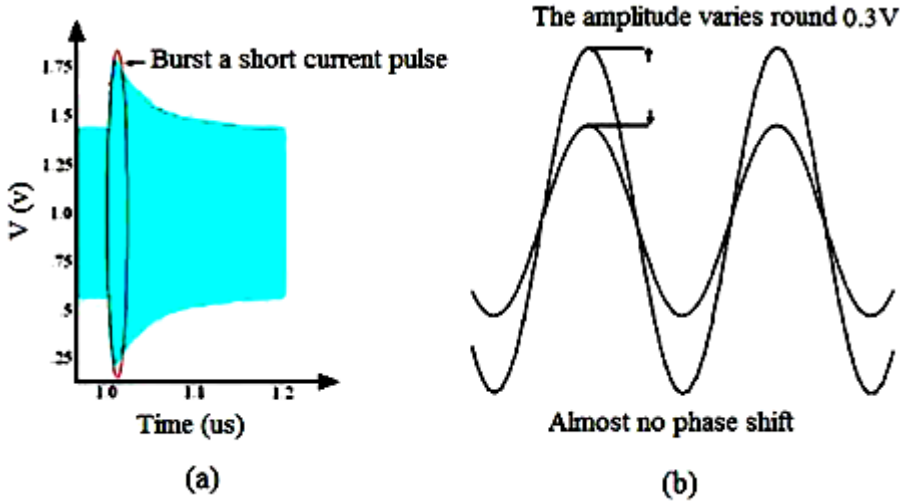


Figure 5.5 (a) Simulation result for the LC-tank oscillator as a SET is injected at the drain of transistor M_3 when a SET happens at the peak amplitude point. (b) Zoomed-in oscillating signal shows only signal amplitude changes when a SET happens at the peak amplitude point.

Table 5-1 shows one set of simulation results for the aforementioned current pulse with 120fC charge deposited on the drain of each transistor in Fig. 5.2. The table shows that the oscillator is less vulnerable to the deposited charge when the bias current is large (voltage-limited operation). It is understandable, since the larger bias current can quickly recover the node voltage.

Table 5-1 Phase and amplitude shifts when 120fC SET charges injected to the drains of M_1, M_2 and M_3 at various bias current values.

Bias current	**Phase shift (degree)**	**Phase shift (degree)**	**Amplitude shift (mV)**	**Amplitude shift (mV)**
	M_1, M_2	M_3	M_1, M_2	M_3
0.75mA	<5	<5	≈0	88
0.70mA	<5	<5	≈0	93
0.65mA	<5	<5	≈0	101
0.60mA	<5	≈20	≈0	110
0.55mA	<5	≈70	8	114
0.45mA	≈10	≈90	50	120

Simulation results from Table 5-1 clearly identifies transistor M_3 is the most vulnerable transistor in the circuit. This is as expected since bias circuits are known to be very sensitive to SETs. Bias circuits, as the name suggests, provide proper operating voltages to the transistors. For analog and mixed-signal circuits, any changes in these voltages induced by a single-event hit in bias circuit, will result in perturbed circuit operation.

Phase shift of the VCO increases with larger charge injected into the drain of M_3, which is shown in Fig. 5.6. This relationship is useful for designing a VCO in PLL since the recovering time may be out of specification of the PLL if the phase shift is too large.

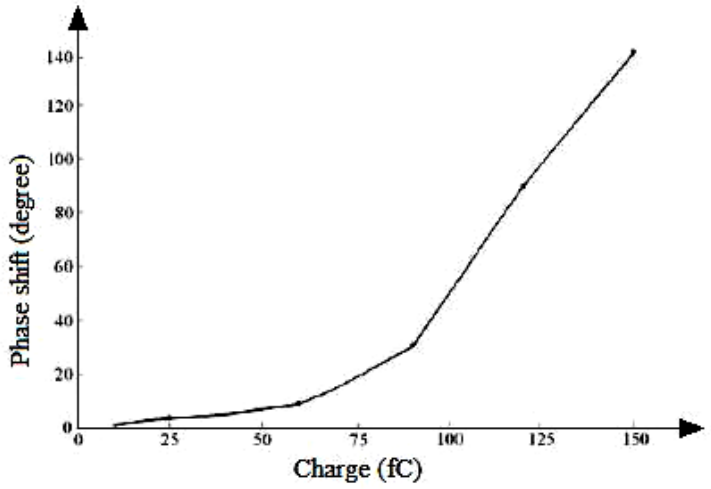


Figure 5.6 Phase shift associates SET charges injected on the drain of M_3 with a bias current of 0.45μmA.

One way to mitigate the SET effects on the bias-circuit is to isolate (or decouple) the bias-circuit from the rest of the circuit. For the LC-tank oscillator, such decoupling can be easily achieved by inserting a resistor between the bias-circuit and the differential pair as shown in Fig. 5.7. The insertion of resistor R_3 not only delays any perturbation in the bias circuit for the differential pair, but also consumes some of the voltage drop caused by the single-event charge. This results in less amplitude and phase shift when transistor M_3 is hit by an ion. However, the value of this resistance must be in a certain range. For a relatively small resistance, the circuit is still working in the current-limited region, and the oscillator is still vulnerable to SETs. For a relatively large resistance, the circuit may have difficulty to maintain oscillations. In addition, the resistor introduces

extra thermal noise which makes the phase noise issue worse. Lastly, larger resistance will require more area in the layout. The circuit used in this example is a general purpose VCO with a simple bias circuit; the decoupling principle is also valid for any complex bias circuits.

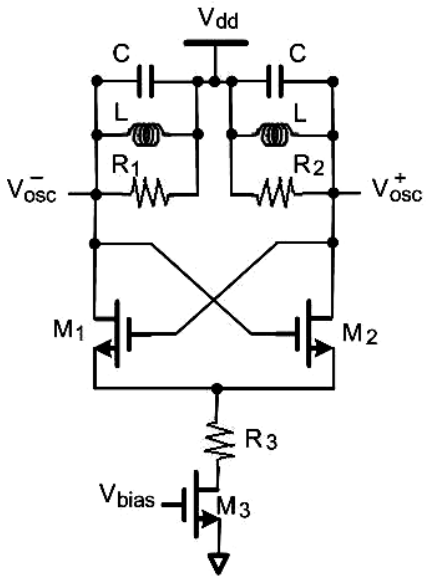


Figure 5.7 Schematic of the LC-tank VCO with the decoupling resistor R_3.

In this design, a range of resistance values is simulated. Simulation results are listed in the Table 5-2. The charge injection condition in Table 5-2 is kept the same as those in Table 5-1. Simulation results clearly show that the decoupling resistor effectively mitigates SETs on LC-tank circuits. The phase and amplitude shifts decrease dramatically with the increasing value of the resistor for identical charge injection conditions. The drawback of such decoupling, as mentioned previously, is the increase in phase noise, area, and the decrease in output signal amplitude due to the additional voltage drop across the resistor. However, VCO circuit outputs are always buffered before being fed to

another circuit. As a result, any loss in amplitude and an increase in phase noise due to the presence of a decoupling resistor can be accounted for by the buffer stage.

Table 5-2 List of resistances of R_3 and corresponding phase and amplitude shifts at the bias current of 0.45mA.

R_3 (Ω)	**Phase shift (degree)**	**Phase shift (degree)**	**Amplitude shift (mV)**	**Amplitude shift (mV)**
	M_1, M_2	M_3	M_1, M_2	M_3
0	≈10	≈90	50	120
0.5K	<5	≈15	60	103
1K	<5	<5	≈0	32
2K	<5	<5	≈0	10

As the time-domain waveforms for SE hits on VCO has been presented by others [75-77], results here are presented in the frequency domain. Fig. 5.8(a) shows the signal spectrum without SE pulses while Fig. 5.8(b) shows the signal spectrum with SE charge of 120 fC. Fig. 5.8(c) shows the signal spectrum with decoupling resistor of 1k**Ω** using the same SE charge collection. All of these simulations are in the bias current of 0.45 mA. The results clearly demonstrate distortion of the output signal spectrum in the presence of a single-event and the improvements in the circuit response due to the presence of the decoupling resistor.

5.3 Experimental Results

Both circuits of Fig. 5.2 and Fig. 5.7 were fabricated using STMicroelectronics 90nm CMOS process technology. The on-chip spiral inductor was built using metal7 and was extracted using ASITIC for simulation purpose [79]. The pi model of the inductor

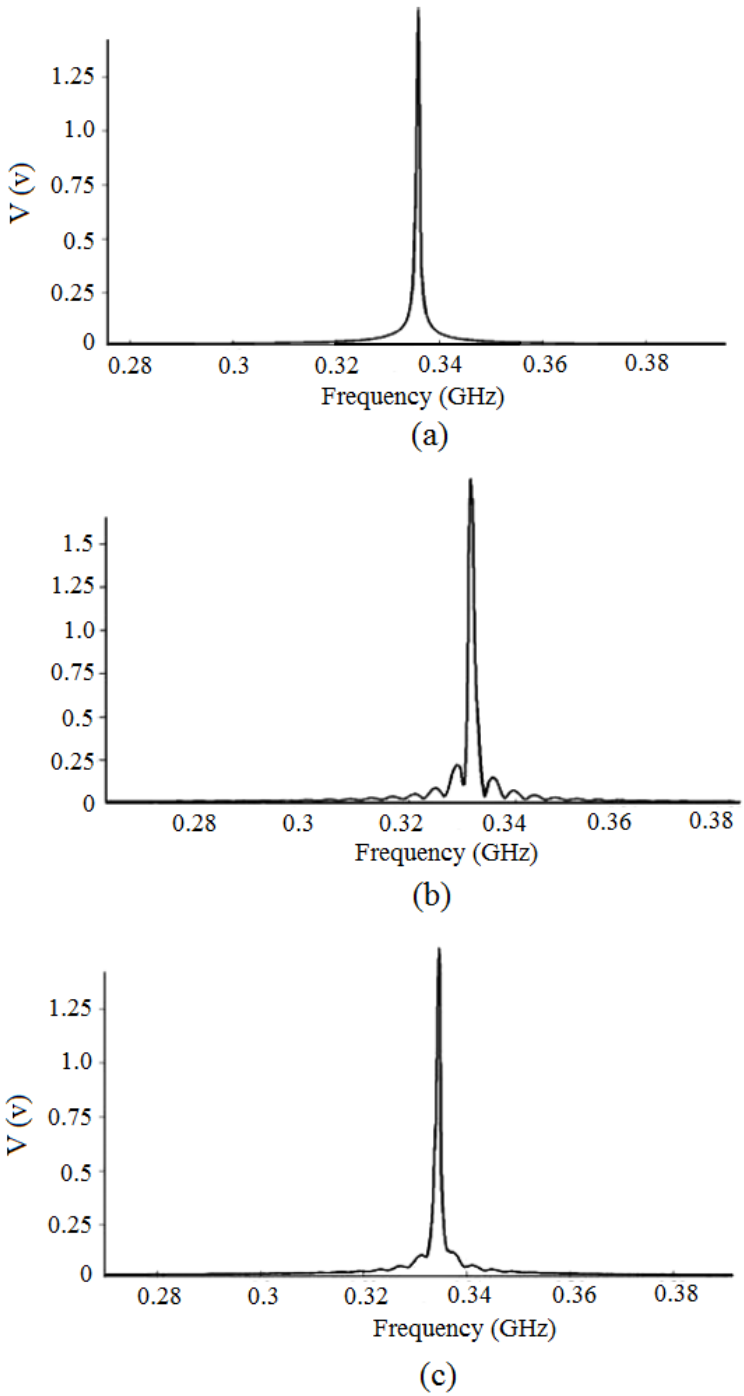


Fig 5.8. (a) The output signal spectrum without SET pulses at a bias current of 0.45 mA. (b) The output signal spectrum with 120fC SET charge at the drain of M_3 at bias current of 0.45 mA. (c) The output signal spectrum using 1kΩ decoupling resistor R_3 with 120 fC SET charge at the drain of M_3 at bias current of 0.45 mA.

extracted from ASITIC is shown in Fig. 5.9. In the model, L is 953pH, series resistor Rs of the on-chip spiral inductor is 2.36Ω, equivalent capacitors from metal7 to the substrate $C_{1,2}$ are 83.2fF and 92.9fF, respectively, and the substrate resistors $R_{1,2}$ are 1.49KΩ and 1.15KΩ. The capacitance in the LC-Tank is 2.2pF, which is implemented using MIM cap in the STMicroelectronics 90nm CMOS technology. The width of transistors is 10μm. The resistor of 1.14kΩ [2] is implemented with rnpo, a poly resistor of area of 43μm^2, from the STMicroelectronics 90nm CMOS standard library.

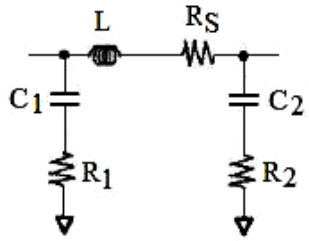
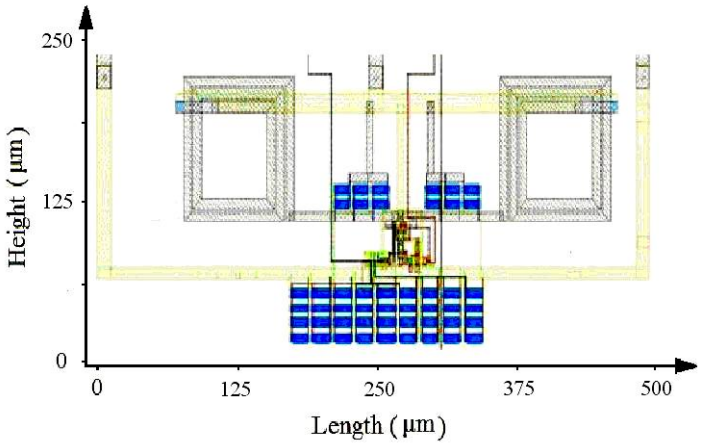


Figure 5.9 pi model of a spiral inductor.

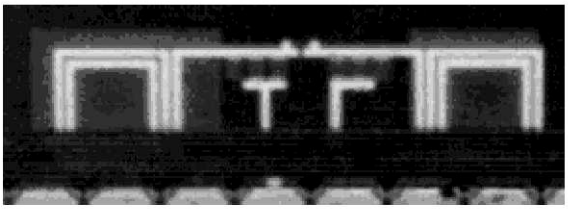
The chip layout view is shown in Fig. 5.10(a). The whole area of the die shown in Fig. 5.10(b) was scanned with the pulsed-laser beam to find the sensitive area. As expected, hits on (or near) transistors M_1, M_2, and M_3 were found to be the source of SET effects. One way to measure the relative hardness of these LC-tank circuits is to identify the minimum energy necessary to perturb the measurable shift in the output signal. This is similar to identifying the minimum LET of particles that causes a perturbation in the output voltage. To identify the threshold laser energy, maximum laser

[2] Due to the process variation, resistance close to 1kΩ was built with poly layer.

energy was used at first to generate the distortion at the outputs. Then the energy level was gradually reduced and recorded until it reached a threshold. The threshold is defined as the minimum laser energy to generate an observable distortion on the signal.



(a)



(b)

Figure 5.10 (a) Layout view of the oscillator. (b) Die photograph of the oscillator.

The output signal of the LC-tank were observed on a high-speed oscilloscope and a spectrum analyzer. Screen captured of the spectrum analyzer before and during the single-event hit are shown in Fig. 5.11(a), (b), and (c). These diagrams illustrate how the spectrum of the sinusoidal signal is distorted when the laser energy is higher than the threshold. Fig. 5.11(a) shows the signal spectrum before the pulsed-laser beam irradiation. Fig. 5.11(b) and (c) show the signal spectrum with and without the decoupling resistor

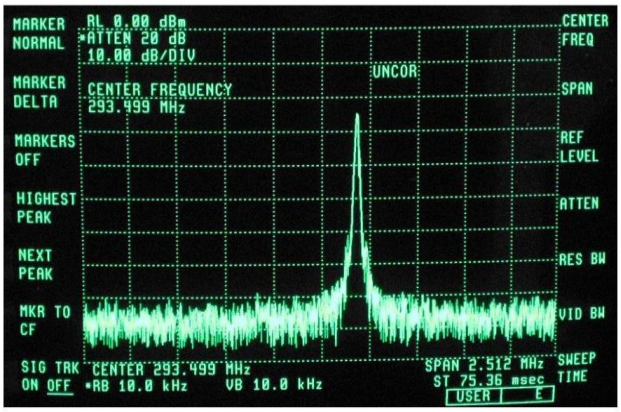
using the same laser energy irradiation. It clearly demonstrates that the decoupling resistor effectively mitigates SET effects. For identical bias currents, the corresponding minimum threshold laser energy required to cause a waveform distortion on the spectrum analyzer (observable distortion at the oscillator output) increases approximately by a factor of 6 for the RHBD design as compared with the conventional design. Table 5-3 lists the actual data of threshold laser energy to generate upset from the experiment results.

Table 5-3 Threshold laser energy for the bias current of 0.45mA for the conventional and RHBD designs.

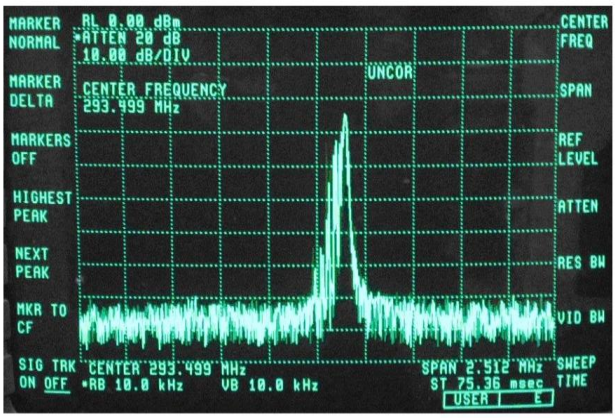
Design	**Threshold laser energy**
Conventional	0.44nJ
RHBD	2.5nJ

5.4 Summary

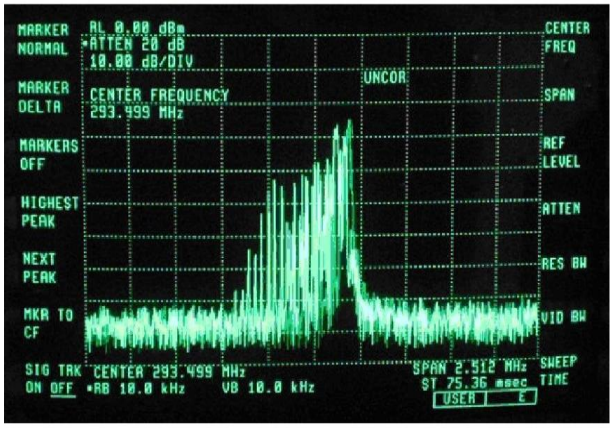
LC-tank oscillators can be biased in current-limited or voltage-limited regimes. Both simulation and experimental results show that the bias current greatly affects SET tolerance of an LC-tank oscillator. In SET-tolerant point of view, the oscillator performs better in the voltage-limited regime than in the current-limited regime, with the cost of higher power consumption. If the oscillator must be biased in the current-limited regime, an additional decoupling resistor in series with the tail transistor should be added to mitigate SET effects. The decoupling principle introduced in this example can be used for other biasing circuits to mitigate SET effects.



(a)



(b)



(c)

Figure 5.11 Oscillator output spectrum (a) Before the pulsed-laser beam irradiation. (b) During the pulsed-laser beam irradiation with a decoupling resistor. (c) During the pulsed-laser beam irradiation without a decoupling resistor.

6. A Single-Event Transient-Tolerant Monolithic Phase-Locked Loop Design [1]

VCOs are commonly used in control systems such as PLLs in order to provide the accurate frequency or phase alignment at the output signals in practical applications. It is beneficial to study radiation effects on PLLs since the transition time of the oscillating signal in PLLs is one of the critical parameters for analog circuit design in radiation environments.

6.1 Basic Technology and Operating Principles of Phase-Locked Loops

A PLL is a particular control system that synchronizes the output signal with a reference signal in both frequency and phase. PLLs are widely used as a functional block in many applications, such as local oscillators in wireless communications, clock recovery circuits in the front-end of the serial or parallel data links, and frequency synthesizers in digital systems. Traditionally, the PLL is a feedback system that can be modeled as shown in Fig. 6.1 which consists of four basic functional blocks: a VCO, a phase frequency detector (PFD), a low pass filter (LPF), and a frequency divider. The VCO produces a frequency of output signal V_o of N times that of the reference signal, V_{ref}, where N is the division ratio generated by the frequency divider. PFD is used to generate the signal V_{pfd} whose DC voltage is proportional to the phase difference of V_{ref} and V_{div} as shown by

[1] The major results of this chapter were published in the IEEE Workshop on Silicon Errors in Logic- System Effects, Stanford University, 2010.

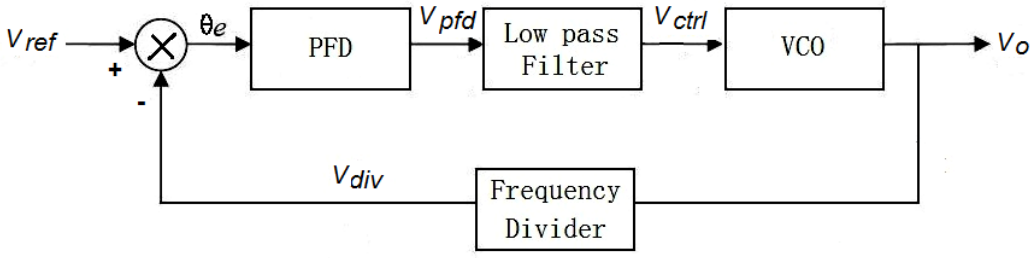


Figure 6.1 A PLL model.

$$V_{pfd} = K_{pfd} * \theta_e \tag{6.1}$$

where K_{pfd} is the gain of PFD while θ_e is the phase difference between V_{ref} and V_{div}. Due to the noise issue, signal of V_{pfd} contains both of DC voltage and high frequency components. High frequency components will cause the frequency variation at the VCO output. In order to decrease the high frequency component at the control voltage V_{ctrl}, a LPF is interposed between the PFD and VCO to suppress high-frequency components from the PFD output. The VCO oscillates at a frequency ω_o is determined by the output signal V_{ctrl} of the LPF. The frequency ω_o is given by

$$\omega_o = \omega_{free} + K_{vco} * V_{ctrl} \tag{6.2}$$

where ω_{free} is free oscillation frequency of the VCO without control voltage, and K_{vco} is the gain of the VCO. In terms of excess signal phase variation θ_o, during the locked state, θ_o is given by

$$\theta_o = K_{vco} * \frac{V_{ctrl}}{S} \tag{6.3}$$

In the locked state, the frequency of V_{ref} and V_{div} are exactly the same while the phase difference between them can be zero or kept constant with time depending on the different PLL implementation architectures. For some reasons, if the frequency of V_{ref} increases, in order to track the input frequency, the PFD generates a higher DC voltage to control the VCO in such a way that a higher frequency oscillation signal is obtained to keep up with the input frequency. This mechanism is shown in Fig. 6.2 [50].

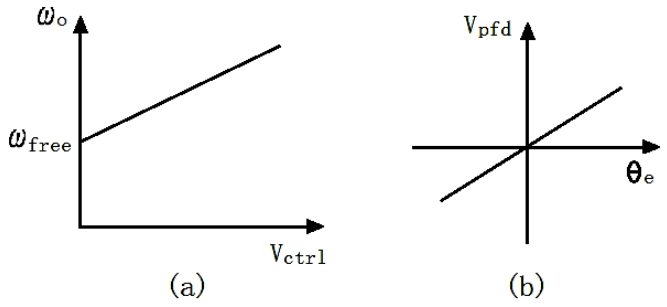


Figure 6.2 (a) Ideal transfer curve of VCOs. (b) Ideal transfer curve of PFDs [50].

Two types of PLLs are popular in the frequency synthesizer design: analog linear PLLs and digital PLLs. The PFD block is usually implemented by a multiplier in analog linear PLLs while digital PLL consists of two edge-triggered, resettable D flip-flops (DFFs). Depending on the different PFDs implementation approaches, the output from PFD can either be applied directly to the loop filter, or converted to a current by a charge pump (CP). The difference in architecture makes analog linear PLLs and digital PLLs have different characteristics and performances. However, both can have the same VCO implementation.

In analog linear PLL, the multiplier is used as a PFD. For two input signals of $A_1\cos\omega_1 t$ and $A_2\cos(\omega_2 t+\Omega)$, the output of multiplier is

$$y(t) = A_1 \cos \omega_1 t * A_2 \cos(\omega_2 t + \Omega) \tag{6.3}$$

$$y(t) = \frac{A_1 A_2}{2} \cos[(\omega_1 + \omega_2)t + \Omega] + \frac{A_1 A_2}{2} \cos[(\omega_1 - \omega_2)t - \Omega] \tag{6.4}$$

where A_1 and A_2 are amplitudes of those two signals, respectively. Both of the signal frequencies are the same while the phase difference is Ω. After the stage of LPF which ω_{3db} is smaller than the $\omega_1 + \omega_2$, the signal becomes

$$y = \frac{A_1 A_2}{2} \cos \Omega \tag{6.5}$$

Fig. 6.3 shows that the characteristic of PFD implemented using a multiplier. Due to the non-monotonic characteristic of multiplier PFD, in order to keep the frequency tracking, the phase difference between V_{ref} and V_{div} cannot go beyond π/2. In other word, the static track range of PLLs is limited by the multiplier PFD.

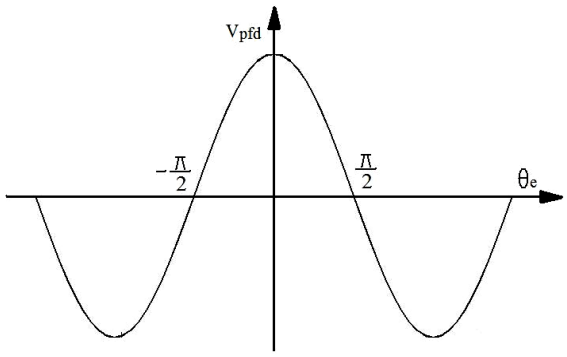


Figure 6.3 Characteristic of multiplier PFD.

Digital PLLs are used in the modern on-chip PLLs design. Digital PLLs are hybrid systems built from analog and digital function blocks such as PFD. System implemented with DFF is efficient in dealing with large error in frequency. DFF is

typically accompanied with a CP as shown in Fig. 6.4. Digital PFD consists of two rising edge-triggered, resettable DFFs with their D inputs tied to V_{dd}. V_{ref} and V_{div} serve as the clocks for the flip-flops. A digital PFD detects the phase difference between V_{ref} and V_{div} and converts the phase difference into two control signals Up and Dn. Up and Dn are then fed to the down-stream CP implemented with two current source/sink I, pMOS transistor M_1, nMOS transistor M_2, and a capacitor C. The main function of the CP is to convert Up and Dn pulses into a DC current. This current charges/discharges the capacitor C to achieve the required control voltage. In contrast to the multiplier PFD, the digital PFD can detect not only the phase error, but also the frequency error of V_{ref} and V_{div} [81].

This example illustrates the mechanism of a digital PFD with the CP. When the frequency of V_{ref} is higher than that of V_{div}, the rising edge of V_{ref} makes the logic of Up to high and the logic of Dn to low, this state turns the pMOS transistor M_1 on, and keeps nMOS transistor M_2 off. Current I charges the capacitor C, increasing the output voltage of V_{ctrl} speeding up the VCO frequency to keep up the frequency of V_{ref} . When the rising edge of V_{div} is sampled, logic of Dn becomes high. During this period, both M_1 and M_2 turn on. Ideally, the control voltage keeps constant if the current source is equal to the current sink. However, after a certain delay time of the AND gate, both DFFs are reset to zero. During this time, both transistors M_1 and M_2 are turned off, and the control voltage is in the floating state. A diagram of Fig. 6.5 shows each of input/output signal waveforms of digital PFD with the CP.

Digital PLLs offer several advantages over the analog linear PLLs. Using digital PFD, the acquisition range is not limited by the PFD. In other words, digital PLLs have

wider acquisition range than that of analog linear PLLs. Digital PLLs also do not have a steady state phase error if the transistor mismatch issue is not considered.

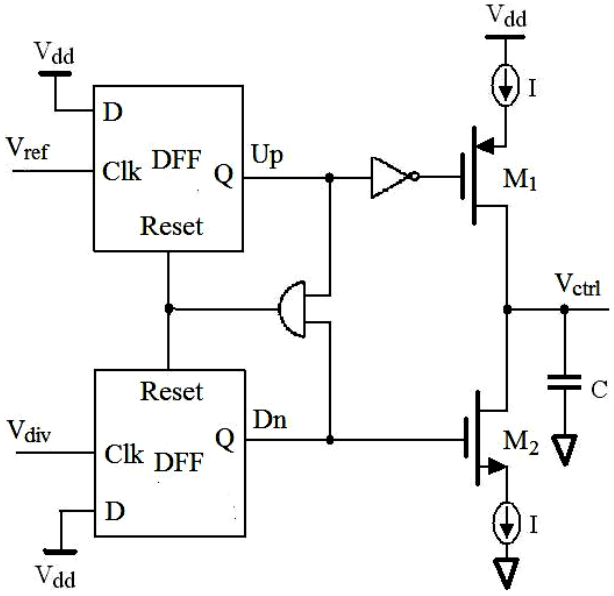


Figure 6.4 Architecture of the PFD with the CP.

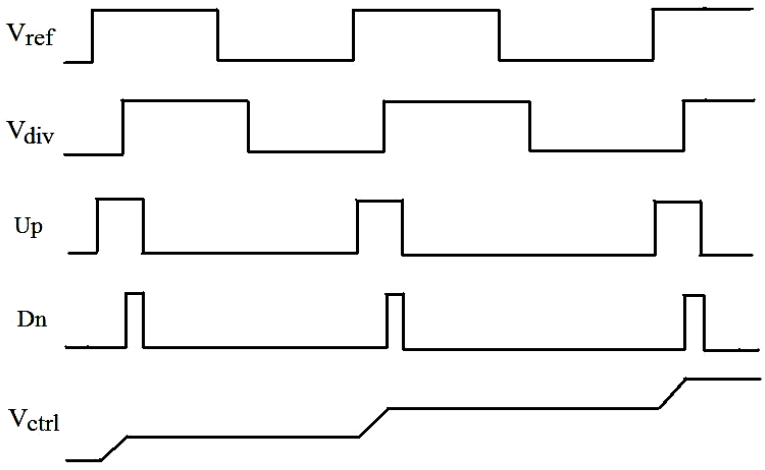


Figure 6.5 Input/output signal waveform of the digital PFD with the CP [80].

6.2 Phase-Locked Loops in Radiation Environments

For electronics and communication systems used in aerospace applications, SET effects may result in an abrupt frequency or phase shift. In fact, PLLs have been reported to be susceptible to SET effects and more attention was paid in the design and implementation of PLLs in radiation environment applications [31] [70]. Recent studies have analyzed circuit performances for SETs and have proposed design techniques to improve PLL performance under SET effects [75-77] [82-83]. Boulghassoul, et al. [82] have analyzed SET effects on the CP module and presented a solution method which was implemented by Loveless, et al. [75]. CP module is identified to be the most sensitive block of PLLs to SETs [75]. In order to improve the SET tolerance in the CP module, the voltage-based CP [84] is used instead of the current-based CP shown in Fig. 6.6.

In the current-based CP shown in Fig. 6.6 (a), M_{3-6} are made up of transmission-gate switches controlled by the Up and Dn signals. With a certain bias voltage, the current source/sink is composed by M_1 and M_2, respectively. The module of CP is vulnerable to SETs since a single ion strikes on any node in the CP circuit, will significantly change the output voltage. For the conventional current-based CP described in [84], there are six vulnerable transistors in the output stage. Furthermore, the output stage is directly connected to the capacitive node of the LPF [75]. To eliminate the problem, a voltage-based CP shown in Fig. 6.6 (b) is used in which the current sources are removed and a resistor is introduced to provide isolation between the output node and the SETs critical parts. However, while using this method, a special technique must be used to decrease power supply fluctuation. As shown in Fig. 6.6 (b), the two transmission-gate switches are connected to V_{dd} or GND, fluctuation of V_{dd} and substrate

noise which are usually in the mixed-signal circuits such as PLLs affect the output voltage even they are attenuated by the isolation resistor R. In addition, adding a resistor increases non-linear response in the tracking period and thus decreases tracking speed of the PLLs. Also, extra thermal noise is introduced with the insertion of resistor R.

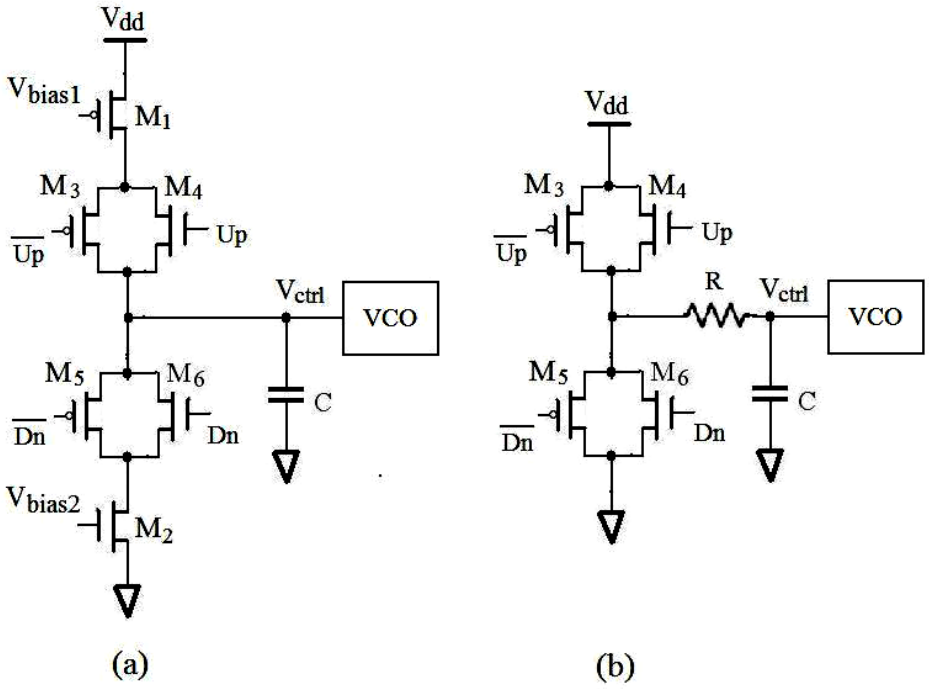


Figure 6.6 (a) Schematic of the current-based CP. (b) Schematic of the voltage-based CP.

Experiments show that VCO is also very susceptible to SETs [76]. Study of the current-starved VCO illustrated in Fig. 6.7 shows that a SET occurring in the input bias stage will result in transients on the bias voltage nodes and significantly varies the frequency as shown in Fig. 6.8. This type of transient occurrence in the VCO can be effectively mitigated using an analog redundancy method in the input-bias stage. However, each of the VCO cells which are SET vulnerable is not protected in this

method. Instead, an approach based on the triple modular redundancy (TMR) VCO is provided to achieve a higher radiation tolerance level compared to a single VCO method for a price of complexity and cost. The drawback of this method is that the three self-running VCOs have their own feedback paths and thus they are very difficult to be synchronized. This also results in a much more time jitter in the output signals.

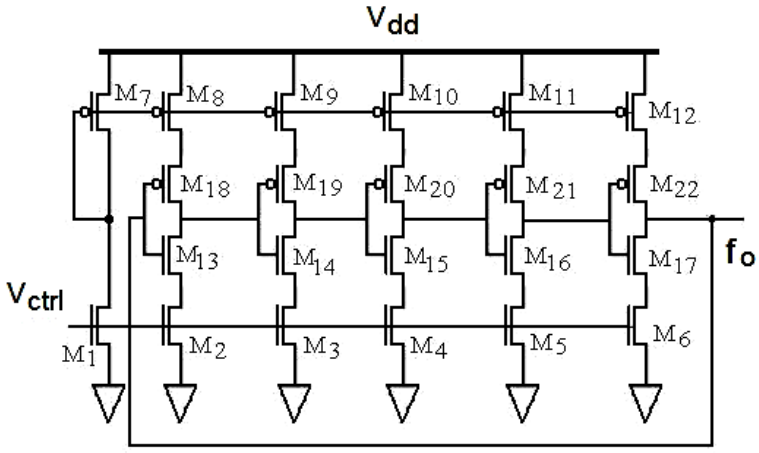


Figure 6.7 Schematic of the five-stage current-starved ring VCO.

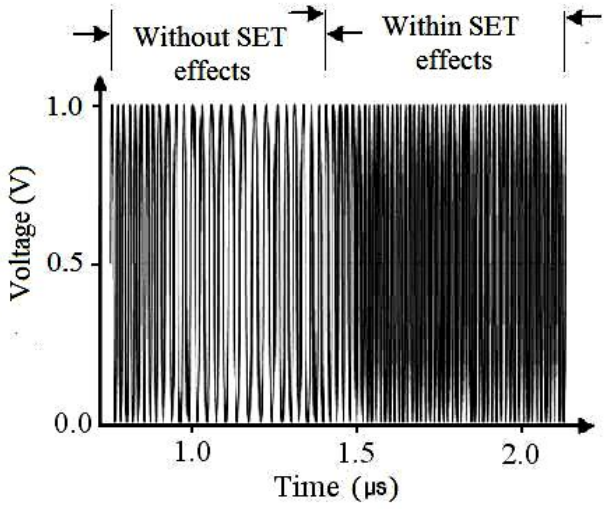


Figure 6.8 Waveform of the VCO under the SET strike.

6.3 A Triple Modular Redundancy Scheme in RHBD PLLs Design

All of these SETs analysis and related RHBD techniques focus only on some of the sub-blocks in the PLLs such as the CP and the VCO. Frequency and phase shifts are still generated by SET effects in other sub-blocks such as the PFD and the frequency divider. The other main shortcoming of these RHBD approaches in PLLs is that the problem of PLLs under radiation environments such as frequency and phase shift are not efficiently solved. It seems that those RHBD approaches are redundant schemes because PLLs themselves have a function to track the output frequency to the reference frequency. In other word, without RHBD design, the frequency can be corrected by the negative topology of PLLs if the frequency shift is not beyond tracking range of the PLLs. In this way, a new RHBD PLL approach of TMR RHBD PLL is provided. Contrary to the previous RHBD schemes in PLLs, this approach prevents signal frequency from shifting under SET effects.

The TMR PLL is followed by a voting circuit. To achieve a better synchronized signal, only one feedback path is used as shown in Fig. 6.9. The PLL is designed and implemented using digital approach. A single voter can remove signal errors introduced by one of the three PLLs in the previous stage. However, the voting circuit does not protect itself if a SET strikes upon it. To eliminate the problem, an approach of at least three parallel voting circuits (five parallel voting circuits in this design) to drive a single node is introduced. If a SET happens in one of them, the other four still provide enough driving capacity to maintain the correct logic. In the layout, these voting circuitries should be spread throughout the die to reduce the chance of SETs striking more than one of the voting circuitries at the same time.

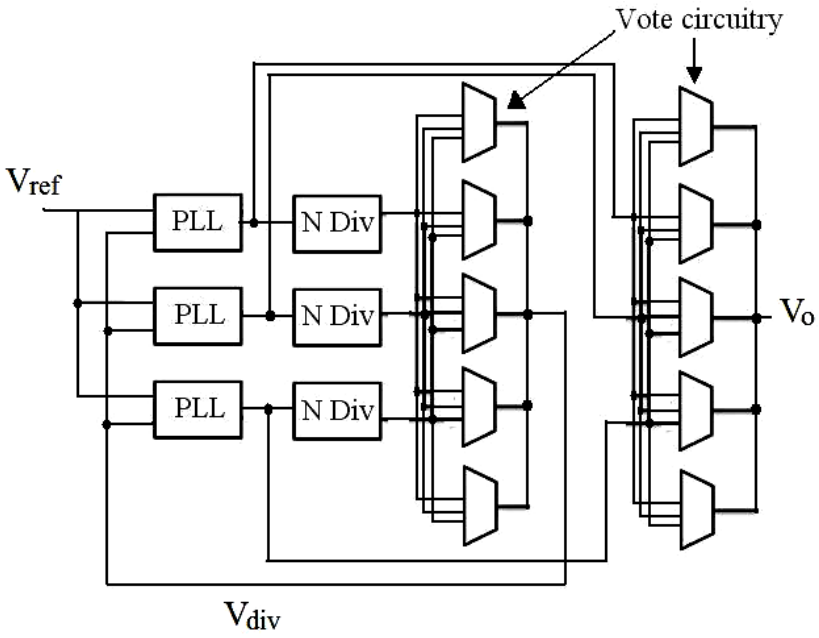


Figure 6.9 Block diagram of the TMR PLL with voting circuit.

Unlike conventional voting logic circuits, it is possible to have two signals with the same frequency and still get an incorrect result due to the jitter problem in the high frequency signal. This is illustrated in the diagram of Fig. 6.10. Assuming that signals X and Y are two ideal correct signals without jitter, both signals have exactly the same frequency at a fixed phase difference but Z has a relatively large time jitter as shown. Simulation results show that a significant frequency variation appears in the output signal. It will be much worse in reality since time jitter always exists in all signals. To guarantee this phase-induced voting error will not occur, one method is to add the signal "dead zone" of the voting circuit by choosing large size transistors. The other method is used in this design: the phase difference among these three signals must be smaller than the minimum pulse width to which the voter will respond. This requires a stable PLL design to minimize the phase-induced voting error.

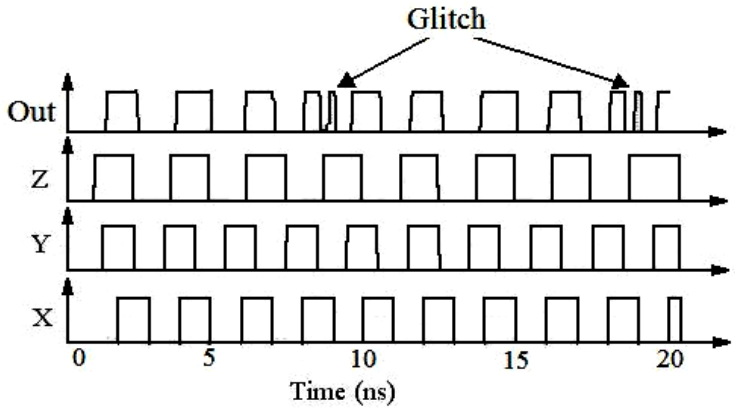


Figure 6.10 Phase-induced voting error [85].

Since stability is the most critical parameter in this radiation tolerant PLL design, a narrow bandwidth with low loop gain is targeted. With the guarantee of the voting circuit working with a low jitter PLL, even SETs happens in one of the PLL branches, a correct output signal with stable frequency is still achieved. A simulation of a control voltage VCO for low bandwidth and low loop gain design is shown in Fig. 6.11. A PLL with high loop gain and large bandwidth was implemented and the result is shown in Fig. 6.11 (a). From the phase-induced voting error analysis above, this design introduces a significant time jitter and is not suitable for the TMR PLL-hardened design. Fig. 6.11 (b) shows that if the bandwidth of ω_n decreases by a factor of 25, the signal variation is slightly improved. Decreasing the bandwidth can be obtained by decreasing the value of current source/sink in the CP or increasing capacitance of the LPF. The acquisition range is not significantly affected in digital PLLs; however, decreasing the current value makes the transistors more vulnerable to SET effects while increasing capacitor C leads to more area occupation. Fig. 6.11 (c) shows the result from the low gain PLL implementation. As

the VCO gain is intentionally reduced, significant stability is achieved. In this way, this work focuses on discussion how to decrease the gain of the VCO to improve the stability performance of the PLL.

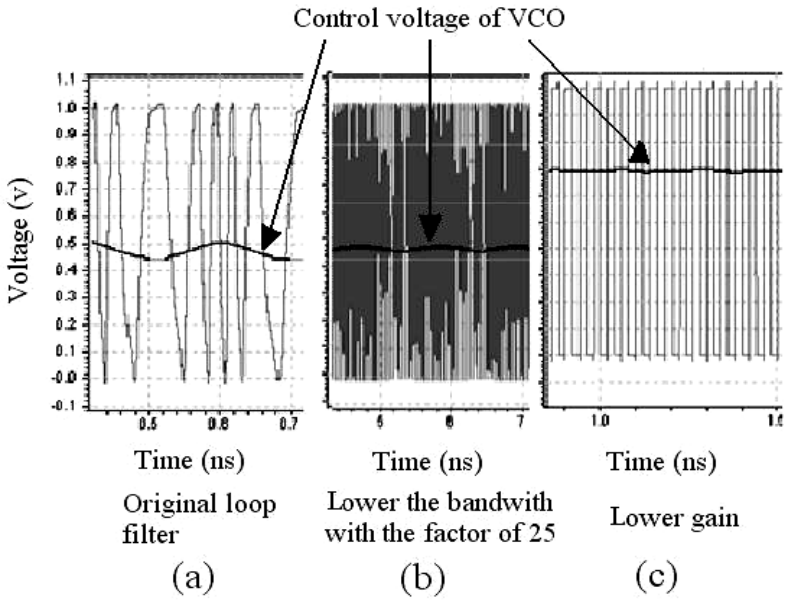


Figure 6.11 Stability management and comparison [85].

In this work, a current-starved VCO is used [86–88]. The diagram is shown in Fig. 6.12. The control voltage Vctrl determines the current sink consisted of transistors M_{1-6}. Through the current mirrors, this voltage also determines the amount of current source to the five cascode inverters using transistors M_{7-12}. Transistors of M_{13-22} form the inverter chain. The current source and the current sink determine the rising and the falling transition times of the inverter. By changing the control voltage, Vctrl, output frequency can be changed by the following equation:

$$I + \Delta I = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 + \mu_n c_{ox}\frac{W}{L}(V_{gs} - V_{th})\Delta V_{gs} \quad (6.6)$$

$$\frac{dv}{dt} = \frac{\Delta I}{C} \tag{6.7}$$

where μ_n is the mobility of electrons, C_{ox} is the total capacitance between the gate and silicon per unit area. W and L are the width and effective length of transistor, respectively. C is the total capacitance of the output nodes of each inverter. The frequency changes with variable capacitor charge and discharge time. The transfer characteristic of the current-starved VCO is such that when the control voltage, V_{ctrl}, is near the threshold voltage of the transistor M_1, a very wide variation in frequency occurs for tiny changes in V_{ctrl}. In other words, the voltage to frequency gain, K_{vco}, is very high when the control voltage V_{ctrl} is close to the transistor threshold voltage [89]. The reason is that bipolar dominates the transistor characteristics when transistors work in the sub-threshold region. The transconductance of bipolar is much great than that of MOS transistor with a same bias current which is given by

$$\frac{g_m(MOS)}{I_{bias}} = \frac{2}{V_{gs} - V_{th}} \tag{6.8}$$

$$\frac{g_m(bipolar)}{I_{bias}} = \frac{1}{V_T} \tag{6.9}$$

where V_T is the thermal voltage, around 26mV at room temperature. Normally, the overdrive voltage of V_{gs}-V_{th} is around 200mV for a good design which a tradeoff among the gain, voltage swing, bandwidth, noise, etc. In order to obtain a low loop gain, a relatively high control voltage V_{ctrl} is intentionally applied in the locking period. This can be accomplished by inserting capacitors C_{1-4} at the output nodes of each inverter in such a way that lower the VCO free oscillation frequency.

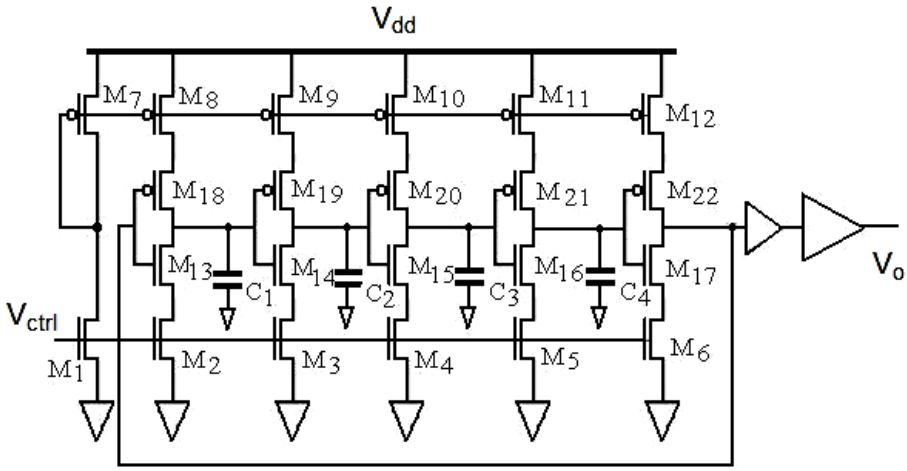


Figure 6.12 Schematic diagram of the low-gain current-starved ring VCO.

To obtain current matching in PLL implementation, the CP is implemented by a current-steering charge pump which is shown in Fig. 6.13 [90]. Also, for the low-pass filter, a second order passive LPF implemented with R_1 and $C_{1,2}$ is used in this design. A frequency divider factor 16 is implemented using DFF chains.

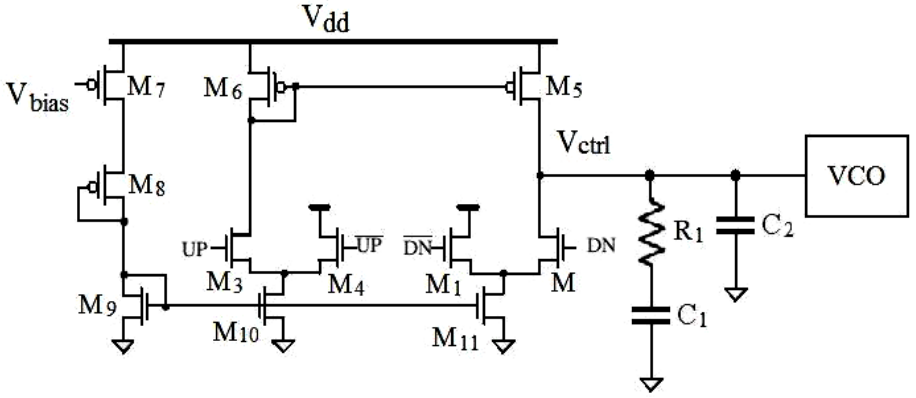


Figure 6.13 A practical implementation of the current-steering charge pump [90].

To verify the SET effects, a transient double exponential current pulse (10ps rising time, 3ns falling time, and 300μA magnitude,) is injected at the output node of one

of the VCO cells. In addition to the double exponential current pulse with parameter mentioned above to stimulate SETs on the new design approach, two noise sources are also added to simulate the power supply fluctuation and substrate noise. This intentionally introduces more time jitter into the system. Fig. 6.14 shows the simulation results of the designed TMR RHBD PLL with SET effects. The top diagram is the control voltage and the middle one is the output signal which provides an oscillation frequency of 800MHz. Frequency of V_{div} is 50MHz in the bottom diagram is equal to the reference frequency at the locking period. When a SET happens at around 1.5μs, the control voltage shows a very small change in amplitude while the oscillation frequency remains constant. Fig. 6.15 zooms in the output signal from 1.5μs to 1.55μs when a SET strikes. It shows that there is no frequency variation at the output introduced by a SET.

One important factor negatively affects the output signal purity. This factor is the phase noise associated with physical devices in the PLL. Phase noise limits quality of the oscillation signal. Phase noises of the PLL without RHBD design and with RHBD design are shown in Fig. 6.16. With the TMR RHBD PLL, performance of the phase noise is reduced due to more transistors are used in the circuits.

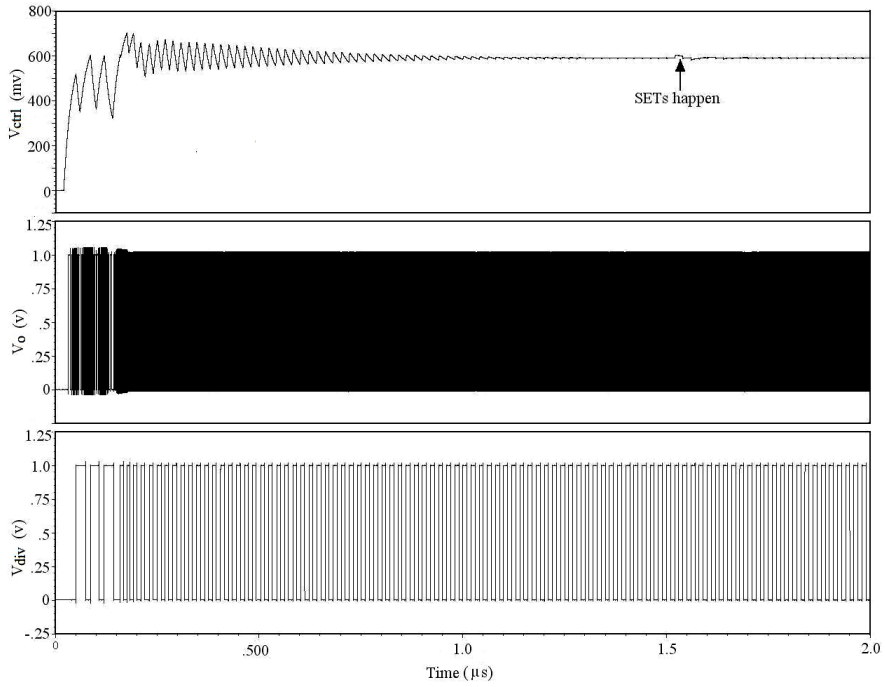


Figure 6.14 Output waveform of the PLL under SETs event with radiation hardened design.

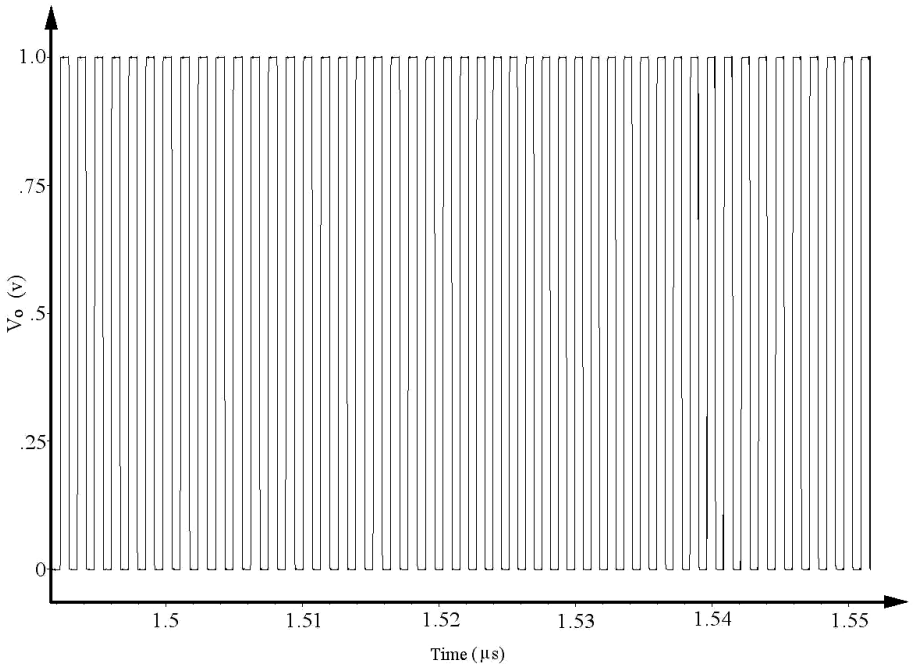


Figure 6.15 A zoom-in view of the output waveform of a PLL at a SET event.

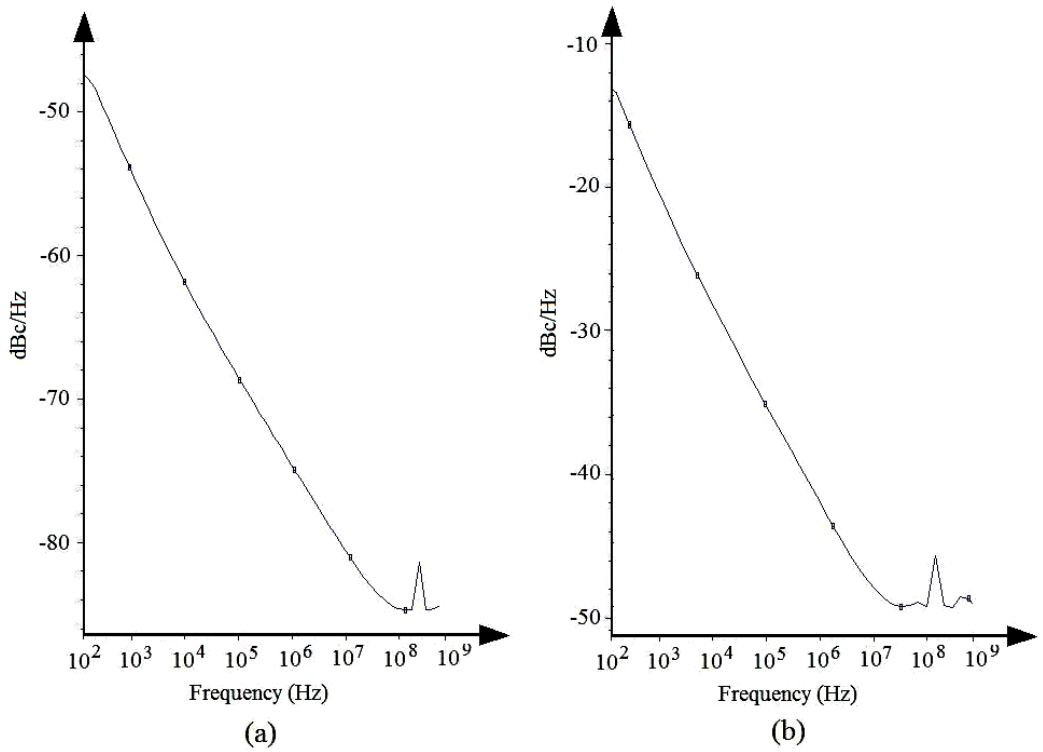


Figure 6.16 (a) The phase noise of the PLL without RHBD design. (b) The phase noise of the PLL with RHBD design.

A layout view and the photo of the die of the PLL are shown in Fig. 6.17. A total area of 0.1008mm^2 was used for this design in the TSMC 90nm CMOS technology. Majority of the area is occupied by the capacitors.

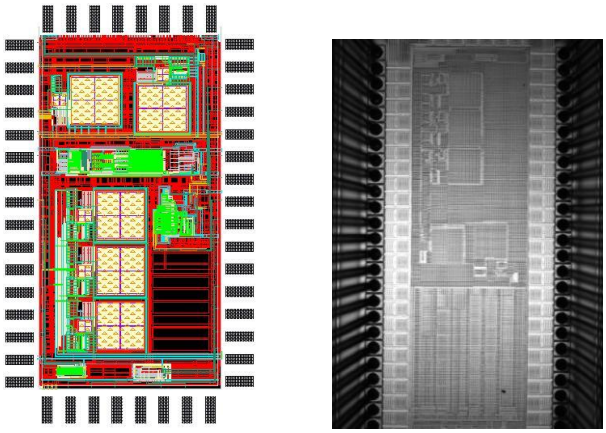


Figure 6.17 A PLL layout view and photograph of the PLL.

6.4 Summary

A new SET tolerant PLL was designed and implemented with redundancy topology. Based on the TMR topology requirement, this chapter analyzes two important parameters, loop gain and bandwidth in PLL design, and concludes how to design these parameters which are suitable for SET tolerance. It is obvious that the area and power consumption will increase by using TMR method. So this approach may not be suitable for certain low-power applications. In the field of analog RHBD design, this approach also provides a general method to mitigate SET effects which is independent on a particular circuit.

7. Single-Event Transients Detection [1]

A new voltage-mode bulk built-in current sensing circuit design and a new current-mode bulk built-in current sensing circuit are presented in this chapter. The development of such sensor will greatly enhance designers ability to isolate SE faults and develop efficient mitigation strategies.

7.1 Motivation

With the ever-decreasing geometries in modern ICs, the soft error rate is predicted to increase significantly with technology scaling trends. Hardening techniques are the most common approaches to mitigate SET pulses in electronics used in radiation environment. However, the area and power overhead required for such approach is too high. Also, such mitigation techniques are based on error correction instead of detection and correction. If the occurrence of an SET event in an IC could be detected and the hit location can be located in real time then various mitigation approaches could be implemented at the system level. Two examples of a microprocessor and a FPGA are illustrated in Fig. 7.1 and Fig. 7.2, respectively. If SETs happened in one stage in the pipeline architecture such as the write back stage in Fig. 7.1, and SETs could be detected instantly, then the error can be eliminated by executing a jump back instruction which re-loads the instruction several clock cycles [91] [92]. In another example, SET-induced errors happened in one of the

[1] The major results of this chapter were published in the Workshop on Silicon Errors in Logic - System Effects, Stanford University, 2010.

look-up tables (LUTs) in FPGAs can be detected and located with X-Y sense array shown in Fig. 7.2. Once the location of SETs is identified, proper error-correction mechanisms can be implemented accordingly. Therefore, the method of SET detection is a critical way in this type of SET-tolerant approach. Thus, it is apparent that the SET-induced bulk current can be utilized in the application of SET detection.

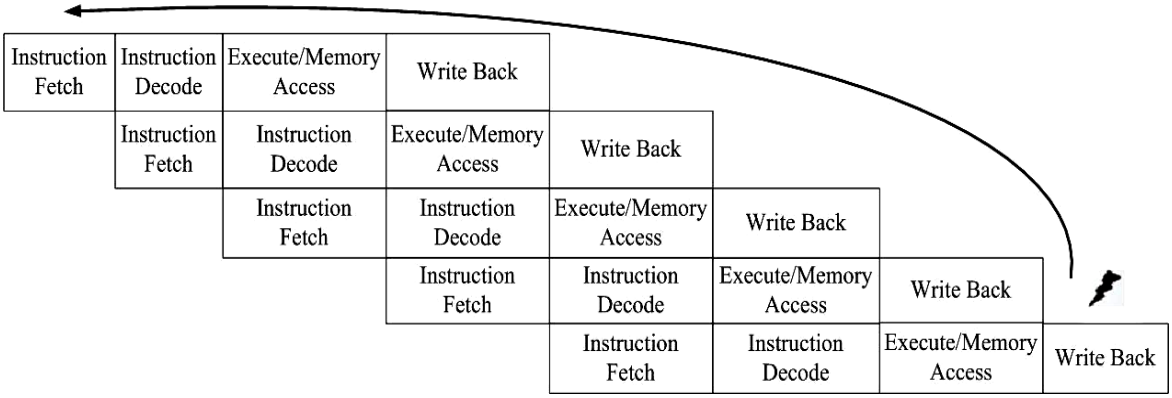


Figure 7.1 Flow chart of SET-induced errors elimination in the pipeline architecture microprocessor.

A number of research works have focused on the approach of built-in current sensors (BICS) on SET detection [93] [94] [95]. Neto, et al. in [93] introduced a SET detection in SRAM cell arrays based on BICS. However, this solution does not work properly for combinational logic, because the BICS must be connected to the power lines and ground lines, which cannot effectively differentiate the currents between internal signals propagating through the logic and that from the SETs. For this reason, a modified BICS was proposed in [43]. During the normal operation, the current in the bulk is approximately zero and the output is constant. When an energetic particle generates a current in the bulk, the voltage change in the bulk will transfer to the output and make the

latch flip to the opposite state, indicating that a current from the IC bulk was detected. However, there are still some problems in this approach. First, The DC path existing in the circuit can increase the power consumption dramatically. Second, the current sensor needs two opposite reset signals at the same time. The reset circuit will increase sensor complexity as well as overhead area. A new design of a voltage mode and a current mode BICS for SET detection are proposed in this chapter, aimed to solve the weakness in the previous designs.

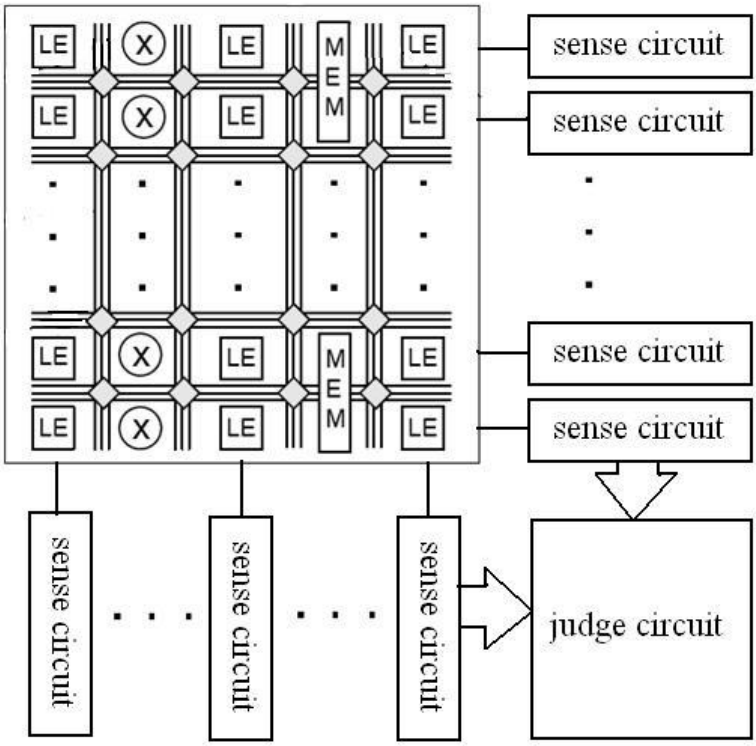


Figure 7.2 Diagram of the SET-induced errors detection and location in FPGAs.

7.2 Voltage Mode Bulk Built-In Current Sensing Circuit for Single-Event Transient Detection

As mentioned in Chapter 2, a current pulse induced by the energetic particle can either lead the pMOS transistor's bulk to a voltage less than V_{dd} or the nMOS transistor's bulk to a voltage greater than GND, depending on charging or discharging of the hit node. Consequently, the current sensors built in n-bulk and p-bulk should be designed separately. Fig. 7.3(a) shows the n-bulk BICS schematic and its working principle. The sensor is composed of a sensing cell followed by an asynchronous latch composed by M_{3-6}. The outputs of the latch out_n and out_n_bar are initialized to zero and one respectively by giving a high voltage reset signal. The body-ties of the nMOS transistors being monitored are connected to GND through transistor M_1.

During normal situation (no particle strike) the current flowing through M_1 is negligible and the logic state of the gates of M_2 and M_8 are at GND level. As a result, the voltage of the body-ties should be zero. A reset signal is given at first and thus the latch circuit maintains a state where the out_n is zero and the out_n_bar is one. When an energetic particle strike occurs, bulk current from nMOS of circuit under test (CUT) charges the equivalent gate capacitors of M_2 and M_8 leading M_2 and M_8 to turn on and then flip the latch to the opposite state. The output out_n will change from logic zero to logic one and be latched until the system is given a reset signal. In the circuit, M_2 and M_8 are the control transistors to read the data into the latch. To make sure the latch can be flipped, the size of M_2 and M_8 should be relatively large while the size of latch circuit can be relatively small. The voltage change at the bulk can be amplified only if the gate voltages of M_2 and M_8 reach their threshold voltages. Consequently, the size of M_1

cannot be too large to avoid pulling down the voltage change. A similar design could be used to detect particle strikes at the pMOS transistors, as shown in Fig. 7.3(b). The layout view of n-bulk BICS and p-bulk BICS SET detection circuit is shown in Fig. 7.4. The total chip area is $9.1 \times 4.5\mu m^2$ in 90nm CMOS technology.

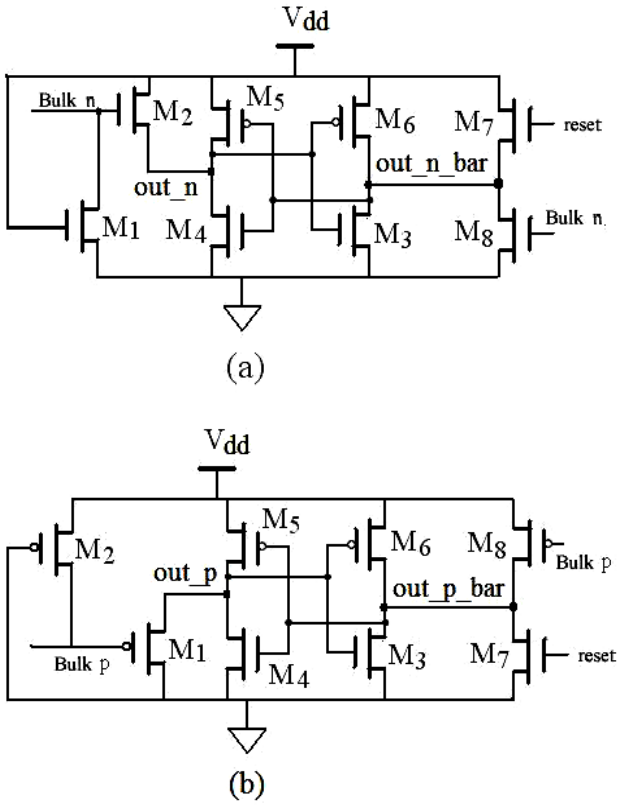


Figure 7.3 (a) Schematic of the voltage mode n-bulk BICS detection circuit to detect SETs. (b) Schematic of the voltage mode P-bulk BICS detection circuit to detect SETs.

An inverter with a minimal size representing the general logic circuit is used as a CUT to exemplify the ability of the bulk-BICS detecting SETs in combinational logic circuits. The circuit is implemented using TSMC 90nm CMOS technology. The length of the pMOS transistor is 100nm and transistor channel width is 400nm, while the nMOS transistor width is 200nm.

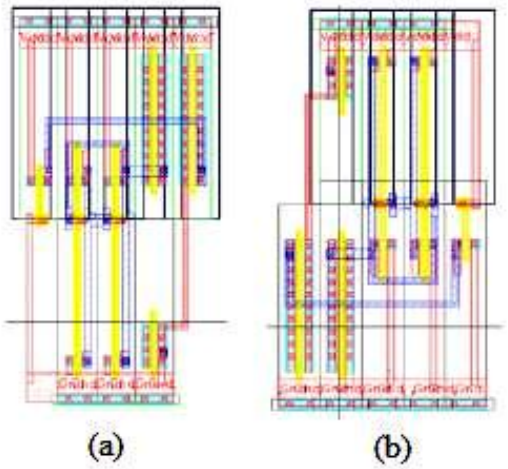


Figure 7.4 (a) Layout view of the voltage mode n-bulk BICS detection circuit. (b) Layout view of the voltage mode P-bulk BICS detection circuit.

Different circuit scales can be used with different parameter values of "multiplier" in the property of nMOS/pMOS transistor. For example, 100 of "multiplier" means the CUT includes 100 transistors having the same dimension. To verify the design, a transient current exponential pulse with 100ps of rising time, 550ps falling time, and 200μA in magnitude is injected at the output node of the CMOS invert. The simulation result is shown in Fig. 7.5. By increasing the number of transistors, it has been confirmed that a single bulk-BICS can monitor at most 50 pMOS transistors with 400nm width and 100 nMOS transistors with 200nm width. This is mainly because the large capacitance connected to the sensing circuit decreases the voltage change needed to trigger the SET detection and extends the delay time between particle hit and SET detection by the bulk-BICS, as shown in Fig. 7.6. Besides, the power consumption for this design is negligible compared with previous work because the current in the bulk BICS during normal situation is approximate to zero.

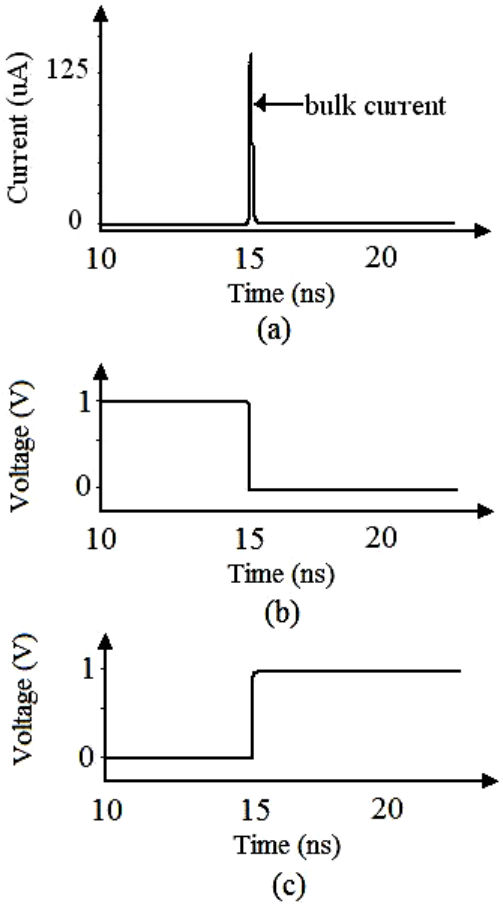


Figure 7.5 SET detection simulation results with voltage mode. (a) SET-induced current flows in/out through the bulk. (b) Signal of out_p in Fig. 7.3(b). (c) Signal of out_n in Fig. 7.3(a).

It is obvious that the drawback of the voltage mode bulk BICS is the size of transistor M_1 in the n-bulk BICS or M_2 in the p-bulk BICS limits the number of transistors in the CUT. To guarantee the normal operation of the CUT, which keeps the reverse-biasing of pn-junction in nMOS and pMOS, the size of the transistor M_1 cannot be too small. However, for a relatively large size of transistor M_1, the voltage increase induced by SETs may not be sufficient to flip the latch. The area overhead (area of bulk BICS circuit divide by area of CUT) is around 20-30 percent. With this approach applied

in the radiation tolerant microprocessors, many of BICS detection circuits must be implemented and spread across the die to ensure a complete detection.

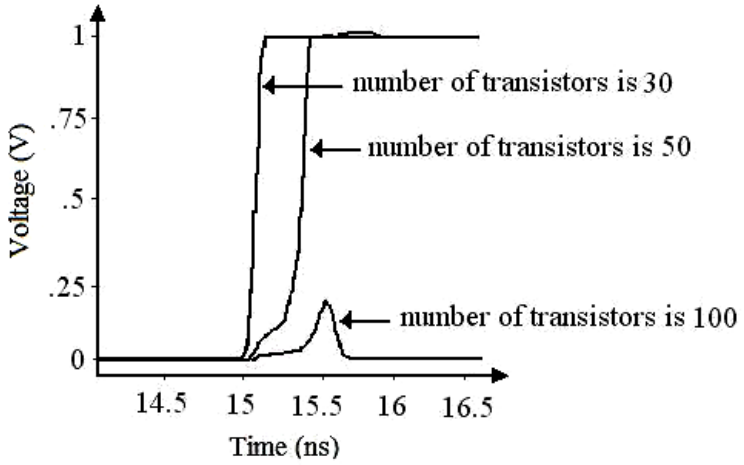


Figure 7.6 Impact of transistor number on SET detection with voltage mode n-bulk BICS.

7.3 Current Mode Bulk Built-In Current Sensing Circuit for Single-Event Transients Detection

A new current mode bulk BICS is applied to overcome the drawback mentioned in the voltage sensing approach. Instead of utilizing bulk current to charge or discharge an equivalent capacitor of MOS transistors in order to get a voltage variation to trigger the latch, a circuit of current conveyor [96] with current amplifier is inserted between the latches. This design includes three parts: the current conveyor, the amplifier, and the latch, which is shown in Fig. 7.7. A simple current conveyor application is current bias generation which is independent of the power supply variation and ground fluctuation [50]. An important application of a current conveyor is a sense amplifier in SRAMs [97].

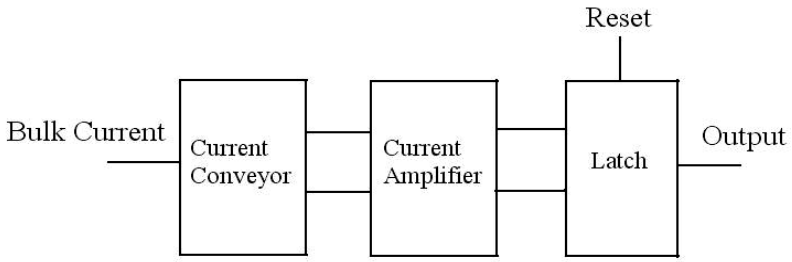


Figure 7.7 Block diagram of the proposed current mode BICS sensing circuit.

The schematic of the current mode bulk BICS sensing circuit is shown in Fig. 7.8. In Fig. 7.8(a), the current conveyor circuit is composed of the transistors M_{1-8}. The drain of M_1 is connected to the bulk of pMOS transistors of the CUT. Similar to the voltage mode bulk BICS detection circuit, the bulk potential of pMOS transistors of CUT is set to V_{dd} through M_1. M_2 is added to obtain the symmetrical potential between the "bulk p" and "bulk ref" at the drain of M_2. The functionality of the cross couple transistors of $M_{3,4}$ and two pseudo transistors of $M_{5,6}$ is not only to isolate the relative large capacitance at the node of "bulk p", but also to transfer the current from the source of M_3 to the drain of M_5. A pair of differential voltage signals at the drain of M_5 and M_6 are generated with the load of M_7 and M_8. The next part is the amplifying stage consisting of transistors M_{9-15}. The amplification stage includes a differential amplifier with current mirror M_{9-12} and the common-source amplifier M_{13-14}. Through the amplifier stage, the current detection sensitivity is greatly increased. The last stage is a latch built by M_{16-20}. Once the circuits are powered up, a pulsed-reset signal sets the state of the latch to a known logic. In Fig. 7.8, the logic state of the output is low at the initial state. The bulk current induced by SETs is detected by the current conveyor and amplified by the current amplifier and the output of the latch is flipped to high. Fig. 7.9 shows the circuit detecting the bulk current from nMOS and pMOS transistors. Similar to the test environment in the voltage mode,

more than 2,000 transistors affected by SETs can be detected using a single sensing circuit.

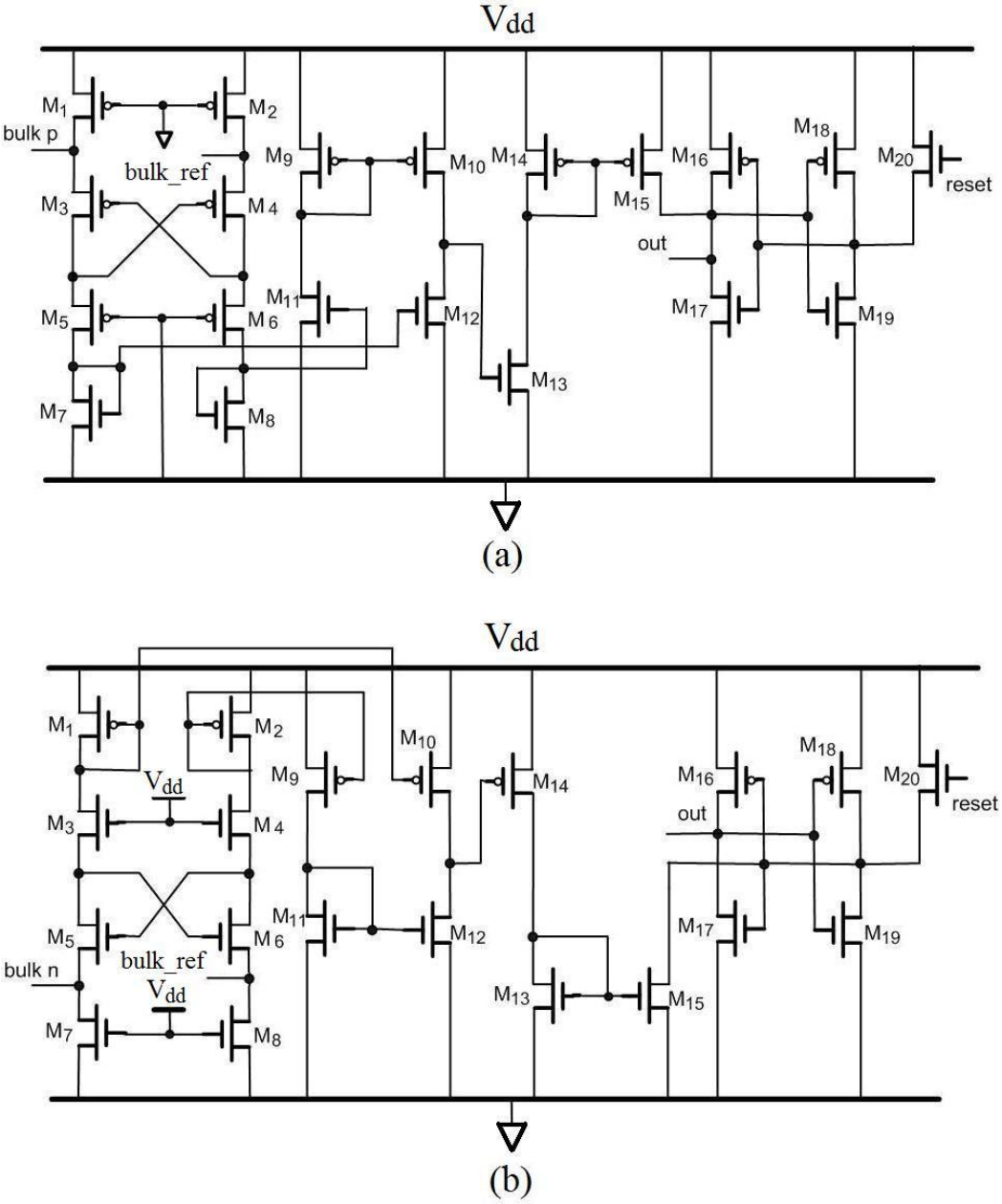


Figure 7.8 (a) Schematic of the current mode p-bulk BICS detection circuit to detect SETs. (b) Schematic of the current mode n-bulk BICS detection circuit to detect SETs.

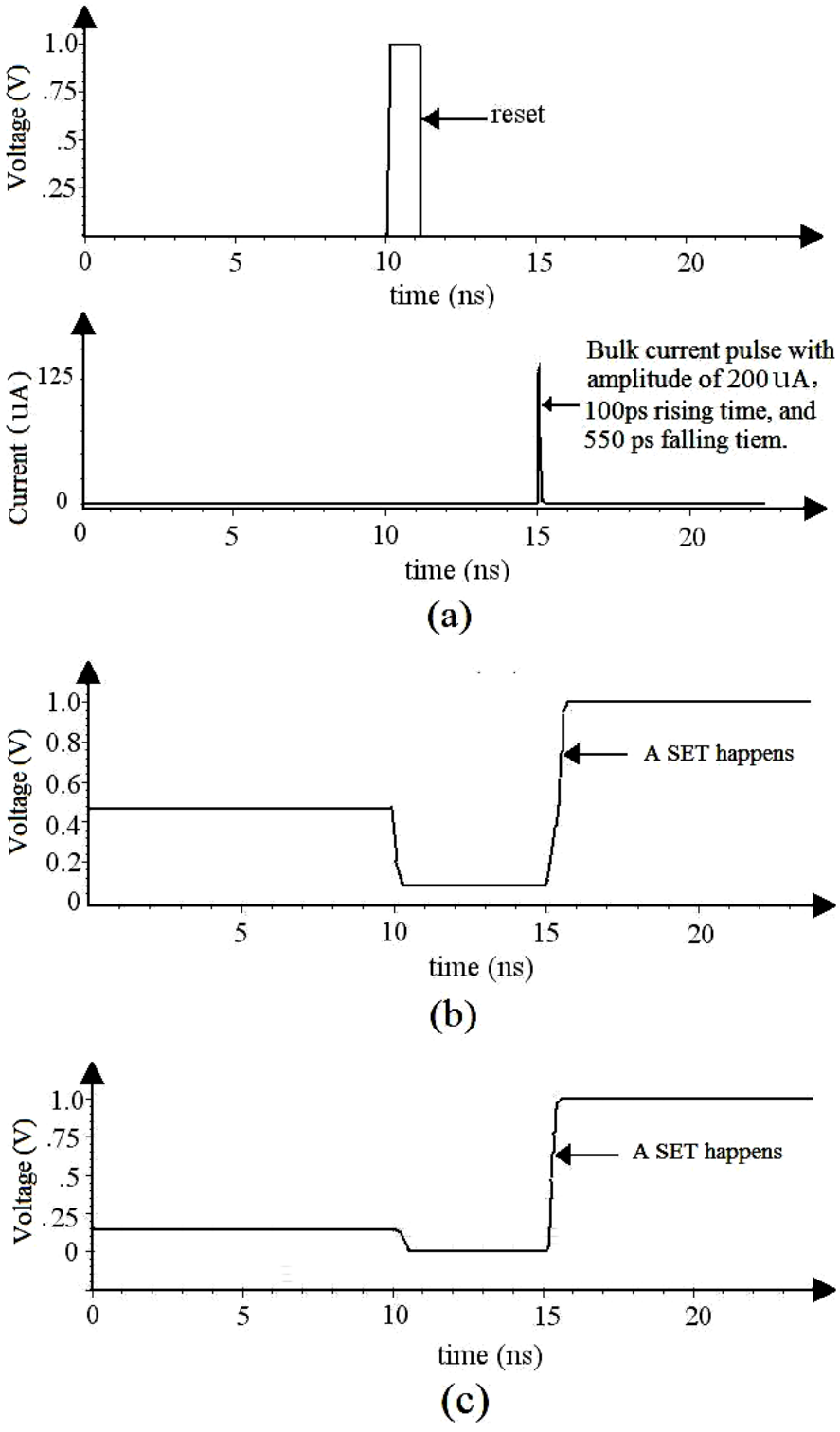


Figure 7.9 (a) Reset signal and SET-induced current pulse. (b) SET detection simulation result for current mode n-bulk BICS. (c) SET detection simulation result for current mode p-bulk BICS.

A 4-bit multiplier is used as a test vehicle in this work since the multiplier is a typical combinational logic circuit. One n-bulk BICS and one p-bulk BICS circuits are used to detect SETs in the nMOS and pMOS transistors, respectively. A set of current pulses is injected into the sensitive nodes to simulate SETs that may be propagated to the outputs. Simulation results show that one n-bulk BICS and p-bulk BICS circuit can sufficiently detect the SET pulses in the 4-bit multiplier. However for the voltage mode sensing circuits, 3 n-bulk BICS and 5 p-bulk BICS sensing circuits are needed to detect all of the transistors in the multiplier. The die size is 80μm^2 and shown in Fig. 7.10.

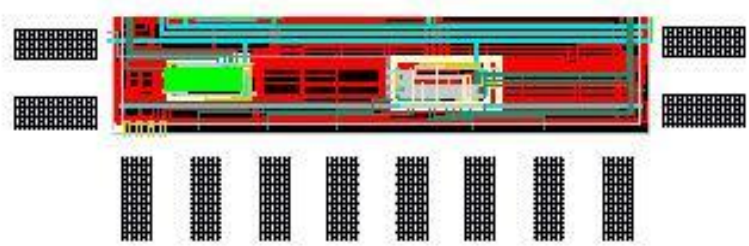


Figure 7.10 Die photograph of the BICS sensing circuit.

7.4 Summary

Aiming to reduce the power consumption and area overhead, a new design of voltage mode of the bulk BICS to detect SETs was developed. Simulation results indicate that efficiency and applicability of the bulk BICS of this work are improved while the power consumption is reduced. A novel current mode sensing approach to detect SETs is introduced which can greatly reduce the area overhead and increase the sensitivity of the sensor. Designs were verified by a 4-bit multiplier with TSMC 90nm CMOS technology using Cadence simulation tools.

8. Summary, Conclusion and Future Work

8.1 Summary

With device scaling down, analog ICs have received increasing attention in the radiation effect research community. This dissertation studies SET effects on analog CMOS circuits and presents RHBD approaches for these circuits. The target circuits are op amps, dynamic comparators, LC-tank oscillators, and PLLs since they are the typical circuits in analog building blocks. Studies of SET effects on these circuits include design and simulation, SET sensitive analysis, RHBD approach, implementation, functional testing, laser verification, and comparison between with RHBD and without RHBD designs. All of the designed circuits are simulated, laid out, and taped out using Cadence tools with STMicroelectronic 90nm CMOS process or TSMC 90nm CMOS process. CAD tools and fabrications are supported by CMC Microsystems. To verify SET effects, laser experiments were performed on the dynamic comparator and the LC-tank oscillator at the Saskatchewan Structural Sciences Centre (SSSC). Experimental results match theoretical analysis and simulation results.

For the op amp, three approaches of auto-zeroing cancellation techniques to mitigate SET effects are presented and implemented in the op amp. Simulation results with a current pulse striking at the critical circuit nodes indicate that the duration of SET effects is shorter than the cancellation period. In this way, when there are erroneous signals introduced by SET effects, these erroneous signals are limited to a short period of time. This approach can be applied to RHBD designs such as switch-capacitors and ADCs.

For the dynamic comparator, transistors can be implemented using dual-well or triple-well process technology to mitigate SET effects. Previous work has been performed using simulations or data from either dual-well or triple-well technology, but not from both. In this dissertation, for the first time, laser experiments on a circuit fabricated on a single die using triple-well and dual-well structure in a 90nm CMOS process are presented.

For the LC-tank oscillators, the device can be biased in current-limited or voltage-limited regimes. Both simulation and experimental results show that the bias current profoundly affects the SET tolerance of the LC-tank oscillator. From SET-tolerant point of view, the oscillator performs better in the voltage-limited regime than in the current-limited regime with the cost of higher power consumption. If the oscillator must be biased in the current-limited regime, an additional decoupling resistor in series with the tail transistor should be added to mitigate the SET effects. The decoupling principle introduced in this example can be used for other biasing circuits to reduce SET effects.

Not only TMR is used in the RHBD digital designs, but also in the analog and mixed signal circuits and systems such as PLLs. Many of previous RHBD PLL works focused on some of the sub-blocks such as CP or ring oscillator. SET sensitivity analysis and improvement methodologies based on these sub-blocks were presented. However, PLL is a functional system rather than a simple circuit. SET effects from the sub-blocks affect the characteristics and performances of the output signal. In this way, a new SET mitigation approach in PLLs based on TMR is presented. The other advantage of this method is that it prevents signal frequency from shifting under SET effects so that the PLL do not need to re-track the reference frequency again when a SET event occurs. This approach can also be extended to other RHBD analog and mixed signal circuit designs.

The presented technique for SET detection has a potential application in the radiation-hardened digital ICs. In addition to the work on SET on analog circuits, new designs of voltage mode and current mode of the bulk BICS to detect SETs were developed. Simulation results indicate that the bulk BICS of this work can increase detecting efficiency with a reduction in power consumption and overhead area.

Based on the testings involving the dynamic comparator and the LC-tank oscillator, experimental results can be well explained by schematic simulations. The results demonstrate that the SET analysis on those particular circuits are correct and thereby illustrate that those RHBD methods are effective in mitigating the effects of SET. These RHBD approaches are not only working for one particular circuit but also provide guidance for designing SET-tolerant analog circuits in radiation environments. For example, the circuit should be implemented either with dual-well or triple-well process technology depending on the circuit topology. Also, the RHDB design with the insertion of a resistor between the SET sensitive node and the rest of the circuit is simple and effective in analog RHBD designs. RHBD PLL design demonstrates that the TMR approach is not only a method to mitigate SET effects in digital circuits but also an effective way for the mixed-signal RHBD design. Shortcoming of the TMR approach used in the PLL circuit is the introduction of extra phase noise. However, there are two distinguishing points of this RHBD PLL design from previous designs: First, this approach prevents the signal frequency from shifting under SET effects rather than correcting the frequency after SETs have happened. Second, this approach is analyzed and implemented based on the system point of view rather than one of the sub-function blocks in the PLL.

8.2 Conclusion

1. The signal amplitude and the signal state during transition time are sensitive to SET effects. Signal amplitude of the op amp is distorted under SET effects. Variation in signal amplitude and phase-shift depend on the temporal location of the single-event hit in the LC-tank VCO. SET effects cause burst change of signal frequency in the PLL. In summary, SETs have different impacts on each individual analog circuit in terms of signal amplitude and state. Depending on what type of analog circuits, particular issue and solution must be targeted when developing RHBD approaches.
2. This work characterizes SET effects in different process technologies, such as dual-well process and triple-well process. Triple-well results in higher vulnerability for p-hits due to lower electron mobility, while results in lower vulnerability for n-hits due to lower charge collection. Also, experiment results show that the upset laser energy threshold is a strong function of circuit topology. Devices implemented with triple-well or dual-well in this example can be used for other circuits to mitigate SET effects.
3. Instead of studying only one particular analog circuit and introducing one particular RHBD approach, the work is based on multi-level, namely system, circuit, or transistor to mitigate the SET effects on various analog circuits. The SET mitigation proposed methods are not only used in the circuits in this dissertation but also can be applied to other RHBDs. For example, a physical decouple resistor which isolates the circuit from SET source can be used in the bandgap reference and other bias circuits. The use of TMR in this work

illustrates that this approach is not only used in digital circuits but also can be applied in analog and mixed signal design.

4. SET detection circuits provide a unique approach for system-level RHBD. A practical characteristic of this design is the real-time SET detection with low power consumption and low area overhead. This technique can be applied to FPGAs and microprocessors to detect SET events in order to develop efficient mitigation strategies.
5. The pulsed-laser experiment demonstrates to be an effective, low cost, and convenient method to study the SET effects on integrated circuits. In this work, the results from SPICE simulations and pulsed-laser experiments agree with each other and thus validates performances and effectiveness of the proposed SET mitigation approaches.

8.3 Future Work

There are two categories for future explorations. Because op amps and comparators are the fundamental sub-blocks of the ADC design, the RHBD approaches in op amps and comparators can be extended and utilized in RHBD ADC. A typical flash ADC is shown in Fig. 8.1. The RHBD comparator discussed in the work can be implemented in each of the comparator-blocks. Also, the PLL in Chapter 6 is an integer N PLL. In practical applications, such as wireless communications, fractional N PLL is frequently used. The RHBD LC-tank oscillator in Chapter 5 can be used and the TMR approach can be realized in the fractional N PLL since the Delta-Sigma frequency divider is usually implemented using digital circuits.

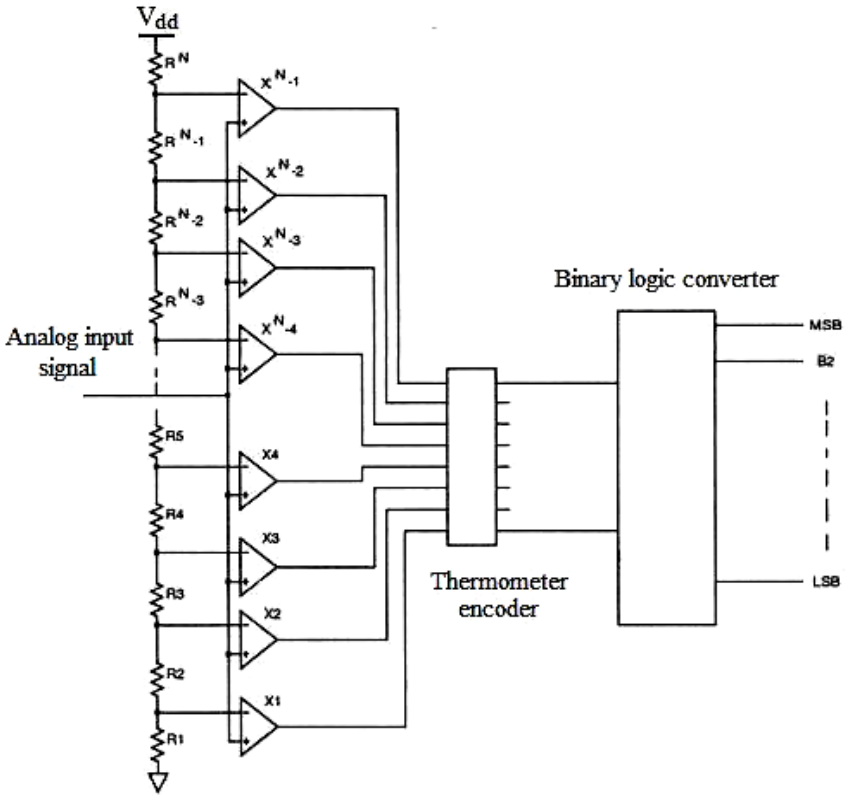


Figure 8.1 Architecture of a typical flash ADC.

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