HIGH LINEARITY UNIVERSAL LNA DESIGNS FOR NEXT GENERATION WIRELESS APPLICATIONS

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By

ZHICHAO ZHANG

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ABSTRACT

Design of the next generation (4G) systems is one of the most active and important area of research and development in wireless communications. The 2G and 3G technologies will still co-exist with the 4G for a certain period of time. Other applications such as wireless LAN (Local Area Network) and RFID are also widely used. As a result, there emerges a trend towards integrating multiple wireless functionalities into a single mobile device. Low noise amplifier (LNA), the most critical component of the receiver front-end, determines the sensitivity and noise figure of the receiver and is indispensable for the complete system. To satisfy the need for higher performance and diversity of wireless communication systems, three LNAs with different structures and techniques are proposed in the thesis based on the 4G applications.

The first LNA is designed and optimized specifically for LTE applications, which could be easily added to the existing system to support different standards. In this cascode LNA, the nonlinearity coming from the common source (CS) and common gate (CG) stages are analyzed in detail, and a novel linear structure is proposed to enhance the linearity in a relatively wide bandwidth. The LNA has a bandwidth of 900MHz with the linearity of greater than 7.5dBm at the central frequency of 1.2GHz. Testing results show that the proposed structure effectively increases and maintains linearity of the LNA in a wide bandwidth. However, a broadband LNA that covers multiple frequency ranges appears more attractive due to system simplicity and low cost. The second design, a wideband LNA, is proposed to cover multiple wireless standards, such as LTE, RFID, GSM, and CDMA. A novel input-matching network is proposed to relax the tradeoff among noise figure and bandwidth. A high gain (>10dB) in a wide frequency range (1-3GHz) and a minimum NF of 2.5dB are achieved. The LNA consumes only 7mW on a 1.2V

supply. The first and second LNAs are designed mainly for the LTE standard because it is the most widely used standard in the 4G communication systems. However, WiMAX, another 4G standard, is also being widely used in many applications. The third design targets on covering both the LTE and the WiMAX. An improved noise cancelling technique with gain enhancing structure is proposed in this design and the bandwidth is enlarged to 8GHz. In this frequency range, a maximum power gain of 14.5dB and a NF of 2.6-4.3dB are achieved. The core area of this LNA is 0.46x0.67mm^2 and it consumes 17mW from a 1.2V supply.

The three designs in the thesis work are proposed for the multi-standard applications based on the realization of the 4G technologies. The performance tradeoff among noise, linearity, and broadband impedance matching are explored and three new techniques are proposed for the tradeoff relaxation. The measurement results indicate the techniques effectively extend the bandwidth and suppress the increase of the NF and nonlinearity at high frequencies. The three proposed structures can be easily applied to the wideband and multi-standard LNA design.

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LIST OF ABBREVIATIONS

BPF	Bandpass filter
BW	Bandwidth
CDMA	Code-Division Multiple Access
CG	Common-Gate
CMOS	Complementary Metal-Oxide Semiconductor
CS	Common-Source
GPS	Global Positioning System
DCS	Digital Cellular Service
DS	Derivative Superposition
GSM	Global System for Mobile Communications
HSPA	High Speed Packet Access
IIP3	Third-order Input Interception Point
IMT-Advanced	International Mobile Telecommunications Advanced
ITU	International Telecommunication Union
ITU-R	ITU Radiocommunication Sector
LAN	Local Area Network
LNA	Low-Noise Amplifier
LO	Local Oscillator
LTE	Long Term Evolution (LTE)
MDS	Modified Derivative Superposition
MEMS	Micro-Electro-Mechanical Systems
MIM	Metal insulator Metal
NF	Noise Figures
PCN	Personal Communications Network
PCS	Personal Communications Service
RF	Radio Frequency
RFID	Radio Frequency Identification

SNR	Signal-to-Noise Ratio
UMTS	Universal Mobile Telecommunications System
UWB	Ultra-wideband
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	WiFi Local Area Network

CHAPTER 1

INTRODUCTION

Communication and semiconductor technologies are undergoing continuous improvement due to the demands of numerous applications. To make wireless communication systems compatible and efficient, numerous standards have been developed. In the past, standards were based on the need for applications and on bandwidth allocation. Such standards are categorized as a different generation of cellular communications [1-4], Radio Frequency Identification (RFID) [5-7], Global Positioning System (GPS) [8-13], WiFi Local Area Network [14-16], Zigbee [17-20], and Bluetooth [21-23]. Since the early 1990s, new wireless communication standards, transmitting in the gigahertz range, have become popular, one of such standards is GSM and the market for this standard has exploded. Most standards are co-existing because systems, devices, and applications are not quickly changing to the new standard system. The cost of building a device and a system that is compatible for each standard is very high. There is a demand for a single system (or handset in the case of consumer wireless communications) that has the ability to support multiple standards over a wide range of frequency bands [24]. A highly integrated and low cost solution for the multi-standard handset is attracting research interest. Wireless communications and semiconductor technologies, in particular CMOS, play a key role in finding solutions for the current and future handsets for wireless applications.

1.1 The CMOS Technology

Until the late 1980s, large-scale integrated circuit technology was thought to be inapplicable for wireless communication devices. Radio frequency circuits are implemented by adopting

discrete components, such as transistors, inductors, capacitors, and resistors. These components are optimized for high frequency applications and the circuits are bulky and expensive [25]. The advances of microelectronic technology bring more integrated circuits into wireless communication devices and systems. One of such technology is the Complementary Metal-Oxide Semiconductor (CMOS). The CMOS process of fabricating devices is advanced enough that any device and system can be implemented for wireless communication applications.

CMOS technology is becoming an attractive solution due to its low cost and high level of integration. As the size of the transistor gets smaller, according to Moore Law, the technology is more applicable to high-speed circuits. The peak unity-current-gain frequency (f_T) for the CMOS transistor is now higher than 400GHz in the 65nm CMOS [26]. This frequency increases as the transistor size is shrinking. The maximum oscillation frequency, f_{max}, which determines the highest working frequency for the active devices, has exceeded 200GHz and 100GHz for 65nm and 0.13μm CMOS technologies, respectively [27,28]. Noise figure (NF) is one of the most important parameters of an active device. The minimum device NF for CMOS 0.13μm technology is around 0.7dB at 5GHz [29]. To minimize NF, many optimization methods with specified quality factor *Q* and power consumption have been proposed.

The other technologies such as 0.18μm and 90nm CMOS are also widely adopted for analog and RF implementations because of their excellent technological performances. In addition to active devices, the realization of on-chip passive elements in CMOS, such as the MIM capacitors [30] and spiral inductor [31] also increases the device speed and reduces the size and cost of the wireless communication systems. A huge number of highly performed CMOS RF circuits and subsystems has been designed and fabricated in last few years [32-36]. To compare the

performance of different technologies, Table 1.1 is included. The CMOS 0.13μm technology will be the targeted process for this work due to its good technology performance and low fabrication cost. In addition, the included passive elements library in the available design tools makes the parameters extraction more convenient and accurate.

Table 1.1 Mixed-Signal and RF CMOS Process Overview

	0.18μm	**0.13μm**	**90 nm**	**65nm**
DC Supply (V)	1.8/3.3	1.2/2.5, 3.3	1.0/1.2/1.8/2.5/3.3	0.9/1.0
Metal Layers	6	8	9	8
$V_{t\_}N$, $V_{t\_}P$ (V)	0.40, -0.48	0.34, -0.36	0.54, -0.51	0.29
Low-V_t (V)	0.24, -0.30	0.24, -0.27	0.3	0.2
NMOS f_t (GHz)	60 (Vds=1.8V)	80 (Vds=1.2V)	100	360
NMOS f_{max}(GHz)	65 (Vds=1.8V)	>100 (Vds=1.8V)	150	420
PMOS f_t (GHz)	23	40	60	238
PMOS f_{max}(GHz)	38	60	>110	295
NF_{min} @ 2.4GHz	1.4 (Vds=1.8V, Vgs=1V)	=<1.4 (Vds=1.8V, Vgs=1V)	0.8 (Vds=1.0V, Vgs=0.7V)	0.4dB at 2GHz
Deep N-well	Yes			

1.2 The Need for Multi-standard Mobile Terminal

Over the past decade, a high number of wireless communication standards have been proposed and implemented. In 2004, the ITU-R [37] specified the International Mobile Telecommunications Advanced (IMT-Advanced) requirements for 4G standards. The peak speed for 4G service can reach up to 100Mbit/s in fast moving communications, such as trains or cars. For slow moving communications, such as pedestrians and stationary users, the data speed can be

as high as 1Gbit/s [38]. The 4G standard opens a new door for advanced wireless applications, such as video chatting, web browsing, and online gaming. Pre-4G technologies such as mobile's WiMAX and Long Term Evolution (LTE) have been on the market since 2006 and 2009 [39, 40]. Although the current use of LTE and WiMAX is often branded as 4G, their downloading and upstream peak bitrates are just 144Mbit/s and 100Mbit/s, respectively. Currently, design and development of the next generation systems (i.e., 4G) is one of the most active and important areas of research and development in the wireless communication world.

Various wireless communication standards have already been proposed and used before the emergence of 4G. This is due to the limited frequency resource and the increasing demand for high-speed applications. The Global System for Mobile Communications (GSM) is a standard that was developed by the European Standards Committee. The original version of GSM was used in the 900MHz band throughout Europe. The 1800MHz band, originally called Personal Communications Network (PCN) [41], was added for the up-band version of GSM. The PCN was later renamed to Digital Cellular System at 1800MHz (DCS1800) [42]. After that, the Enhanced-GSM version was created by adding extra 10MHz frequency to both receiver and transmitter lower bands.

In the United States, the 1900MHz band was chosen for applying the European GSM and named PCS1900 [43]. PCS1900 is an evolution of the GSM900/DCS1800 European cellular systems for the 1.9GHz North American emerging technologies. The Wideband-CDMA (Code-Division Multiple Access) [44] is a technology for wideband digital radio communications for internet, multimedia, video, and other capacity-demanding applications. WCDMA is the dominating 3G technology, providing higher data rates to increase capacity for voice and video applications. WCDMA's peak speed can reach up to 2Mbps for local area access and 384Kbps for

wide area access. A new version of the WCDMA is going to be released where the speed can reach up to more than 10Mbps. WCDMA is also known as the Universal Mobile Telecommunications System (UMTS) and has been adopted as a standard by the International Telecommunication Union (ITU) under the name IMT-2000 direct spread [45]. For a smooth transition from 3G and 2G to 4G technology, the next generation wireless systems and devices must simultaneously support all the mentioned existing wireless standards.

Besides mobile wireless communications, other applications, such as Global Positioning System (GPS), Wi-Fi Local Area Network (WLAN), Radio Frequency Identification (RFID), and Bluetooth have been widely used and continue to evolve. This leads to a very desirable prospect for a multiple radio functionalities mobile terminal to support different application standards. Thus, next generation wireless communication devices will require new designs and innovative solutions to create multi-band handsets with low power consumption at the least cost. Such devices should include a transmitter and a receiver comprised of an essential component, a low noise amplifier (LNA).

1.3 A Universal Radio Receiver and LNA

In the recent years, most of the multi-band handsets were built by combining individual receivers that optimized for individual standards. This technique required larger chip areas, higher cost, and higher power consumption not mentioning the complexity of the interface between the receivers. In order to realize a high level of integration, many wireless communication standards should be integrated into a single hardware system. The single receiver, which can be called “Universal Radio Receiver”, can be reconfigured for different wireless applications. The size and cost of the receiver are then dramatically reduced.

The basic concept of a universal radio receiver is shown in Figure 1.1. The circuits of the universal radio must work across a wide frequency range and have to meet the performance specifications required by the individual standards [46, 47]. This is the main difference from the previous multi-standard receiver designs in which each building block is optimized and dedicated for one specific standard. For the universal receiver, the zero-intermediate frequency (or direct-conversion) architecture is much preferred because the carrying frequency of the received signal is down-converted to zero. Compared to the traditional super-heterodyne architecture, the direct-conversion structure have more inherent advantages, such as lower complexity, low power consumption, no image frequency, and easier to be reconfigured.

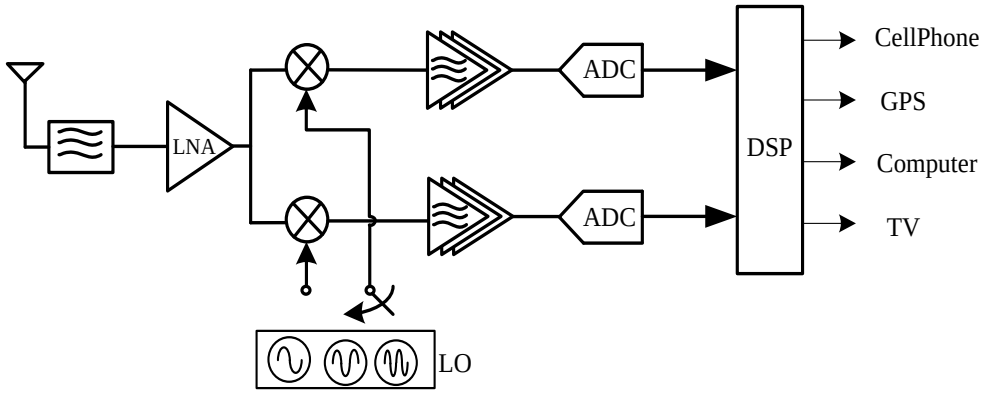


Figure 1.1 Illustration of a universal radio for multiple standards [46]

In addition to direct-conversion receivers, there is another attracting architecture candidate called “Digital RF” [48]. By adopting the high-speed sampling and processing techniques, a series of traditional analog blocks in the heterodyne receiver, such as mixer and filtering, are being replaced by their digital counterparts [49-50]. This technology is getting more popular because of the continuous scaling of CMOS technology with higher switching speed. The main

drawback of the digital RF is that the high-speed sampling technique introduces more noise to the received signal. The signals need to be pre-processed to increase the Signal-to-Noise ratio before sending to the next stages to suppress the noise. Therefore, the low noise amplifier remains indispensable for either architecture of a universal receiver. There is no demodulation scheme in wireless communications that can eliminate the need for an LNA.

In order to be part of a high performance receiver, the LNA must have certain characteristics. The most decisive characteristics of LNA are its amplifying gain, bandwidth, noise figure, and linearity. Noise Figures (NF) and sensitivity of the receiver (or system) depend strongly on the NF and gain of the LNA used at the front end. In addition, the nature of the LNA's transfer function and its reverse isolation affects the overall system linearity. A wideband LNA that can cover multiple standard bandwidths is very attractive to the development of devices and systems for future generations of wireless communications. By definition, when the bandwidth of the circuit is larger than 10% of the center frequency, it is called wideband. However, designing such an amplifier poses numerous challenges which will be addressed in the thesis in the subsequent chapters.

1.4 Research Goals and Contributions

From the concept of sharing a single LNA for a universal receiver, this research targets on the design of multi-standard LNAs suitable for 4G wireless communications and other applications such as GSM, WCDMA, WLAN, etc. Based on the realization for the 4G applications, three LNAs targeting different spectrums are designed, as shown in Figure 1.2.

1. The most economical way to upgrade existing devices to support 4G application is to design a receiver that specific for the 4G and combine it with the existing system. Since LTE is the

most widely used standard for 4G applications, the first LNA is mainly designed to fulfill the basic LTE standard. The RFID (860-969MHz) and GSM (865-960MHz) spectrums are also covered since they are located in the neighboring bands.

2. Combining different circuit blocks that are optimized for specific standards makes the device bulky and expensive. Sharing circuits is the best way to maximize the integration level. A LNA that can support different cellular technologies (4G/3G/2G) and other local wireless standards (WiFi/Bluetooth) is highly desired in creating a smooth transition between different communication generations. A wider bandwidth LNA, which covers nearly all the existing wireless frequency ranges, will be proposed in the second design.

3. Although LTE is generally considered to be the dominant wireless technology of the future, WiMAX, the other candidate for 4G, is another promising technology. However, there is no uniform global licensed spectrum for WiMAX, the spectrums are very fragmented and vary from country to country as shown in Figure 1.2. The third design implements the first wideband multimode LNA for 4G wireless applications that covers both the LTE and WiMAX frequency ranges.

This thesis work contributes to the advancement of multi-standard LNAs for the next generation of wireless communications. The works also provides a smooth transition between generations and/or allows the co-existence of different standards in a cost effective way. Unlike the narrow-band LNA, co-existing of different signals in a single device can interfere with each other and degrade the receiver sensitivity. Linearity of the new LNA must be excellent in order to provide good performance for multi-standard devices. Although numerous techniques have been proposed for enlarging the LNA bandwidth, unfortunately, the noise also proportionally increases

with the bandwidth. Keeping the noise within an acceptable level while increasing the LNA bandwidth is a challenging task.

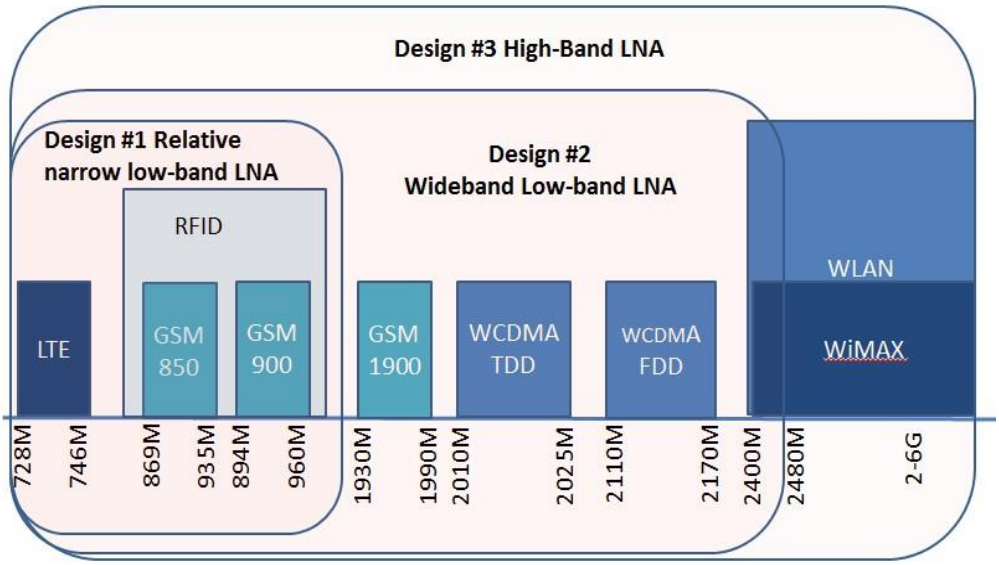


Figure 1.2 Frequency spectrum bands of different standards.

In addition, the LNA linearity drops quite quickly as the frequency increases. There are very few studies of the linearity improving methods, especially for the wideband LNAs. In this thesis, the tradeoff among noise figure, linearity, and wideband input impedance matching are well addressed. New noise cancelling and linearity enhancing techniques that can be very effective in a wide frequency range are introduced. All the wideband, noise figure, and linearity improving techniques are incorporated and implemented simultaneously to the LNA designs in the thesis.

1.5 Thesis Organization

Following this chapter, Chapter 2 begins with an introduction of the basic performance metrics desired from a LNA, such as the input matching, noise figure, gain, bandwidth, linearity,

and power consumption. Chapter 3 introduces the basic techniques used to improve impedance matching, noise figure, and linearity of the LNA. Some limitations of the precedent analysis approaches are also addressed in this chapter. Chapter 4 reviews the deficiency of the existing distortion characterization method and presents an alternative linearity enhancement approach, targeting the first multi-band LNA ranging from 0.7 to 1 GHz that was described in the first objective. Chapter 5 analyzes the trade-off between the input matching and noise figure in more detail. This chapter also introduces a novel input matching technique for the second LNA (targeting the frequency band from 0.7-2.4GHz). For the third LNA, Chapter 6 presents a modified noise and distortion cancelling LNA prototype. Analysis, synthesis, design, implementation, fabricating, and testing of the three LNA's are included in Chapter 4, Chapter 5, and Chapter 6. Chapter 7 concludes the thesis work and provides direction and discussion for future investigations.

CHAPTER 2

LNA FUNDAMENTAL REQUIREMENTS AND CIRCUIT SPECIFICATIONS

In order for the multimode Low Noise Amplifier (LNA) to be used in a universal receiver, it should not only support different standards bandwidths and simultaneously satisfy other requirements, such as sensitivity, linearity, and noise factor. In this chapter, some of the key performance parameters of a LNA will be discussed, such as input/output impedance matching, gain, noise figure, and linearity.

2.1 Scattering Parameters (S-parameters)

Low-Noise Amplifier (LNA) can be considered as a two-port network, shown in Figure 2.1. The incident wave at each port is indicated by "*a*" while the reflected wave for each port is represented by "*b*". The wave includes both the amplitude and phase information. The relationship between the reflected wave, incident wave, and the S-parameter matrix is given by [51]:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

Expanding the matrix yields:

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad \text{and} \quad b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.2}$$

According to the definition of S-parameters, port2 is terminated in a load identical to the system impedance (Z_0), normally 50Ω, then, by the maximum power transfer theorem, b_2 will be totally absorbed making a_2 equal to zero. Therefore

$$S_{11} = \frac{b_1}{a_1} \qquad \textit{and} \qquad S_{21} = \frac{b_2}{a_1} \tag{2.3}$$

Similarly, if port1 is terminated in the system impedance of 50Ω, then a_1 becomes zero, giving

$$S_{12} = \frac{b_1}{a_2} \qquad \text{and} \qquad S_{22} = \frac{b_2}{a_2} \tag{2.4}$$

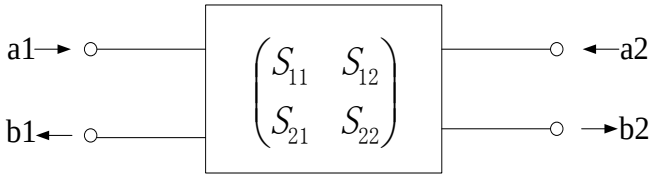


Figure 2.1 Two-port network for S-parameters

For an amplifier, S_{11} indicates the input return loss, which is a scalar measure of how close the input impedance of the amplifier is to the system impedance (i.e., 50Ω). S_{21} indicates the gain of the amplifier. S_{12} and S_{22} are the reverse isolation and the output return loss, respectively. In practice, for convenience, most of the parameters are expressed in decibel (dB) [52]. For example, the dB expression for the S_{11} is 20log(S_{11}). A S_{11} of less than -10dB is considered acceptable. This indicates more than 90% signal energy absorption. For a LNA, the gain, S_{21}, of 10dB is acceptable. The isolation between the input and the output, S_{12}, should be as small as

possible otherwise the output signal will leak into the input as a feedback signal and oscillation may occur making the circuit unstable.

2.2 Impedance Matching

LNA is the first block on the receiver to receive and amplify the incoming signal from the antenna. Before reaching the LNA input, the signal must pass through various components, such as the traces on the PCB, filter or duplexer, package pins, and bonding wires. If the LNA input impedance does not match well with the characteristic impedance of the antenna, the signal energy may reflect back to the antenna and becomes noise. As a result, the input matching is one of the most important parameters for LNA. In addition, the signal energy that is received and amplified by the LNA must be transferred to the subsequent stages for further processing. Therefore, the output of the LNA needs to be connected to other stages that have a low input impedance. In that case, the LNA output impedance also is required to be matched with the input of the preceding stages. As described in Section 2.1, S_{11} is used to indicate the input matching of a LNA and a S_{11} less than -10dB is considered to be acceptable.

One of the most popular LNAs is the inductively degenerated common-source LNA (CS-LNA) [53], shown in Figure 2.2. This amplifier is commonly used in narrow-band applications due to its low NF, ease of input matching, high gain, and low power consumption. The input impedance of this amplifier can be found as:

$$Z_{in} = s(L_s + L_G) + \frac{1}{sC_{gs}} + (\frac{g_{m1}}{C_{gs}})L_s \tag{2.5}$$

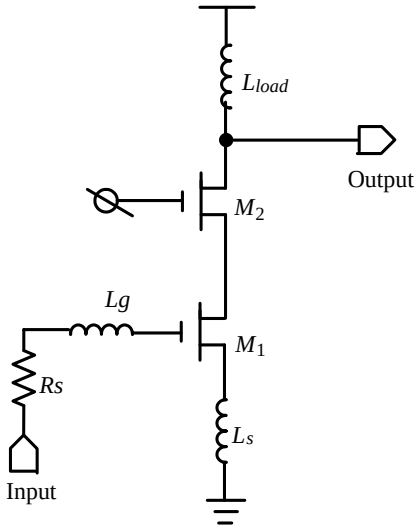


Figure 2.2 Basic cascode topology of the proposed circuit

Even though there is not a real resistor in the circuit, the real impedance $(\frac{g_{m1}}{C_{gs}})L_s$ is formed, this is shown in Eq. 2.5. At the series resonance of the input circuit, the impedance is purely real and proportional to L_s. The real term can be made equal to 50Ω by choosing appropriate value of the inductor L_s. For example, if f_T, which equals to $(\frac{g_{m1}}{C_{gs}})$, is 10 GHz, then a 50Ω impedance requires a L_s of 800 pH.

The gate inductance L_g is being used to compensate for the imaginary part that is caused by the gate-to-source capacitance C_{gs}, this happens once L_s is already chosen to satisfy the criteria of 50Ω input impedance. As a result, the resonant frequency ω_0 of the circuit becomes:

$$\omega_0 = \frac{1}{\sqrt{C_{gs}(L_s+L_g)}} \tag{2.6}$$

For this input series *RLC* network, the quality factor can be expressed as

$$Q = \frac{1}{R_s \omega_0 C_{gs}} \tag{2.7}$$

For low frequency circuit, the bandwidth is defined by the 3dB bandwidth where the gain is 3dB lower than the targeted value. For RF circuit, the bandwidth is defined as the range of frequencies over which a device performs to the rated specifications, such as the S11 is smaller than -10dB and gain is larger than 10dB.

The matching bandwidth is inversely related to Q:

$$BW = \frac{\omega_0}{Q} \tag{2.8}$$

Assuming $Rs = 50\Omega$ and f_0 is in the GHz range, Q of Eq. 2.7 is greater than 1 for a practical C_{gs} value. As a result, the bandwidth of this amplifier is very limited to not more than ω_0. To enlarge the bandwidth of a LNA, several topologies have been adopted for wideband impedance matching. The most straightforward way is combining more than one narrow-band pass-filter, as shown in Figure 2.3 [54].

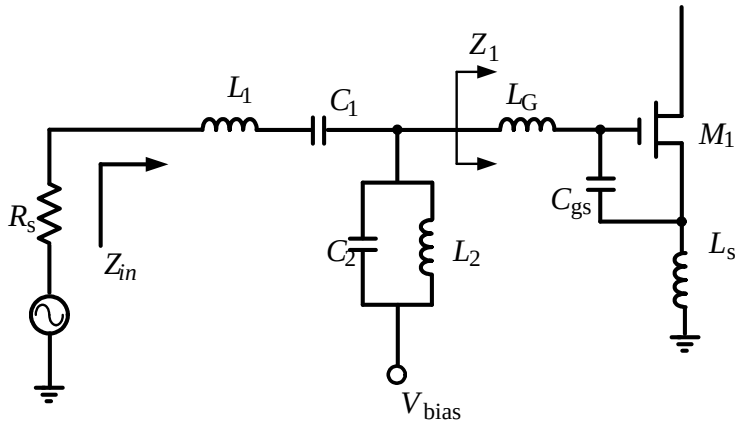


Figure 2.3 A band-pass filter input matching network [54]

The input impedance of the source degenerated CS amplifier can be expressed as:

$$Z_1(s) = \frac{1}{s(C_{gs}+C_p)} + s(L_s + L_g) + \omega_T L_s$$

$$Z_1(s) = \frac{s^2(L_s+L_g)(C_{gs}+C_p)+s\omega_T L_s(C_{gs}+C_p)+1}{s(C_{gs}+C_p)} \quad (2.9)$$

where $\omega_T = g_m/(C_{gs} + C_p)$ and C_p is the parallel capacitance. For the whole input matching network shown in Figure 2.3, there are three complex zeros. It is possible to provide wideband input matching by properly arranging the zeros at the expense of an in-band ripple, as shown in Figure 2.4. However, because of a large number of inductors required in the structure, the band-pass filter matching network consumes a substantial amount of power and chip area.

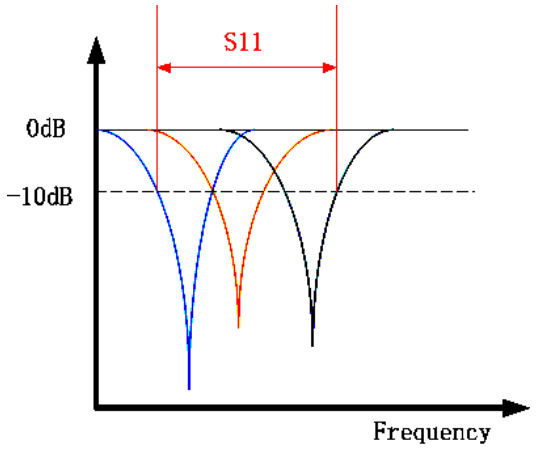


Figure 2.4 S11 of the combined narrow band input matching

In order to reduce silicon area, inductorless broadband LNAs are gaining interest in the research community. There are two well-known broadband topologies currently being used: the common-gate (CG) [55-57] and the shunt-shunt feedback amplifiers [58-60], which are both shown in Figure. 2.5.

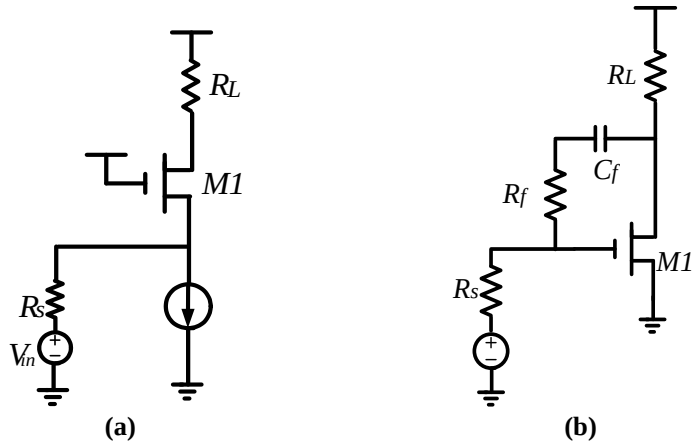


Figure 2.5 (a) Common-gate LNA (CS-LNA), (b) Common-source LNA (CG-LNA) with resistive feedback

The CG LNA can provide a wide bandwidth by using a small die area. This is because no inductor is required for the input impedance matching. The impedance can be expressed as:

$$Z_{in,CG} = \frac{r_0+R_L}{1+g_m r_0} \approx \frac{1}{g_m} \tag{2.10}$$

in which r_0 is the resistance of the transistor; this resistor is much larger than the load resistor R_L. The load resistance can be ignored in this approximation. The pre-determined g_m limits the choice of the device size and power consumption. For the shunt-shunt feedback structure, the input impedance is

$$Z_{in,FB} = \frac{R_F+R_L||r_0}{1+g_m(R_L||r_0)} \approx \frac{R_F+R_L}{1+g_m R_L} \tag{2.11}$$

From Eq. 2.10 and Eq. 2.11, the input impedances are very easy to be matched to 50Ω by varying both g_m and the load resistance values. However, when the frequency increases, the

effects of the parasitic capacitance becomes serious and limits bandwidth and gain of the amplifier. In addition, both the CG and the feedback structure suffer from poor noise performance which will be discussed in the following sections.

2.3 Noise and Noise Figure Requirements

Noise Figure (NF) is one of the most important parameters of a high performance LNA. As the first block, NF of the LNA determines the noise performance for the entire receiver. To properly design a LNA, a basic understanding of noise sources and noise analysis is required. There are two types of noise: interference noise and inherent noise [61]. Interference noise is mainly coming from unwanted interaction that is generated by different components inside the circuit or by other parts outside the circuit, such as power supply noise and coupling problems between signal wires. Careful circuit wiring and layout can effectively reduce interference noise. In contrast, inherent noise is a random noise coming from the fundamental properties of the circuit and its components. This type of noise cannot be avoided. This section deals only with inherent noises, namely thermal noise and flicker noise.

2.3.1 Thermal Noise and Flicker noise

Thermal noise or white noise is generated due to the Brownian motion of the conductor [62]. The measured voltage across the conductor may fluctuate because of the random motion of the electrons in the conductor even if there is no current flowing into it. Power of the thermal noise is proportional to the absolute temperature of the device.

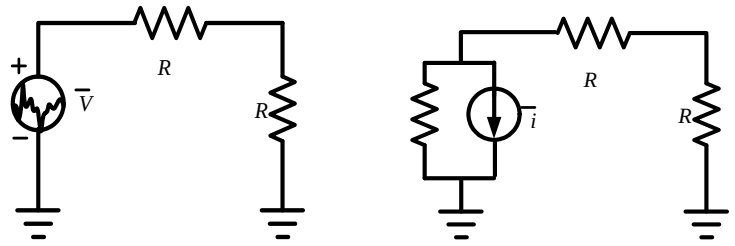
As shown in Figure 2.6 (a), the thermal noise of a resistor can be modeled by a series voltage source, with a power density of:

$$S_v(f) = 4kTR, \quad f \geq 0 \tag{2.12}$$

where $k = 1.38 \times 10^{-23} J/K$, is the Boltzman's constant. T is the absolute temperature in Kelvin and R is the resistance. The unit for $S_v(f)$ is V^2/Hz. Therefore, the noise "voltage" can be expressed as

$$\overline{v^2} = 4kTR\Delta f \tag{2.13}$$

where Δf is the noise bandwidth in Hz.



(a) (b)

Figure 2.6 Thermal noise model for a resistor

Similarly, the thermal noise of a resistor can also be represented by a parallel current source, as shown in Figure 2.6 (b). Using Ohm's law:

$$\overline{i^2} = \frac{\overline{v^2}}{R^2} \tag{2.14}$$

then the current can be expressed as

$$\overline{i^2} = \frac{4kT\Delta f}{R} \tag{2.15}$$

The dependence of the thermal noise upon *T* suggests that a low-temperature operation can decrease the noise. However, it is not practical since the circuits are designed to work at normal (or room) temperature, also the cooling equipment is very expensive to keep operating temperature low.

From Eq. 2.13 and 2.15, it can be seen that the noise power also depends on the bandwidth, Δf. That explains why the noise performance becomes worse as bandwidth increases. As a result, the only means for reducing thermal noise is to reduce the bandwidth by adopting very sharp filters.

Contrary to the wide bandwidth of thermal noise, flicker noise has a smaller bandwidth at the lower frequency range. Flicker noise is inherent of the material used to build the device such as silicon. The crystal lattices at the interface between the gate oxide and the silicon substrate of a MOSFET are not pure and the connections between the silicon are not stable. As charge carriers move at the interface, some are randomly trapped and later released by the "dangling" stages, introducing "flicker" noise in the drain current of a transistor.

Different from the thermal noise, flicker noise is generated randomly and the power density is very difficult to predict. The flicker noise may vary considerably between different CMOS technologies because of the "purity" of the oxide-silicon interface. The power of the flicker noise can also be modeled as a voltage source, which is connected in series with the gate of a transistor:

$$\overline{v^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f}\Delta f \tag{2.16}$$

where *K* is a device specified as constant on the order of $10^{-25}\ V^2F$ [62]. As shown in Eq. 2.16, the noise power is inversely proportional to the frequency. Therefore, the flicker noise is also called 1/*f* noise. As the frequency increases, the 1/*f* noise will fall off quickly, and its amplitude is much smaller compared to white noise. Eq. 2.16 also suggests that a larger device area may reduce *1/f* noise. The PMOS has a smaller flicker noise compared with the NMOS transistors. This is because the former takes the holes as carriers instead of electrons.

In order to compare the significance of different noise sources, both 1/*f* noise and thermal noise are plotted on the same graph, as shown in Figure 2.7. The intersection point of the 1/*f* and the white noises is called the "corner frequency", f_C. It is given by:

$$f_C = \frac{\mathrm{K}}{C_{ox}WL} g_m \frac{3}{8kT} \tag{2.17}$$

Eq. 2.17 shows that f_C depends on the size of the device and on g_m. However, when the length *L* is determined the corner frequency is relatively constant, which locates between 500kHz to 1MHz. Therefore, in a high frequency circuit the flicker noise can be neglected. By using these two types of noise, a MOS transistor can be modeled and analyzed its performance due to noise.

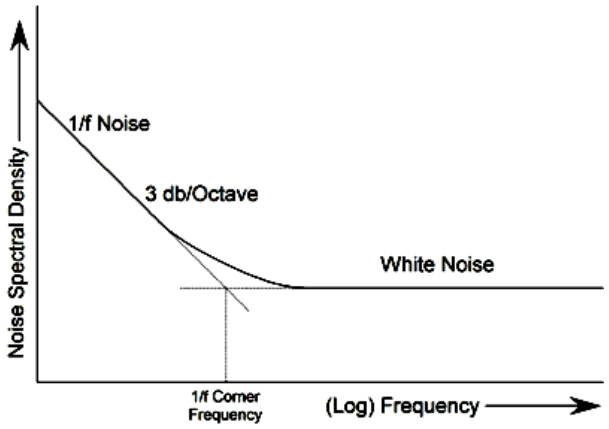


Figure 2.7 Corner frequency due to noise.

2.3.2 Noise Model for Standard MOSFET

The dominant noise source in a CMOS transistor is its channel thermal noise. This noise source is commonly modeled as a current source that is in parallel with the transistor. The CMOS noise model, which is considered as white noise, is shown in Figure 2.8.

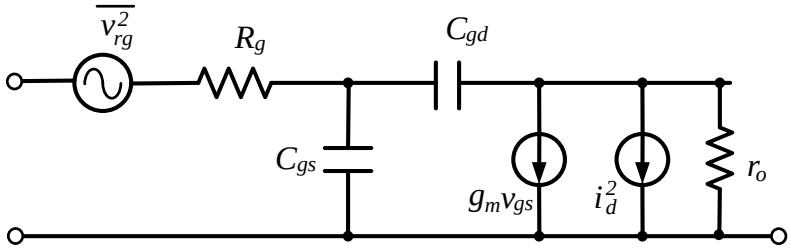


Figure 2.8 A standard CMOS noise model

The noise power density can be expressed as [62]:

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{2.18}$$

where g_{d0} is the drain conductance of the transistor when the gate is biased at zero, and γ is a bias-dependent factor. For long-channel devices, the value of γ is

$$\frac{2}{3} \leq \gamma \leq 1 \tag{2.19}$$

When the transistor is in saturation and the drain-source voltage is zero, γ can be constant at 2/3. However, for short-channel devices, γ is much larger than 2/3 when the devices operating in saturation, which is always as high as 2 to 3, depending on the bias condition [63, 64].

Another main source of noise in a MOS transistor is the gate noise generated by the gate resistance [63]. This noise source can be modeled as a white noise source that is in series with a resistor in the gate circuit. In order to decrease the gate resistance and reduce the contribution of the noise source in the gate, the multi-finger structure can be used in the layout of the transistor and connecting two ends of the fingered gates. In that condition, the resistance of the gate can be expressed as

$$R_g = \frac{R_{\square} W}{12n^2 L} \tag{2.20}$$

where $R_{\square}$ is the sheet resistance, *W* is the total gate width, *L* is the length of the gate, and *n* is the number of gate fingers in the layout. The connection between two ends of the fingers can be routed in a metal layer instead of directly using the polysilicon layer to reduce gate resistance.

Since the sheet resistance of a metal layer is much lower than polysilicon layer, the interconnect resistance can also be decreased.

2.3.3 Noise Figure and Sensitivity

The Noise Figure, which is used to evaluate noise performance of the circuit, can be analyzed by using the above CMOS noise model. Noise figure is a metric to evaluate Signal-to-Noise Ratio (SNR) degradation by a noisy circuit after a signal passing through it.

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{2.21}$$

There is another expression for the NF, which is

$$NF = \frac{Total\ output\ noise}{output\ noise\ due\ to\ source} = 1 + \frac{output\ noise\ due\ to\ the\ circuit}{output\ noise\ due\ to\ source} \tag{2.22}$$

In a series system, each building block generates noise from its own circuit but the contribution and influence to system noise coming from each stage is different. The system noise figure can be expressed by Friis formula:

$$NF_{all} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots + \frac{-1}{\prod_{j=1}^{i-1} G_j} \tag{2.23}$$

where NF_i and G_i are the noise factor and gain of each stage, respectively [61]. As shown in Eq. 2.23, the receiver noise is mainly determined by the first stage, LNA. The effect of noise coming from the subsequent stages is decreased by the gain of the LNA.

The sensitivity of a receiver defines the minimum signal power that can be processed by the receiver. Noise figure specification of a receiver is mainly determined by the receiver's sensitivity, as shown in the following equation.

$$P_{sens} = SNR_{Rx} + P_{n,s} + NF_{Rx} \tag{2.24}$$

in which SNR_{Rx} is the output signal-to-noise ratio. $P_{n,s}$ and NF_{Rx} are the source noise power and the noise figure of the receiver. The unit in this expression is in dBm for power and dB for the ratio. A lower sensitivity indicates that the receiver can receive weaker signal power at a longer distance from the transmitter; this determines the maximum range for receiving a signal. Therefore the LNA noise figure must be as low as possible in order to provide a better sensitivity for the receiver. For most of the communication standards, minimum sensitivity and SNR are specified in their specifications. Table 2.1 shows some typical receiver input sensitivity and noise figure. Accounting for these extra NF degradations, a noise figure of 3dB is expected for LNA in most applications [65,66].

Table 2.1 Sensitivity and Noise Figure specifications

	WCDMA	WLAN	GPS	WiMAX	BlueTooth	GSM/PCS	LTE	RFID
P_{sens} (dBm)	-117	-65	-136	-65	-70	-102	-102	-70
SNR (dB)	5.2	28	7	24	21	9	8	11.6
NF (dB)	9	7.5	2	7	23	9	9	39

2.4 Linearity

Linearity is another important consideration in the design of a high performance LNA, especially for multi-standard applications. This is because of the blocking problem, which will be discussed in the following section. Linearity also determines the largest signal level of the system in combination with a certain Signal-to-Noise ratio. When the received signal power is higher than the normal level (where the harmonics are negligible), the non-linear effects become noticeable, such as the harmonics, gain compression, desensitization, cross-modulation, intermodulation, and others.

2.4.1 Harmonics

The nonlinearity of the transistor is mainly caused by the nonlinear transconductance of the MOSFET. Assume the nonlinear relationship between the output and input of the system, the output can be described as [61]:

$$S_{out} = \alpha_1 * S_{in} + \alpha_2 * S_{in}^2 + \alpha_3 * S_{in}^3 + \cdots + \alpha_n * S_{in}^n \tag{2.25}$$

Assume the input of the system is

$$S_{in} = A\,sin(\omega_1 t) \tag{2.26}$$

Substitute Eq.2.26 into Eq.2.25 and neglect higher order terms, the output becomes:

$$S_{out} = \alpha_1 * \mathrm{A}\sin(\omega_1 t) + \alpha_2 * \mathrm{A}^2\sin^2(\omega_1 t) + \alpha_3 * \mathrm{A}^3\sin^3(\omega_1 t)$$

$$= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3}{4}\alpha_3 A^3)\sin(\omega_1 t) + \frac{1}{2}\alpha_2 \mathrm{A}^2 \sin(2\omega_1 t) + \frac{1}{4}\alpha_3 \mathrm{A}^3 \sin(3\omega_1 t) \tag{2.27}$$

Eq. (2.27) shows that the output contains the DC component $\frac{a_2 A^2}{2}$ and the fundmental component $(\alpha_1 A + \frac{3}{4}\alpha_3 A^3)\sin(\omega_1 t)$. Besides the fundamental harmonic, there are two additional terms at $2\omega_1 t$ and $3\omega_1 t$, which are the 2nd and 3rd harmonics.

2.4.2 Gain Compression

From Eq. 2.27, it can be seen that the fundamental amplitude $(\alpha_1 A + \frac{3}{4}\alpha_3 A^3)$ is distorted by $\frac{3}{4}\alpha_3 A^3$. If $\alpha_3 < 0$, then the gain of the fundamental signal decreases with the increasing of the magnitude *A*. This is characterized by P_{1dB} point. This point occurs where the nonlinear gain decreased by 1dB or 11%, smaller than α_1, as shown in Figure. 2.9.

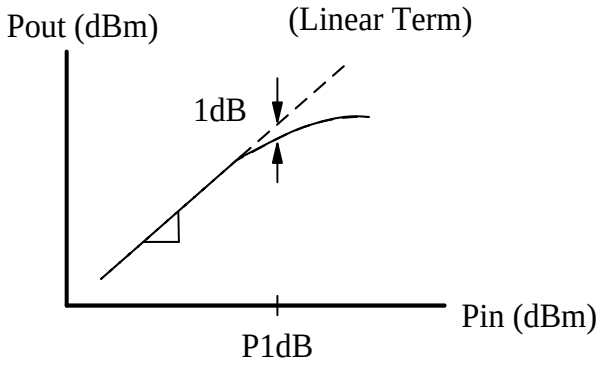


Figure 2.9 Definition of the 1dB compression

The 1dB point can be calculated by:

$$\alpha_1 + \frac{3\alpha_3}{4}A^2 = \alpha_1 * 10^{(\frac{1}{20})} \tag{2.28}$$

Solving Eq. 2.28, the $A_{P1\mathrm{dB}}$ can be expressed as:

$$A_{P1\mathrm{dB}} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.29}$$

2.4.3 Desensitization and Blocking

In a nonlinear circuit, a large interferingsignal may reduce the gain or "block" the desired weak signal, this phenomenon is called "desensitization". Assume there are two frequencies for the input signal passing through the system:

$$S_{in} = \mathrm{A}_1 \sin(\omega_1 t) + \mathrm{A}_2 \sin(\omega_2 t) \tag{2.30}$$

The results for the output becomes

$$\begin{aligned} s_{out} = {} & \left(\alpha_1 A_1 + \tfrac{3}{4}\alpha_3 A_1^3 + \tfrac{3}{2}\alpha_3 A_1 A_2^2\right)\sin(\omega_1 t) + \left(\alpha_1 A_2 + \tfrac{3}{4}\alpha_3 A_2^3 + \tfrac{3}{2}\alpha_3 A_1 A_2^2\right)\sin(\omega_1 t) + \\ & \tfrac{1}{2}\alpha_2 A_1^2 \sin(2\omega_1 t) + \tfrac{1}{2}\alpha_2 A_2^2 \sin(2\omega_2 t) + \tfrac{1}{4}\alpha_3 A_1^3 \sin(3\omega_1 t) + \tfrac{1}{4}\alpha_3 A_2^2 \sin(3\omega_2 t) + \\ & \Big(\alpha_2 A_1 A_2 \sin(\omega_1 t + \omega_2 t) + \alpha_2 A_1 A_2 \sin(\omega_1 t - \omega_2 t) + \tfrac{3}{4}\alpha_3 A_1^2 A_2 \sin(2\omega_1 t + \omega_2 t) + \\ & \tfrac{3}{4}\alpha_3 A_1^2 A_2 \sin(2\omega_1 t - \omega_2 t) + \tfrac{3}{4}\alpha_3 A_2^2 A_1 \sin(2\omega_1 t + \omega_2 t) + \tfrac{3}{4}\alpha_3 A_2^2 A_1 \sin(2\omega_2 t - \omega_1 t)\Big) \end{aligned} \tag{2.31}$$

If $A_1 \ll A_2$, the first term in Eq. 2.31 can be simplied to $\left(\alpha_1 A_1 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)$. Then the gain for the singal A_1 can be expressed as $\left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2\right)$. If $\alpha_3 < 0$, the gain of the A_1 decreases with the increasing of A_2. If A_2 is large enough, the gain can be as low as zero, and the signal with the magnitude of A_1 will be blocked.

2.4.4 Intermodulation

If the two frequencies in Eq. 2.31 ω_1 and ω_2 are close enough and the magnitues A_1 and A_2 are the same, the intermodulation terms $\frac{3}{4}\alpha_3 A_1^2 A_2 \sin(2\omega_1 t - \omega_2 t)$ and $\frac{3}{4}\alpha_3 A_2^2 A_1 \sin(2\omega_2 t - \omega_1 t)$ are located near the fundamental signals, which is difficult to identify and eliminate. The concept is shown in Figure 2.10.

Figure 2.11 shows the geometric interpretation of the 1st order and 3rd order extrapolation of the signals in a log-log scale. The P_{in} and P_{out} indicate the input and output signal power, respectively. The Input Interception Point (IIP) indicates the input signal power where the extrapolated curves intercepted. According to [67], the IIP2 and IIP3 can be expressed as

$$IIP_2 = \sqrt{\frac{\alpha_1}{\alpha_2}} \tag{2.32}$$

$$IIP_3 = \sqrt{\left|\frac{4\alpha_1}{3\alpha_3}\right|} \tag{2.33}$$

Comparing Eq. 2.29 and Eq. 2.33, IIP3 is related to P_{1dB} by

$$A_{P1dB} = IIP_3 - 9.6\text{dB} \tag{2.34}$$

It has been shown that the relation between 1dB and IIP3 point is relatively constant [68-71].

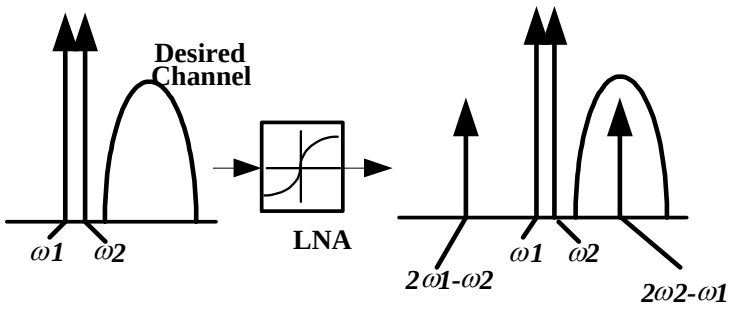


Figure 2.10 Signal corruption due to two-tone intermodulation

For a series system, the intercept point can be expressed as

$$\frac{1}{IIP_x^2} \approx \frac{1}{IIP_{x,1}^2} + \frac{\alpha_{1,1}^2}{IIP_{x,2}^2} + \frac{\alpha_{1,1}^2\alpha_{1,2}^2}{IIP_{x,3}^2} + \cdots + \frac{\prod_{j=1}^{i-1}\alpha_{1,j}^2}{IIP_{x,i}^2} \tag{2.35}$$

where x is the x^{th} order of the input intercept, and the α_i coefficient at the i^{th} stage [61].

Different from noise figure, linearity of the system is determined by each stage instead of just the first stage. The targeted receiver linearity requirements of the multiple standards are shown in Table 2.2. In RFID applications, the IIP3 is dependent on the power of the transmitter. The minimum IIP3 requirement is 1dBm for 20dBm transmitting power and 10dBm for 30dBm transmitting power.

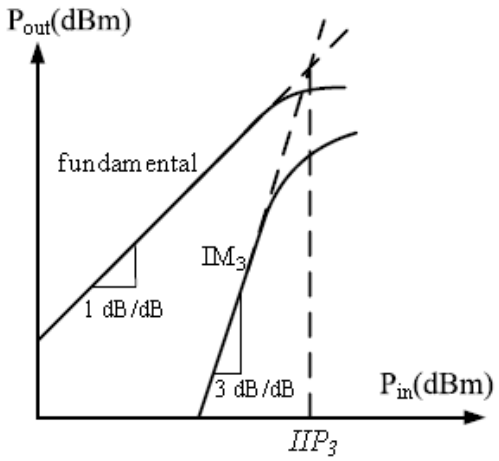


Figure 2.11 dB plot of IIP3

Table 2.2 Signal corruption due to two-tone intermodulation in different standards

	WCDMA	WLAN	GPS	WiMAX	BlueTooth	GSM /PCS	LTE
RX IIP3(dBm)	-4	-20	+14	-8	-15	-18	-7

CHAPTER 3

LNA DESIGN AND OPTIMIZATION

In previous chapter, the basic device and system parameters that are needed to be concerned for the implementation of a low noise amplifier have been introduced and discussed. It is very challenging to design a LNA that simultaneously consists all of the desired performances: wide bandwidth, high linearity, high gain, small NF, and low power consumption. In general, there are tradeoffs between these parameters. In this study, the requirement for area and power consumption is not too stringent. This comes from the fact that by comparing with the solution of employing parallel narrowband LNAs, the method of sharing a single LNA for multiple applications already inherits the benefit in chip area and power usage. In the designs of this thesis work, area and power can be sacrificed to trade-off for the bandwidth, noise figure, and linearity. Based on this design, the noise figure and linearity optimization methods will be discussed in this chapter.

3.1 Noise cancellation techniques

3.1.1 Extended CMOS Noise Model Analysis

The standard CMOS noise model is given in Chapter 2. There are two basic noise sources in a CMOS transistor: the channel thermal noise and the noise that is generated by the gate resistance. Gate resistance is much less significant than channel noise. The resistance can be minimized by adopting multi-fingers in the layout or by decreasing sheet resistance $R_{\square}$. Channel noise can also be simplified to a white noise with the power density shown in Eq. 2.18. In addition to these two noise sources, when the operating frequency increases, there will be a

current generated in the gate because of the capacitive coupling. This limits noise performance of the device.

The noise from the gate has not been considered in previous analyses and will be analyzed in detail in the following introduction for noise optimization. The gate circuit noise model is shown in Figure 3.1(a), which includes a noise current $\overline{i_g^2}$ and a conductance $g_g$in parallel. Similar to the drain noise expressed in Eq. 2.18, the gate noise can be expressed as:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \tag{3.1}$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{3.2}$$

where δ is the coefficient of the gate noise, which equals to 4/3 for long channel transistor. Different from the drain noise in Eq. 2.18, the gate noise is not a white noise. This is because the gate conductance g_g is proportional to frequency.

According to [63], the gate noise is partially correlated with the drain noise with a correlation coefficient

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \approx 0.395j \tag{3.3}$$

where the value of $0.395j$ is a constant for the long channel transistor. Then the gate noise can be expressed as

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g(1 - |c|^2) + 4kT\delta g_g|c|^2 \tag{3.4}$$

where the first term is uncorrelated with the drain noise while the second term is fully correlated.

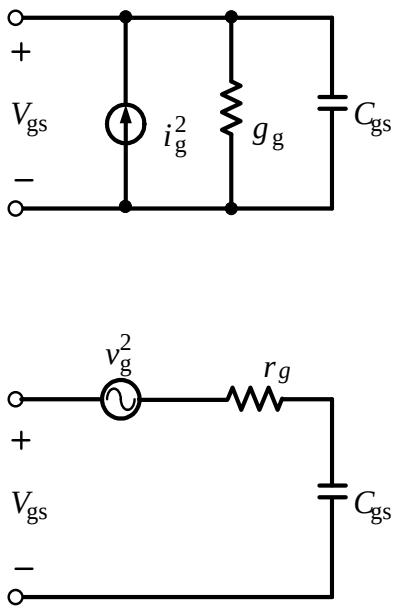


Figure 3.1 Noise model of a gate circuit

Until now, the three main noise sources for the transistor have been introduced and analyzed. Based on this analyses, the NF of a LNA will be evaluated and optimization methods will be proposed.

3.1.2 LNA Noise Analysis

For a typical common source LNA structure shown in Figure 3.2 (a), noise is analyzed using a small signal model, as shown in Figure 3.2 (b). In this circuit, R_l and R_g represent the series resistance of the inductor and the transistor gate, respectively. In the analysis, the noise coming from the following stages are neglected based on the assumption that the first stage has sufficient gain. $\overline{v_l^2}$ and $\overline{v_{rg}^2}$ represent the noise voltages of the inductor and the gate resistance.

$\overline{v_d^2}$ represents the drain current noise of the transistor, which is also channel thermal noise. $\overline{i_{g,u}^2}$ represents the gate noise that is uncorrelated with the drain noise and $\overline{i_{g,c}^2}$ is the noise that is correlated with the drain noise. The input noise voltage will be transferred to an output current because of the transconductance of the transistor. The noise figure of the LNA will be calculated according to the definition in Eq. 2.22.

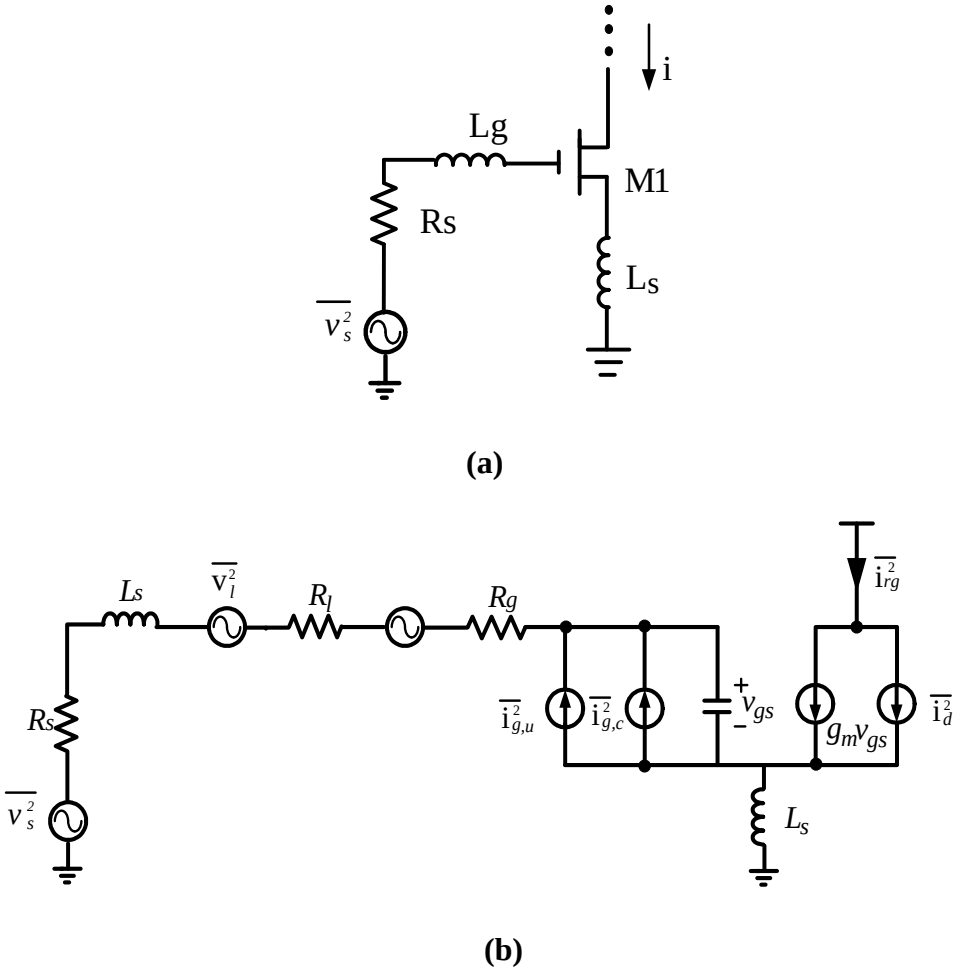


Figure 3.2 (a) Typical common source LNA structure (b) Small-signal model for LNA noise analysis

The four noises coming from the source resistance, the gate inductor and resistance, the channel thermal noise, and the gate noise contribute to the output noise. The output power density due to the 50Ω input source is

$$S_{src} = \frac{4kTw_T^2}{w_0^2 R_s (1+\frac{w_T L_s}{R_s})^2} \tag{3.5}$$

The output noise power density due to the R_l and R_g is

$$S_{R_l,R_g} = \frac{4kT(R_l+R_g)w_T^2}{w_0^2 R_s^2 (1+\frac{w_T L_s}{R_s})^2} \tag{3.6}$$

The channel current is the main contribution of the output noise, which can be expressed as

$$S_{i_d} = \frac{\frac{\overline{i_d^2}}{\Delta f}}{(1+\frac{w_T L_s}{R_s})^2} = \frac{4kT\gamma g_{d0}}{(1+\frac{w_T L_s}{R_s})^2} \tag{3.7}$$

The gate noise is divided into two parts. The portion that correlates with the drain noise can be expressed as

$$S_{i_{g,c}} = \kappa S_{i_d} = \kappa \frac{4kT\gamma g_{d0}}{(1+\frac{w_T L_s}{R_s})^2} \tag{3.8}$$

where κ is correlating parameter,

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + |c|Q\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{3.9}$$

and Q is the effective quality factor, which can be expressed as

$$Q = \frac{w_0(L_s+L_g)}{R_s} = \frac{1}{w_0 R_s C_{gs}} \tag{3.10}$$

The gate noise that is uncorrelated with the drain noise is

$$S_{i_{g,u}} = \xi S_{i_d} = \xi \frac{4kT\gamma g_{d0}}{(1+\frac{w_T L_s}{R_s})^2} \tag{3.11}$$

The total output noise density is the sum of Eq. 3.8 to Eq. 3.11, after simplification, the output noise becomes

$$S_{out} = (\xi + \kappa)S_{i_d} = [1 + 2|c|Q\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2)]\frac{4kT\gamma g_{d0}}{(1+\frac{w_T L_s}{R_s})^2} \tag{3.12}$$

To simplify the expression, the factor χ is defined as

$$\chi = \xi + \kappa = 1 + 2|c|Q\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2) \tag{3.13}$$

Taking it into the Eq. (2.22), the NF can be expressed as

$$NF = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma\chi g_{d0} R_s \left(\frac{w_0}{w_T}\right) \tag{3.14}$$

Taking Q to the expression, the NF can be re-expressed as

$$NF = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q}\left(\frac{w_0}{w_T}\right) \tag{3.15}$$

Through observation of Eq. 3.13 and Eq. 3.15, it can be seen that there is a particular value of Q to provide a minimum NF and makes the process of NF optimization possible.

3.1.3 NF Contour Optimization

It can be seen that the NF can be optimized according Eq. 3.15. All of the parameters have been defined in previous analysis except for γ and δ, which is in Eq. 3.13. The two parameters depend on the drain voltage and the gate bias voltage; normally, it is difficult to account for their contributions into the noise calculation. In order to simplify the calculation both γ and δ are assumed to be the functions of the gate bias voltage, because both have a similar dependence that was previously mentioned.

It can be seen that NF is mainly determined by the last term in Eq. 3.15. The second and third terms can be neglected since the resistances of R_l and R_g are much smaller compared to R_s. Therefore, these two terms will be ignored in the following analysis. The most critical factor Q can be expressed as:

$$Q_L = \frac{P_0}{P_D}\frac{\rho^2}{1+\rho} \tag{3.16}$$

With the definition that

$$\rho = \frac{V_{gs}-V_{th}}{L_{sat}} \tag{3.17}$$

P_0 is a constant which is only determined solely by the technology parameters, as shown

$$P_0 = \frac{3}{2}\frac{V_{dd}v_{sat}\varepsilon_{sat}}{w_0 R_s} \tag{3.18}$$

P_D is the power consumption of the LNA, it can be calculated as

$$P_D = V_{dd} I_d \tag{3.19}$$

The current I_d can be expressed as

$$I_d = W C_{ox} v_{sat} \frac{(V_{gs}-V_{th})^2}{V_{od}+L\varepsilon_{sat}} \tag{3.20}$$

Replacement of current into Eq. 3.19, the power becomes:

$$P_D = V_{dd} W C_{ox} v_{sat} \frac{(V_{gs}-V_{th})^2}{V_{od}+L\varepsilon_{sat}} \tag{3.21}$$

There are two ways to optimize NF: optimization with a constant transconductance (or gain) and optimization with a constant power consumption. Therefore, the quality factor *Q* is related to both power consumption and overdrive voltage.

The above equations provide the design guideline for NF optimization. However it is difficult to directly apply these equations to designing the LNA because there are too many parameters involved at the same time. In practice, a NF contour analysis by sweeping the parameter values is commonly used in order to clearly apprehend the design.

3.1.4 Bruccoleri's Thermal Noise Cancellation

The NF optimization method illustrated in Section 3.1.3 only provides a guideline for choosing the transistor size and power consumption to achieve a relative lower NF. However, if the requirements for power and gain are critical, there is not much freedom allowed to reduce NF because of the trade-offs between NF, power, and bandwidth. Also, the optimized NF only happens at a particular frequency range. For multi-standard applications, the wideband input

matching structures, such as the resistive feedback common-source and the common-gate, show a severe trade-off between NF and the matching requirements.

In [72], Bruccoleri's technology was first proposed for wideband noise cancelling applications and was proved to effectively lower noise figures in the targeted bandwidth without consuming extra chip area and power. In this technique, both thermal noise and distortion of the input transistor can be sensed and cancelled by a feed-forward structure [73]. By adding the feed-forward structure, the potential instability that is caused by the feed-back loop (negative feedback) was eliminated. Both noise and distortion are cancelled at the output, therefore both input matching and noise performance can be optimized simultaneously without any trade-off between them.

The basic concept is to generate signals with the same phase and noises with an opposite phase in different paths. By summing the output, the signals will be added while noises will be cancelled with each other. The basic structure is shown in Figure 3.3. This is the most widely used common source structure of LNA. The resistive feedback structure is used for broadband impedance matching but the use of resistances induces a high noise figure. A feed-forward amplifier with a gain of A_x is used to generate noises with the opposite phase-polarities in different paths and cancel noises at the output. Since the cancellation method has no relevance to the input impedance, this technique can simultaneously achieve low noise figure and broadband impedance matching.

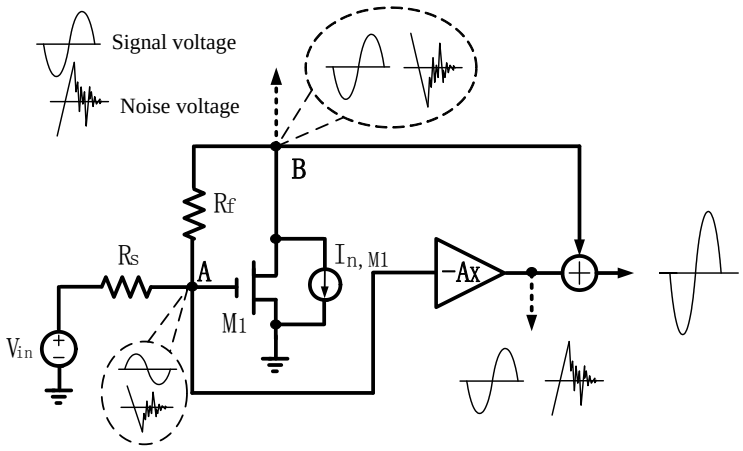


Figure 3.3 Bruccoleri's thermal noise cancellation

For CMOS transistors, the channel thermal noise is considered as the dominant noise component. Therefore, the common-source stage, M1, is modeled as a noise current source between the drain and source. R_f is the feedback resistor, which is used for wideband input matching. The feed-forward voltage amplifier has a gain of A_x. Part of the noise current that is generated by the transistor flows through the feedback resistor R_f to the gate of the amplifier and generates the noise voltage V_A, V_B at the node A and B with the same phase polarity. Let the input impedance be Rs, the noise voltages at A and B can be expressed as

$$V_{A,n} = \alpha I_n R_s \tag{3.22}$$

$$V_{B,n} = \alpha I_n (R_s + R_f) \tag{3.23}$$

where $0 < \alpha < 1$, is the percentage of the noise current that flowing to the feedback resistor.

On the other hand, the signal voltages at nodes A and B have the opposite polarity because the common-source amplifier has an inverting gain. The differences of signal and noise polarities

at node A and B make it possible to cancel the noise while adding the signal contributions. This can be realized by the feed-forward amplifier, which adds one negative scale to the voltage at node A. The output noise voltage after the noise cancelling operation can be expressed as

$$V_{out,n} = \alpha I_n(R_s + R_f) - A_v(\alpha I_n R_s) \tag{3.24}$$

To make sure the $V_{out,n}$ equals zero, the gain of the feed-forward amplifier should be

$$A_x = 1 + \frac{R_f}{R_s} \tag{3.25}$$

It shows that, when *Ax* equals to $1 + (R_f/R_s)$, the noise of the input transistor M1 can be cancelled at the output and the signal gain is enhanced. Assuming that the input impedance of the amplifier matches the source impedance, the overall gain for the signal is:

$$A_v = -R_f(g_{m1} + \frac{1}{R_s}) \tag{3.26}$$

Assuming the input impedance $Z_{in} = 1/g_m = R_s$, the voltage gain *Av* is:

$$A_v = -2\frac{R_f}{R_s} \tag{3.27}$$

By choosing appropriate resistance and gain to match the path gain for concerned drain noise, a complete removal of transistor noise can be achieved.

However, to make sure that the noise can be cancelled at the output, the feed-forward gain should be equal to A_X, which is $1 + (R_f/R_s)$, as shown in Eq. 3.25. In the meantime, the overall signal gain is $-2(R_f/R_s)$, as indicated in Eq. 3.27. Therefore, the noise cancelling requirement restricts freedom for controlling gain of the amplifier [74, 75]. Based on traditional Bruccoleri

technology, a new structure that can enhance the gain of the noise cancelling technology is proposed in the following designs.

3.2 Linearity Enhancement Techniques

According to [76], linearity of a LNA can be improved by increasing the overdrive voltage. However, if the power consumption will be high then thermal noise will also increase. Another linearity enhancing method is to adopt the negative feedback structure. By doing this, the second order linearity can be improved because the input signal is relatively low and the non-linear effects coming from the transistor is alleviated. The third order linearity can also be improved because IIP2 and IIP3 are related [77]. Second and third order linearity of the feedback structure can be improved by a factor of $(1 + T_0)$ and $(1 + T_0)^2$ respectively, where T_0 is the open loop gain. However, for high frequency LNA applications, the feedback structure is less effective.

Another linearity enhancement method is through cancellation. Different from noise, which is random and difficult to be anticipated, the circuit nonlinearity can be predicted and easily to be corrected at the output by adopting a special structure. Many distortion cancellation techniques have been proposed and widely used, which will be introduced in the following sections.

3.2.1 Feedback

As previously mentioned, the feedback structure can improve both the second order and third order linearity of the LNA. The basic schematic is shown in Figure 3.4 in which A is the amplifier with nonlinearity and β is the amplitude of the feedback path. *X* and *Y* are the input and output signal. According to Eq. 2.25, output Y can be expressed as

$$Y = aX + a'X^2 + a''X^3 \tag{3.28}$$

where a, a' and a'' are the closed loop linear gain, and the second and third order nonlinearity coefficients respectively. This can be expressed as:

$$a = \frac{g}{1 + A_0}$$

$$a' = \frac{g'}{(1 + A_0)^3}$$

$$a'' = \frac{1}{(1+A_0)^4}\left(g'' - \frac{2(g')^2}{g}\frac{A_0}{1+A_0}\right) \tag{3.29}$$

A_0, the open loop gain, can be expressed as $A_0 = g\beta$. IIP2 and IIP3 of the closed loop system can be expressed as

$$IIP_2 = \sqrt{\frac{a}{a'}} = \sqrt{\frac{g}{g'}(1 + A_0)^2} \tag{3.30}$$

$$IIP_3 = \sqrt{\left|\frac{4a}{3a''}\right|} = \sqrt{\frac{4g}{3g''}\frac{(1+A_0)^3}{(1-\frac{2(g')^2}{gg''}\frac{A_0}{1+A_0})}} \tag{3.31}$$

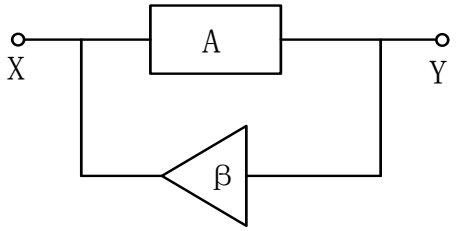


Figure 3.4 Nonlinear amplifier with negative feedback

Compared with the IIP2 and IIP3 expression in Eq. 2.32 and Eq. 2.33, the IIP2 is improved by a factor of $(1 + A_0)$ and IIP3 is improved by $(1 + A_0)^{3/2}$ when $g' \approx 0$. If gg'' is negative (this is the case for typical CMOS transistor), when g' increases IIP3 will be degraded. This phenomenon is called "second-order interaction". Therefore, the feedback structure can eliminate the third order nonlinearity. The main drawback of the feedback structure is that the open loop gain A_0 cannot be too high. In addition, the "second order interaction" can be very serious and degrades the IIP3 of the feedback structure. Therefore, the effectiveness of the feedback linearity enhancing method is limited.

3.2.2 Sweet Spot

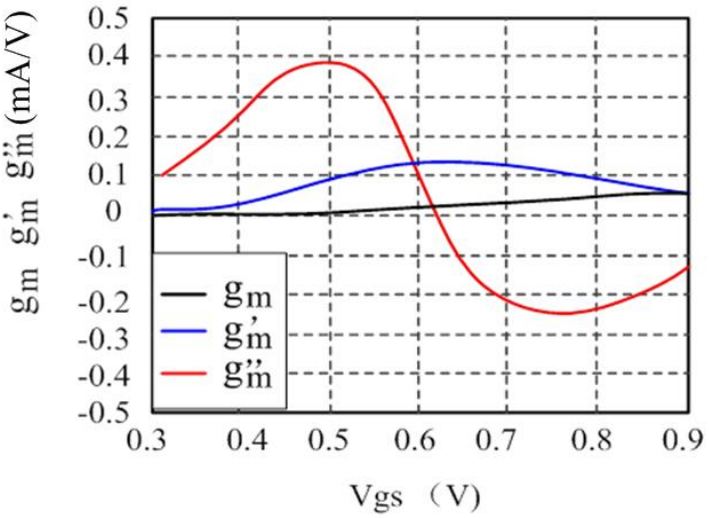
For CMOS transistors, nonlinearity is mainly coming from the transconductance. According to [61], the drain current of the transistor can be expressed as:

$$i_{ds} = g_m v_{gs} + g'_m v_{gs}^2 + g''_m v_{gs}^3 \tag{3.32}$$

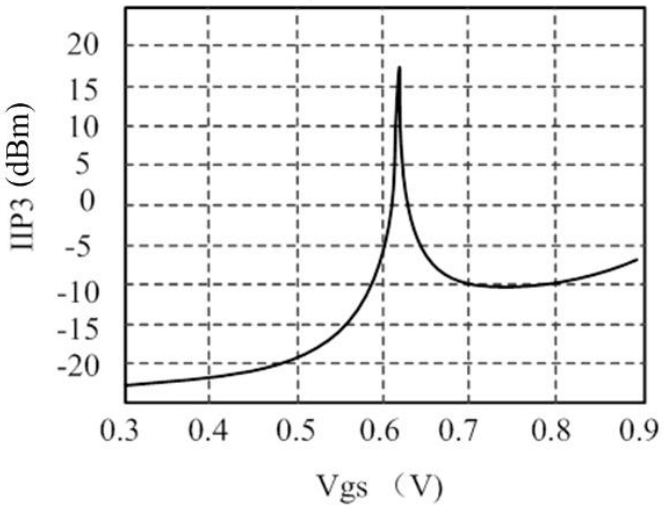
where the v_{gs} is the gate to source voltage. g_m, g'_m and g''_m are the first, second, and third order transconductances. It can be seen that the third nonlinearity is mainly caused by the third

order transconductance g_m''. Therefore, a lower g_m'' makes an excellent third order linearity, which is indicated by IIP3 [78]. From Figure 3.5, it can be seen that there is a peaking or a "sweet spot" in the moderate inversion region of the common-source amplifier. The third order transconductance g_m'' equals to zero at the "sweet spot", and according to Eq. 3.28, the third order nonlinearity is cancelled.

However, the "sweet spot" method is not easily implemented. The IIP3 peak value is too sensitive to the bias voltage. A small offset of the bias will cause a big change in the IIP3 value. Even if the optimized bias voltage can be found in the simulation, it is difficult to be realized because of the process variation [79]. Also, even if the sweet spot can be found in the real circuit, the bandwidth with high IIP3 is limited and cannot be used for wideband LNAs.



(a)



(b)

Figure 3.5 (a) DC transfer characteristic of the Common Source Structure and (b) Plot of IIP3 versus gate-to-source voltage.

3.2.3 Derivative Superposition

When observing the curves in Figure 3.5, it can be seen that g_m'' first goes to a positive peak and then goes down to a negative peak. This happens as the V_{gs} changes from the weak inversion region to the strong inversion region.

If two transistors are put in parallel with proper sizes and bias voltages, as shown in Figure 3.6 (a), the positive and negative polarity regions of the third order transconductances for the two transistors can be aligned and be cancelled each other. By doing this, a relatively wide range of near zero g_m'' can be achieved, as shown in Figure 3.7. This process is called the derivative superposition (DS) technique [80-85]. The DS technique reduces IIP3 sensitivity.

In Figure 3.6 (a), there is one transistor added in parallel with the original common source amplifier. The drain and source of the two transistors are connected together. The transistor M_A is biased in the weak inversion region while transistor M_B is biased in the strong inversion region. The offset of the bias voltage can arrange the g_m'' curves of the two transistors to ensure that the peak of one transistor is aligned with the valley of the other. The size of the two transistors should be matched, allowing for a relatively flat near zero g_m'' to be achieved. Compared to the "sweet spot" technique, the DS method is less sensitive to bias variation and achieves a broader high IIP3 range, as shown in Figure 3.7.

The DS method is proven to be effective only at a lower frequency range. When frequency increases, the nonlinearity that is coming from the parasitic parameters becomes more significant. For the common source structure, the degenerated inductor provides a feedback for the drain current to the gate-source voltage. Even though the third order nonlinearity can be perfectly cancelled out, the second order harmonic components are still contributing to the third order harmonics through the feedback path, as shown in Figure 3.6 (b).

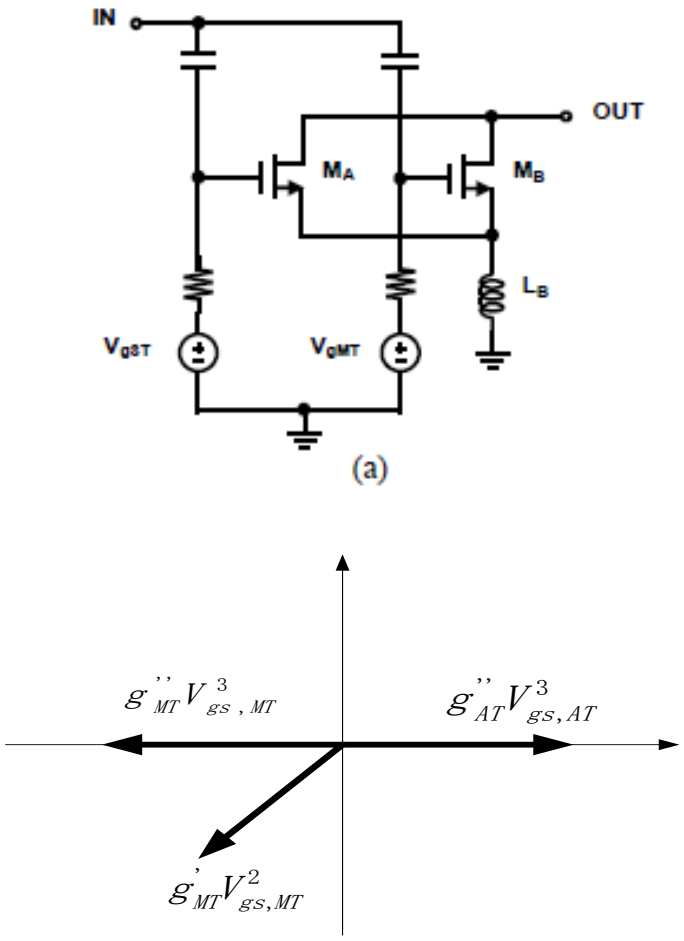
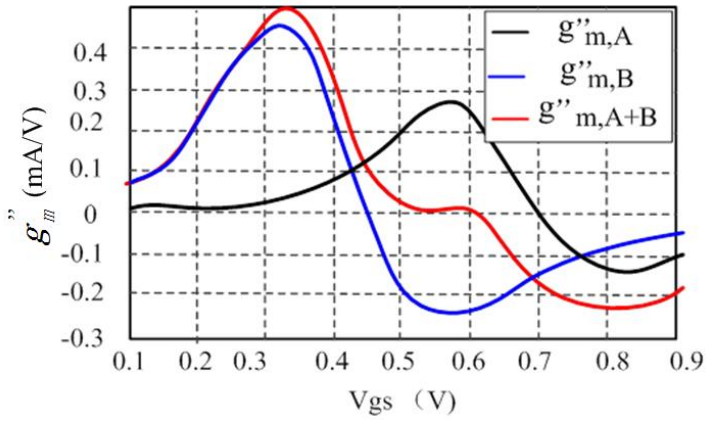


Figure 3.6 (a) Simplified schematic of the derivative superposition technique and (b) Conceptual vector diagram

To illustrate the imperfect cancellation of the DS technique quantitatively, the IIP3 expression of the DS technique is presented as:



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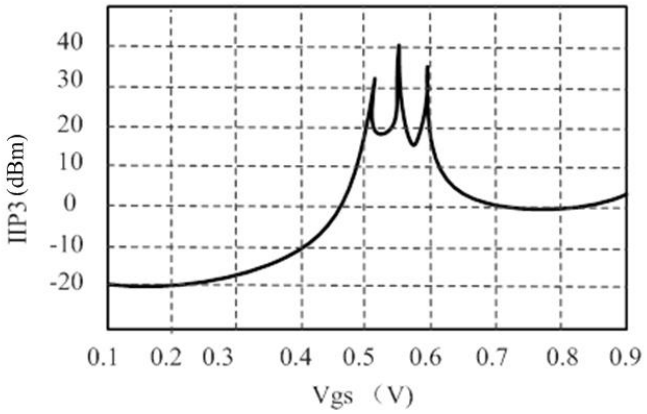


(b)

Figure 3.7 (a) g_m'' of the transistors and (b) Plot of IIP3 versus gate-to-source voltage.

$$IIP3 = \frac{4\omega^2 (g')^2 L_B (C_A + C_B)}{3|\varepsilon|} \tag{3.29}$$

where

$$\varepsilon = g_A'' + g_B'' - \frac{\frac{2}{3}(g_B')^2}{g_B + \frac{1}{j2\omega L_B} + j2\omega(C_A + C_B) + Z_1(j\omega)\frac{C_A+C_B}{L_B}}$$

$$\approx g_A'' + g_B'' - \frac{2(g_B')^2}{3g_B}\frac{1}{1+\frac{1}{j\omega g_B L_B}} \tag{3.30}$$

As shown in Eq. 3.29 and Eq. 3.30, IIP3 is limited because of the second order products in Eq. 3.30 even though the third order part $g_A'' + g_B''$ equals to zero. In addition, it can be seen that the IIP3 is inversely proportional to frequency ω. As a result, the effectiveness of the DS method is limited at higher frequencies.

3.2.4 Modified Derivative Superposition

In order to enhance the effectiveness of the DS techniques at higher frequencies, the modified derivative superposition method was proposed in [86, 87]. As shown in Figure 3.8 (a), the sources of the two parallel transistors are connected to different nodes of the degenerated inductors (L_A and L_B). By regulating the inductance of L_A and L_B, both the phase and the magnitude of the third order harmonics can be adjusted. By adjusting L_A and L_B, the second-order and third-order nonlinearity will cancel each other as illustrated in Figure 3.8 (b).

The quantitative analysis is shown as the following section. The IIP3 of the modified DS technique is expressed as

$$IIP3 = \frac{4\omega^2(g')^2[L_A(C_A+C_B)+L_BC_B]}{3|\varepsilon|} \tag{3.31}$$

$$\varepsilon = g_A''(1 + j\omega L_B g_B)[1 + (\omega L_B g_B)^2]\left[1 + \frac{L_B C_B}{L_A(C_A + C_B) + L_B C_B}\right]$$

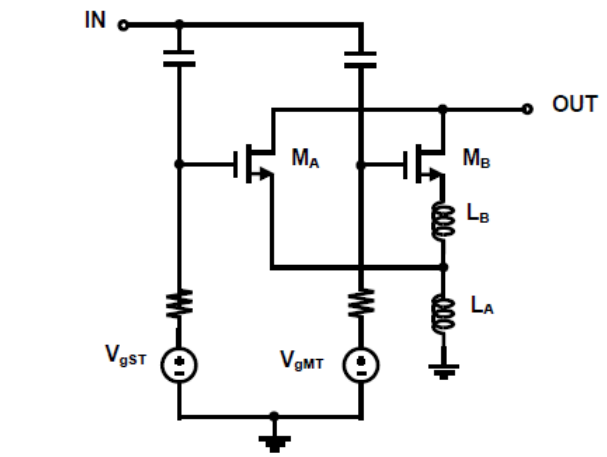
$$+g_B'' - \frac{2(g_B')^2}{3g_B} \frac{1}{1+\frac{1}{2j\omega g_{B(L_A+L_B)}}} \tag{3.32}$$

The second order term can be adjusted by changing inductance of L_A and L_B, causing the second order nonlinearity to be cancelled by the modified DS technique. However, the modified DS technique is effective only for narrow banded LNAs and also, IIP3 is very sensitive to bias voltage.

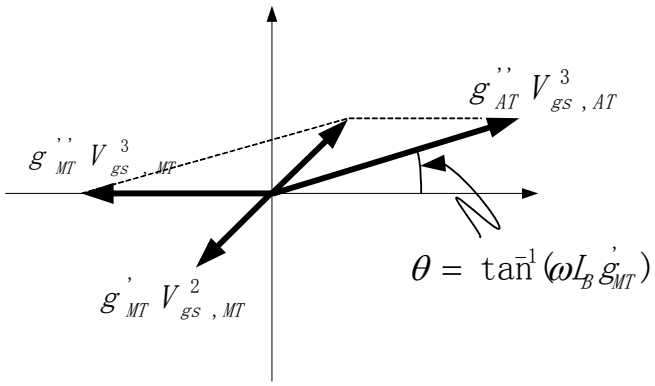
3.2.5 Noise and Distortion Cancellation

This basic idea for the noise and distortion cancellation technique is similar to the Bruccoleri's thermal noise cancellation method. By generating the noise and nonlinearity contributions with opposite phases and the same amplitude in different paths, both the noise and distortion can be cancelled at the output. The circuit in Figure 3.9 was proposed in [88-90].

The input signal is amplified by the common gate amplifier M_A (with the same phase) and M_B (with the opposite phase) and summed at the output. In the meantime, both the nonlinearity and thermal noise of M_A flow through the CG and CS stages are being subtracted at the output. All the intrinsic distortion that generated by the M_A can be cancelled out by this method, including g_m and g_{ds} nonlinearity. However, like the other linear methods, the "sweet spot" and the DS technique method, can only cancel the g_m nonlinearity. After cancelling all the distortion of M_A, the nonlinearity of this method is mainly coming from M_B.



(a)



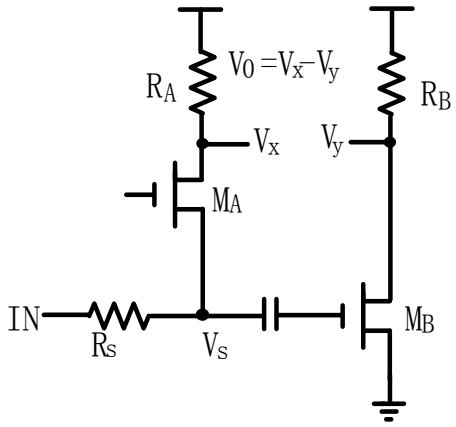
(b)

Figure 3.8 (a) Simplified schematic of the Modified Derivative Superposition technique and (b) Conceptual vector diagram.

3.3 Summary

Table 3.1 compares IIP3, gain, NF, and power consumption of different noise and linearity enhancing methods discussed in previous sections. Only one representative reference is chosen for each method. Note that there is a tradeoff between different parameters of each technique. The noise and distortion technique adopted the feedback structure and achieves the largest

bandwidth. However, both its IIP3 and NF are not as good as the other methods. The modified DS technique achieved the best IIP3 with the increment in power consumption. Optimal biasing achieved the best NF, even it has the lowest power consumption, it is only effective on a particular frequency and it is very sensitive to bias variation.



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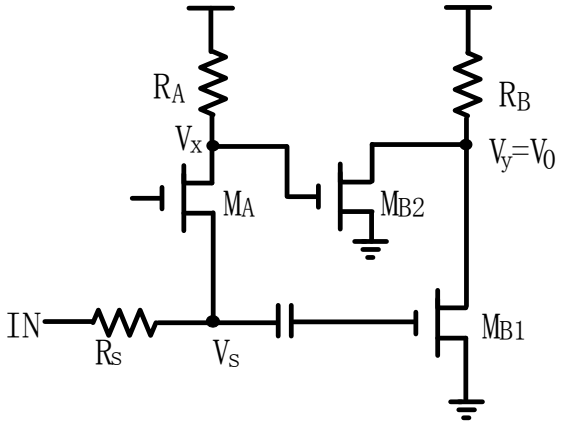


(b)

Figure 3.9 Noise/distortion cancellation. (a) Differential output [88], [90]. (b) Single ended output [89]. Simplified circuit schematic of noise/distortion cancellation.

In the multi-standard LNA design, the LNA receives signals with different channels at the same time. The nearby signals and the on-chip transmitter leakages can interfere with each other and cause severe intermodulation, blocking, and gain compression. Therefore it is very challenging to achieve a high linearity over a wide frequency range without significantly influencing NF and gain of the LNA.

In addition to the challenges of achieving a high linearity with a wide bandwidth, there are several different tradeoffs that must be considered. These tradeoffs will be discussed in the subsequent chapters. Feedback topology was chosen for this work because it can increase the bandwidth and linearity simultaneously with a reduction in gain. In addition, the feedback circuit introduces more noise into the structure. According to [76], a high overdrive voltage improves linearity while consuming much more power.

The DS technique methodology improves linearity effectively by adding an additional transistor for IIP3 cancellation. However, the additional transistor also introduces more noise into the circuit. Therefore, it is very challenging to balance the tradeoff among all of the desired parameters. In the future design, all of the approaches and methodologies previously mentioned will broadly be followed. Some parameters and detailed circuit structures will be regulated for parameters optimization.

Table 3.1. Comparison of linearity enhancement techniques

Linearity Enhancing Technique	Optimal Biasing (sweet spot) [78]	Derivative Superposition (DS) technique [80]	Modified DS technique [86]	Noise and Distortion Cancellation [89]
Frequency	880MHz	2.2GHz	900MHz	0.2-5.2GHz
IIP3 (dBm)	10.5	2.7	20	>0
Gain (dB)	14.6	15.3	16	13
NF (dB)	1.8	2.9	1.4	3.5
Power (mW)	5.4	20	23.4	19.6
Supply Voltage (V)	2.7	2.5	2.6	1.5
Process (μm)	0.25	0.25	0.25	0.18

CHAPTER 4

A HIGH LINEAR BROADBAND CASCODE LNA EMPLOYING COMMON-GATE LINEARITY ENHANCING TECHNOLOGY

The first LNA design, which will be placed in parallel with the existing receiver system, is targeted on the applications of the most commonly used 4G standard LTE, which is located on 700-800MHz. This is the most economical way to upgrade the existing (2G and 3G) devices to new 4G application without significant changes of the existing circuit. The frequency bands of GSM, Zigbee, and RFID are also covered since they are all located at the nearby frequency bands, 850MHz for GSM, 915MHz for Zigbee, and 900MHz for RFID.

This chapter presents a low power and noise, high linearity, wideband cascode LNA that targets on the multi-standard wireless communication applications including LTE, GSM, Zigbee, and RFID. The common source (CS) stage is the main nonlinearity source for a cascode LNA. A modified derivative superposition (MDS) technology is adopted to improve the linearity. In addition, when the operating frequency increases, the nonlinearity influence coming from the common gate (CG) increases and limits the linearity performance of the LNA. Based on the modified MDS technique, this work employs both the derivative superposition (DS) and a terminal LC resonator on the CG stage. The nonlinearity coming from the CG stage is degraded at a higher frequency and, at the same time, high linear bandwidth is also increased. The cascode LNA was designed, analyzed, and implemented using the IBM 0.13μm CMOS technology. The LNA achieved a third-order intercept point (IIP3) of +13.6dBm, 3dB NF and a 12dB gain in a wide frequency from 700MHz to 1.1GHz.

4.1 Introduction

The LNA in this design is targeted on applications to cover the three standards that range from 700MHz to 950MHz. The cascode amplifier has been adopted because of its reputation of high gain, good noise performance and high isolation characteristics. In the design of cascode LNAs, improving the linearity without sacrificing gain or/and noise figure is the most challenging task. The problem is more serious when the LNA is to be used in the multi-standard devices because of the in-band interferences. A linearization method for high frequency wideband applications is desired.

In order to improve linearity of the cascode amplifier, an optimal biasing technology was proposed in [79], in which the third-order derivative of DC transfer characteristics of the field-effect transistor (FET) is adjusted to zero by regulating the biasing voltage V_{gs}. However, the region with high linearity is narrow and the cancellation of third order transconductance is very sensitive to the biasing voltage.

Another method to extend the linearity bandwidth called the derivative superposition (DS) method was proposed in [80-85]. The technique is to combine two parallel transistors of different widths and bias voltages to achieve an extended linear range, in which the third-order derivative approaches to zero. However, IIP3 improvement is limited because of the feedback of the second order derivatives to the input through the gate to source capacitance C_{gs}. The second order derivatives contained in the feedback can generate higher-order derivatives. A modified DS method is proposed in previous designs. In this method, magnitude and phase of the second-order and the third-order nonlinearity contributions are regulated by inserting an extra inductor. As a result, the influence coming from the second-order derivative is reduced.

However, all the reported cascode linear methods consider the common-gate (CG) stage as an ideal current buffer and target only on improving the linearity of the common-source (CS) stage. As the operating frequency increasing, the nonlinearity influence coming from the CG stage becomes more serious and limits the cascode LNA linearity. The nonlinearity of the CG amplifier was analyzed in [99-102] but the analysis did not reveal the role of the CG stage in the cascode LNA. In [99], the effects of the CG stage nonlinearity on the linearity of the cascode were first analyzed. However, there is only a qualitative analysis and no improving method was proposed.

In this design, the cascode LNA is taken as a two-stage amplifier, which is composed of the CS and CG stage. The nonlinearity influence coming from the CG stage is analyzed in more detail. Based on the DS method, linearity of the CS and the CG stage are enhanced separately and at the same time, a high linearity in a relative wide range of frequency is achieved.

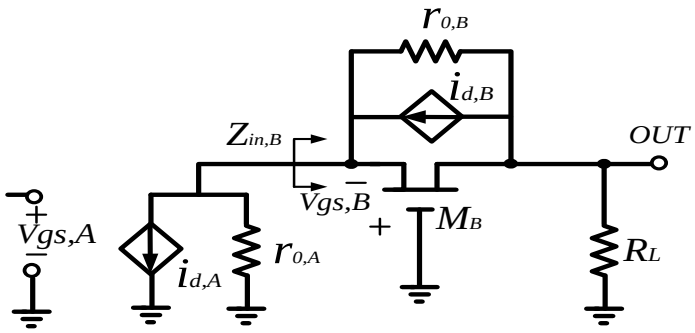


Figure 4.1 Circuit diagram for nonlinearity analysis of the CG stage in cascode LNA

4.2 Circuit Design & Analysis

4.2.1 CG Stage non-linearity analysis

Figure 4.1 shows the circuit diagram for the analysis of the CG stage nonlinearity in cascode LNA. The CS stage is modeled as a current source with output resistance $r_{0,A}$, and the current is controlled by the input voltage $V_{gs,A}$. The current of the CS stage $i_{d,A}$ is the input current for the CG stage. For conventional analysis, the CG stage is taken as an ideal current buffer and the currents of the CG ($i_{d,B}$) and CS stage ($i_{d,A}$) are identical. The current $i_{d,B}$ is driven by the gate-source voltage $V_{gs,B}$, which can be expressed as

$$i_{d,B} = g_{m1}V_{gs,B} + g_{m2}V_{gs,B}^2 + g_{m3}V_{gs,B}^3 + \cdots \tag{4.1}$$

where $g_{mn,B}$ is the nth order transconductance of the CG stage. The gate-source voltage $V_{gs,B}$ can be expressed as

$$V_{gs,B} = R_{in,B}i_{d,A} \tag{4.2}$$

where $R_{in,B}$ is the input resistance of the CG stage, then the drain current $i_{d,B}$ will be

$$i_{d,B} = \mathrm{g}_{m1}R_{in,B}i_{d,A} + \mathrm{g}_{m2}R_{in}^2 i_{d,A}^2 + \mathrm{g}_{m3}R_{in}^3 i_{d,A}^3 + \cdots \tag{4.3}$$

From Eq. 4.3, the second-order and the third-order nonlinear currents of the CG stage increase in proportion to the 2nd and 3rd order of $R_{in,B}$. Therefore, a smaller $R_{in,B}$ for the CG stage generates smaller nonlinear currents. $R_{in,B}$ is expressed as

$$R_{in,B} = \frac{r_0 + R_L}{1 + (1+\chi)g_m r_0} \tag{4.4}$$

where χ is given by

$$\chi = \frac{\gamma}{2\sqrt{V_{SB}+|2\emptyset_F|}} \tag{4.5}$$

V_{SB} is the voltage difference between source and body of the transistor. γ is the body effect parameter and $\emptyset_F$ is the junction potential. It is can be seen in Eq. 4.4, $R_{in,B}$ increases as the load resistance R_L increases and results in more nonlinear currents. In order to limit the nonlinearity coming from the CG stage, R_L should be chosen as small as possible. However, since the gain is proportional to R_L, there is a trade-off between the gain and linearity of a LNA.

Figure 4.2 shows the change of IIP3 of the cascode LNA at 1.5GHz with respect to the increase in the load resistance R_L. The simulation results indicate that there is an optimum value of the load impedance at which the output third order point, OIP3, can reach up to its maximum. This is the trade-off between the gain and linearity as earlier mentioned. The OIP3 curve is flat while R_L is ranging from 75Ω to 125Ω. Therefore, R_L can be changed in the range to balance the better trade-off between linearity and gain without big influence to the output linearity.

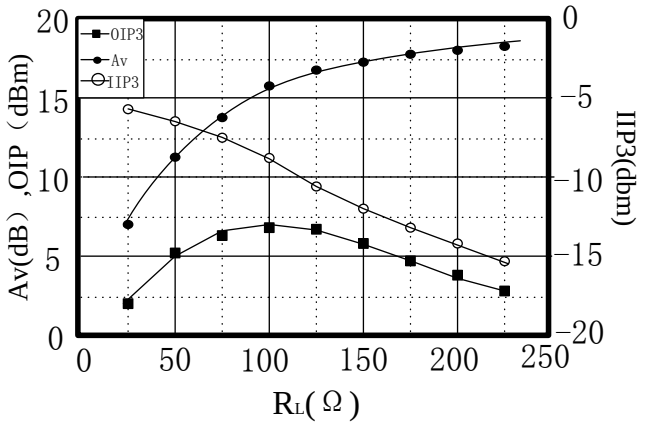


Figure 4.2 Gain, IIP3 and OIP3 of the cascode amplifier

From Eq. 4.4, another way to decrease $R_{in,B}$ is to increase χ. Increasing the body-effect factor λ and decreasing the source-bulk voltage V_{SB} of the CG stage have the same effect in raising χ. Both can be realized by putting the CG stage in a well where the doping density of P^+ is higher than the substrate.

To verify the analysis, a simulation was carried out with the CG stage being placed in the substrate and isolated deep doped P^+ well separately. The transistors are of the same size and under the same bias conditions. The IIP3 of the LNA increases while the CG stage is putting in a heavy doped P^+ well. In other words, connecting the bulk of the CG stage to the source instead of to the substrate can improve the IIP3 to some extent. However, the effectiveness depends too much on the process technology since γ is proportional to the doping density.

Based on the analysis, there are two linearization methods to improve linearity of a LNA. The first one is to limit the loading resistance R_L at the expense of sacrificing the gain. The second is to connect the bulk of the CG FET to the source instead of to the substrate, which is

realized by putting the transistor in a heavily doped well. However, both methods can only improve the linearity of the LNA in a certain bandwidth. The bandwidth of the LNA with high linearity is still limited. Also, the gain cannot be too high to realize a high linearity. In the following section, a LNA having high linearity in a wide bandwidth is proposed.

4.2.2 Circuit Design and Analysis for the Proposed Wideband High Linearity Cascode LNA

The DS linearity is the most effective method for improving the linearity and has been widely used because it does not have a significant influence to the LNA structure and is easy to be realized. However, the DS method is applied to the CS stage in previous works and only one IIP3 peak at the operating frequency can be achieved. As a result, the bandwidth of the high linearity LNA is limited. Since the cascode structure can be taken as two separate stages, assuming that the linearity of two stages are optimized independently to obtain IIP3 peak at the low frequency corner in Figure 4.3 (a) and at the higher frequency in Figure 4.3 (b) and they are merged together.

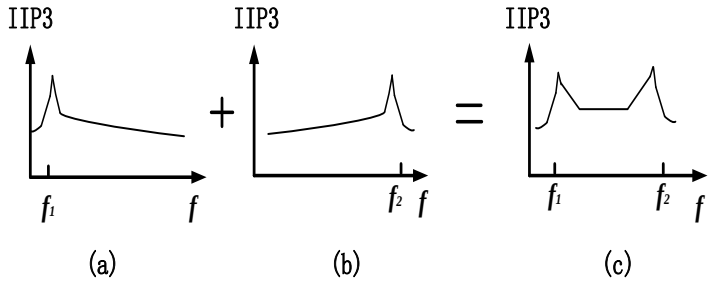


Figure 4.3 (a) IIP3 of the CS stage, (b) IIP3 of the CG stage, and (c) IIP3 for the entire circuit

The two independent IIP3 peaks over the wide frequency range can be achieved as shown in Figure 4.3 (c). Figure 4.4 shows the proposed LNA with linearity-enhanced topologies. In the following sections, the two stages are analyzed in detail.

(1) Common-Source Stage

As shown in Figure 4.4, the CS stage adopts the MDS linearity enhancement technology in which an extra gate to source capacitor C_{gs} is inserted. For the DS method, an auxiliary transistor (AT) with a proper size and bias voltage is added in parallel with the main transistor (MT) to compensate for the third-order nonlinearity.

The second transconductance of the MT has a negative peak in the saturation region, which severely decreases the linearity. The second order response of the AT with different size and biased voltage can be shifted to the right, the g_m'' of AT and the g_m'' of MT will cancel each other to drive the g_m'' of the LNA close to zero. In this way, the third-order nonlinearity will be eliminated.

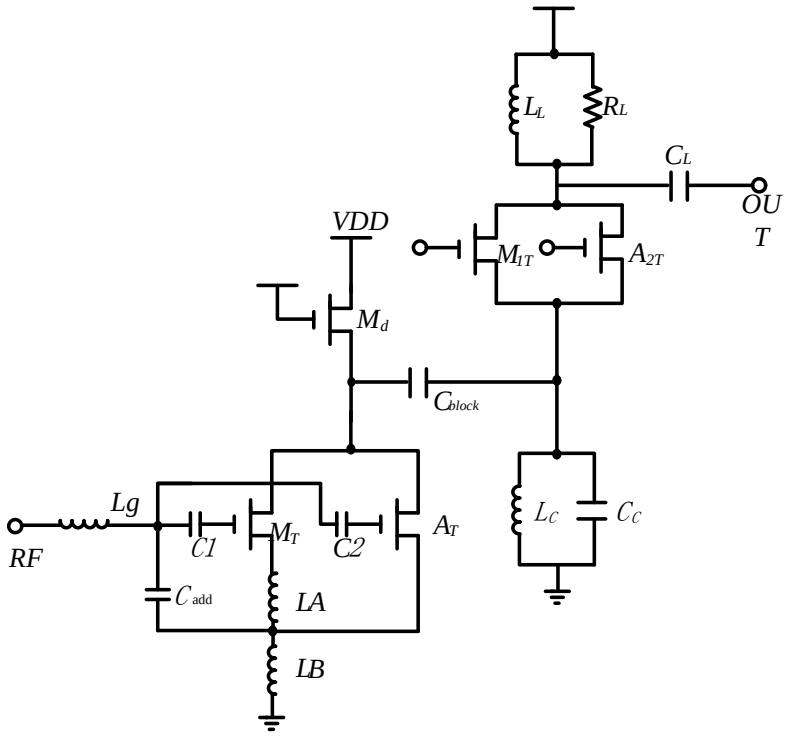


Figure 4.4 Circuit diagram of the proposed cascode LNA

However, for the DS technology, even the third-order nonlinearity can be cancelled by the AT $g_m^{''}$ compensation, the second nonlinearity component still exists and generates additional third-order nonlinearity through the source-gate feedback. The modified DS method proposed in this design addresses the issue of feedback of the second-order frequency components. In this method, the magnitude and phase of second-order nonlinearity contribution to the third-order components are tuned to cancel the third-order nonlinearity contribution, thus resulting in an output current with a minimum third-order component. As shown in Figure 4.4, the transistor MT is biased in the strong inversion region, while the transistor AT is biased in the weak inversion region. The two source degeneration inductors LA and LB connected to the sources of the two transistors are used to tune the magnitude and phase of the third-order components.

In the proposed design, an extra gate-to-source capacitance (C_{add}) is added. The quality factor of the input matching network is indicated as Q_{match} [53]. A lower Q_{match} results in a wider bandwidth, as shown in Eq. 4.6.

$$\frac{BW}{w_0} = \frac{1}{Q} \tag{4.6}$$

Because the Q_{match} is inversely proportional to C_{gs}, adding C_{add} will decrease Q_{match} and results in an increment in bandwidth. In addition, the total output noise will be further reduced by inserting a proper value of the parallel capacitance.

The input matching is mainly determined by the CS stage. Figure 4.5 presents the small signal equivalent circuit, and the input impedance is expressed in Eq. 4.7.

$$Z_{in} = sL_B + \frac{1+Sg_{MT}(L_A+L_B)+S^2C_{MT}L_A}{S(C_{AT}+C_{MT}+C_{add}+Sg_{MT}(C_{AT}+C_{add})L_B+S^2(C_{AT}+C_{add})C_{MT}L_A)} \tag{4.7}$$

Regarding the noise figure (*NF*), the system *NF* is described by the well-known Friis formula

$$F = 1 + (F_1 - 1) + \frac{F_2}{A_1} + \frac{F_3}{A_2} + \cdots \tag{4.8}$$

where F_i, A_i are the noise factor and gain, respectively, of the i^{th} stage down in the chain. Notes that the noise figure of the entire circuit mainly comes from the first stage, which is the CS stage in this case. The noise figure of the CS stage is expressed as:

$$F = 1 + \frac{\gamma' g_{d0,MT}}{4g_{m,TOT}^2 R_s Q^2} + \frac{\beta'(1+4Q^2)R_{s(\omega C_{gs})^2}}{g_{d0,AT}} \tag{4.9}$$

where γ' is the bias-dependent noise coefficient, which equals to 2/3 for long-channel devices but it is 2 to 3 for short-channel devices. g_{d0} is the zero-bias drain conductance of the device.

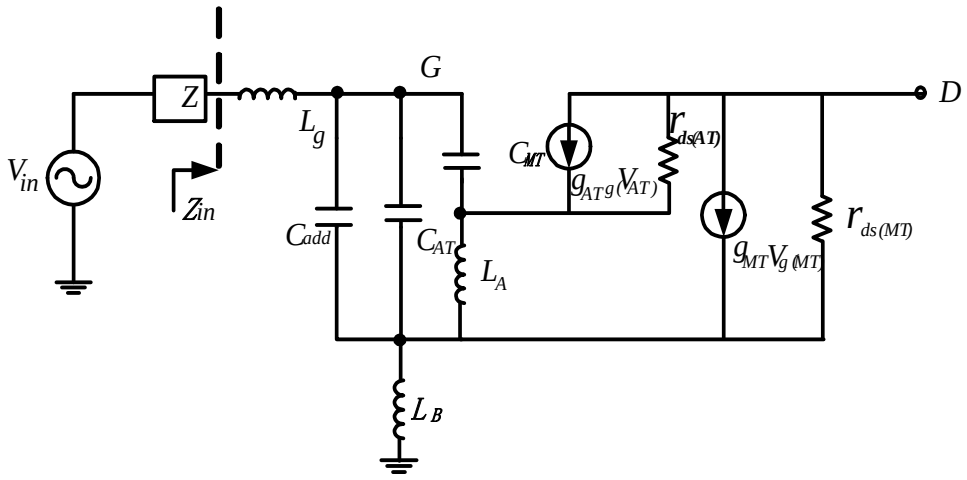


Figure 4.5 Equivalent small signal circuit for the common source stage of the proposed cascode LNA

(2) Common-Gate Stage

As indicated in previous analysis, the linearity of the CG stage decreases as the frequency increases. One way to limit the nonlinear current is to decrease the loading resistance by sacrificing the gain. Another way is putting the CG stage in a highly doped well but the procedure is expensive and the effectiveness is limited.

For the CG stage, the transconductance nonlinearity is also the dominant factor as shown in previous analysis. Therefore, it is possible that the DS compensation can also be applied to the CG stage. The negative value of the third transconductance of the main transistor is compensated with the positive value of the auxiliary transistor, as shown in Figure 4.6. This indicates the effectiveness of the DS technology for the third derivative cancellation.

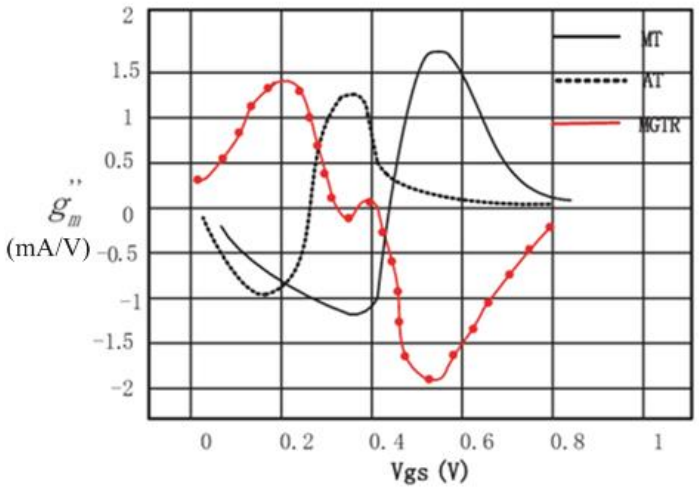


Figure 4.6 Transconductance cancellation of CG stage using DS technology

However, the input driving impedance, which is the output impedance of the CS stage, forms a voltage-current feedback path [103]. Even though the third-order coefficient can be reduced using the DS technology, the second-order nonlinear current can mix with the input through the feedback impedance and generate a third-order distortion. One of the best ways to eliminate the second-order harmonic feedback effect is adopting a RF current source in the high-frequency region. In this design, the CS stage can be seen as a current source with output impedance $Z_{cs.}$ The equivalent circuit for the CG stage is modeled in Figure 4.7.

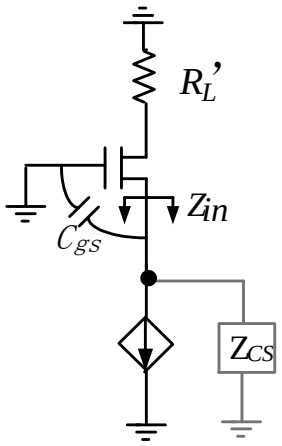


Figure 4.7 Common-gate stage equivalent circuit

V_{gs} and C_{gs} indicate the voltage and capacitance between the gate and the source of the common gate transistor. R_L' represents the load resistance at the operating frequency. The total input impedance of common gate stage Z_{in}, total is given by [104]

$$Z_{in,toal} = \frac{R_L' + Z_{in,d}}{1 + g_{m2} Z_{in,d}} \tag{4.10}$$

where

$$Z_{in,d} = Z_{in} // \frac{1}{jwC_{gs}} \tag{4.11}$$

$Z_{in,d}$ is the impedance looking back from point A. It indicates the equivalent impedance of the entire CS and CG stages.

Assume the operating frequency is ω, according to [98], the IIP3 can be expressed as

$$IIP3 = \frac{g_{m1}}{6} \frac{1}{|(1+g_{m1}A_1(j\omega))|A_1(qjw)|^2 K(\omega)|} \times R_s \quad (4.12)$$

where

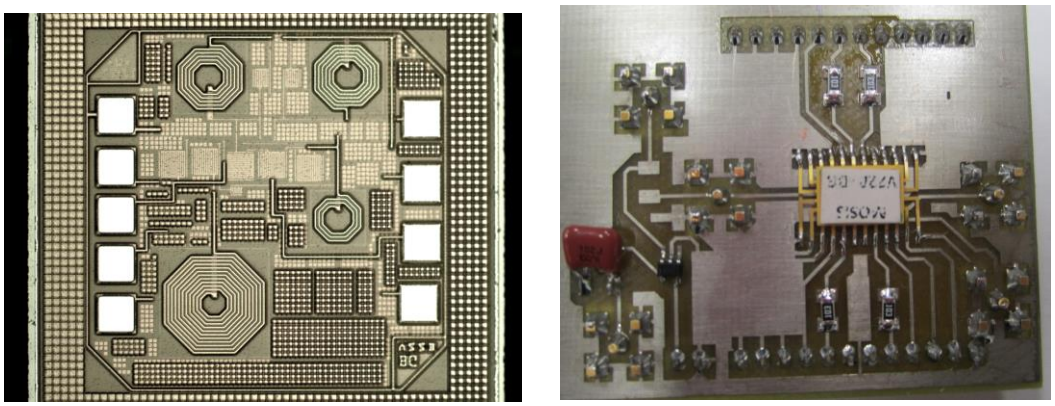
$$K(\omega) = g_{m3} + \frac{2}{3} g_{m2}^2 \left[\frac{1}{Y_T(2j\omega)+g_{m1}} + 2\frac{1}{Y_T(j\Delta\omega)+g_{m1}} \right] \quad (4.13)$$

and $\Delta\omega$ is the frequency difference of the two interfering frequencies. $Y_T(2j\omega)$ and $Y_T(j\Delta\omega)$ are the admittance at 2ω and $\Delta\omega$ separately.

From Eq. 4.13, the IIP3 is limited by $K(\omega)$. IIP3 can be improved by minimizing the harmonic factor $K(\omega)$,which can be realized by decreasing g_{m3}, as well as g_{m2} with $Y_T(2j\omega)$ and $Y_T(j\Delta\omega)$. This affirms the previous analysis that both the third-order and the second-order non-linear currents can reduce IIP3. The DS technology is adopted to improve g_{m3}. The second-order part, as expected from Eq. 4.13, can be minimized by increasing $Y_T(2j\omega)$ and $Y_T(j\Delta\omega)$. This is achieved by adding one LC resonant tank in parallel to tune the input impedance [98]. The structure can provide high impedance at ω and small impedance paths to ground at $\Delta\omega$ and 2ω. Since the admittance $Y_T(2j\omega)$ and $Y_T(2j\omega)$ will be very small. In other words, the second-order non-linear current will be minimized.

4.3 Implementation and Measurement Results

The proposed linearization technique was implemented on the cascode LNA. The designed cascode LNA was fabricated using IBM 0.13μm CMOS technology and the die microphotograph is shown in Figure 4.8 (a). The core size of the LNA is 0.61mm x 0.4mm. The LNA was simulated and fabricated as a standalone device. A separate buffer was adopted for 50Ω output impedance matching. Figure 4.8(b) is the microphotograph of the testing board.



(a) (b)

Figure 4.8 (a) Microphotograph of the LNA, (b) Photograph of the Testing Board

The LNA is powered by a 1.2V supply and the power consumption is 9.2mW. The input matching and the gain are indicated by S11 and S21 of the LNA. In Figure 4.9, S11 is simulated below -10dB ranging from 700MHz to 1GHz, with a bandwidth of 300MHz. However, the measured S11 was shifted to a higher frequency, which is ranged from 900MHz to 1.35GHz. Figure 4.10 shows a maximum measured gain S21 of 12.6dB at around 900MHz with a variation 3dB over 1-1.3GHz. The measured peak appears around 1.3GHz.

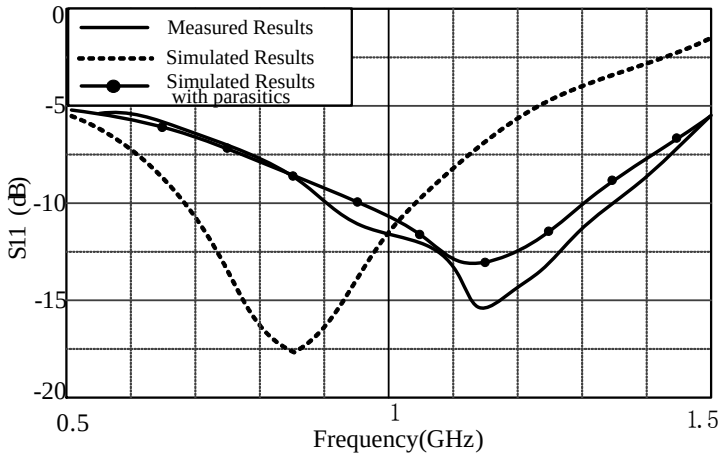


Figure 4.9 S11 of the LNA

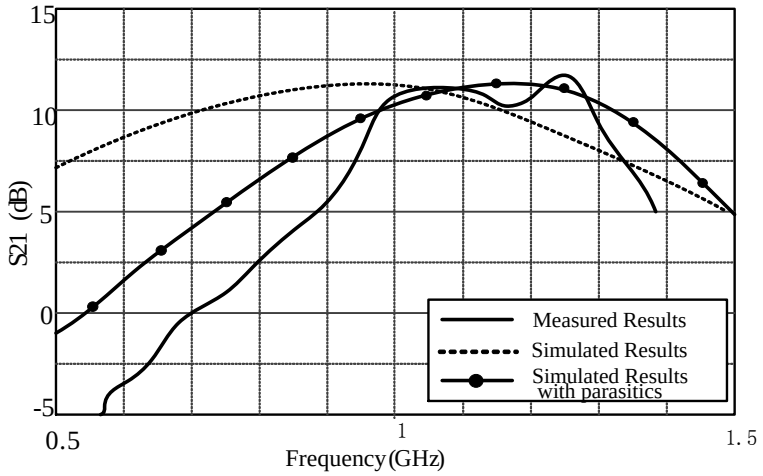


Figure 4.10 S21 of the LNA

As shown in Figure. 4.11, the minimum NF (3dB) also shifts to the higher frequency because of the shifted S11 and S21. The variations in the NF arise from the frequency-dependent gate induced noise and the load resistor noise. The cascode transistor also contributes a level of frequency-dependent noise.

The measured results shift to a higher frequency compared to the simulation results, which is mainly because the IC was tested using a printed circuit board instead of probe testing. All the inductance coming from the bonding wires and the traces on the PCB influence the resonant frequency of the LNA. To validate the analysis, simulation was performed with the consideration of the parasitic capacitance and inductance of the PCB board and bonding wires. The simulated S11 and S21 with parasitic parameters are shown by dotted lines in Figure 4.9 and Figure 4.10, respectively, and in general the results agree well with the measured results. Since S11 is shifted to the higher frequency, there will be lower power transferred in the lower frequency. Therefore, the S21 drops quite significantly in the lower frequency and the bandwidth is decreased.

In the wideband operation, widely spaced tones dominate the IIP3 and IIP2. For example, the targeted standards in this design (GSM, Zigbee, and LTE) can interfere one to each other. Thus the intermodulation products from the interferences with frequency spacing around tens of MHz need to be considered. For IIP3 measurement, two tones with 50MHz spacing were used. The IIP3 was tested in different frequencies and the results are shown in Figure 4.12. In the bandwidth ranging from 0.7-1.1GHz, the IIP3 has the minimum value of 7.5dBm and reaches up to 13.6dBm at the frequency of 900MHz. Since the optimized linearity frequency for the CS and CG stage are assigned to 800MHz and 900MHz, respectively, the measured results indicate the effectiveness of CS and CG stage linearity enhancing technique. The high linearity frequency range does not shift since the optimized frequency is pre-determined by confirming the transistor size and bias voltage.

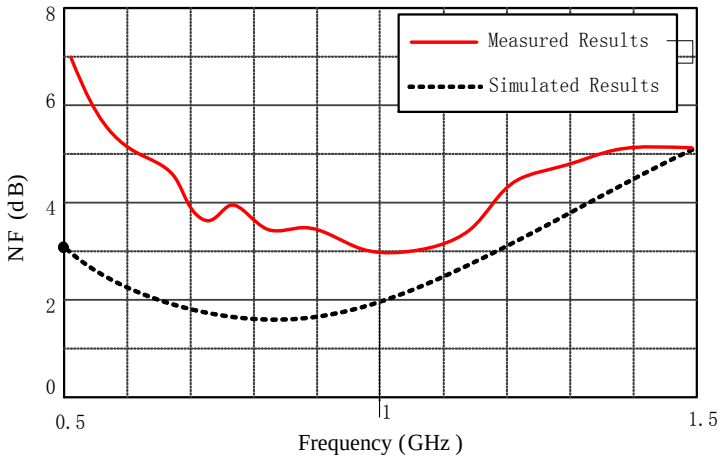


Figure 4.11 Noise Figure of the fabricated LNA

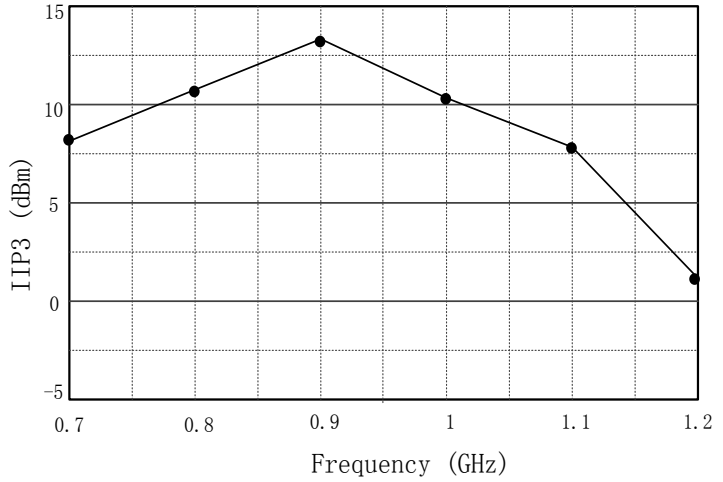


Figure 4.12 IIP3 of the LNA

As for reference only, the performance of this work is compared with other high linear LNAs located in the 900MHz frequency range, as shown in Table 4.1. Most of the previous designs just targeted on improving the linearity on a specific frequency. For multi-standard applications, the proposed LNA achieves a bandwidth of 300MHz with comparable linearity

(>7.5dBm). Although the work in [87] has the highest IIP3, the power usage is very high because of the trade-off between linearity and power consumption. Besides, the linearity is only optimized at 900 MHz and the high linear bandwidth is limited. The LNA proposed in [80] has a very wide bandwidth, however, its IIP3 is the lowest and both the NF and the power consumption are relatively high. Because of the influence of bonding wire and parasitic, the input matching and gain of this design shifted to the higher frequency range 1-1.3GHz.

Table 4.1. Performance Summary and Comparison with Previous Works

Article	[84]	[86]	[87]	[80]	[105]	[106]	This work
Technology	0.25µm CMOS	Bipolar	0.25µm CMOS	65nm CMOS	0.18µm CMOS	0.35µm CMOS	0.13µm CMOS
Frequency (GHz)	0.9	3	0.9	0.2-5.2	0.9	0.9	0.7-1
IIP3 (dBm)	10.5	14	17.2	0-4	9.4	5	7.5-13.6
Gain (dB)	14.6	6.5	15.5	15.6	14.9	18	>10
Noise Figure (dB)	1.8	1.9	1.6	2.9-3.5	1.8	2.6	3
Power (mW)	5.4	0.6	23.4	14	5.6	22.5	9.2

However, the shifted value of S11 (<-10dB), S21 (>10dB), and NF (<4dB) are still comparable. To resolve the shifting problem, instead of using package, the future design can be measured using probe testing by arranging the pads properly to fit the probe size.

4.4 Summary

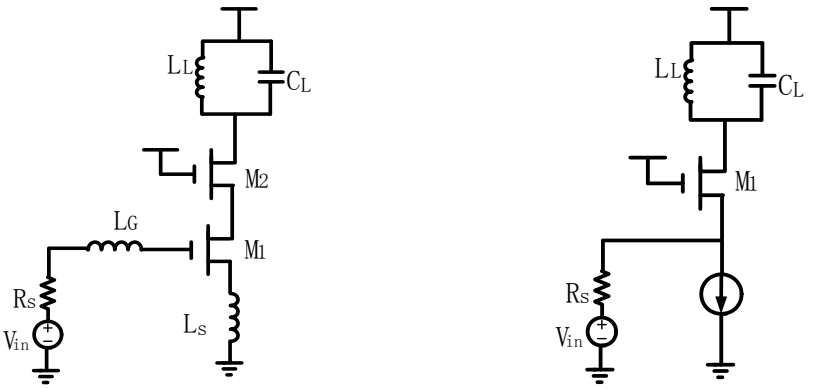
The effects of the CG stage nonlinearity on the linearity of the cascode LNA are investigated and analyzed in this chapter. For the traditional cascode LNA, decreasing the gain or putting the CG stage in a heavily-doped well can assist in improving the linearity at high frequency. However, each method has its own drawbacks and cannot effectively enhance the linearity. In this design, the cascode LNA is considered in two stages and the linearity of each stage is separately improved. For the CS stage, the MDS technology is adopted. For the CG stage, the DS technology is used along with the LC terminal, which can simultaneously decrease the third-order and second-order nonlinear current. The proposed cascode LNA was fabricated using IBM 0.13μm CMOS technology. The input matching S11 and gain S21 are shifted to the higher frequency range of 1-1.3GHz due to parasitic parameters of the testing PCB board. The fabricated LNA achieves a maximum gain of 12dB. The high linearity bandwidth still locates at the targeted frequency range of 0.7-1GHz because the optimized frequency is determined by the size and bias voltage of the transistors and the linearity is higher than 7.5dBm in the targeted range. The results indicate the effectiveness of the proposed linearity enhancing technology for wideband LNA.

CHAPTER 5

A LOW NOISE FIGURE 2-GHZ BANDWIDTH LNA USING RESISTIVE FEEDBACK WITH ADDITION INPUT INDUCTORS

During the transitional time from the existing 2G and 3G to 4G, the easiest way to implement a multi-standard receiver is to combine the existing receiver to a relatively narrowband receiver or LNA that is designed specifically for LTE, such as the LNA that was proposed in Chapter 4. However, chip area and system cost will be relatively high. A broadband low-noise amplifier that covers multiple standard bandwidths is preferred to reduce system complexity and have lower power consumption.

Most of the wideband LNAs proposed in previous works targeted frequency ranges between 3.1-10.6GHz, which is exceptionally defined by FCC for UWB (impulse pulse radio) applications [107]. The UWB system can only be used at a very low energy level for short-range, high-bandwidth communications with a large portion of the radio spectrum. Such wideband LNAs do not apply to the existing narrowband standards such as GSM, LTE, WCDMA, PCS, and WLAN, located in the lower frequency range and spanning from the 700MHz (GSM) up to 2.4GHz (WLAN). Therefore, a wideband LNA (1-3GHz) is proposed and described in this chapter. A novel input inductive network for the wideband LNA is suggested to enlarge the bandwidth. A -10dB S11 is achieved in a wide range of frequency from 1GHz to 3GHz. Within this bandwidth, the LNA has a gain of 7.5dB and a minimum NF of 2.5dB, while consuming 7mW of the power. The results indicate that the proposed input-network effectively alleviates the tradeoff between NF and bandwidth without requiring extra power consumption.



(a) **(b)**

Figure 5. 1 (a) Inductively degenerated common-source LNA (CS-LNA)
(b) Common-gate LNA (CG-LNA)

5.1 Conventional LNA Topologies

To enlarge the bandwidth of LNA, several topologies have been adopted for wideband impedance matching. For example, the common-source LNA combined with an LC filter [108], the common-gate LNA [109] and the resistive feedback LNA [110,111]. Each topology has distinct advantages and limitations. The common-source LNA with an LC filter can achieve broadband in the lower band range but consumes a substantial amount of DC power and chip area. The common-gate LNA and resistive shunt feedback LNA respectively suffer from big noise figure and high power consumption.

The inductively degenerated common-source LNA (CS-LNA), shown in Figure 5.1 (a), is the main topology due to its advantages such as low NF, ease of input matching, high gain, and low-power consumption. The input impedance is shown as:

$$Z_{in} = s(L_s + L_G) + \frac{1}{sC_{gs}} + (\frac{g_{m1}}{C_{gs}})L_s \tag{5.1}$$

Since the pure real impedance is only achieved at the resonant frequency, where $(L_s + L_g) + 1/sC_{gs} = 0$, the bandwidth of the CS-LNA is greatly limited. The common-gate (CG), as shown in Figure 5.1 (b), can provide a wide bandwidth using a small die area because no inductor is required for input matching, which is $Z_{in} = 1/g_m$. However, the pre-determined g_m limits the choice of the device size and power consumption. In addition, the CG amplifier has lower gain and poor NF when the operating frequency (ω_0) is very high [112]. Resistive shunt-shunt feedback is a common technique for wideband amplifier design. Figure 5.2 (a) and (b) shows a typical common-source amplifier with the resistive feedback and its equivalent small signal circuit.

M_1 is the input transconductance device, R_L represents the load resistance at the operating frequency, R_f is the feedback resistor and C_f is used just for DC blocking. When C_f is chosen to be large, it can be ignored in the analysis and the input impedance Z_{in} of the shunt-shunt feedback amplifier is given by

$$Z_{in} = R_{FB} // \frac{1}{sC_{gs}} = \frac{R_{FB}}{1+sC_{gs}R_{FB}} \tag{5.2}$$

where $R_{FB} = (R_f + R_L)/(1 + g_{m1}R_L))$ is the equivalent resistance looking into the feedback resistor R_f. C_{gs} and g_{m1} are the gate-source capacitance and transconductance of the transistor M_1, respectively. At low frequency, Z_{in} is dominated by R_{FB}, which is pre-determined to be 50Ω as the real part of the input impedance to be the matched impedance.

However, as the frequency increases, the imaginary part coming from the intrinsic capacitance C_{gs} also increases. Good input matching cannot be realized in the higher frequency range. To alleviate this problem, a series input inductor L_G is added in the gate of the transistor, as shown in Figure 5.2 (c) [113].

$$Z_{in} = (R_{FB} // \frac{1}{sC_{gs}}) + sL_G \tag{5.3}$$

According to [114], there are two frequencies at which a perfect match can be obtained. The first one is $\omega_1 = 0$, and the second one is $\omega_2 = 1/\sqrt{L_G C_{gs}}$. If ω_1 and ω_2 is not too far apart, a good input matching is achieved from ω_1 to ω_2. However, the NF for this structure is still very large due to the feedback path.

5.2 Proposed Low NF, High Gain LNA Architecture

To alleviate the tradeoff between NF and input matching, a new input scheme is proposed in this work, as shown in Figure 5. 3 (a).

Based on the resistive shunt-shunt feedback structure with the gate inductor L_G, an extra inductor L2 is inserted in the feedback loop. The introduction of L2 provides more freedom while balancing the trade-off between NF, bandwidth, and gain. More detail analysis is to be followed in the next sections.

5.2.1 Input Matching

Figure 5.3 (b) shows the small signal equivalent of the proposed amplifier. The DC blocking capacitors, C_{in} and C_f in the feedback path are shorted since they have small impedance at the

operation frequencies. In addition, the impedance of M2, $1/g_{m2}$, is much smaller than R_L and will be neglected in the following analysis. The input Z_{in} of the amplifier can be expressed as

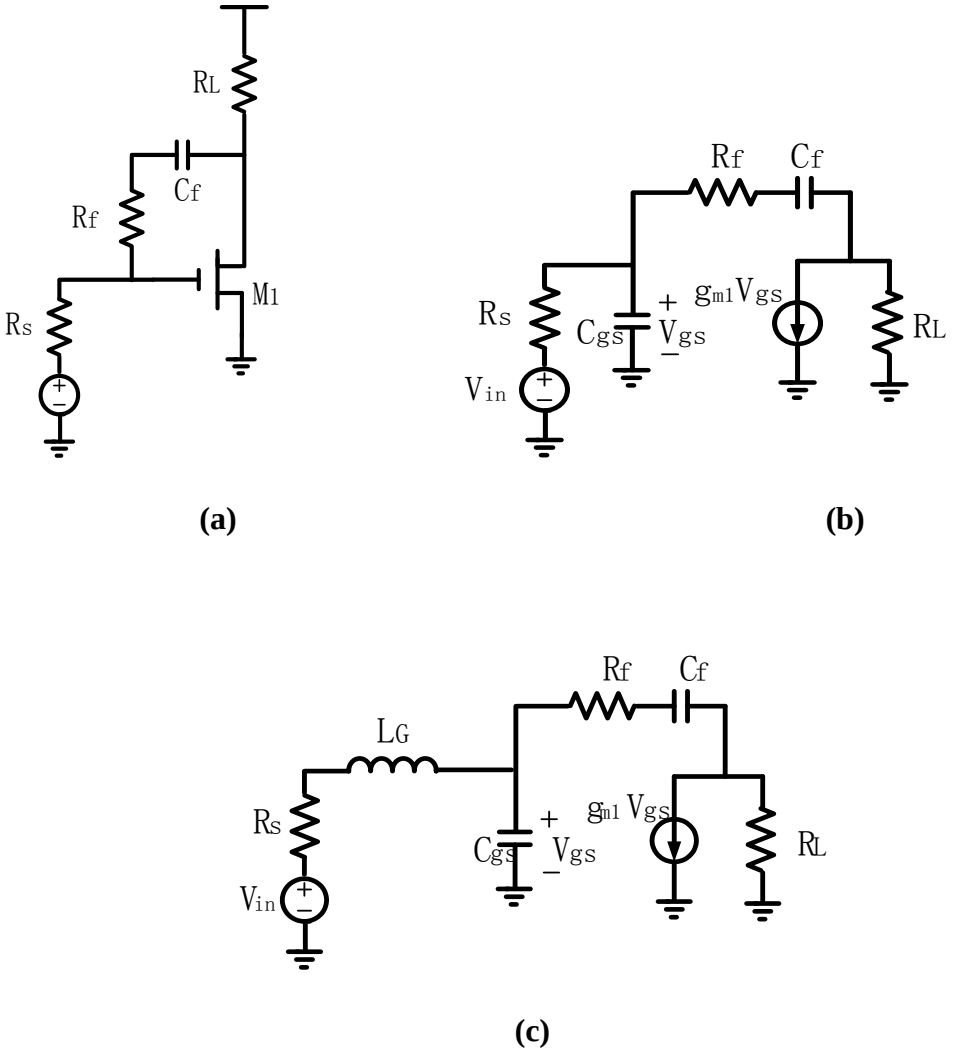


Figure 5. 2 (a) Schematic and (b) equivalent small signal circuit of the resistive shunt-shunt feedback amplifier. (c) Equivalent small signal circuit of resistive shunt-shunt feedback amplifier with additional series input inductor

$$Z_{in} = sL_1 + \left[\left(\frac{1}{sC_{gs}} + sL_2\right)||R_{FB}\right]$$

$$= \frac{s^3 L_1 L_2 C_{gs} + s^2 C_{gs}(L_1 + L_2) R_{FB} + sL_1 + R_{FB}}{s^2 C_{gs} L_2 + sC_{gs} R_{FB} + 1} \tag{5.4}$$

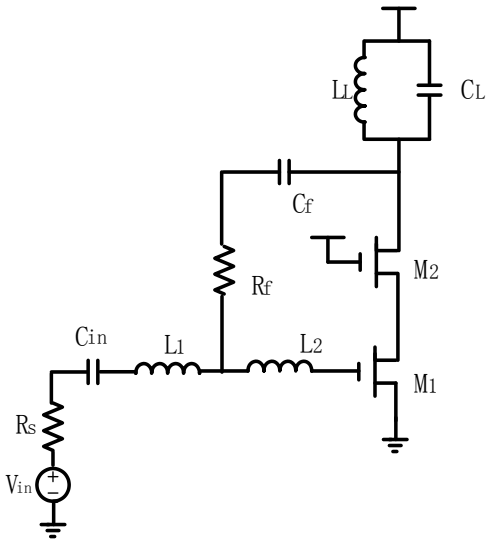
There are three perfect input impedance matching frequencies can be derived as follows:

$$\omega_1 \approx 0 \tag{5.5}$$

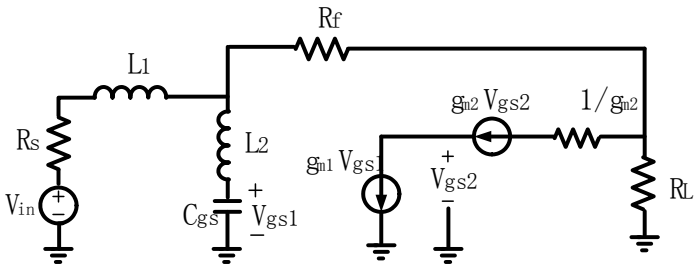
$$\omega_2 = \frac{-C_{gs}L_1R_{FB} + \sqrt{\left(C_{gs}L_1R_{FB}\right)^2 - 4L_1L_2C_{gs}(1 - C_{gs}^2R_{FB})}}{2C_{gs}L_1L_2} \tag{5.6}$$

$$\omega_3 = \frac{-\mathrm{C_{gs}L_1R_{FB}} - \sqrt{\left(\mathrm{C_{gs}L_1R_{FB}}\right)^2 - 4\mathrm{L_1L_2C_{gs}}(1 - \mathrm{C_{gs}^2R_{FB}})}}{2\mathrm{C_{gs}L_1L_2}} \tag{5.7}$$

In which ω_1, ω_2, and ω_3 are the frequencies at which a perfect match can be obtained. At $\omega_1 \approx 0$, the input impedance is chosen to be 50Ω to ensure the input impedance of the amplifier is well matched at the lower frequency. The other two frequencies, ω_2 and ω_3, given by Eq. 5.6 and Eq. 5.7 are the two other points where the good input matching is achieved. As a result, the two dips in the frequency response of S11 are predicted, which is proven to be true in the simulation results, as shown in Figure 5.4.



(a)

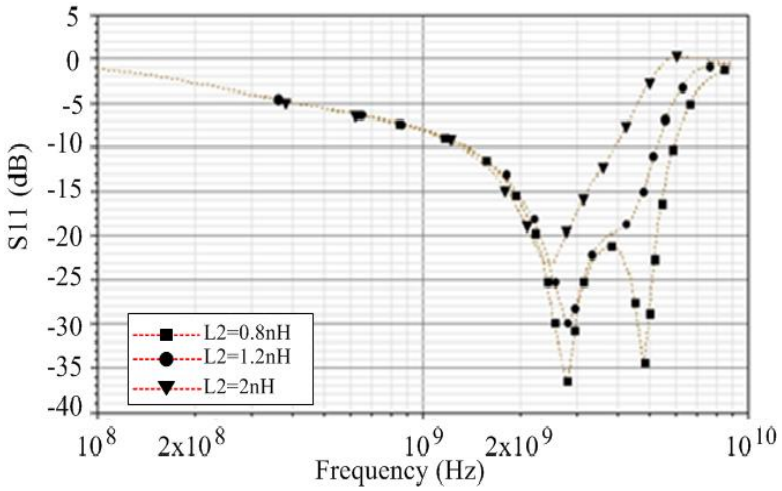


(b)

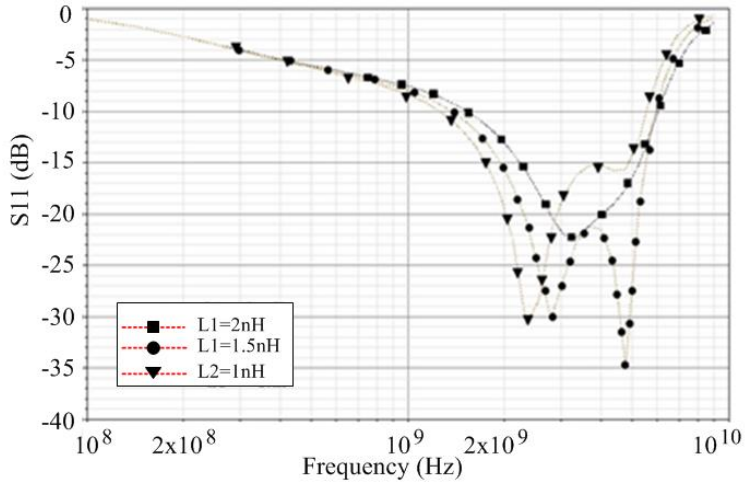
Figure 5.3 (a) The proposed resistive feedback LNA with separate input inductors (b) Equivalent small signal circuit

In Figure 5.4 (a), L1 was set constant at 1.5nH and L2 was varied. It can be seen that the frequency with good S11 goes up with the decreasing in L2. However, the two dips also increase which indicates the input matching is getting worse when enlarging the bandwidth. Similarly, when L2 is constant and L1 is changed, it is can be seen that the lower edge of S11 is getting lower when the value of L1 increases, but S11 is, again, getting worse. Therefore, the two

solutions in Eq. 5.4, ω_2 and ω_3, can be regulated by varying the value of L1 and L2. As shown in Figure 5.4, in the design process, one can try to vary the value of L1 and L2 to get the best balance between the input matching and bandwidth.



(a)



(b)

Figure 5. 4 Simulated S11 of the designed LNA for different inductors

5.2.2 Noise Figure

The cascode structure can be viewed as a two-stage amplifier, where the first stage is a common-source amplifier and the second stage is a common-gate amplifier. According to Friis equation, the noise figure for a series system is dominated by the first stage, therefore the cascode transistor is neglected in the following noise analysis. The small signal model of Figure 5.5 is employed to perform the noise analysis. R_{l1} and R_{l2} are the loss of the gate inductors L1 and L2. R_L is the load impedance. The noise factor of the proposed topology is given by

$$F = 1 + \frac{R_{l1}}{R_s} + \frac{R_{l2}}{R_s(1+g_m R_L)} + F_f + F_g + F_d \tag{5.8}$$

The second term and third term R_{l1}/R_s and $R_{l2}/R_s(1 + g_m R_L)$ represent the noise factor contributed by the inductor loss. Since R_{l1} and R_{l2} are much smaller compared with Rs, R_{l1}/R_s and $R_{l2}/R_s(1 + g_m R_L)$ will be much smaller than 1 and can be neglected. For the third term, F_f, which is the noise factor coming from the feedback resistor, can be expressed by

$$F_f = \frac{(R_f+2R_L)^2}{R_F R_L^2 (1+Q^2) g_m^2 R_s} \tag{5.9}$$

However, this expression is generated only under the narrowband assumption, a parallel-to-series impedance conversion can be applied to the input matching network. In that case, the noise factor F_f can be simplified to $1/g_m R_L$, which is relatively uncorrelated to the frequency and Q. For wide bandwidth, the case is similar and F_f is relatively constant and also smaller than 1, which is about 0.2-0.4 [114]. In this analysis, the maximum 0.4 is used. The last two terms in Eq. 5.8 are the noise factor coming from the amplifying transistor gate and drain current and they are the main contribution to NF. Then, the noise factor is simplified to

$$F = 1.4 + \frac{\gamma}{\alpha}\left[\frac{1}{Q} + 2|c|Q\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(\frac{1+Q^2}{Q}\right)\right]\left(\frac{\omega_0}{\omega_T}\right) \quad (5.10)$$

where α is the ratio between the device transconductance and the zero-bias drain conductance, γ is the factor of channel thermal noise, δ is the factor of the induced gate noise, and c is the correlation coefficient between the induced gate noise and the drain noise. For long channel devices, $\alpha = 1, \gamma = 2/3, \delta = 4/3$, and $c = -j0.395$.

From Eq. 5.10, one can see the noise factor F contains terms which are proportional to Q as well as inversely proportional to Q. Therefore, the minimum F exists for a particular Q.

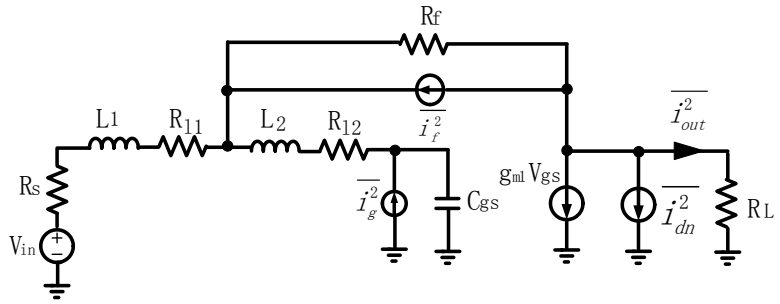


Figure 5. 5 Small signal model of the resistive feedback LNA for noise analysis

5.2.3 Gain

Feedback analysis [115] can be done by opening the loop and determining the open-loop trans-resistance gain R_{open}. The general feedback loop gain expression is given by

$$A = \frac{1}{\alpha_f}\frac{T}{1+T} \quad (5.11)$$

where α_f is feedback transconductance, $T = R_{open}\alpha_f$ is the loop gain and R_{open} is the open loop gain. In this design, the feedback type is shunt-shunt, whereas the input signal is a current quality. Therefore, V_{in} and Rs are replaced by a Norton equivalent as shown in Figure 5.6, $I_{in} = V_{in}/R_s$, and the feedback is broken for calculation.

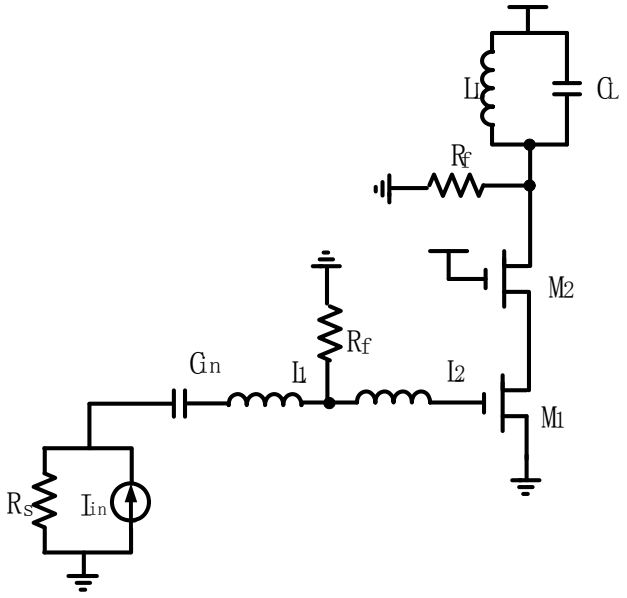


Figure 5.6 Small signal model of the resistive feedback LNA for noise analysis.

The open-loop gain, which is the trans-impedance of the transistor, can be expressed as

$$R_{open} = \frac{V_{out}}{I_{in}}|_{open} = -(R_s||R_f)g_{m1}(R_L||R_f) \tag{5.12}$$

Since the feedback network consists of only R_f, the feedback transconductance can be expressed as

$$\alpha_f = -1/R_f \tag{5.13}$$

and the loop gain is $T = R_{open}\alpha_f$. Thus the voltage gain is

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{I_{in}R_s} = \frac{1}{R_s}\frac{-(R_s||R_f)g_m(R_L||R_f)}{1+g_m(R_L||R_f)R_s/(R_s+R_f)} \tag{5.14}$$

Eq. 5.14 is only valid when the frequency is around zero, which is used for hand calculation to pre-determine the values of the resistors. When the frequency increases, according to [113], the voltage gain of the resistive feedback LNA can be expressed as

$$\mathrm{A_v} = \frac{-(R_s||R_f)(\frac{1}{R_f}-g_{m1})}{s^2+s\left(\frac{\omega_{pole}}{Q}\right)+w_{pole}^2} \tag{5.15}$$

where ω_{pole} and Q represent the pole frequency and quality factor, respectively of the circuit of the LNA. From Eq. 5.15, it can be seen that the bandwidth of the LNA is determined by both ω_{pole} and Q, which are mainly determined by of values of C_{gs}, L1 and L2. The value of C_{gs} cannot be changed once the size of the transistor is determined, therefore, the frequency response of the gain mainly comes from the inductors.

The quantitative analysis was given by doing simulation and observed that the gain peak and bandwidth is mainly determined by the inductor L2, as shown in Figure 5.7. It can be seen that as the inductance of L2 increases, the gain in high frequency is higher but the bandwidth is reduced.

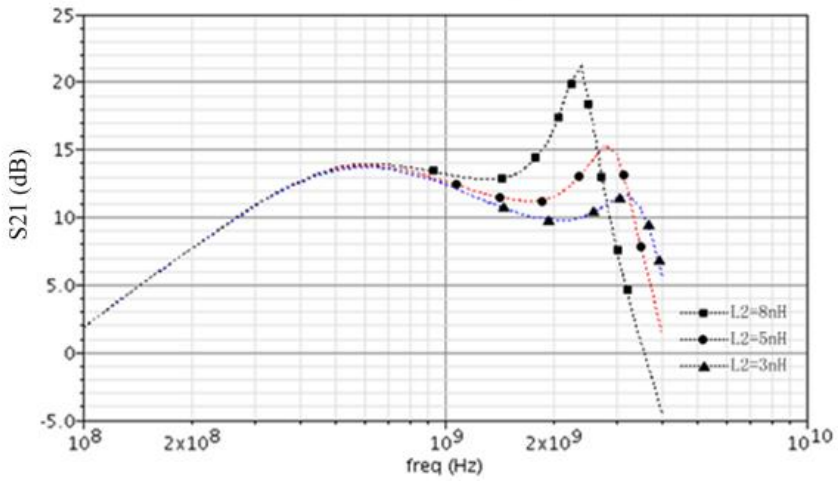


Figure 5.7 S21 of the LNA

5.3 LNA Design and Implementation

Based on the above analysis, a LNA was designed. There are two approaches for NF optimization, which are the fixed transconductance and the fixed power consumption. For the wide bandwidth design, a fixed gain is difficult to implement.

Therefore, in this design, the NF is optimized with a fixed power condition. According to the analysis in [53], the minimum NF and optimum *Q* factor are given by

$$F_{min,P_D} = 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right) \tag{5.16}$$

and

$$Q_{L,opt.} = |c|\sqrt{\frac{\gamma}{\sigma}}\left[1 + \sqrt{1 + \frac{3}{|c|^2}\left(1 + \frac{\sigma}{5\gamma}\right)}\right] \tag{5.17}$$

in which $\gamma = 2.5,\ \sigma = 5,\ |c| = 0.395$. The minimum NF and the optimum *Q* become

$$F_{min} \approx 1 + 1.62\left(\frac{\omega_0}{\omega_T}\right), \text{ and } \quad Q_{opt} \approx 3.9 \tag{5.18}$$

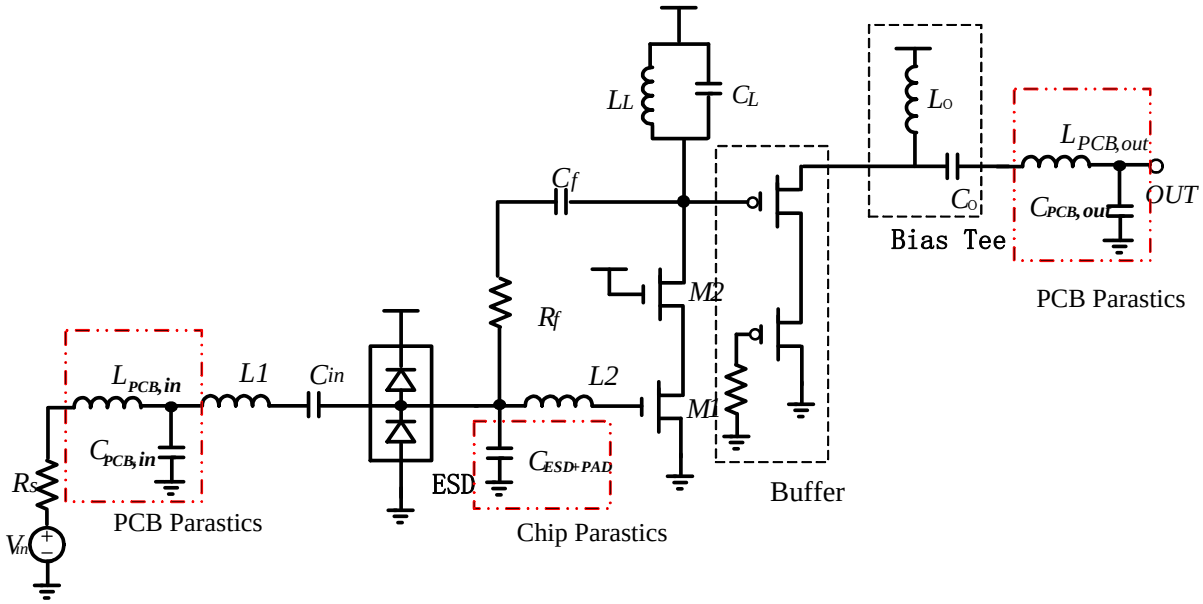


Figure 5.8 A complete schematic of the LNA.

For wideband LNAs, a relatively low and flat NF is required instead of just a minimum F at a particular frequency. This can be realized by making the minimum F locate at the central frequency. Since Q can be expressed as $Q = (\omega_0 L_{ser})/R_{ser}$, $L_{ser} = L_1 + L_s$, $R_{ser} = (R_f + R_L)/(1 + g_m R_L) \approx 50$, the quality factor, Q is now expressed as

$$Q = \omega_0 \frac{(L_1 + L_2)}{50} \tag{5.19}$$

By regulating the inductances of L1 and L2, one can make the optimized Q locate at the center frequency of the desired frequency range. Therefore a relatively flat and low noise factor can be achieved. In previous designs, as shown in Figure 5.2, the inductance of the input inductor

L_G is pre-determined for the input-matching consideration. The frequency location of optimized Q cannot be adjusted.

After determining the minimum NF and optimum Q_L, the sum of L1 and L2 are confirmed as well. It is not the same as previous designs, there are more freedom in balancing the input matching, NF, and gain. As previously analyzed, both S11 and S21 can be adjusted by regulating L1 and L2 independently. Therefore, even the sum of L1 and L2 is pre-confirmed by the NF optimization, the value of L1 and L2 can also be regulated separately to get the best balance according to the specifications.

Most of the existing wireless communication standards nowadays are located in the GHz range, such as 2GHz for the UMTS, 0.9 GHz and 1.9GHz for GSM in Canada and USA, 2.4GHz for WiFi, 1.7-1.9GHz for LTE, and so on. Therefore, in this design, the center frequency is chosen to be 2.4GHz with the attempt to cover most of the wireless standard ranges. To demonstrate the performance of the proposed LNA, the LNA was designed and fabricated in a standard 8-metal 0.13μm CMOS technology. The complete schematic of the LNA is shown in Figure 5.8. The core amplifier is a cascode structure, which can improve the reverse isolation and reduce the Miller effects. The input inductor L1 is formed by the bonding wire inductance for space saving. The ESD protection Pcell is included in the 0.13μm CMOS RF library, which are four bipolar transistors connected in series. The LNA has been designed using standard V_{th} transistors, metal-insulator-metal (MIM) capacitors, and standard spiral inductors. The output buffer is a source follower structure, which transfers the voltage to the power gain. Figure 5.9 is the photograph of the wideband LNA. The die has a small chip area of only 0.28x0.61mm^2. The parameter of the components can be found in Table 5.1.

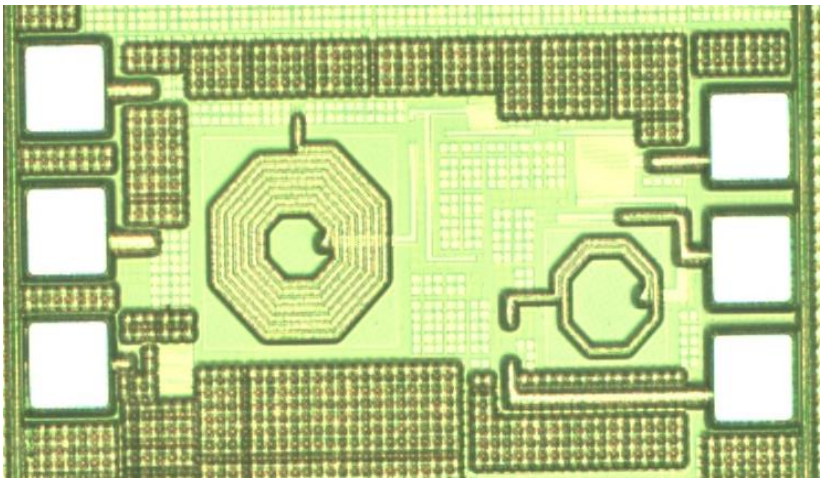


Figure 5.9 Die photograph of the LNA

Table 5.1. Value of the components of the proposed LNA

Component	Value	Component	Value	Component	Value
M1	0.12/250 μm	R_f	280Ω	$C_{PCB,in}$	0.072pF
M2	0.12/200 μm	C_f	2pF	$C_{pad+ESD}$	By Spice
L1	2nH	L_L	5nH	$L_{PCB,out}$	1nH
L2	5nH	C_L	5pF	$C_{PCB,out}$	0.072pF
C_{in}	10pF	$L_{PCB,in}$	2.9nH		

5.4 Simulation and Testing Results

To demonstrate the performance of the proposed technique, the LNA was designed and fabricated in the standard 8-metal 0.13μm IBM CMOS process. Figure 5.9 shows the photograph of the wideband LNA. The die was bonded in a high-frequency package (CQFP44) for testing.

The LNA is powered by a 1.2V supply and the current consumption of 6mA was measured. For S11 and S21, the simulation results are for both schematic and post-layout simulation results with consideration of the PCB parasitic parameters. Testing results are indicated by the lines with circle, rectangle and square respectively in Figure 5.10 and Figure 5.11. The simulated and tested S22 results are also shown in Figure 5.11. In the targeted frequency range (1-3GHz), the measured input reflection coefficient S11 is less than -10dB except for the small peak between 2-2.3GHz due to the input matching influence coming from the testing PCB board. The measured small signal gain (S21) achieves a maximum value of 16.5dB at 2.2GHz, and has a minimum value of 7.5dB at 1.7GHz. In this frequency range, the measured output return (S22) is less than -10dB.

In general, the test measurements agree well with the simulation results. However, at the frequency around 1.7GHz, the measured S11 goes up as shown in Fig. 9, which means there is lower signal power is transmitted into the LNA. Therefore, the S21 should also degrade at this frequency as shown in Figure 5. 11.

The measured S21 agrees with the analysis, which decreases at near 1.7GHz range. The discrepancy between measured and simulated results mainly comes from the parasitics from the chip and the testing PCB board, as shown in Figure 5.8. The parasitic capacitance of the pads and ESD components on chip are mainly extracted and taken into post-layout simulation by Spectre. Since L1 is realized by the bonding wire, the equivalent capacitor of the pads and ESD cell is put after L1.

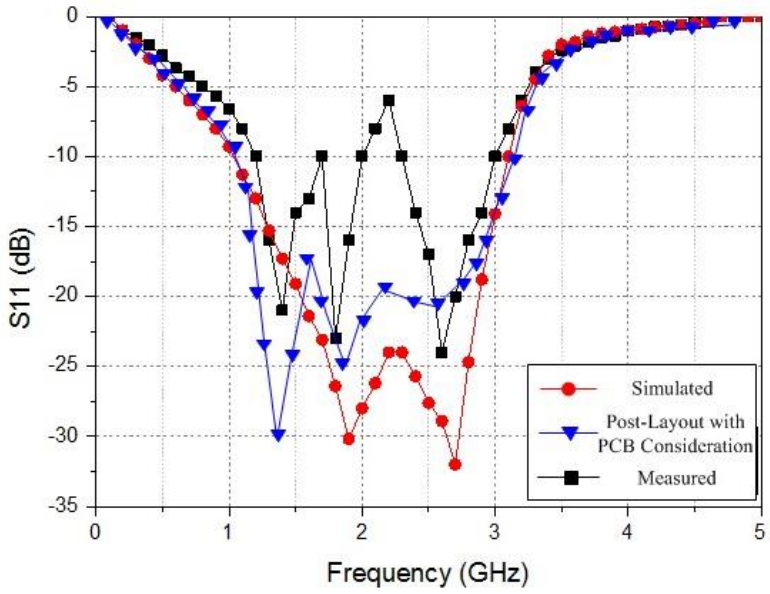


Figure 5.10 S11 of the LNA

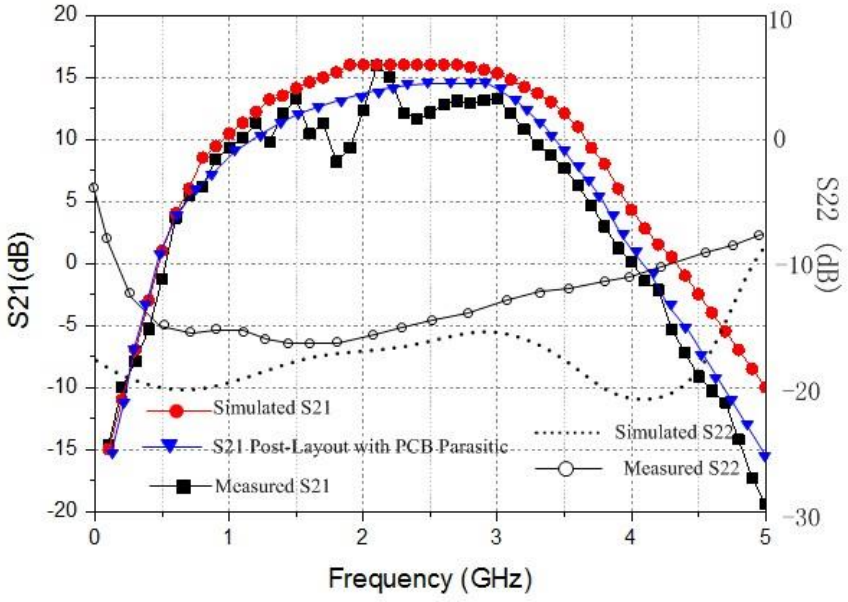


Figure 5.11 S21 and S22 of the LNA.

For the PCB parasitics, there are two main sources. One is the parasitic capacitance that mainly contributed by the sealing pads and another parasitic is the inductance coming from the PCB traces. The values can be approximated by the size of the PCB wires and sealing pads, as indicated in Table 5.1. After the parasitic parameters are taken into account, post-layout simulations and the simulation results are well aligned with the measurements except the sawtooth shape in the measured S21.

The sawtooth is partly coming from the not so perfect input matching, which has been indicated in the post-layout simulation, where the S21 decreases in 1.4-2GHz. Besides, the sawtooth shape of the response can come from coupling problems on both the PCB and the chip, which is difficult to simulate. In the future design, the layout for both PCB and die should be more carefully considered.

The simulated S22 is lower than -15dB in the 1-3GHz frequency range. The discrepancy can be attributed from the source follower used for output matching. It is worth to mention in the actual measurements, it is very difficult to bias the circuit exactly the same as it was used in the simulations.

Figure 5.12 shows the schematic simulation, post-layout simulation, and measured NF from 1 to 3GHz of the designed LNA. The results show a minimum NF of 2.1dB at 1.5GHz and a maximum NF of 5.4dB at 3GHz (within the 1-3GHz range as the design parameter). The sharp rise of the measured NF above 2GHz was not observed in simulations but appears in the measurement results. This is partly due to the degradation of S22 at higher frequency and is partly due to the high-frequency noise coming from the measurement setup.

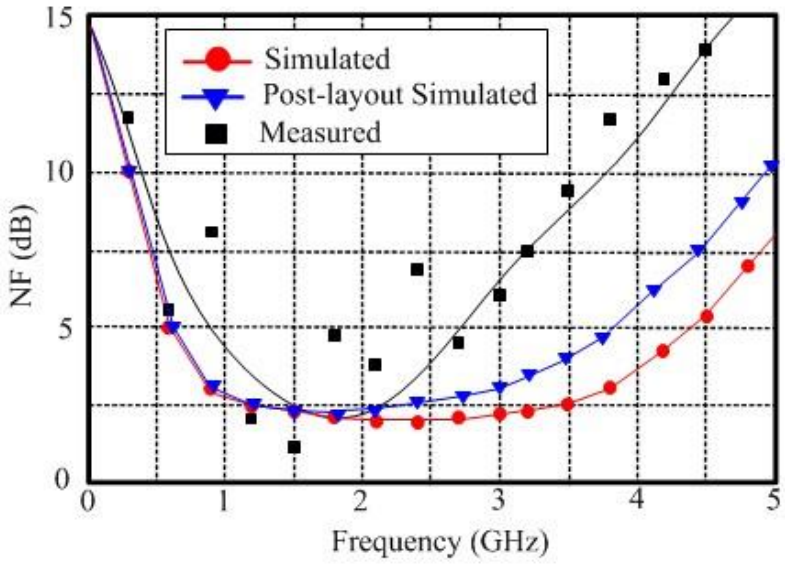


Figure 5. 12 Noise Figure of the LNA.

The NF below 2GHz is measured by a NF testing function of the HP network analyzer. The NF in the frequency above 3GHz was measured by a noise source and a noise meter. The method may increase value of the measured NF.

Table 5.2 summarizes the performance of the designed LNA and compares with those of other recent designs. As shown in the table, the proposed design achieves the second highest gain and the second lowest NF with low power consumption. The wideband LNA with added inductor benefits the best trade-off between NF, wideband input matching, high gain, and moderate power consumption.

5.5 Summary

In this chapter, a novel input network for the wideband LNA is proposed combined with the conventional resistive feedback structure. By inserting two input inductors in and out of the feedback, more freedom of choices are introduced in the design process. This structure is

applicable to the multi-standards applications due to its high performance in a very wide bandwidth. At first, the frequency range and central frequency are chosen according to the specifications. The optimized *Q* is chosen then the minimum NF is obtained in the central frequency. Since only the sum of L1 and L2 is limited by the optimum *Q*, the value of L1 and L2 can also be regulated accordingly in order to get the best balance between input matching and gain. If the covered standards changing, the S11 and S21 edges can be adjusted easily by changing the value of L1 and L2. The cascode LNA was designed and fabricated using IBM 0.13um CMOS technology. A high and flat gain (greater than 10dB) with a 16.5dB peak is achieved in a wide frequency range (1-3GHz), the S11 is below -10dB in this range and a minimum NF of 2.5dB is achieved. The power consumption is only 7mW on a 1.2V supply. The proposed input-network can be easily realized and effectively alleviates the tradeoff between NF, input matching and gain without extra power consumption.

Table 5.2 Performance Summary and Comparison with Previous Works

Parameters	[113]	[116]	[117]	[89]	[118]	[119]	This work
CMOS	130nm	180nm	90nm	130nm	130nm	180nm	130nm
Frequency (GHz)	2.4	2-4.6	2.5-4.0	0.8-2.1	0.2-3.8	1.05-3.05	1-3
Supply Voltage (V)	1.2	1.8	1	1.2	1	1.8	1.2
Power (mW)	4.8	12.6	8.0	17.4	6	12.6	7
Max. Gain (dB)	28	9.8	19.6	14.5	13	10.9	16.5
Noise Figure (dB)	2.0	2.4	4.0	2.6	3.4	2.6	2.4
Core Area (mm^2)	0.578	0.6	0.2	0.9	0.025	0.073	0.7

CHAPTER 6

A 0.1-8 GHZ WIDEBAND LOW-NOISE AMPLIFIER EXPLOITING GAIN-ENHANCED NOISE-CANCELLING TECHNIQUE

Although LTE is generally considered to be the dominant wireless technology in the near future, WiMAX, the other candidate for 4G, is another promising technology. However, there is no uniform global licensed spectrum for WiMAX, the spectrums are very fragmented and vary from country to country. The bandwidth of the third design will be enlarged further to cover all the LTE and WiMAX frequency ranges. Targeted on the third design, an ultra-wideband LNA that can support the two different 4G standards (LTE and WiMAX) at the same time is presented.

In this design, a modified noise cancelling architecture is exploited, which extends the bandwidth and a gain enhancing component is added for gain compensation. Conventional wide band LNAs suffer from serious tradeoff between the wide-band input matching and high gain. Based on the conventional noise cancelling technology, a gain enhanced noise cancelling architecture is proposed. For the input matching, a common source stage with active feedback is adopted to relax the trade-offs between gain and bandwidth. A peaking inductor is inserted to improve the gain flatness and the bandwidth. For the noise cancelling stage, a common gate stage is added in the forwarding path and therefore the overall signal gain is improved by the factor of the A_{v2}, which is the gain of CG stage.

Section 6.1 reviews wideband noise cancelling techniques. Section 6.2 presents and discusses in detail of the modified wideband noising cancelling architecture with higher gain and wider bandwidth. Section 6.3 is the experimental results and Section 6.4 gives the conclusions.

6.1 Detail Analysis of Existing Wideband Noise Cancelling Techniques

The noise-cancelling technology is originally proposed in [120]. The basic concept is to generate the noises with the opposite phase and signals with the same phase in different paths. By summation at the output, the signals are added while the noises are cancelled with each other. Since the cancellation method has no relevance with the input impedance, the technique allows for simultaneously noise cancellation and impedance matching. The basic structure is shown in Figure 6.1.

The channel thermal noise is considered as the dominant noise component in the CMOS device. Therefore, the common-source stage, *M1*, is modeled as a noise current source between the drain and the source. R_f is the feedback resistor, which is used for the wideband input matching. The feed-forward voltage amplifier has the gain of A_V.

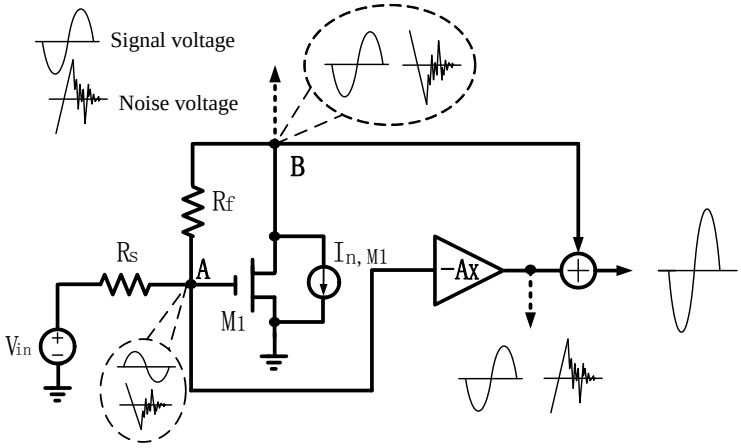


Figure 6.1 Simplified resistive shunt feedback LNA using a conventional noise cancelling technique

A portion of the noise current flows through the feedback resistor R_f to the gate of the amplifier and generates the noise voltage V_A, V_B at the node A and B with the same phase polarity separately. Assuming the input impedance is *Rs*, the noise voltages at A and B can be expressed as

$$V_{A,n} = \alpha I_n R_s \tag{6.1}$$

$$V_{B,n} = \alpha I_n (R_s + R_f) \tag{6.2}$$

where $0 < \alpha < 1$, which is the percentage of the noise current that flowing to the feedback resistor.

On the other hand, the signal voltages at nodes A and B have the opposite polarity because the common-source amplifier has an inverting gain. The differences of signal and noise polarities at node A and B make it possible to cancel the noise while adding the signal contributions. This can be realized by the feed-forward amplifier, which adding one negative scale to the voltage at node A. The output noise voltage after the noise cancelling operation can be expressed as

$$V_{out,n} = \alpha I_n \big(R_s + R_f\big) - A_X(\alpha I_n R_s) \tag{6.3}$$

To ensure the $V_{out,n}$ equals to zero, the gain of the feed-forward amplifier should be

$$A_X = 1 + \frac{\mathrm{R}_f}{R_s} \tag{6.4}$$

It can be shown that, when the A_X equals to $1 + (\mathrm{R}_f/R_s)$, the noise of the input transistor M1 can be cancelled at the output, and the signal gain is enhanced. Assuming the input impedance of the amplifier matches the source impedance, the overall gain for the signal is

$$A_v = \frac{V_{out}}{V_A} - R_f(g_{m1} + \frac{1}{R_s}) \tag{6.5}$$

Assuming the input impedance $Z_{in} = 1/g_m = R_s$, *Av* can be expressed as:

$$A_G = -2\frac{R_f}{R_s} \tag{6.6}$$

To sum up, the noise cancelling architecture can be modeled as the combination of the input matching amplifier and the noise cancelling amplifier path, as indicated in Figure 6.2.

Figure 6.3 shows the LNA designs in previous publications that exploiting thermal noise cancelling technique. In Figure 6.3 (a), the wideband input impedance matching path is realized by the common-source stage (M1) with local resistive shunt-shunt feedback. M2 is the cascode stage for isolation. For the noise cancelling concept, the noise current of M1 (and M2) flows out of node B through the feedback resistor R_f and therefore the noise voltage at node A and node B have equal sign. The combining stage is realized by M3 and M4. Both the signal and noise voltages at node A are amplified inversely by the common-source stage M3 while the signal and noise voltages at node B are just transferred by the source follower stage M4 with no inversion. Therefore, the equal signed signals and opposite-signed noise voltages are produced and added together at the output. To make sure the noise can be cancelled at the output, the voltage of common-source stage M3 should equal to A_X, which is $1 + (R_f/R_s)$, as shown in Eq. 6.4. In the meantime, the overall signal gain is $-2(R_f/R_s)$, as indicated in Eq. 6.6.

From Eq. 6.6, it can be seen that the signal gain Av is proportional to R_f. However, a large R_f induces much more thermal noise. Also, the bandwidth for the shunt-shunt feedback structure

is mainly determined by the resistance of R_f . As R_f is to be increased to improve the gain, the bandwidth will also be reduced.

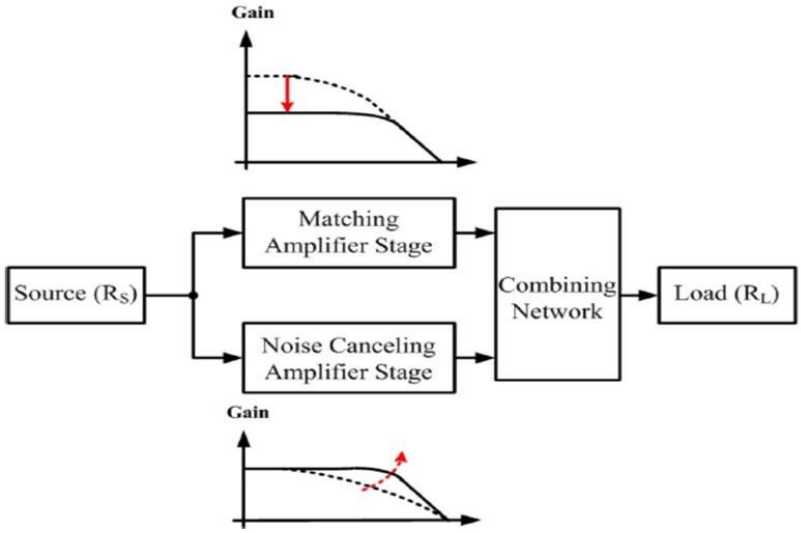
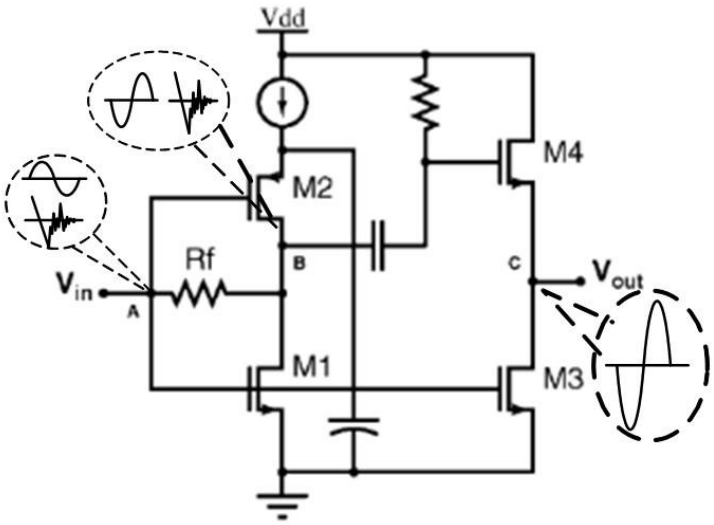
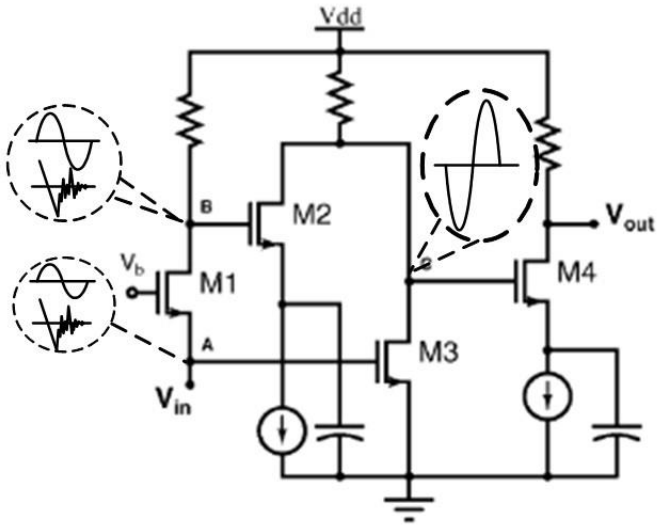


Figure 6.2 Basic structure of the noise cancelling method

A noise cancelling configuration, as shown in Figure 6.3 (b) is proposed in [89]. Instead of using the resistive shunt feedback structure, a common-gate input stage is employed for the wideband input matching. The principle for noise cancelling is similar. The noise current of M1 flows into node A but out of node B and therefore two fully correlated noise voltages with opposite phases are created. These two noise voltages are amplified by M2 and M3 respectively. By properly designing M2 and M3, the noise coming from the main transistor M1 can be cancelled at the output. On the other hand, the signals at nodes A and B have the same phase and are added together at the output. However, common-gate structure has the impedance matching problem in high frequency and cannot provide a very high gain.



(a)



(b)

Figure 6. 3 (a) Common-source LNA and (b) Common-gate LNA exploiting noise cancelling

Therefore, for both noise cancelling architectures, there is less freedom in controlling the gain performance, especially in the high frequency range. The trade-off between gain and bandwidth for the noise cancelling technology is more serious, even if the input matching and noise cancellation are both completed. Based on the conventional noise cancelling technology, a gain enhancing technique is proposed in this design.

6.2 Gain-Enhanced Wideband Noise Cancelling Technique

6.2.1 Basic idea of the gain-enhanced noise cancelling technique

Figure 6.4 shows the simplified schematic of the proposed modified gain-enhanced noise cancelling architecture. Compared with the traditional noise cancelling structure in Figure 6.1, there is an extra voltage amplifier A_Y is added in the feedforward path.

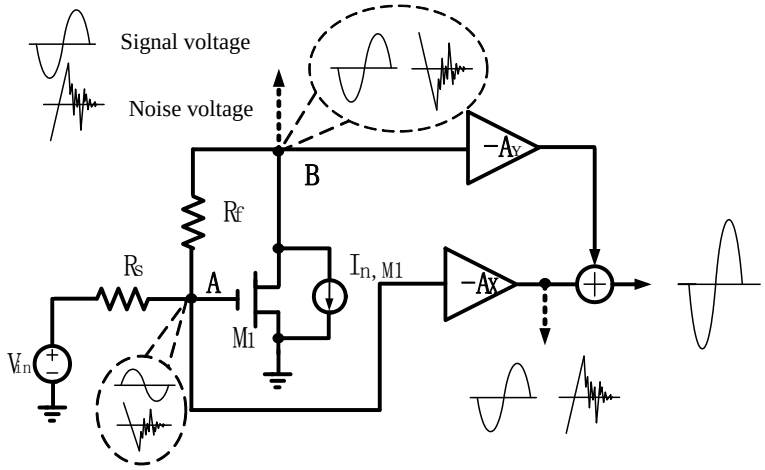


Figure 6. 4 Gain enhanced Common-source LNA

The noise voltages at A and B are the same as calculated in Eq. 6.1 and Eq. 6.2 and have an opposite polarity. Because of the extra amplifier A_Y at the output, the output noise voltage will be

$$V_{out,n} = A_Y \alpha I_n (R_s + R_f) - A_X (\alpha I_n R_s) \tag{6.7}$$

In order to make the output noise $V_{out,n} = 0$, the relationship between A_X and A_Y must satisfy

$$A_X = A_Y (1 + \frac{R_F}{R_S}) \tag{6.8}$$

and the gain *Av* will be

$$A_v = \frac{V_{out}}{V_A} = A_Y (1 - g_m R_f) - A_X = A_Y R_f (g_m + \frac{1}{R_s}) \tag{6.9}$$

when $1/g_m = R_s$, the overall gain *Av* will be $-2A_Y(R_F/R_s)$. Compared with the Eq. 6.6, the gain is amplified by A_Y.

Even if the overall gain is enhanced by this technology, there is still tradeoff between the gain and bandwidth. For the multi-standard applications, the high gain requirement for the LNA is not so critical because the gain can be supported by the subsequent stages. Therefore, a wideband LNA is to be designed to achieve a required bandwidth with a moderate gain and the gain enhanced technology can provide extra gain to be sacrificed for bandwidth extension.

6.2.2 Circuit realization of the gain-enhanced technique

Figure 6.5 shows the noise-cancelling LNA. The input matching is realized by a common-source stage with an active shunt-shunt feedback. M1 is the main amplifying transistor, and M_f, R_f, and C_f are the feedback source follower, resistor and capacitor respectively. A peaking inductor L_g is inserted in front of the gate of the amplifying transistor M1 to improve the

input matching and gain in the high frequency range. R_s is the 50Ω source impedance. A current mirror is used for biasing the source follower in the feedback loop.

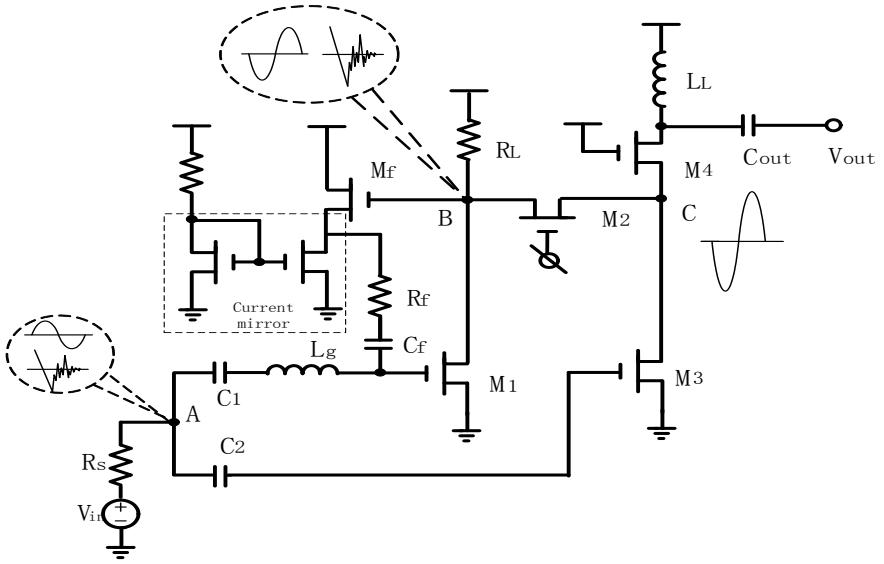


Figure 6.5 Schematic of the gain-enhanced wideband LNA with noise cancelling

For the noise cancelling consideration, the principle is similar with the conventional noise cancelling method. The equal signed signals and opposite-signed noise voltages are produced on node A and B of the feedback common source stage. An additional CG stage is used to re-amplify the signal and noise voltages on node B without changing the phase. After that, the amplified voltages reach to the combination stage for noise cancellation. In the design of [120], the gain of the combining stage is constrained by the noise cancelling principle because gains of the two stages have to match to get equal-amplitude noise voltages for cancellation. By adding the extra CG stage, the gain of the combing stage can also be increased accordingly. Therefore, the gains in both paths are enhanced and the final signal gain is also greatly improved.

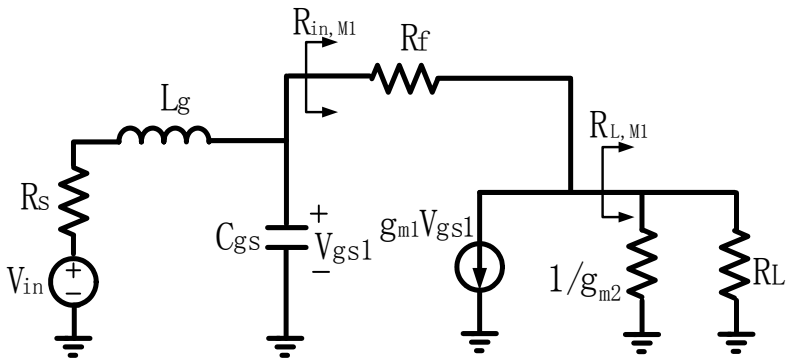


Figure 6.6 Equivalent small signal circuit for the input stage

6.2.3 Input Matching Stage

Instead of adopting the feedback resistor, in this design, a source-follower buffer is inserted in the feedback loop. By adopting the active feedback structure, the trade-off between bandwidth and gain is extremely relaxed. The detailed analyze is given in the followings.

For the resistor feedback amplifier, the input impedance is

$$R_{in} = sL_g + (\frac{1}{sC_{gs}} || R_{in,M1}) \tag{6.10}$$

where $R_{in,M1}$ is the input resistance of the CS stage M1 with shunt-shunt feedback, which is

$$R_{in,M1} = \frac{R_f + R_{L,M1}}{1 + g_{m1} R_{L,M1}} \tag{6.11}$$

where $R_{L,M1}$ is the equivalent load resistance at the drain of M1. The resistance equals to the parallel combination of the R_L and the input impedance of M2, $1/g_{m2}$.

$$R_{L,M1} = R_L || \frac{1}{g_{m2}} = \frac{R_L}{1+g_{m2}R_L} \tag{6.12}$$

where the g_{m1} is the transconductance of the input transistor M1. Meanwhile, the input impedance of the active feedback amplifier can be expressed as Eq. 10.

$$R_{in} = sL_g + \frac{R_L+R_f(1+g_{m2})R_L}{1+(g_{m1}+g_{m2})R_L+sC_{gs}[R_f(1+g_{m2})R_L+R_L]} \tag{6.13}$$

When the frequency is around zero, R_{in} equals to $(R_L + R_f(1 + g_{m2})R_L)/1 + (g_{m1} + g_{m2})R_L$, which is set to 50Ω to achieve a perfect input matching. As the frequency increases, the imaginary part coming from the intrinsic capacitance C_{gs} also increases and the input impedance will derivate from 50Ω. Therefore, a gate inductor L_g is inserted to compensate the imaginary part generating by the parasitic capacitance and the bandwidth of the LNA can be extended. Besides, the high-frequency gain and gain flatness can also be enhanced by adding the peaking inductor in front of the transistor gate. Figure 6.7 shows the simulation results by adopting different L_g inductance.

Compared with Figure 6.4, the bandwidth is increased and very good gain flatness is obtained. Furthermore, the input matching and noise performance are significantly improved. Besides, the gain and NF tradeoff can be clearly observed in Figure 6.7. As the gate inductance increases, the gain and bandwidth can both be effectively improved. However, a large gate inductor can lead to an over-peaking of the gain, and hence, circuit instability. Therefore, the inductance 3nH is chosen according to the simulation to balance the trade-off.

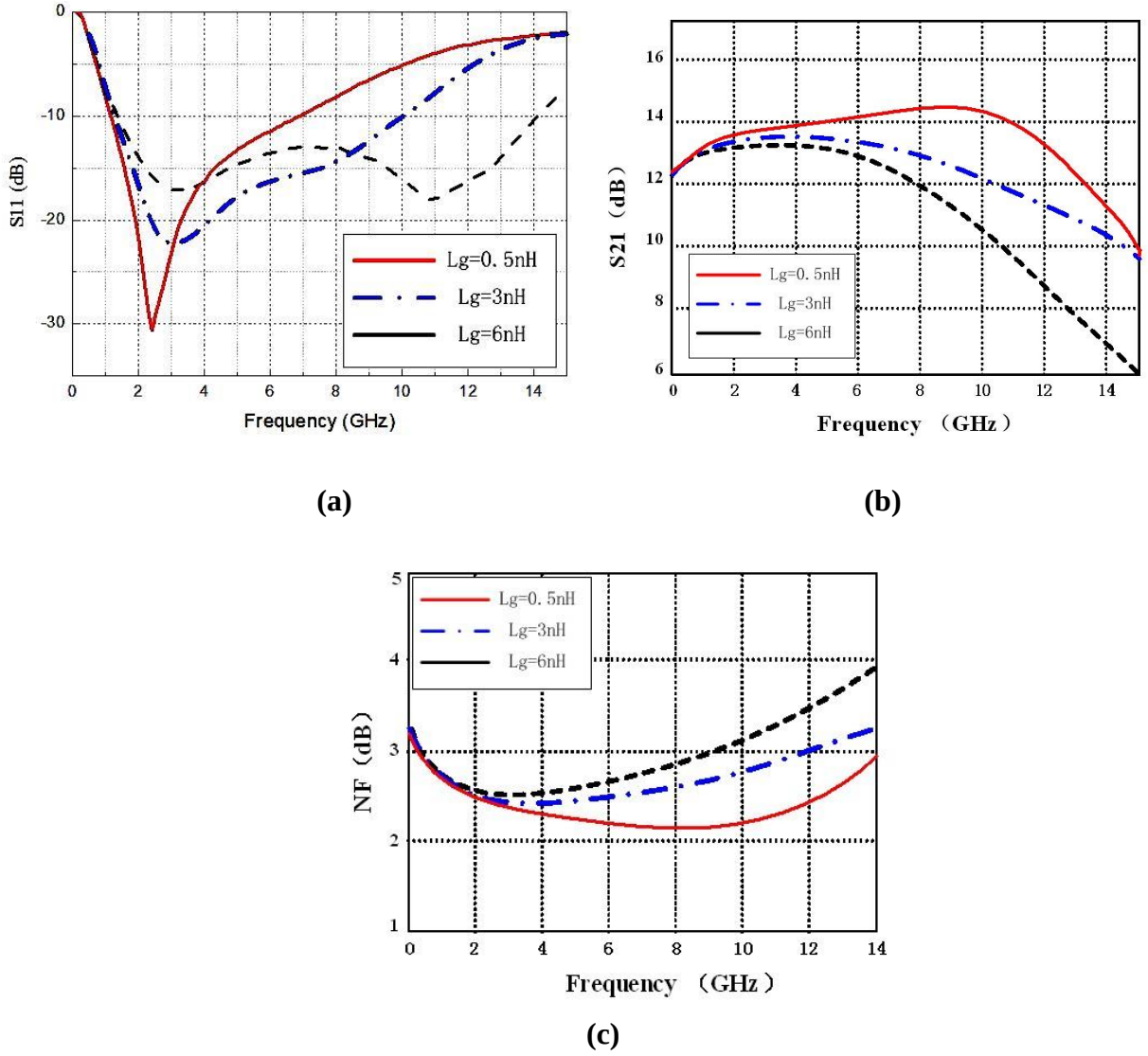


Figure 6.7 Simulated (a) S11, (b) S21 and (c) Noise Figure with different Lg

6.2.4 Gain-enhanced Noise Cancelling Stage

For the noise cancelling consideration stage, the principle is similar to the conventional noise cancelling method. The feedforward amplifier A_X in Figure. 6.1 is implemented in a common-source configuration by M3. Besides, an additional common-gate stage M2 is exploited

in the feedforward path for gain enhancing. There are two main purposes of this gain-enhanced noise-cancelling technique; one is to increase the overall voltage gain, and the other is to match the phase delay for two paths. Assuming the gain of the CS stage M1, CG stage M2 and combing stage M3 are A_{M1}, A_{M2}, and A_{M3}, respectively. By using the similar calculations, according to Eq. 6.4, the output noise voltage is cancelled, when

$$A_{M3} = A_{M2}(1 + \frac{R_f}{R_s}) \tag{6.14}$$

and A_{M3}, A_{M2} can be expressed as

$$A_{M3} = g_{m3}R_{L3} \tag{6.15}$$

$$A_{M2} = \frac{V_C}{V_B} \approx \frac{(1/g_{m4})//r_{o3}}{R_L/\,/r_{o1}//(1/g_{m1})} \tag{6.16}$$

$$R_{L1} = R_L//(1/g_{m1})//r_{o1} \tag{6.17}$$

$$R_{L3} = (1/g_{m4})/\,/r_{o3}//(g_{m2}r_{o2}R_{L1}) \tag{6.18}$$

Where $1/g_{m1}$ is the equivalent resistance of the feedback looking back from point B. R_{L1} and R_{L3} are the equivalent load resistances at the drain of M1 and M3. The gain of M2 is approximated to the ratio of the resistance at the drain to the resistance at the source of M2. Take Eq. 6.11 to Eq. 6.14 into Eq. 6.10, the noise-cancelling condition becomes

$$\frac{g_{m3}R_{L3}(R_L/\,/r_{o1}//(1/g_{m1}))}{r_{o4}//(1/g_{m3})} = 1 + \frac{R_f}{R_s} \tag{6.19}$$

In this condition, the signal gain equals to

$$A_{V,G} = \frac{V_{out}}{V_A} = A_{M2}\left(1 - g_{m1}R_f\right) - A_{M3} = -R_f \frac{(1/g_{m4})//r_{o3}}{R_L/\,/r_{o1}//(1/g_{m1})}\left(\frac{1}{g_{m1}} + \frac{1}{R_s}\right) \quad (6.20)$$

6.3 Measuring Results

The proposed low noise amplifier was implemented in the IBM 0.13μm CMOS technology. Figure 6.8 shows the die micrograph. The overall chip area is 0.58mm x 1mm and the core circuit area is only 0.46x0.67 mm^2. Powered by a 1.2V supply and the simulated DC current consumption is only 17mA. The chip was tested by on-wafer coplanar probing.

In Figure 6.9, S11 is below -10dB ranging from 0.1GHz to 8GHZ, with a bandwidth of around 8GHz. In the frequency range, the S21 is above 10dB with a 14.5dB peak, as shown in Figure 6.10. In general, the simulation results agree well with the measured results.

Figure 6.11 shows both the simulated and measured NF in the frequency range with a minimum of 2.6dB and a maximum of 4.3dB. The relatively large discrepancy in NF can be attributed to the buffer added for testing. Simulation and testing results prove that the proposed noise cancelling technique is effective for wideband LNA. The circuit performances are summarized in Table 6.1 and compared with other designed wideband LNAs. Clearly, this design achieves the highest gain and widest bandwidth. The NF is also one of the lowest compared with the other designs.

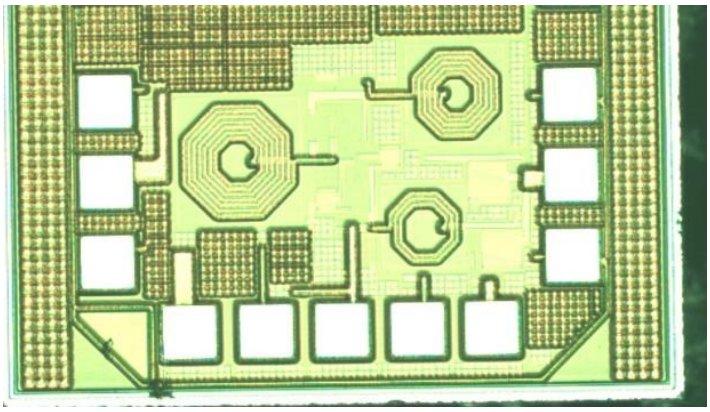


Figure 6.8 Micrograph of the proposed LNA

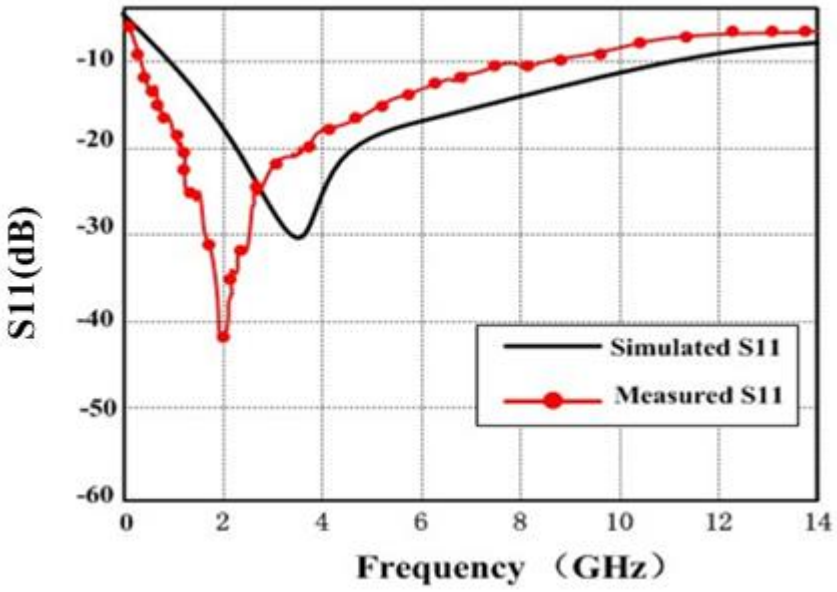


Figure 6.9 S11 of the LNA

6.4 Summary

A compact 0.1-8GHz Ultra-Wideband LNA using gain enhanced noise cancelling technique is proposed and implemented in the IBM 0.13μm CMOS technology. For the input matching, a common source stage with an active feedback is adopted to relax the trade-off between gain and bandwidth. Besides, a peaking inductor is inserted to improve the gain flatness and the bandwidth. In the targeted bandwidth, the gain of >12dB (with a 14.5dB peak) is obtained and a minimum NF (2.6dB) is achieved. The total power consumption is only 17mW. The results

Table 6.1 Summary and Comparison with Previous Works

References	**[4]**	**[5]**	**[6]**	**[7]**	**[8]**	**This Work**
Technology	0.25μm	0.13 μm	0.18 μm	0.13 μm	90nm	0.13 μm
Frequency (GHz)	0-1.6	0.8-2.1	1.2-11.9	2-9.6	2.5-4.0	0.1-8
Supply Voltage (V)	2.5	1.2	1.5	1.5	1.2	1.2
Power (mW)	35	11.7	20	19	16	17
Max. Gain (dB)	13.7	14.5	9.7	11	10.6	14.5
Noise Figure (dB)	2.4	2.6	4.5	3.6	4.0	2.6

indicated that the proposed gain enhanced noise cancelling technique effectively alleviated the tradeoff between gain, noise figure and bandwidth without extra power consumption.

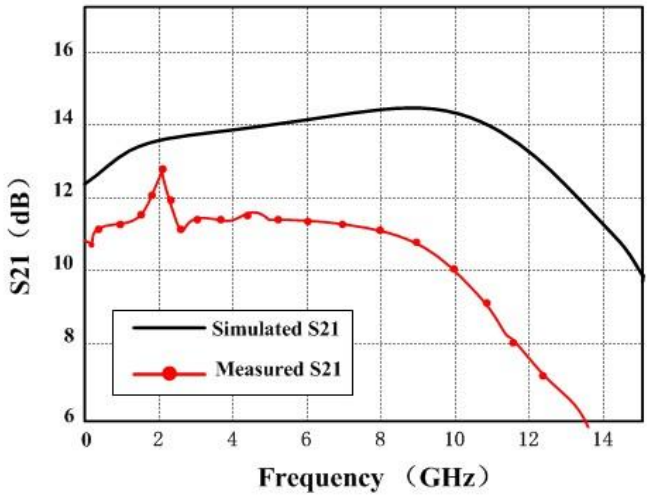


Figure 6.10 S21of the LNA

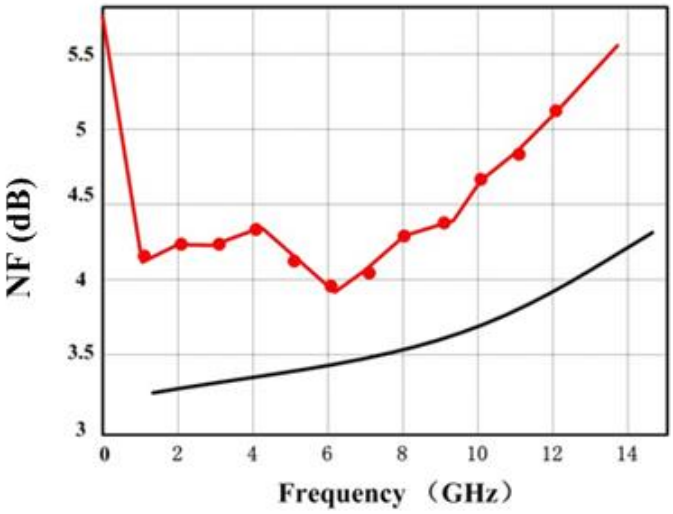


Figure 6.11 Noise Figure of the LNA

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

This thesis work provides the ease and effective ways to implement a single front end of the receiver for the next generations of wireless communications. The work also helps to smooth out the transition between generations allowing the co-existing of different wireless communication standards.

7.1 Conclusions

Three LNAs are proposed for different considerations in order to assist the upgrading of the existing devices and systems to support 4G applications. In the proposed LNAs, the input matching network, noise and distortion cancelling techniques are analyzed and implemented to circuit designs to relax the tradeoff among low noise figure, high gain, high linearity, and wider bandwidth. The designs can be considered as pioneers that are proposed specific for the 4G wireless communications.

The first design is optimized particularly for the LTE applications. The LNA is easily added in parallel with the existing dedicated circuit systems. For the classical cascode structure, the common source (CS) stage is considered to be the main nonlinearity contribution to the LNA. As the frequency increasing, the nonlinearity influence of the CG stage increases and limits the high linearity bandwidth. The nonlinearity coming from the common source (CS) and the common gate (CG) stage are analyzed in detail. The CS and CG stages are considered to be two separate stages in the design and different linear techniques are adopted to enhance the linearity of the LNA. For the CS stage, the MDS technology is adopted and for the CG stage, the DS technology is employed

along with the degenerated LC resonator. The use of both techniques simultaneously decreases the third-order and second-order nonlinear currents. The fabricated LNA has a bandwidth of 300MHz with the linearity of greater than 7.5dBm. The results indicate that the proposed structure effectively increases the linearity of the LNA and maintains the high linearity for a wide bandwidth.

The second design targets the universal wideband LNA for the so-called transition time. Nearly all the existing wireless standards, such as LTE, RFID, Bluetooth, and others can share a single LNA in the system. The sharing not only reduces system cost but also saves the chip area and dramatically reduces power consumption. A novel input network for the wideband LNA is proposed combining with the conventional resistive feedback structure. By inserting two input inductors, one within and one out of the feedback path, more freedom of choices are introduced in the design process. This structure is applicable to the multi-standard applications due to its high performance in a very wide bandwidth. The cascode LNA was designed and fabricated using the IBM 0.13μm CMOS technology. A high and flat gain (greater than 10dB) with a 16.5dB peak is achieved in a very wide frequency range (1-3GHz). The matching parameter, S11, is below -10dB in this frequency range and a minimum NF of 2.5dB is achieved. The power consumption of the LNA is only 7mW on a 1.2V supply. The proposed input-network using in this design effectively alleviates the tradeoff between NF, input matching, and gain without extra power consumption. The structure is very simple to implement in a multi-standard receiver.

The bandwidth of the third design is enlarged to 8GHz in order to cover all the bandwidth, including the WiMAX standard. The conventional noise cancelling method has limitation in the gain of the LNA. An improved noise cancelling structure is proposed to enhance the gain of the conventional technique. The gain-enhanced noise-cancelling technique is illustrated by the design

and fabrication of a wideband 130μm CMOS LNA. The measured maximum power gain is 14.5dB and the NF is 2.6-4.3dB in the frequency ranging from 0.1GHz to 8GHz. The core area of the LNA is 0.46x0.67mm^2 and the LNA consumes 17mW of power from a 1.2V supply. The testing results prove the effectiveness of the gain enhanced noise cancelling method for wideband LNAs to be used in the multi-standard wireless communications. As up to date, this s the first designs that proposed specific for the 4G wireless communications.

The three novel techniques are proposed in the LNA to balance the trade-off among bandwidth, noise figure, and linearity. The proposed noise cancelling and linearity enhancing techniques can be very effective in a wide frequency range and can be widely implemented to the future wideband LNA designs.

7.2 Future work

The testing results of the LNAs in this design have relatively large discrepancy compared to the simulated results. The differences mainly come from the parasitics of the chip and of the testing printed circuit boards. In the future design, these parasitic parameters should be more carefully considered and probe testing should be used instead testing PCB. One of the most challenging works in future implementation is the integration of the LNAs into a CMOS receiver. A new architecture of the receiver should be proposed with better functionality to process signals from different standards effectively.

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