Fabrication and Characterization of Nanocrystalline Silicon LEDs: A Study of the Influence of Annealing

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Abstract

This thesis describes the fabrication of a set of bright, visible light-emitting silicon LEDs. These devices were fabricated in-house at the University of Saskatchewan using a custom plasma ion implantation tool, an annealing furnace, and a physical vapour deposition system. A high-fluence ($F = 4 \times 10^{15}$ cm^{-2}) implantation of molecular hydrogen ions (i.e. H_2^+) extracted from an RF inductively coupled plasma at an energy of 5 keV was used to create a heavily damaged region in the silicon centered approximately 40 nm below the silicon surface with a width of approximately 56 nm. A matrix of annealing (e.g. thermal processing) processes at 400 °C and 700 °C and different durations (30 minutes and 2 hours) as well as an aluminum gettering procedure were tested with the goal of increasing the output electroluminescence intensity. Current-voltage characterization was used to extract information about the defect-rich nanocrystalline, light-emitting layer as well as the Schottky barrier height. This enabled comparison of these new devices with previous silicon LEDs based on porous silicon and other approaches. The processes which were used to fabricate these devices are compatible with standard CMOS processing techniques and could provide one solution to the problem of optical interconnect on multi-core chips. The scientific significance of this work is the demonstration of bright, visible light emission at mean photon energies ~ 1.84 eV corresponding to a photon wavelength of $\lambda \approx 675$ nm. This is remarkable given that ordinary crystalline silicon is an indirect bandgap material with a bandgap energy of 1.1 eV, in which band-to-band radiative recombination is forbidden by momentum conservation. The devices fabricated in this thesis have light emission properties similar to previous silicon LEDs based on nanocrystalline or nanoporous silicon. They have the advantage of being easily electrically driven. The nanocrystalline region which is the source of the light emission was nucleated from the ion-implanted layer below the surface of the silicon. This makes these devices mechanically robust and insensitive to environmental conditions. The engineering significance of this work is the production of CMOS compatible light emitters. This study demonstrated increased light emission efficiency at higher annealing temperatures which is likely due to enhanced diffusion and nucleation of silicon nanocrystals in the ion-implant damaged layer.

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For my mother, who is strong.

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List of Abbreviations

AC	Alternating Current
BBT	Band-to-Band Tunneling
CMOS	Complementory Metal Oxide Semiconductor
DC	Direct Current
ECR	Electron Cyclotron Resonance
ICP	Inductively Coupled Plasma
IGBT	Insulated Gate Bipolar Transistor
IV	Current-Voltage
LED	Light Emitting Diode
MOS	Metal Oxide Semiconductor
PDG	Phosphorus Diffusion Gettering
PII	Plasma Ion Implantation
RF	Radio Frequency
SRH	Shockley-Read-Hall
SRIM	Stopping and Range of Ions in Matter
TAT	Trap-Assisted Tunneling
UV	Ultraviolet
VCSEL	Vertical Cavity Surface Emitting Laser

Chapter 1

Introduction

1.1 Optical Interconnect as a Future Technology

As we move into the second decade of the 21st century, computer processors have evolved. Clock speeds have topped out at around 3-5 GHz and higher processor capacities have been achieved using multicore configurations. In the new multicore environment, fast interconnect between the cores will be a major technological advance. Conventional metal interconnect will limit on-chip communication speeds in the future [1]. The high communication speed and bandwidth associated with optical communications [2] has long been desired for computer chips. On-chip optical interconnects will overcome interconnection bottlenecks on chips by routing signals with light (IR or visible). Because photons do not interact or scatter off of one another, crosstalk can be much reduced. This technology is currently of great world-wide interest. In addition to Intel Corporation, which has pioneered many aspects of silicon technology, there is a European Silicon Photonics Cluster actively pursuing this, and Luxtera Corporation and ST Microelectronics have partnered to produce silicon photonic chips (see Luxtera press release "Luxtera and ST Microelectronics to enable high-volume silicon photonics solutions" March 1 2012 PR No. T3279H).

1.2 Silicon Photonics

The technology of integrating optical communications on computer chips is referred to as *silicon photonics*. Several major companies and university research consortia (e.g. Intel, the European Silicon Photonics Cluster) are aggressively pursuing silicon photonics systems. Currently the main barrier to using light on-chip is the fact that silicon, while an excellent

semiconductor in most respects, has an indirect bandgap which prohibits efficient band-to-band radiative recombination. A number of groups worldwide are pursuing potential technological solutions to this problem. For example, Intel has experimented with so-called wafer bonding techniques to attach an Indium phosphide (InP) laser to a silicon chip.

1.3 Light-emitting Nanostructured Silicon

The ideal silicon photonic solution would rely on modification of silicon to make it an efficient light emitter. This was first demonstrated by Canham *et al.* in 1990 [3] when they obtained moderately bright red light emission from anodically etched porous silicon. This launched a flurry of activity and many porous silicon light-emitting devices were fabricated [4]. However, porous silicon proved to be too fragile and also presented difficulties in terms of contact formation as well as extreme sensitivity to atmospheric contaminants. A slightly different approach used various methods to fabricate silicon nanodots embedded in a glass matrix; while these exhibit interesting luminescence properties when optically pumped, it is unclear how they would be integrated with electrical drive transistors given the high resistivity of the glass matrix. A comprehensive summary of work on light-emitting silicon is given by Osscini *et al.* [5].

1.4 Plasma Ion Implantation for Silicon LEDs

A promising approach to the problem of fabricating a silicon light emitter makes use of the standard semiconductor processing techniques of ion implantation followed by high temperature annealing (e.g. thermal processing) in an inert atmosphere or vacuum. This can be used to make light emitting devices on a silicon chip. The process is fully maskable and thus can be integrated with standard CMOS technologies. The group of Paul Chu *et al.* at the City University of Hong Kong demonstrated light emission from plasma ion implanted silicon in 2003 [6]. This preliminary work was followed up by Desautels *et al.* [7] [8], who showed broadband emission from plasma ion implanted (PII)-fabricated silicon Schottky LEDs. The peak emission wavelength of these LEDs could be controlled by varying the ion implantation

parameters (e.g. ion species and implantation energy).

The work described in this thesis builds on the foundation laid by Desautels *et al.* by investigating the effect of thermal processing parameters (e.g. annealing parameters). It is well known that semiconductor device parameters depend sensitively upon the thermal processing/annealing regime chosen. This thesis reports on annealing of hydrogen-implanted silicon Schottky LEDs at different temperatures and extraction of device parameters from detailed electrical and electroluminescence characterization methods. Such information will be of critical importance for engineers and applied physicists working to integrate silicon light emitters of this type with CMOS chips.

1.5 Plan of Thesis

This thesis will describe a series of experimental silicon LED devices which were fabricated under different conditions to test the influence of two distinct thermally driven processes: annealing and Al gettering. Table 1.1 shows the experimental matrix for the processing conditions tested. The influence of annealing temperature and time was investigated as these parameters are believed to play a crucial role in the nucleation and growth of silicon nanocrystallites in the heavily damaged layer formed by plasma ion implantation. Al gettering (described in more detail in Section 2.3.3) was investigated since it is known to improve device performance in the presence of contamination by transition metals.

Chapter 2 provides a brief background on semiconductor physics (including charge transport and light emitting processes) as well as a discussion of the semiconductor processing techniques used to fabricate the devices for this thesis (including plasma ion implantation, annealing, and gettering). Chapter 3 gives details of the experimental work (device fabrication followed by electrical and optical characterization) done for this thesis . Chapter 4 describes the characterization of the fabricated devices and discusses these results in the context of various models for the nanostructured silicon light-emitting layer formed by plasma ion implantation and annealing. Chapter 5 summarizes the conclusions which can be drawn from this series of experimental silicon LED devices and suggests some results for future engineering work.

Device Fabrication Conditions	400 °C Anneal 30 minutes	400 °C Anneal 120 minutes	700 °C Anneal 30 minutes	700 °C Anneal 120 minutes
No Gettering	Devices 1 & 2	Devices 3 & 4	Devices 5 & 6	Devices 7 & 8
Al Gettering	Devices 9 & 10	Devices 11 & 12	Devices 13 & 14	Devices 15 & 16

Table 1.1: Experimental matrix for devices fabricated for this thesis under different annealing and Al gettering process steps. Note that 16 devices were fabricated in total; all processing was done at the University of Saskatchewan.

Chapter 2

Background

2.1 Properties of Silicon

2.1.1 Silicon as an Electronic Material

Silicon is by far the most widely used semiconductor material. This is because it is available in high-quality, large-area crystal wafer form. Silicon is abundant, chemically inert, non-toxic, and mechanically robust. It can be doped with group V electron donor atoms (e.g. As) to make n-type silicon in which conduction by electrons dominates or group III electron acceptor atoms (e.g. B) to make p-type silicon in which conduction by positively charged holes is dominant. While pure silicon is a poor conductor, when doped to reasonable levels it can have very low resistivity because of its relatively high electron and hole mobilities. Another important feature of silicon is its ability to grow a stable chemically inert, robust oxide which is the key enabling feature for the MOS (Metal Oxide Semiconductor) insulated-gate transistors which form the backbone of today's CMOS electronics and information technology infrastructure. Silicon is far cheaper than other semiconductors; for example, a 300 mm diameter wafer costs $50 US. By comparison, one typical III-V InP wafer at 50 mm diameter costs $60. So silicon is about 30 times cheaper than InP. GaN is still more expensive. This is one of the reasons why we see individual light emitters made from III-V semiconductors, but not large area integrated circuits. Current worldwide production of silicon is about 10^5 tonnes (Mineral commodity summaries US Geological Survey January 2006 page 150-151). Table 2.1 lists some important properties of silicon (taken from [9]).

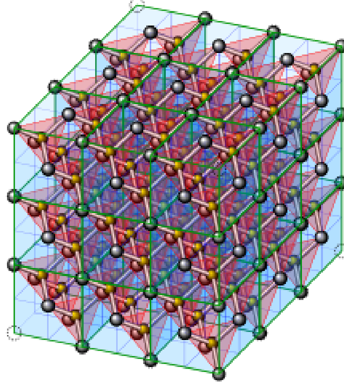
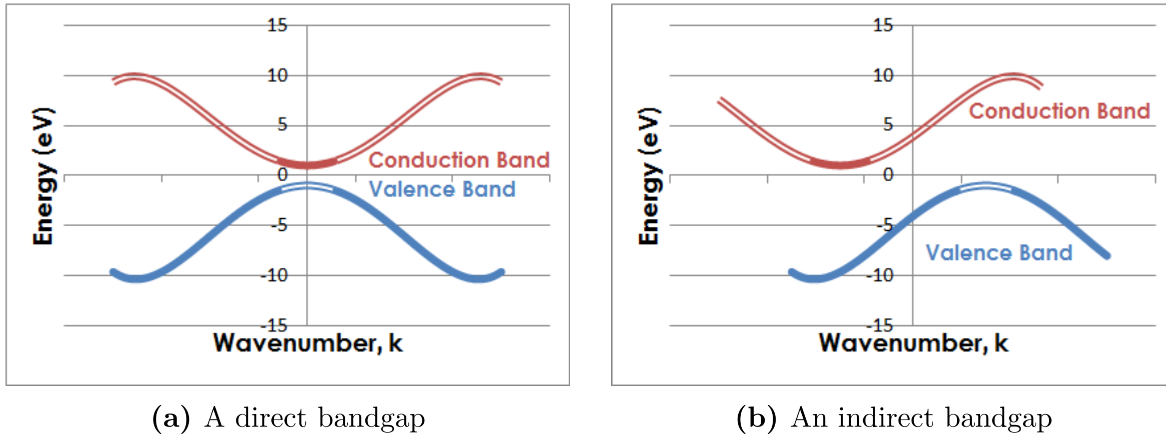


Figure 2.1: Visualization of the silicon (i.e. "diamond-cubic") lattice. Figure from Wikimedia Commons (author Cmglee), reproduced under Creative Commons Attribution Share Alike 3.0 Unported license.

Property	Typical value
Crystal Lattice Type	diamond-type lattice
Atomic Density	5×10^{22} atoms/cm^3
Bandgap Energy	1.1 eV
Electron Mobility μ_e	1350 cm^2/V·s
Hole Mobility μ_h	480 cm^2/V·s
Relative Permittivity ϵ_{Si}	11.7

Table 2.1: Properties of silicon relevant to electronic device applications. [9]



(a) A direct bandgap **(b)** An indirect bandgap

Figure 2.2: A direct bandgap (left) and an indirect bandgap (right). The solid lines indicate states occupied by electrons; the hollow lines indicate states that are not occupied by electrons, but are instead occupied by positively.

2.1.2 Band Structure

Bandgaps: Direct & Indirect

The defining characteristic of a semiconductor's electron density of states is an energy gap (1.1 eV for silicon) separating the valence and conduction bands. This "bandgap" is the minimum energy that an electron must acquire or lose in a single interaction in order to undergo a band-to-band transition. Materials are further differentiated by the features of their band structure: the set of states that can be occupied by electrons, and the relationship between the energy and momentum of those states.

An electron may fall from the conduction to the valence band simply by emitting a photon if (and only if) the momentum of the state in the conduction band matches the momentum of the state in the valence band into which the electron is falling. This occurs in materials where the conduction band's lowest energy states and the valence band's highest energy states have the same value of crystal momentum; an illustration of this condition is shown in Figure 2.2a. Such materials are known as direct bandgap semiconductors; they exhibit efficient band-to-band recombination radiation. The class of III-V semiconductor materials are all direct bandgap semiconductors with parabolic conduction band and valence band edges. Some commonly used III-V materials are InP, GaN, GaP, GaAs, as well as others.

The group IV semiconductors, Si and Ge are indirect bandgap materials. The minimum

energy point of the conduction band is offset in crystal momentum space relative to the highest energy point of the valence band. An electron at the bottom of the conduction band must somehow change momentum to fall to the valence band. Because of this, the most likely de-excitation pathways are non-radiative: the electron loses energy through collision with either a phonon or another electron.

Figure 2.3 shows the band structure of silicon [10]. It can be seen that the minimum energy point of the conduction band is offset in momentum space relative to the maximum energy of the valence band. A direct band-to-band recombination process between electrons at the bottom of the conduction band and holes at the top of the valence band is therefore impossible as it is forbidden by momentum conservation (in radiative recombination the photon does carry momentum but the photon momentum $\frac{h}{\lambda}$ carried by the $\lambda = 1.06\mu$m photon corresponding to the 1.1 eV silicon bandgap is negligible). When energetic electrons are injected into the conduction band from a Schottky contact or other injection mechanism they quickly thermalize and end up at the conduction band minimum energy point. They are then unable to recombine with the holes by photon emission. For this reason, indirect bandgap semiconductors are not efficient light-emitting semiconductors.

2.1.3 Semiconductor Physics

The chief impediment to silicon photonics is the lack of a suitable silicon-based light emitter. As outlined above, this is due to the indirect bandgap of silicon. A semiconductor's bandgap depends upon how conduction electrons move in the potential well environment created by the surrounding silicon ion cores in their diamond-type lattice. The description of a semiconductor's electrical properties begins with its electrons. They are, after all, what move in response to an applied voltage and their collective flow is measured as the electric current. These ideas are simple, but clear; and it is a straightforward matter combining them with the other ideas which build the richness of semiconductor physics.

Several of these ideas result from quantum mechanics. For one is the wave-like nature of the electron. Because of this nature an electron has a wavevector, k, which is synonymous with its momentum. It becomes useful to define an entire space — momentum space — in which an electron exists while simultaneously existing in real space. The second major result

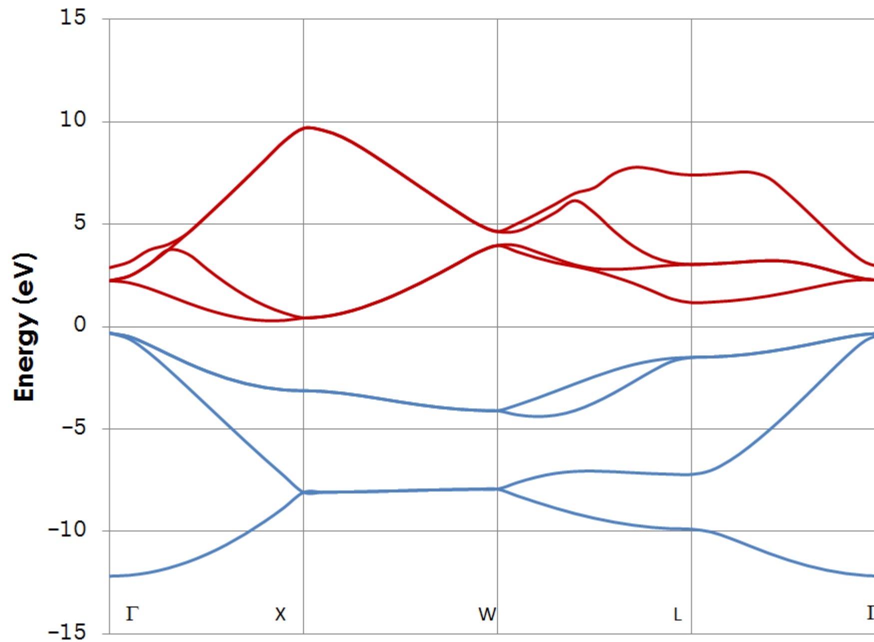


Figure 2.3: The band structure of silicon. The reference energy is the Fermi energy. For more detail see Chelikowsky and Cohen's 1974 paper [10].

of quantum mechanics is the requirement that an electron's wavefunction must satisfy the Schrödinger equation:

$$i\hbar\frac{\partial\psi}{\partial t} = \frac{-\hbar^2}{2m}\nabla\psi + V(\mathbf{r})\psi \tag{2.1}$$

Where $\psi(\mathbf{r})$ and m are the electron's wavefunction and mass, and $V(\mathbf{r})$ is the potential energy. Here, in the form of the potential energy term, enter the particles surrounding the electron: the positively charged, relatively immobile ion cores, and the negatively charged electrons. Because of their immobility, the ion cores dominate the form of the potential energy. It is fortunate that when these cores came together and solidified, their forces on each other caused them to settle in regular positions — because of this, they create a periodic potential consisting of wells localized on the ion core positions. It was shown by Bloch that an electron in a such a periodic potential has a wavefunction which has the following form:

$$\psi_k(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}}u_k(\mathbf{r}) \tag{2.2}$$

Where $u_k(\mathbf{r})$ is a function with the same periodicity as the lattice. The wavefunction of every electron in a crystal can be resolved into a linear combination of Bloch-type wavefunctions. The Bloch waves are not the wavefunctions of actual electrons, but rather a consistent set of basis states their properties yield insight into the electron's behaviour, and their form is a major part of the reason why the energies of electrons are organized into a band structure; i.e. why the energies of electrons only fall within specific ranges with gaps in between.

2.1.4 State Transition Rates

Consider the case of an electron excited by incident light from the valence band of a semiconductor to the conduction band. As this interaction is involves a transition between stationary states of the electron's wavefunction, it is described by time-dependent perturbation theory.

What follows is a semi-classical development of the description of that transition, taking the relevant results from time-dependent perturbation theory but not requiring familiarity with it.

The effect of the incident light beam's magnetic field is negligible compared to that of the electric field; therefore, consider the electric field of a plane light wave propagating in the z-direction:

$$\vec{E} = E_0 \hat{x} e^{i(\vec{k}\cdot\hat{z} - \omega_L t)} \tag{2.3}$$

The energy of an electron in the valence band, U_v, is given by the Hamiltonian operating on the electron's wavefunction, $|v\rangle$:

$$\mathcal{H}_v |v\rangle = U_v + \left(\frac{\hbar^2 k_e^2}{2m}\right) |v\rangle \tag{2.4}$$

Where U_v is the potential energy of the electron at the top of the valence band and k_e is its wavevector. The excitation of the electron by the light is adequately approximated by the electric dipole interaction and neglecting the magnetic field. The Hamiltonian of this excited electron is then given by [11]:

$$\mathcal{H}_{excited} = \mathcal{H}_v - e\vec{r} \cdot \vec{E} \tag{2.5}$$

$$= \mathcal{H}_v + \mathcal{H}_{eR} \tag{2.6}$$

Where $\mathcal{H}_{eR} = -e\vec{r} \cdot \vec{E}$ is the perturbation to the wavefunction of the valence band electron. This perturbation can be used as an operator on the valence state to give the wavefunction of an excited valence electron.

At this point the orthogonality of the wavefunctions becomes important. Certainly, in the absence of the perturbing electric field, the wavefunctions of the valence band and the conduction band electrons are orthogonal:

$$\langle c|v\rangle = \int \Psi_c^*(\mathbf{r})\Psi_v(\mathbf{r})d\mathbf{r} = 0 \tag{2.7}$$

However, in the presence of the applied perturbing electric field, the electron can tranisition from the valence state to the conduction state provided that $\langle c|\mathcal{H}_{eR}|v\rangle \neq 0$. Moreover, the rate of this event is given by Fermi's Golden Rule, a key result of time-dependent perturbation theory:

$$\Gamma_{v\to c} = \frac{2\pi}{\hbar} \left|\langle c|\mathcal{H}_{eR}|v\rangle\right|^2 \cdot \rho(E_c) \tag{2.8}$$

Where $\Gamma_{v\to c}$ is the transition rate at which an electron transitions from the valence band to the conduction band and $\rho(E_c)$ is the electron density of states near the destination state in the conduction band. $\Gamma_{v\to c}$ has units of inverse time that is, it describes transitions per unit time.

Modifying the Silicon Bandgap

The worldwide search for a silicon-based photonic emitter is driven by the desire to bring optical communication to computer chips. There are two broad strategies: the first consists of finding a way of bonding an efficient light-emitting semiconductor (e.g. a III-V device) to a silicon chip containing the rest of the necessary circuitry. Intel Corporation in particular has pioneered this approach, and in 2006 announced a hybrid "silicon laser system" consisting

of an InP laser wafer-bonded onto a silicon backplane which contained optical waveguides for routing photonic signals. While this approach is interesting, there are problems with scalability and yield. Therefore there is continuing interest in the second approach, namely finding a pure silicon-based solution.

Nanocrystalline Silicon

Porous Silicon

In 1990, silicon photonics received a tremendous boost when anodically etched porous silicon was shown to be an efficient visible light emitter by Lee Canham at the UK Defense Research Establishment Agency [3]. The anodic etching process (an electrochemical etching process in dilute HF acid) results in hexagonal pores separated by a thin lattice of silicon nanowires. Quantum confinement of charge carriers in the nanowires results in exciton energy levels separated by 2 eV. While LEDs can be fabricated in porous silicon, the material is mechanically fragile and tends to degrade over time. Light emission is easily quenched by surface impurities and this is also a problem for device fabrication.

Silicon Nanocrystals in Glass

Another route using nanocrystalline silicon involves growing silicon nanocrystals in a glassy matrix. While this generally gave good photoluminescence properties, silicon nanocrystals embedded in high resistivity glass cannot be easily electrically excited and therefore are difficult to integrate with CMOS circuits. Thus, it may not be a good silicon photonics solution.

Buried Silicon Nanocrystal Layers

Another route to fabricating silicon nanocrystals with light emission properties is to use high-dose ion implantation to amorphize a silicon layer below the surface of the silicon wafer. An annealing step is to recrystallize the silicon as a series of nanocrystallites with bandgaps larger than the regular silicon 1.1 eV bandgap due to quantum confinement. This was the approach followed in this thesis.

Quantum Confinement in Nanocrystals

The physics of charge carriers in nanocrystals leads to properties which can be markedly different from those of the original bulk material from which the nanocrystals are made. The reason for this is the strong size dependence of the carrier electrons and holes in potential wells with sizes of or less than a nanometer [13]. Quantum mechanics must be used to calculate the energy levels of charge carriers in this regime and the simplest possible calculation is the so-called "particle in a box" model. This predicts energy level separations increasing proportionally to $\frac{1}{L^2}$ where L is the characteristic length scale of the nanoparticle in question. For silicon nanocrystals of the order of a nanometer in size, the separation between energy levels predicted by this equation is greater than 1 eV; that is, greater than the base bandgap of bulk silicon. In addition, radiative recombination rates between particle-in-a-box energy levels can be large. Quantum confinement is not the only effect influencing energy levels in nanocrystals. The large surface-to-volume ratio of nanocrystals means that surface states and contaminants play a much greater role in determining the properties of the nanocrystals than is the case for the bulk material.

Various groups have made numerical calculations of quantum confinement effects in silicon nanocrystals using a variety of calculation techniques. Delley and Steigmeyer calculated the bandgap for silicon nanocrystals with hydrogen passivation on the outer surface [14]. Similarly, Hill and Whaley [15] calculated the effect of excitons (i.e. bound electron-hole pairs) in silicon nanocrystals. It was pointed out by Delerue [16] that these calculations are semi-empirical and potentially subject to error. Fauchet made an experimental study of porous silicon quantum dots and correlated it with *ab initio* calculations [17]. All of the variants on nanostructured silicon (e.g. porous silicon, silicon nanowires, silicon nanocrystals embedded in glass, and chemically nucleated colloidal suspensions of silicon nanocrystals [18]) are expected to exhibit some combination of quantum confinement and surface effects, and the majority show strong visible photoluminescence, although the mechanism can be complicated [17].

Silicon Nanocrystal LEDs

The first demonstrations of increased bandgap in porous or nanocrystalline silicon were done using photoluminescence in which a UV photon promotes electrons to an excited state and the visible light luminescence is monitored using a spectrometer. Many groups use photoluminescence to characterize nanocrystalline semiconductor light-emitting properties; however, electroluminescent devices are required for integration with CMOS chips, which is the ultimate goal of silicon photonics research. Because electroluminescent and photoluminescent mechanisms differ, this work has focused on electroluminescent LEDs with the understanding that an efficient LED developed in the laboratory could be easily ported to a standard silicon CMOS fab. This is a great strength of electroluminescent measurements compared with photoluminescence.

Some groups have made LEDs based on porous silicon. This presents certain challenges because of the fragile nature of the porous silicon surface and its susceptibility to surface contamination. Any electrically-driven device inevitably involves a choice of contact electrode materials and these can strongly influence the overall device performance based on parameters such as the work function. In addition, light-emitting devices that at least one electrode be semi-transparent to the emission wavelength expected.

Halliday *et al.* reported a porous silicon LED with a polyaniline (e.g. organic polymer) top electrode. The photoluminescence emission from the device was a broad Gaussian peak centered around 620 nm, FWHM of 130 nm, prior to coating with polyaniline. After coating, the electroluminescence shifted to the red, peaking at 792 nm and broadening to a FWHM of 267 nm [19]. Sercel *et al.* fabricated an all-silicon device consisting of an n-type amorphous hydrogenated silicon layer (n-type a-Si:H) on top of a porous silicon layer with a crystalline porous silicon layer below. The contact to the n-type silicon was made via a thin semi-transparent metal (Al or Pd) top contact [20]. The peak emission was around 700 nm wavelength. Liu *et al.* used plasma ion implantation followed by annealing to fabricate visible-light emitting LEDs. The peak emission wavelength was approximately 578 nm at very high drive voltages from 18 – 24 V [6].

Transition Rates in Silicon Nanocrystals

Proot *et al.* [12] determined that when the electron wavefunctions specific to silicon nanocrystals are considered, the specific form of Eq. (2.8) is:

$$\Gamma_{c\rightarrow v} = \frac{1}{\tau} = \frac{16\pi^2}{3} n \frac{e^2}{h^2 m^2 c^3} E_0 |\langle i_{BC}|p|f_{BV}\rangle|^2 \tag{2.9}$$

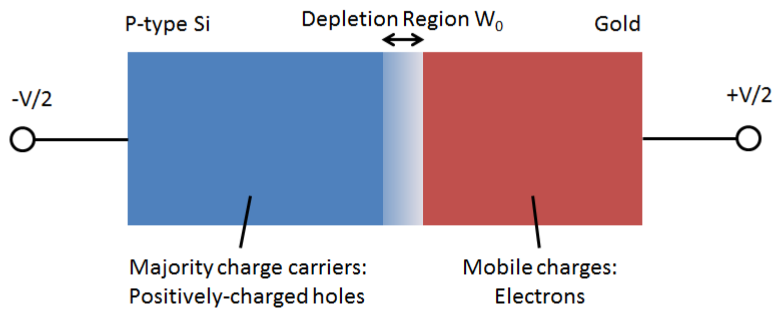
Where n is the refraction index of silicon, E_0 is the energy of the transition, $|i_{BC}\rangle$is the initial state of the electron, and $|f_{BV}\rangle$ is the final state of the electron in the valence band.

Silicon Laser

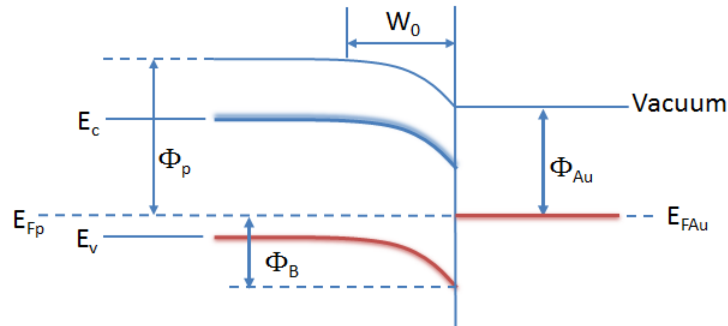
One of the ultimate goals of silicon photonics research is electrically pumped injection diode laser based on silicon. While some groups have reported optical gain in silicon nanocrystal structures under certain conditions [21], there has been some question about the accuracy of these measurements [22] and no group has yet demonstrated a working injection silicon laser.

2.2 Silicon Devices

Electronic devices fabricated from silicon rely on junctions between differently doped regions to create appropriate potential barrier profiles and charge carrier distributions for the intended functionality [23] [24]. The simplest semiconductor electronic device, and the oldest, is the Schottky diode, which consists of a metal-semiconductor junction (see Figure 2.4a). Upon electrical contact electrons diffuse from the Au into the p-type Si and combine with the dopant acceptor atoms, thus creating a depletion region void of charge carriers. This region is negatively charged on the p-type Si side and positively charged on the Au side. Because this is a result of charge redistribution and no charges were added to the device, the junction overall is neutrally charged. The electric field associated with this charge distribution halts further diffusion of electrons from the Au contact into the p-type Si. Note that Au/n-doped silicon Schottky contacts are more commonly discussed, but Au/p-doped silicon can be fabricated [25] [26] [27]. For a metal-semiconductor junction to function as a rectifying Schottky contact, the relative values of the electron work functions must be in the appropriate relation



(a) An Au/p-type Si junction under zero bias. Electrons are the mobile charge carriers in the Au contact, whereas positively charged holes are the majority charge carrier in the p-type Si.



(b) Band diagram of the Au/p-type Si junction. E_c and E_v are the energies of the conduction and valence bands, respectively. E_{Fp} and E_{FAu} are the Fermi energies in p-type Si and Au relative to vacuum. Φ_p and Φ_{Au} are the work functions of p-type Si and Au, respectively. Φ_B is the Schottky barrier height.

Figure 2.4

[24].

Like the more familiar pn junction diode, the Schottky diode exhibits strong rectifying behaviour, allowing current to flow with a low voltage drop in one direction (the so-called "forward direction") and blocking current flow in the reverse direction when the sign of the voltage drop is inverted. When the device is conducting current in the forward direction it is said to be "forward biased".

2.2.1 Conductivity of Doped Silicon

Pure, single-crystal silicon is a poor conductor. However, the conductivity of silicon may be controlled over a wide range by the addition of precise amounts of dopant atoms. Dopants from Group III (most commonly B) function as acceptors and result in free holes serving as positive charge carriers. Similarly, dopants from Group V (e.g. As and P) serve as electron donors and result in free electrons acting as negative charge carriers. The conductivity σ of doped silicon is given by

$$\sigma = e(\mu_h n_h + \mu_e n_e) \tag{2.10}$$

Where e is the elementary charge, $e = 1.602 \times 10^{-19}$ C, μ_h and μ_e are the hole and electron mobilities, respectively, and n_h and n_e are the charge densities (per unit volume) of holes and electrons. For p-doped silicon, the electron contribution is neglected, resulting in

$$\sigma = e(\mu_h n_h) \approx e\mu_h N_A \tag{2.11}$$

Where N_A is the volume density of acceptor dopant atoms. Note that this expression assumes that every acceptor becomes negatively ionized and therefore results in a mobile hole. The silicon used for the devices in this thesis had a quoted resistivity, $\rho = 1/\sigma$ in the following range:

$$5\,\Omega \cdot \mathrm{cm} < \rho < 25\,\Omega \cdot \mathrm{cm} \tag{2.12}$$

This corresponds to boron doping densities in the following range:

$$5.2 \times 10^{14}\text{cm}^{-3} < N_A < 2.60 \times 10^{15}\text{cm}^{-3} \tag{2.13}$$

2.2.2 The Unbiased Diode at Equilibrium

When the diode is electrically isolated so that no current is driven through it, a condition of charge carrier equilibrium is reached. The recombination of electrons and holes near the semiconductor-metal interface results in a region which is depleted of free charge carriers. This region is referred to as the "depletion region". The width W is given by:

$$W = \sqrt{\left(\frac{2\epsilon_{Si}\epsilon_0}{e}\right)\left(\frac{1}{N_A}\right)V_0} \tag{2.14}$$

This width follows from the redistribution of electrons and the electric field associated with it: as the electric field grows large enough to stop further redistribution, the depletion region reaches the width shown above and equilibrium is reached.

For our boron doping density $N_A \approx 1 \times 10^{15}$ cm^{-3} and built-in potential $V_0 \approx 0.5$ V, this gives a depletion layer width $W = 800$ nm for the unbiased junction.

2.2.3 Forward Bias Analysis

When a diode is forward biased (this corresponds to a negative potential applied to the gold electrode of the silicon Schottky LEDs fabricated for this thesis, relative to the bulk silicon), the current is well-described by the diode equation:

$$J = J_s\left(e^{\frac{eV}{\eta kT}} - 1\right) \tag{2.15}$$

where J_s is the current scale parameter, e is the elementary charge (1.602×10^{-19} C), V is the applied voltage, η is the so-called ideality factor, k is Boltzmann's constant (1.38×10^{-23} J/K), and T is the temperature in kelvin. This equation is valid for a wide range of diode-like devices, including Schottky diodes as well as conventional pn junction diodes [23] [24], and LEDs made from III-V semiconductors [28] (Note that it is sometimes necessary to include the effect of a series resistance for devices made from low-conductivity material). All these devices can be described by the diode equation with different values of the current scale

parameter and the ideality factor. Note that the ideality factor η is unity for the theoretical diode model derived using drift-diffusion equations; real diodes differ from this typically by having $\eta > 1$. In this sense the term "ideality factor" is a misnomer, because values of $\eta \gg 1$ correspond to devices which deviate significantly from the simple "ideal" model.

The current scale parameter J_s depends upon the barrier height in accordance with the following expression:

$$J_s = A^* T^2 e^{-\frac{\Phi_B}{kT}} \tag{2.16}$$

Where A^* is the effective Richardson constant, $A^* = 32$ A/cm$^2\cdot$ K^2 for p-type silicon and Φ_B is the barrier height. Note that this expression can be used to extract the barrier height as follows:

$$\Phi_B = -kT \ln\left(\frac{J_s}{A^* T^2}\right) \tag{2.17}$$

The diode equation describes both the conventional pn junction diodes as well as Schottky diodes which consist of a semiconductor bonded to a metal electrode. While the standard Schottky diode consists of an n-doped silicon bonded to a metal electrode, it is also possilble to fabricate Schottky diodes on p-doped silicon [25]. Whether a metal-semiconductor junction is ohmic or rectifying (i.e. diode-like) depends upon the relative values of the metal and semiconductor work functions [24].

2.2.4 Reverse Bias Analysis

When the Schottky diode is reverse-biased (negative potential applied to the gold top electrode, relative to the bulk silicon) the current is much less than in the forward direction, but is not identically zero. The diode equation predicts a reverse current $J = -J_s$ and this is indeed a reasonable approximation for small reverse bias voltages, but does not capture the full complexity of reverse current conduction. A variety of mechanisms (e.g. Zener breakdown, avalanche breakdown [23], and trap-assisted tunneling [29]) exist for so-called "reverse breakdown" in semiconductor devices. The Schottky LEDs fabricated for this thesis exhibited interesting reverse bias behaviour including breakdown for the 700 °C-annealed

devices. Hurkx *et al.* developed a thorough device model [29] for reverse bias devices including breakdown effects and this was used to analyze the reverse bias behaviour of the silicon Schottky LEDs fabricated for this thesis. The model is much more complicated than the diode equation and details are given in Appendix A.

2.3 Semiconductor Device Fabrication Techniques

2.3.1 Ion Implantation

Ion implantation is a versatile materials processing technology which uses high energy ions to modify the properties of a material. Ions with energies above approximately 1 keV/u penetrate below the surface of solid materials and come to rest at a depth determined by their energy [30]. The problem of the depth of penetration of energetic ions into solid matter (the so-called "ion-stopping problem") is a classic one that has been studied since the time of Niels Bohr [31]. It has been calculated for both elements as well as compounds [32]. The large amount of historical, theoretical, and experimental work on the stopping problem has been codified into a widely-used computer code called SRIM[33]. SRIM is the most widely-used, standard simulation code for calculating the disitance energetic ions travel in a solid before coming to rest. This is the so-called "projected range" R_p. The projected range of an energetic ion is the mean distance it travels before coming to rest. Because of the stochastic nature of the nuclear collision processes involved in bringing the ion to rest, the depth of a set of ions implanted into a solid is described by a distribution. This distribution is well-described by a skewed Gaussian curve. The mean value of this Gaussian is the projected range and the standard deviation of this Gaussian curve is referred to as the "longitudinal straggle" (the ions also experience lateral deviations due to scattering as they come to rest; this is referred to as "lateral straggle"). The SRIM code can be used to calculate the parameters of the ion implant projected range and longitudinal straggle; a summary of select topics addressed by SRIM follows.

Figure 2.8 shows ion penetration depth distributions for energetic hydrogen ions (i.e. protons) into silicon calculated using SRIM. It can be seen that for energies of 2.5 keV per

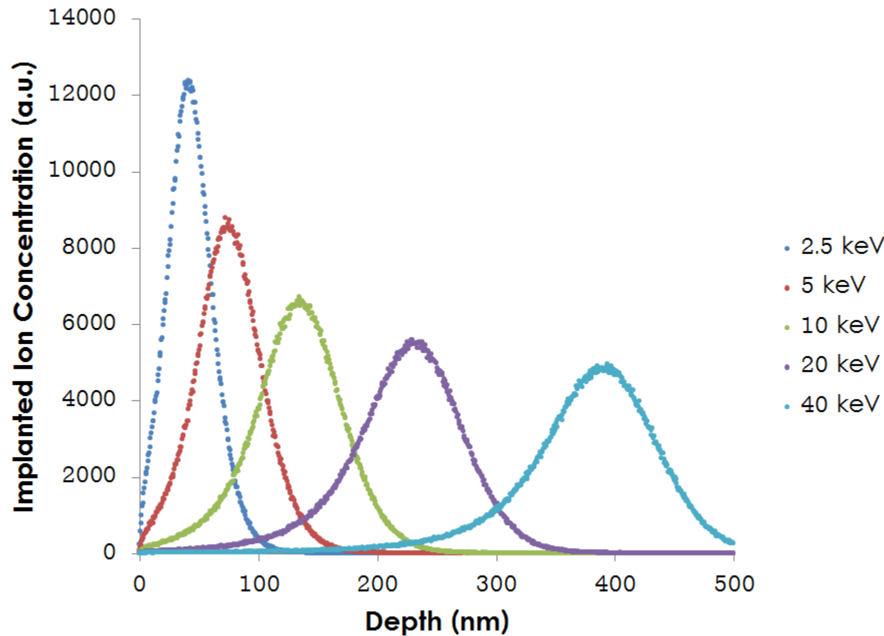


Figure 2.5: Relative concentration vs depth profiles for implantation of energetic H^+ ions (e.g. protons) into silicon for energies between 2.5 keV and 40 keV. The SRIM 2013 simulation code [32] was used to simulate trajectories of 10^6 protons striking the silicon target for each energy chosen; a bin size of 0.6 nm was used. For the proton implant energy of 2.5 keV relevant for this work SRIM predicts a projected range $R_p = 40.3$ nm and a longitudinal straggle $\Omega_R = 28$ nm.

proton (used in this work) the mean penetration depth is approximately 40 nm.

Flux, Fluence, Concentration and Dose

In plasma ion implanation the target wafer being implanted is exposed to a flux of projectile ions (molecular hydrogen ions H_2^+ in the case of this thesis). The flux of energetic projectile ions striking the target surface is $J(t)/e$ where $J(t)$ is the time-dependent current density extracted from the plasma, and e is the elementary charge (note that it is assumed here that all the ions extracted from the plasma are singly ionized, with charge = +1 e. It is very difficult to maintain higly charged ions in an ICP plasma, with ECR (electron cyclotron resonance) sources being required for this.

Because of the high density of ions in an ICP plasma, the flux of energetic ions delivered to the target wafer is quite large. This can cause significant wafer heating and even buckling

or melting. PII systems are therefore usually pulsed, with a pulse repetition frequency (prf) $\sim$ 1 kHz. The total integrated flux delivered to the target wafer is usually referred to as the "fluence" F (units = ions/cm^2 or simply cm^{-2}) and can be written as follows (note that the symbol Φ is sometiomes used for fluence but since we are concerned with electronic devices and Φ is widely used for potential we will use F for fluence):

$$F = N_{pulses} \int_0^{t_{pulse}} (J(t)/e)dt \tag{2.18}$$

The total ion fluence delivered to a target wafer during an ion implantation process often referred to colloquially as the "dose".

Due to the multiple scattering processes which occur when an energetic ion enters a target material, the ions come to rest below the surface and are distributed through a volume referred to as the "implanted region". This region contains the implanted ions (typically as interstitial impurities as well as many vacancies due to target atoms being scattered out of the lattice as well as target atom interstitials lodged where they have come to rest (the combination of vacancy plus interstitial is referred to as a Frenkel pair. See Figure 2.6). Note also that the term Schottky defect refers to a single vacancy with no corresponding interestitial atom. Schottky defects are to be expected when a film is grown because vacancies may be produced due to imperfect deposition. Frenkel defects are expected to dominate the damaged region in ion implantation because each vacancy results from a displaced target atom which remains in the crystal.

The Stopping of Energetic Ions in Matter

Sigmund [30] lists the following processes which affect the stopping of charged ions in matter:

1. Excitation and ionization of target electrons

2. Projectile excitation and ionization

3. Electron capture

4. Recoil loss (also known as "nuclear stopping")

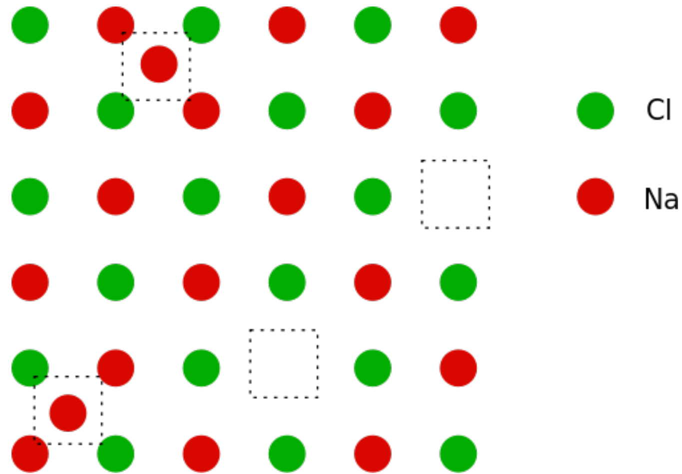


Figure 2.6: Schematic of Frenkel defect showing displaced atoms as occupying interstitial positions and leaving behind vacancies. Each interstitial-vacancy pair is referred to as a Frenkel defect. Figure author Gabriel Rosser, Oxford University, used under the Creative Commons Attribution-Share Alike 3.0 Unported license.

There are additional processes (electromagnetic radiation and nuclear reactions) which can occur, but these are negligible for ions except at very high energies. The nuclear stopping process dominates at low and medium ion velocities and when the ion velocity v is less than the Bohr velocity $v_0 = \frac{c}{137.036}$; we are in the low-speed region. Here the ion velocity is less than that of all but the outer shell electrons of the target atoms. Roughly this corresponds to an energy per nucleon being less than 20 keV/u.

When energetic ions strike a target material, a number of processes can occur. When the ion energy is greater than 0.1 keV, the ion will penetrate the target and travel within it before coming to rest. Note that if the ion is a molecular ion, such as H_2^+, it will fragment upon striking a solid target with each fragment taking a mass-weighted fraction of the original molecular ion energy. This occurs because the projectile ion kinetic energy typically greatly exceeds the chemical binding energy of the molecular ion (2.8 eV for H^{2+} [34]). calculation of the slowing of the energetic ion in the target is referred to as the "stopping problem." It is characterized in terms of the so-called "stopping power" (this is a mis-nomer; the correct term should really be "stopping force" [35] but convention dictates the use of the former term):

$$F_s = -\frac{dE}{dl} \tag{2.19}$$

Where E is the energy of the incident projectile ion (extracted from a plasma for this work, as discussed below), and l is the length traversed in the target. It can be seen by inspection that this has units of force.

It is common to denote a "stopping cross-section," S:

$$S = -\frac{1}{n}\frac{dE}{dl} = \frac{1}{n}F_s \tag{2.20}$$

Where n is the number density of atoms in the target (e.g. 5×10^{22} atoms/cm^3 for silicon).

Range along the path:

$$R = \int_0^{E_0} \frac{dE}{nS(E)} dE \tag{2.21}$$

Range Straggling

The projected range is always less than the full distance travelled by the ion because of its lateral straggling. This is illustrated in Figure 2.7. We may refer to the detour factor, $\frac{R_p}{|R|}$; this is always less than one. The energy loss due to straggling is described by the variance Ω_R^2. The energy loss spectrum tends toward a Gaussian as the energy loss exceeds the energy loss in a single scattering event [31].

$$\Omega_R^2 = \int_0^{E_0} \frac{nw(E)}{[nS(E)]^3} dE \tag{2.22}$$

Where $w(E)$ is the average energy lost per collision.

Figure 2.8 shows the results of the SRIM code used to calculate ion projected range and straggle. SRIM predicts the following parameters for the 2.5 keV H^+ ions (i.e. protons) used to implant the silicon Schottky diodes fabricated in this thesis:

Projected range: $R_P = 40.3$ nm

Longitudinal straggle: $\Omega_R = 28.0$ nm

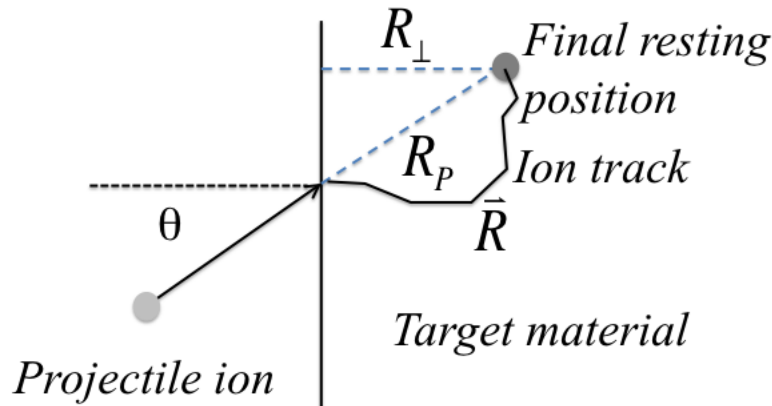


Figure 2.7: Schematic illustration of range concepts. The projectile ion strikes the target at angle θ as shown. The ion follows a non-linear path due to multiple stopping events before coming to rest. The projected range R_P is the distance of the entry point of the ion to its resting point along the axis defined by the original direction of the projectile ion. Note that the projected range is always less than the full distance traversed by the ion. (After Figure in [30])

Lateral straggle: 22.8 nm

Note that the lateral straggle is the distance travelled by the ion perpendicular to its original trajectory due to direction-changing nuclear collisions. Note also that SRIM reports distances in Angstrom units which have been converted to nm.

Channeling

Channeling effects in which ions move along relatively open channels in the crystal lattice of the target material can increase the ion range by reducing scattering due to nuclear stopping. These effects generally occur at higher energies ($>$ 50 keV) and can generally be ignored for energies accessible using plasma ion implantation

Defect Formation

Implantation of energetic ions into a crystalline target results in damage to the crystal lattice. Atoms of the target material (silicon for this thesis) are displaced from their lattice positions (leaving behind a vacancy) and come to rest in new interstitial positions, i.e. between other lattice atoms. The resulting crystal lattice defect consists of one displaced (and now interstitial) target atom + one vacancy. Together the interstitial + vacancy are referred to as a "Frenkel pair". The number of defects produced per unit volume N_d can be estimated using the following formula:

$$N_d = N\sigma_d \nu F \tag{2.23}$$

where N is the number of atoms per unit volume of target material ($N = 5 \times 10^{22}$ atoms/cm^3 for silicon), σ_d is the cross section for production of the "primary defects", i.e. the first target atom knocked out of its lattice position, usually referred to as "primarily knocked-out atoms" or PKA [36], ν is the average number of displaced atoms for each PKA ($\nu > 1$ due to recoil cascades), and F is the fluence of projectile ions.

The Khinchin-Pease model [36] is usually used to calculate ν, as follows:

$$\nu = \frac{\left(\frac{dE}{dx}\right)_N}{(2E_d)(N\sigma_d)} \tag{2.24}$$

The above Khinchin-Pease approximation, when substituted for the expression for N_d above, gives the following final result for the number of defects formed in terms of the total fluence F of ions delivered:

$$N_d = F\left(\frac{dE}{dx}\right)_N / 2E_d \tag{2.25}$$

where $(dE/dx)_N$ is the "nuclear stopping power", e.g. the energy lost by the projectile ion per unit length travelled in the target due to the contribution of nuclear scattering events to the total stopping power. Note that this is not the total energy loss experienced by the ion as a significant amount of the ion's energy is lost to interactions with the electrons of the target material. It is these nuclear scattering events which lead to displacement of target lattice atoms and thus Frenkel defects. SRIM 2013 was used to calculate the nuclear

stopping parameter and gave $(dE/dx)_N = 0.188$ eV/angstrom. E_d is the threshold energy for the formation of a Frenkel defect pair. For a typical semiconductor 15 eV $< E_d <$ 20 eV [36].

Damaged Layer

The average volume concentration of implanted ions N_i in the implanted region is given by

$$N_i = F/2\Omega_R \tag{2.26}$$

where F is the total implanted fluence (ions/cm^2) and Ω_R is the (longitudinal) range straggle.

Amorphizing Dose

Nuclear stopping results in recoil of the target atom. The recoil energy can be large enough to displace the target atom from its lattice position, leaving behind a vacancy. The recoiling atom itself can have enough energy to cause subsequent recoils due to nuclear stopping collisions. This is referred to as a "recoil cascade." The resulting buildup of vacancies results in a damaged crystal lattice in the implanted layer. When the ion fluence exceeds a critical value, the damage is so great that all long-range order is lost and the layer becomes amorphous. A rough estimate for the amorphizing dose is obtained by setting the density of induced defects equal to the atomic density of the target crystal (e.g. $N_d = N_{silicon}$ for silicon targets). In general for medium mass ions in silicon the median amorphizing dose corresponds to $\sim 10^{14}$ ions/cm^2. The exact number depends on the particular ion used. [37]

2.3.2 Annealing

A substance's crystal structure is its state of lowest potential energy. Annealing a crystal is the process of heating it to the point at which its atoms have enough energy to move around, but not so much as to melt it. As the material cools, its atoms are allowed to find and settle into the positions of lowest potential energy. This process is affected not only by its temperature and duration but by the cooling rate as well. Quenching an anneal freezes

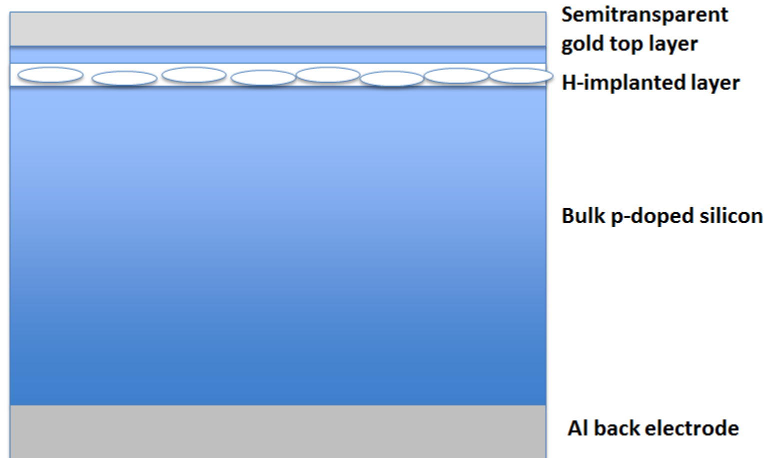


Figure 2.8: Schematic of silicon LED device fabricated for this thesis work. The device is a Schottky type diode with a semi-transparent gold top electrode forming the Schottky contact and also providing access for light extraction.

atoms in place, leaving unnecessary defects behind, whereas a slow cool allows the atoms more time to settle and increases the likelihood that they settle into crystal lattice positions.

2.3.3 Gettering

The concept of gettering originated in the context of vacuum systems, in which a getter is a reactive substance used to chemically react with residual gases and thus sequester them. In the context of metallurgy, a gettering substance removes impurity atoms from the gettered material. Impurities and their associated defect hinder electroluminescence because they provide competing non-radiative pathways for electrons to fall from the conduction band to the valence band.

Oxygen Gettering

Oxygen has been found to getter iron in silicon[38]. Defect sites associated with SiO_2 precipitates serve as nucleation sites for silicide precipitates, significantly accelerating their formation. This does not affect the solubility of interstitial iron atoms but does effectively sequester iron. Considering the ubiquity of oxide layers coating silicon, some $FeSi_x$ precipitate formation is to be expected as a by-product of thermal processing. A schematic of an

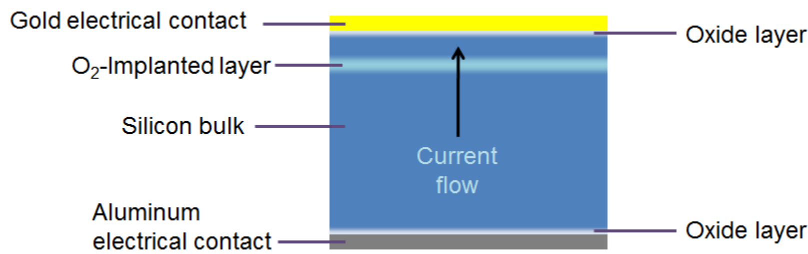


Figure 2.9: Cross-sectional view of an O_2-implanted Au/p-type Si Schottky diode.

oxygen-implanted device is depicted in Figure 2.9.

An implanted oxygen layer would form SiO_2 precipitates and could act as a getter of iron, but could significantly add to the resistance of any resulting devices. Any gains due to gettering would almost certainly be negated by this added resistance. Moreover, there are already two naturally occurring oxide layers incorporated into the device.

Phosphorus Diffusion Gettering

Phosphorus diffusion gettering (PDG) is not fully understood. Myers [39]suggests a mechanism which converts substitutional impurities to interstitial impurities; this mechanism is described below. These interstitials then migrate from the bulk to the near-surface region where the mechanism is inactive and the impurities switch back to substitutional positions. During phosphorous in-diffusion, interstitial phosphorous atoms (P) form bound pairs (P-I) with interstitial silicon atoms (self-interstitials, I). As these P-I pairs diffuse into the bulk and out of the region of phosphorus saturation they break up, leading to a super-saturation of self-interstitials. The self-interstitials then kick out substitutional metal impurities which diffuse in turn to the near-surface region where P concentrations are high and the self-interstitials are still bound in P-I pairs. Myers reported a difference in concentratios of five orders of magnitude between the near-surface region and the gettered bulk.

Unfortunately, any luminescent nanostructures formed by ion implantation with energies on the order of 10kV will be in the near-surface region where impurities gettered by PDG are deposited, rendering them incompatible.

Figure 2.10: Cross-sectional view of phosphorus diffusing into a silicon wafer during PDG. Impurities diffuse from the bulk into the region of phosphorus-rich silicon.

Aluminum Gettering

Aluminum gettering takes advantage of the low Al-Si eutectic point at 577 °C and the fact that above this point, 3d metal impurities (such as Fe, Co, Ni, and Cu) are much more soluble in the Al-Si melt than in silicon. By applying a layer of aluminum to one side of the silicon wafer and heating it above the eutectic point, metallic impurities simply diffuse from the silicon bulk into the melt at the interface. This process is somewhat reversible. That is, as the system cools, impurities diffuse back into the bulk from the melt. However, the solubility remains greater in the melt than in silicon and diffusion of most impurities does not occur quickly enough to negate the sequestering effect.

Of these techniques, aluminum gettering was considered to be the most promising and an attempt was made to test its effects on the devices fabricated for this work. The method used to implement it is described in Section 3.1.2.

2.4 Structure of Light Emitting Semiconductor Devices

This thesis describes the fabrication of silicon Schottky LEDs based on a nanocrystalline silicon light-emitting layer. The Schottky LED architecture is an ideal platform from which to investigate different approaches to nanocrystalline light-emitting silicon LEDs because it is relatively simple to fabricate. Since the silicon Schottky LED is the simplest possible semiconductor light-emitting device, it will be useful to briefly review the structure of more complex semiconductor light emitters.

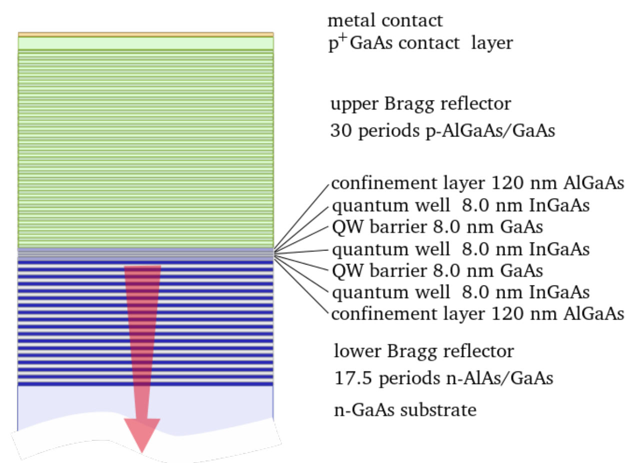


Figure 2.11: Vertical cross-sectional view of the semiconductor die in a VCSEL. The active electroluminescent layer is quite thin, only a few wavelengths of light thick. It is sandwiched between distributed bragg reflectors to form an optical cavity. By reflecting photons back and forth, these reflectors extend the amount of time spent in the cavity by the photons and their chance of stimulating emission of further photons. The reflector must allow electrical current to pass through to drive the active layer. Figure from Wikimedia Commons.

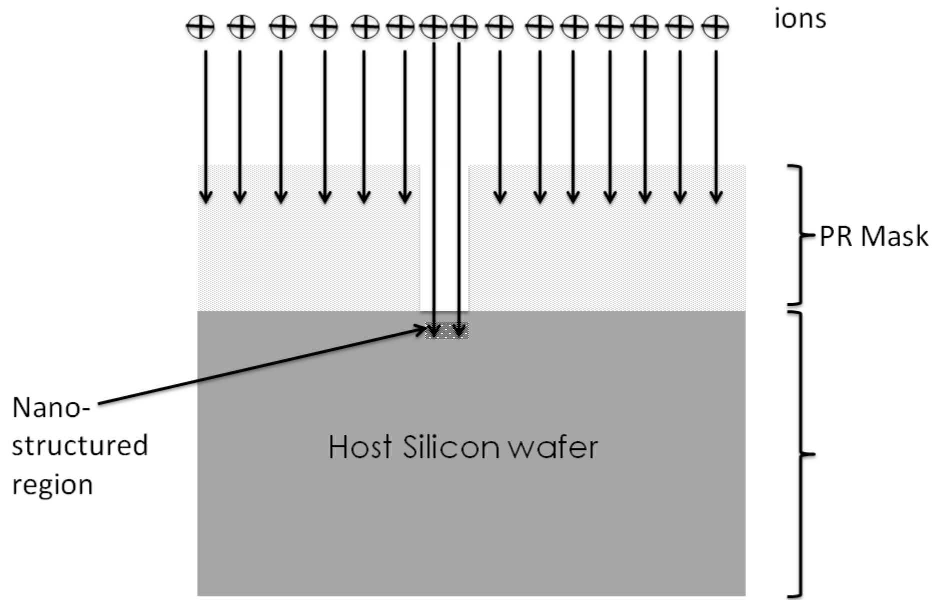


Figure 2.12: A polymer photoresist (PR) mask is used to perform an ion implant on a specific location. The ions are stopped by the mask, but are implanted the semiconductor where the mask was removed by photolithography. Following ion implantation the mask is removed by a plasma ashing step.

The nanocrystalline silicon light-emitting layer formed by the processing techniques described in this thesis could potentially serve as the basis for a silicon-based laser for on-chip optical communications. Such a laser would require two high-reflectivity reflectors to form the laser cavity with the light-emitting silicon nanocrystalline layer sandwiched in-between. The most likely architecture would be that of the Vertical Cavity Surface Emitting Laser (VCSEL) architecture as shown in Figure 2.11. VCSELs emit light vertically as opposed to the more classical edge-emitting lasers. The chief advantage provided by this architecture is that such lasers could be placed in silicon devices at arbitrary positions, rather than being restricted to an edge.

The fundamental structure of the VCSEL is shown in Figure 2.11. Stimulated emission occurs in a layer parallel with the surface. Since this layer is thin only a few wavelengths thick and light can pass through it quickly without stimulating further photon emission, it is important to reflect photons back through the layer multiple times in order to increase the gain in optical signal. This requires reflectors with high transparency and reflectivity;

such properties are found in distributed Bragg reflectors (DBR), which employ constructive interference and whose reflectivity may be increased by adding layers.

Note that the horizontal width of the device is unimportant to its operation; such a laser could be scaled from 1 cm wide in its horizontal dimensions to 1 um wide without changing the quality of its optical output as long as the current density driving it remained constant. Our devices require drive currents of 2.5A, which is large for an LED, but this is because the devices themselves are physically large at 1 square centimeter. Their current densities are 2.5A/cm^2, which is comparable to drive currents of typical LEDs.

PII implants the entire surface of a target with atoms, but this is not always desirable. It is not difficult to restrict an implant to specific locations, however, with the use of a mask. This is a protective layer applied to the target before implanting through which the accelerated ions cannot pass. Holes in this layer are made at the locations where an implant is desired. When the implant proceeds, it only affects the locations unprotected by the mask. This is a common procedure in silicon device fabrication.

Chapter 3

Experimental

3.1 Fabrication of Silicon LEDs

The first part of this chapter describes the fabrication process used to make our visible-light emitting silicon LEDs. These devices are based on a nanostructured silicon buried layer fabricated into a Schottky diode-type device with a semi-transparent gold top electrode. It is important to note that all fabrication steps (ion implantation, thermal processing, and contact deposition) were carried out in-house at the University of Saskatchewan.

The experimental matrix describing the devices fabricated for this thesis was given in Table 1.1. The following subsections give the detailed parameters for the PII, annealing, and gettering steps used in the device fabrication. A detailed summary of the processing conditions for each device is given in Table 3.2. All devices were fabricated from stock silicon wafers with a standard <100> crystal orientation (purchased from University Wafer Inc.). The wafers were p-doped in the melt with boron, to give a final quoted lot resistivity range of 5-25 Ω·cm. A single wafer was used for all devices; post implant the wafer was diced into 1 cm × 1 cm pieces.

3.1.1 Plasma Ion Implantation (PII)

Ion implantation was introduced in the previous chapter. Its versatility has led it to become a major processing technique in semiconductor device fabrication. In this work, ion implantation was used to modify the nanostructure of silicon below the surface of the silicon wafer. The ordered silicon lattice (which gives rise to the indirect band structure) was made amorphous (amorphized) by implanting a very high dose of hydrogen ions at an energy of 2.5

keV/proton leading to a mean depth of 40 nm over an implantation region of approximately 40 nm total width (this was due to the longitudinal straggle).

The extremely high ion doses required to amorphize the silicon lattice and render it ready for a thermally driven nanocrystallization cannot easily be achieved by conventional, accelerator-style beamline ion implanters. A better technique is that of plasma ion implantation (PII) [40]. Plasma tools are widely used in the semiconductor industry to etch, deposit thin films, and otherwise modify semiconductor wafers [41]. PII takes advantage of the very high ion concentrations achievable in inductively-coupled plasmas (ICP). The PII system in the Plasma Lab at the University of Saskatchewan is described in [42] and has been used in a variety of semiconductor applications. A custom-designed, fast-switching high voltage modulator based on insulated-gate bipolar transistors (IGBTs) is used to provide the high voltage pulses which accelerate the ions toward the silicon target [43]. A schematic of this system is shown in Figure 3.1.

For this work, the plasma chamber was evacuated to a base pressure of 1.7×10^{-5} Torr then fed H_2 gas at a mass flow of 20 sccm to a pressure of 1.0×10^{-2} Torr. Radio frequency (RF) power was applied through an inductive coil, separated from the vacuum chamber by a quartz window, to generate a dense hydrogen ion plasma. Langmuir probe measurements were used to characterize the plasma parameters. The Langmuir probe system is described in [7]. The electron temperature was $T_e = 2.63 \pm 0.26$ eV, its plasma density and potential were $n_0 = 1.12\times10^{15} \pm 0.12\times 10^{15}$ m^{-3} and $\Phi_{plasma} = 12.5\pm 1.3$ V, respectively.

Using in-house software developed by our group and based on the Lieberman model [44] and discussed further in Risch *et al.* [45], we calculate $J(t)$ during the pulse. Note that $J(t)$ is not constant because of plasma sheath expansion effects. The fluence per pulse $F_{pulse} = \int_0^{t_{pulse}}(J(t)/e)dt$ is calculated by the code using input plasma parameters n_{ion} and T_e measured using a Langmuir probe system described above. The total fluence ("dose") is given by $F = N_{pulses} \times F_{pulse}$. The H_2^+ ions were implanted with a total fluence of $F = 4.0\times10^{15}$ cm^{-2} and an energy of 5 keV, applied in square-wave pulses at a frequency of 50.8 Hz and a duration of 22.6 μs, for a duty cycle of 0.11%.

The SRIM (Stopping and Range of Ions in Matter) program of Ziegler *et al.* [33] was used to predict the implant depth . SRIM has been well-calibrated by many workers for common

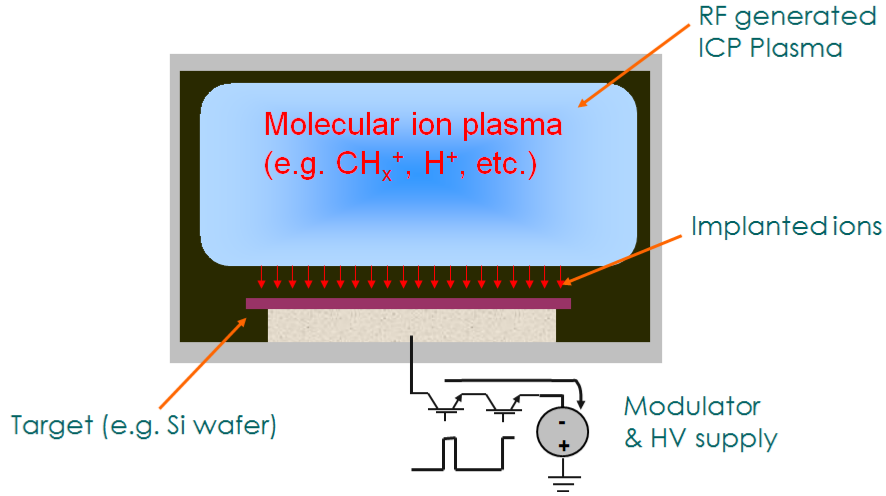


Figure 3.1: Schematic of the RF ICP plasma chamber used in this work. For more details see Risch *et al.* [42]

ion species in silicon and the results are generally quite accurate. Upon impact the 5 keV H_2^+ ion fragments into two 2.5 keV protons because the kinetic energy is so much greater than the 2.8 eV bonding energy of the molecular hydrogen ion. Because of this fragmentation the total fluence of protons delivered by the process is 8 $\times 10^{15}$ cm^{-2}, twice the fluence of molecular hydrogen ions. This is a very high implanted proton dose resulting in an average concentration of protons in the implanted region of $N_{proton} \approx F_{proton}/2\,\Omega_R = 4 \times 10^{15}\text{cm}^{-2}/56 \times 10^{-7}$ cm $= 7 \times 10^{20}$ protons/cm^3 (as shown in Figure 2.8 the longitudinal straggle $\Omega_R \approx 28$ nm $= 28$ $\times 10^{-7}$ cm).

3.1.2 Annealing Processes

The wafer was then cut into pieces roughly 1 cm square, 8 of which were then annealed at temperatures of either 400 °C or 700 °C, for durations of 30 or 120 minutes. The anneals were performed in rough vacuum.

Property	Typical value
Base Gas Pressure	17 μTorr
H_2 Gas Pressure	10 mTorr
Plasma Density	$1.12 \pm 0.12 \times m^{-3}$
Plasma Potential	12.5 ± 1.3 V
Electron Temperature	2.636 ± 0.26 eV

Table 3.1: Characteristics of a hydrogen plasma typically produced in the lab's ICP chamber.

Gettering

Devices 9 – 16 were created to attempt test the effect of aluminum gettering. For these 8 devices, the aluminum backcontacts were applied prior to the anneal so that the anneal heating step could be combined with the gettering thermal treatment. These treatments were combined to avoid annealing devices 9 – 16 an extra time. Devices 9, 11, 13, and 15 were prepared to test the effect of gettering on the quality of the aluminum backcontact's electrical performance. They were to be coated with a second aluminum back contact after the anneal/gettering heating was performed. Ultimately this proved unnecessary as the aluminum contact exhibited unremarkable electrical performance.

The complete set of annealing and gettering conditions of the devices are summarized in Table 3.2.

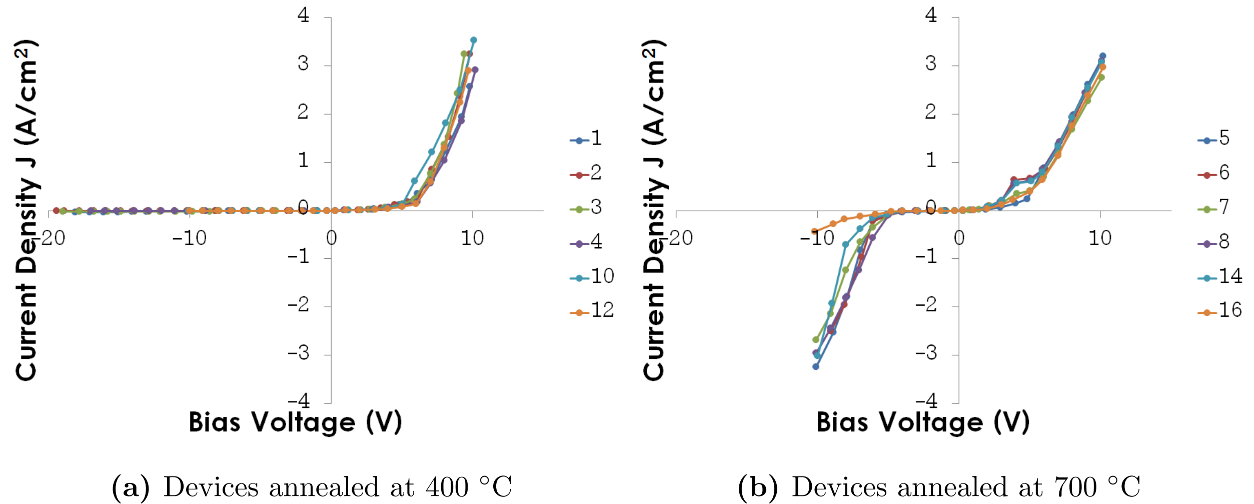
3.1.3 Contact Formation and Diode Behaviour

The gold and aluminum contacts were then applied by physical vapour deposition to thicknesses of 22.5 nm for the gold contact and 1519 nm for aluminum. To activate them the devices were annealed a second time in rough vacuum at a temperature of 400 °C. This "contact firing" was necessary to obtain high-quality, stable Schottky diode characteristics.

A 1519 nm thick aluminum ohmic back contact was applied using physical vapour deposition. This was followed by the deposition of a thin, semi-transparent front side Schottky

Device	Aluminum Gettered?	Anneal Temperature (°C)	Anneal Duration (minutes)	Aluminum Contact Re-applied?	H_p (dimensionless)
1	No	400	30	N/A	5.16
2	No	400	30	N/A	5.16
3	No	400	120	N/A	5.56
4	No	400	120	N/A	5.56
5	No	700	30	N/A	7.47
6	No	700	30	N/A	7.47
7	No	700	120	N/A	8.05
8	No	700	120	N/A	8.05
9	Yes	400	30	No	5.16
10	Yes	400	30	Yes	5.16
11	Yes	400	120	No	5.56
12	Yes	400	120	Yes	5.56
13	Yes	700	30	No	7.47
14	Yes	700	30	Yes	7.47
15	Yes	700	120	No	8.05
16	Yes	700	120	Yes	8.05

Table 3.2: Summary of the anneal and gettering conditions of the devices fabricated for this work. Devices 9 – 16 were gettered, but are otherwise prepared identically to devices 1 – 8. Note that device 10 was destroyed as a result of human error.



(a) Devices annealed at 400 °C **(b)** Devices annealed at 700 °C

Figure 3.2: Current-voltage behaviour. Note that the semi-transparent gold contact is the negative electrode. The devices show classic diode behaviour with no reverse breakdown up to -20V reverse bias among the devices annealed at 400 °C, whereas there is reverse breakdown at -7V reverse bias among all but one of the devices annealed at 700 °C (probably due to trap-assisted tunneling). In the forward bias direction their diode knees are around 5V. The slope of the forward curve of the 700 °C-annealed devices indicates a higher resistivity.

contact consisting of 22.5 nm gold. To ensure good silicon-gold contact the devices were low-temperature fired in vacuum at 400 °C, well below the melting point of aluminum (660 °C). Following the contact firing the current-voltage curves of the devices were measured. Figure 3.2a shows the current-voltage curve for the 400 °C annealed devices. These data exhibit rectifying behaviour with no reverse breakdown up to -20V and a forward-bias knee voltage around 5 V. Figure 3.2b shows the current-voltage curve for the 700 °C annealed devices. The most striking difference is that these high-temperature annealed devices exhibit reverse breakdown around -7 V. This is probably due to trap-assisted tunneling, as illustrated in Appendix A.

Both sets of devices exhibited classic Schottky diode-like behaviour which will be discussed in more detail below. In addition, all the devices exhibited visible light emission when forward biased. This was easily visible to the naked eye in a darkened room at drive current densities of 2.5 A/cm^2, which is comparable to the drive densities used in conventional III-V based LEDs.

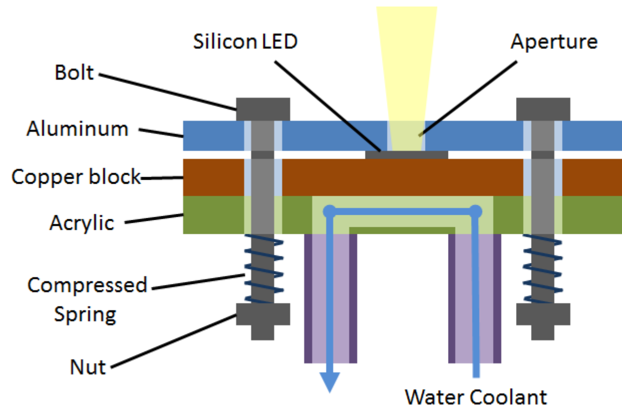


Figure 3.3: Schematic of the spring-loaded device holding clamp. It allows simultaneously for the electrical biasing and water cooling of the device while electroluminescence measurements are taken through the aperture. The silicon devices are 0.5 mm thick and have a cross-sectional area of ∼1 cm × 1 cm. Devices are held firmly in fixed position by this apparatus, as is the light collector of any spectrometer taking measurements.

3.2 Characterization of Silicon LEDs

3.2.1 Device Holder

The silicon Schottky LEDs fabricated by the above procedure were clamped in a custom-designed, spring-loaded, water-cooled device holder assembly (described in [7]). A schematic of the device holder is shown in Figure 3.3. The cooling was necessary because the high forward current of the devices at the operating voltage resulted in significant power dissipation. The spring-loaded clamping was necessary to achieve good electrical contact to these large area ∼1 cm × 1 cm devices. The metal clamp contacting the semi-transparent gold top electrode had a threaded circular aperture into which a fiber optic cable mount could be attached in order to facilitate electroluminescent spectrum measurements as described further below.

3.2.2 Current-Voltage Measurement

Current-voltage curves were measured for each device using the assembly shown in Figure 3.3. The measured currents were normalized by the device cross-sectional area (in units of

cm^2) to obtain curves of diode current density J vs bias voltage V over the range from -20 V $< V <$ 12 V. These curves of current density vs voltage are plotted in Figure 3.2. Note that for these Au/p-type silicon Schottky LEDs the forward bias is achieved when the gold electrode is made more negative than the aluminum ohmic back contact.

3.2.3 Device Heating

The devices were tested for forward luminescence with a forward current around 2.5 A and forward device voltage drop of $\approx$ 9 V. This resulted in power dissipation $P = VI = 22.5$ W. This non-trivial power dissipation resulted in Joule heating and a rise in the diode operating temperature. Because of the need for electrical isolation as well as optical access it was difficult to make accurate measurements of the device temperature during forward bias operation. However, the temperature rise may be estimated because the thermal properties of silicon are well known [46]. These are given in Table 3.3.

Using a simple lumped thermal model, the temperature rise due to the joule heating

$$\Delta T = P \times R_{TH} \tag{3.1}$$

Where the effective "thermal resistance", R_{TH}, is given by:

$$R_{TH} = \left(\frac{1}{\kappa}\right)\left(\frac{L}{A}\right) \tag{3.2}$$

Where L is the device thickness and A is the cross-sectional area. This calculation gives $R_{TH} = 0.039$ °C/W and thus predicts a temperature rise $\Delta T = 0.87$ °C. The thermal equilibration time for the silicon device is given by

$$\tau_{TH} = A/\alpha = 1\text{cm}^2/0.8\text{cm}^2\text{s}^{-1} = 1.25\text{s} \tag{3.3}$$

This is the time constant for the device to come to thermal equilibrium. Note that these estimates are based on a lumped model and do not take into account lateral variations of conductivity across the device and as a function of depth. However, they are sufficient for first-order estimates. These calculations show that although the device power dissipation is fairly high, device heating is not too great of a problem. It should also be borne in

Thermal Properties	Typical value
Thermal Conductivity κ	1.3 W/cm °C
Specific Heat c_P	0.7 J/g °C
Thermal Diffusivity α	0.8 cm^2/s
Melting Point $m.p.$	1412 °C

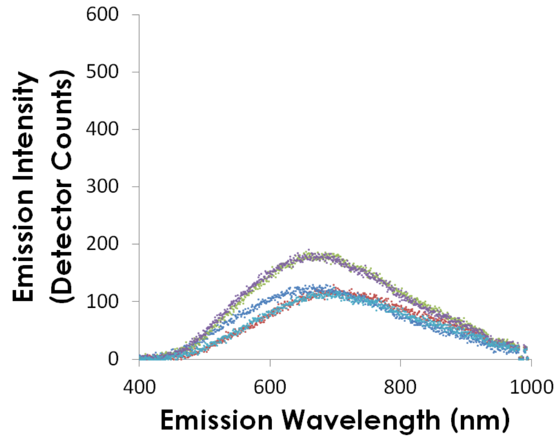
Table 3.3: Thermal properties of silicon. Source: online semiconductor reference data from Ioffe Institute [46].

mind that when implemented in CMOS, the cross-sectional area of the LEDs would be much smaller, resulting in a correspondingly smaller power dissipation. What is important is that while the power dissipated by these large area devices may seem somewhat large, the power dissipation per unit area is not excessive and thus device heating will not be a major problem for applications.

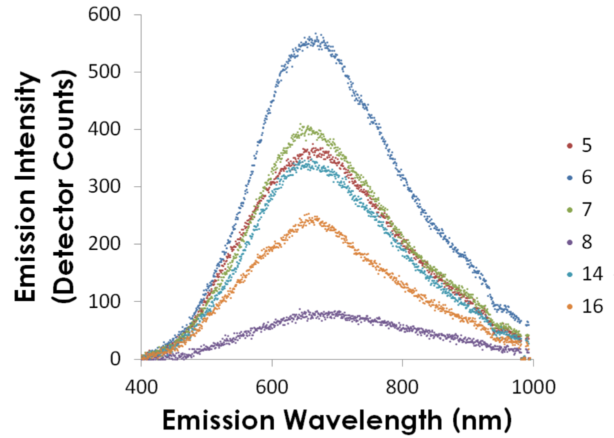
3.2.4 Electroluminescent Spectrum Measurement

When forward biased, all the fabricated devices exhibited broadband, visible spectrum electroluminescence emission, visible to the naked eye in a darkened room. The apparent colour was orange in hue, which is typical of silicon nanocrystals and porous silicon light emission. The devices did not exhibit light emission when reverse-biased. A fiber-optic cable was used to guide the emitted light to an Ocean Optics Spectrometer interfaced to a computer for spectral data acquisition. The spectra were acquired at a constant forward current density of $J = 2.5$ A/cm^2 for all devices. These electroluminescent spectra are graphed in Figure 3.4.

The most dramatic result in the EL data is the effect of anneal temperature. Most devices annealed at 700 °C emitted twice as much light as the devices annealed at 400 °C, but they exhibit wider variation: the devices which exhibited both the least and greatest luminescence were annealed at 700 °C. Longer anneal duration improved electroluminescence, but this effect is only apparent in the 400 °C-annealed devices. The wide variance among the devices annealed at 700 °C may be masking any effect anneal duration has at that temperature.

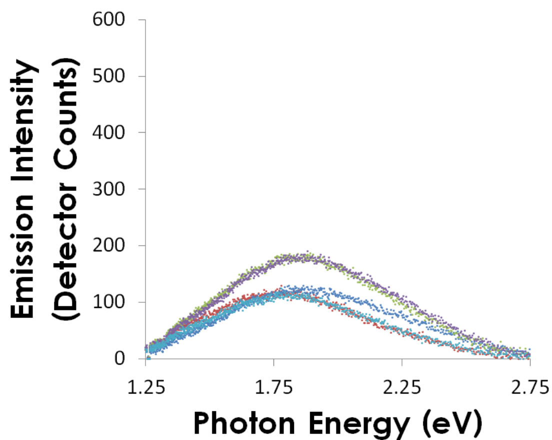


(a) Devices annealed at 400 °C

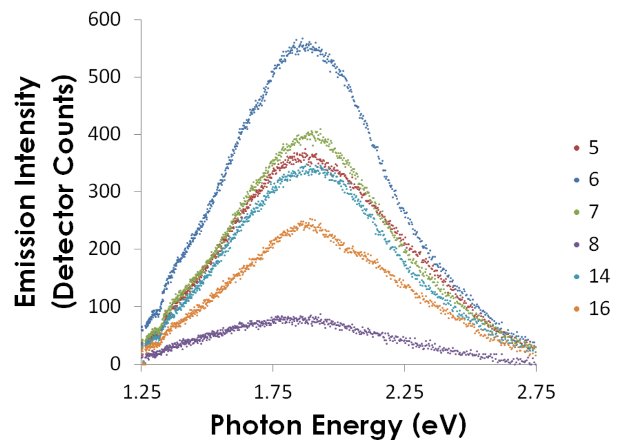


(b) Devices annealed at 700 °C

Figure 3.4: Emission spectrum of the devices plotted vs wavelength (in nm). Plotted in (a) are the devices annealed at 400 °C, whereas the devices in (b) were annealed at 700 °C. Note that all of the devices in (b) except device 8 were brighter than the 400 °C-annealed devices. The electroluminescence spectra were measured at a constant current density of $J = 2.5$ A/cm^2 for all devices.



(a) Devices annealed at 400 °C



(b) Devices annealed at 700 °C

Figure 3.5: Emission spectrum of the devices plotted vs photon energy $\hbar\omega$ (in eV units). Note that the skewness due to plotting vs wavelength has disappeared.

Chapter 4

Characterization of Fabricated Silicon LEDs

4.1 Forward Bias J vs V Analysis

It is well-known that semiconductor junction diodes (both pn and Schottky) exhibit an exponential increase of the current as a function of the voltage in the forward bias direction. Figure 4.1 shows the band diagram for such a device. For this reason, the electrical parameters of semiconductor junction devices are normally analyzed by plotting a *log-linear* JV curve (i.e. a plot of current density J vs forward bias voltage V graphed with a logarithmic vertical axis). Such log-linear curves are plotted in Figure 4.2 for the devices fabricated for this thesis. Inspection of these log-linear JV curves shows clearly two distinct regions with different slopes (corresponding to different ideality factors η). Such two-component behaviour is common in nanocrystalline silicon LEDs. It is conventional to fit each region with separate values J_s and η. The break for these devices — the crossover from high η to low η — occurs around 2 V for both 400 °C- and 700 °C-annealed devices. By using least-squares best fit straight line to the

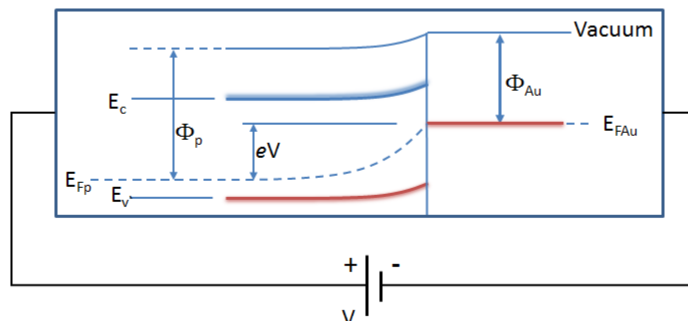
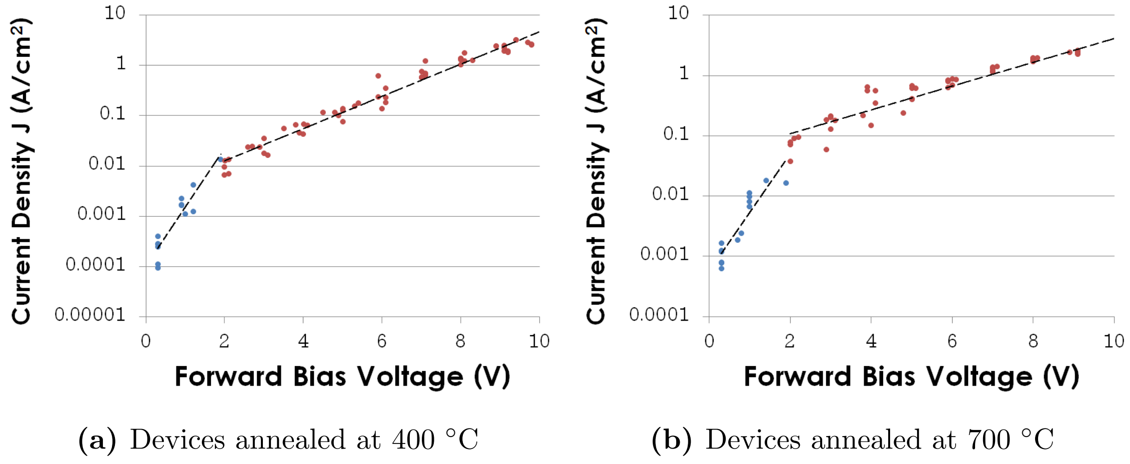


Figure 4.1: Forward-biased “ON-state” Au/p-type Si Schottky junction. V is the voltage drop across the diode junction.

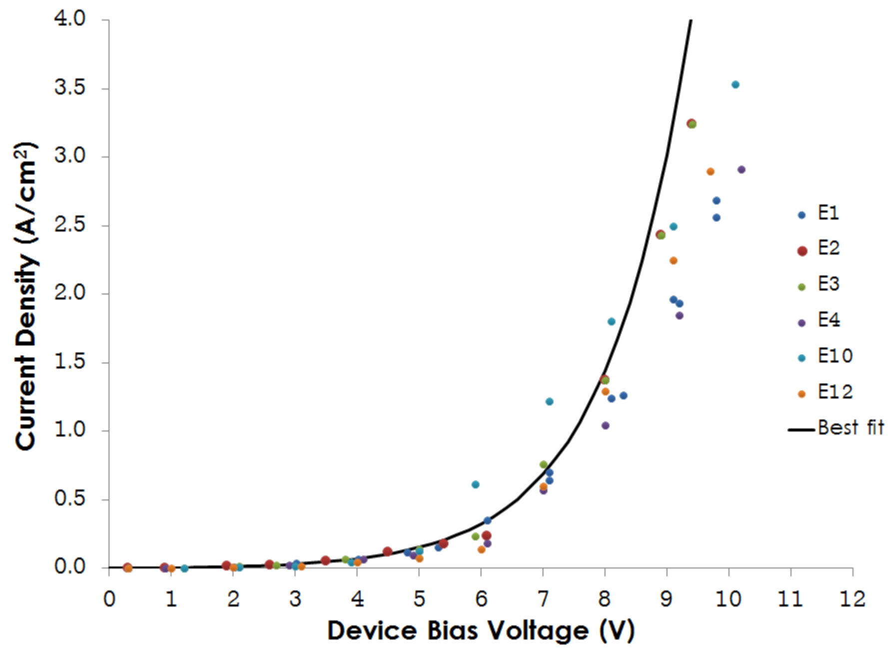


(a) Devices annealed at 400 °C **(b)** Devices annealed at 700 °C

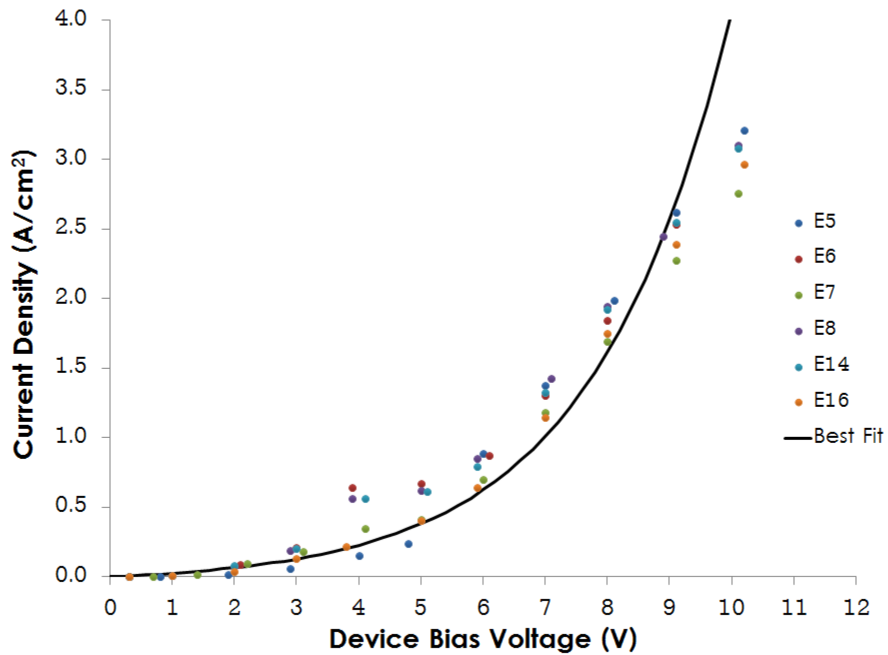
Figure 4.2: Log-linear plots of forward current density J vs forward bias voltage V. The segmentation of the behaviour into a low voltage regime $V < 2$V and a "medium" voltage regime $V > 2$ V can be clearly seen. As discussed in the text this is consistent with other reported nanocrystalline silicon LEDs. The best-fit slopes of the log-linear J vs V curves were used to extract the ideality factors η.

Anneal Temperature (°C)	J_s (A/cm^2)	η_{LV} (dimensionless)	η_{HV} (dimensionless)	Φ_B (V)	R^2 (dimensionless)
400	0.0029	15.0	50.7	0.55	0.970
700	0.0437	38.5	189.8	0.48	0.907

Table 4.1: Best-fit results for diode equation parameters for both 400 °C- and 700 °C-annealed devices. η_{HV} is the ideality factor for forward-bias voltage $V > 2$ V (i.e. the regime of nomal operation). The low forward bias regime < 2 V required a different ideality factor η_{LV} to give a good fit as is consistent with silicon nanocrystalline LEDs.



(a) Devices annealed at 400 °C.



(b) Devices annealed at 700 °C. Note the pronounced kink at $V \approx 4$ V in the J vs V curves for devices 6, 8, and 14. This deviation represents non-Schottky behaviour.

Figure 4.3: Current-voltage (IV curve data) for devices annealed in vacuum. Superimposed on the data are the best-fit curves to the diode equation, obtained from the log-linear plots of Figure 4.2. The fit parameters are given in Table 4.1. The deviation of the fit from the data at high forward currents is due to the increased device series resistance due to device heating.

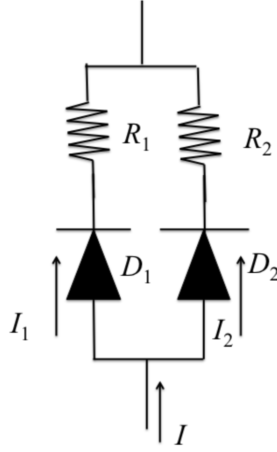


Figure 4.4: Two diode model for silicon Schottky LED devices. This model is suggested by the two straight-line regions of the log-linear JV plots of Figure 4.2. Diode D_1 corresponds to the high-η behaviour in the region with $V > 2$ V and diode D_2 is an additional shunt (i.e. parallel) path for current and corresponds to the lower η fit in the region $V < 2$ V. The series resistance values R_1 and R_2 are included to make the model more general, but they are negligible in our case ($< 1\ \Omega$) and reduced the correlation coefficients of the fits when included.

log (J) vs V curves in the low-voltage (i.e. < 2 V) and medium voltage (i.e. > 2 V) values of J_s and η were extracted. These values are reported in Table 4.1 along with the correlation coefficient R^2 for the fits (> 0.9 in each case). Note that the value of J_s in the "low voltage" region is reported in Table 4.3 as it is important for the reverse-bias characteristics but plays no significant role in forward-bias operation in the normal operating regime with $V > 2$ V.

The DC JV curves in the forward direction were fitted to the standard diode equation for a forward-biased diode eq. 2.16. The standard procedure was followed (the term -1 is normally dropped as it is negligible in comparison with the exponential term except for very small values of reverse bias). Taking the natural logarithm of equation 2.16 we obtain

$$\ln(J) = \left(\frac{eV}{\eta kT}\right) + \ln(J_s) \tag{4.1}$$

this equation has the standard linear form $y = mx + b$ with slope

$$m = \frac{e}{\eta kT} \tag{4.2}$$

and y-intercept

$$b = \ln(J_s) \tag{4.3}$$

Thus, least-squares fitting of a straight line to a plot of ln (J) vs V in a region where it is linear can be used to extract diode equation parameters J_s and η. From the value of J_s the junction barrier height can then be obtained using eq. 2.17.

4.1.1 Two-Diode Model

Inspection of the log-linear JV curves for the devices (see Figure 4.2) reveals two linear regions with a transition at around 2 V forward bias. Each linear region can be fit to yield separate values of J_s and η. These are tabulated in Table 4.1. These two regions taken together correspond to a circuit model consisting of two parallel diodes (this is shown schematically in 4.4).The results of the fitting to the two-diode composite model of Figure 4.4 are given in Table 4.1 for the groups of devices annealed at 400 °C and 700 °C, respectively.

The two-component curve fit reveals much smaller values of J_s of the order of 10−4 A/cm^2 for the low voltage region compared with the values of J_s of the order of 10^{-3} A/cm^2. In the context of the two parallel diode model, these data have a simple interpretation in terms of device cross-sectional area. While real silicon LEDs based on this process would be micron scale in lateral cross-section, with the dimensions defined by lithographic masking (recall that the process used to create buried luminescent nanocrystals in this work is fully compatible with standard CMOS processing), these devices were fabricated on 1 cm × 1 cm dies as broad-area emitters. There is some inhomogeneity observed across the device with certain regions emitting more light than others — although overall the device's luminescence is fairly uniform. It is likely that while the majority of the implanted silicon layer is crystalline, some regions (of the order of 1% of the cross-sectional area) are non-luminescent due to process variations. These non-luminescing regions are essentially resistive, damaged silicon and therefore will exhibit Schottky-like curves with small ideality factors. They only represent a small fraction of the total cross-sectional area of the device which reduces their effective value of J_s. As the forward voltage across the device is increased, these non-light-emitting

diodes start conducting but carry relatively low current until the forward bias exceeds the knee voltage. Once the forward voltage exceeds ~ 2 V voltage the high-ideality factor, light-emitting regions of the chip begin to strongly conduct and carry the majority of the current. Once this voltage is exceeded, the light-emitting diodes begin to strongly conduct and carry the majority of the current. Note that in addition to the metal-porous silicon Schottky LEDs reported by Maruska *et al.* [27] and Dimitrov [26], Halliday *et al.* reported very similar behaviour (e.g. distinct low- and high-current regimes with different ideality factors [19]) for their broad-area polyaniline devies.. This model would also apply to their broad-area, pollyaniline top-electrode devices. Table 4.2 summarizes results reported by various groups for similar silicon Schottky devices.

Model for Large Ideality Factors η

The results of the fitting of the Schottky LEDs to the diode equation are very large ideality factors (see Table 4.1. Large ideality factors ($\eta \sim 5$) are seen in other luminescent devices such as GaN based diodes [28] and very large values ($\eta > 10$) are also commonly observed in LEDs based on nanocrystalline silicon [27] [26]. For a nanocrystalline silicon device of the type we have fabricated, the large ideality factors can be explained in the context of a model used by Maruska *et al.* [27] in the context of porous silicon LEDs, and originally developed by Card and Rhoderick [47]. This model is based upon a 2-layer picture in which the bulk crystalline silicon is overlaid by an "interphase" layer of damaged or modified (e.g. annealed and nanocrystallized) silicon. The model gives the following formula for the ideality factor η of a 2-layer device of this type:

$$\eta = 1 + \frac{\delta \epsilon_{Si}}{W \epsilon_{ncL}} + \frac{\delta e D_s}{\epsilon_{ncL}} \epsilon_0 \tag{4.4}$$

where D_s is the area density of surface states per unit energy (units: $\mathrm{m}^{-2} \cdot \mathrm{V}^{-1}$), W is the width of the semiocnductor space charge region, ϵ_{Si} is the relative permittivity (i.e. the dielectric constant) of crystalline silicon (= 11.7) and ϵ_{ncL} is the relative permittivity of the nanocrystalline region (estimated to be $\epsilon_{ncL} \approx 10$ due to the slightly lower density of the nanoporous nanocrystalline region relative to the bulk silicon). δ is the thickness of the nanocrystalline region and thus $\delta \approx 2\sqrt{2} \times \Omega_R = 2\sqrt{2} \times 28$ nm ≈ 80 nm for our devices.

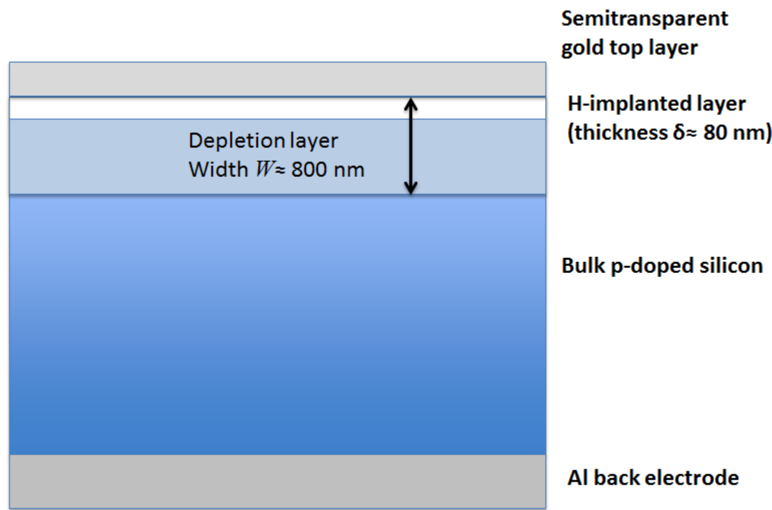


Figure 4.5: Device schematic showing nanocrystalline H-implanted layer (thickness $\delta = 80$ nm) as well as the depletion layer (of width $W \approx 800$ nm at neutral bias due to the built-in potential). Note that the depletion layer width $W >> \delta$ even at neutral bias.

This model is shown schematically in Figure 4.5. Note that the depletion width $W >> \delta$. Figure 4.6 shows variation of the ideality factor as a function of the surface density of defect states. Large ideality factors such as those observed for the devices described in this thesis are consistent with surface defect state densities of the order of 10^{14} cm$^{-2} \cdot$ V^{-1}.

Deviations from the Model for 700 °C Annealed Devices

As with the EL characteristics, the greatest effect on the devices' electrical behaviour resulted from the temperature of the anneal. The 700 °C-annealed devices exhibited significantly higher ideality factors than the 400 °C-annealed devices. In addition, some of the devices (namely, devices 6, 8, and 14) annealed at 700 °C exhibited a pronounced kink under forward bias ˜2V below the turn-on voltage. This is readily apparent in Figure 4.3b. The origin of this is unclear.

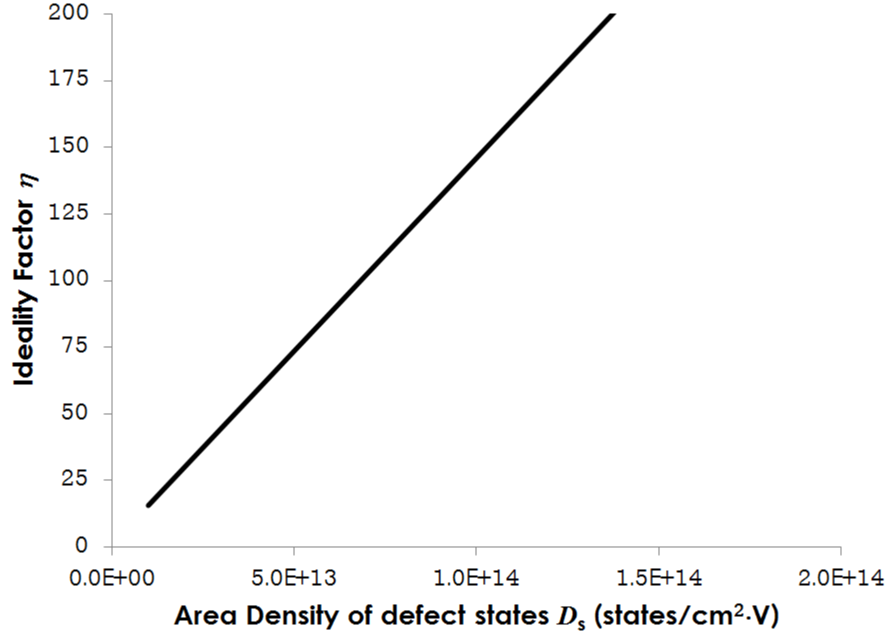


Figure 4.6: Variation of ideality factor as a function of the density of defect states in the nanocrystalline region. The straight line is a plot of equation 4.4 with the following parameters: $\delta = 80$ nm, $W = 800$ nm, $\epsilon_{Si} = 11.7$, $\epsilon_{ncL} \approx 10$, $e = 1.602 \times 10^{-19}$ C, and $\epsilon_0 = 8.85 \times 10^{-12}$ F/m.

Group	Device Area (cm^2)	R_{series} (Ω)	J_s (A/cm^2)	η	Φ_B (V)	Device Type
Maruska [27]	0.05	500	No value given	8.4	0.80*	ITO on porous Si
Dimitrov [26]	No value given	100	No value given	14	0.67	metal on p-doped Si
Halliday [19]	2	1600	3×10^{-7}	1.3	0.80	polyaniline on n-doped Si
Moloi** [25]	0.03	0	3.7×10^{-4}	1.9	0.69	gold on p-doped Si

Table 4.2: Results of electrical characterization of comparable silicon devices. *Note that Maruska *et al.* do not explicitly show how their claimed barrier height of 0.80 eV was measured. **Note that Moloi *et al.* did not fabricate LEDs.

4.1.2 Reverse Bias J vs V Curve Analysis

As with the forward bias data, there is a significant qualitative difference between the reverse bias data for the devices annealed at 400 °C and those annealed at 700 °C, namely the 700 °C-annealed devices exhibit strong reverse breakdown at around -7V reverse bias while the 400 °C annealed devices exhibit no such breakdown up to -20 V reverse bias. While a simple inspection of the diode equation would suggest a reverse current density equal to $-J_s$, in reality reverse bias operation is more complicated because of the possibility of reverse breakdown. There are two mechanisms commonly responsible for reverse breakdown: Zener breakdown due to field-induced ionization and avalanche breakdown due to collisional ionization. The model of Hurkx *et al.* is used to fit the reverse breakdown characteristics for both groups of diodes. The Hurkx model contains 7 parameters and thus requires a multi-parameter fit. Fitting to the Hurkx model was constrained by the use of values of J_s obtained from the low-voltage portion of the forward characteristics. Values of the Hurkx parameters p and V_{int} were obtained independently from capacitance-voltage (CV) profiling measurements carried out using a prototype setup developed by Himanshu Rai. This system is described in more detail in Appendix B. Good fits were obtained in both cases and the reverse currents are shown in figures 4.7 and 4.8. Note that the Hurkx model is comprehensive and is capable of modelling both reverse breakdown in 700 °C annealed devices as well as the lack of a reverse breakdown in the 400 °C devices.

4.2 Emission Spectra of Silicon LEDs

The silicon LEDs fabricated were effective visible light emitters, visible to the naked eye in a darkened room. The spectra were remarkably consistent from device to device; however, as a group the high temperature annealed devices exhibited much better emission as can be seen from comparing figures 3.4a and 3.4b. All of the devices annealed at 400 °C emit at relatively low intensities (around 200 Ocean Optics Spectrometer counts but constant for the entire set of spectral measurements) whereas the high-temperature devices were much higher: between 400 to 500 units on the same scale except for device 8 which was anomalously dim, probably

Parameter	400 °C: Fit A (Lower Bound)	400 °C: Fit B (Upper Bound)	700 °C: Fit C
p (dimensionless)	0.7	0.7	0.7
V_{int} (V)	1.5	1.5	1.5
F_{mbr} ($\times 10^6$ V/m)	0.5	7	2.5
V_{br} (V)	-100	-100	-5.25
c_{bbt} (A/V)	2	2	2
c_{SRH} ($\times 10^{12}$ $m^{-3}s^{-1}$)	2×10^6	2×10^6	2×10^6
J_s (A/cm^2)	0.0001	0.0001	0.0006
$R_{effective}$ (Ω)	1.5	1.5	1.5
Temperature (K)	300	300	300

Table 4.3: Results of fitting model of Hurkx *et al.* to reverse bias region including breakdown. Note that the values of J_s used were those obtained from the "low-voltage" portion of the log-linear forward-bias JV fits (see Figure 4.2)in order to ensure continuity as the device crosses from forward to reverse bias.

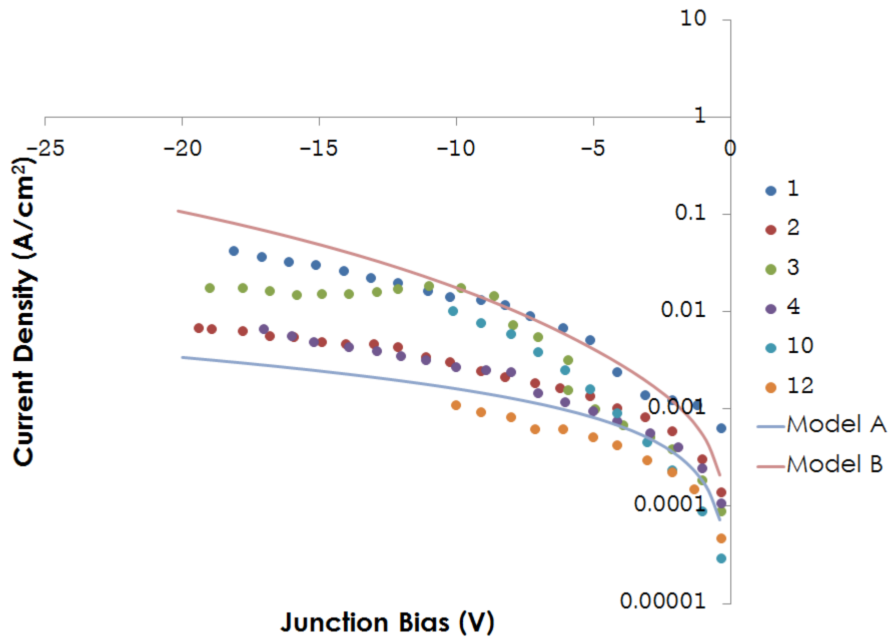


Figure 4.7: Curve fit model of Hurkx *et al.* to reverse breakdown region for devices annealed at 400 °C. Note the absence of reverse breakdown.

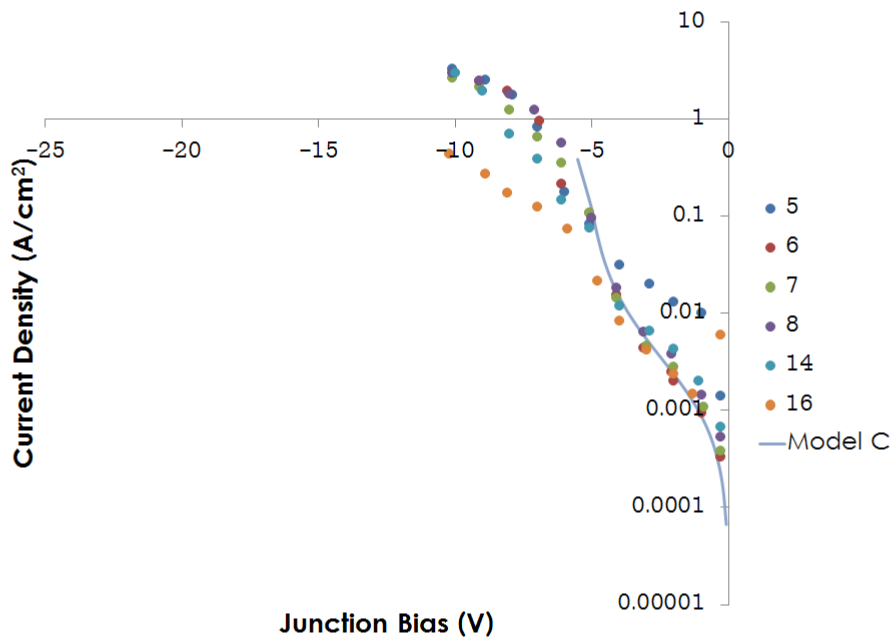


Figure 4.8: Curve fit to model of Hurkx *et al.* to 700 °C annealed devices. The reverse breakdown is well-represented by the model chosen.

due to a bad contact or other manufacturing flaw.

The peak emission wavelength of the emission spectra is around 650 nm and the spectra are roughly 100 nm wide. The light from these devices is broadband and appears yellow-orange to the eye. These emission spectra are consistent with spectra seen from various forms of silicon nanocrystals sometimes in the presence of oxide interfaces. When detector counts are plotted vs wavelength the spectra appear slightly skewed toward longer wavelengths; however, this is an artifact and when the spectra are re-plotted versus photon energy $\hbar\omega$ they are very close to Gaussian curves.

Solid state light emitters often exhibit Gaussian-type profiles for intensity vs frequency. This is because very narrow-band individual light emitters (nanocrystals in our case) find themselves in a local environment which exhibits some randomness and causes a random shift of these narrow band emitters. A single isolated light emitter will normally have an emisson spectrum characterized by a Lorentzian curve with a very narrow line width inversely proportional to the radiative decay lifetime.

$$L(\nu) = \frac{1}{(\nu - \nu_0)^2 + \Gamma^2} \tag{4.5}$$

Where ν is the frequency, ν_0 is the frequency corresponding to the energy difference between ground and excited states in the nanocrystal and Γ is the radiative decay rate. This Lorentzian is characteristic of atomic-like light emitters in which radiative decay can be rapid. Our model for the nanocrystalline buried layer is an ensemble of Lorentzian emitters with randomly distributed center frequency ν_0.

The total spectrum seen from an ensemble of such emitters randomly shifted by their local environment would be a Gaussian (describing that local randomness) convolved with the individual narrow-band Lorentzians. In the case of extreme broadening such as that due to a highly disordered solid state matrix such as that of our amorphized silicon layer the Gaussian is so much broader than the individual Lorentzians that they may be taken to be represented by delta functions that we may simply fit the spectra to a Gaussian. This is referred to as a regime of strong inhomogeneous spectral line broadening [48].

Figure 4.9 shows Gaussian curve fits to graphs of detector counts vs photon energy in eV. It can be seen that the Gaussians described all of the data very well confirming the hypothesis

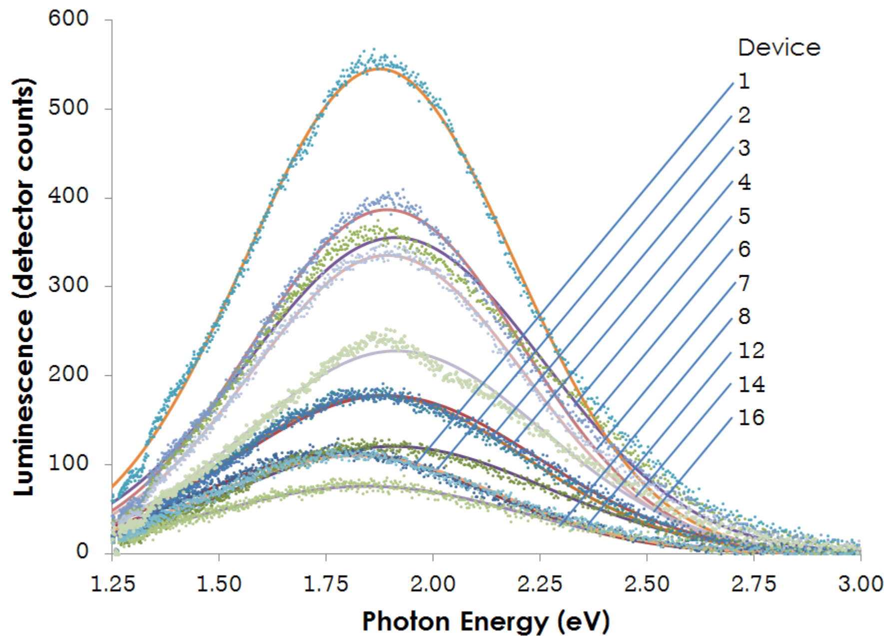


Figure 4.9: Graph of luminescense plotted versus photon energy in eV. Gaussian fits have been superimposed on the experimental data. High values of r^2 confirm the appropriateness of the gaussian model which corresponds to an ensemble of narrow-emitting centers inhomogeneously broadened by their local environment. The r^2 values are given in Table 4.4.

of strong inhomogeneous broadening. The mean peak photon energy was approximately 1.8 eV corresponding to a wavelength of 670 nm. Proot *et al.* [12] determined that silicon nanocrystals of diameter $D \approx 3.3$ nm emit light at this energy. When oxidation is taken into account, it is found to have an effect on nanoparticles of diameters smaller than 3 nm [17], but not particles such as those produced for this work.

4.3 Influence of Annealing

4.3.1 Higher Annealing Temperatures Lead to Greater Luminescence

The most striking observation of this work is the strong increase in the light emission of the high temperature annealed silicon LEDs relative to the lower temperature anneals (see Figure

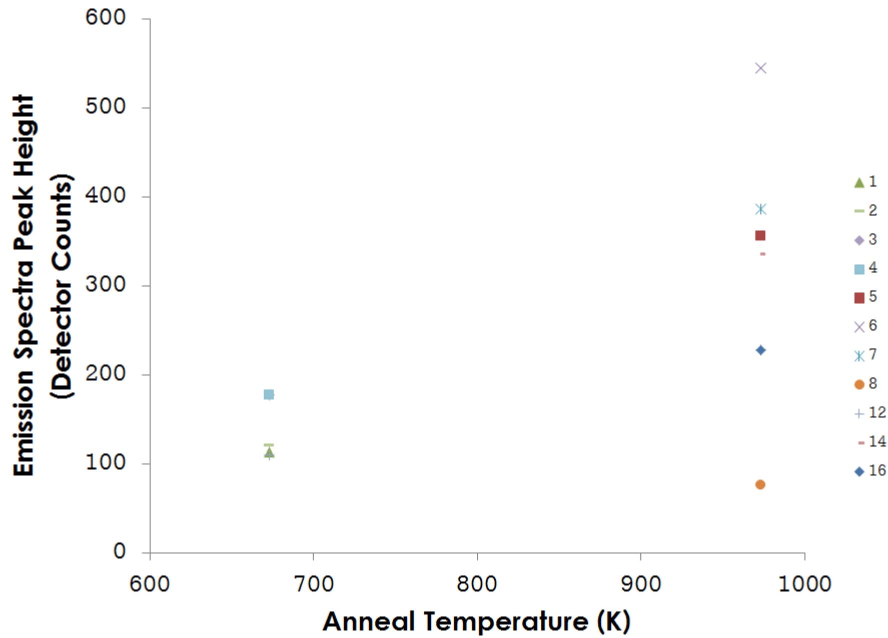


Figure 4.10: The effect of anneal temperature on electroluminescence. Note that these peak heights are taken from the Gaussian fits to the raw data.

4.10). This is an important discovery for future fabrication of silicon photonic devices of this type. In general, high temperature processing techniques involve both temperature and time and to some extent, these two parameters may be traded off against one another. However, because of the exponential dependence on temperature of chemical activation processes, an increase in temperature is generally much more significant than an increase in time.

4.3.2 Correlation with Reverse Breakdown

Note that in addition to being brighter than the 400 °C devices, the 700 °C devices also exhibited reverse breakdown at -7V onset. While we were able to fit the reverse breakdown using the model of Hurkx *et al.*, the connection with nanocrystal emission, if any, is less clear. This is in contrast with the forward bias case, where the large ideality factor clearly correlates with strong emission and the model of a wide defect-rich luminescent nanocrystalline layer [27].

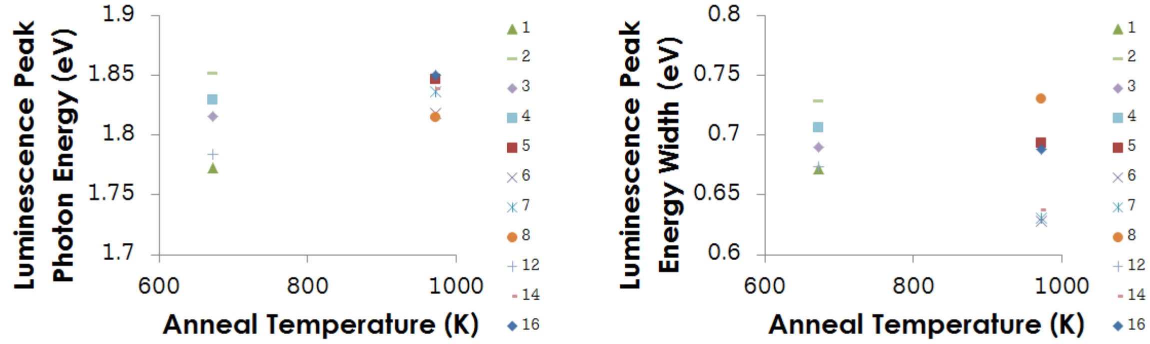
4.3.3 Correlation with Kink in Forward Bias J vs V Curve

As noted above, several of the devices annealed at 700 °C (devices 6, 8, and 14) exhibited a pronounced kink feature in the forward bias region of the JV curve at a forward bias voltage between 4 and 5 V. The striking nature of this feature prompted speculation as to whether it correlated with increased light emission. However, no such correlation was observed. Inspection of Table 4.4 makes this clear. Device 6 had the greatest emission (545 counts), device 8 had anomalously low emission power (76 counts), probably due to a fabrication yield issue, and device 14 was of average emission strength for the 700 °C-annealed group. Thus, there is no direct correlation between the kink's presence and EL: the devices with the most pronounced kinks, 6 and 8, are the devices with the greatest and the least emission powers.

4.3.4 Variation of Peak Photon Emission Energy with Processing Parameters

The peak photon energy (in eV units) corresponding to the peak of the most common photon energy for the measured luminescence spectra of the silicon LEDs is plotted in Figure 4.11a as a function of the annealing temperature in kelvin. No strong trend is discernible, which is also evident from the spectra graphed in Figure 4.9. The small variations in peak position are apparently random and are negligible compared to the very broad width of the spectral curves. Figure 4.11b is a plot of the widths of the Gaussian curves fitted to the luminescence spectra. Note that the width has been taken to be twice the standard deviation. Again, no real trend is discernible from these data.

In our model of an ensemble of randomly distributed nanocrystals with differing local environments, the constancy of the fit parameters of the luminescence spectra suggest that the number density of the nanocrystals increases with annealing temperature, leading to better emission, but the distribution of sizes which is reflected in the Gaussian fit remains roughly constant with temperature. It does not depend strongly on annealing temperature.



(a) Luminescence peak position (in eV) plotted as a function of of annealing temperature (K).

(b) The width of the best-fit Gaussian peak to spectrum. The widths shown here are the FWHM.

Figure 4.11

Nanocrystallite Formation – Recrystallization from the Damaged Layer

There are a variety of methods for producing nanocrystals in solid-state materials. One of the most important of these is the production of nanocrystals in an initially non-crystalline layer by an annealing process. The nanocrystals produced by this technique are commonly referred to by metallurgists as Type III Nanocrystals [49]. The growth of the nanocystalline phase is strongly influenced by the annealing temperature. Lu *et al.* [50] summarize a variety of data and show results from He *et al.* [51] found a silicon grain size 7.0 nm with an annealing temperature $T_{melt}/2$ for silicon nanocrystal size recrystallized from an amorphous melt.

As discussed previously, and as illustrated in Figure 4.12, the high fluence hydrogen ion implantation used for this work caused significant lattice damage in the implanted region. In addition, the use of hydrogen made the situation more complicated because of the tendency of the implanted hydrogen to accumulate and diffuse out during the annealing process, leaving behind nanocavities. For the ion implant parameters chosen, this diffusion is known to leave behind permanent nanometer-scale cavities in the implanted, damaged region. These cavities are surrounded by silicon nanocrystals randomly bonded together [52] [6].

4.3.5 Physics of Annealed Amorphized Silicon

The formation of nanocrystals from the amorphized ion-implanted layer during annealing is a thermally driven process of diffusion and nucleation. Silicon atoms displaced from their

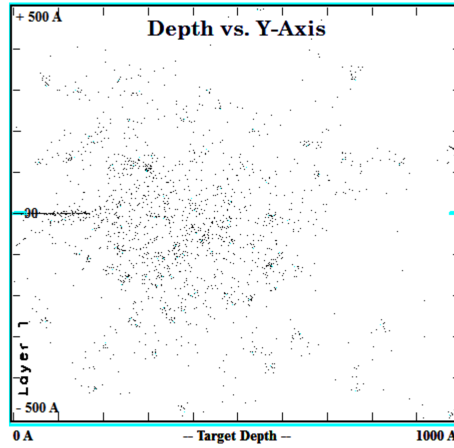


Figure 4.12: SRIM plot of simulated lattice damage associated with target atoms recoiling from collisions with 2.5 keV H^+ ions. Atom dislocations are shown as white. These collisions were simulated by SRIM 2013.

lattice positions by recoil cascades will nucleate and regrow silicon crystals. The size of the crystallites formed during recrystallization is determined by thermodynamic considerations. The steady state homogeneous rate for the nucleation of nanocrystallites is given by

$$r_{st} = r_0 e^{-\frac{Q}{RT}} e^{-\frac{L\Delta G_c}{RT}} \tag{4.6}$$

Where r_0 is a constant, L is the Locshmidt number, Q is the activation energy, ΔG_c is the critical energy required for a crystal of the critical size [50]. From an engineering point of view, it will be necessary to control the nanocrystal growth parameters e.g. temperature and time required to grow an ensemble of nanocrystals of a specified mean size. Thermodynamic modeling can give a general idea of the scaling rules to be expected in a process of nanocrystal growth from the amorphous phase produced by ion implantation. Indeed, He *et al.* [51] found that nanocrystals of the order of 7 nm in diameter were formed when annealing amorphized silicon took place at a temperature T equal to half the melting temperature. The data of He *et al.* is a bit sparse but the order of magniture of the size of the nanocrystals is consistent with the size of nanocrystals which would give rise to the 670 nm luminescence we observe if quantum confinement is the mechanism for the increased photon emission energy above the bandgap and also the enhanced radiative recombination efficiency relative conventional,

crystalline, indirect bandgap silicon.

While the general model of nanocrystals nucleated from heavily damaged silicon seems correct, the damaged layer produced by the PII H^+ implantation process is complicated by the presence of the hydrogen in the lattice. Hydrogen diffuses easily in silicon and at elevated temperatures is well known to cause blistering of the silicon as it nucleates in vacancies and builds up a gas pressure which exceeds the bulk modulus of the heated silicon. Most of the hydrogen is driven off during such an annealing process leaving behind a blistered, damaged layer [52]. The damaged layer is used in new semiconductor processing techniques such as "ion-cut" and "SMART CUT." It is also this blistered damaged layer which was likely responsible in the first hydrogen-implanted silicon luminescent devices reported by Liu *et al.* [6] which were the inspiration for this work.

4.3.6 Search for a Suitable Annealing Parameter

First principles modelling of nucleation and growth of nanocrystals is possible in principle [53], however there is difficulty in obtaining accurate parameters involved in making a first principles calculation. A different approach pioneered by metallurgists is to construct semi-empirical phenomenological parameters which capture the correct physics scaling of the annealing problem but do not require complete microscopic knowledge of all relevant processes. One such parameter is the Holloman-Jaffe parameter originally encountered in the tempering (e.g. high temperature heat treating) of steel.

The Hollomon-Jaffe Parameter

Annealing is the name commonly applied to thermal treatment of semiconductor wafers. Annealing has a long history in materials science dating back to metallurgical applications. It has long been known that high temperature can provide sufficient energy that atoms displaced from their normal crystal lattice position can move back to their preferred lattice positions and thereby lower their strain energy [54]. Thermal processing can also be used to produce nanocrystals in the solid solution [49]. This is emerging as a new technique for nanocrystal growth in situ. Such techniques have great potential in semiconductor processing as they provide a way to grow nanocrystals within an existing semiconductor device wafer.

Because of the exponential form of the Arrhenius equation for thermally driven processes, temperature increases in annealing are typically much more significant than increases in annealing time. Nonetheless time also plays a role and both temperature and time effects must be considered when annealing schemes are being optimized for material or device production. The Hollomon-Jaffe parameter one such attempt to predict the effect of an anneal based on its temperature and duration. It quantifies the assertion that increasing an anneal's temperature has the same effect as increasing its duration. The Arrhenius equation relates the rate of a reaction with the temperature at which it occurs:

$$k = Ae^{-\frac{E_A}{k_B T}} \tag{4.7}$$

in which k_R is the rate of the reaction involved, A is a constant, E_A is the reaction's activation energy, k_B is the Boltzmann Constant, and T is the temperature. Hollomon and Jaffe, while studying the effect of annealing on the hardness of steel, found in their case that E_A is not constant but was itself a function of time [55] [56]. Instead what remained constant was the value t_0, calculated as shown below:

$$t_0 = te^{-\frac{E_A}{k_B T}} \tag{4.8}$$

Rearranging this leads to the form:

$$\frac{E_A}{k_B} = T(\log t - \log t_0) \tag{4.9}$$

Then, defining $H_p \equiv \frac{E_A}{k_B}$ and $c \equiv -\log t_0$ gives the form of the Hollomon-Jaffe parameter:

$$H_p = T(c + \log(t)) \tag{4.10}$$

c is a constant specific to the material being annealed; because of logarithmic addition, it is essentially a scaling factor for t. For steel, values of c are typically in the range of 12-15. Note that as c is increased the influence of time becomes correspondingly less since in the Hollomon-Jaffe equation c is a fixed offset against which the $\log t$ parameter must compete.

Figure 4.14 shows the peak luminescence power for each device plotted as a function of the Hollomon-Jaffe parameter. The Hollomon Jaffe parameter was originally developed in

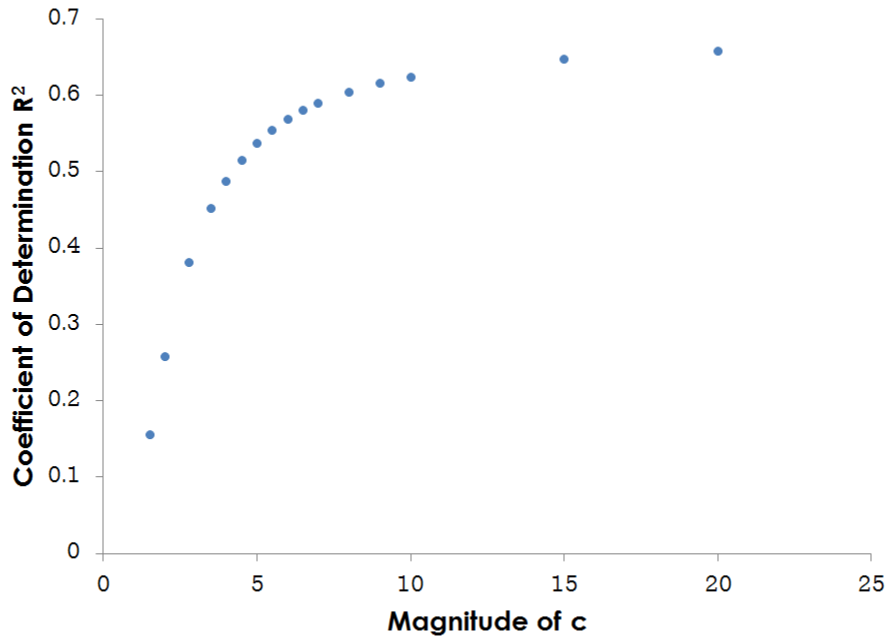


Figure 4.13: The influence of the constant c on the Hollomon Jaffe parameter.

the context of steel tempering and contains a constant parameter which must be a function of the material system used and will not a priori be the same for hydrogen in silicon as for steel (e.g. carbon in iron). To determine the best fit Hollomon-Jaffe constant for this system a straight line was fit to power vs Hollomon Jaffe parameter with the Hollomon-Jaffe constant c treated as a variable parameter. Figure 4.13 shows the correlation coefficient of this linear fit as a function of parameter c. The interpretation of this is that linear fits between light emission and Hollomon Jaffe parameter describe the experimental data relatively well for values of c greater than 8. Figure 4.14 shows the linear fit of light emission to Hollomon-Jaffe parameter when $c = 8$ was used.

The importance of the Hollomon-Jaffe parameter comes when this silicon light-emitting device fabrication process is brought to the silicon fab. The silicon photonics engineers will require some means of quantifying the influence of annealing on light emission power from silicon LEDs and predicting the effect of future anneals on ultimate light emission of the devices they make. The Hollomon-Jaffe may prove to be a useful tool in this context.

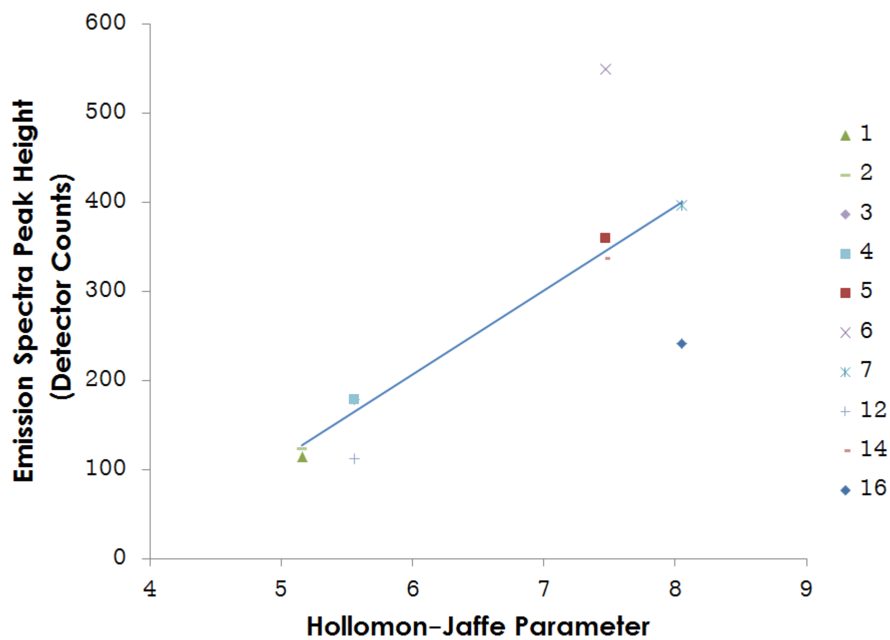


Figure 4.14: Dependence of electroluminescence peak height on the Hollomon-Jaffe parameter. The linear trend interpolated from these data is shown. A value of 8 was used for the constant c. Note that the low-lying outlier has been omitted. Note that these peak heights are taken from the Gaussian fits to the raw data.

Device	Peak Energy (eV)	Peak Wavelength (nm)	Peak Width FWHM (eV)	Peak Height (a.u.)	R^2 (dimensionless)
1	1.77	700	0.79	114	0.834
2	1.85	670	0.86	121	0.872
3	1.82	683	0.81	178	0.913
4	1.83	678	0.83	178	0.907
5	1.85	672	0.82	356	0.934
6	1.82	682	0.74	545	0.959
7	1.84	676	0.74	387	0.952
8	1.81	684	0.86	76	0.801
12	1.78	696	0.79	110	0.860
14	1.84	675	0.75	336	0.954
16	1.85	671	0.81	228	0.920

Table 4.4: Characteristics of the emission spectra and Gaussian fits to luminescence vs energy. Fauchet [17] determined that silicon nanocrystals of diameter $D \approx 3.3$ nm emit light with energy 1.85 eV.

Chapter 5

Conclusion

This thesis described the fabrication of bright, visible-light emitting silicon LEDs. Such devices could be candidate silicon photonic emitters for future optical interconnect applications. The devices were fabricated entirely in-house at the University of Saskatchewan using a custom PII system, an annealing furnace, and PVD system. The purpose of this thesis was to investigate the influence of annealing parameters on Schottky LED performance. The following itemized points were the main findings of this work:

- Devices annealed at 700 °C exhibited higher electroluminescence power by a factor of ~ 2, relative to those annealed at 400 °C.

- All devices annealed at 400 °C were lower-power emitters compared to those annealed at 700 °C.

- The luminescence spectrum peak photon emission wavelength and spectral width did not vary with annealing temperature or time. The peak energy of 1.84 eV corresponds with a silicon nanocrystal of size 3.3 nm.

- Aluminum gettering had no appreciable effect on either J-V curves or electroluminescence.

- One of the 700 °C-annealed devices (device 8) exhibited anomalously low emission power.

- All devices exhibited very high ideality factors consistent with a model of a broad, defect-rich silicon nanocrystalline layer.

- Devices annealed at 700 °C exhibited reverse breakdown at $V \approx -7$ V while devices annealed at 400 °C did not exhibit any reverse breakdown up to -20 V.
- Some of the 700 °C-annealed devices exhibited a "kink" in the forward bias characteristic.

To summarize, it was found that the annealing temperature had significant influence on the light emission from the silicon LEDs with higher temperatures leading to significantly brighter devices than those annealed at lower temperatures. All the silicon Schottky LEDs exhibited broad (spectral width $\sim$ 100 nm) visible light emission centered around a wavelength of 675 nm (corresponding to a photon energy of 1.84 eV). This is consistent with a luminescence mechanism due to buried silicon nanocrystals fabricated by a process of ion implantation induced local amorphization followed by annealing-driven recrystallization to form a nanocrystalline buried layer. This work has given hints as to the mechanisms at play in the operation of PII-fabricated silicon nanocrystal LEDs; further work will be required to increase the efficiency of the devices. It is important to note that the plasma ion implantation technique used to make the emitting layer is fully compatible with existing CMOS production techniques and could be integrated with existing chips.

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Appendix A

Model for Reverse Bias Including Breakdown

A.1 Device Modeling

Currents flow in the reverse bias direction despite the potential energy barrier because specific mechanisms allow electrons and holes to meet and recombine. Hurkx et al. [29] presented a model which incorporates three such mechanisms:

J_{SRH}: **Shockley Read Hall Recombination**
Crystal defects/trap states act as sites at which charge carriers are bound inside the barrier, and allowed to recombine.

J_{bbt} : **Band-to-band Tunneling**
Charge carriers quantum tunnel across the barrier and meet. This requires a relatively short depletion width.

J_{tat} : **Trap-assisted Tunneling**
Charge carriers get stuck in trap states which are near enough to the boundary to allow quantum tunneling further and through potential barrier.

$$J_d = \frac{(J_{bbt} + J_{tat})e^{-\mu_{av}} + (J_{SRH} + J_i)(1 + e^{-2\mu_{av}})/2}{1 - \frac{\mu_{av}}{1-\epsilon}(1 - e^{-2\mu_{av}})} \tag{A.1}$$

J_d is the total current density, and J_i is the simple exponential diode current density. ϵ is the proportionality constant between α_n and α_p: $\alpha_p = \epsilon\alpha_n$. It is not significant and is assigned a value of $\epsilon = \frac{1}{2}$.

$$J_{bbt} = c_{bbt} V_j \left(\frac{F_m}{F_o}\right)^{\frac{3}{2}} e^{-\frac{F_o}{F_m}} \tag{A.2}$$

c_{bbt} is an adjustable parameter associated with the magnitude of the band-to-band tunneling current. F_m is the maximum electric field across the junction and F_o is a effectively a constant proportional to the bandgap of the material: $F_o \sim E_g^{\frac{3}{2}} \approx 1.9 \times 10^7 V/cm$.

$$J_{SRH} = -qc_{SRH}(W - W_o) \tag{A.3}$$

q is the elementary charge, c_{SRH} is an adjustable parameter associated with Shockley Read Hall recombination. W_o is the width of the junction when no external voltage is applied to it, whereas W is the junction width as a function of the voltage applied to the junction.

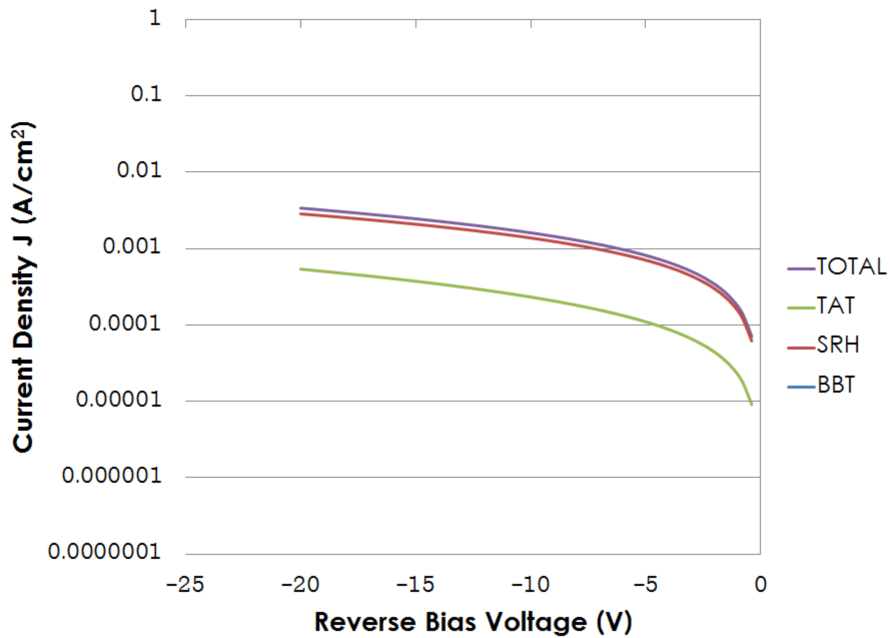


Figure A.1: Breakdown of the current contributions from the various reverse breakdown mechanisms accounted for in the model of Hurkx *et al.* using the parameters described as Model A in table 4.3. The current contribution due to band-to-band recombination is not shown because it is several orders of magnitude smaller than the other current densities. Note that for this fit, the current due to Shockley-Read-Hall recombination is roughly an order of magnitude greater than the current due to trap-assisted tunneling.

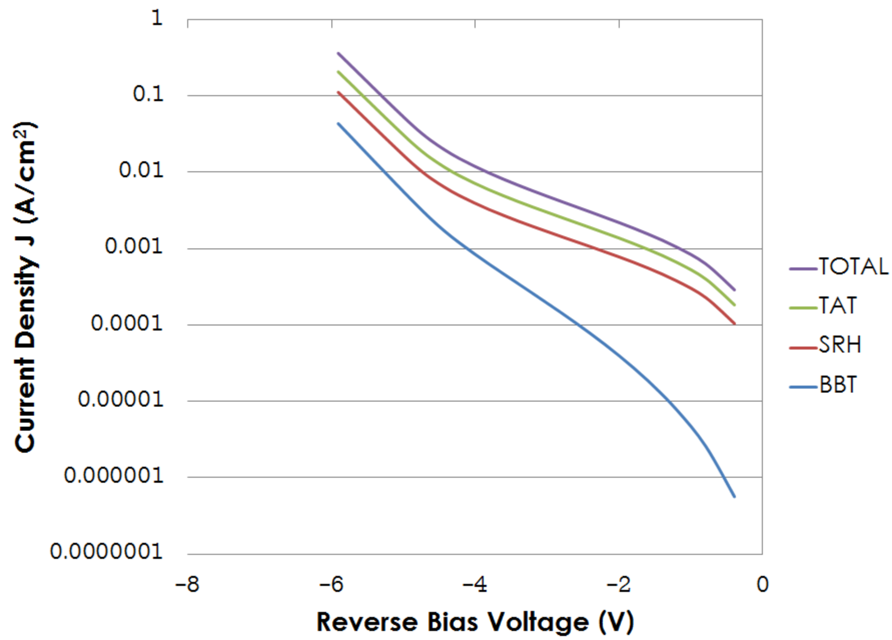


Figure A.2: Breakdown of the current contributions from the various reverse breakdown mechanisms accounted for in the model of Hurkx *et al.* using the parameters described as Model C in table 4.3. For the devices described by this model, the contribution due to trap-assisted tunneling has increased in relative intensity to surpass the current due to Shockley-Read-Hall recombination.

$$J_{tat} = -q\sqrt{3\pi}c_{SRH}W\frac{F_\Gamma}{|F_m|}\left[exp\left(\frac{F_m}{F_\Gamma}\right)^2 - exp\left(\frac{F_mW_o}{F_\Gamma W}\right)^2\right] \tag{A.4}$$

$$\mu_{av} = 0.3295\left(\frac{F_m}{F_{mbr}}\right)exp\left(b_n\frac{F_m - F_{mbr}}{F_mF_{mbr}}\right) \tag{A.5}$$

F_{mbr} is the magnitude of electric field across the junction at its highest value at the point of breakdown.

$$W = W_o\left(1 - \frac{V_j}{V_{int}}\right)^p \tag{A.6}$$

V_j is the voltage applied across the junction. V_{int} is the intercept voltage and, along with p, is a parameter which may be determined by C-V measurement. V_{br}, another parameter, is the junction's breakdown voltage.

$$F_m = F_{mbr}\left(\frac{V_{int} - V_j}{V_{int} - V_{br}}\right)^{1-p} \tag{A.7}$$

$$F_\Gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar} \tag{A.8}$$

m^* is the electron's effective mass in this material and is assumed to have a value of $m^* \approx 0.25m_e$.

A.2 Analysis of Models

A fitting was performed to produce device models which match the IV characteristics displayed by the LED devices fabricated for this work. Certain parameters, the saturation current J_{sat} and the intercept voltage V_{int}, were derived or estimated from device measurements. The resulting device models shown in Figures 4.7 and 4.8 approximate the features of the data closely.

c_{SRH} is relatively large: it is six orders of magnitude larger for these devices than for example devices modelled by Hurkx [29]. Such a large c_{SRH} indicates a high concentration of trap states at energies near the intrinsic Fermi level. This is consistent with a large concentration of defects caused by ion implantation.

Breakdowns of the models are shown in Figures A.1 and A.2. They show the contributions of currents due to the three recombination modes (band-to-band, trap-assisted tunneling, and Shockley-Read-Hall recombination). The breakdowns indicate that the current due to trap-assisted tunneling is the most prominent for the devices annealed at 700 °C. For the devices annealed at 400 °C the current due to Shockley-Read-Hall recombination is the most significant by an order of magnitude.

Appendix B

Depletion Capacitance

A diode junction that is not ”on” behaves similarly to a plate capacitor: it does not allow current to flow through it, but applying a voltage to it causes charge to accumulate in it. This is shown in figure B.1a which illustrates the existence of a depletion region of width W which is depleted of mobile charge carriers. An electric field E_d of average magnitude V/W exists in the depletion region due to the applied reverse-bias voltage V. This field acts to sweep mobile charge carriers out of the depletion region.

In the case of a junction, the two contacts act as the plates and are separated by the diode's depletion region. Since the depletion region's width W depends on the bias voltage, the junction's capacitance in turn is affected:

$$C = \frac{\epsilon A}{W(V)} \tag{B.1}$$

where ϵ is the permittivity of the junction material and A is the junction's surface area.

B.1 Measurement of the Depletion Capacitance

A diode's depletion capacitance is determined from measurements of the current response to a small AC voltage swing about a fixed DC offset. The parallel plate capacitor model only describes its behaviour below the diode's turn-on voltage. The relationship between the steady-state DC current and the AC current response is not simple. The circuit used to determine depletion capacitance thus has two tasks:

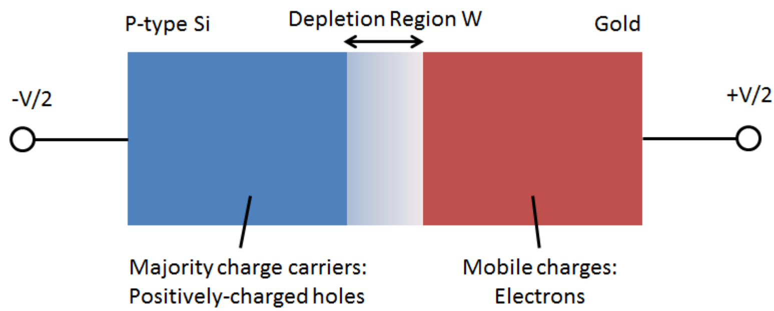
1. Establish an offset voltage

2. Supply a small AC signal to the device under test

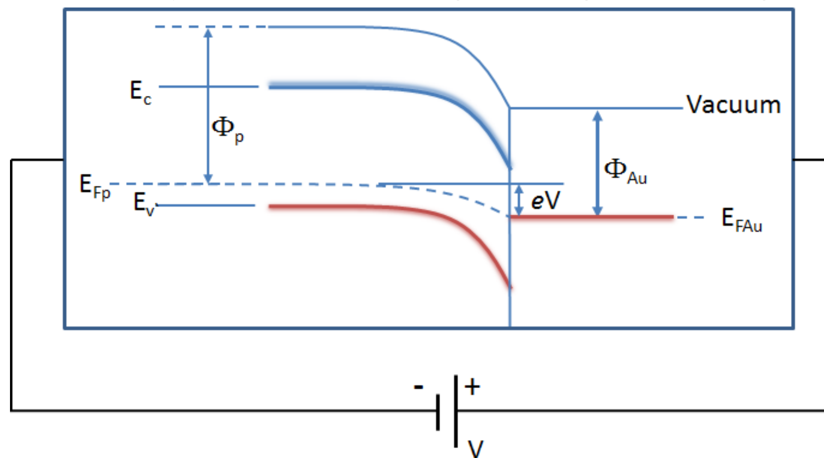
The DC and AC equivalent circuits are shown in (a) and (b) respecitvely. Meters are not shown. For simplicity's sake the coupling capacitor is not shown in either diagram. Its capacitance is chosen so as to have negligible reactance compared to the rest of the circuit in the AC regime, yet isolate the AC power supply in the DC regime by acting as an open switch.

B.1.1 The DC Behaviour

$R_1$and R_2act as a voltage divider providing a stable DC voltage offset to the device under test. The coupling capacitor acts as an open switch, isolating the AC power supply.



(a) A reverse-biased Schottky junction. Charge drawn to the junction by the applied voltage cannot traverse the carrier-depleted junction and instead further deplete the majority charge carriers, charging the two sides of the junction and extending the charge-depleted region.



(b)

Figure B.1

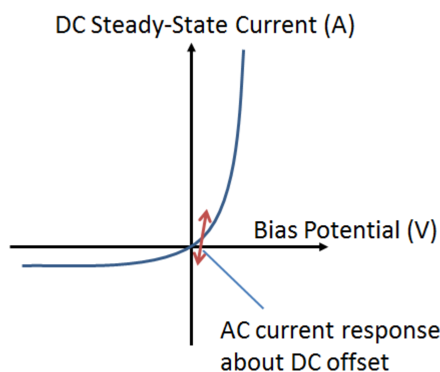


Figure B.2: The AC current swings about a fixed offset voltage. It is shown superimposed upon the steady-state DC IV curve.

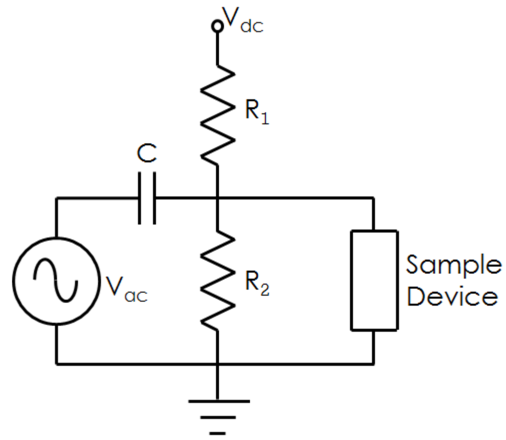


Figure B.3: The circuit used to measure depletion capacitance.

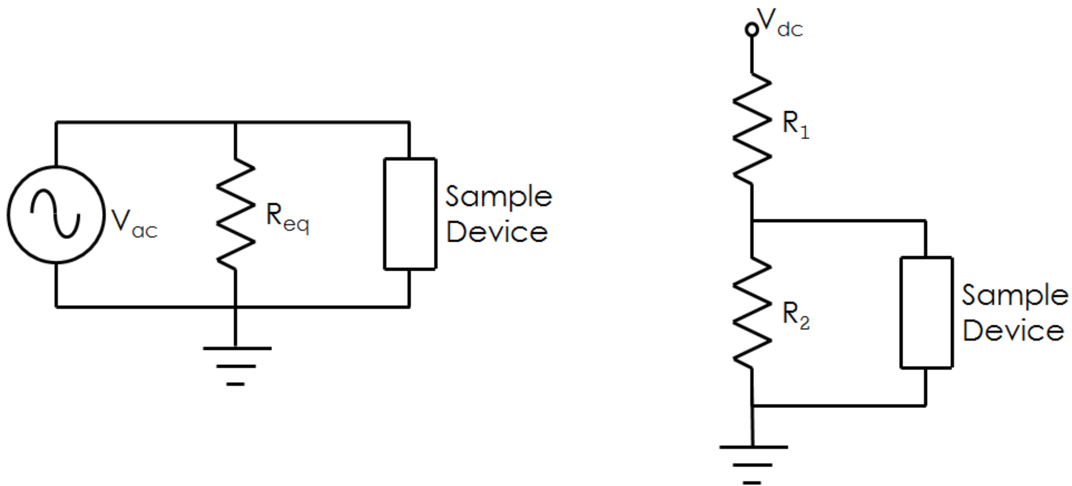


Figure B.4: The AC and DC equivalent circuits are shown on the left and right, respectively. The coupling capacitor is omitted.

B.1.2 The AC Behaviour

At the probe's operating frequencies the coupling capacitor's reactance has a small enough effect that it can be considered a closed switch, connecting $V_{ac}$to the device and R_{eq}, the AC equivalent resistance of $R_1$and R_2.

B.1.3 Choosing Components

V_{ac}should be small because a diode's current response's non-linear behaviour significantly distort the measurement otherwise.

B.1.4 Depletion Capacitance

When a Schottky diode is off it behaves like a parallel-plate capacitor: the boundaries of the depletion region act as the parallel plates where charge accumulates, whereas the depletion region itself acts as the dielectric separating them. Thus, the width of the depletion region is the separation distance of the capacitor. That width, however, varies with applied voltage; the region shrinks under forward bias until the conductive regions touch, the the barrier to DC current disappears, and the diode turns on. Under increasing reverse bias, the depletion region expands instead.

The capacitance of a capacitor, C_{cap}, depends on the separation distance, d_{cap}:

$$C_{cap} = \frac{\epsilon A_{cap}}{d_{cap}} \tag{B.2}$$

Where $A_{cap}$is the area of the plates. This relation holds for a diode's depletion capacitance, C_{dep}, with the complication that d_{dep}varies with applied voltage — and as a result, so does C_{dep}:

$$C_{dep}(V) = \frac{\epsilon A_{dep}}{d_{dep}(V)} \tag{B.3}$$

Ultimately, the capacitance's dependence on voltage is

$$C_{dep} = \sqrt{\frac{q\epsilon_s N_D}{2(V_{bi} - V - \frac{kT}{q})}} \tag{B.4}$$

Where the ϵ_s is the permittivity of the semiconductor, $N_D$is the is the concentration of donor atoms, and $V_{bi}$is the Schottky barrier potential. At constant temperature and uniform donor concentration profile, the relation simplifies to:

$$\frac{1}{C_{dep}^2} = \frac{2(V_{bi} - V - \frac{kT}{q})}{2(\epsilon_s N_D)} = kV \tag{B.5}$$

Non-Ideal Schottky Contacts

Deep levels/defect sites are physical positions at which electrons and holes may position themselves. Defect sites in or near the depletion region therefore allow more charge to accumulate, increasing the device's depletion capacitance.