STUDY OF SINGLE-EVENT EFFECTS ON DIGITAL SYSTEMS

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ABSTRACT

Microelectronic devices and systems have been extensively utilized in a variety of radiation environments, ranging from the low-earth orbit to the ground level. A high-energy particle from such an environment may cause voltage/current transients, thereby inducing Single Event Effect (SEE) errors in an Integrated Circuit (IC). Ever since the first SEE error was reported in 1975, this community has made tremendous progress in investigating the mechanisms of SEE and exploring radiation tolerant techniques. However, as the IC technology advances, the existing hardening techniques have been rendered less effective because of the reduced spacing and charge sharing between devices. The Semiconductor Industry Association (SIA) roadmap has identified radiation-induced soft errors as the major threat to the reliable operation of electronic systems in the future. In digital systems, hardening techniques of their core components, such as latches, logic, and clock network, need to be addressed.

Two single event tolerant latch designs taking advantage of feedback transistors are presented and evaluated in both single event resilience and overhead. These feedback transistors are turned OFF in the hold mode, thereby yielding a very large resistance. This, in turn, results in a larger feedback delay and higher single event tolerance. On the other hand, these extra transistors are turned ON when the cell is in the write mode. As a result, no significant write delay is introduced. Both designs demonstrate higher upset threshold and lower cross-section when compared to the reference cells.

Dynamic logic circuits have intrinsic single event issues in each stage of the operations. The worst case occurs when the output is evaluated logic high, where the pull-up networks are turned OFF. In this case, the circuit fails to recover the output by pulling the output up to the supply rail. A capacitor added to the feedback path increases the node capacitance of the output and the feedback delay, thereby increasing the single event critical charge. Another differential structure that has two differential inputs and outputs eliminates single event upset issues at the expense of an increased number of transistors.

Clock networks in advanced technology nodes may cause significant errors in an IC as the devices are more sensitive to single event strikes. Clock mesh is a widely used clocking scheme in a digital system. It was fabricated in a 28nm technology and evaluated through the use of heavy ions and laser irradiation experiments. Superior resistance to radiation strikes was demonstrated during these tests.

In addition to mitigating single event issues by using hardened designs, built-in current sensors can be used to detect single event induced currents in the n-well and, if implemented, subsequently execute fault correction actions. These sensors were simulated and fabricated in a 28nm CMOS process. Simulation, as well as, experimental results, substantiates the validity of this sensor design. This manifests itself as an alternative to existing hardening techniques.

In conclusion, this work investigates single event effects in digital systems, especially those in deep-submicron or advanced technology nodes. New hardened latch, dynamic logic, clock, and current sensor designs have been presented and evaluated. Through the use of these designs, the single event tolerance of a digital system can be achieved at the expense of varying overhead in terms of area, power, and delay.

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LIST OF ABBREVIATIONS

ASET	Analog Single Event Transient
BJT	Bipolar Junction Transistor
CPU	Central Processing Unit
CVSL	Cascode Voltage Switch Logic
DICE	Dual Interlocked Storage Cell
DSET	Digital Single Event Transient
ECC	Error Correction Code
FIT	Failure in Time
HI	Heavy Ion
IC	Integrated Circuit
LEO	Low Earth Orbit
LET	Linear Energy Transfer
MBU	Multiple Bit Upset
MCU	Multiple Cell Upset
NSREC	Nuclear Science and Space Radiation Effects Conference
RHBD	Radiation Hardened By Design
RVT	Regular Voltage Threshold
SBU	Single Bit Upset
SCU	Single Cell Upset
SE	Soft Error
SEE	Single Event Effect

SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SEL	Single Event Latch-up
SEGR	Single Event Gate Rupture
SIA	Semiconductor Industry Association
SOI	Silicon on Insulator
SPA	Single Photon Absorption
SRAM	Static Random-Access Memory
TAMU	Texas A & M University
TCAD	Technology Computer Aided Design
TDICE	Transistor DICE
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TPA	Two Photon Absorption

I. INTRODUCTION

1.1 Introduction

An Integrated Circuit (IC) may be exposed to potential radiation environments (e.g. low-earth orbits or flight altitude). A high-energy particle from such an environment may ionize the semiconductor material, thereby generating electron-hole pairs along its track. These excess carriers will then presumably be collected by the struck device, as well as its neighboring devices. This is usually followed by current/voltage transients at these affected nodes. Such effects are termed Single Event Effects (SEEs) [1][2]. Although some types of SEE errors can be recovered by writing new data to the inflicted circuit or repowering up the system, they still pose a serious reliability concern for micro-electronic circuits, specifically in regards to the highly reliable mission control system.

Binder et al. uncovered single event errors observed in satellites for the first time in history [3]. Cosmic ray particles bombarding the satellite ICs were identified by the authors as the source inducing these errors. Three years later, May and Woods reported alpha-particle-induced soft errors in terrestrial memory chips [4]. Avionics SEU errors had not been reported until Taber and Normand released their finding in 1992 [5]. These findings all validate the fact that single event errors may occur at different altitudes, ranging from the earth's surface to outer space. In 1980, the IEEE Nuclear and Space Radiation Effects Conference (NSREC) began to establish a special issue for researchers to collaborate and share their relevant work in the field of single event effects [6]. Ever since then, SEE has attracted attention from researchers and engineers; as a result, this community has made tremendous progress in investigating the mechanisms of SEE and exploring radiation tolerant techniques.

Although a variety of natural radiation environments exist, the majority of radiation sources are protons, neutrons, heavy ions, and alpha particles. They are also reproduced in laboratories with help of particle accelerators for the objective of SEE hardness assurance testing.

The proton is a particle carrying a positive charge. Its atomic number (i.e. the number of protons) is 1 and it deposits less charge per unit length when compared to heavy ions. However, in the natural space environments, it makes 85% of cosmic rays and 90-95% of solar particles [7]. The abundant presence of protons renders them a serious threat to space-borne microelectronic

circuits. Figure I-1 compares the flux of a number of particles in cosmic rays. As illustrated, the flux of protons denoted by the symbol H is ~10X as high as that of alpha particles denoted by the symbol He and at least two orders of magnitude higher than that of other heavy ions (denoted by the symbols C, O, etc.).

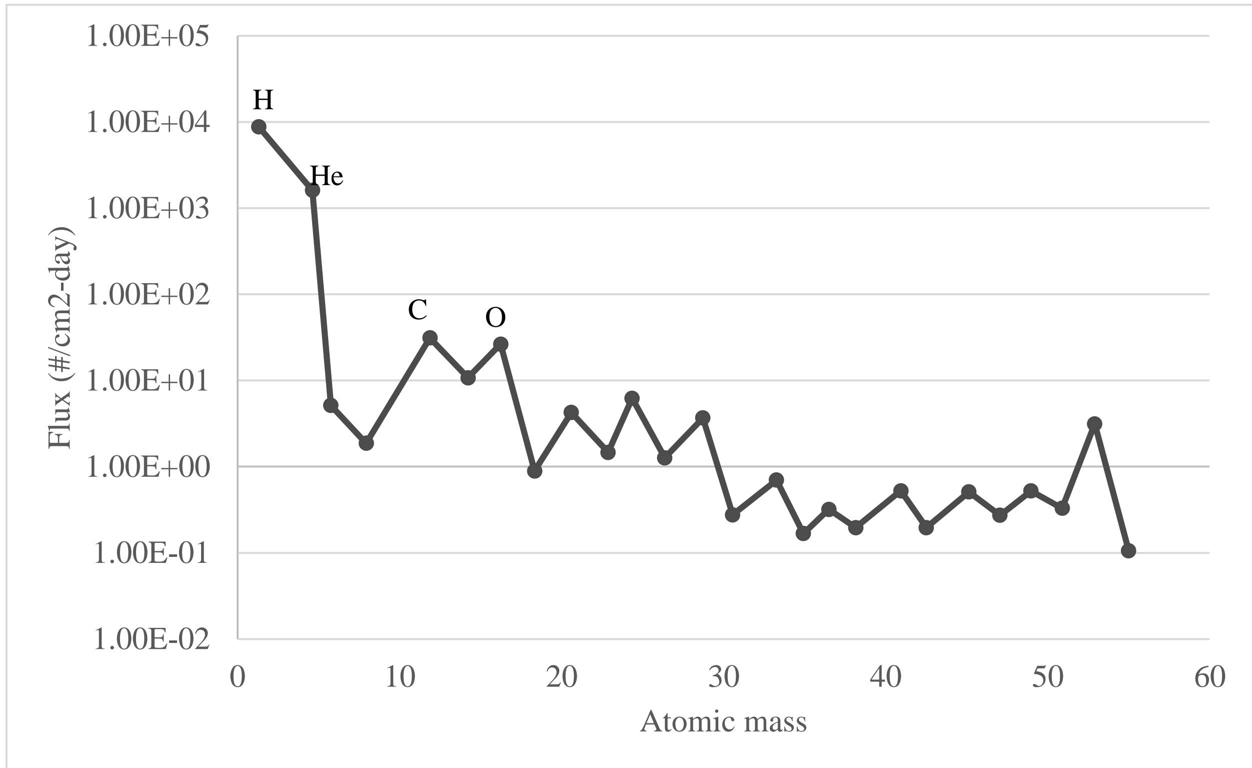

Figure I-1. Cosmic ray flux [1]

Unlike the proton, the neutron carries no charge. Therefore, it does not interact with silicon, nor does it generate electrons and holes in a direct manner. But for a highly energetic neutron, as it passes through the semiconductor material, it may generate secondary charged particles heavier than the neutron itself after colliding with a silicon nucleus. Neutrons manifest themselves as a major cosmic radiation source at terrestrial altitudes. Neutrons, as well as other cascade particles such as muons and pions, are created when cosmic rays enter the atmosphere [2]. Figure I-2 illustrates that an air shower of secondary particles is generated, followed by the proton colliding with molecules in the air. Recent discovery has identified neutron flux as being strongly dependent on key parameters such as altitude, latitude and longitude [8]. In addition, low energy thermal neutrons may be generated by the boron-doped phosphosilicate glass (BPSG) layers. In some cases, BPSG may even dominate the ground-level soft error rates [2].

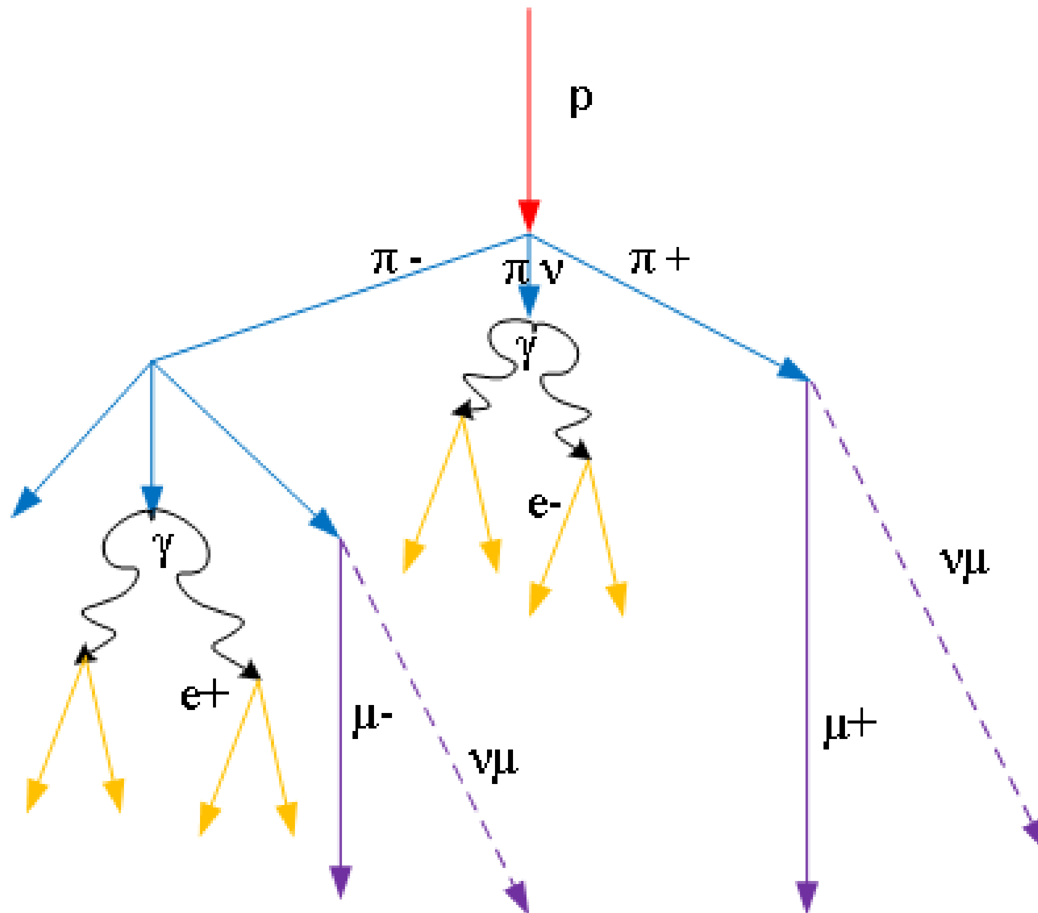

Figure I-2. An air shower [20]

The alpha particle is an ion identical to a helium nucleus, possessing two protons and two neutrons. Because there are no electrons in its structure, the alpha particle carries a net charge of +2. It constitutes 14% of cosmic rays and causes reliability issues for space-borne parts [7]. To exacerbate the problem, such particles may potentially be emitted by unpurified IC materials and packaging materials. For example, as Ziegler discerned, single event failures in Intel circuits were traced to a uranium mine [1].

Heavy ions are particles which have an atomic number larger than 1. Examples of heavy ions are alpha particles, Ne, Ar, Ni. etc. Although only 1% of cosmic rays are heavy ions, solar events may significantly increase the concentration of heavy ions. It may be increased to ~50% of the background heavy ion concentration due to a large solar event [7]. Because heavy ions can have a longer penetration depth and larger charge deposition, heavy ion facilities have been built around the world for SEE performance evaluation and parts screening.

1.2 Motivation

Radiation events in digital systems have the potential to affect both combinatorial and sequential systems. If an SEE error belongs to a logic circuit, it is referred to as a Single Event Transient (SET). On the other hand, if this error affects the logic state of a storage cell (i.e. a memory cell or a latch), it is referred to as a Single Event Upset (SEU).

These radiation-induced errors in an IC can be measured by a variety of merit figures. Two popular merit figures are FIT and cross-section. FIT stands for Failure In Time. 1 FIT is 1 error withiin 10^9 hours of device operation. The cross-section measures a device's area sensitive to single event errors as a function of Linear Energy Transfer (LET). It possesses two key parameters: upset LET threshold and saturation cross-section data. An ion with an LET larger than the upset LET threshold will induce a SEE error, whereas an ion with an LET smaller than the upset LET threshold will fail to cause a SEE error. As the ion LET increases, the cross-section increases until it is able to reach the saturation value.

The Semiconductor Industry Association (SIA) roadmap has identified soft errors induced by radiation strikes as the major threat to the reliable operation of electronic systems in the future [9]. In order to maintain an acceptable Soft Error Rate (SER) for an IC in deep-submicron technologies, efforts have been put forth to explore the new mechanisms of SET/SEU, to investigate the efficacy of hardening techniques, and to propose new SET/SEU-tolerant structures.

A considerably straightforward and obvious strategy is to shield the IC with Aluminum. This is a common practice for spacecrafts and satellites. Typical shielding for spacecrafts is in the range of 100-250 mils [1]. However, shielding has been found to be ineffective for neutrons. While concrete has proven to be a substitute material for the shielding of neutrons, as well as an effective material in the reduction of neutron-induced soft errors, this technique has proven problematic for certain applications [2]. Another straightforward approach is to purify fabrication materials by avoiding contamination and removing BPGSG during the IC fabrication and packaging process. As a consequence, SER from alpha particles and thermal neutrons may be significantly reduced.

From the perspective of ASIC designers and vendors, single-event mitigation techniques may be classified into three levels: the system level, the device (process) level, and the circuit

level. System-level approaches include, but are not limited to, Triple Modular Redundancy (TMR) and Error Checking Code (ECC) circuits. TMR takes advantage of three spatially redundant circuits of interest and a majority voter, which is used to compare all of these outputs. This technique is effective, barring instances in which 2+ circuits experience SEE errors at the same time. By physically spacing these three copies, the probability of causing errors within them may be simultaneously reduced. Another frequently used approach is ECC, which uses additional bits to check and possibly correct erroneous data. This technique is especially effective in protecting SRAM chips. Evidently, applying either ECC or TMR at the system level incurs heavy overhead in terms of power and/or area, but this may be the only available option if sensitive components must be utilized [10].

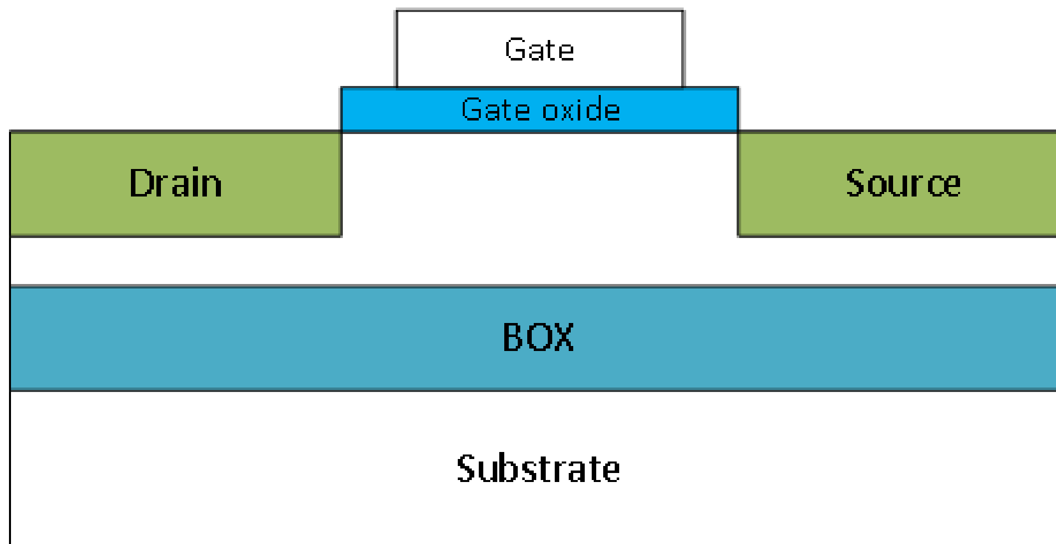

Figure I-3. The structure of a SOI technology

Device (process) level techniques involve IC fabrication changes. Silicon on insulator (SOI) is an SEE-tolerant process, as it reduces charge sharing between adjacent devices through the use of a thin layer composed of silicon oxide. This layer is referred to as BOX and acts as electrical insulator beneath transistors, isolating them from the substrate of the wafer, as displayed in Figure I-3. Irradiation experimental results collected by Rodbell et al. substantiated the fact that the single event tolerance of SOI is significantly higher than that of the bulk technology [11].

The remaining single event issues may be addressed by circuit-level techniques. These specific techniques do not require modification at either the process or technological level.

Rather, they rely on changes in the schematics or layouts of the design of interest. Calin et al. proposed Dual Interlocked storage CEll (DICE) [12], which is a structure that consists of eight transistors or four pairs of inverters, as displayed in Figure I-4. This design consists of four storage nodes, half of which are redundant. If one node is hit and experiences a positive or negative transient, the other nodes will help the latch remain in the correct state and eventually recover the hit node. As an alternative to a traditional D latch, DICE is immune to single node upsets and demonstrates unprecedented single event tolerance in old technology nodes.

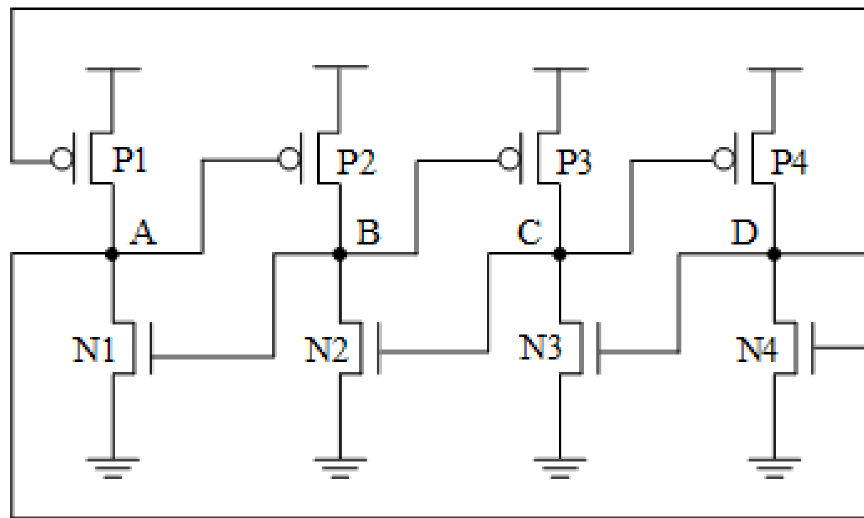

Figure I-4. The structure of DICE [12]

In addition to the changes in schematics, circuit-level techniques can be applied at the physical layout. Examples of layout-based techniques include spatially separating sensitive nodes, as well as placing high-density well/substrate contacts. As Amusan et al. pointed out, in a 130nm technology, if the spacing between adjacent devices increases from 0.18um to 0.9um for PMOS/NMOS, the charge shared by the passive PMOS (NMOS) device (i.e., non-hit device) decreases by 50% (17%). Separating DICE nodes has the potential to improve the single event tolerance [13].

However, as technology advances, newer processes lead to smaller spacing between devices, a smaller capacitance representing a logic value, a lower supply voltage, and smaller driving capabilities. All these modifications have rendered the aforementioned techniques less effective. For example, experimental results have demonstrated that DICE is only 20X, 5X, or 1.5X when compared to a regular DFF in advanced technology nodes [14][15][16]. Charge-sharing has been

found to cause multiple nodes in DICE to collect charge simultaneously and upset the latch. Simulation results presented in Figure I-5 illustrate that a charge as low as ~5 fC deposited at nodes A and B has the potential to induce an SEU error in a 45nm technology node [17]. All the 12 possible NMOS-PMOS pairs displayed sensitivity [18].

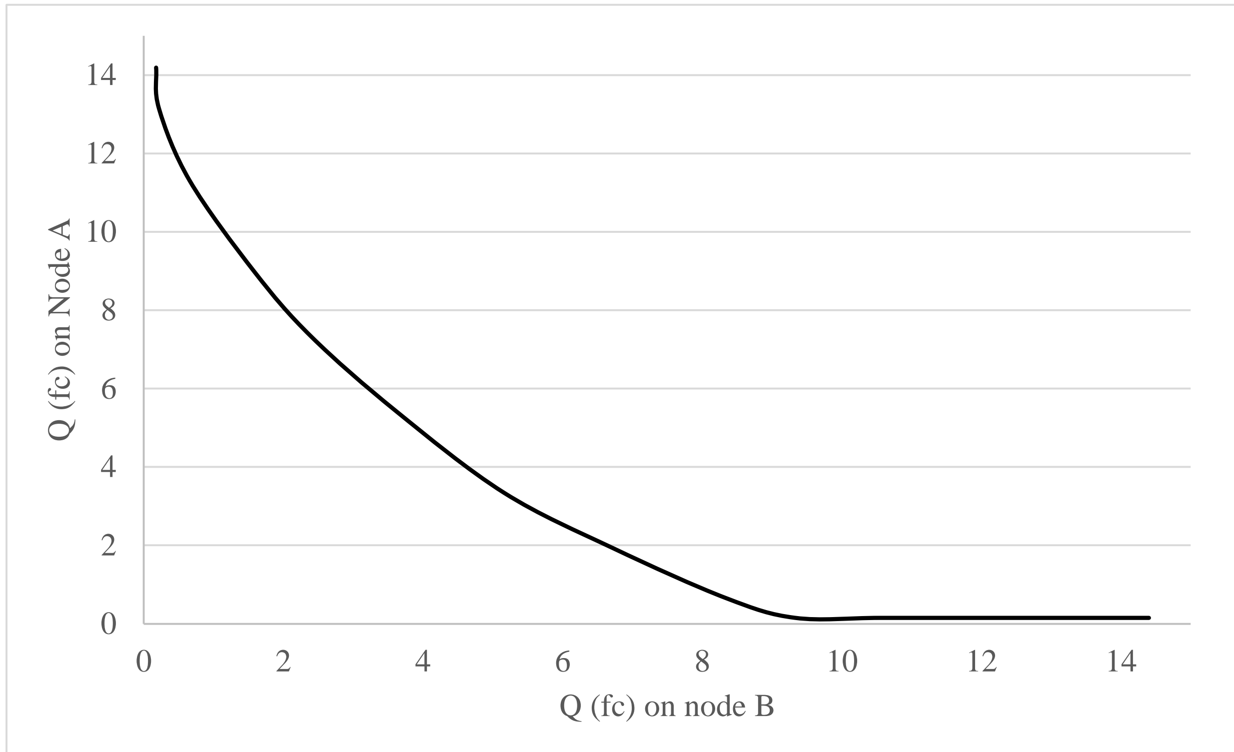

Figure I-5. The critical charge curve of double node charge collection [17]

In the report issued by International Technology Roadmap for Semiconductors (ITRS), SEU in SRAMs is regarded as a considerable challenge for process below 16nm for terrestrial applications [10]. This becomes a grave concern for high-speed applications. As SIA identified in 2009, SEE became the main reliability challenge for new technology processes. This organization also predicted that multiple-bit single event upset errors would be the predominant issue in 2016.

1.3 Objectives

The SET/SEU upset thresholds have been found to decrease with feature size. This is the case for both bulk and SOI technologies. Specifically, for bulk technologies below 250nm and SOI technologies below 90nm, IC devices become sensitive to alpha particles [10]. Not

surprisingly, even ASIC designers of commercial products must endure reliability issues caused by SEE errors. Therefore, hardening techniques pose critical design challenges and must be investigated and explored. In this thesis, I will propose RHBD designs through various techniques, which will be tested through the use of simulations and experimental data.

- RHBD flip-flop designs:

In digital systems with aggressive pipelines, the flip-flops may occupy a larger area than the combinational logic [19]. I will propose hardened flip-flop structures while maintaining area and/or power efficiency. All of these existing techniques outlined in previous sections, such as TMR or ECC, demonstrate excellent SEU performance. However, they are also associated with a severe performance penalty in terms of area and power. I have the objective of utilizing hardening techniques in order to reduce area and/or power, whilst simultaneously maintaining an adequate single event tolerance.

- RHBD dynamic logic designs:

Dynamic logic previously employed its applications in high-speed modules, such as advanced processor design and DSP architecture, yet the correspondingly high single event susceptibility when compared to static logic rendered it unfavorable in such applications. Considering the fact that logic errors will be comparable to SEU errors with device scaling, as researchers have indicated, my objective is to increase single event tolerance of the dynamic logic family.

- Hardened clock network:

As for a synchronous digital system, a global single-event resilient clock distribution network is the key to ensuring reliable operations. Thus, high performance global clock architecture is required in order to distribute clock signals across the die with near-zero skew, sharp edges and the optimal use of routing resources. Considering the fact that the most common approaches are the clock tree and clock mesh, any SET errors on these clock networks may cause a significant number of circuit failures. Hence, special attention must be paid to harden clock networks.

- Design verification:

All of the proposed designs will be verified through SPICE and/or TCAD simulations. Following the verification of their functionality, test chips containing these structures will be fabricated in bulk CMOS technology nodes. The test chips will then be experimentally tested using protons, heavy ions, pulsed lasers, and X-ray irradiation facilities. These experimental results will be examined to confirm the SET/SEU performance of these designs.

1.4 Thesis Overview

This thesis is based on the author's manuscripts published or still under review during the author's PhD study. All of the simulation and experimental results demonstrated in these manuscripts are assembled to show the author's work in the study of single event effects on digital systems. Each chapter begins with a brief summary, which touches on the relationship between the given chapter and the previous one. A brief conclusion ends each chapter. The organization and main contents of this thesis are summarized below.

Chapter 1 gives a very brief introduction to various radiation environments, single event effects, and existing hardening techniques. Charge sharing in new technologies have rendered existing techniques less effective, and thus, this chapter continues with the motivation to explore the new mechanisms and propose new techniques. The author then presents objectives stating that new hardened latches, dynamic logic circuits, and clock network designs will be investigated and tested using simulations and irradiation experiments.

Chapter 2 reviews the basic mechanisms of single event effects, including charge deposition and charge collection. Multiple node collection in deep-submicron and advanced technologies induces charge sharing between adjacent devices, thereby worsening the single event tolerance of the ICs. The physics are discussed for charge sharing in both NMOS and PMOS devices. Classifications of single event effects are outlined, which emphasize single event upsets and transient errors. Hardening approaches at the circuit-level, which are applied at the schematics and layout of the design of interest, are demonstrated. Some of these approaches are using time/space redundancy, adding well/substrate taps of high-density, and applying layout techniques to cancel charge, etc. Testing methodologies and major challenges of heavy ion and lasers arising with new processes and packaging options are presented at the end of this chapter.

Chapter 3 presents a manuscript regarding a hardened latch design based on the reference cell DICE. As discussed, DICE may upset if multiple storage nodes collect charge, and thus, DICE variants have been proposed to overcome this issue. One of the designs adds four extra transistors to the feedback loops of DICE. These extra transistors are turned ON only if the latch is in its write mode. Therefore, the feedback time is increased due to the resistance of these OFF transistors in the hold state. However, if these feedback transistors are hit or collect charge at the same time from a single ion hit, this modified structure remains unable to recover. In my design, four feedback transistors are added, two of which are PMOS transistors and the other two NMOS transistors. These PMOS (NMOS) feedback transistors are connected to PMOS (NMOS). Consequently, even if both of these feedback transistors are struck simultaneously, they fail to flip the state of DICE. Simulation and experimental results demonstrate that this design has a much higher upset threshold and lower cross-section.

Chapter 4 includes another manuscript, in which a Quatro variant is presented. This structure is based on Quatro, which has single node upset issues. By adding two feedback transistors, the proposed design is tolerant to single node upsets. Its single event performance was simulated and evaluated through heavy ion experiments. In the tested heavy ion LET range, the worst case was ~5X magnitude reduction in cross-section when the proposed design was compared with the original Quatro. Monte-Carlo simulations across process variations, corners, supply voltages, and temperatures were carried out as well.

Chapter 5 discusses two single event resilient dynamic logic designs. Traditional dynamic logic circuits have single event issues at each operating stage. The worst case occurs when the output is evaluated high during the evaluation phase. In this case, the pull-up network is turned OFF, so any high -> low flip at the output node cannot be recovered. One proposed design is to add a feedback capacitor across the static inverter. The single event tolerance of this design increases as a result of two occurrences: 1) the increased nodal capacitance, which results in a larger critical charge, and 2) the increased feedback time. The other design is a differential structure with two differential inputs and outputs. This design has no upset issues, as not all of the pull-up paths are cut-off. Therefore, the output nodes can be charged up to Vdd with no errors latched up.

Chapter 6 demonstrates the single event performance of various clock structures. A test chip containing several shift registers was fabricated in a 28nm bulk technology. Each shift register has a clock mesh, which distributes the global clock signal all over the flip-flop chains. All of these shift registers are connected as daisy chains through clock buffers. These two clock structures (clock mesh and daisy clock schemes) were tested using alpha particles, protons, heavy ions, and lasers. No burst errors were observed from the clock buffers in the cases of alpha particles, protons, and heavy ions below 10 MeV-cm^2/mg. This signifies the high tolerance of these clock networks. Errors with heavy ions of LET > 10 MeV-cm^2/mg were analyzed and found out to be induced by striking the daisy chain clock buffers.

Chapter 7 is associated with a built-in current sensor design and its experimental results in a 28nm technology node. Radiation-induced currents in the n-well are an important indicator for single event response. This is a result of striking a PMOS device in the n-well, which has the potential to result in well-collapse and correspondingly cause single event errors. This sensor is designed to detect n-well single-event transients (SETs) in an integrated circuit (IC). It was simulated and fabricated in a 28nm bulk CMOS technology. Laser experiments were conducted to confirm the validity of the proposed design, substantiating the fact that that this sensor can be utilized for advanced technologies.

This work is summarized with chapter 8, which is related to summaries and conclusions. Additionally, it outlines the contributions of this thesis and future directions for research.

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II. BACKGROUND

2.1 Single Node Charge Collection

Although the basic mechanisms of heavy-ion-induced single event effects are not exactly the same as those of proton-or-neutron-induced effects, two fundamental processes are always involved: charge deposition and charge collection [1][2]. Charge deposition refers to the process of depositing charge by the incident particle through direct or indirect ionization. Charge collection refers to the process of collecting the deposited charge by devices through either drift or diffusion.

As a charged heavy ion particle goes through an IC, its energy is transferred from the ion itself to the semiconductor material. Consequently, this material undergoes ionization. The resulting electrons and holes are generated in the shape of a cylinder along the ion's path. This is illustrated in Figure II-1. The initial charge track is usually modeled as a cylinder whose radius is 0.1 um. It is worth noting that the radius may be as large as 0.5 um for galactic cosmic ray particles [3]. Therefore, for deep submicron or more advanced technology nodes, where the spacing of inter-devices is in the range of nano-meters, an ion-induced charge track may be large enough for neighboring devices to collect charge.

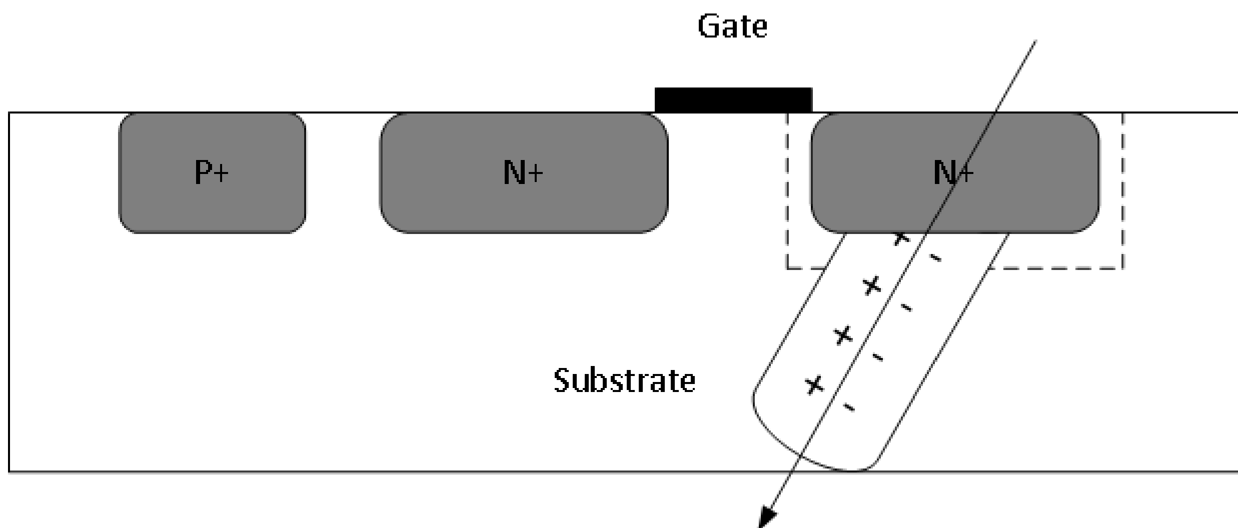


Figure II-1. The charge track for an NMOS hit by a charged particle

LET is defined as the energy loss per unit path length as the ion travels through the target material [1]. Figure II-2 displays such a curve for a 290-MeV Carbon ion traveling through high-density polyethylene. As illustrated in this figure, the LET is not a constant value. In fact, the LET increases as the ion travels deeper into the target material before reaching the Bragg peak, which occurs immediately before the incident ion comes to rest. After the Bragg peak has been surpassed, the LET drops until the particle comes to rest. Silicon is the most common target material because ICs are usually fabricated on silicon wafers. In this material, an LET of 100 MeV-cm^2/mg is roughly equivalent to a charge deposition of 1 pC/um. The effective LET is dependent on the incident angle; As the angle shifts from normal to grazing angles, the particle travels a longer distance and deposits more charge as a result. Therefore, the effective LET is larger for angled strikes than normal incident strikes.

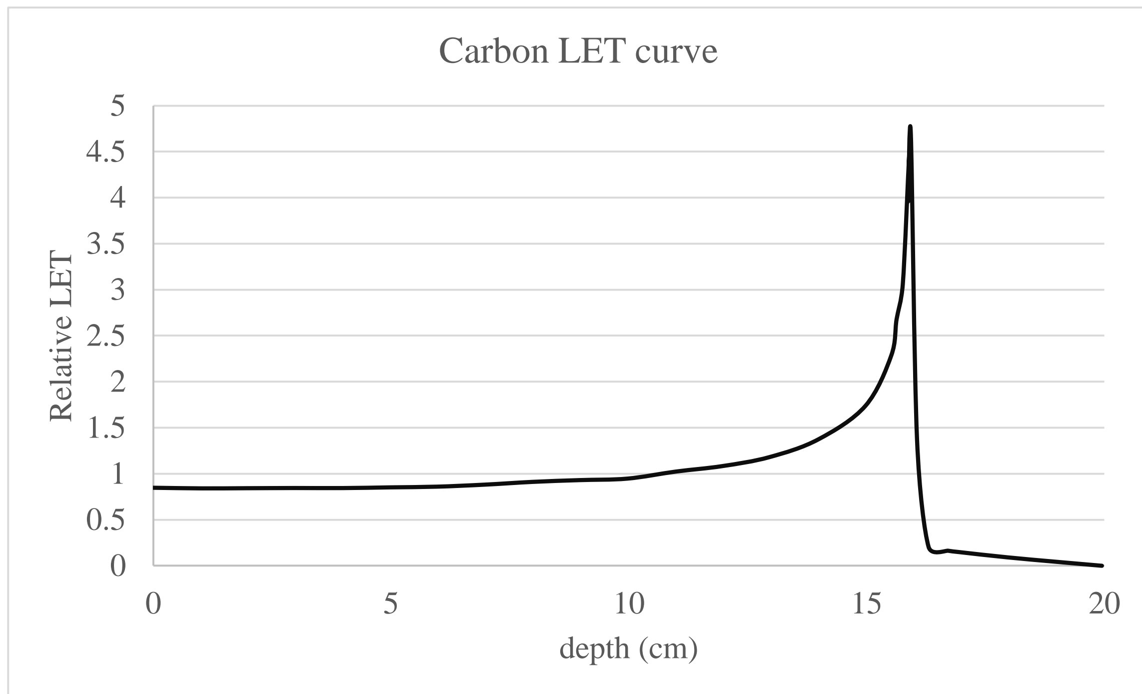


Figure II-2. The curve of LET as a function of penetration depth for a 290 MeV ion

Light particles, such as protons and neutrons, do not deposit charge through the process of directly ionizing silicon as heavy ions do. As a high-energy proton or neutron enters the semiconductor material, however, it may collide with a silicon nucleus and produce secondary particles (e.g., alpha or gamma particles). These particles deposit higher charge densities because

they are heavier than the incident particles [1]. As a result, they may still produce significant numbers of single event failures.

Moreover, the amount of deposited charge may also depend on ion energy and ion species. For instance, in advanced technologies, there were distinct differences in heavy ion experimental data for high-energy and low-energy particles. The authors concluded that these differences were caused by secondary particles during nuclear interactions in instances where lower LET ions would collide with silicon [5]. However, the authors also pointed out, for old technologies (1 to 0.5 um), ion energy does not make any significant differences in the IC's single event response [4].

After the electron and hole pairs are generated, both drift and diffusion may contribute to charge collection. The most sensitive regions are believed to be reverse-biased PN junctions [1]. Taking the NMOS device displayed in Figure II-1 as an example, it is evident that there is a strong electric field pointing towards the substrate in the vicinity of the depletion region, which is formed by the drain and the p-substrate. Furthermore, electrons in or near the depletion region will be swept into the drain node over a very short period of time. In the meantime, electrons nearby may diffuse to the depletion region and subsequently get collected through the electric field. A resulting transient at this drain node is demonstrated in Figure II-3. It is modeled as a double exponential function in order to simulate fault injection by a single event strike [6]. t_r is defined as the time constant for initially establishing the ion track, while t_f represents the collection time constant of the junction.

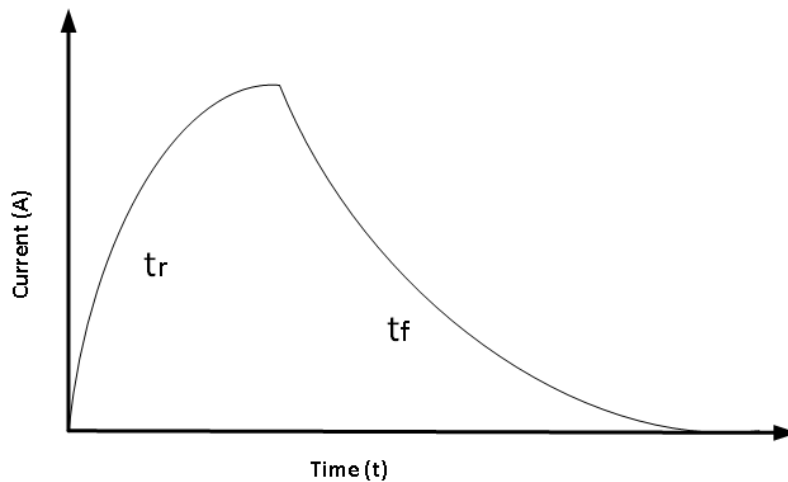


Figure II-3. The single event transient

The charge collection mechanism of a PMOS is similar to that of a NMOS. However, a NMOS collects more charge as compared to a PMOS. This phenomenon is explained as follows: Assume a particle with the same LET value strikes NMOS or PMOS with the same incidence angle, as illustrated in Figure II-4. Apparently, the amount of deposited charge is the same for both devices. However, in regards to the PMOS device, there are two depletion regions. One is formed by its drain and n-well, while the other is formed by the n-well and p-substrate. Although the former depletion region's high field helps to collect holes, the latter's field repels holes in the p-substrate because the filed is directed towards the p-substrate. The funnel shape is also limited by the n-well. Therefore, PMOS devices usually collect a smaller amount of charge when compared to their NMOS counterparts.

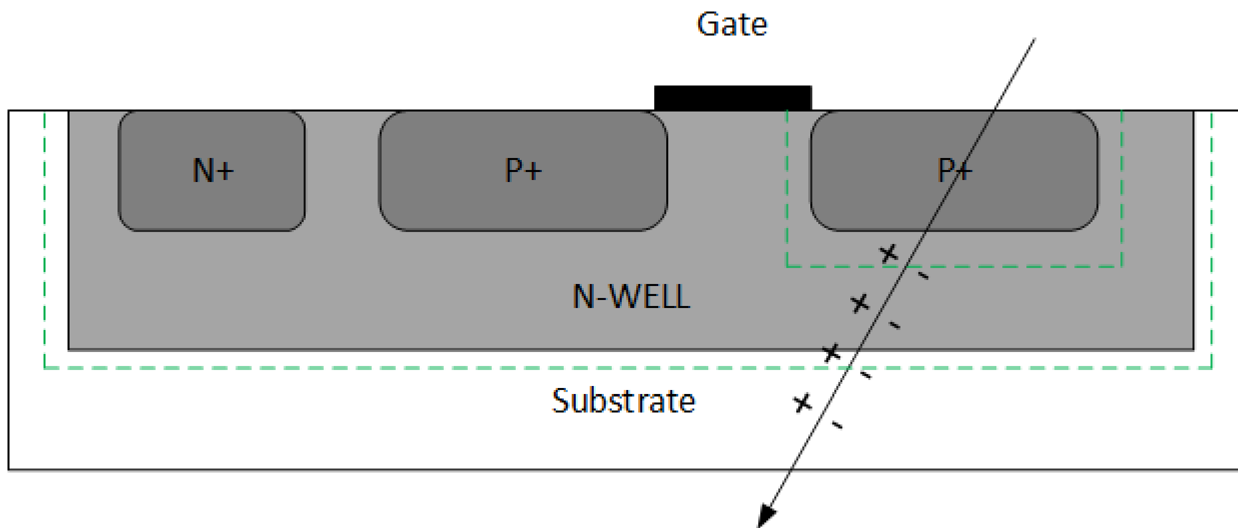


Figure II-4. The structure of a PMOS device indicating it collects less charge than NMOS

2.2 Multiple Node Charge Collection

As we move toward deep-submicron or nano-scale technologies, the IC susceptibility has been shown to increase with device scaling. The assumption that the deposited charge is predominantly collected by the struck node no longer holds true for these new technologies. The preeminent reason underlying this phenomenon is that multiple adjacent nodes may collect sufficient charge from a single ion hit as a result of decreased spacing between devices, which is termed charge sharing in this community. For example, normally incident particles were shown to induce upsets in multiple neighboring cells in static memory chips by Song et al. in 1988 [7].

Generally speaking, for NMOS devices, diffusion plays a significant role in charge sharing, while parasitic bipolar enhancement (PBE) contributes to an increase in collected charge for PMOS devices. Reducing the feature size decreases the base width and this, in turn, translates to a larger gain. As a result, PBE becomes more pronounced [1]. Figure II-5 shows the structure of these parasitic bipolar junction transistors (BJTs). They are formed by the source (emitter), drain (collector), and n-well (base). A particle striking PMOS may result in a high concentration of electrons in the N-well, immediately followed by holes collected by the drain. This causes a well potential drop in the n-well and may subsequently forward-bias the source/n-well junction, thereby turning on the parasitic BJT. Hence, the source terminal acts as an emitter and injects minority carriers (holes) into the n-well. Moreover, the parasitic bipolar transistor significantly increases the total charge collected by the neighboring node.

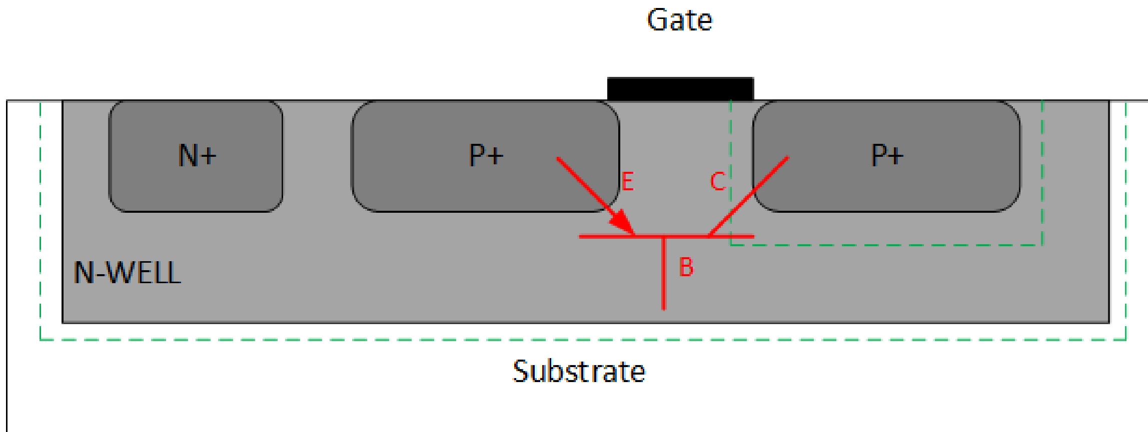


Figure II-5. The cross-sectional view of parasitic bipolar transistors

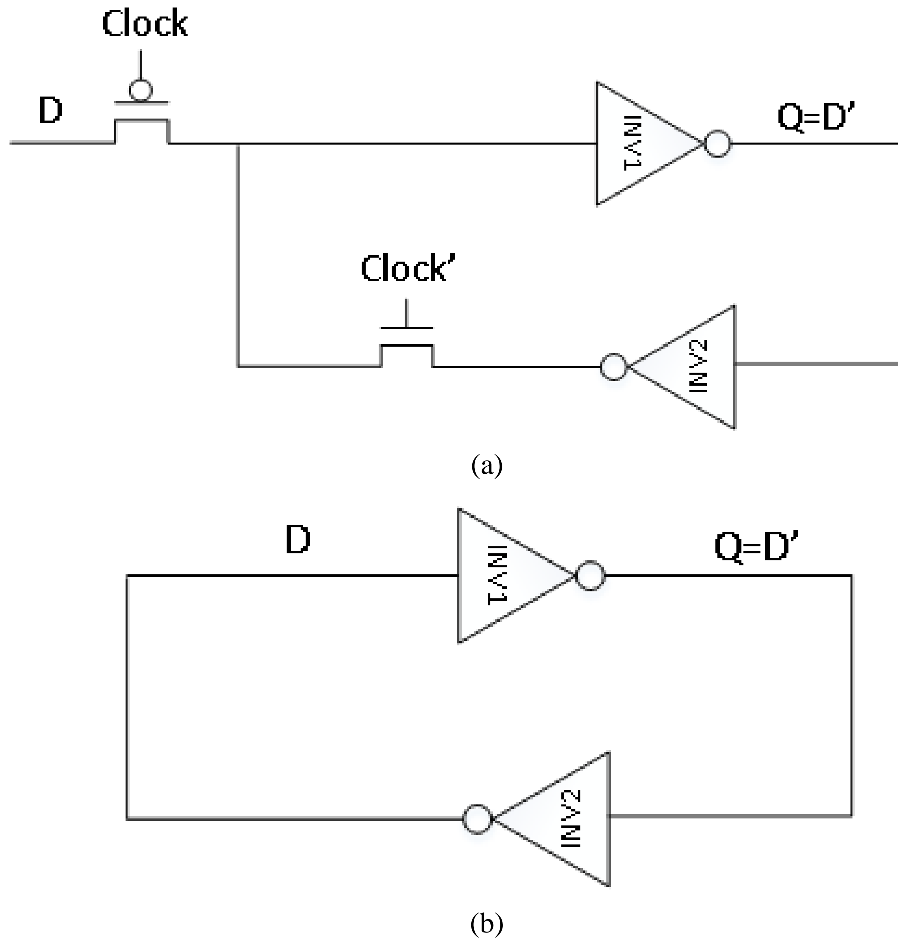
Ensuring the parasitic BJT in its OFF state is pivotal to annealing the PBE effect as much as possible. Considering the fact that the effective resistance between the strike location and the N-well contacts limits the current supplied from the contacts, adding more well contacts helps the n-well potential well to be maintained at Vdd.

2.3 Major Classifications of Single Event Effects

Radiation strikes have the potential to cause soft errors or permanent errors. The former refers to those non-destructive errors that do not cause any potential permanent system failures, while the latter refers to radiation-induced gate rupture, latchup, or burnout errors.

2.3.1 Single Event Upset (SEU)

Figure II-6 illustrates the structure of a typical D latch, which consists of two pass transistors and a pair of inverters with a positive feedback loop. Let's assume that D=H and CLOCK=H. If the D structure stays in the hold state, it can be simplified as Figure II-6 (b). The NMOS of INV1 and PMOS of INV2 are OFF, and hence, they are sensitive to radiation strikes. If a particle strikes the NMOS drain of INV1, for example, the resulting current may be large enough and exceed the restoring current provided by the PMOS transistor of INV1. The voltage perturbation at the struck node will then propagate to the opposite inverter (INV2) and probably cause an unintended state of change in the D latch. This is referred to as an SEU. SEUs also occur in SRAM cells, DRAM cells, and dynamic logic circuits.



(a)

(b)

Figure II-6. The structure of a traditional D latch (a) a traditional D latch; (b) a simplified D latch

2.3.2 Single Event Transient (SET)

A SET refers to a voltage or current transient in analog or digital circuits. They are called Analog SET (ASET) and Digital SET (DSET), respectively. Because of the fact that this thesis focuses on digital systems, only DSETs are discussed here.

The first DSET occurrence was reported by Diehl et al. back in 1987 [8]. Following that, new DSET effects have been observed as a result of technology scaling. Rossi reported multiple SETs (MSETs) at IRPS in 2005 [9]. His research attributed this to multiple node collection. In 2009, Albin re-evaluated the effect of charge sharing and indicated in this study charge sharing may result in beneficial effects, such as pulse quenching (i.e. shorter SET pulse widths) [10].

If logic circuit generating SETs are followed by a register-like storage element, they may be captured as an SEU error by this element. As the clock frequency increases, the probability of capturing such SETs correspondingly increases as well. Therefore, the SET-induced failure rate increases with the operating speed, and SETs may limit the maximum speed of the system [11]. Dodd et al. suggested that even alpha particles may significantly increase the SER rate in sub-100nm technologies [12]. Studies conducted by other researchers have also indicated that, in deep submicron technologies, DSETs will elicit a more grave concern [11].

2.3.3 Single Event Latchup (SEL)

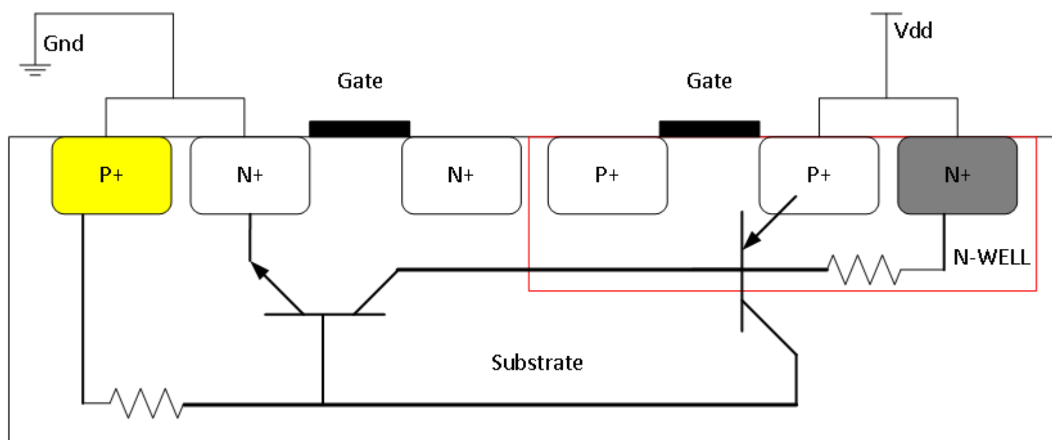


Figure II-7. The structure of the parasitic thyristor

In bulk CMOS technologies, an intrinsic thyristor is formed by a parasitic PNPN structure, in which a PNP and a NPN are stacked. If these thyristors are turned on, they may shorten the power

and ground rails, consequently destroying the chip. These thyristors may also be triggered by radiation strikes.

Figure II-7 displays these parasitic structures. The parasitic NPN transistor is formed by the source (emitter), p-substrate (base), and n-well (collector). Similarly, a parasitic PNP transistor is formed by the source (emitter), n-well (base), and p-substrate (collector).

2.3.4 Destructive Single Event Effects

Although the SEL may destroy the ICs, other destructive single event effects may occur as well, especially in the cases where high electric fields are present [1]. Thus, power devices are believed to be victims in most cases. One example of these destructive effects is single event gate rupture. This is because a single energetic-particle strike may cause the electric filed of the gate oxide exceeding the dielectric breakdown field strength [1].

2.4 SEE Tolerant Designs by Circuit-Level Mitigation Techniques

2.4.1 Time and/or Space Redundancy

Both logic and flip-flop circuits can be hardened using temporal and/or spatial redundancy techniques. A variety of time-redundant structures have been explored and evaluated. Nicolas et al. proposed an error detection structure, taking advantage of two latches followed by a comparator [13]. As illustrated in Figure II-8, the clocks of these two latches are not aligned. Instead, their clock signals have a time difference of δ, which determines the maximum SET pulse width (δ-Dsetup-Dhold). Dsetup and Dhold are setup time and hold time of the latch, respectively. Any SET pulse widths larger than δ will be captured by these two latches simultaneously, thus rendering them unable to be differentiated.

The comparator can be replaced by a guard gate [14]. As displayed in Figure II-9, it has four transistors connected in series. The output is taken from the node between the pull-up network and pull-down network. If both inputs are the same, the guard gate outputs their complement. Otherwise, this structure remains floating in the high impedance state.

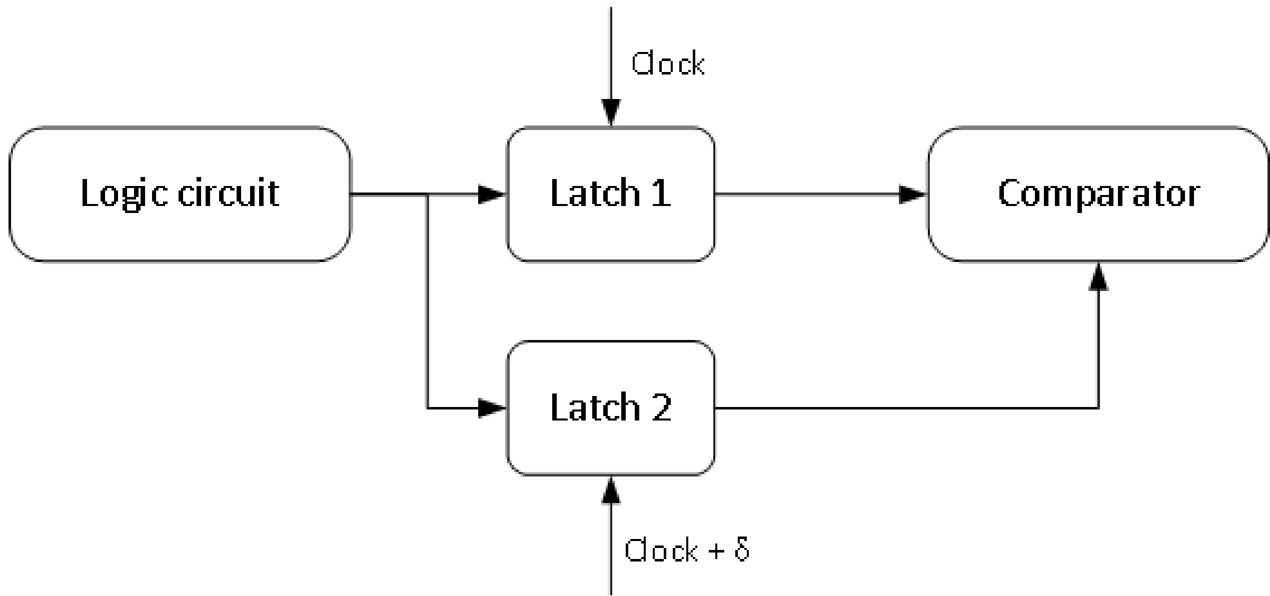


Figure II-8. The time-redundancy-based design [13]

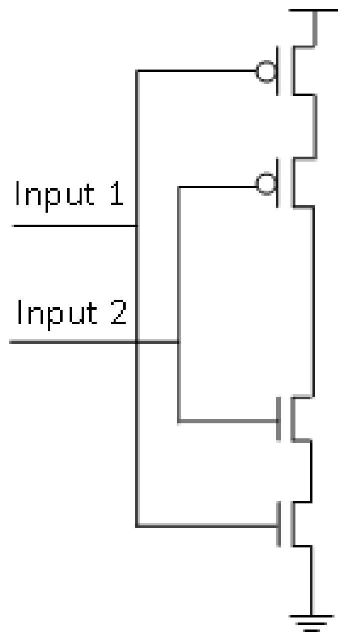


Figure II-9. Guard gate [14]

Knudsen et al. presented a D latch using time redundancy. As depicted in Figure II-10, this structure has three feedback paths, namely MD, MDb, and MDDb. MD is delayed by δ to generate MDb, and MDb is delayed by δ to get MDDb. These three redundant feedback paths are connected to a majority voter. This voter evaluates the latch's logic output by comparing the logic values of MD, MDb, and MDDb [15].

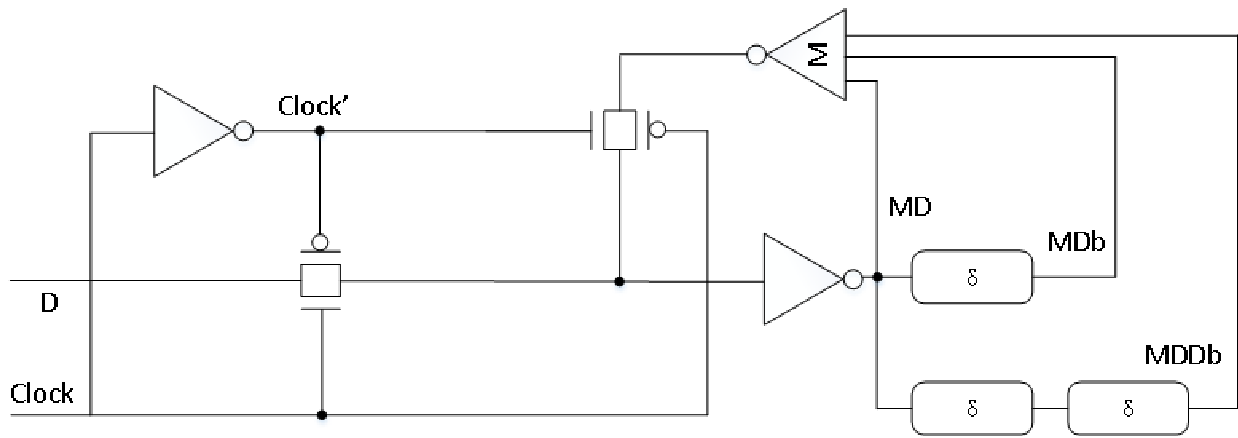
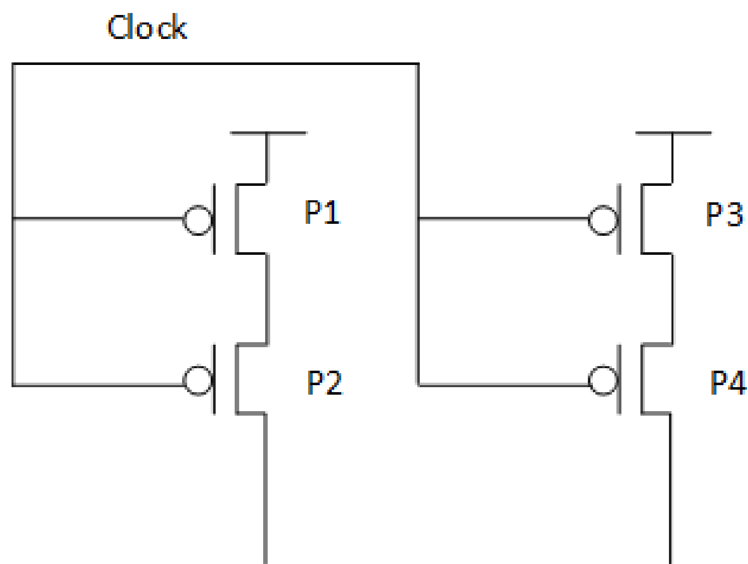


Figure II-10. The temporal latch design [15]

Although the temporal approach demonstrates immunity to both SET and SEU, its drawback is very obvious. It introduces large delays in the circuit, and therefore, the setup time of a temporal hardened latch has increased [16].

Erstad proposed a hardened precharge circuit in his patent. The precharge circuit consists of 4 PMOS transistors, P1 through P4. P1 and P2, as well as P3 and P4, are connected in series. These two serial paths are connected, forming two parallel branches. The dual-output dynamic circuit is hardened using this hardened precharge circuit and two duplicated pull-down networks [17].



(a)

(b)

Figure II-11 Hardened Dynamic Logic circuit [17]

2.4.2 Resistive Hardening

The SEU process is in essence a race between feedback and recovery time, as illustrated in Figure II-12. Therefore, The SEU sensitivity can be reduced by either increasing the feedback delay or decreasing the recovery delay [1]. Feedback resistors made by lightly doped polysilicon regions are commonly implemented in order to delay the feedback time. However, this technique has proven to bring about severe performance degradation due to the increased write delay. In the meantime, it does not scale very well for advanced technology nodes. This is because the feedback resistance must be increased while the nodal capacitance is being reduced with technology scaling [18].

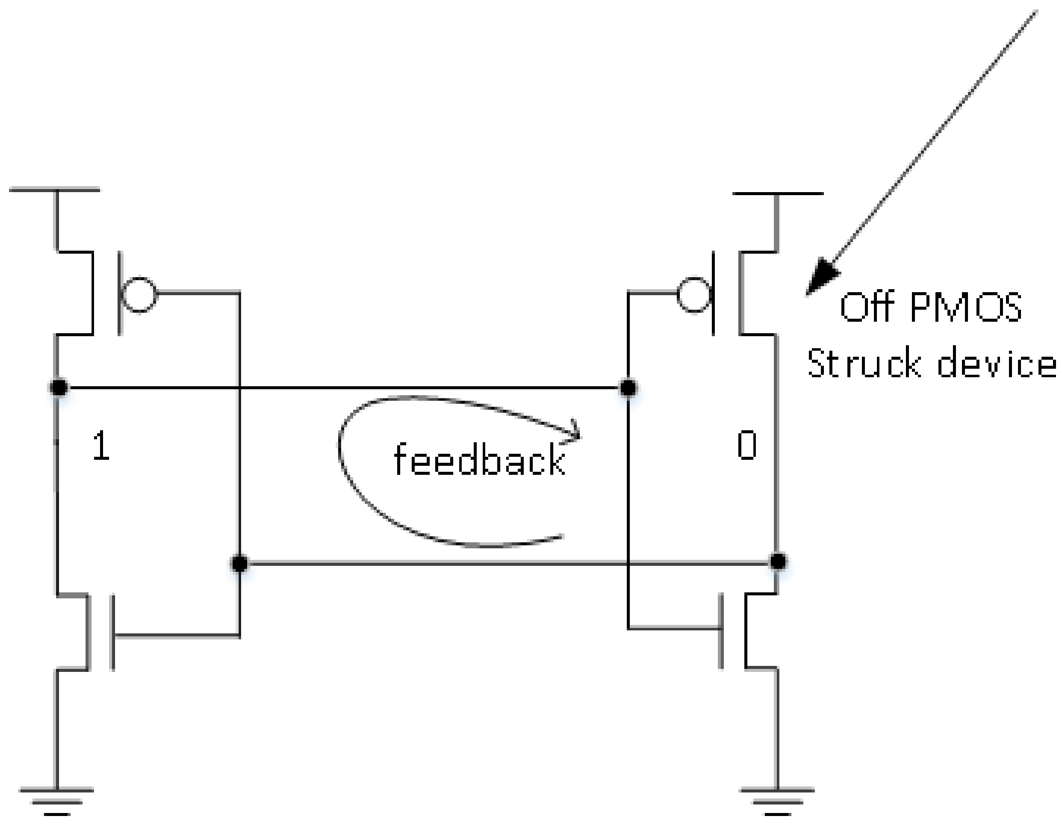


Figure II-12. The illustration of feedback and recovery process [1]

2.4.3 Differential Structures

Differential structures have revealed tolerance to SEE effects in analog circuits [19][20]. In turn, their efficacy has also been investigated in digital circuits. Cascode Voltage Switch Logic (CVSL) is a type of differential circuit with differential inputs and outputs. As displayed in Figure II-13, it has two complementary pull-down networks and two PMOS transistors that are connected in a cross-couple fashion. Casey et al. simulated a CVSL-based latch, demonstrating the latch's tolerance to multiple node charge collection [21]. Hatano also indicated that the tolerance of the static CVSL circuit is ~200X relative to its CMOS counterparts [22]. Quatro is another hardened storage cell utilizing the differential structures, demonstrating significant SEU improvement when compared to a D latch or 6T memory cell [23]. Hatano investigated the single event tolerance of the clocked CVSL circuit, which was composed of two domino gates. Its reduction in cross-section is ~20X relative to the CMOS circuit [22].

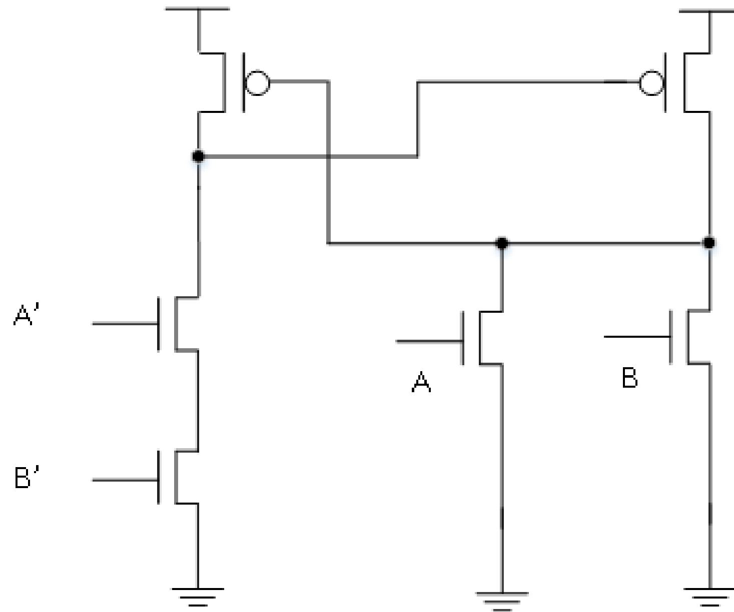


Figure II-13. A CVSL NOR Gate

2.4.4 Well/Substrate Taps

As illustrated in Figure II-14, well (substrate) taps are heavily doped p+ (n+) contacts buried in the n-well (p-substrate). These taps are used to provide low resistant paths, and thus, they can provide a better bias for the body terminals of PMOS/NMOS at Vdd/Gnd. Guard rings and guard bands are high-density contacts surrounding the devices of interest. Guard drains are in fact another form of heavily-doped regions placed near the devices of interest, presenting themselves as reversed biased diodes [24]. They are displayed in Figure II-15.

High density well contacts are particularly effective for PMOS devices [24]. This is because charge collection in PMOS transistors is predominantly caused by nwell collapse and the resulting parasitic bipolar enhancement. By adding high-density well contacts, the well potential is prone to being firmly held at Vdd so that the bipolar transistor is less easily be turned on. On the contrary, guard drains are particularly effective for NMOS devices, whose mechanism of charge sharing is dominated by diffusion.

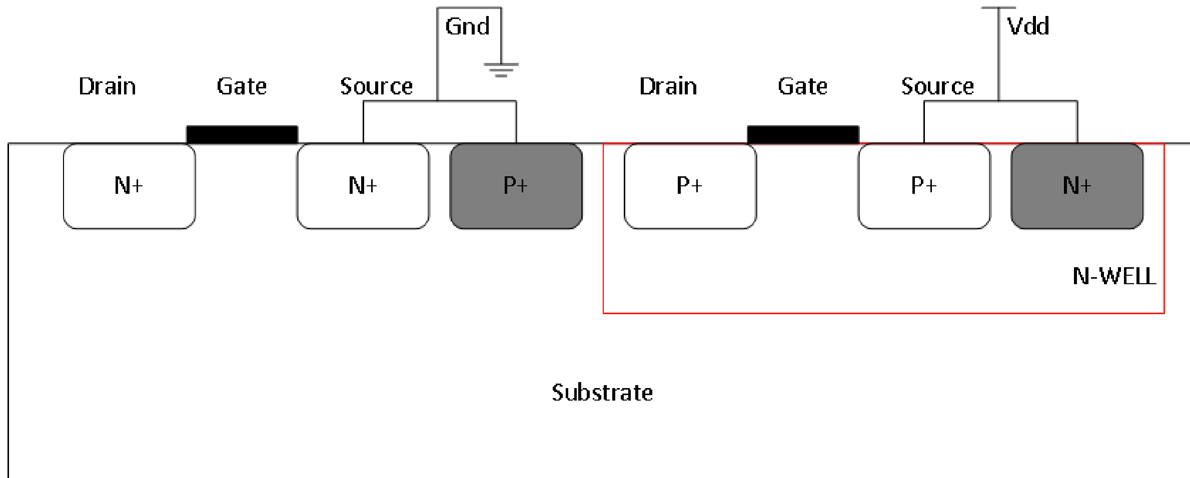


Figure II-14. Well and substrate contacts

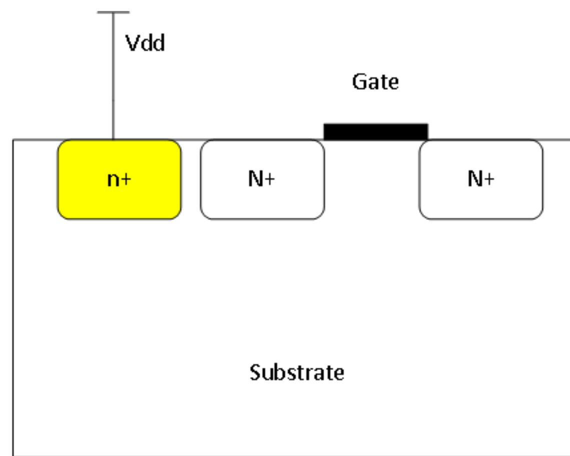


Figure II-15. Guard drains for NMOS devices [24]

2.4.5 Charge Cancellation via Layout Manipulation

For analog circuits, a common centroid layout illustrated in Figure II-16, in which transistors are split into multiple blocks and re-placed for better device matching, has been simulated and experimentally evaluated in terms of its response to single event strikes by researchers. This layout technique has been found to promote charge sharing, thereby reducing the circuit sensitive areas [19][20].

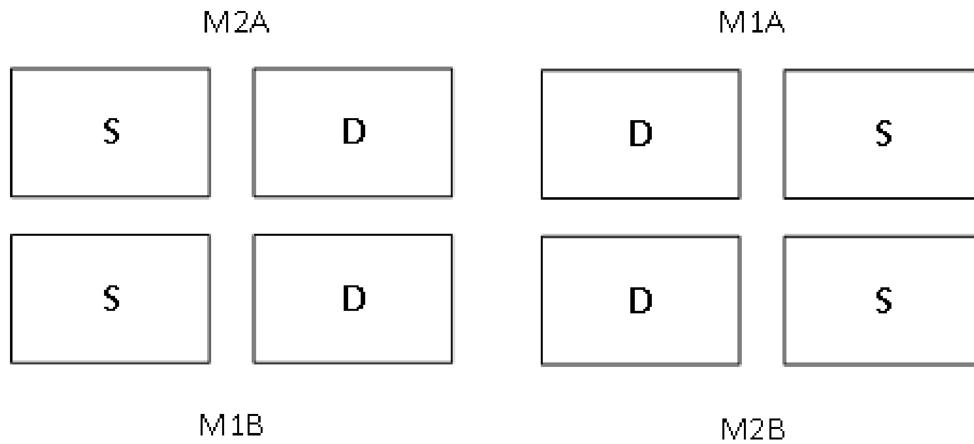
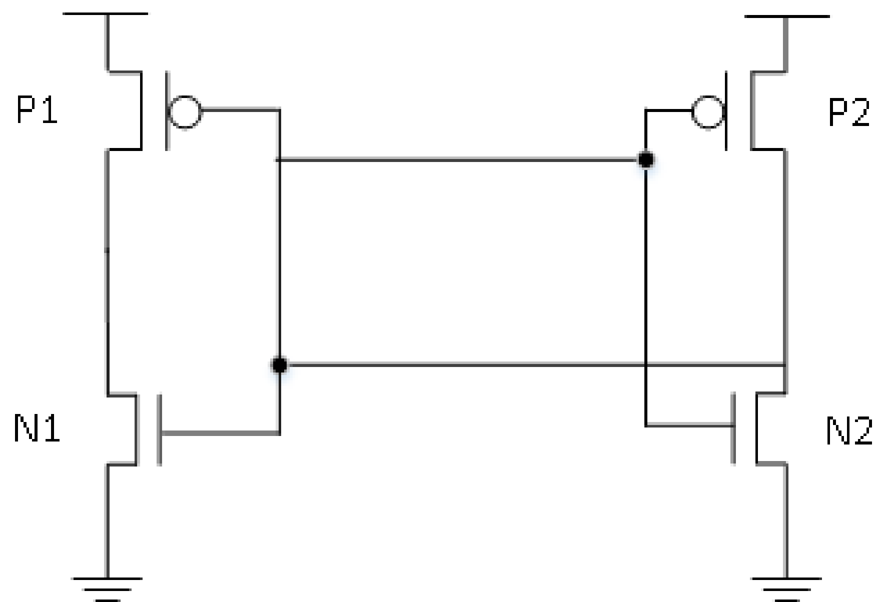
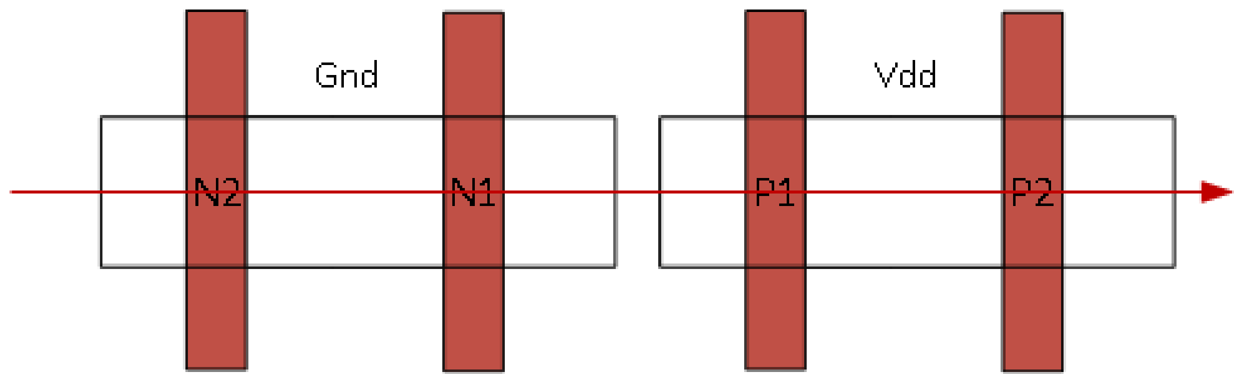


Figure II-16. Common centroid layout [19][20]

Lee et al. proposed a layout technique illustrated in Figure II-17, in which multiple drains are placed in a fashion that is beneficial to cancelling the overall single event response. Their experiments demonstrated that the LEAP-DICE flip-flop fabricated in a 180nm CMOS test chip experienced a reduction of SER by 5X and 20X when compared to the reference DICE or flip-flop, respectively [25].



(a)



(b)

Figure II-17. The LEAP layout example for an inveter pair [25]

2.5 Testing Methodologies and Challenges

2.5.1 Particle Accelerators

There are a variety of particle accelerators dedicated to single-event hardness assurance testing purposes around the world. These facilities provide radiation particles of a wide range of ion species, energy, and flux. Some of the most frequently accessed facilities are Texas A&M, Berkeley lab, Indiana University Cyclotron Facility, and Brookhaven National Laboratory. Texas A&M offers beams with energy as high as 40 MeV/nucleon.

Proton tests may need to be carried out if available heavy ion experimental results show that the IC is sensitive to low-LET ions. Examples of high-energy proton facilities are the Indiana University Cyclotron Facility (IUCF), and Canada's TRIUMF. The proton energy spectrum offered by the latter spans from 20 MeV to 500 MeV, which is ideal for low-earth radiation tests.

For proton testing with energy > 30 MeV, de-liding or de-packing the ICs is not usually necessary because protons in such an energy spectrum are able to penetrate packing materials. However, for proton energy lower than 30 MeV, the lid of the IC must be removed to ensure that the devices can be reached by protons. De-liding also applies to heavy ion and alpha testings [26].

2.5.2 Pulsed Lasers

The term laser stands for light amplification by stimulated emission of radiation. A laser can operate in two modes: continuous or pulsed. Lasers of the latter mode are tightly focused laser spots, presenting themselves in the form of light pulses.

Pulsed lasers have been widely used for radiation hardness assurance testing in this community [27]–[41]. Two types of pulsed lasers exist, namely Single Photon Absorption Lasers (SPA) and Two Photon Absorption Lasers (TPA). The former refers to a single photon with a corresponding energy that is larger than the bandgap of the semiconductor material and therefore is able to generate a pair of electrons and holes. Weakly absorbed laser beams are more optimal candidates because they generate low charge density in the charge track and can travel long distances into the semiconductor material [36]. Results presented by researchers show that the risetimes for heavy-ion-induced SET pulse are ~20 ps. Thus, to better simulate heavy ions, the pulse length of pulsed lasers are configured in the range of ps [31].

Although SPA picosecond pulsed lasers have been used in this community prior to TPA lasers, they have their intrinsic limitations. As the IC technology advances, this trend is accompanied by the increasing thickness of overlayers (e.g., metal or insulator). Therefore, SPA lasers whose wavelength is relatively short are not able to penetrate deep into silicon and reach the target devices. TPA lasers were introduced and have gained favor because TPA lasers use a larger wavelength [36]. As illustrated in Figure II-18, as the wavelength gets larger, the absorption coefficient decreases.

Unlike SPA lasers, TPA lasers need to absorb two photons simultaneously in order to generate a single pair of electrons and holes. A single photon cannot generate an electron because its energy is in the sub band gap region [36]. In order to get these types of lasers working, high light intensity is required. This is because two-photon absorption is a third-order process, which is much weaker than a SPA absorption process.

However, new packaging options have posed challenges for laser testing. Specifically, the flip-chip packaging technique is widely used in many modern ICs. This technique enables lasers to irradiate the circuits of interest from the backside, thereby avoiding the chance of being stopped. On the other hand, a great deal of difficulty exists in thinning the substrate over the entire die uniformly. Considering the fact that TPA lasers depend on the higher orders of the

pulse irradiance, even a small variation in pulse irradiance on the substrate surface may significantly change the single event response [29].

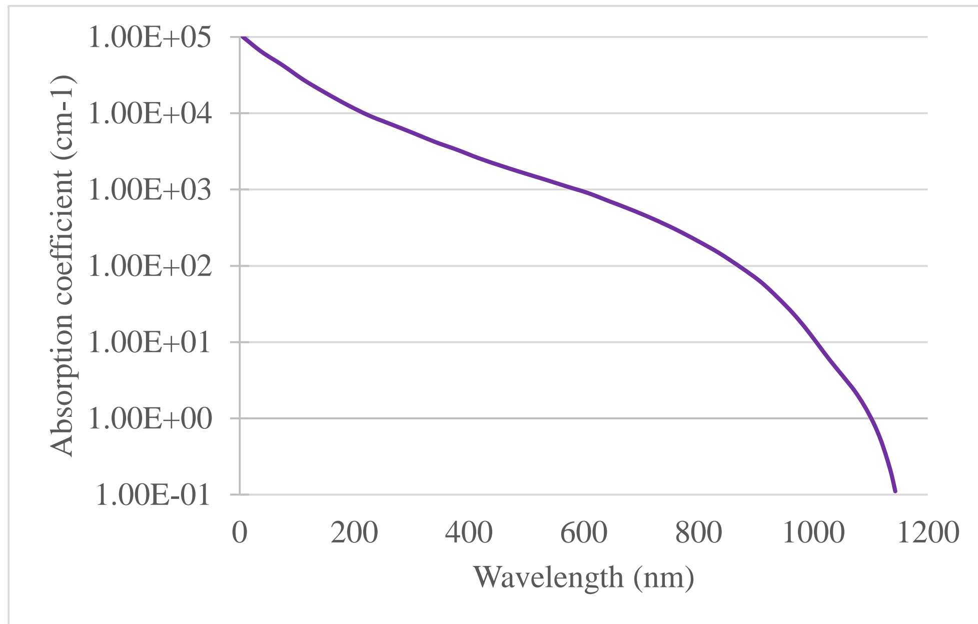


Figure II-18. The curve of absorption coefficient vs. wavelength at room temperature for both visible and near-infrared regions [36]

Although lasers are a valuable alternative to heavy ions, there remains differences between heavy ions and lasers. The charge track caused by heavy ions is less than 100nm, while the laser has a much larger diameter of the laser spot (>1um). As a consequence, for advanced technology nodes, a laser spot can irradiate several sensitive locations simultaneously when compared to heavy ions. Moreover, the laser produces a broad Gaussian-shaped charge distribution, while the ion produces charge that is more localized along the track [31]. In addition, users have unique control on the timing and location of the charge collection through the use of lasers, while this same control fails to exist in broad-beam heavy ion testings [30]. Finally, lasers do not cause the total dose or displacement damage that is characteristic of heavy ions [28] [45].

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III. AN SEU-TOLERANT DICE LATCH DESIGN WITH FEEDBACK TRANSISTORS

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Wang, H.-B.; Li, Y.-Q.; Chen, L.; Li, L.-X.; Liu, R.; Baeg, S.; Mahatme, N.; Bhuva, B.L.; Wen, S.-J.; Wong, R.; Fung, R., "An SEU-Tolerant DICE Latch Design With Feedback Transistors," *IEEE Transactions on Nuclear Science*, vol.62, no.2, pp.548-554, April 2015.

Basic physics of single event effects and hardening techniques are presented in the previous chapter. In old technologies, a single ion hit may probably result in one node collecting charge. However, in deep submicron and advanced technologies, packing densities have been significantly increased, thereby decreasing the spacing of devices. This in turn increases charge sharing between neighboring devices and as a result decreasing the single event tolerance of a hardened design. Due to these changes, those tolerant techniques have been made less effective. Among those hardened storage cell designs, DICE, which enjoyed wide popularity in the industry due to its single node upset immunity, showed no significant improvement in single event performance when compared to regular D latch. Therefore, new single event resilient structures need to be proposed and evaluated.

In this manuscript, DICE is hardened by using resistive hardening techniques. Feedback transistors are added to these feedback loops of DICE. These extra transistors are turned ON if the latch is in a write mode, otherwise, it is turned OFF. As a consequence, the write time of this proposed design does not see a significant increase, while the feedback time in the hold time increases significantly. Moreover, the extra PMOS transistors are connected to a PMOS, and the extra NMOS transistors are connected to a NMOS. The benefit of these configurations is hitting a feedback PMOS (NMOS) may drive its output up (down) without turning on the PMOS (NMOS) connected to this hit device. TCAD simulation results demonstrate fewer sensitive node pairs than the traditional DICE, suggesting increased single event tolerance. Irrational experimental were

also carried out. These results indicate that the proposed design has a higher upset threshold and a high magnitude reduction in cross-section.

An SEU-Tolerant DICE Latch Design with Feedback Transistors

Wang, H.-B.; Li, Y.-Q.; Chen, L.; Li, L.-X.; Liu, R.; Baeg, S.; Mahatme, N.;

Bhuva, B.L.; Wen, S.-J.; Wong, R.; Fung, R.

Abstract

This paper presents an SEU-tolerant Dual Interlocked Storage Cell (DICE) latch design with both PMOS and NMOS transistors in the feedback paths. The feedback transistors improve the SEU tolerance by increasing the feedback loop delay during the hold mode. The latch design was implemented in a shift register fashion at a 130-nm bulk CMOS process node. Exposures to heavy-ions exhibited a significantly higher upset LET threshold and lower cross-section compared with the traditional DICE latch design. Performance penalties in terms of write delay, power, and area are non-significant compared to traditional DICE design.

Index terms

Soft error, dual interlocked storage cell (DICE), single event upset, radiation hardening, charge sharing.

3.1 Introduction

A SINGLE EVENT UPSET (SEU) is an error induced by an incident particle on an integrated circuit (IC) [1][2]. The incident particle generates electron-hole pairs as it traverses through the semiconductor material. The electrons (or holes) may get collected at a circuit node, resulting in a voltage perturbation at that node. Such a transient then may propagate through the circuit connected to the affected node and may introduce operational errors. If the affected node belongs to a latch design, the data stored in the latch may get altered, resulting in an SEU.

SEU mitigation is required to ensure data integrity in critical components, even though these SEU errors do not cause any long-term effects by their very nature. The Semiconductor Industry Association (SIA) Roadmap has identified SEU effects as the major threat to reliable operation of electronic systems in the future [3]. Researchers have used radiation hardening techniques at the circuit and system level to improve SEU performance of ICs. Such Radiation-Hardening-by-Design (RHBD) techniques may include spatial as well as temporal redundancy. For arrayed cells, such as memory circuits, Error Correction Codes (ECC) are also used [4]. Temporal redundancy uses multiple sampling of a given node during one clock cycle to ensure data integrity [5]. Such techniques require extra design efforts and usually exact heavy performance penalties. Spatial redundancy techniques, such as Triple Modular Redundancy (TMR) and Dual Interlocked Storage Cell (DICE) designs, increase the reliability of the system at varying levels of performance penalties [4]-[7]. Because of superior SEU performance and acceptable performance penalties possible, DICE-based designs are preferred by designers over all other latch designs. DICE-based latch designs are virtually immune to SEU when a single node collects charge. Various techniques have been developed for DICE-based latch designs that include separating sensitive nodes [8]-[10], use of well contacts, guard bands, or guard rings [8]-[12], and charge cancellation via layout manipulation [13]. All of these techniques show excellent SEU performance with varying design complexity and performance penalty.

However, as the ever-shrinking feature size on an IC continues to scale down and spacing between transistors decreases, the charge deposited at a single node may be collected at multiple nodes. This becomes the norm for heavy-ion exposures in deep-submicron CMOS bulk technologies [8][12]. Due to charge sharing, the cross-section magnitude decrease of DICE was demonstrated to be only 30%-50% compared with a D flip-flop [14]. The implication of previous work necessitates latch designs tolerant to multi-node upsets in deep-submicron CMOS bulk technologies. In this paper, the design of a novel DICE-based latch using transistors in the feedback paths to mitigate multiple node upsets is presented. The rest of the paper is organized as follows: Section II reviews DICE-based designs and their issues; Section III presents the proposed design and its TCAD simulations to address these issues; Section IV shows the test chip design fabricated in a 130nm technology node; Section V presents the experimental results obtained from heavy ion testing followed by discussions in Section VI.

3.2 Background

A digital static storage cells (e.g., a traditional D latch) is involved with a positive feedback loop. To overwrite the data already present in the cell, a transient signal longer than the feedback loop delay should be introduced at one of the storage nodes in the cell. Along the same line, if a single-event induced transient (or voltage perturbation) is longer than the feedback loop delay of the cell, an upset will occur. A DICE cell demonstrates significant single node upset tolerance because it is designed such that increases in the feedback loop delay during the hold state are significantly high. The increase in write time, however, is minimal because data is written to multiple storage nodes directly.

Figure III-1. The structure of the TDICE design [16]; two feedback transistors (N12 and N34) of this design are hit simultaneously during the hold mode to illustrate its single event susceptibility.

Resistive hardening techniques can be applied to harden DICE by increasing the feedback loop delay, but this introduces the performance penalty because of an increase in the write time of the cell [15]. D'Alessio et al. introduced TDICE, where four additional feedback NMOS transistors were added in the DICE design as shown in Fig. 1. The additional transistors are ON only when the cell is in a write operation, yielding very low resistance and low feedback delay. During the hold mode, the transistors are OFF, resulting in higher feedback loop delay and

improved SEU performance. Results presented by D'Alessio et al. show ~3X improvement in critical charge of sensitive pairs [16].

However, the TDICE cell is susceptible to striking feedback transistors simultaneously. For instance, assume nodes A, B, C, and Q store 0, 1, 0, and 1 respectively, during the hold mode, as shown in Fig. 1. If two feedback transistors, N12 and N34 for example, are struck by an ion particle, their drain voltages will go down. This may lead to a cascade of switching on their adjacent PMOS devices, P1 and P3, and then the voltages of A and being pulled up and flipped, which in turn may flip B and Q, as shown in Fig. 2. Therefore, the feedback transistors may not be as effective as expected if these two such transistors are hit simultaneously or collect charge from a single ion hit.

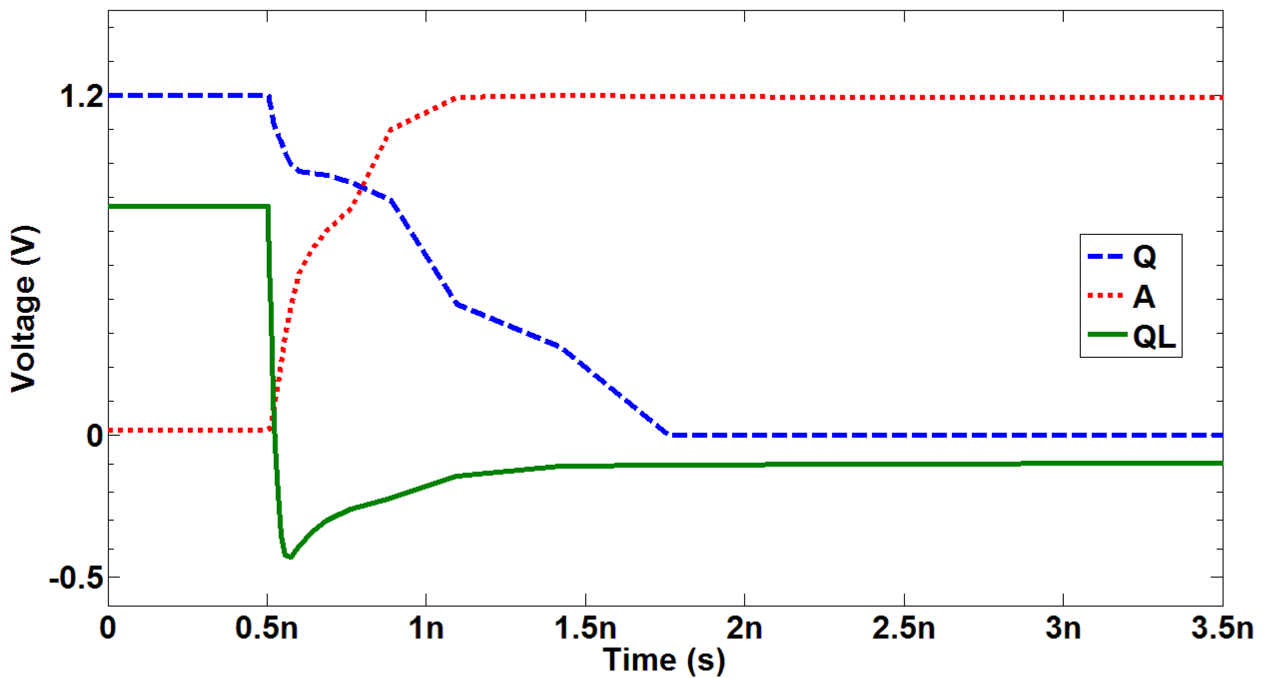


Figure III-2. Accuro simulation results of striking feedback transistors N12 and N34 simultaneously by an ion particle with MeV*cm^2/mg when Q=1.

3.3 Proposed Design and Simulation Results

3.3.1 Proposed Design

The structure of the proposed DICE latch is shown in Fig. 3. Different from the design shown in Fig. 1, the proposed latch uses both PMOS and NMOS devices as the feedback transistors. One pair of PMOS and NMOS (P12 and N23) is connected to node B, and another pair (P34 and N41) is connected to node Q.

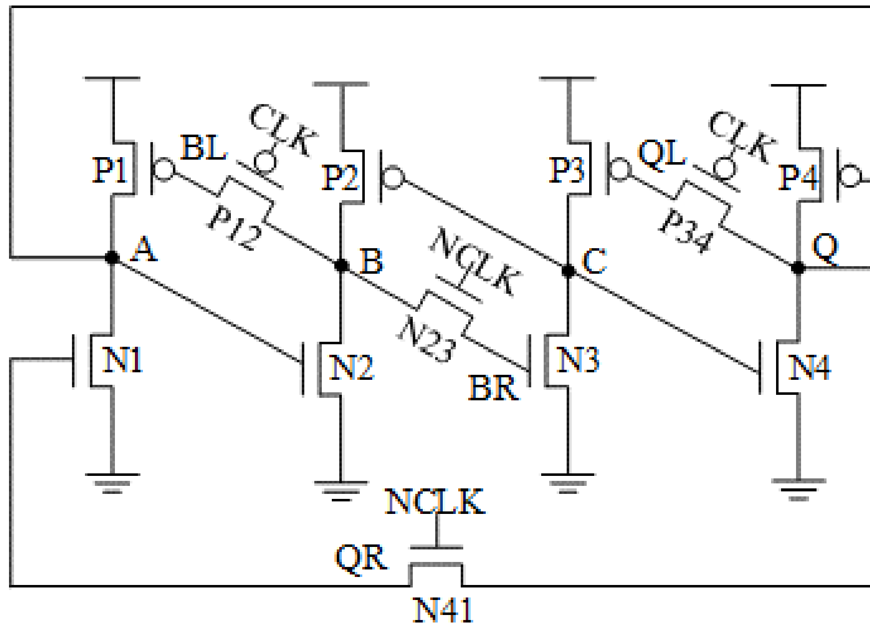


Figure III-3. The structure of the proposed design in this paper. It has four more transistors than DICE. These transistors are placed in the feedback loops and they are turned ON only if the cell is in the write mode.

During a write operation, CLK and NCLK are driven to logic LOW and HIGH respectively, thus turning ON all the four feedback transistors. Like traditional DICE cell, the logic values of B and Q can be written to nodes BL, BR, QL, and QR through those four on-state clocked transistors. As a consequence, new data and its complementary value can be written into the four internal nodes A, B, C, and Q. On the other hand, when CLK and NCLK are driven to logic HIGH and LOW respectively, all the four clocked transistor are turned OFF, and the latch is in the hold mode.

In order to evaluate the SEU performance of the proposed design in the device level, Accuro, a TCAD software, has been used throughout the work. By fully taking into account layout, substrate, and circuit details, Accuro is able to accurately simulate single event charge distribution and charge collection with varying particle LET values and incident angles [13].

3.3.2 Single Node Upsets Analysis

In the case when there is a single event strike on node A, the induced SET pulse may flip one adjacent node (B or Q). However, the incorrect logic value at this adjacent node is not able to propagate because of the off-state clocked transistors. Once the charge injected to A is removed by the on-state transistors, all nodes return to their original states. The same analysis applies to node C as well.

If node B is struck, the voltage glitch at this node cannot propagate to other nodes because both of the feedback transistors (P12 and N23) connected to this struck node are turned OFF. The deposited charge will eventually be removed and the state of the hit node will be recovered. This is the same thing for node Q.

Striking one of the additional four nodes BR, BL, QR, and QL does not flip the cell. For example, in the case where A, B, C, and Q store logic 1, 0, 1, and 0 respectively, the logic values of BR, BL, QR, and QL are logic 0. If node BL, which is connected to a reverse-biased junction, sees a positive single event transient. This transient only makes node A float (high impedance state) by turning off P1, and therefore, this will not change the logic state of A.

3.3.3 Double Node Upsets Analysis

Because the structure of the proposed latch is symmetric, double node upset is analyzed assuming that nodes A, B, C, and Q store 1, 0, 1, and 0 respectively.

If two transistors P2 and P4 are hit simultaneously that causes both alternate nodes (B and Q) to observe positive SET transients, but B and Q are not able to propagate. Since the logic state of A is determined by uncorrupted nodes BL and QR, and the state of C is determined by uncorrupted nodes QL and BR, A and C do not flip; and B and Q will then recover. The analysis is verified by a heavy ion particle travelling through the center of P2's drain area and the center

of P4's drain area with LET = 20 MeV*cm^2/mg and the tilt angle of 90^0 (i.e., along the power rail) in Accuro as shown in Fig. 4.

If two transistors N3 and P4 are hit simultaneously, C and Q may observe a negative and positive SET pulse respectively. Even if B is corrupted as a result, it will not propagate. Once node C recovers because of uncorrupted nodes BR and QL, Q and will recover too. This is illustrated in Fig. 5.

The only sensitive node pair is [BL, A]. This is explained as follows. Let us assume node A sees a 1 -> 0 SET pulse and node BL sees a 0 -> 1 SET pulse at the same time, node A will not be able to recover because node BL turns OFF P1 and cuts off the conduction path of node A to the supply rail. As a consequence, node Q may flip depending on the drive strength of P4 vs. that of N4. This is illustrated in Fig. 6. Similarly, [BR, C] is identified to be the sensitive node pair when nodes A, B, C, Q store logic 0, 1, 0, and 1 respectively.

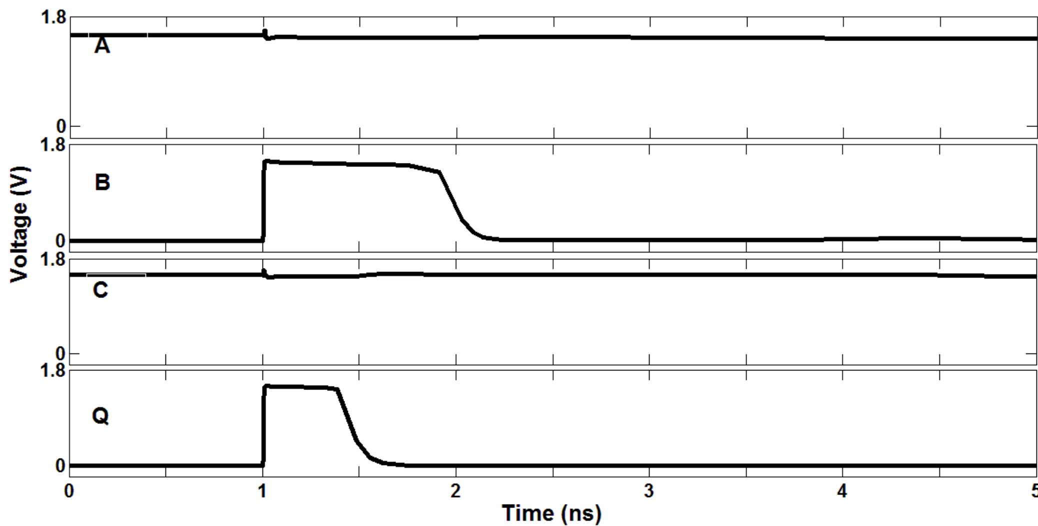


Figure III-4. Accuro simulation results of striking P2 and P4 simultaneously by an ion particle with 20 MeV*cm^2/mg when Q=0. Nodes B and Q are able to recover. The latch does not upset showing the insensitivity of alternate node pairs.

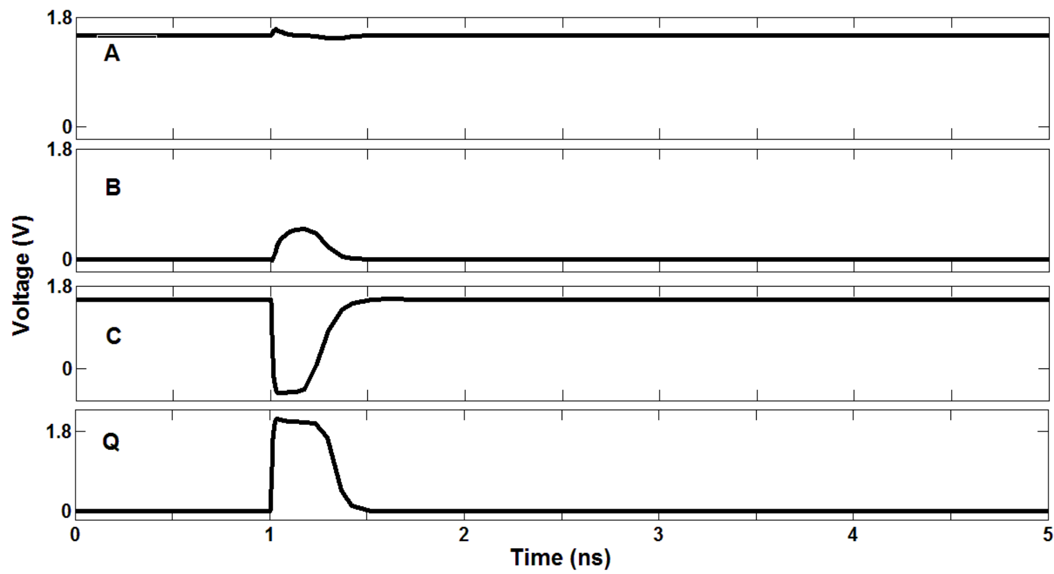


Figure III-5. Accuro simulation results of striking N3 and P4 simultaneously by an ion particle with 20 MeV*cm^2/mg when Q=0. Nodes C and Q are able to recover. The latch does not upset showing the insensitivity of adjacent node pairs.

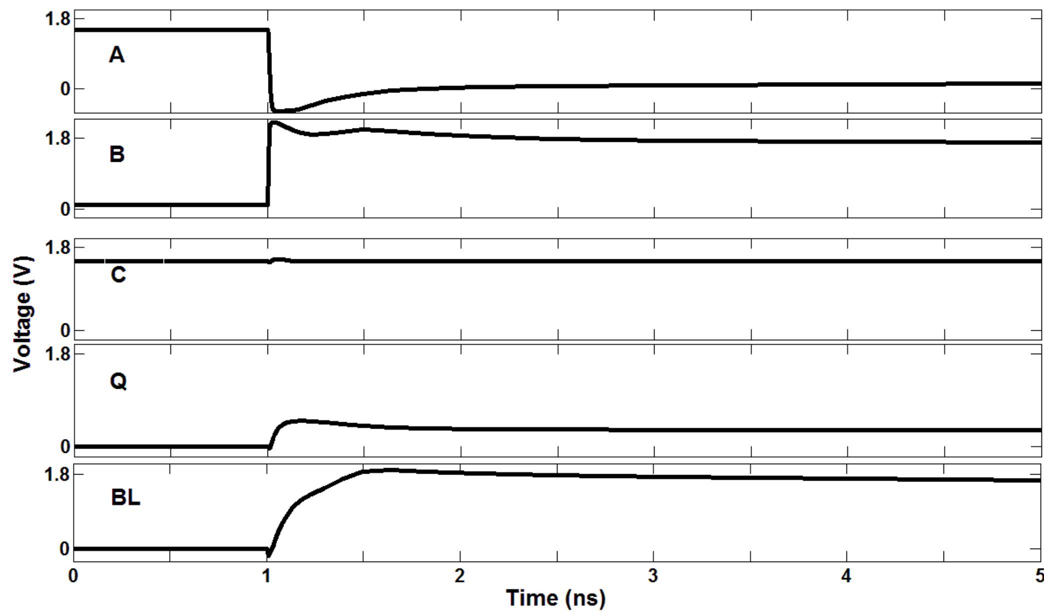


Figure III-6. Accuro simulation results of striking N1 and P12 simultaneously by an ion particle with 20 MeV*cm^2/mg when Q=0. Nodes BL and A are not able to recover. This illustrates that [BL, A] is a sensitive node pair.

To conclude, the proposed design has only 1 sensitive node pair, while DICE cell has 6 pairs [17]. Fewer sensitive node pairs leads to higher SEU tolerance when compared to DICE cell. By

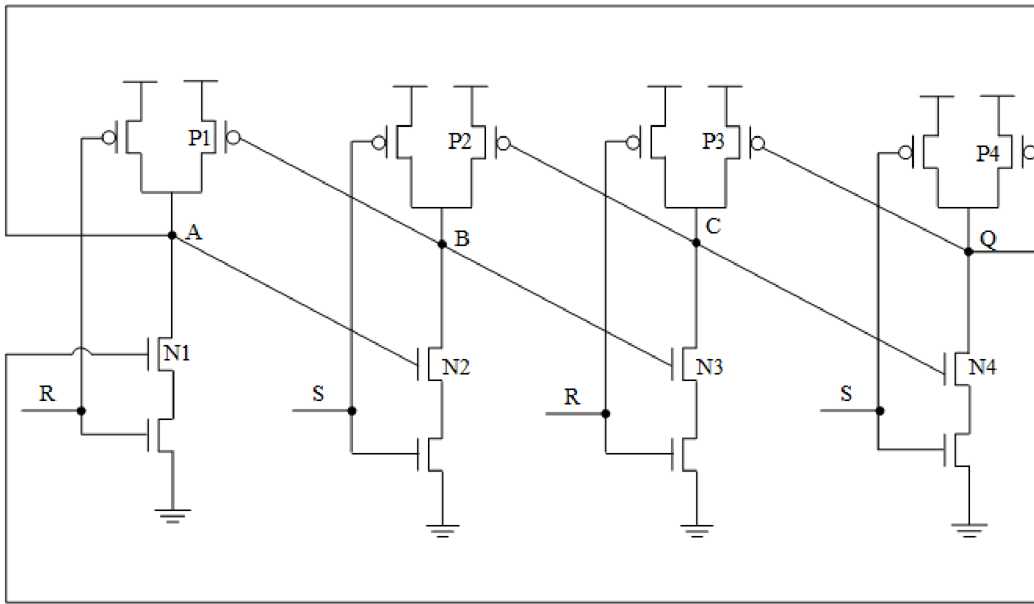
separating this sensitive node pair, the proposed design is expected to have better SEU performance.

3.4 Test Chip Design

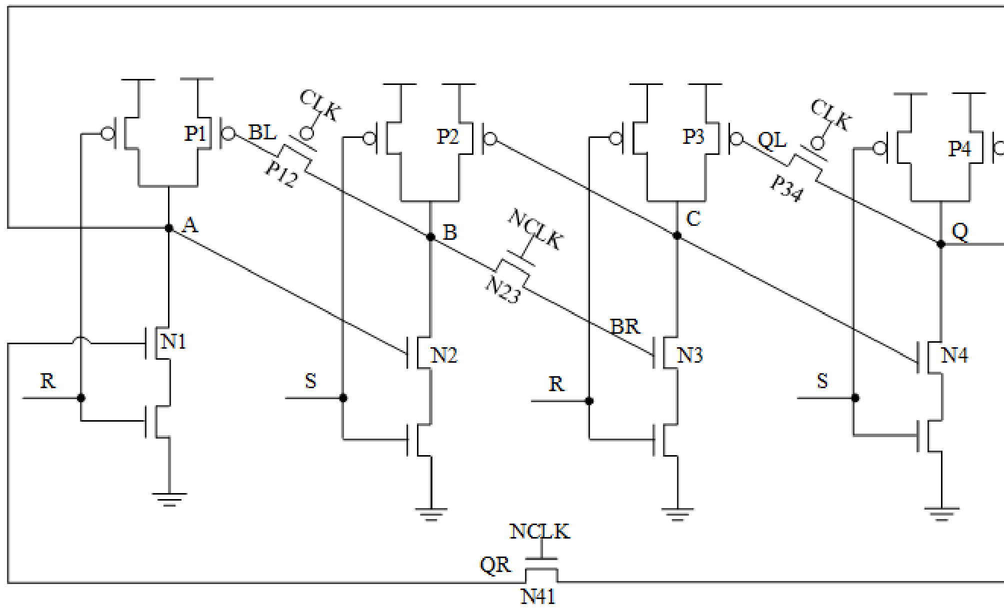
A test chip utilizing an array of the proposed design and the reference DICE cell was designed in a shift register and fabricated at a 130nm bulk CMOS process node. The nominal core voltage in this process is either 1.2V or 1.5V. Test structures were comprised of two shift register chains, each containing 792 flip-flops. Each flip-flop consists of one master SR latch and one slave SR latch. As shown in Fig. 7, the latch is built in an SR-style with NAND gates because (1) the SR latch is the most flexible type of latch and it can be easily converted to any other types of latch by using simple external logic circuits [18]; and (2) this is a ratioless latch structure, which implies that its function does not depend on the size of the transistors (i.e., P1, N1, etc.).

The SR-generation circuit illustrated in Fig. 7 (c) is used to generate input signals (S and R) for the SR latch. In the scenario of CLK = H and NCLK = L, the SR latch in the hold state because S = H and R = H. On the other hand, when CLK = L and NCLK = H, the latch is in the transparent phase and new data can be written to the latch. (1) D = L results in S = H, R = L, and Q = L; (2) D = H results in S = L, R = H, and Q = H.

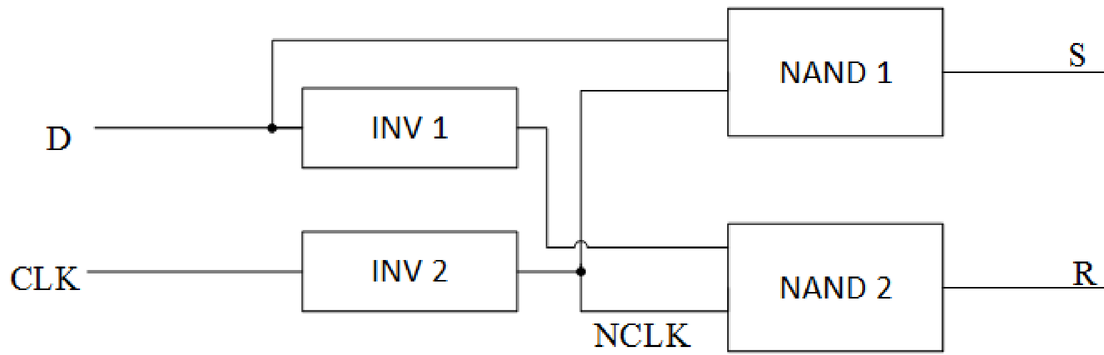
Hold violation and clock skew issues of the shift registers are addressed by using the reverse clocking scheme. By using this approach, the clock signal propagates through the flip-flop chains in the reverse direction with respect to data.



(a)



(b)



(c)

Figure III-7. (a) and (b) the SR latch in the configuration of either DICE or proposed design built with NAND gates; (c) the SR-generation circuit used to generate the input signals for both SR latches. The DICE latch is constructed of (c) directly connected to (a), while the proposed Latch is constructed of (c) directly connected to (b).

3.5 Heavy Ion Experimental Results

The SEU cross sections for these designs were measured with heavy ions obtained from the heavy-ion accelerator at the Cyclotron Institute of Texas A&M University. This facility provides a variety of heavy ion beams for single event effects tests.

Three sets of heavy ion testings were carried out. During these experiments, 1.2V was applied to power the test chip. The test system is composed of an FPGA board and a daughter card on which the 130nm test chip is mounted. The FPGA board counts SEU errors and sends them to a computer for processing in real-time.

A fixed logic LOW with the clock frequency of either 10 kHz or 1 MHz were fed into the shift register chains. It is noted that the input pattern of checkerboard (0101...) was not used in order to eliminate burst errors caused by hitting the clock buffers.

The test chip operating at 10 kHz was bombarded by normal incident heavy ions. The ion profiles used for this experiment are tabulated in Table I. Fig. 8 shows the cross-section data of the proposed design and various baseline DICE cells fabricated in 130nm technologies [11][19]. The proposed design demonstrated a much higher upset threshold when compared to these reference DICE cells because it did not see any SEU errors for an LET up to 35 MeV*cm^2/mg. This verifies the effectiveness of the proposed design.

TABLE III-1 NORMAL INCIDENT HEAVY IONS USED FOR THE EXPERIMENT WITH 10 KHZ

LET (MeV*cm^2/mg)	Ion	Fluence	Energy (MeV/u)	Range (um)
1.3	N	8.03^8	14.3	397.6
2.7	Ne	6.22^8	14.1	285.4
10	Ar	5.55^8	9.6	122.8
35	Kr	1.67^8	6.2	63.3

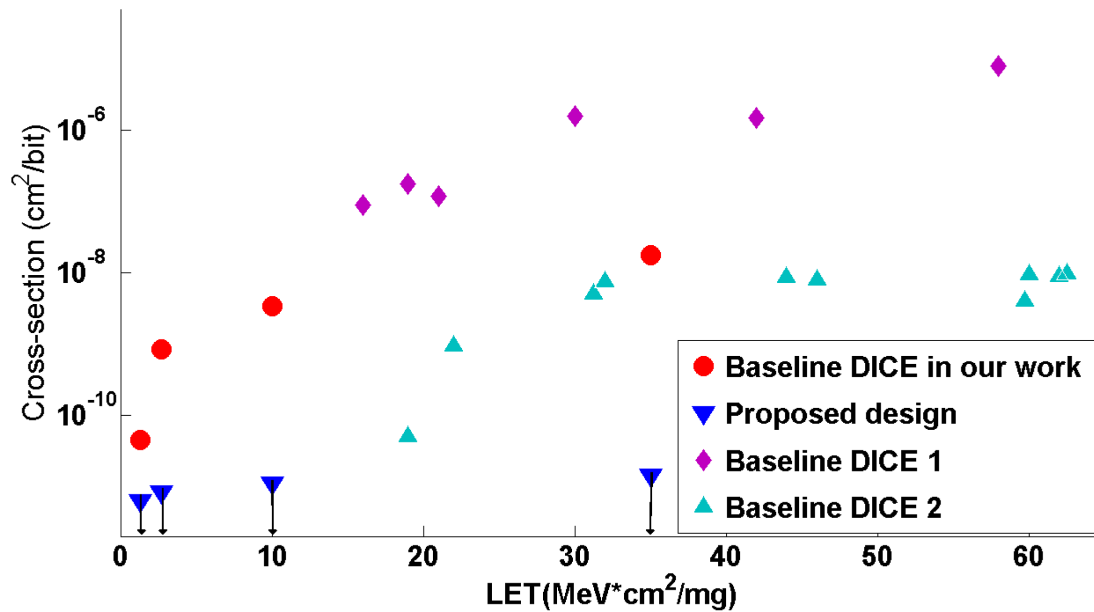


Figure III-8. Cross-section data of the proposed design and our reference DICE cell for normal strike with the clock frequency of 10 kHz and all 0s as the input; No SEU errors were observed for the proposed design. Experimental results of baseline DICE 1 and 2 were presented in [11][19].

The test chip operating at 10 kHz was then irradiated by angular strikes. Table II shows the profiles of these ions used for this experiment. Due to the limitation of the test system setup, the maximum angle used was 50^0. Fig. 9 illustrates that both DICE and the proposed design showed a much higher soft error rate, which is as large as approximately 5X. The proposed design started to see errors at an LET of 28 MeV*cm^2/mg.

TABLE III-2 HEAVY IONS USED FOR EITHER 50^0 STRIKES OR 1 MHZ CLOCK FREQUENCY

LET (MeV*cm^2/mg)	Ion	Fluence	Energy (MeV/u)	Range (um)
1.3	N	1.50^8	14.1	385.6
2.7	Ne	1.00^8	13.7	273.5
8.4	Ar	5.00^8	13	186.1
28	Kr	1.00^8	11.8	128

A higher clock frequency, 1 MHz, was used to drive the shift register chains. The same types of ions as illustrated in Table II were directed to strike the test chip with normal incidence. Fig. 10 illustrates that both DICE and the proposed design demonstrated much lower soft error tolerance when compared to 10 kHz. The upset LET threshold of the proposed design decreased to 28 MeV*cm^2/mg.

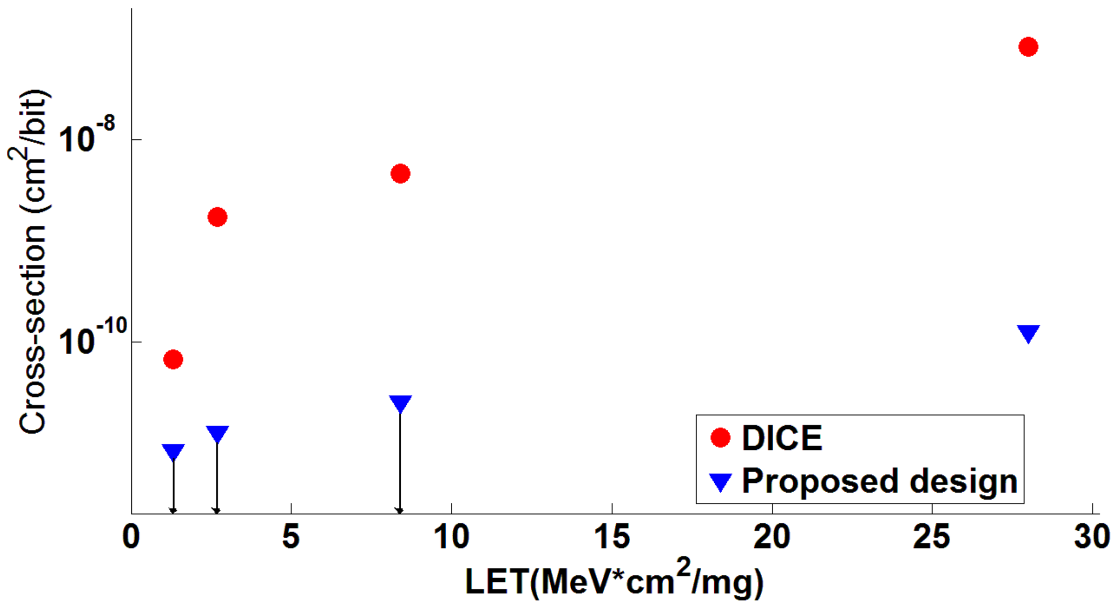


Figure III-9. Cross-section data of both DICE and the proposed design for strike with the clock frequency of 10 kHz and all 0s as the input; the proposed design started to see SEU errors at 28MeV*cm^2/mg.

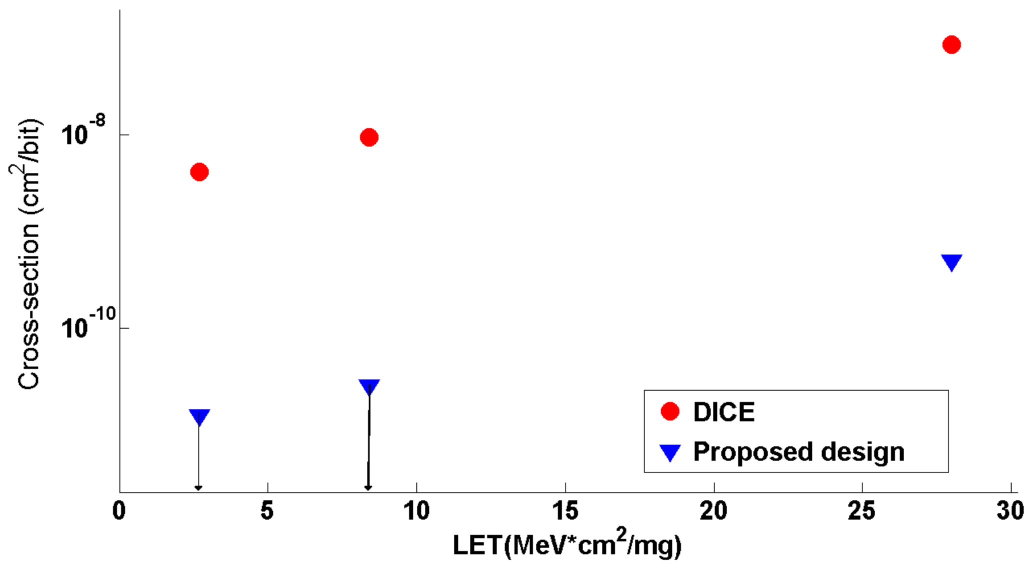
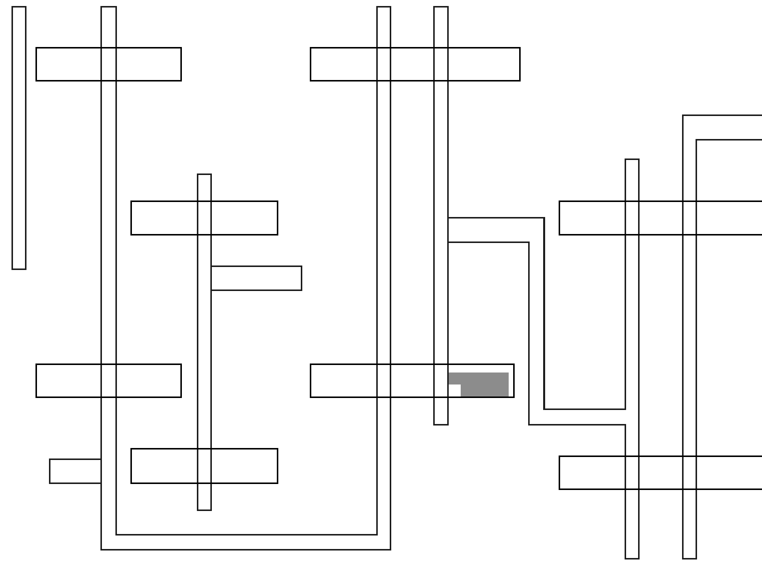


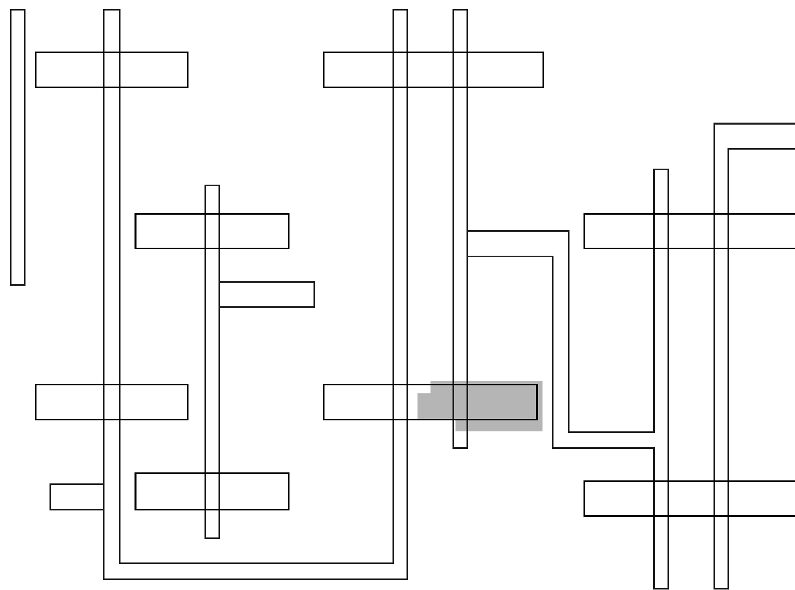
Figure III-10. Cross-section data of both DICE and the proposed design for normal strike with the clock frequency of 1 MHz and all 0s as the input; the proposed design started to see SEU errors at 28MeV*cm^2/mg.

3.6 Discussions

Interestingly, our baseline DICE cell built in SR-style with NAND gates demonstrates a lower upset threshold when compared to designs built with INVs presented in [7][19]. The SR-generation circuit shown in Fig. 7 (c) is found to be susceptible to single event strikes. Because DICE is not immune to double node upsets, a 1 -> 0 SET pulse at the input signal (S or R) during the hold mode may still cause the latch to upset. The sensitivity map of this circuit obtained from Accuro simulations shown in Fig. 11 (a) demonstrates the sensitive areas for LET = 4 MeV*cm^2/mg. A particle with LET = 4 MeV*cm^2/mg that strikes a single transistor (e.g., the NMOS diffusion area of NAND1 or NAND2 used to generate S or R) may cause a negative SET at S (or R). The sensitivity map of this circuit for LET = 15 MeV*cm^2/mg illustrated in Fig. 11 (b) shows larger sensitive areas when compared to LET = 4 MeV*cm^2/mg. By contrast, any voltage glitch caused by striking a single transistor (N5, N6, N7, or N8) in the INV-style latch shown in Fig. 12 only affects one storage node (A, B, C or Q). This does not flip the cell at all. Hence, IC designers need to take into consideration the tradeoff between flexibility and SEU tolerance when using the NAND-style SR latch.



(a)



(b)

Figure III-11. The sensitivity maps of the SR-generation logic circuit used in the traditional DICE SR latch for (a) 4 MeV*cm^2/mg and (b) 15 MeV*cm^2/mg when Q=0 and D=0. Particles hitting the NMOS diffusion area causes a 1 -> 0 SET pulse on S and then flips Q. (Only poly lines and diffusion areas are illustrated).

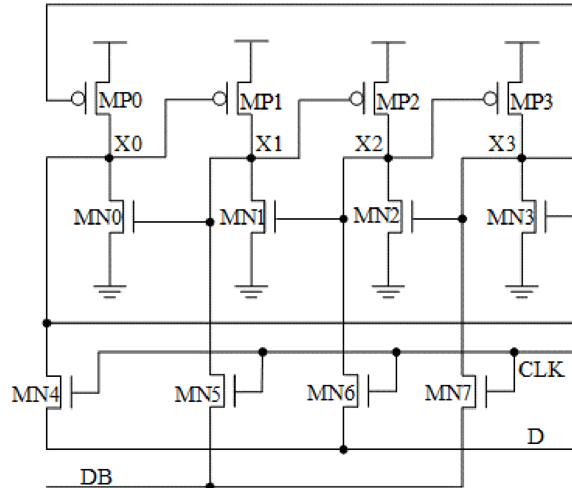
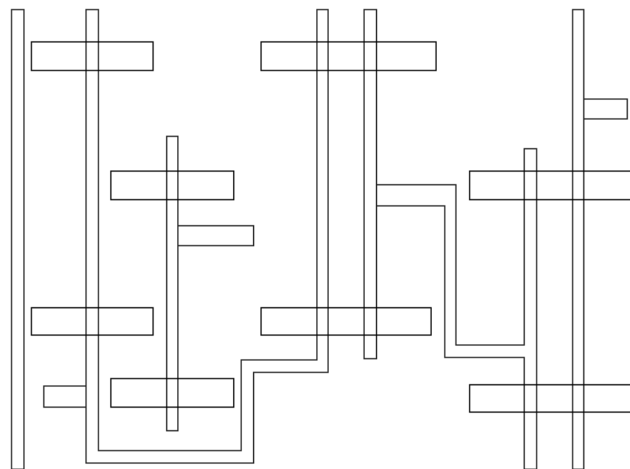
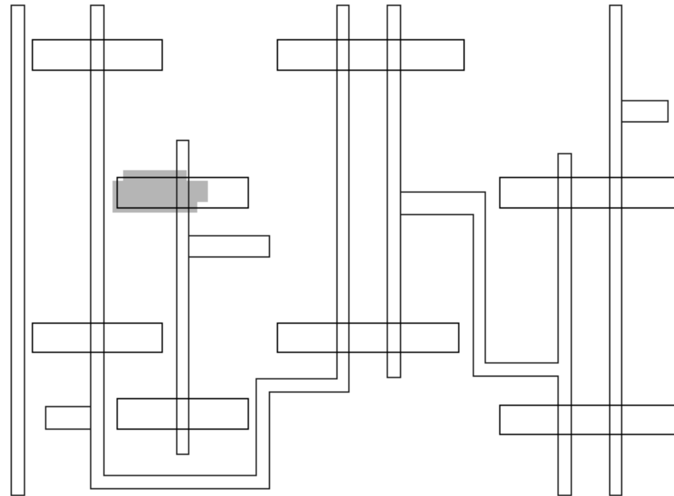


Figure III-12. The INV-based DICE structure [7] used in [11][19]. A strike on a single device (N5, N6, N7 or N8) may not upset the cell because the resultant SET pulse only affects one storage node and DICE is immune to single node upsets.

Input pattern dependency of the proposed design is simulated, albeit not tested. Fig. 13 compares the sensitivity map for constant 0s with that for 01 as the data input. As can be seen, the design has sensitive areas around the PMOS diffusion area (i.e., the transistor of INV2 used to generate NCLK) when the input is checkerboard. This is because striking INV2 may cause a 0 -> 1 SET pulse on NCLK and thereby result in a false write operation even in the nominal hold state. It is also noted that the proposed design is not susceptible to an SET pulse at S or R when the input is all 0s because this design is not sensitive to double node upsets.



(a)



(b)

Figure III-13. The sensitivity maps of the SR-generation logic circuit used in the proposed latch design when Q=0 and the input is (a) constant 0s, and (b) checkerboard (i.e., D transitions from 0 to 1 when the latch switches to or stays in the hold mode) for 15 MeV*cm^2/mg. (Only poly lines and diffusion areas are illustrated).

The SER of flip-flops has been demonstrated to be relatively independent on clock frequency [20]. This assumption holds true for static latch upsets (i.e., these SEU errors during the hold state). On the other hand, an SET pulse right before the clock transition may still get latched as an SEU error. The error rates of such latch upsets (transient latch upsets) are believed to increase with clock frequency [21]. Both DICE and the proposed design clearly show the frequency dependency of SEU errors.

The overall SEU rate is not only a function of particle LET values and clock frequency, but also a function of the orientation of incident particles [22]. The device sensitivity goes up as the tilt angle increases from 0^0 to grazing incidence [23]. As expected, both designs saw a higher SEU rate at the tilt angle of 50^0 vs. normal incidence.

Two storage nodes of the proposed design (A and C) are left floating in the hold state. Their states can be maintained because the subthreshold leakage current of N23, for example, is larger than the gate leakage of N3 [24]. Sophisticated Monte Carlo simulations across temperature (from -10^0C to 80^0C) and voltage (from the nominal core voltage 1.2V to a lower voltage 1V) have been performed to ensure the data integrity of the design. Functionality tests were also

carried out across the above temperature and voltage ranges, demonstrating the validity of the design.

The improved SEU performance of the proposed design comes along with design overhead in terms of power, delay and area cost. Due to the four extra transistors, the nominal area cost and power consumption increase by 33% and 26% respectively when compared to DICE. The increase in D-Q delay of the proposed design is ~5% due to the channel resistance of the blocking transistors when writing new data into the cell. Table III compares different figures of merit at different temperatures for both cells.

TABLE III-3 OVERHEAD COMPARISION

Temperature (^{0}C)	DICE		Proposed Design	
	D-Q Delay (ps)	Power Consumption (uW)	D-Q Delay (ps)	Power Consumption (uW)
0	135.3	0.46	137.8	0.63
25	142.5	0.52	145.7	0.65
50	148.3	0.54	152.9	0.67
75	153.5	0.55	160.1	0.67

3.7 Conclusions

We have presented a latch design that adds transistors in the feedback loops of the DICE cell. Fewer sensitive node pairs than DICE help reduce the single event susceptibility. The simulation, as well as, irradiation experimental results show that the proposed design has improved SEU tolerance at the expense of modest area, speed, and power penalties.

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IV. AN AREA EFFICIENT SEU-TOLERANT LATCH DESIGN

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In the previous chapter, the proposed design taking advantage of the traditional DICE and extra feedback transistors is presented and evaluated in terms of single event performance and system overhead of area, power, and delay. This design shows a much higher upset LET threshold and reduced cross-section at different clock frequencies and incident angles of heavy ions. It is worth noting that this design has four more transistors than DICE. Because of this, its area, power, and delay also increases. ASIC designers need to take into consideration the tradeoff between overhead and single event resilience.

In this manuscript, an area efficient design is proposed. It is based on Quatro, a CVSL-style structure. Quatro has two fewer transistors than DICE, thereby presenting itself as an area and power efficient alternative to DICE. However, Quatro is not tolerant to single node hit. Specifically, if an internal node of Quatro is struck, the cell will upset. The proposed structure is designed to eliminate this issue by adding two small feedback transistors. These extra transistors block these feedbacks, and therefore, hitting any one of the internal nodes does not result in upsetting the cell. Because these feedback transistors are turned ON when the cell is in the write mode, there is no significantly write delay introduced. Both simulation and heavy ion experimental results show the cell's better single event upset tolerance compared with Quatro. Its fewer transistors than DICE and the proposed DICE design in the previous chapter make the modified Quatro design appealing from the aspects of power, area, and delay.

AN AREA EFFICIENT SEU-TOLERANT LATCH DESIGN

Wang, H.-B.; Bi, J.-S.; Li, M.-L.; Chen, L.; Liu, R.; Li, Y.-Q.; He, A.-L.; Guo, G.

Abstract

This paper presents a new SEU-tolerant latch design based on Quatro and NMOS feedback transistors. By using these feedback transistors, the SEU susceptibility is decreased because of the cutoff feedback loop. Simulation results demonstrate that the proposed design is immune to static single node upsets. The proposed latch and the reference Quatro were designed and fabricated on a 130nm process. The test chip was exposed to heavy ions at the TAMU Cyclotron facility. The testing results show that the proposed design has a higher upset LET threshold and lower cross-section when compared to the reference latch. Its lower SEU vulnerability comes with small area penalty.

Index terms

Charge sharing, Quatro, radiation hardening, single event upset, soft error.

4.1 Introduction

A single event upset (SEU) is a particle-induced soft error in a sequential circuit element or storage cell of any micro-electronics device [1],[2],[3]. Fig. 1 shows the core structure of a typical latch - a back-to-back inverter loop. If the current induced by the ion hit on the NMOS drain is large enough and exceeds the drive capability of the on PMOS transistor, the voltage perturbation at the struck node can propagate to the opposite inverter and cause an upset of the cell state through the positive feedback, which is referred to as an SEU.

Although these types of soft errors can be mitigated by refreshing the corrupted data, SEU mitigation techniques, such as Radiation Hardening by Design (RHBD) approaches, are still

required to reduce soft error rates and ensure data integrity. A wide spectrum of Error Correction Codes (ECCs) is used in memory structures, but ECCs introduce extra delays in the path of write data and read data [4]. Hardware redundancy, the duplication of critical components in a system, for instance, Triple Module Redundancy (TMR) or temporal hardening, increases the reliability of the system [4],[5],[6], but the area efficiency is very low. In addition, the layout-based hardening approaches include, but are not limited to, physically spacing sensitive nodes [7],[8], use of high-density well contacts [9],[10], and charge cancellation through Layout Design through Error-Aware Transistor Positioning (LEAP) [11]. However, the layout techniques generally require large area to implement.

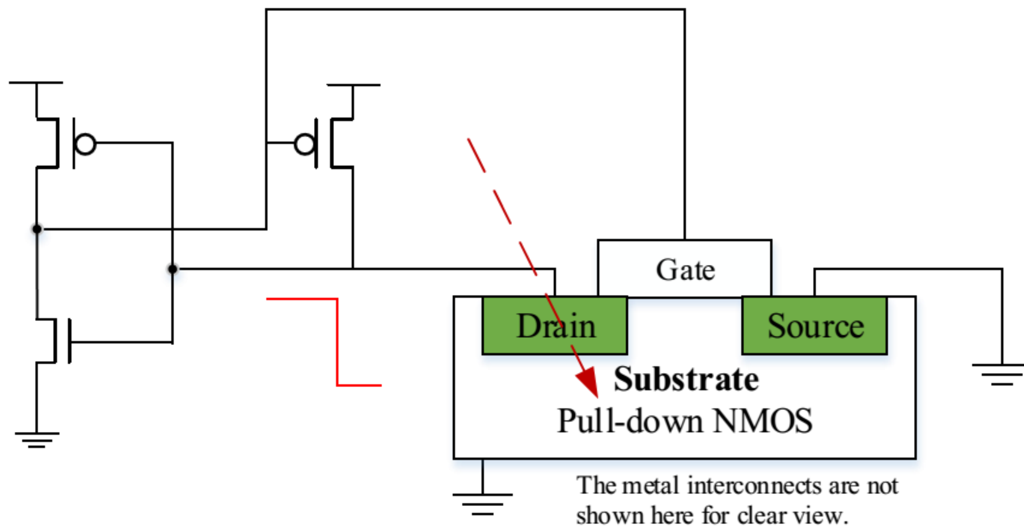
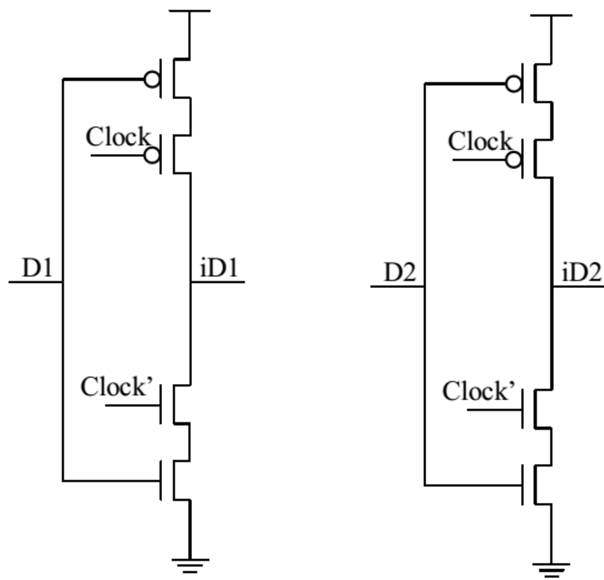


Figure IV-1. Mechanism of an SEU in a back-to-back inverter loop.

The SEU-tolerant storage cells with small area overhead are preferred by designers. Although Dual Interlock Storage Cell (DICE), a latch consisting of four interlocked inverters, has been widely used to mitigate SEU errors [12], the SEU hardness is achieved at the expense of doubled transistor counts compared with the 6T memory cell. This makes DICE design less attractive for applications where compact layout is critical such as SRAMs. Jahinuzzaman et al. introduced the 10T-Quatro cell, which uses fewer transistors compared with DICE [13]. This design reduces power by ~40% and layout area by ~30% compared with those of DICE [14]. However, the issue of Quatro is that it may still upset even if only one node is hit during the Hold mode in some cases [13].



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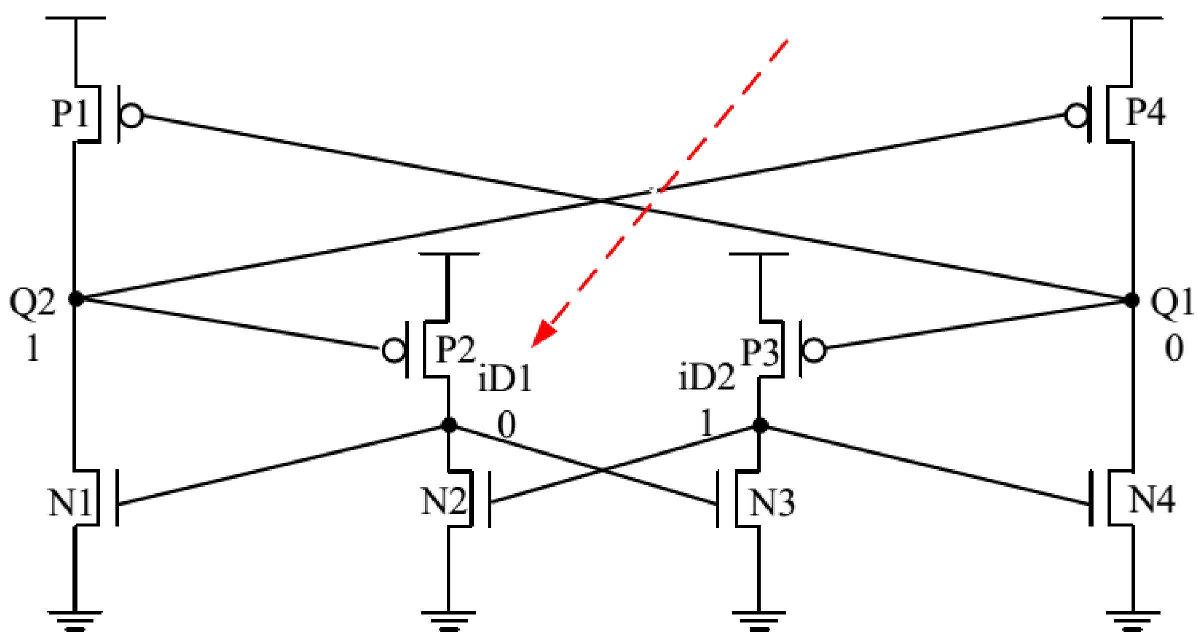


(b)

Figure IV-2. The Quatro latch structure consisting of (a) tri-state inverter transfer gates and (b) Quatro cell [13]. The differential inputs are D1 and D2; the differential outputs are Q1 and Q2.

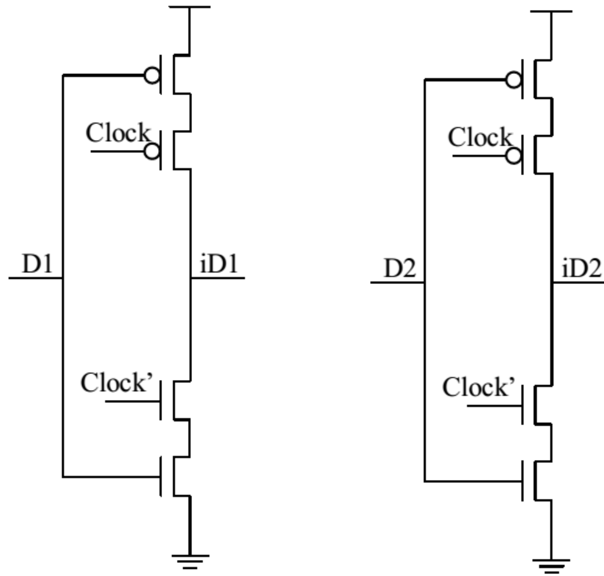
In this paper, we present the design of a new latch based on Quatro, where two extra NMOS transistors controlled by the clock signal are introduced to block the feedback paths during the Hold state. This design has single node upset immunity in the Hold mode and improved SEU hardness with small area overhead. The rest of the paper is organized as follows: Section II presents the proposed design to address the single node upset issue and demonstrates the principles of operation; Section III shows SPICE and Technology Computer Aided Design (TCAD) simulation results to illustrate the effectiveness of the design in mitigating SEUs and compares simulation results of power consumption and delay among Quatro, DICE and the proposed design; Section IV presents the test chip design in a 130nm CMOS bulk technology and functionality test; and Section V presents the experimental results obtained from heavy ion test.

4.2 Proposed Design

The original Quatro latch, the structure of which is shown in Fig. 2, is a Cascode Voltage Switch Logic (CVSL)-style circuit and has four storage nodes Q1, Q2, iD1 and iD2. It is not immune to single node upsets in the Hold state. For instance, assume the logic values of nodes Q1, Q2, iD1 and iD2 are 0, 1, 0 and 1, respectively, as shown in Fig. 2 (b). If the transistor P2 is struck by an ion particle, the voltage of its drain iD1 would rise, and as a result, the transistors N1 and N3 may be turned on. This may lead to a cascade of pulling down and flipping the voltage of node Q2, and pulling up and flipping the voltage of node Q1. Although the cell's SEU tolerance can be improved by increasing the width of these driver transistors N2 and N3, extra area cost will be introduced inevitably [13].

The proposed design is illustrated in Fig. 3. Like the original design, it is a CVSL-style circuit and has two pairs of differential-input differential-output inverters. However, it has two extra NMOS transistors; N12 and N34 are added in the feedback loops. N12 is placed between the gate of N1 (node iD1L) and node iD1, while N34 is placed between the gate of N4 (node iD2R) and node iD2. The gates of these extra NMOS transistors are connected to Clock'. The design has two internal storage nodes (iD1 and iD2) and two output nodes (Q1 and Q2).

During a write operation, Clock is Low, Clock' is High, the blocking transistors N12 and N34 are turned on. The cell behaves like an original Quatro cell except for additional resistance added to the paths.



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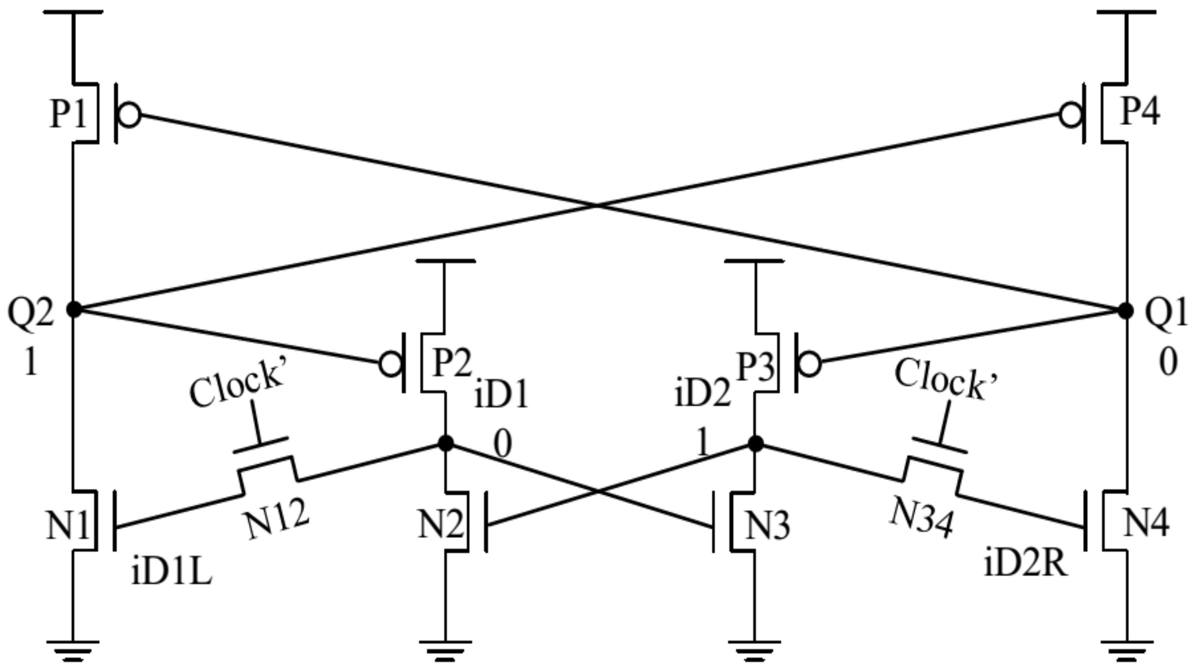


(b)

Figure IV-3. The proposed latch structure consisting of (a) tri-state inverter transfer gates and (b) Quatro variant which has two extra NMOS devices. The differential inputs are D1 and D2; the differential output nodes are Q1 and Q2; and the two internal storage nodes are iD1 and iD2.

During a Hold mode, Clock is High, Clock' is Low, the blocking transistors N12 and N34 are turned off, thus, iD1L and iD2R are left floating. However, the voltages of these two nodes are able to be maintained by using subthreshold leakage currents [15]. For example, assume that iD1L is logic High initially and left floating after N12 is turned off. As long as the subthreshold leakage of N12 is larger than the gate leakage of N1, iD1L can still maintain its voltage.

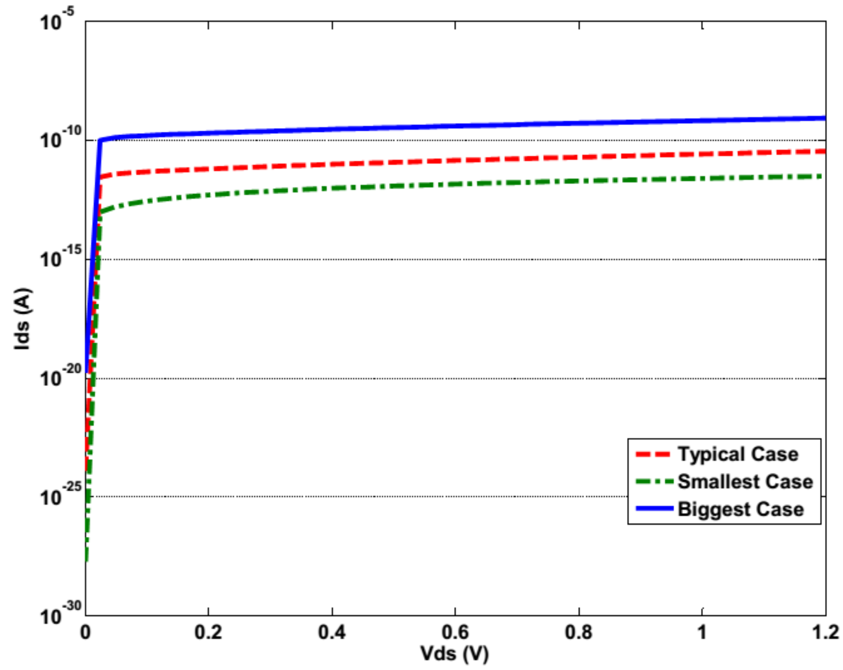
4.3 Simulation Results and Overhead Evaluation

4.3.1 Data Integrity Simulations

As mentioned in the last section, the states of the floating nodes (iD1L and iD2R) depend on subthreshold leakage currents. Since the subthreshold leakage increases exponentially with temperature and the gate leakage shows weak temperature dependency [16], sophisticated Monte Carlo simulations covering process variation and mismatch have been performed on a Regular Threshold (RVT) NMOS feedback device whose width is 0.28 um at 0 ^{o}C to simulate data integrity at low temperatures.

Fig. 4 shows that the smallest and largest drain leakages may vary for up to two orders at 0 ^{o}C. The zoomed-in IV curve shown in Fig. 4(b) demonstrates that even in the worst case, when the drain-source voltage is 70mV, the subthreshold leakage equals the biggest gate leakage (0.25pA) of a 0.68 um RVT NMOS used as a pull-down NMOS transistor in our design. Take iD1L with the initial value as logic High as an example again, the node voltage may drop because of the gate leakage of N1, however, once the voltage goes down for more than 70mV, the drain leakage of the blocking transistor N12 will try to pull this node voltage back. Therefore, even if the value of the floating nodes may be degraded, they can still be recovered.

However, the gate leakage increases with technology scaling. It may become comparable to the subthreshold leakage in some sub-100nm technology nodes. As a result, the state of the cell may not be able to be maintained at very low clock speed; and other techniques should be used to increase the subthreshold leakage, for instance, by biasing and tuning physical parameters (W, L, etc.).



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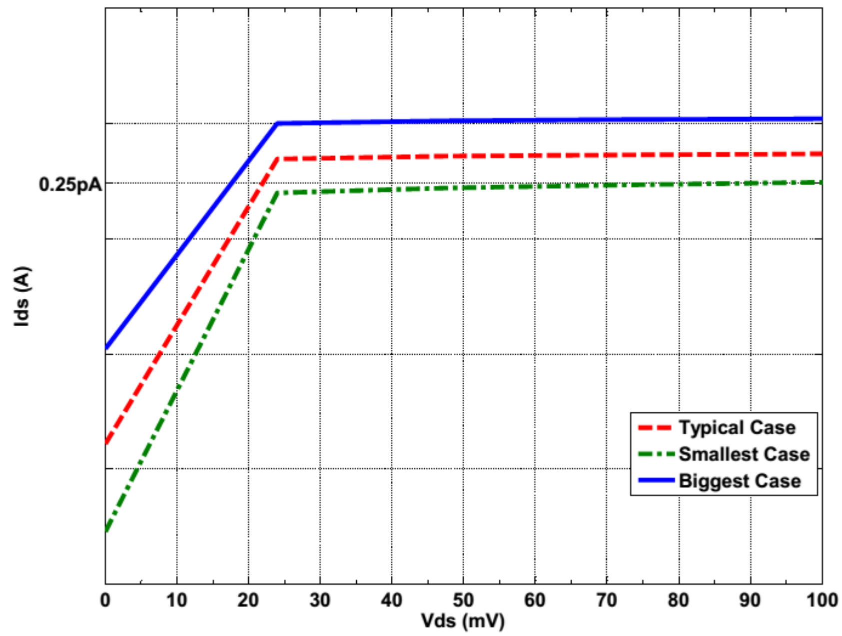


(b)

Figure IV-4. (a) The subthreshold leakages for a 0.28 um RVT NMOS feedback device used in our design obtained from 5000 Monte Carlo simulation runs at 0 ºC; (b) the zoomed-in IV curve.

4.3.2 SEU Simulations

Single Node Upsets Simulation

The current pulse induced by heavy ion particle strike on the drain node of a transistor can be modeled as a double exponential function given by

$$I_{inj}(t) = I_0\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right)$$

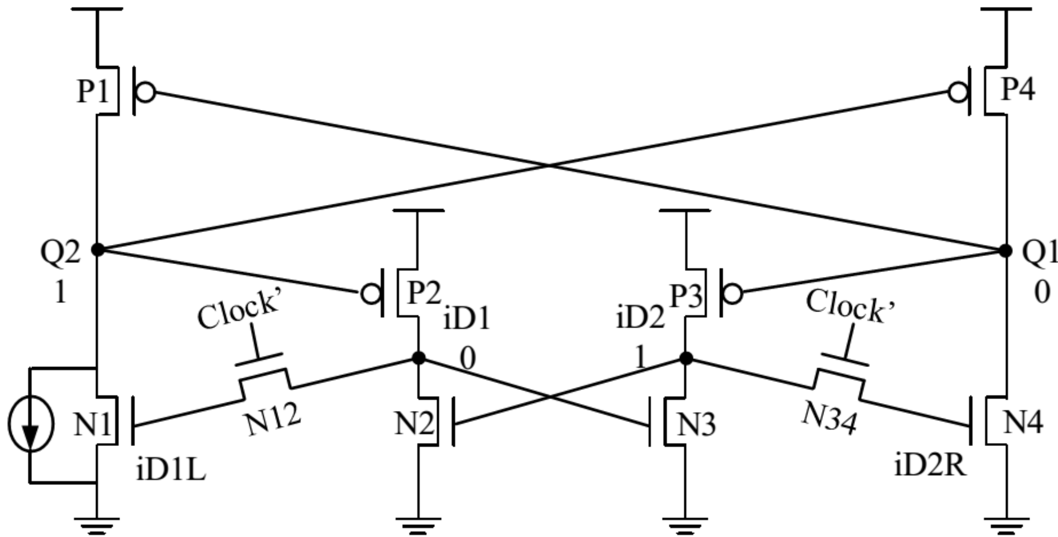
I_0 is the maximum current and can be expressed as $Q/(\tau_\alpha - \tau_\beta)$, where Q is the amount of deposited charge, τ_α is the collection time constant of the junction, and τ_β is the ion track establishment time constant [17].

In this paper, this current pulse with τ_β of 50ps and τ_α of 200ps is applied.

When the cell is in the Hold state, the blocking transistors are turned off. Assume the logic values of nodes Q1, Q2, iD1 & iD2 are 0, 1, 0 & 1, respectively. Four scenarios that might cause SEUs have been simulated to investigate the effectiveness of the design's hardness.

Case 1: a negative transient at node Q2

If N1 is struck, this negatvie pulse on Q2 will not flip Q1 because N4 has stronger drive capability than P4. Likewise, iD1 will not flip because N2 has stronger drive capability than P2. The simulation test bench and waveforms are shown in Fig. 5.



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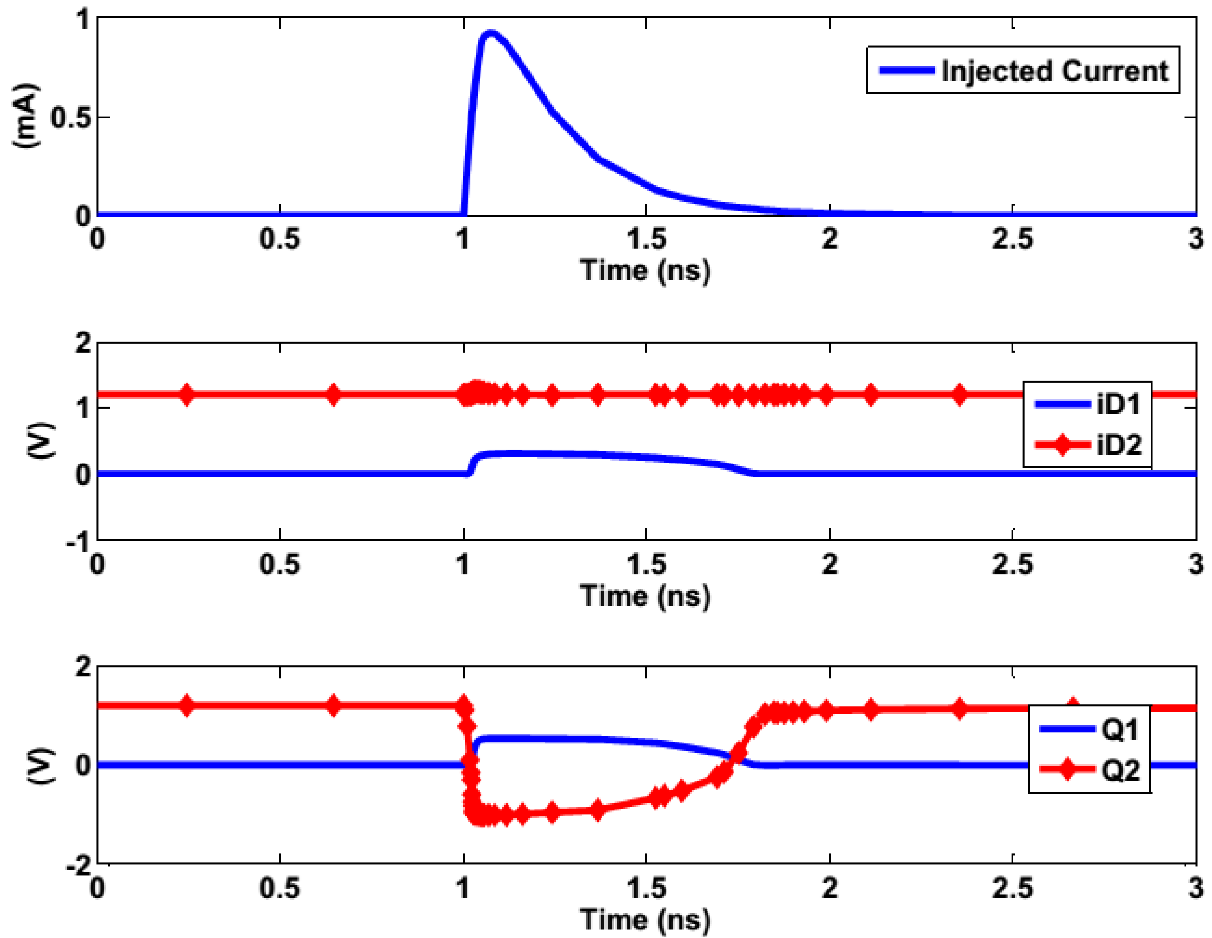


(b)

Figure IV-5. (a) Striking N1 by an ion particle is simulated by injecting a double exponential current with τ_β of 50 ps and τ_α of 200 ps at node Q2 in SPICE when Q1 & iD1 = 0, Q2 & iD2 = 1; (b) the waveforms of the injected current, nodes iD1 & iD2, nodes Q1 & Q2 from top to bottom.

Case 2: a positive transient at node iD1

If P2 is struck, iD1 may flip and lead to a cascade of switching on N3 & flipping iD2. However, the erroneous iD1 & iD2 will not propagate to Q2 & Q1 because N12 blocks the connection between iD1 and the gate of N1, and N34 blocks the connection between iD2 and the gate of N4. Therefore, the output nodes of the latch, Q1 and Q2, remain unaffected. This is illustrated in Fig. 6. The recovery speed of the internal nodes iD2 and iD1 depends on the ratio of the drive strength of P3 vs. that of N3. The larger the ratio, the faster the recovery speed. Similarly,

if iD1 and iD2 are initially 1 and 0 and they see negative and positive SETs respectively, the recovery speed depends on the ratio of the drive strength of P2 vs. that of N2.

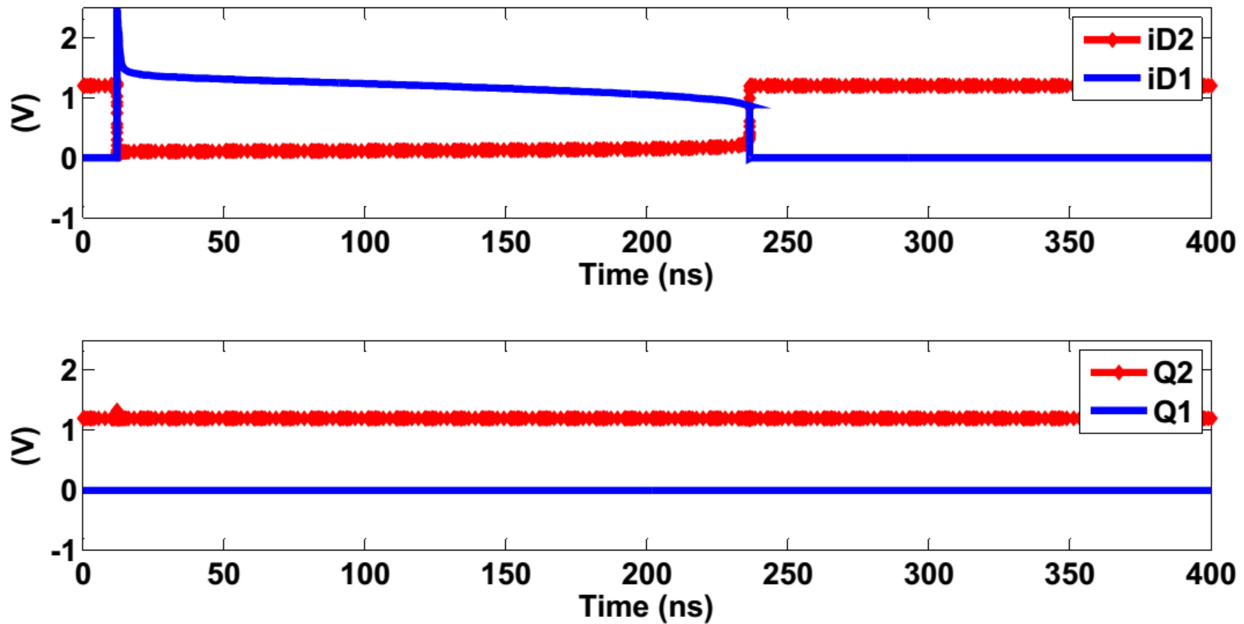


Figure IV-6. SPICE simulation results of striking P2 by injecting 807fC charge when Q1 & iD1 = 0, Q2 & iD2 = 1; the waveforms of nodes iD1 & iD2, nodes Q1 & Q2 from top to bottom.

Case 3: a negative transient at node iD1L

The benefit of the proposed design is the cell does not upset even if one of the blocking NMOS transistors is hit because the blocking transistors will not turn on their adjacent NMOS devices. For example, if node iD1L is hit, the node voltage will go down, but its adjacent NMOS device N1 will not be turned on.

Case 4: a negative transient at node iD2R

If the blocking transistor N34 is hit when iD2 =1, the SET pulse will not turn on its adjacent transistor N4. Although the voltage of iD2R cannot be recovered from the hit immediately, the other four nodes (Q1, Q2, iD1 and iD2) remain their correct values, as shown in Fig. 7.

Q1 is left floating in this case and its voltage might get pulled up because of the leakage current of P4. However, the large voltage difference across N34 makes it leak larger currents thereby helping to restore iD2R and then Q1. The larger drive capability of N4 leads to a even faster recovery speed of Q1. Eventually the internal node iD2R will recover with Q1 not getting

degraded. On the other hand, for high speed applications, iD2R keeps being loaded with new data in the succeeding clock cycles. By reducing the size of blocking transistors, the probability of hitting them is very low, and the occurrence of this case is expected to be very rare.

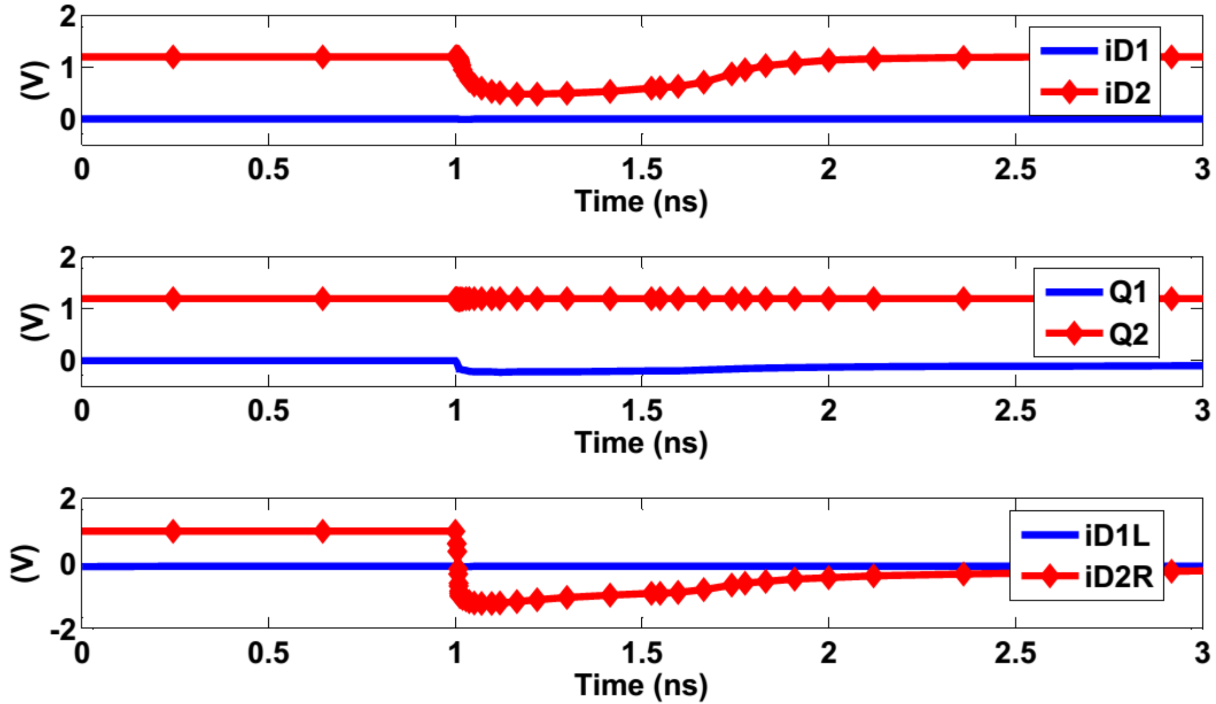


Figure IV-7. SPICE simulation results of striking N34 by injecting 403fC charge when Q1 & iD1 = 0, Q2 & iD2 = 1; the waveforms of nodes iD1 & iD2, nodes Q1 & Q2 from top to bottom.

It is noted that in Quatro and the proposed design, an SET pulse just prior to the clock transition may get latched as an SEU error, which is referred to as a transient latch upset. These types of errors show clock frequency dependence [18]. As the frequency increases, it contributes to an increase in soft error rates.

Multiple Node Upsets Simulation

A single ion hit may cause charge sharing between adjacent devices and even upset hardened designs that are virtually immune to single node charge collection [7][19]. The SEU rate is not only a function of LET, but also a function of the tilt angle ɵ and the rotation angle ϕ. The SEU rate over the tilt angles peaks at grazing incidence [20].

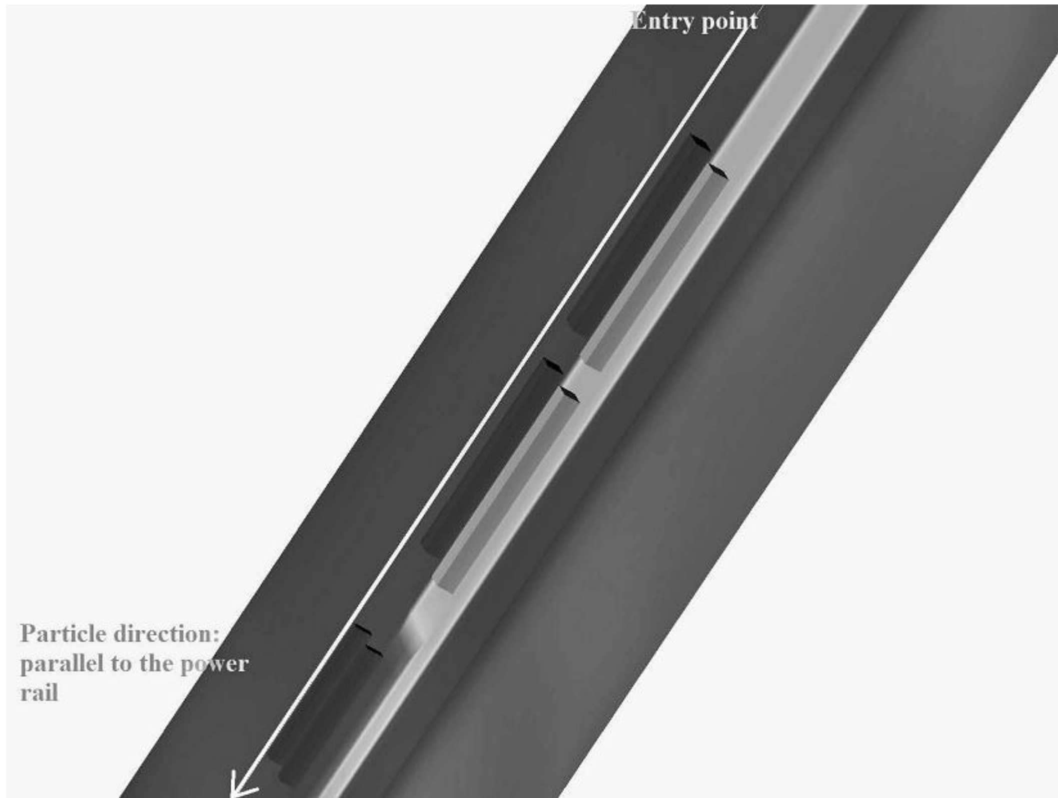


Figure IV-8. The 3D layout structure of the proposed design imported to Accuro for analysis and the trace of a heavy ion particle with (ɵ, ϕ) of (90°, 0°). ɵ is the tilt angle and ϕ is the rotation angle.

In order to analyze charge sharing effects on the proposed design, Accuro, a TCAD tool suite from Robust Chip Inc., has been used to simulate particles coming from grazing angles. This software constructs a full 3D representation of the design by reading in its layout file, and applies 3D transport simulation to describe the charge generation and transport [21]. It is capable of plotting sensitivity maps which visualize cross-section regions on top of the layout. Fig. 8 demonstrates the 3D structure of the proposed design and the trace of the incoming particle with (ɵ, ϕ) of (90°, 0°), which corresponds to the direction parallel to the power rails.

Quatro is susceptible to multiple node upsets, especially when the two nodes of the same logic level are hit [13]. Fig. 9 shows the simulation waveforms in Accuro. Fig. 10 (a) demonstrates that a particle of LET = 4 MeV*cm^2/mg traversing through the diffusion areas of these NMOS devices in Quatro is able to upset the cell. Fig. 11 (a) shows a particle of LET = 20 MeV*cm^2/mg going through either PMOS or NMOS devices flips the state of the cell.

By contrast, the proposed design does not upset at LET = 4 MeV*cm^2/mg as illustrated in Fig. 10. Its sensitive region is ~2-3X smaller than that of Quatro at LET = 20 MeV*cm^2/mg as illustrated in Fig. 11 (b). The proposed design shows improvement in hardening against PMOS hits. As illustrated in Fig. 12, although Q2 and iD2 flip, they can still recover from hit. The blocked paths prevent erroneous iD2 and iD1 from propogating. The recovery speed of them is determined by the drive capability of P3(P2) vs. that of N3(N2), as discussed in previous sections.

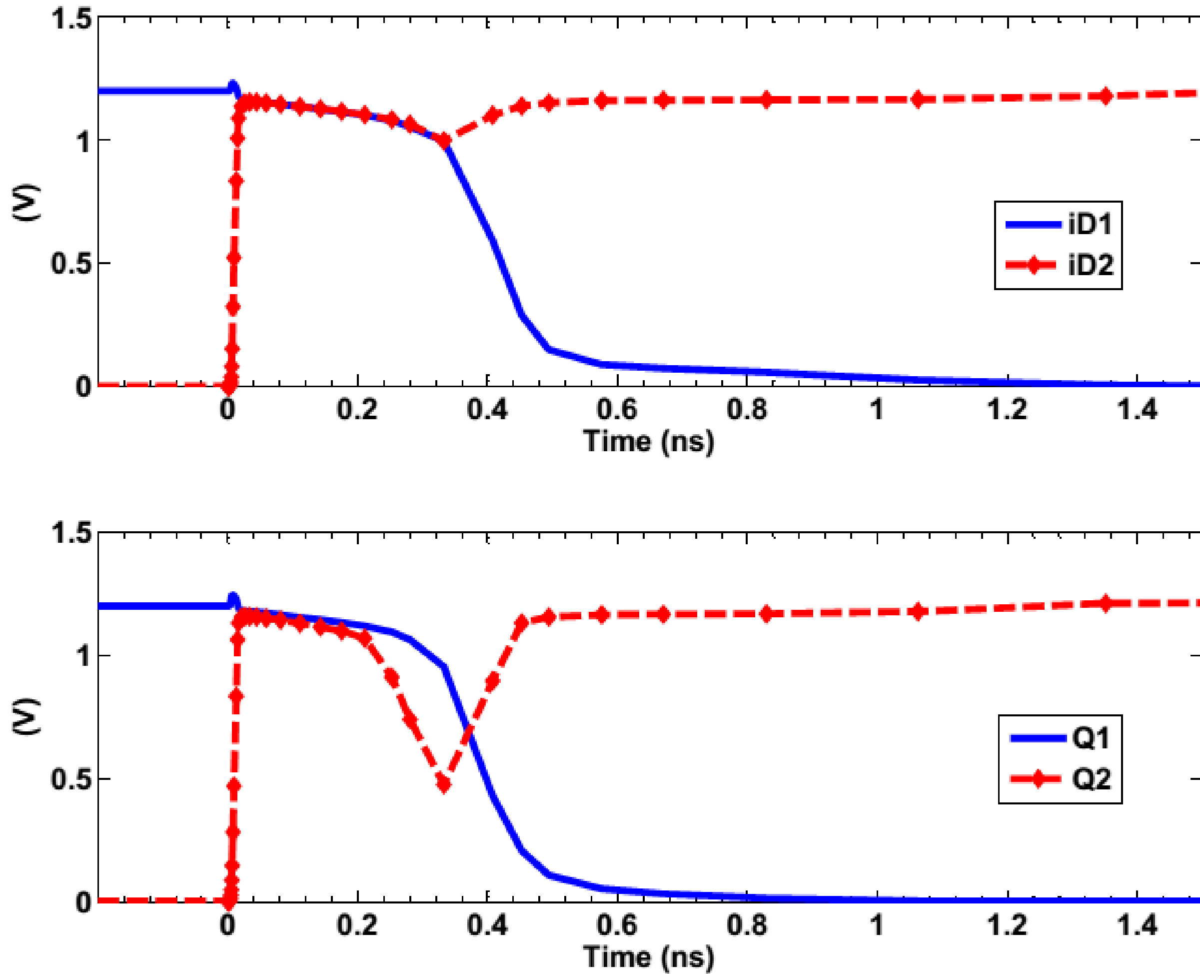
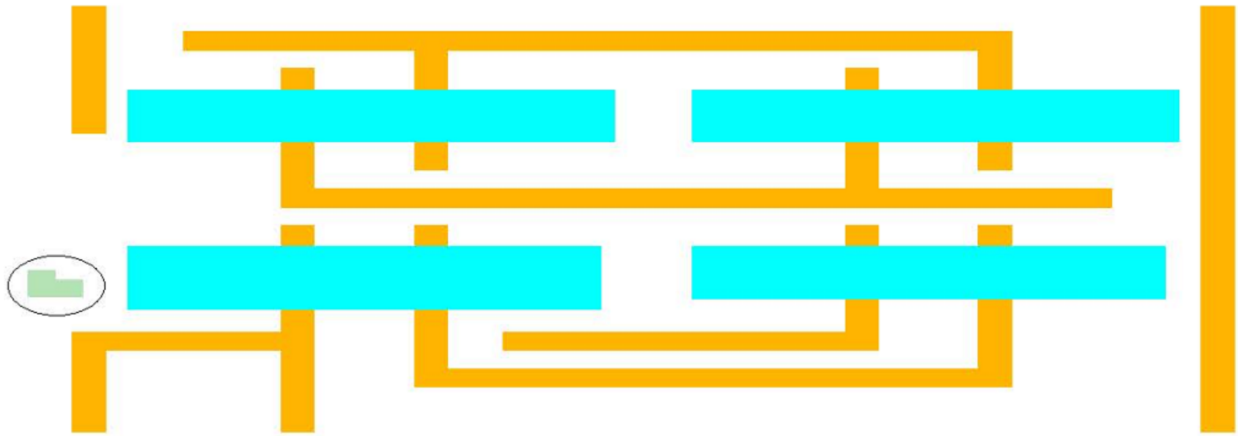


Figure IV-9. Accuro simulation results of striking all the PMOS devices of Quatro by an ion particle of 20 MeV*cm^2/mg and (ɵ, ϕ) of (90°, 0°).



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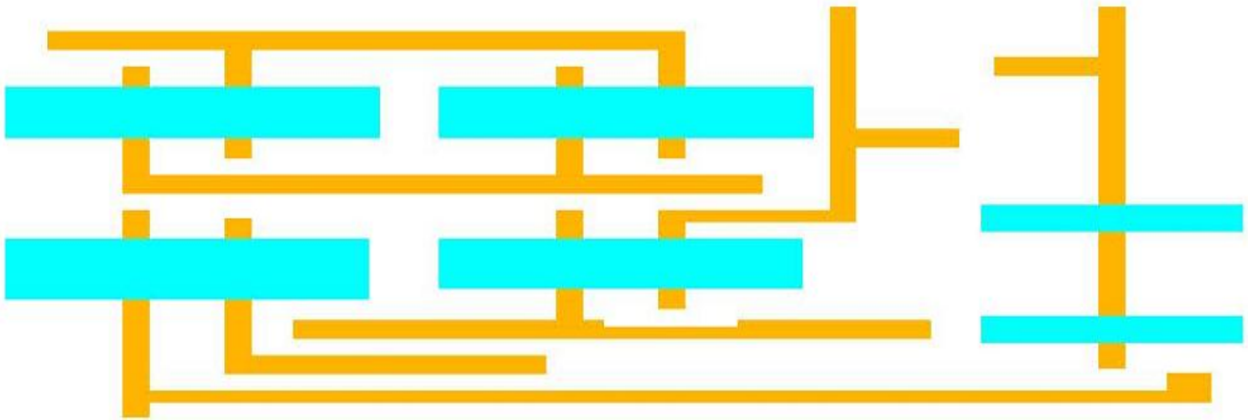
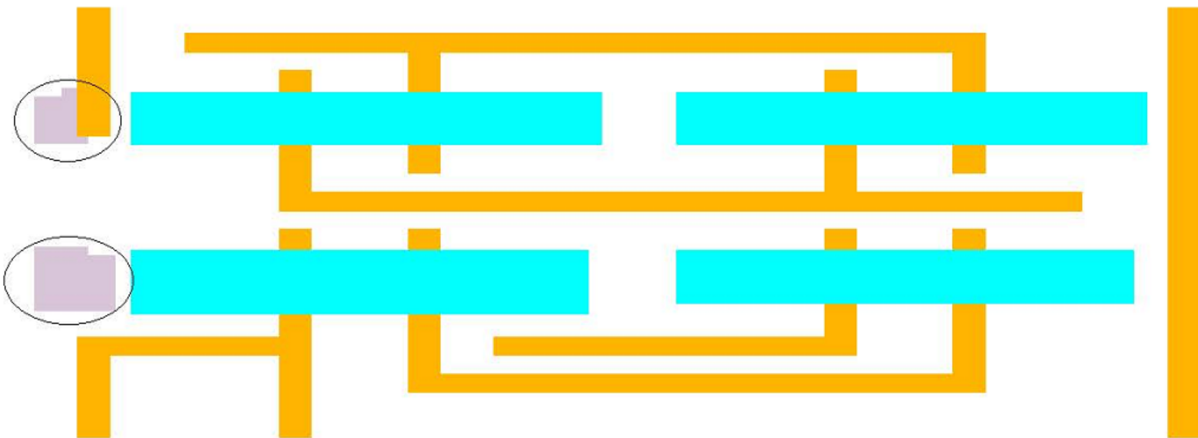


(b)

Figure IV-10. Sensitivity maps of (a) the reference Quatro and (b) the proposed design for 4 MeV*cm^2/mg and (ɵ, ϕ) of (90°, 0°). The sensitive regions are circled in the figure. A particle of this LET that falls in these regions will upset the design.



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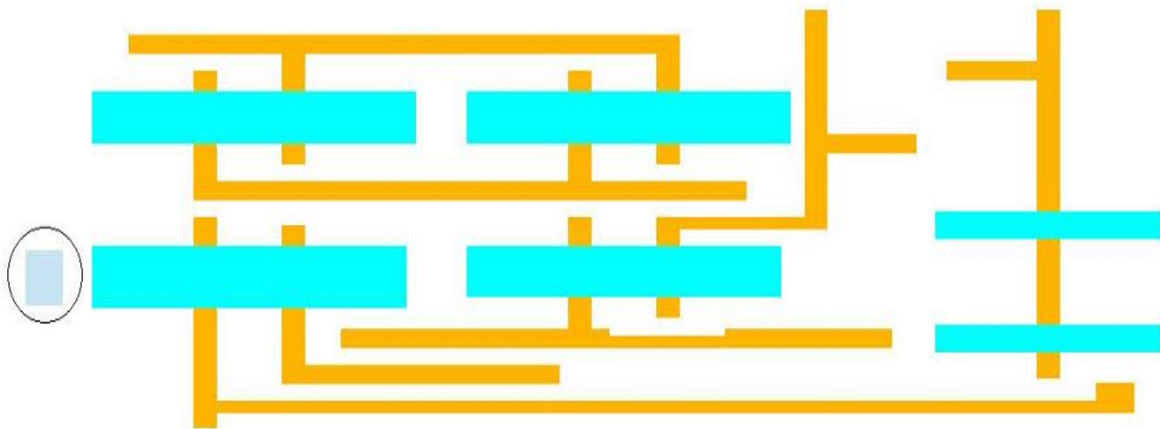


(b)

Figure IV-11. Sensitivity maps of (a) the reference Quatro and (b) the proposed design for 20 MeV*cm^2/mg and (ɵ, ϕ) of (90º, 0º). The sensitive regions are circled in the figure. A particle of this LET that falls in these regions will upset the design.

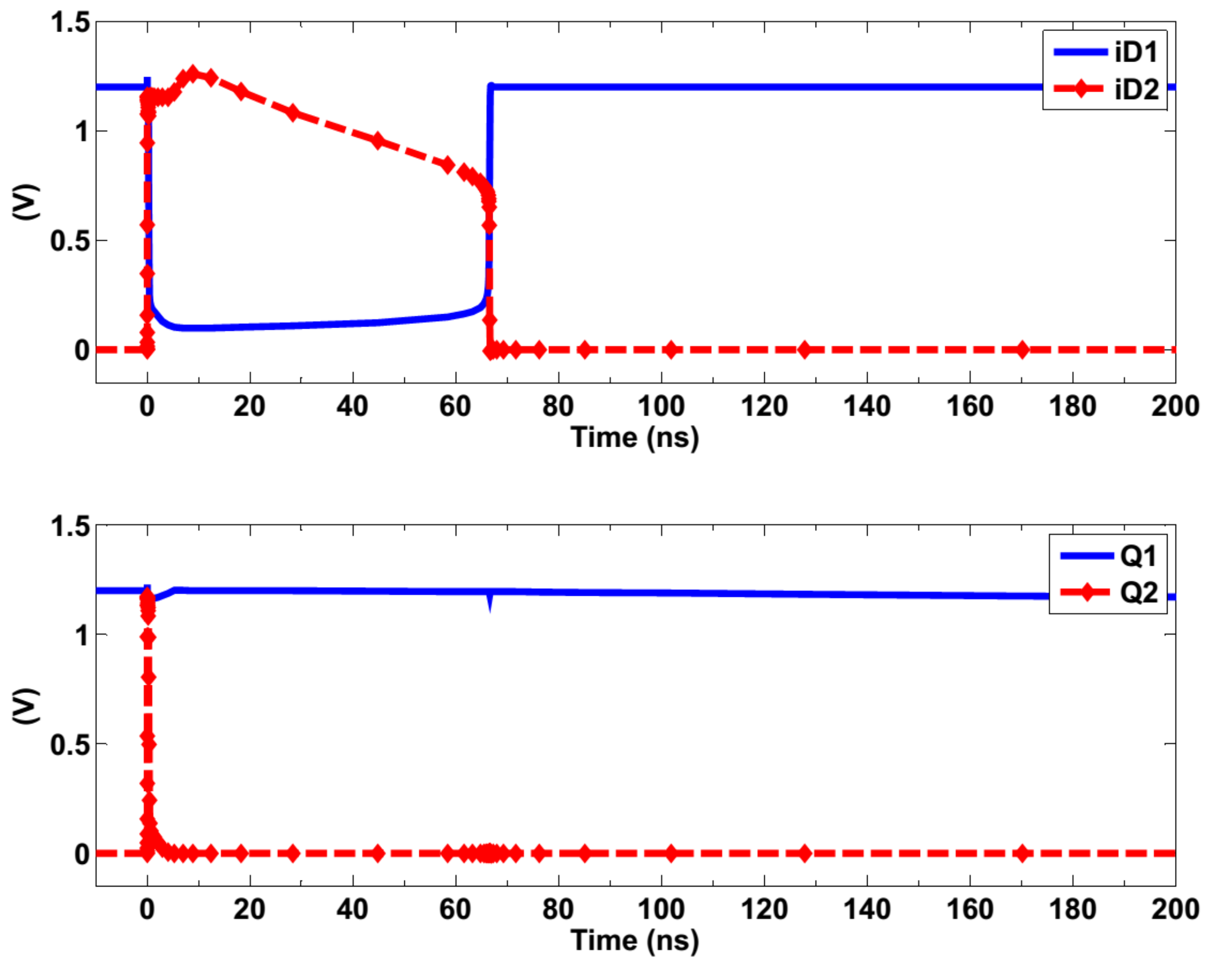


Figure IV-12. Accuro simulation results of striking all the PMOS devices of the proposed design by an ion particle of 20 MeV*cm^2/mg and (ɵ, ɸ) of (90°, 0°).

Overhead Evaluation

Compared with the original Quatro design, the proposed latch introduces some penalties in area, power, and performance. Table I lists the ratio of all these parameters of the proposed design versus those of Quatro and DICE.

Since two more transistors are added to the reference latch, the nominal area increase of this proposed design could be 25%. However, the actual area increase is only about 10% by using smaller transistors. The total area is expected to be reduced further if compact layout techniques are applied.

The extra two blocking transistors also result in approximately 50% increase in both power and delay of the proposed latch. The delay penalty mainly comes from the blocking transistors' resistance which makes the writing data process slower. Likewise, due to the two extra transistors, the power dissipation of the proposed design increases by 50% compared with Quatro as well.

TABEL IV-1 RELATIVE PERFORMANCE COMPARISON

	Original Quatro	DICE	Proposed design
Area	1	1.20	1.11
Delay	1	1.28	1.50
Power	1	1.31	1.50

4.4 Test Chip Design and Functionality Test

The proposed design and the reference Quatro cell were fabricated in a 130nm bulk CMOS technology. 792 stages of original Quatro flip-flops (FFs), each of which consists of a master latch and a slave latch, are connected in a shift register fashion, as shown in Fig. 14. The proposed design is connected as a shift register in the same manner as well. Both of these two shift registers take the same Clock signal (labelled as Clock_In) and data input (labelled as D1) from the outside of the chip. The other data input D2 is generated before going into the register chains inside the chip by an inverter whose input is D1.

As shown in Fig. 14, data travel through the registers in one direction, while Clock propagates to each FF in the reverse direction. This is referred to as the reverse clocking scheme. In this scheme, a delay is purposefully inserted to the clock of each preceding FF. Therefore, the subsequent FF will receive the active-clock edge before the preceding FF. Using the reverse clocking scheme can get around hold violation and clock skew issues, although this is achieved at the expense of setup time.

The IC was tested in a temperature-controlled chamber with the temperature ranging from -10 to 80 ^{o}C and the voltage ranging from the nominal core voltage (1.2V) to a lower voltage (1V), as shown in Fig. 13. The register chains were clocked at 10 kHz. No errors were captured. The test chip showed full functionality across tempeature and voltage.

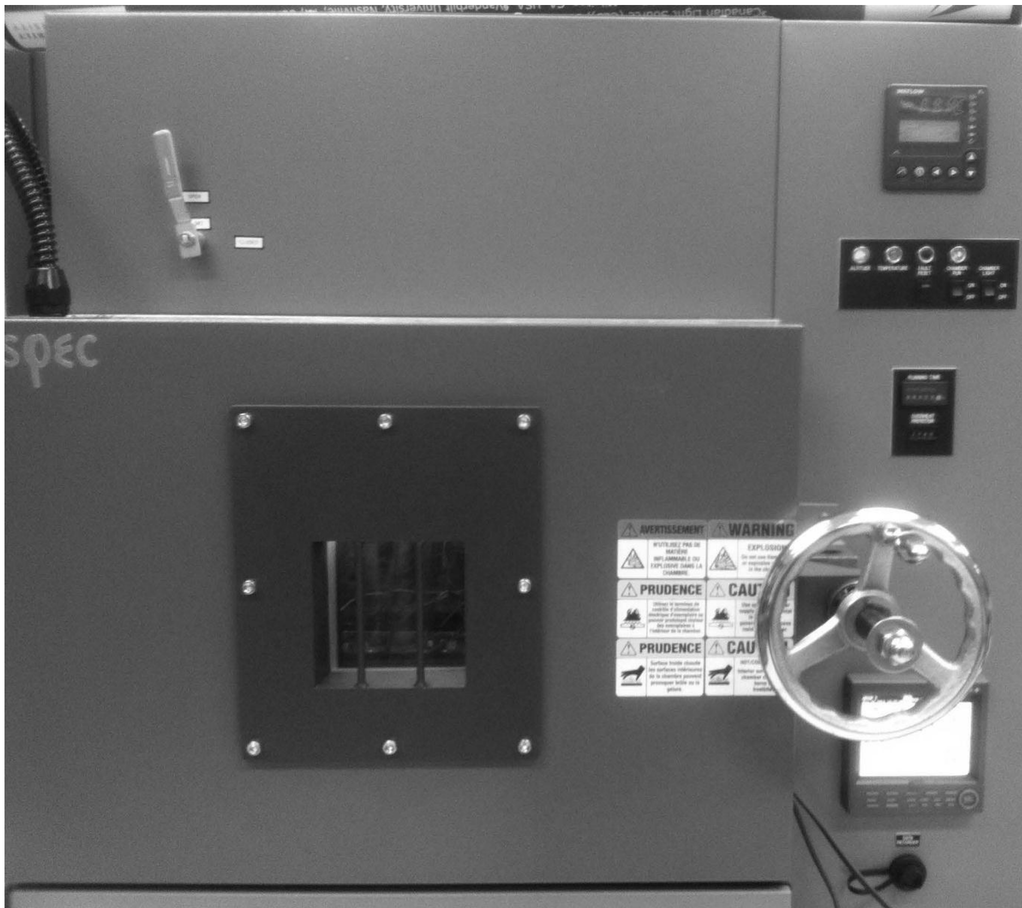
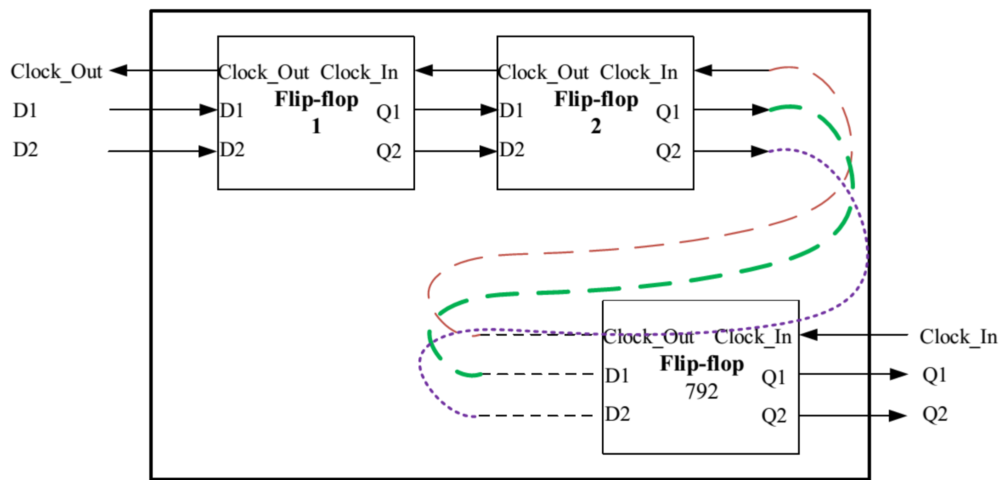
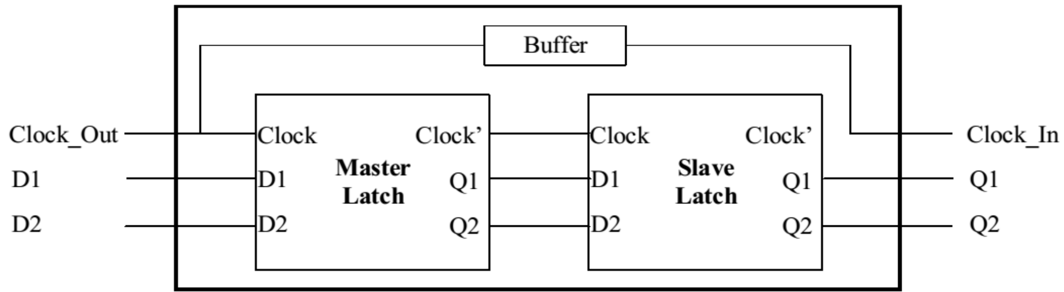


Figure IV-13. The temperature-controlled chamber was used to test the funcionality of the design at temperatures from -10 to 80 ^{0}C. The IC and the testing motherboard were placed inside the chamber.



(a)



(b)

Figure IV-14. (a) Block diagram of the shift register chain in the test chip; (b) block diagram of each flip-flop design in the shift register chain.

4.5 Irradiation Experimental Results

The irradiation experiment was performed at the Cyclotron Institute of Texas A\&M University. During testing, the two flip-flop shift register chains were exposed to normal incident ion particles (N, Ne, Ar, K) with LET values ranging from 1.3 to 35 MeV*cm^2/mg.

The shift registers were fed with blanket 0s and 1s as the input patterns. The clock frequency of 10 kHz was used, and as a result, the transient-induced latch upsets (not those static upsets in the Hold mode) were reduced to a negligible level in both chains at this low frequency. The experimental data obtained from the heavy-ion testing is summarized in Table II.

Fig. 15 shows the cross-section curves of the reference cell and the proposed design. In this figure, since there were no errors recorded at 2.7 MeV*cm^2/mg and there were only 3 errors at 10 MeV*cm^2/mg, the proposed design had a much higher upset LET threshold (larger than 2.7 MeV*cm^2/mg. In addition, since the proposed design may not tolerant against multiple node upsets because of charge sharing effect, it started to show errors with high-LET ions. It exhibited nearly 5X improvement in terms of SEU errors when compared to the Quatro cell at the LET of 35 MeV*cm^2/mg. Experimental results demonstrated that the original Quatro was 4X better than DICE in cross-section [13]. Thus, it may be fair to conclude that the proposed design has superior hardness over DICE with similar area cost.

TABEL IV-2 HEAVY-ION TESTING RESULTS

LET (MeV*cm^2/mg)	Fluence	Traditional Quatro		Proposed Design	
		Errors	Cross section	Errors	Cross section
1.3	8.03E+8	33	4.71E-11	0	0
2.7	6.22E+8	193	3.85E-10	0	0
10	5.55E+8	1427	4.72E-09	3	6.58E-12
35	1.67E+8	3344	1.78E-08	685	3.44E-09

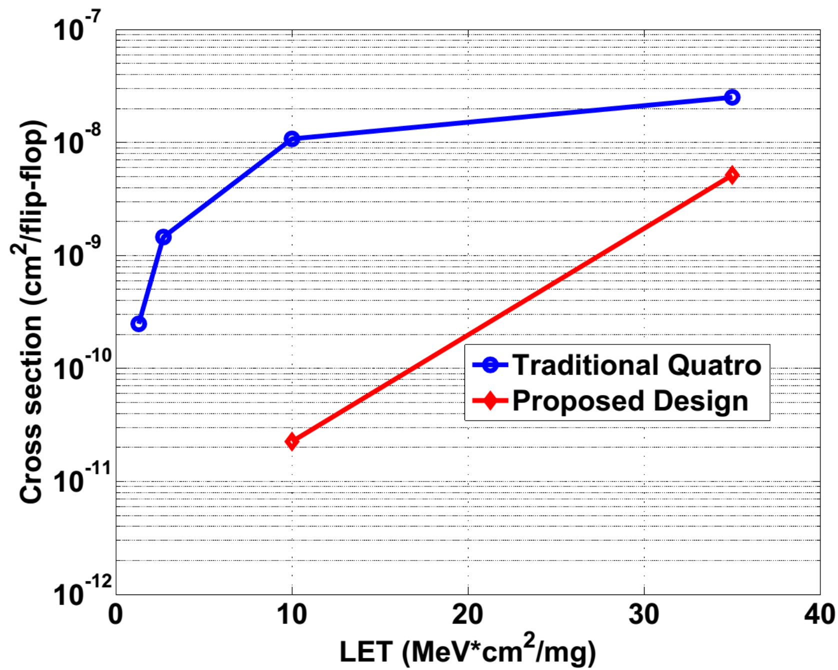


Figure IV-15. Cross-section curves of both Quatro and the proposed design exposed to normal incident particles.

4.6 Conclusions

The original Quatro latch has single node upset issues during the Hold mode in some scenarios. We have presented an area-efficient Quatro variant which adds two blocking NMOS transistors in the cell. These small transistors help the cell to recover to its correct state after any single node is struck by single event particles in the Hold state.

Circuit simulations demonstrate that the proposed design is immune to single node upsets in the Hold mode and it has improved hardness against particles coming from grazing angles. Exposure to normal incident heavy ion particles at the Cyclotron Institute of Texas A&M University illustrates that the proposed design demonstrates at least 5X more hardness than the original Quatro design for the experiments conducted. The small area penalty, non-significant delay penalty and superior SEU tolerance compared with DICE and Quatro make the proposed design more suitable for area-constraint applications. Research along this line is in progress.

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V. SINGLE EVENT RESILIENT DYNAMIC LOGIC DESIGNS

Published as:

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Two single event hardened latch designs are presented in the previous two chapters. These designs are proposed to tackle the issue of charge sharing in deep-submicron and advanced technology process nodes. Charge sharing leads to multiple node charge collection and can reduce the critical charge of a sensitive node significantly. DICE, which shows single node upset immunity, demonstrates no significant increase in single event tolerance when compared to D latch. By adding extra transistors in these feedback loops, the feedback time increase, and thus, the single event tolerance increases. Because these feedback devices are turned ON when the structure is in the write mode, the performance degradation in the write time is not significant.

Although sequential elements, for instance, flip-flops or SRAM cells, are the major source of single-event errors, errors in logic circuits cannot be neglected. Logic may become a serious threat to the reliability of the system when the speed is very high. In such high-speed systems, dynamic logic circuits have found their wide applications. However, these types of circuits have significant single event upset issues. Little attention has been shifted toward hardening dynamic logic. In this manuscript, two dynamic logic designs (No. 2 and 3) are proposed. One design is using a feedback capacitor, while the other takes advantage of the differential structure. These designs were simulated using SPICE models by injecting a current pulse of a double exponential function. Improved single event tolerance of both designs was confirmed, and the latter shows no upset issues. Heavy ion experimental results were also presented, indicating the validity of these designs.

It is worth noting that the first design in this published paper was proposed by my fellow student Mulong Li. He is currently a master's student.

Single Event Resilient Dynamic Logic Designs

H.-B. Wang, M.-L. Li, L. Chen, R. Liu, S. Baeg, S.-J. Wen, R. Wong, R. Fung and J.-S. Bi

Abstract

Dynamic logic families are commonly used in high speed applications, but they are susceptible to single event errors. This paper presents and evaluates three techniques of hardening dynamic logic -- layout manipulation using charge sharing, addition of a feedback capacitor across the static inverter, and dual-rail domino logic with differential keepers. The layout-based design has better single event tolerance by sharing charge between NFET devices of the dynamic and static inverters; the design with a feedback capacitor makes the keeper more effective in recovering the hit node because of the increased propagation delay; the differential-keeper structure shows superior SET performance because the hit node could recover through the restoring path in the case of charge loss. These proposed designs along with the reference traditional keeper-based design were fabricated in a 130nm technology node as shift register chains and then irradiated by heavy ion particles. Experimental results verified the mechanisms and effectiveness of these proposed designs.

Index terms

Charge sharing, dynamic logic, radiation hardening, single event effect, soft error.

5.1 Introduction

DYNAMIC logic is an alternative to standard static logic in implementing combinational logic circuits. Although the former has disadvantages of charge sharing, weaker noise immunity, and difficult design activity due to the lack of automated design tools, its ability to implement complex logic circuits makes dynamic logic a candidate in designing high-speed modules with area constraints. Dynamic logic has been used in Central Processing Units (CPUs) and digital signal processors, for instance, Intel Pentium 4, Alpha microprocessors [4,7,8,19].

When a high energy particle strikes a dynamic logic circuit, a voltage perturbation resulting from electron-hole pairs collected at the sensitive nodes may cause a single event transient (SET) [5,14]. Due to the very nature of dynamic logic circuits -- the lack of a restoring path, the SET may get latched up and behave as a single event upset (SEU) instead, which is common in storage cells. Although the weak keeper increases the traditional dynamic logic hardness with the smallest area overhead, but it cannot work in the precharge phase.

A variety of techniques have been used to harden dynamic logic circuits. Triple modular redundancy (TMR) is one such technique that relies on a majority voter and three copies of critical circuits [12,20]. Although this approach is easy to implement, the significant area overhead makes it less attractive to designers. Erstad proposed an approach taking advantage of duplicated pull-up and/or pull-down networks in his patent [6]; and based on this, She et al. proposed three design variants [15]. However, the area cost of these approaches is at least 2X compared to that of the traditional keeper-based dynamic logic circuit [15]. By adding extra isolation devices, the logic circuit demonstrates better single event resilience [9]. Radiation experimental results show that the cross-section of this approach is ~50% lower than that of the keeper-based design [15]. However, to achieve better suppression, large area overhead has to be introduced [9].

The Semiconductor Industry Association (SIA) roadmap has identified radiation-induced soft errors as the major threat to reliable operation of electronic systems in the future [18]. Researchers have also pointed out that logic errors will be comparable to SEU errors with device scaling [16]. Therefore, dynamic logic hardening techniques pose critical design challenges and need to be investigated and explored. In this paper, we present three different structures with varying design complexity: the charge-sharing-based layout manipulation technique, the addition of a capacitor in the feedback path between the input and output of the static inverter stage, and the use of differential keepers in a dual-rail circuit. All of these proposed designs have better single event performance with relatively small area overhead.

The rest of the paper is organized as follows: Section II analyzes the single event issues with the traditional keeper-based design; Section III shows the electrical operating principles of these designs and their mechanisms of hardening against SETs; Section IV verifies these proposed designs by presenting SPICE or 3D Technology Computer Aided Design (TCAD)

simulation results; Section V demonstrates experimental results obtained from heavy ion testing and compares the cross-sections of the proposed designs; Section VI discusses area, power, delay and SEU performance among static and dynamic designs; and Section VII is the conclusion.

5.2 Background

Dynamic logic operates in two phases governed by a clock signal: precharge and evaluation. For the keeper-based design illustrated in Fig. 1, during the precharge phase, the clocked pMOS (CP1) is ON and initializes the output (O) high. During evaluation, CP1 is turned OFF and the output (O) may stay HIGH or LOW depending on the input. SET errors induced by high energy particles may occur in all of these operation phases.

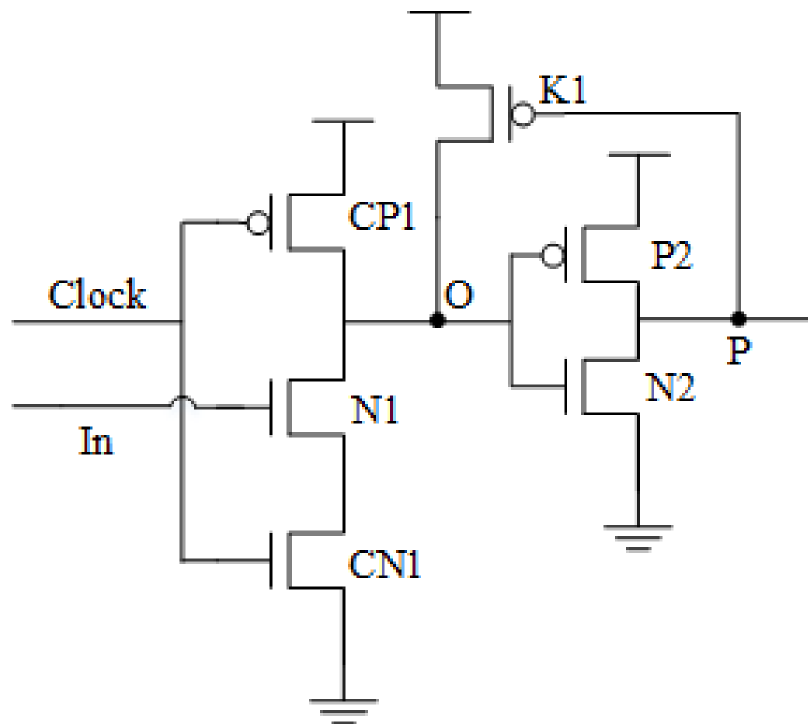


Figure V-1: The keeper-based design, which is also the reference design used in our work.

5.2.1 Precharge Phase – N hit

When the pull-down nMOS transistors are hit, which is referred to as N hit, the resulting charge loss may cause a negative SET transient at Node O. This is not of serious concern because such transients cannot propagate to the subsequent dynamic gates that are being precharged [9]. However, if the SET pulse width is too long and the hit node is not able to fully recover before

the evaluation phase starts, the negative transient may get latched as a static error. In this paper, we call such errors SEUs.

5.2.2 Evaluation Phase – N hit

In the evaluation phase and the hit node (O) is logic HIGH, the N hit may cause the voltage of Node O to be pulled down. Because the pull-up pMOS is OFF and the restoring path to the supply rail is blocked, the hit node may not be able to recover, and as a result, the SET error may get latched as an SEU. This is the worst-case scenario.

The higher clock frequency leads to a lower probability of SEUs. In [8], the probability is given by:

$$p = 1 - \frac{t_p}{t_{eva}} \qquad (1)$$

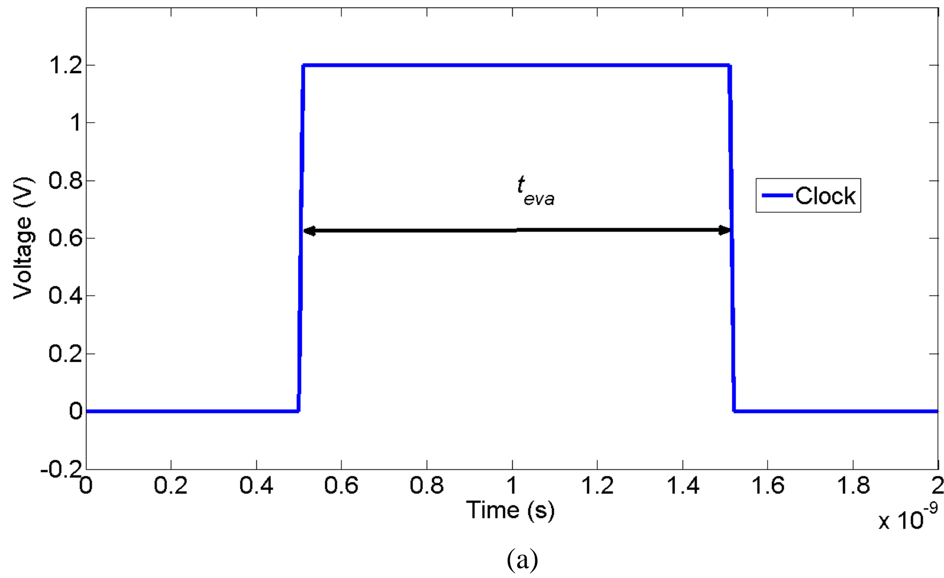
The propagation delay t_p is measured from the SET-induced falling edge at Node O to the resulting rising edge at Node P; and t_{eva} is the duration of the evaluation period. t_p and t_{eva} are labeled in Fig. 2.

In this scenario, the keeper (K1) is effective because it attempts to recover the hit Node O to vdd before the negative voltage transient propagates through the static inverter. As a result, the effectiveness of the keeper depends on the propagation delay of this inverter. The larger the propagation delay, the more effective the keeper.

5.2.3 Evaluation Phase – P hit

In the evaluation phase and the hit node (O) is logic LOW, when the pull-up pMOS transistor is hit, which is referred to as P hit, the hit node only observes a positive transient instead of an SEU. The reason is that after the excess charge is drained away, the always ON pull-down nMOS transistors will be able to recover the hit node voltage.

In all of these three scenarios, the P hit during the evaluation phase is the least severe because the SET pulse may get attenuated by electrical masking, logical masking or latching window masking [17]. Therefore, our designs aim to mitigate the first two types of SEU errors; this paper focuses on simulations and verifications on these two cases.



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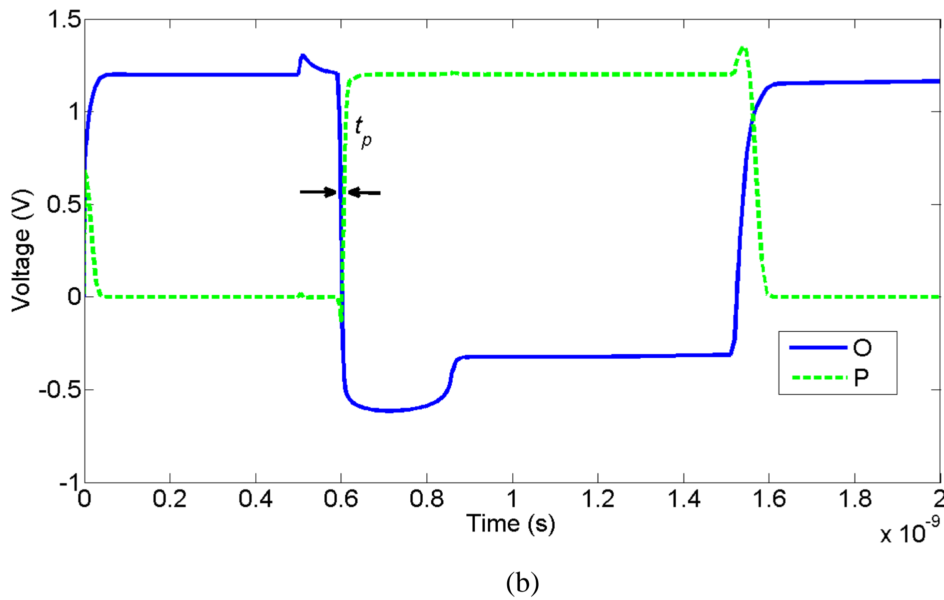


(b)

Figure V-2: The waveforms of (a) Clock (b) Node O and P in the case of N-hit during the evaluation phase.

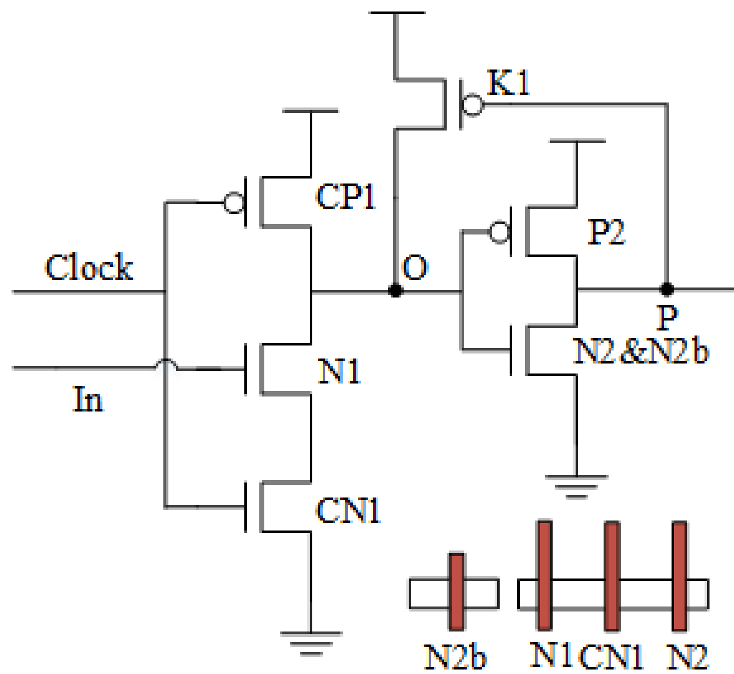
5.3 Proposed Designs

The first design is a variant of the baseline keeper-based circuit. As shown in Fig. 3(a), rather than modifying the schematic design, this structure involves layout manipulation. By duplicating the nMOS device (N2) of the static inverter on both sides of the pull-down nMOS (N1), negative charge is expected to be effectively shared by both the hit node O (the input of the

static inverter) and the output P. As a result, the transient at Node O cancels that at Node P. This reduces the overall voltage perturbation and leads to better single event tolerance with small area overhead.

The second design introduces a feedback capacitor across the static inverter of the domino gate at the schematic level, as shown in Fig. 3(b). The capacitor increases the propagation delay between the hit node O and the domino output P, and thus, this makes the weak keeper more effective. Another benefit is the increased critical charge due to the increased node capacitances of Nodes O and P. By having the capacitance across the static inverter, the effectiveness of the capacitance is increased by Miller capacitance.

Fig. 3(c) shows the third design, which is the dual-rail domino circuit with differential keepers. In the precharge phase, both keepers (K1 and K2) are turned OFF and the outputs (O and O') stay HIGH. On the other hand, during the evaluation phase, the output that goes low turns on the keeper on the other branch, the output of which will therefore be driven to HIGH. This design demonstrates particularly superior SEU performance in the evaluation phase - N hit because there is a conducting path to the supply rail through one of the keepers. Therefore, the hit node may still be able to recover in the case of charge loss.



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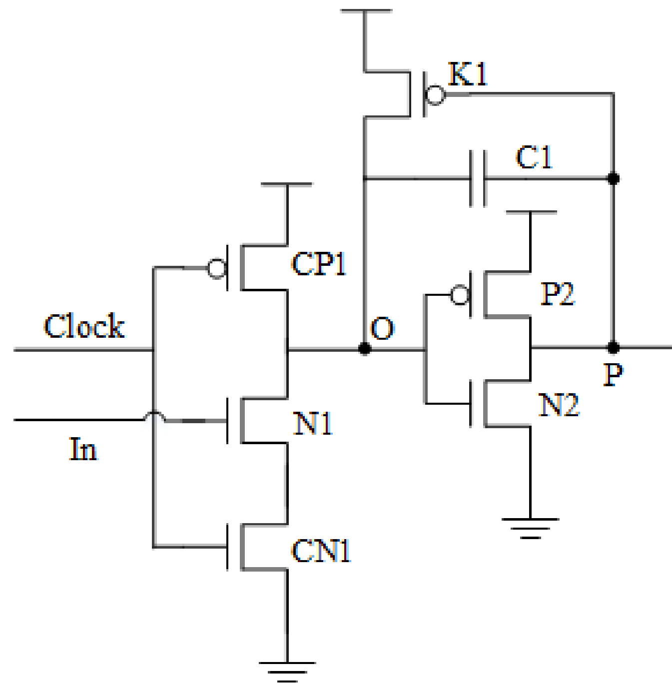

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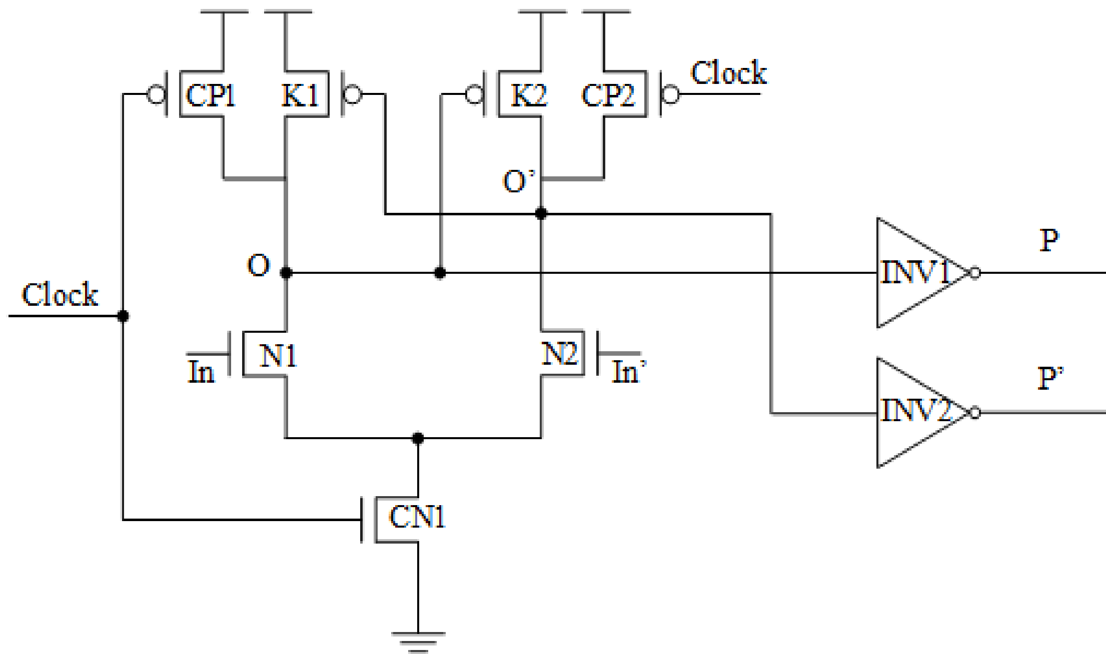


(c)

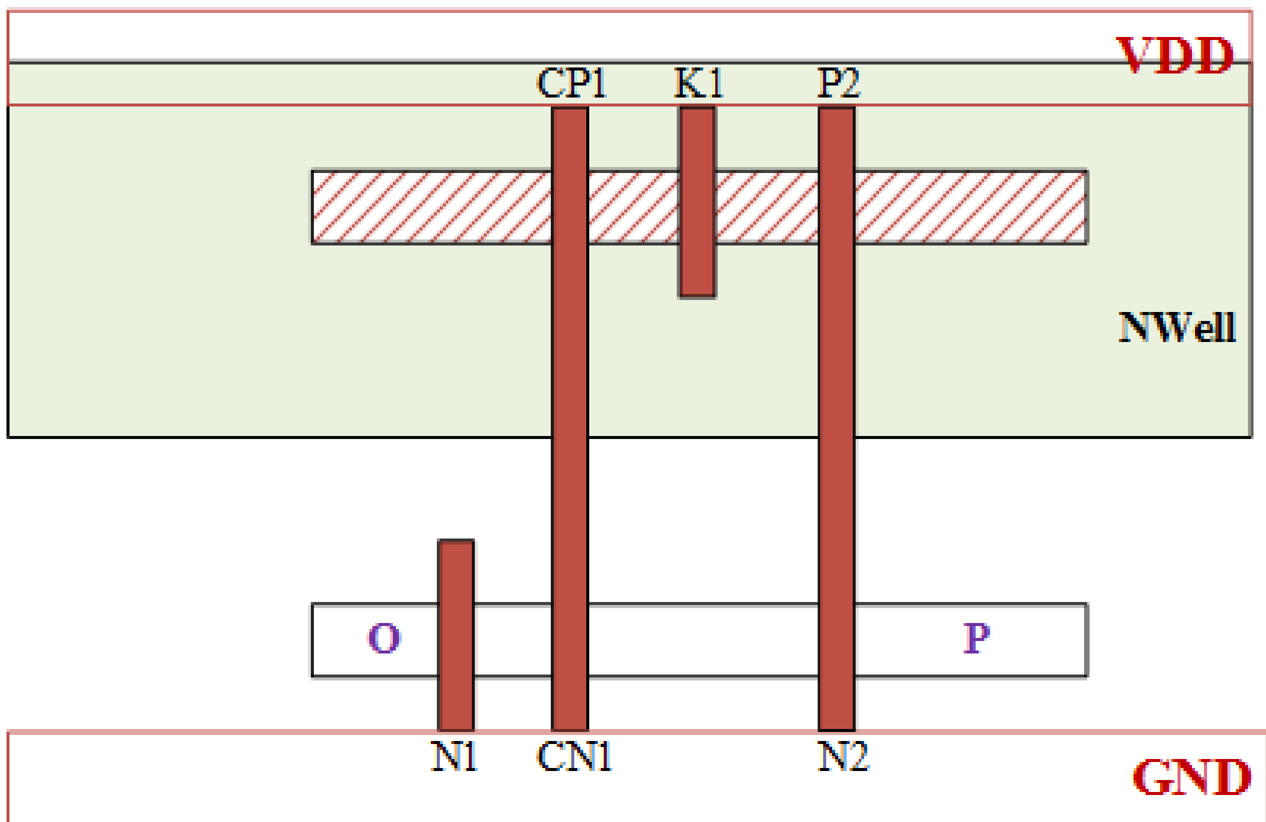
Figure V-3. The proposed designs: (a) the layout-based design (b) the design with a feedback capacitor (c) dual-rail dynamic logic design with differential keepers.

5.4 SINGLE EVENT SIMULATIONS

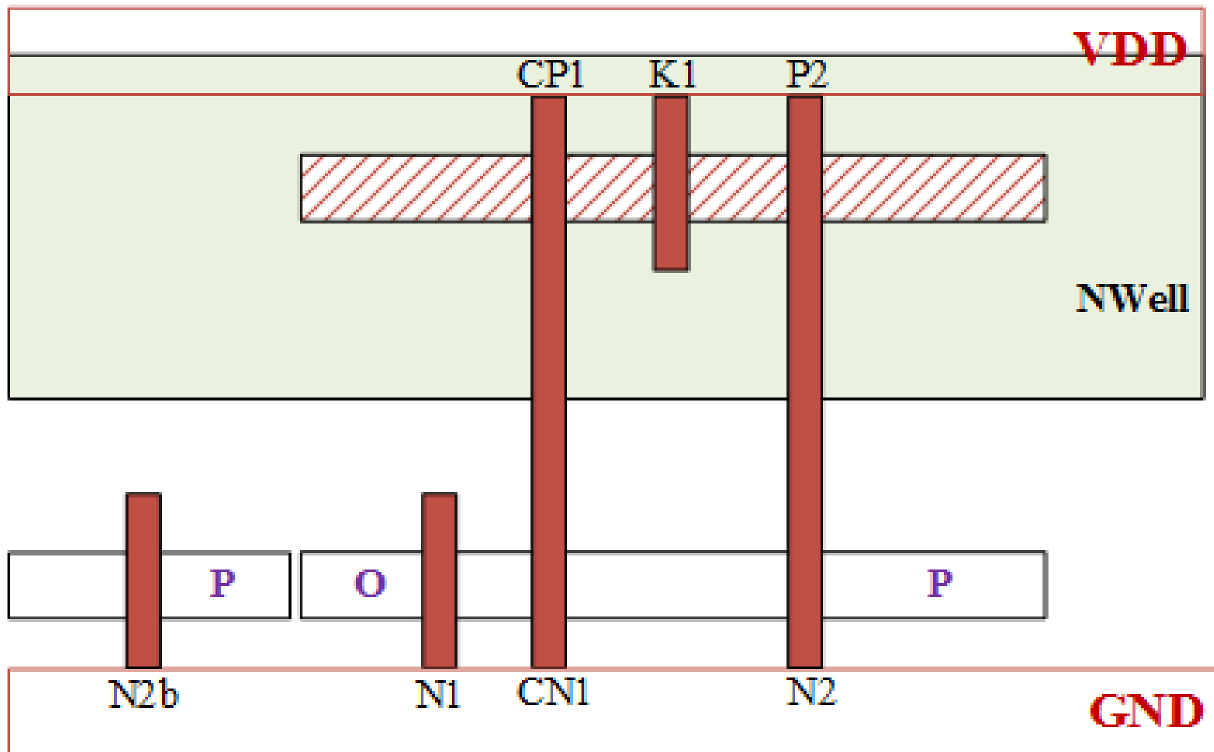
5.4.1 SEU Simulations on Dynamic Logic Using Charge-Sharing-Based Layout Technique

Figs. 4 (a) and (b) show the layouts of both the traditional design and the proposed design using charge sharing technique respectively. The NFETs N1, CN1 and N2 in the proposed design are placed is the same way as they are in the traditional layout. By adding N2b, a duplicate of N2, in the proposed layout, Node O is surrounded by Node P on both sides.

Such layout design promotes charge sharing between nodes O and P, thereby suppressing SET pulse at Node O [2]. Minimum space between Node O and the two copies of Node P is applied to optimize area and charge sharing efficiency. Mixed-mode 3D Synopsys TCAD simulations are performed, in which Node O is hit by ion particles with different LETs and 75o incident angle.



(a)



(b)

Figure V-4. The layouts of (a) reference design; and (b) the proposed design using charge sharing layout technique.

A. Evaluation Phase – N hit

For the design using traditional layout, an SEU at the hit node O propagates to Node P. As a result, its voltage is flipped from LOW to HIGH after the propagation delay of the static inverter, as shown in Fig. 2 (b).

However, as for the design using the proposed layout technique, Node P shares the negative charge deposited at Node O. As a result, the voltage of Node P tends to be pulled down, thereby delaying the SET pulse, as shown in Fig. 5.

Both the reference design and the proposed design are simulated with the clock frequency of 0.5 GHz and the duty cycle of 50%. As can be seen from Table I, the SEU probability of Design 1 decreases with the increasing LET value. SEUs are ~50% less likely to occur compared to the reference design.

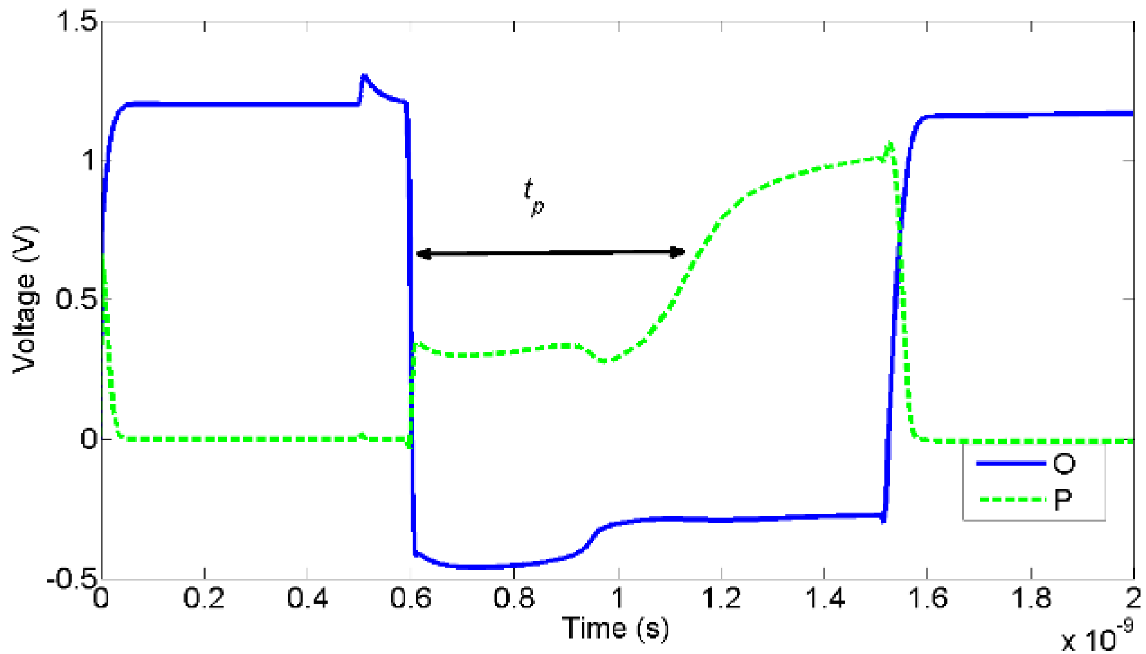


Figure V-5. The waveforms of both Node O and P in the proposed layout.

B. Precharge Phase – N hit

The extra transistor not only increases the capacitance of Node O, but also enhances the pull-down capability of the static inverter, thus making Node O easier to recover. Simulation results for different LETs and these SET pulse widths are shown in Table II. No SET pulse was observed for LET less than 35 MeV*cm^2/mg.

TABLE V-1 SEU PROBABILITY IN EVALUATION

LET (MeV*cm^2/mg)	Reference Design	Design 1
0.6	0	0
0.7	90.1%	0
1	98.7%	93.5%
2	98.8%	93.3%
5	98.9%	85.7%
10	99.0%	75.8%
35	99.1%	46.1%

TABLE V-2 OUTPUT PULSE WIDTH IN PRECHARGE

LET (MeV*cm^2/mg)	Reference Design (Unit: ps)	Design 1 (Unit: ps)
1	0	0
2	46.6	0
5	113.3	0
10	171.0	0
35	360.2	0

5.4.2 SEU Simulations on Dynamic Logic with a Feedback Capacitor

Fig. 3(b) shows the domino logic design with a capacitor placed in the feedback path across the static inverter. The capacitor can be manufactured by an n+ doped polysilicon over an n-well, a p+ doped polysilicon over a p-well, or the vertical natural capacitor formed from metal wire fingers.

The double exponential current source was used to model particle-induced single event current on the drain node of CMOS transistors [10].

$$I_{in}(t) = I_0\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \quad (2)$$

Where τ_α is the collection time constant of the junction, τ_β is the ion track establishment time constant, and I_0 is the maximum current. I_0 can be expressed as $Q/(\tau_\alpha - \tau_\beta)$, where Q is the amount of deposited charge. In this paper, an exponential current pulse with τ_α of 200ps and τ_β of 50ps is injected at node O.

In order to ensure the independency on processes for the proposed design, a pMOS transistor with the drain and source tied together is used. Therefore, the major capacitance comes from the gate capacitance, which is positively proportional to length L and width W. The improved SET hardness is achieved by the increased node capacitance and propagation delay.

A. Evaluation Phase – N hit

SPICE simulation results with varying amplitude of the current source are summarized in Table III. As expected, with the increasing product of W and L, the critical charge increases. With the W/L of 480/480 and 640/480, the critical charge is ~1.55X and ~1.75X respectively compared to that of the reference design.

TABLE V-3 SPICE SIMULATION RESULTS IN EVALUATION

	Design 2 (W/L:nm)				Reference Design
	480/120	640/120	480/480	640/480	
Critical Charge (fC)	0.084	0.087	0.105	0.120	0.068

B. Precharge Phase – N hit

During the precharge phase, the upset cannot propagate to the subsequent stage, but the shorter SET pulse width reduces the probability of SEUs. As shown in Table IV, when the injected charge is 0.4fC, the largest value in all W/L configurations, the pulse width with the capacitor sized W/L=640/480 is ~64% when compared to the reference design.

TABLE V-4 SPICE SIMULATION RESULTS IN PRECHARGE

	Design 2 (W/L:nm)				Reference Design
	480/120	640/120	480/480	640/480	
Critical Charge (fC)	0.339	0.346	0.386	0.400	0.328
Pulse Width of O @ 0.4fC (ps)	287	281	237	190	298

5.4.3 SEU Simulations on Dual-rail Dynamic Logic with Differential Keepers

To the authors' best knowledge, no research has been done to study the SEU performance of the dual-rail dynamic logic with differential keepers. A double exponential current source of the model depicted in the previous section is applied at Node O.

A. Evaluation Phase – N hit

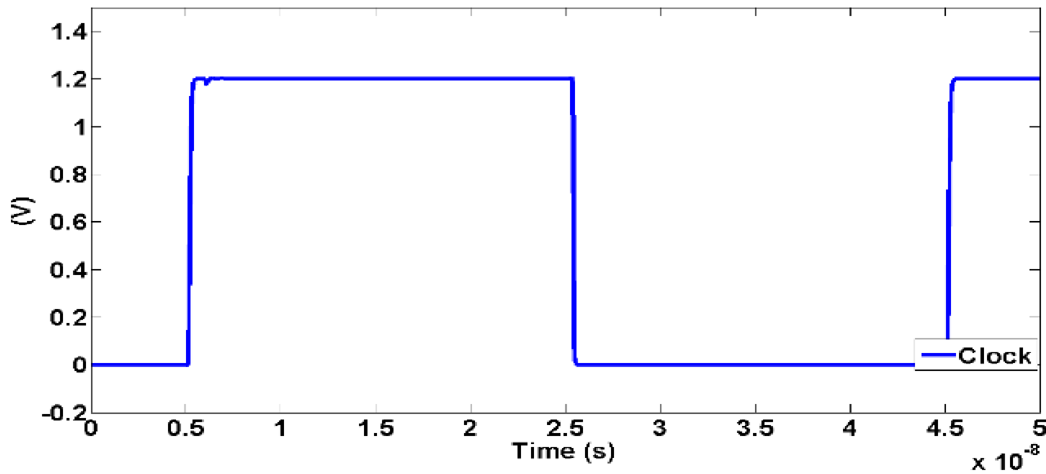
Assume the In and In' are ‘0’ and ‘1’; and the nodes of O and O' are ‘1’ and ‘0’ respectively. The voltage of the hit Node (O) is pulled down because of charge loss, and as a result, this may lead to a cascade of turning on the keeper K2, pulling up O', and inverting P and P'. These differential outputs will be propagated to the subsequent stage.

On the other hand, In' turns on the pull-down nMOS N2 and keeps pulling down Node O', the voltage of which depends on the drive capability of N2 and K2. Once the excess charge deposited at Node O is swept away, all the nodes will recover. This is illustrated in Fig. 6.

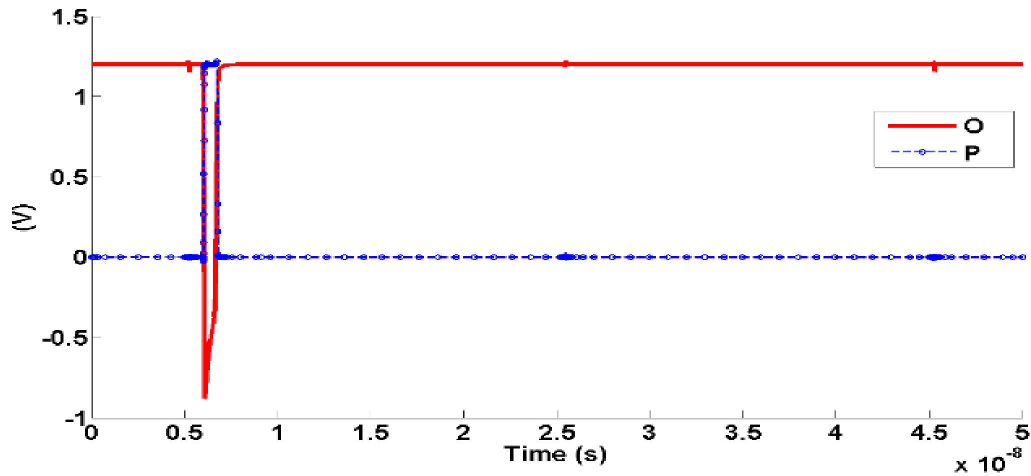
Therefore, the differential keeper domino logic only observes a transient instead of an SEU during the evaluation phase. This significantly increases its single event resilience.

B. Precharge Phase – N hit

The negative transient of the hit Node O may turn on the keeper K2 and inverts the output P. On the other hand, because the output O’ remains HIGH, it still turns off the keeper K1, as shown in Fig. 7. This is the same as the reference design.



(a)



(b)

Figure V-6. The waveforms of (a) clock (b) the voltage of Node O and P when the charge of 0.135 fC is injected at Node O

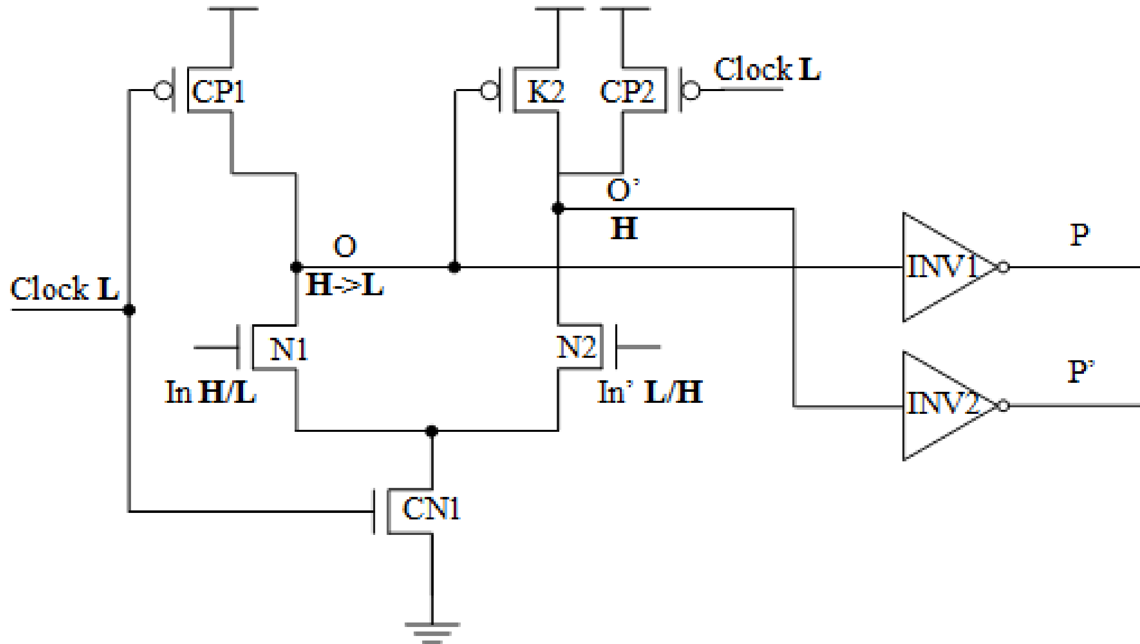


Figure V-7. When the N-hit occurs during the precharge phase, the equivalent structure of the differential-keeper dynamic logic

5.5 Experimental Results

These three proposed designs along with the reference structure were fabricated in a 130nm bulk CMOS technology. Test structures were comprised of 108 composite blocks, which contained 4 stages of domino logic followed by an SEU resilient Dual Interlocked Storage Cell (DICE) flip-flop [3]. Fig. 8 shows the test system composed of an FPGA board and a daughter card, on which the 130nm test chip (the device under test) is mounted.

The heavy ion experiment was carried out to test the SEE hardness of these four logic chains at the Texas A&M University Test Facility. In order to capture SEU errors instead of SET glitches, the logic chains were clocked at 10 kHz. During the testing, the test chip was bombarded with four types of particles (N, Ne, Ar, Kr) whose Linear Energy Transfer (LET) values were 1.3, 2.7, 10 & 35 MeV*cm^2/mg respectively.

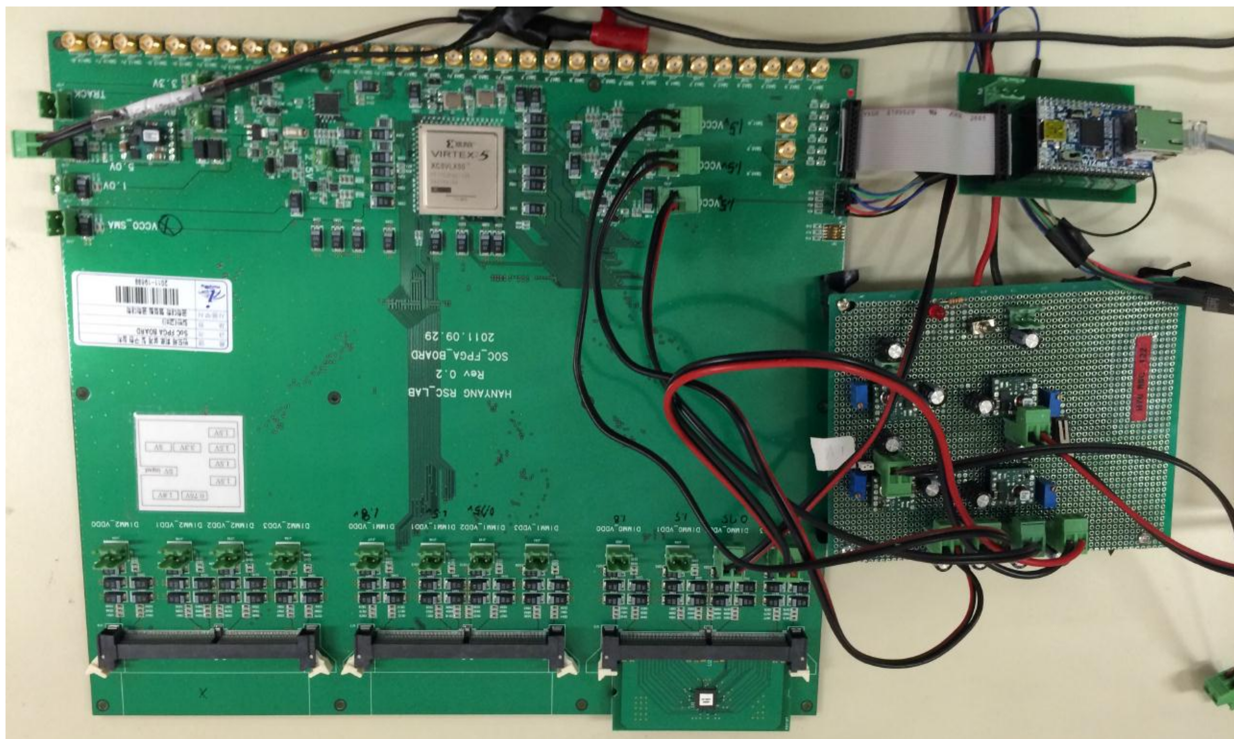


Figure V-8. The test system composed of an FPGA board and a daughter card with the test chip.

The irradiation experimental results are summarized in Table V, which lists the heavy ion LET, the total number of SEU errors, and the upset cross-section for each logic type. Fig. 9

compares the upset cross-section of these logic designs as a function of particle effective LET value.

For the layout-based logic design, its cross-section at very low LET values was approximately the same as that of the reference design. This is because the charge sharing efficiency is pretty low. However, the improvement of cross-section increased to ~30-50% at high LETs.

The design with a feedback capacitor showed significant improvement (~2X) when the LET is lower than 10 MeV*cm^2/mg. On the other hand, the improvement decreased to approximately 40%-90% at higher LETs.

The domino logic design with differential keepers exhibits superior SEU performance. Although it saw ~4X of magnitude decrease in cross-section over the reference design at the LET larger than 35 MeV*cm^2/mg, the decrease was more than 10X at LET values smaller than 35 MeV*cm^2/mg.

TABLE V-5 HEAVY-ION TESTING RESULTS

LET (MeV*cm^2/mg)	Fluence	Traditional Keeper Logic		Differential Keeper Logic		Dynamic Logic with a Capacitor		Layout-based Dynamic Logic	
		Errors	Cross section	Errors	Cross section	Errors	Cross section	Errors	Cross section
1.3	4.12E+08	242	5.44E-09	1	2.25E-11	25	5.62E-10	232	5.21E-09
2.7	3.11E+08	431	1.28E-08	22	6.54E-10	151	4.49E-09	284	8.45E-09
10	4.54E+08	860	1.76E-08	61	1.25E-09	457	9.33E-09	684	1.40E-08
35	8.82E+07	1560	1.64E-07	314	3.30E-08	1117	1.17E-07	1072	1.12E-07

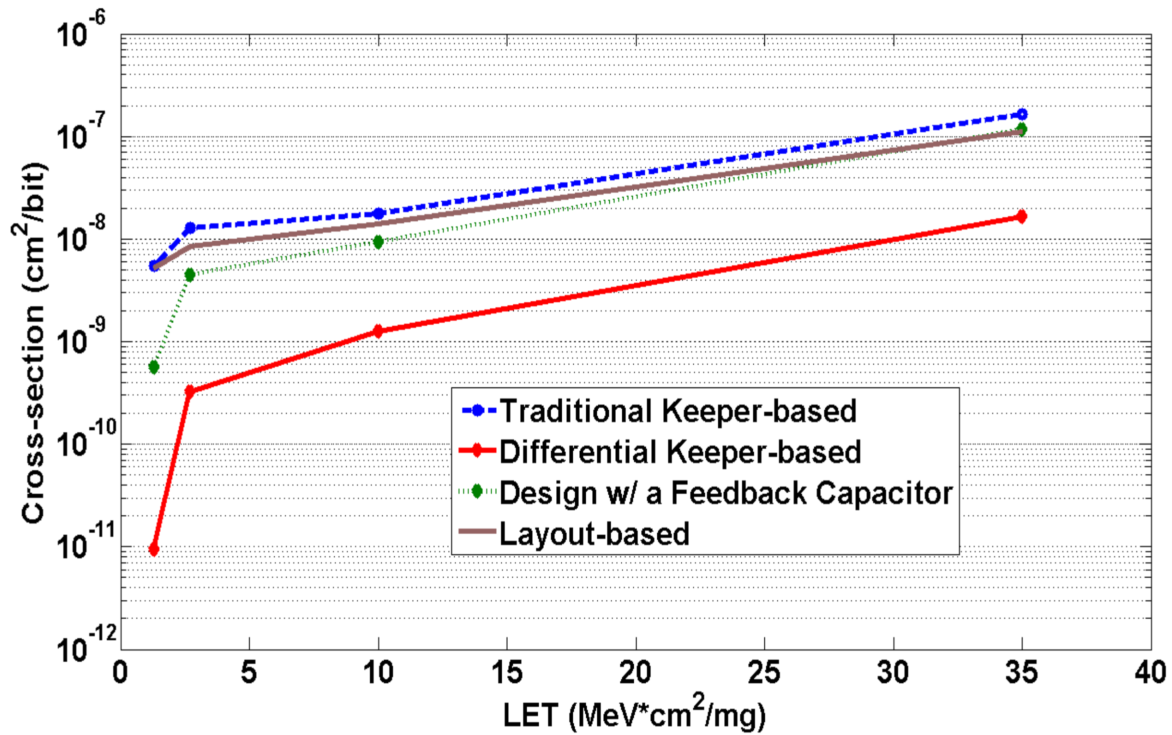


Figure V-9. Measured cross-section curves of the reference and proposed designs.

5.6 Discussions

Table VI compares the figures of merit among static logic and dynamic logic. Data regarding area, delay and power at the clock frequency of 0.5 GHz were obtained from simulations on eight-input dynamic multiplexers with split storage nodes used in Intel 64-bit Itanium 2 Microprocessor [11]. The cross-section data are from our testing results and the published literatures.

The reference design, the differential-keeper-based design, and the layout-based design have smaller delays than static logic. This is expected, by removing the pMOS transistor network from their static counterparts, the overall fan-in, fan-out and interconnect capacitance is lowered. By contrast, the TMR structure and the proposed design with a feedback capacitor have larger delays.

The overall power consumption of dynamic logic is larger than static logic, after the clock power consumption is factored in. Among all the dynamic logic derivatives, the TMR structure

has the largest dynamic power consumption because of a significant increase in transistor numbers.

Table VI also clearly shows that the TMR-based design has the largest area cost. The differential-keeper-based design occupies approximately the same area as static logic.

Monte-Carlo simulations covering process and mismatch have been carried out to evaluate the effect of process variation on delay and power. The deviation between these numbers of delay and power in the worst case and typical case is approximately 15-40%, as shown in Table VI. In addition, process variation may vary critical charge of Design 2 or pulse width of Design 3 by approximately 20-40%.

To conclude, while both the layout-based structure and the one with a capacitor are comparable to the TMR design in terms of soft error suppression, the differential-keeper-based design has significant improvement compared to TMR with smaller area overhead. However, in the area-constraint applications, identifying the single event sensitivity of the target logic circuit and hardening the vulnerable gates are recommended in order to reduce the overall soft error rates while maintaining relatively small area overhead [1,13].

5.7 Conclusions

In this paper, we have investigated three techniques of hardening dynamic logic with increased SEU hardness: the charge-sharing-based layout manipulation technique, the addition of a capacitor in the feedback between the input and output of the static inverter stage, and the use of differential keepers. Both simulation results and irradiation experimental data illustrate that the dual-rail logic with differential keepers shows a significant decrease in cross-section compared with the traditional keeper-based design. The performance gain comes along with an increase in area budget. The overall area cost of the differential-keeper-based design is as large as ~2X when compared to the reference design.

TABLE V-6 PERFORMANCE COMPARISION

	Traditional Keeper Logic		Differential Keeper Logic		Dynamic Logic with a Capacitor		Layout-based Dynamic Logic		TMR-based Keeper Logic		Static Logic	
	Typical	Worst case	Typical	Worst case	Typical	Worst case	Typical	Worst case	Typical	Worst case	Typical	Worst case
Delay	1	1.30	1.05	1.37	1.86	2.50	1.19	1.58	1.98	2.53	1.27	1.68
Power	1	1.32	1.54	1.75	1.73	2.26	1.28	1.54	3.64	4.35	0.82	1.17
Area	1		2.2		1.2		1.1		3.6		2.4	
Cross-section	1		0.05~0.2		0.10~0.71		0.68~0.95		0.64~0.79 [9]		N/A	

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VI. SINGLE-EVENT PERFORMANCE EVALUATION OF CLOCK NETWORKS AT 28-NM CMOS TECHNOLOGY NODE

Submitted as:

H.-B. Wang, N. Mahatme, M. Newton, L. Chen, Y.-Q. Li, R. Liu, B. Bhuva, K. Lilja, S.-J. Wen, R. Wong, R. Fung, and S. Baeg, "Single-Event Performance Evaluation of Clock Networks at 28-Nm CMOS Technology Node," *IEEE Transactions on Nuclear Science*, 2015.

Latches are critical for a digital system because they need to be used to store states. For high speed systems, latches have found their wider popularity in the design of pipelines. Dynamic logic also plays a crucial role in building such a system. In the previous chapters 3 through 5, single event tolerant structures of latch and dynamic logic are presented and evaluated. These hardened designs facilitate a fault-tolerant system design.

In this manuscript, clock networks are evaluated in terms of single event performance. For a digital system, clock signals need to be distributed across the die with no or little skew. Otherwise, the synchronous components in this system cannot function properly. In advanced technology nodes, however, single event performance of clock networks need to be evaluated as well due to the increased single event sensitivity. A 28nm test chip containing two clock schemes – clock mesh and daisy chain clock tree, was fabricated and tested. Experimental results show that clock mesh has significantly high single event tolerance. It did not see errors when the LET is below 10 MeV*cm^2/mg. These errors at high LETs were found out to be caused by these daisy chain clock buffers.

Single-Event Performance Evaluation of Clock Networks at 28-nm CMOS Technology Node

H.-B. Wang, N. Mahatme, L. Chen, Y.-Q. Li, R. Liu, B. Bhuva, K. Lilja, S.-J. Wen,

R. Wong, R. Fung, and S. Baeg

Abstract

Two clock networks including clock meshes and daisy-chain clock buffers designed to synchronize 5 DFF chains were fabricated in a 28nm bulk CMOS technology. Alpha and proton results did not trigger any errors indicating the significant single event tolerance of these clock networks. Heavy ion data are presented showing few occurrences of burst errors induced by single event transients (SETs) propagation through the clock network when the input pattern was checkerboard (alternate 1 and 0). The same phenomena were observed in laser tests. These burst errors occurred (1) simultaneously in a DFF chain and its subsequent chains, or (2) in a single chain with subsequent chains unaffected. The distinct mechanisms of these burst errors were found to be the electrical masking effect of the daisy-chain clock buffers.

Index terms

Clock jitter, clock mesh, clock race, radiation hardening, single event effect, soft error.

6.1 Introduction

As a radiation particle travels in the silicon substrate of a microelectronic circuit, excess electrons and holes are generated along its track. These charges may be collected by sensitive nodes nearby and therefore cause voltage perturbations at these nodes. For combinational circuits, the deposited charge can induce a transient voltage pulse at the output, which is referred to as a single event transient (SET) [1]. In digital systems, an SET may propagate through the subsequent logic path and finally get latched by a storage cell such as a flip-flop to cause an upset.

For synchronous digital systems, clock signal is the reference signal to which all components on an IC are synchronized. Since all components on an integrated circuit (IC) operate synchronously, it is necessary to ensure that they receive the clock signal at the same time. If the clock edges are not perfectly synchronized for different components on an IC, communication between these components may fail, resulting in functional failure of the IC. As components that are electrically next to each other (communicate with each other) may not be physically next to each other, synchronized clock distribution becomes very difficult to achieve, especially when the operating frequency is pushing the limits of a technology node [2].

Scaling reduces minimum dimensions on an IC, resulting in desired properties of close proximity of transistors and reduced nodal capacitances. For the latest generation of technology node, the number of transistors on an IC has reached multiple billions, making the synchronized clock distribution to each component on an IC a very difficult task. Close proximity of metal lines to each other results in higher interconnect capacitances, requiring optimal use of routing resources and buffers for a clock network in an IC at such an advanced technology node. There have been many different techniques developed to distribute a clock signal across the whole IC, such as H-tree distribution, clock-mesh, clock-grid, reverse-clocking, etc. The effectiveness of these techniques have been verified and proven at multiple technology nodes [3].

Unfortunately, single-event (SE) effects are fast becoming a major reliability problem at advanced technology nodes. For previous generations, single-event effects used to be a problem for space and military environments only. For the latest generation of technology nodes, failures caused by single-events are expected to overshadow all other failure mechanisms even in the terrestrial environment [4],[5]. Since any failure on a clock network guarantees the operational failure of an IC, it has become critical to characterize and evaluate clock networks for single-event effects.

This work evaluates the single event performance of clock mesh technique preferred by IC designers at advanced technology nodes. A test IC was designed and fabricated at a 28-nm bulk, planar CMOS technology node. The fabricated IC was exposed to alpha particles, protons, heavy ions, and laser irradiations to experimentally characterize the single-event performance of the clock mesh. Results identified weak points in the clock mesh designs. Since clock networks

provide the heartbeat of an IC, such information is necessary to allow designers to harden their clock networks effectively and optimally.

The rest of the paper is organized as follows: Section II illustrates the commonly used clock distribution techniques and radiation-induced clock errors; Section III introduces the test chip design and the clock scheme used in our test chip; Section IV presents alpha, proton, laser and heavy ion testing data; Section V analyzes the mechanisms of burst errors when the input pattern is checkerboard at the heavy ion testing by using SPICE and 3D Technology Computer Aided Design (TCAD) simulation results; and Section VI concludes the paper.

6.2 Common Clock Tree Structures

All clock distribution scheme require buffers at multiple levels to distribute clock. Figure VI-1 (a) shows a simple fanout-of-4 buffers to distribute clock signal. If not done appropriately, the nodal capacitances for all buffers at a given level may not be identical, resulting in clock skew. Clock-mesh technique eliminates this problem by connecting all buffers at a given level as shown in Figure VI-1 (b). This results in many buffers driving a huge capacitor. Any imbalance in load distribution is eliminated at the global level, resulting in minimal clock skew.

As technology advances and on-chip variations are becoming significant in advanced technologies, clock tree is losing favor because of the skew introduced by the delay variation on different tree branches [6]. By contrast, although the mesh consumes a large amount of power, low clock skew, low variations, and high reliability make the clock mesh network commonly used in high-end VLSI designs [7],[8].

Radiation strikes on these buffers and inverters may cause system failures due to either radiation-induced clock jitter or radiation-induced clock race.

If excess charge is deposited in the clock node near the clock transition, the clock edge may be shifted backward or forward depending on the charge polarity and device type. Such a clock variation may result in setup time or hold time violation. This is referred to as radiation-induced clock jitter. The contribution due to jitter is less than 2% of the overall clock path SER [9].

Since the buffers and inverters in the clock networks are combinational gates and do not possess any logical masking effects, an SET with high enough amplitude and long enough

duration may propagate to the sinks. Therefore, this new clock pulse may lead to the false opening of these sinks and thereby sampling the wrong data. This is referred to as radiation-induced race.

From the perspective of the sinks, the malfunction of clock may generate a significant number of errors in a very short period of time. The local clock nodes are estimated to make up 20% of the overall SER [9]. Researchers from the industry and the academic field have developed techniques of designing local rad-hard clock drivers [10], [11].

The global clock network is believed to contribute to less than 0.1% of the overall clock path SER. However, to the authors' best knowledge, no public literature has investigated and evaluated the single event performance of different global clock distribution techniques.

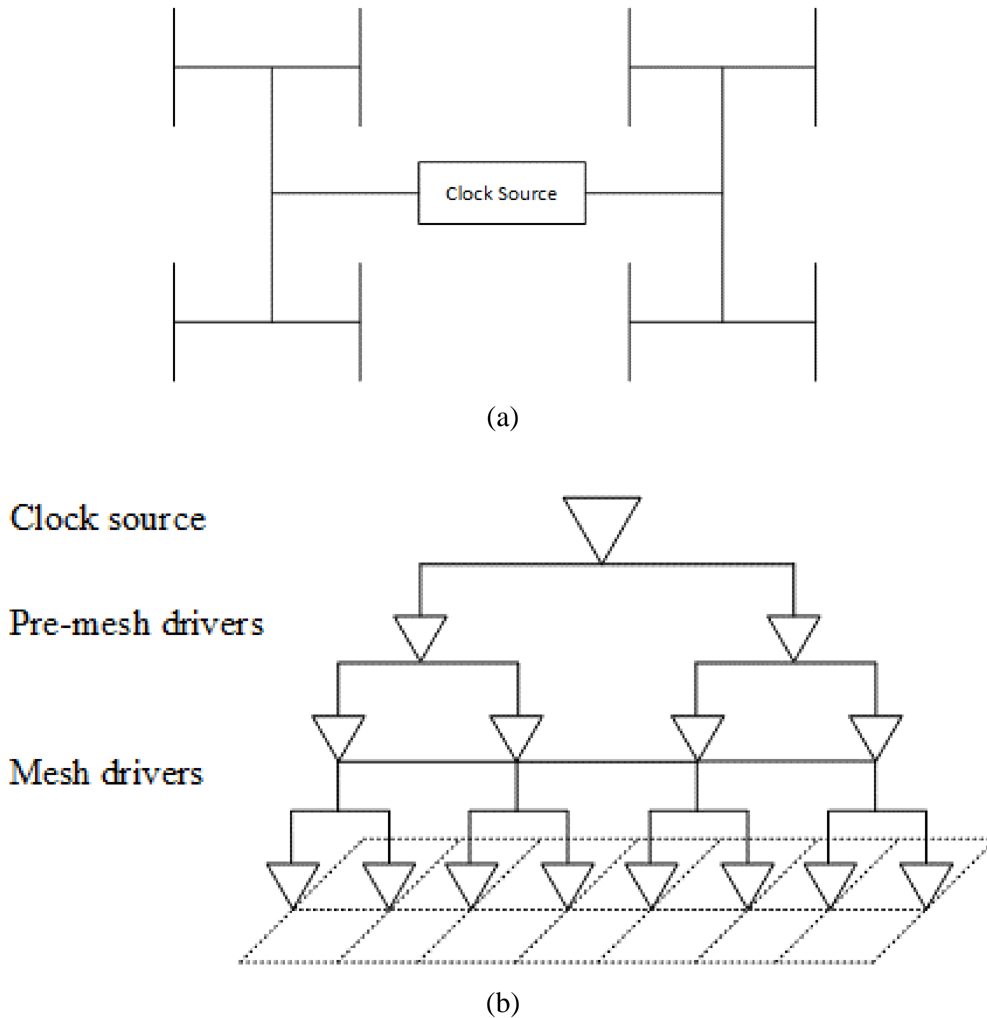


Figure VI-1. Clock distribution networks: (a) H-tree (b) clock mesh

6.3 Clock Network and Test Chip Design

Among clock distribution techniques employing balanced-load strategy, such as H-tree or reverse-clocking, the requirement that all buffers at a level have equivalent nodal capacitances is difficult to meet. Grid-based techniques, such as clock-grid or clock-mesh, on the other hand, do not necessarily require a balanced load at each level. It must be kept in mind that balanced load will make clock-mesh technique much more effective. In addition, if done properly, clock-mesh will allow designers to place a clock buffer within a very short distance from each logic gate needing a clock signal. As a result, designers prefer clock-grid or clock-mesh techniques over balanced load techniques for ICs designed at advanced technology nodes. This work primarily focuses on the clock-mesh technique for these reasons.

For the test chip, the clock distribution scheme is evaluated by using a shift register chain. For a shift register chain, hits on individual flip-flops will result in single error at a time (if individual FF designs are placed far enough apart to avoid charge sharing between FF). If the input to the shift register is kept constant during the testing, all hits on the clock networks are masked. If the input to the shift register is alternated between 1 and 0, all hits on clock network will also be observed as errors. Depending on the number of burst errors occurring within a clock cycle, one can determine the buffer level of the SE hit within the clock network.

For the test IC, two different clock distribution schemes were used. The global clock distribution uses daisy-chain buffers to distribute clock signal to individual shift register chains, as shown in Figure VI-2. Each daisy-chain clock buffer consists of a 10X inverter followed by a 40X inverter and is located outside of each register chain, as illustrated in the diagram.

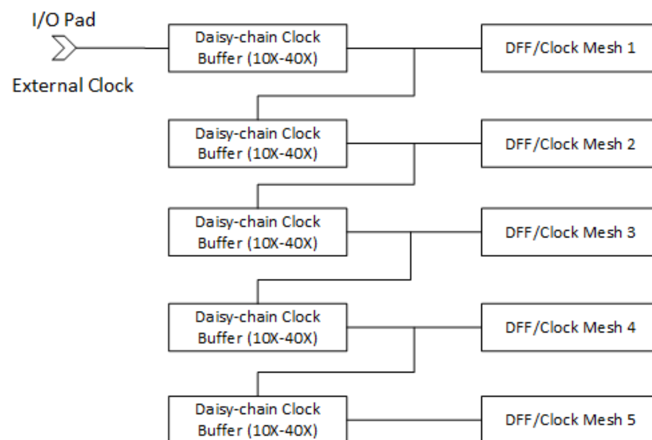
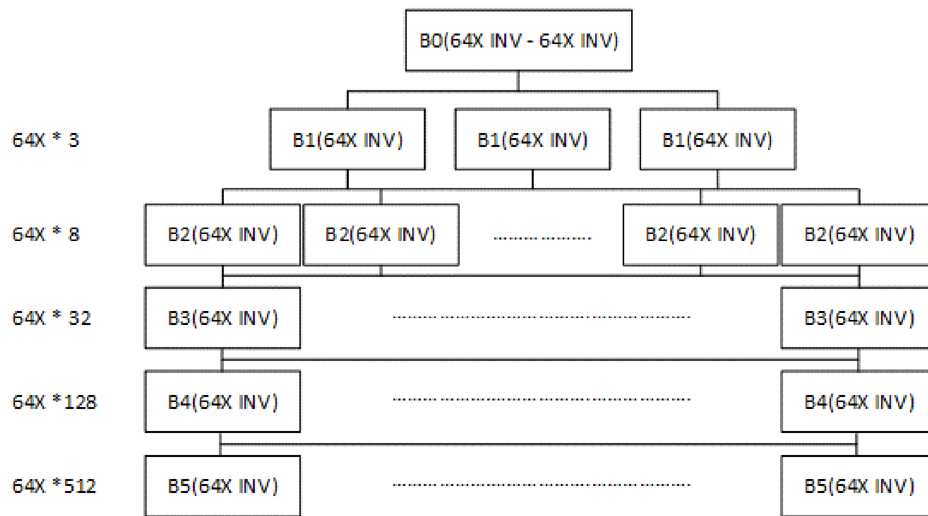


Figure VI-2. The global clock distribution network consisting of daisy-chain buffers

Within each shift register chain, local clock distribution was carried out with the clock-mesh structure. Figure VI-3 shows the local clock distribution used for the test IC. For the clock-mesh, 6 levels of buffers were used, with all buffers at a given level shorted to each other. All of the buffers inside of the mesh are sized as 64X. A balanced tree is used at all levels to minimize local clock skew. The shorting of clock buffers results in a large capacitance and large sourcing current capabilities. All buffers were designed to yield equal NMOS and PMOS current drives. Each shift register contains 5k different flip-flops.



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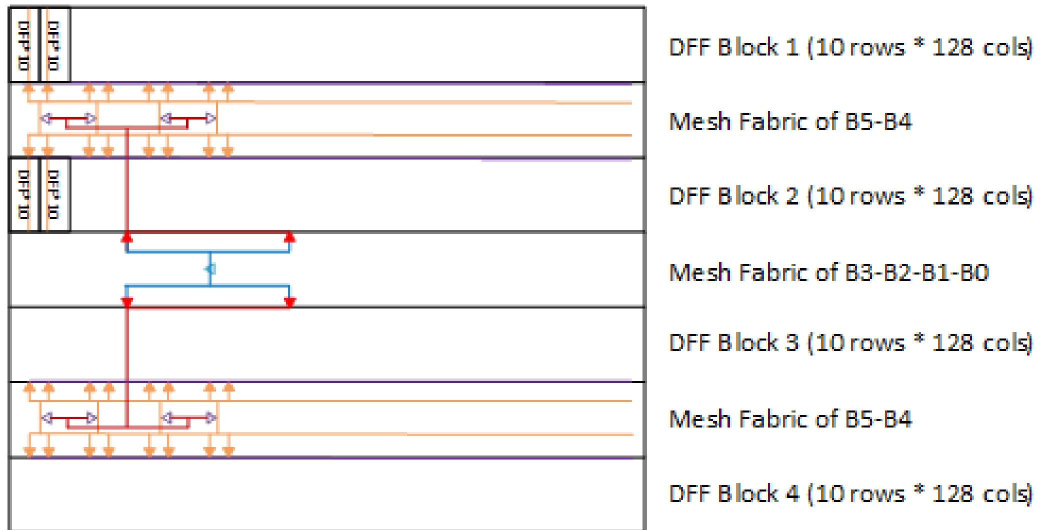

(b)

Figure VI-3. (a) The logical structure and (b) the physical structure of the clock mesh

6.4 Experimental Results

The test IC was exposed to multiple radiation sources to determine the vulnerability of clock networks used on the IC. Alpha particle exposures will most likely affect individual FF design, but not clock-mesh buffers due to their high-capacitance nodes and high-restoring-current buffers. Alpha particles might affect the daisy-chain buffers due to their lower critical charge requirements to cause an SET compared with clock-mesh design. Heavy-ions and laser irradiations will affect all clock networks.

The device under test (DUT) mounted on a daughter card is controlled by a Xilinx Virtex-5 FPGA board. The FPGA program generates a clock signal for the DUT and records errors for each chain. These errors are sent to the computer via a 100M Ethernet port for processing.

6.4.1 Alpha Particle Exposure

Alpha testing was carried out at the University of Saskatchewan using an Americium-241 alpha source with 2.5 uCi activity and $4.61e^{7}$ a/cm^{2}/hour emissivity. The input to the shift registers was either all 0s, all 1s or checkerboard (1010). The supply voltage was varied from 1 V to 0.8 V (the nominal supply voltage for this technology node is 1 V). The clock frequency was varied from 10 kHz to 100 MHz. No burst errors were observed within the shift registers during the test. This means all clock networks, daisy-chain and clock-mesh, were immune to alpha particles.

6.4.2 Proton Exposure

Proton testing was carried out at the Korean Institute of Radiological & Medical Sciences (KIRAMS). The energy of protons used for testing was 45 MeV. A single test-chip was exposed to an average flux of $1.64e^{11}$ proton/cm^{2}/second. All the three input patterns were fed to these shift registers with the clock frequency of 1 MHz. The supply voltage was varied from 1V to 0.7V. Same as the alpha testing, no burst errors were captured.

6.4.3 Heavy-Ion Experiment

The flip-flop shift register chains were tested at the Cyclotron Institute of Texas A&M University. This facility offers a variety of heavy ion beams for single event effects research.

Figure VI-4 shows the heavy ion test setup. The FPGA board was bombarded by normal incident particles. During testing, four different heavy ions N, Ne, Ar, and Kr with effective LETs ranging from 1.3, 2.7, 10 to 35 MeV-cm^2/mg were used. The input to the shift registers was all 1s, all 0s or checkerboard. The shift registers were clocked at 10 kHz and the supply voltage was 1V.

Figure VI-4. The test setup at the Cyclotron Institute of Texas A&M University

Exposure to heavy ion particles resulted in burst errors as shown in TABLE VI-1 and TABLE VI-2. Burst error were observed only when the input pattern was checkerboard and only for higher LET particles (10 and 35 MeV-cm^2/mg). The run times at LET=10 and 35 MeV-cm^2/mg are 30 and 35 minutes, respectively. At an LET of 10 MeV-cm^2/mg, 11 burst error events were recorded, while 28 burst-error events were noticed at an LET of 35 MeV-cm^2/mg.

The burst errors listed in these tables fall into two distinct categories. One type of these errors (marked as X) appeared in multiple chains or appeared in the last chain (DFF5). The other type of errors (marked as S) only appeared in one chain (but not the last chain), and did not show in the following chains. It is noted that, at LET=10 MeV-cm^2/mg, the total occurrences of burst errors including both multi-chain and single chain errors were 11; while at LET=35 MeV-cm^2/mg, the number increased to 28. The overall affected time slices out of the total run times are 0.3% and 0.67% for LET=10 and 35 MeV-cm^2/mg, respectively. More specifically, at LET=10 MeV-cm^2/mg, the single-chain errors occurred 3 times, while it occurred only once at LET=35 MeV-cm^2/mg.

It is obvious that the multiple chain burst errors (X-type) should be caused by the hits on daisy-chain buffers; otherwise the errors would not be able to propagate to the following chains. On the other hand, the single chain burst error could be caused by hits on either clock-mesh buffers inside of the chain, or the daisy-chain buffer in front of the chain, however, it did not propagate to the following chains. In order to further understand this this phenomenon, laser experiments were carried out, and the laser setup and results are described in the following section.

TABLE VI-1 CLOCK BURST ERRORS FROM EACH CHAIN AT THE HEAVY ION EXPERIMENT FOR LET=10 MEV-CM^2/MG

Event No. of Burst Errors	1	2	3	4	5	6	7	8	9	10	11
DFF1							X	X			
DFF2						X	X	X			
DFF3	X		X			X	X	X	**S**	X	**S**
DFF4	X	X	X	**S**		X	X	X		X	
DFF5	X	X	X		X	X	X	X		X	

TABLE VI-2 CLOCK BURST ERRORS FROM EACH CHAIN AT THE HEAVY ION EXPERIMENT FOR LET=35 MEV-CM^2/MG

Event No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DFF1	X			X						X				X					X	X		X	**S**		X			
DFF2	X	X	X	X		X	X	X		X				X	X				X	X		X		X	X			
DFF3	X	X	X	X	X	X	X	X	X	X				X	X				X	X		X		X	X			
DFF4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				X	X		X		X	X	X	X	X
DFF5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X

6.4.4 Laser Test

Two-photon irradiation facility located at the SSSC at University of Saskatchewan consists of a Ti:Sapphire pulsed laser and a Laser Scanning Microscope (LSM). The pulsed laser system uses a continuous wave (CW) green diode-pumped solid-state (DPSS) laser as the pump laser, which provides 18W output at 532 nm. Its output goes into a regenerative amplifier (RegA) who

uses Ti:Sapphire as its gain medium. The RegA can provide a repetition rate from 10 kHz to 300 kHz internally. To achieve an even lower repetition rate for the experiment, an external signal generator is connected to its timing controller. In fact, 1 kHz is used in our experiments. Note that the RegA is also seeded with a femtosecond pulsed laser.

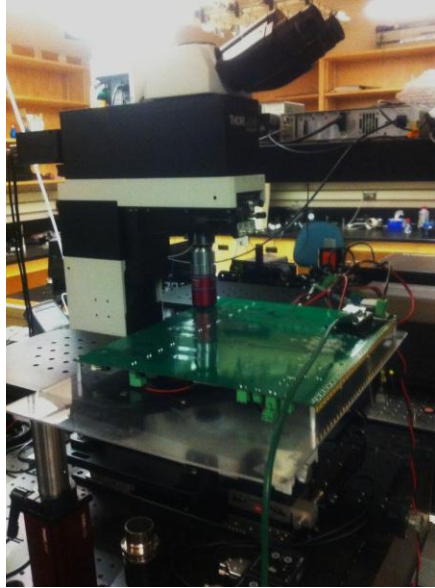

Figure VI-5. The TPA laser setup at the University of Saskatchewan

The pulse energy of the seed laser is amplified dramatically by the RegA. After that, it is injected into an optical parametric amplifier (OPA) which extends the wavelength coverage. In our experiment, the 1250 nm wavelength is adopted. The final output of the pulsed laser system is merged with imaging laser and sent to the optical path of the LSM. The imaging laser is applied on the DUT and its reflection photons are collected by a detector and sent to the computer for image processing.

The X-Y-Z directions are fully controlled by the computer with a step size of 0.05 μm for XY and 0.1 μm for Z. During the scan, the area is divided into 256 by 256 pixels with a dwell time of 5 μs on each pixel. Thanks to the 50X objective, the minimum area can reach to 3.84 μm by 3.84 μm, which provides decent accuracy in the experiments.

The laser power ranging from 0 μW to 1.60 μW was used to scan each shift-register chain, in which the clock-mesh buffers reside. Our laser testing results showed that scanning inside each of the chain did not cause any burst errors even when the maximum laser energy in the range was applied. This indicates that clock-mesh drivers did not cause any burst errors.

Then the daisy-chain clock drivers located outside of the chains were scanned by the laser. Single chain errors (S-type errors shown in the table I and II) were observed when the laser power was approximately 0.56 μW, while multiple-chain errors (X-type errors) were observed when the laser energy were around 1.2 μW.

6.5 Discussions and Analysis

The results of the heavy ion and laser experiments indicate that the burst errors are induced by the hits in the daisy-chain buffers instead of the clock-mesh buffers. This is understandable, since the size of the clock-mesh driver (64X) is much larger than the inverter (10X) in the daisy-chain buffers. However, it is not very clear why most of the hits caused multiple chain errors, and few hits caused single chain errors. In order to fully understand this phenomenon, SPICE and TCAD simulations are carried out to study the two types of clock distribution networks.

6.5.1 Comparison of Critical Charge for Two Clock Networks

As illustrated in our irradiation experiments, the daisy-chain buffers were identified to induce single event errors, while the clock-mesh drivers showed a much higher tolerance.

Simulations using SPICE have been used throughout the work to compare the single event tolerance of these two clock networks. The critical charge in this work is defined as the charge that the output of the clock buffer switches to 0.5 * Vdd. 0.5 * Vdd is used because the PMOS/NMOS in each clock inverter has balanced driving capability.

The double exponential current source was used to model particle-induced single event current on the drain node of CMOS transistors [12].

$$I_{in}(t) = I_0\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \quad (1)$$

where τ_α is the collection time constant of the junction, τ_β is the ion track establishment time constant, and I_0 is the maximum current. I_0 can be expressed as $Q/(\tau_\alpha - \tau_\beta)$, where Q is the amount of deposited charge. In this work, an exponential current pulse with τ_α of 100ps and τ_β of 20ps is applied.

For the daisy-chain clock buffer (a 10X inverter followed by a 40X inverter), the 10X inverter is hit by injecting a double exponential current source. The critical charge obtained from the SPICE simulation is 58 fC.

For the clock mesh, B0, the first clock mesh level consisting of 3 shorted inverters, is the weakest because fewest number of clock buffers in this mesh-based clock network are shorted at this level. The obtained critical charge is 360 fC.

By comparing the critical charge of these two cases, the daisy-chain clock buffers demonstrate worse single event tolerance. This substantiates the fact that the clock-mesh buffers are more tolerant than the daisy-chain buffers, which were shown in heavy ion and laser results.

6.5.2 Analysis of Two Distinct Types of Clock Errors

Accuro is used to investigate the underlying mechanisms of two distinct types of burst errors. Accuro is a TCAD tool suite from Robust Chip Inc., and it is capable of building a full 3D representation of the design based on its layout file and doping profiles. The simulation engine in Accuro applies a full 3D transport model to simulate the charge transport and charge collection [13].

The burst errors started to show up at an LET = 10 MeV-cm^2/mg in the heavy ion experiments. Our TCAD simulations show that a particle with such an LET hitting clock-mesh drivers (64X) cannot generate errors. Figure VI-6 compares the typical SET pulses in this case. The pulse widths of 64X and 40X are approximately 0 ps and 10 ps, respectively. Therefore, the daisy-chain buffers instead of the clock-mesh drivers should be the root cause.

Hitting these daisy-chain clock buffers is expected to generate errors in its subsequent shift register chains. However, there were burst errors observed in a single shift register for LET = 10 MeV-cm^2/mg. A test bench is built in Cadence to investigate this unique mechanism. The test bench is shown in Figure VI-7.

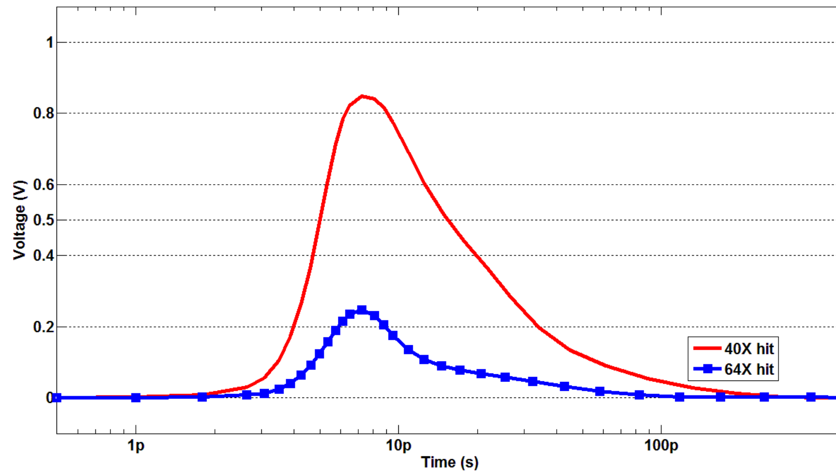

Figure VI-6. The worst-case SET pulses of 64X, 40X hit by a particle of LET=10 MeV-cm^2/mg. The figure is plotted in a log x scale and linear y scale. The figure shows that pulse width of the SET pulses are approximately 0 ps and 10 ps for 64X and 40X respectively.

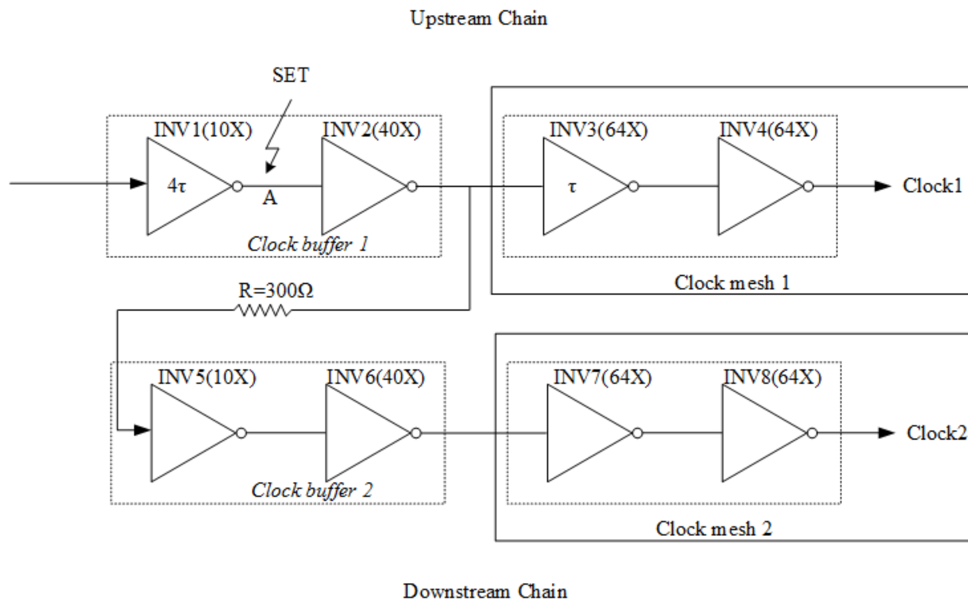

Figure VI-7. The testbench used to simulate a particle of LET=10 MeV-cm^2/mg hitting a 10X inverter. The piece-wise voltage source is injected into Node A.

As demonstrated in this figure, this test bench has two daisy-chain clock drivers (denoted as clock driver 1 and 2 respectively) and their subsequent clock meshes (denoted as Mesh 1 and Mesh 2). In this test bench, a lumped resistor R is inserted between daisy-chain clock drivers 1 and 2 to model the parasitic resistances of a metal wire interconnect.

A voltage source described above with varying amplitude is injected to Node A (the output of the 10X inverter inside the daisy-chain clock driver 1) to simulate a heavy ion strike on a 10X inverter. The outputs of the upstream and downstream chains, Clock1 and Clock2, are chosen as observation points to check SET propagations in these two DFF chains.

Interestingly, if the injected voltage amplitude is between 0.7 and 0.8V, the SET pulse propagates to Clock1, but it gets masked while propagating to Clock2, as illustrated in Figure VI-8. The distinct difference suggests different electrical masking effects for the two clock paths.

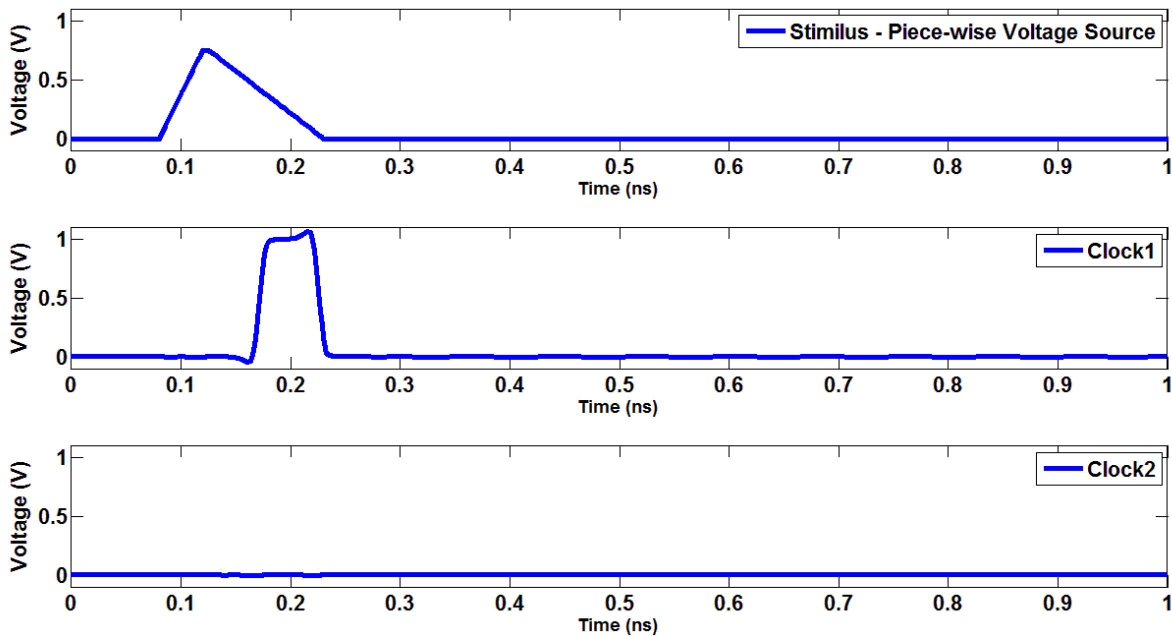

Figure VI-8. The SET goes through the subsequent gates and propagate to Clock mesh 1, but it gets masked while propagating to Clock mesh 2.

This is explained based on the first-order analysis as follows. The delay of an inverter could be approximated as the product of RC, where R is the effective resistance of a transistor and the C is the load capacitance.

For two inverters connected in series, the delay of the inverter is proportional to the size ratio of its downstream inverter vs. itself. For example, if we define the delay of the upstream inverter INV3 as τ (size ratio=64:64=1:1), the delay of INV5 is approximately 4τ (size

ratio=40:10=4:1). The larger delay of INV5 when compared to INV3 results in larger filtering effects.

Thus, some pulses at Node A may not be able to propagate through the downstream daisy-chain clock buffers (for instance, INV5). The parasitic resistor R further enhances the filtering effect, as it introduces extra delay along the propagation path.

6.6 Conclusions

In this paper, two clock networks including clock meshes and daisy-chain clock networks fabricated in a 28nm process have been presented and evaluated. Irradiation experiments demonstrated the significant single event resilience of the clock mesh. Daisy-chain clock buffers were identified to be the weak points in the clock mesh designs.

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VII. A NOVEL BUILT-IN CURRENT SENSOR FOR N-WELL SET DETECTION

Submitted as:

H.-B. Wang, M.-L. Li, L. Chen, R. Liu, "A Novel Built-in Current Sensor for N-WELL SET Detection," *Journal of Electronic Testing*, 2015.

Single event issues can be addressed, to some extent, by using hardened designs. Previous chapters are associated with these designs. In this manuscript, an alternative approach is presented. This approach uses built-in current sensors targeted to sense single event induced currents in the n-well. These sensors were simulated and fabricated in a 28nm CMOS process. Two photon lasers were used to test them. By applying these sensors in a large ASIC system, single event strikes can be detected and then execute fault correction actions, if implemented.

A Novel Built-in Current Sensor for N-WELL SET Detection

H.-B. Wang, M.-L. Li, L. Chen, R. Liu

Abstract

This paper presents and evaluates a new built-in current sensor used to detect n-well single-event transients (SETs) induced by radiation strikes in integrated circuits (IC). A 28nm bulk CMOS test chip containing the proposed sensor design was irradiated by two-photon absorption lasers. Both simulation and experimental data confirm the validity of the proposed design and demonstrate that it can be used for SET detection in advanced technology nodes. Simulation results also demonstrate that this structure has increased SET detection capability across a wide range of voltage and temperature when compared to the reference design. This comes at the expense of minor area overhead.

Index terms

Single event transient, built-in self-test, integrated circuit reliability, electrical test, ionizing radiation.

7.1 Introduction

When micro-electronic circuits are exposed to radiation environments, electron-hole pairs may get generated and then disrupt the normal operation of the system [1]. Such phenomena are called Single Event Effects (SEEs). SEEs have not only been observed in outer space and at high altitude, but also have been reported at ground level [2][3].

There have been circuit hardening techniques of mitigating SEE errors at different levels, i.e., gate level, circuit level, or system level [4][5]. All these techniques are somewhat involved with time or spatial redundancy, for instance, Dual Interlocked Storage Cell (DICE), guard gate, temporal hardening, or Triple Modular Redundancy (TMR) [6][7][8][9]. DICE seems to be

appealing to designers and enjoy a wide popularity in the industry, because it demonstrates immunity to single node charge collection.

However, as the feature size gets smaller, such designs have been found to be more susceptible to single event strikes. Experimental results have shown that DICE is only 20X, 5X, or 1.5X when compared to a regular DFF in advanced technology nodes [10][11][12]. Charge sharing, i.e., multiple node charge collection due to a single node strike, has been identified to be the root cause [13].

In addition to these improved designs tolerant to multiple node upsets, an alternative is to detect single event errors and then execute proper fault correction actions [14]. For example, if the sensing circuitry is implemented in a microprocessor, the instructions in the pipeline of the microprocessor can be reloaded and re-executed to avoid any potential error once the detecting circuit senses an SET event.

In our patent [15], we proposed a SET detection circuit capable of sensing the SET current in the n-well. In this paper, we present simulation results by using TCAD and SPICE models of a 28nm bulk CMOS technology. This design has been fabricated on this process and shown to operate reliably under wide voltage and temperature variations. The two-photon absorption (TPA) laser, a means of emulating single event strikes, has been used to inject SET errors. Experimental results verified the functionality of the proposed design.

The rest of the paper is organized as follows: Section II reviews the mechanisms of SET and the existing Built-in Current Sensor (BICS) approaches. The new BICS structure is demonstrated and analyzed with TCAD and SPICE simulation results in Section III. Section IV presents the test chip design, laser test setup, and test results. This paper concludes the work in Section V.

7.2 Background

7.2.1 Mechanisms of SET Currents

Charge sharing may occur in either PMOS transistors or NMOS transistors, but it is much more pronounced in the PMOS transistors (i.e., the n-well) [13]. This is because an ion strike causes bigger voltage perturbations in the n-well than in the p-well or p-substrate and the parasitic bipolar transistors in the n-well may be turned on.

Figure VII-1 shows the cross-sectional view of a PMOS buried in the n-well on a twin-well process. All the electrodes are labeled in this figure. The OFF drain node of a PMOS is believed to be the most sensitive area [1]. As an incident particle strikes the drain and travels in silicon, excess electron-hole pairs are generated along the charge track. Excess holes get collected by the drain through drift, and as a result, the potential of the drain node would go up.

It should be noted that the ion strike also causes the voltage in the n-well to drop, and as a consequence, the potential gradient between the strike location and the n-well contact, which is tied to VDD, is established. The gradient results in electrons exiting through the n-well tie; and the SET current flows in the n-well from the strike location. In the meantime, the parasitic bipolar transistor, whose collector, emitter, and base are the drain, source, and n-well respectively, may also be turned on [13]. The resultant current in the drain gets amplified by a factor of the bipolar gain when compared to the SET n-well current. Therefore, the SET current in the n-well is an indicative measure of a single event strike.

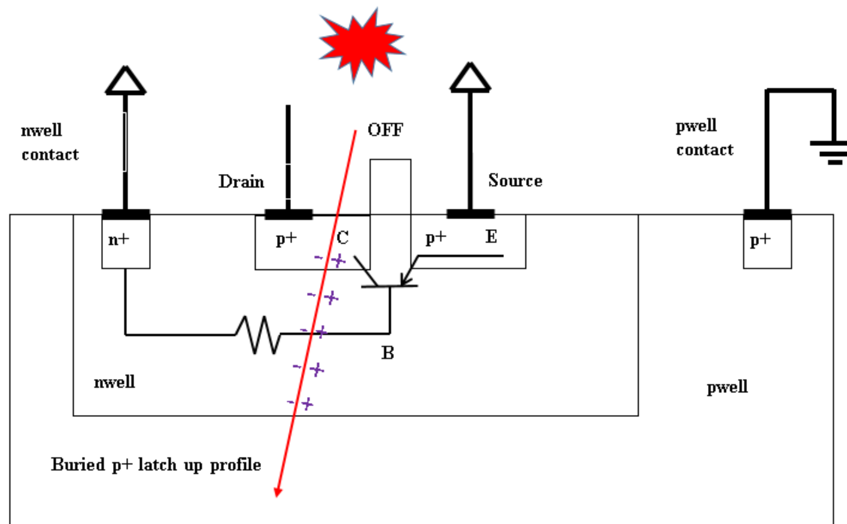

Figure VII-1. The cross-sectional view of a PMOS device fabricated in the n-well on a twin-well process. The well-contacts are connected to VDD. Two parasitic bipolar transistors are formed. One is formed by the drain, source, and n-well; the other one is formed by the source, n-well and p-well. The charge collected by the drain would be amplified if the bipolar transistors are turned on.

7.2.2 Previous Work

Gill et. al. presented a BICS design capable of monitoring SETs in SRAM cell arrays by tapping the sensor to the power rails [16]. However, this solution does not work properly for combinational logic because the currents of logic signals propagating through the logic and those of SETs cannot be effectively differentiated [17].

For this reason, various BICS designs with sensing transistors connected to the n-well (or bulk) contacts of monitored transistors have been proposed [17-19]. They are able to sense n-well (or bulk) SET currents. Zhang at. al. introduced an area and power efficient variant by removing the bias circuitry [20]. Its schematic is shown in Figure VII-2. This is the reference design used in our paper.

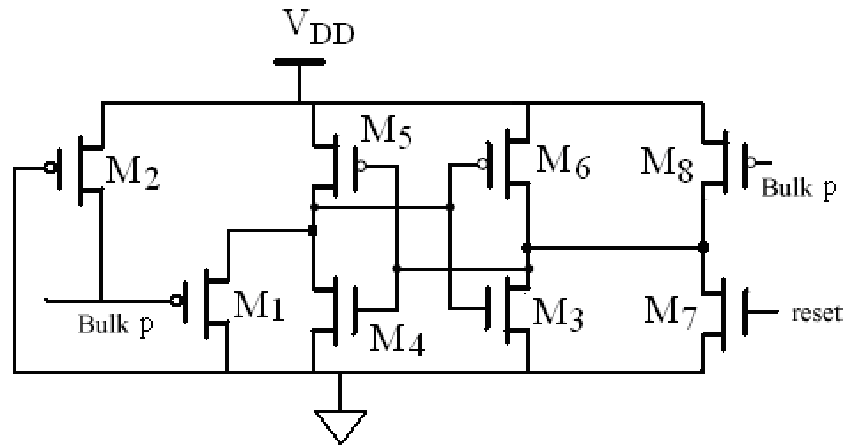

Figure VII-2. The structure of the BICS presented in [20]. This is the reference design in this work.

To ensure the normal operation of PMOS transistors in the n-well, the pn-junctions of these PMOS need to be reverse-biased. Therefore, the sensing transistor M2 has to be large enough in order to provide a good conduction path to VDD. On the other hand, an SET-induced voltage perturbation may not be able to flip the latch as a result of the large capacitance introduced by M2.

The number of detectable transistors in the n-well is limited by M2. Simulations performed on the reference design indicate that a single BICS can effectively monitor from tens to hundreds of transistors in a 90nm technology process [20].

For complex and large-scale circuits, a large number of BICS detection circuits have to be implemented because the sensitivity of previous designs is limited by the sensing transistor. This will introduce large area overhead inevitably.

7.3 Proposed Design and Simulation Results

7.3.1 Operating Principles of the Proposed Design

In our patent [15], we proposed a new current-mode BICS for detecting SETs in sequential and combinational logic with better sensitivity and reduced area cost. The schematic of the sensing circuit is shown in Figure VII-3. The design is composed of three parts: a current conveyor, a current amplifier, and an asynchronous latch.

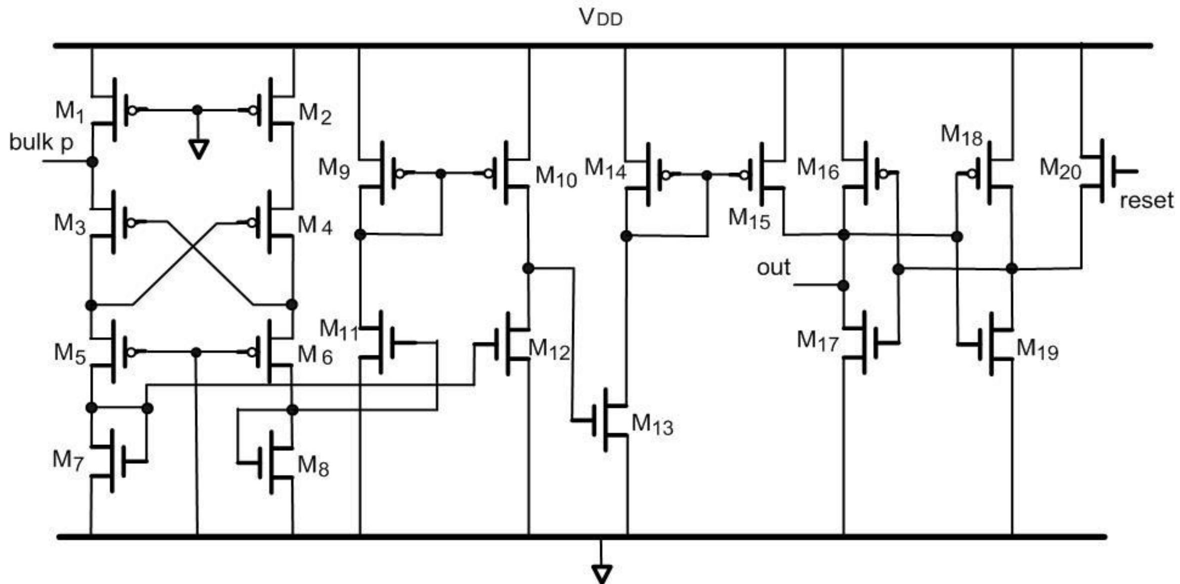

Figure VII-3. The schematic of the proposed BICS detection circuit. The drain of M1 (i.e., bulk_p) is connected to the n-well contacts.

The current conveyor circuit contains transistors M1-8. The drain of M1 is connected to the n-well contacts. Similar to previous work, the n-well potential of PMOS transistors is held at VDD through M1. M2 is added to obtain the symmetrical potential between the "bulk_p" and "bulk_ref" at the drain of M2. Due to the relative large capacitance at the node of "bulk_p", a current conveyor is built by M3, M4, M5, and M6 to transfer the current to the differential voltage signals at the drain of the M5, and M6 with the load of M7 and M8.

The next part is the amplifying stage composed of transistors M9-15. It includes a differential amplifier (M9-12) and a common-source amplifier (M13-14). Through the amplifier stage, the current detection sensitivity is greatly increased.

The last stage is a latch built by M16-20 to store the information of an SET occurrence. After the circuits are powered on, the state of the latch, whose output node is labeled as out in Figure VII-3, is initialized to logic LOW by applying a positive reset pulse at the input reset. When an SET event is induced by radiation strikes, the logic state of the latch will be flipped and stay until a new reset signal excites the circuit.

7.3.2 TCAD Simulation Setup and Results

The single event effects induced by a particle hit depend on many factors, for instance, the size or load of the struck device, the angle or LET of the incident particle, etc. [21][22]. It is therefore extremely difficult to characterize the SET pulse in a technology process.

However, for the purpose of simulation analysis, a double exponential current source has been used by researchers to model particle-induced SET current on a CMOS transistor [23][24][20]. It is expressed as

$$I_{in}(t) = I_0\left(e^{-t/\tau_F} - e^{-t/\tau_R}\right) \quad (1)$$

where τ_F is the decay time of the current pulse, τ_R is the time constant for initially establishing the ion track, and I_0 is the maximum current.

In order to find out these parameters in a 28nm technology node, we have used Accuro to simulate single event strikes on two inverters of different sizes. Accuro is a TCAD tool capable of building a full 3D representation of the design based on its layout file and doping profiles. It has been used in previous work [25][26].

Figure VII-4 illustrates the typical SET pulses of a 64X inverter hit by a particle of LET=1.25, 2.5, 5, or 10 MeV-cm^2/mg. Although its pulse amplitude in all cases varies, the risetime is approximately in the orders of 10ps, and the falltime is in the orders of 100ps.

In our SPICE simulations, the SET pulse is characterized as a double exponential current source, whose risetime and falltime are 5ps and 100~500ps respectively.

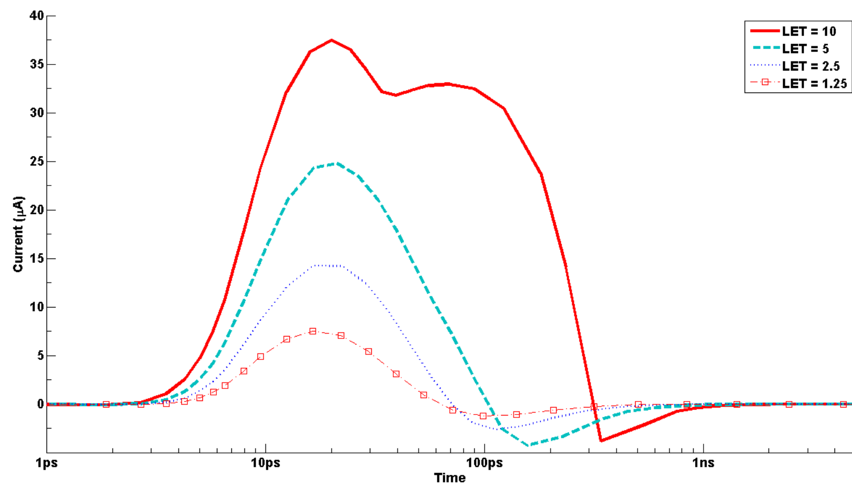

Figure VII-4. The SET pulse of hitting a 64X inverter by a heavy ion particle of LET=1.25, 2.5, 5, or 10 MeV-cm^2/mg

7.3.3 SPICE Simulation Results

Figure VII-5 shows the test bench throughout our work. The test vehicle is 1K inverters. We connect the proposed current-mode BICS to the body-ties of the test vehicle.

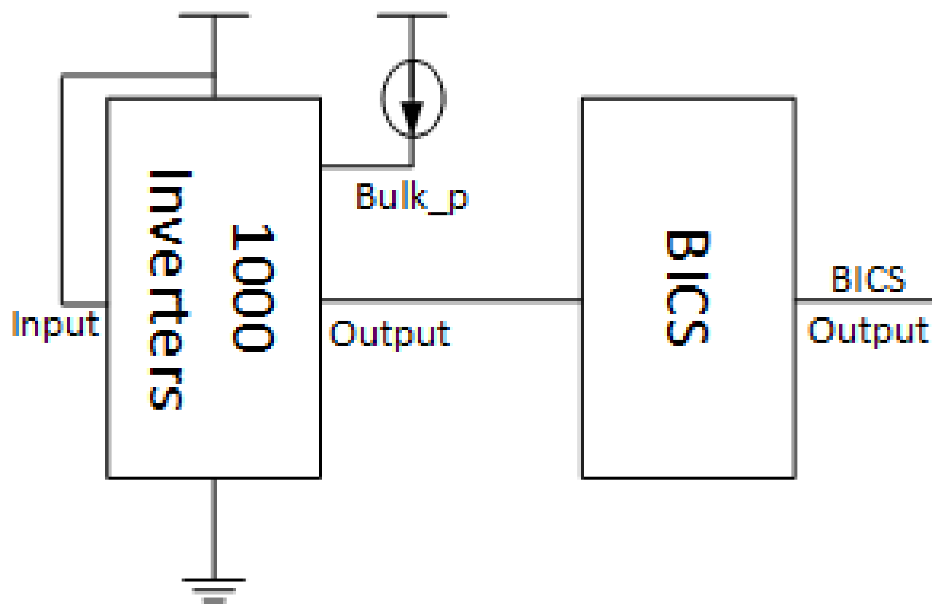

Figure VII-5. Test bench used throughout the work to simulate the functionality of the proposed BICS design. The body ties of these 1K inverters are connected to the BICS sensor.

The sensitivity of the BICS SET sensor is determined by current pulse length. The minimum peak trigger current is simulated over a range of pulse lengths, as shown in TABLE VII-1. The parameters of the current source are configured as follow -- $\tau_R = 5$ ps, but both τ_F and I_0 are varied. This table shows that a SET pulse peak as small as 12 µA may be detected if the pulse length increases to 500ps.

Impact of supply voltage on its sensitivity is also evaluated by simulations. TABLE VII-2 depicts the worst-case results for a VDD variation of +/- 10% when $\tau_R = 5$ ps and $\tau_F = 200$ ps. This shows that the BICS structure is very sensitive to the supply voltage. As the supply voltage drops by 10%, its minimum current peak increases by 4X. As a result, maintaining the supply voltage at the standard voltage level is very critical.

TABLE VII-1 MINIMUM CURRENT PEAK VS. PULSE LENGTH

Pulse Length	Minimum Current Peak
100ps	90 µA
200ps	50 µA
300ps	18 µA
400ps	14 µA
500ps	12 µA

TABLE VII-2 COMPARISON OF MINIMUM CURRENT PEAK

Voltage	Minimum Current Peak
0.9V	250 µA
1V	50 µA
1.1V	20 µA

7.3.4 Comparative Analysis

The number of detectable transistors is a critical factor for a complex VLSI system. For the reference BICS sensor, 290 transistors can be monitored in this 28nm technology, if the transient exponential current pulse with rising time of 5ps, falling time of 300ps, and magnitude of 1000 µA, is injected to the monitored PMOS transistors.

By comparison, the proposed design has significant improvement in detectable transistor counts, as demonstrated in TABLE VII-3.

TABLE VII-3 NUMBER OF DETECTABLE TRANSISTORS

Current Peak	τ_F = 100 ps
100 µA	5.5K
200 µA	24K
500 µA	80K
1000 µA	180K

TABLE VII-4 compares the minim current peak between the proposed design and the reference design at different temperatures where τ_R = 5 ps and τ_F = 200 ps. The data clearly shows that the proposed design has improved performance when compared to the reference design.

TABLE VII-4 COMPARISON OF MINIMUM CURRENT PEAK

Temperature	Proposed Design	Design in [20]
-25^0	550 µA	4 mA
25^0	40 µA	4.1 mA
50^0	30 µA	4.2 mA

7.4 Test Chip Design and Experimental Results

7.4.1 Test Chip Design

A test chip containing two proposed BICS designs and an inverter was fabricated on a 28nm CMOS bulk process, as shown in Figure VII-6. Two BICS circuits are placed either 2µm or 8µm away from the inverter.

The inverter servers as the source of SET currents. The input of the inverter is tied to VDD, and thus, the PMOS is turned OFF and it is sensitive to single event strikes. By striking this inverter using heavy ion particles or laser beams, SET currents will be generated in the n-well and then detected by the SET current sensors.

The reset signal is shared by these two BICS sensors and connected to an I/O pad. Each of the sensors has an individual I/O pad for its latch output. Buffers are added to improve the drive capability of the latch of the sensor. Since these buffers do not affect the circuit from the functionality point of view, they are not shown in this figure.

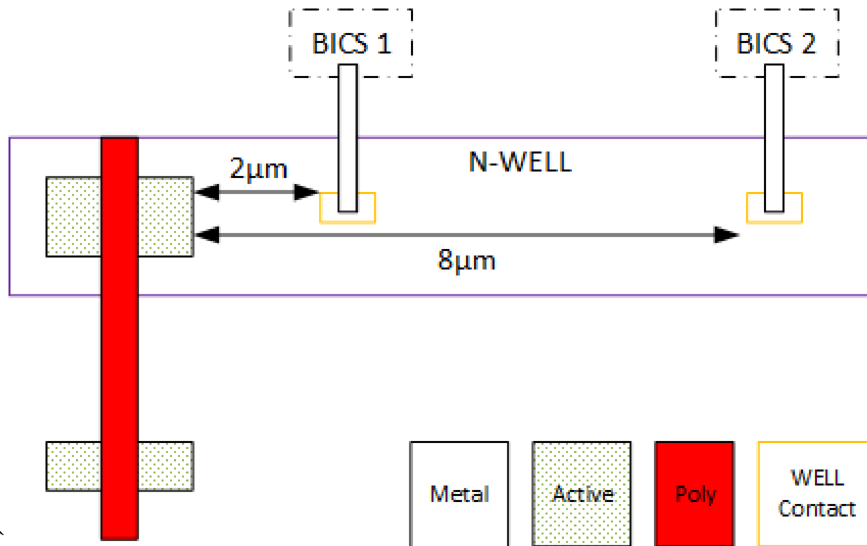

Figure VII-6. The test circuit composed of two BICS sensors along with a target inverter fabricated in a 28nm technology node.

The test chips were in a wire-bonded package. In order to carry out the backside laser irradiation, the front side was fixed first with an underfill process, and then the backside of the chips were opened, and thinned and polished. The thickness of the die is about 120um after the process. The backside of the die after thinning and polishing is shown in Figure VII-7.

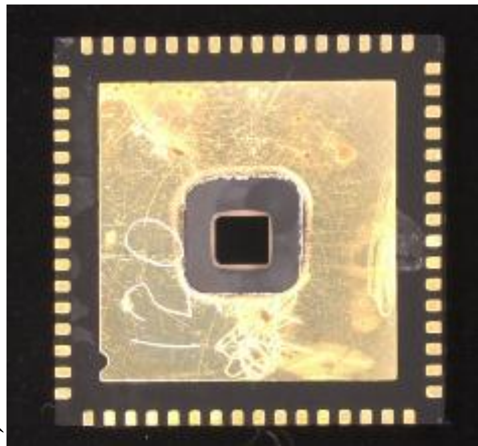

Figure VII-7. The diagram of the package backside after thinning and polishing.

7.4.2 Laser Setup

The irradiation facility used to carry out the laser experiments is the two-photon-absorption laser system located in the SSSC at University of Saskatchewan, as shown in Figure VII-8. It includes a Ti:Sapphire pulsed laser facility and a Laser Scanning Microscope (LSM).

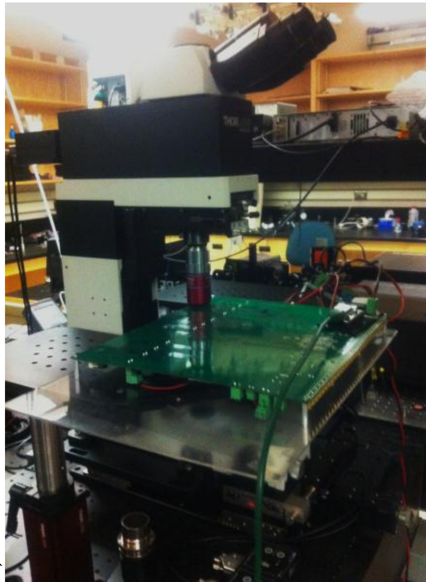

Figure VII-8. The laser setup

The pulsed laser system uses a continuous wave (CW) green diode-pumped solid-state (DPSS) laser as the pump laser, which provides 18W output at 532 nm. Its output goes into a regenerative amplifier (RegA) who uses Ti:Sapphire as its gain medium. The RegA can provide a repetition rate from 10 Khz to 300 Khz internally. To achieve an even lower repetition rate for the testing, an external signal generator is connected to its time controller. In fact, 1 kHz is used in our experiments. Note that the RegA is also seeded with a femtosecond pulsed laser.

The pulse energy of the seed laser is amplified dramatically by the RegA. After that, it is injected into an optical parametric amplifier (OPA) which extends the wavelength coverage. In our experiment, the 1250 nm wavelength is adopted. The final output of the pulsed laser system is merged with imaging laser and sent to the optical path of the LSM. The imaging laser is applied on the DUT and its reflection photons are collected by a detector and sent to the computer for image processing.

The X-Y-Z directions are fully controlled by the computer with a step size of 0.05 μm for XY and 0.1 μm for Z. During the scan, the area is divided into 256 by 256 pixels with a dwell

time of 5 µs on each pixel. Thanks to the 50X objective, the minimum area can reach to 3.84 µm by 3.84 µm, which provides decent accuracy in the experiments.

7.4.3 Laser Test Results

The supply voltage was varied from 1V to 0.8V to power up the test chip. The device under test (DUT) mounted on a daughter card is controlled by a Xilinx Virtex-5 FPGA board. The FPGA program generates a reset signal for the DUT and keeps record of the output voltage in real-time for each sensor. These logic values are sent to the computer via an Ethernet port for processing. Table V shows the recorded BICS1 output voltage and laser energy per pulse. If the sensor detects a SET pulse, its voltage flips to logic High, otherwise it is logic Low.

TABLE VII-5 BICS1 OUTPUT VOLTAGE VS. LASER ENERGY

Laser Energy (pJ)	BICS1 @ 1V	BICS1 @ 0.9V	BICS1 @ 0.8V
40	L	L	L
60	H	L	L
80	H	L	L
100	H	L	L
120	H	H	L
140	H	H	L
160	H	H	L
180	H	H	H

The laser energy per pulse ranging from 40 pJ to 180 pJ was used to irradiate the inverter. The laser energy thresholds of BICS1 were found out to be approximately 60 pJ, 120 pJ, and 180 pJ for 1V, 0.9V, and 0.8V respectively. This agrees very well with our simulation results: these sensors are very sensitive to voltage variation. If the voltage drops by 20%, the laser energy threshold goes up by 2X.

7.5 Conclusions

In this paper, we have presented and evaluated a novel current sensing circuit intended to detect SETs. It has high detection sensitivity to SETs with small area overhead. Both simulation

results and irradiation data demonstrate the validity of the structure. Applying this structure is an effective way to detect SEE errors in logic or sequential circuits.

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VIII. SUMMARY, CONTRIBUTIONS, AND FUTURE WORK

8.1 Summary

This work examines the single event effects in critical digital system components, namely latches, dynamic logic circuits, and clock networks. Existing hardening techniques, such as DICE, have been rendered more vulnerable to single event strikes due to charge sharing in deep submicron and advanced technologies. Moreover, this work explores new hardened designs. These designs are summarized below:

1. Two tolerant latch designs taking advantage of resistive hardening techniques:
   - A modified DICE structure with four more transistors than DICE demonstrates fewer sensitive nodes, higher upset LET threshold, and a reduction in cross-section magnitude. However, these improvements are at the expense of non-significant area, power, and delay overhead.
   - A Quatro variant is demonstrated with single node upset immunity. This is achieved by adding two feedback transistors. The transistors are turned OFF when the latch in the hold mode, thereby yielding considerable resistance in this mode. On the other hand, they are turned ON in the write state, thereby incurring a small area and power penalty.
2. Two single event tolerant dynamic logic designs:
   - A feedback capacitor is added to the feedback path across the static inverter of the dynamic logic circuit. The nodal capacitance of the output increases, which translates to a larger critical charge. This capacitor also increases the feedback time, rendering the output node more resilient.
   - A differential-style dynamic logic is investigated in terms of overhead and single event performance. This design does not encounter the upset issues characteristic of the regular dynamic logic circuit. Instead, it only has SET issues as standard logic. Its intrinsic features of high speed and single event tolerance render it favorable in these applications, as area and power are not the most critical constraints.
3. A current sensor design used to detect single event strikes:

- A novel current sensor design is presented. This sensor is capable of detecting a large number of transistors through the process of sensoring the SET current in the n-well. It can be used for both memory and logic circuits.
- This design is simulated using SPICE models. Its performance is subsequently evaluated across process variation, temperature, and supply voltage. Laser irradiation results substantiate its validity.

4. Single event performance evaluation of clock networks:

- Two clock structures – clock mesh and daisy chain clock – were evaluated and compared in terms of single event performance. These structures were contained in a 28nm CMOS technology. Clock errors became apparent at high LET values (>10Mev*cm^2/mg).
- Two photon lasers were used to verify the heavy ion results. Daisy-chain clock buffers demonstrated a significantly lower upset threshold relative to clock mesh.

8.2 Contributions

The central contributions of this work are related to single event effects in advanced technology nodes and single event tolerant designs.

I proposed two single event tolerant flip-flop designs, both of which have a significantly higher upset threshold and cross-section reduction in comparison to the reference designs. These designs have been published in the *IEEE Transactions on Nuclear Science* journal. Other proposed designs are under review by this journal.

Moreover, my study demonstrates that a SR latch built with NAND gates is more sensitive to single event strikes, as compared to a regular latch built with INVs. A SR latch is a widely popular commodity in the industry, as it is conceived to be the most flexible form of latches with the ability to be converted to other types by means of simple extra logic circuits. However, my research suggests that SR latches must be used with caution in ASIC applications.

It is worth noting that I was the first person to identify the superior single event tolerance of the differential-keeper-based dynamic logic. This type of circuit does not encounter single event upset issues, which are intrinsic problems characteristic of regular dynamic logic circuits with

cut-off pull-up paths. Instead, it has only single event transient issues. My findings conclusively suggest that dynamic logic, with the associated decrease in radiation susceptibility, may be advantageous in fault-tolerant high-speed applications.

8.3 Future Work

By implementing the latch and dynamic logic designs demonstrated in this work in nano-technologies, such as a 28nm bulk CMOS node, evaluating their single event performance under different voltage and frequency conditions, and comparing these results with the existing data in a 130nm technology, the trend of single event tolerance of these designs will be determined, projecting their validity to more advanced technology nodes. Moreover, noise analysis will be needed in order to improve these circuits' performance and make them more robust with the interference with various noise sources.

In our work, a current sensor detecting the n-well SET has been fabricated and tested through the use of two-photon lasers. By exposing this sensor to micro-beam heavy ions, the correlation of laser energy with heavy ion LET values will be able to be determined, thereby providing a guideline for implementing these sensors in space and ground applications.

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