A 0.18µm CMOS UWB Wireless Transceiver for Medical Sensing Applications

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ABSTRACT

Recently, there is a new trend of demand of a biomedical device that can continuously monitor patient's vital life index such as heart rate variability (HRV) and respiration rate. This desired device would be compact, wearable, wireless, networkable and low-power to enable proactive home monitoring of vital signs. This device should have a radar sensor portion and a wireless communication link all integrated in one small set. The promising technology that can satisfy these requirements is the impulse radio based Ultra-wideband (IR-UWB) technology.

Since Federal Communications Commission (FCC) released the 3.1GHz-10.6GHz frequency band for UWB applications in 2002 [1], IR-UWB has received significant attention for applications in target positioning and wireless communications. IR-UWB employs extremely narrow Gaussian monocycle pulses or any other forms of short RF pulses to represent information.

In this project, an integrated wireless UWB transceiver for the 3.1GHz-10.6GHz IR-UWB medical sensor was developed in the 0.18µm CMOS technology. This UWB transceiver can be employed for both radar sensing and communication purposes. The transceiver applies the On-Off Keying (OOK) modulation scheme to transmit short Gaussian pulse signals. The transmitter output power level is adjustable. The fully integrated UWB transceiver occupies a core area of $0.752\,mm^2$ and the total die area of $1.274\,mm^2$ with the pad ring inserted. The transceiver was simulated with overall power consumption of 40mW for radar sensing. The receiver is very sensitive to weak signals with a sensitivity of -73.01dBm. The average power of a single pulse is 9.8µW. The pulses are not posing any harm to human tissues. The sensing resolution and the target positioning precision are presumably sufficient for heart movement detection purpose in medical applications. This transceiver can also be used for high speed wireless data communications. The data transmission rate of 200 Mbps was achieved with an overall power consumption of 57mW. A combination of sensing and communications can be used to build a low power sensor.

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List of Abbreviations

A/D	Analog to Digital converter
ASIC	Application Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
DRC	Design Rule Check
DS-OFDM	Direct Sequence Orthogonal Frequency-Division Multiplexing
EIRP	Equivalent Isotropic Radiated Power
FCC	Federal Communications Commission
FHSS	Frequency Hopping Spread Spectrum
HRV	Heart Rate Variability
IC	Integrated Circuit
ILO	Interlevel Oxide
IR-UWB	Impulse radio ultra-wide band
LNA	Low Noise Amplifier
MOS	Metal Oxide Semiconductor transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
nMOS	n-channel MOS
OOK	On-Off Keying
PAM	Pulse-Amplitude Modulation
pMOS	p-channel MOS
PPM	Pulse-Position Modulation
RF	Radio Frequency
SNR	Signal to Noise Ratio
TSMC	Taiwan Semiconductor Manufacturing Company Ltd.
UWB	Ultra-wideband

Chapter 1 Introduction

In the last decade, the technology advancements in the standard CMOS silicon process have made the realization of small-size, low-power, and complex multi-functional integrated circuit possible. More and more Application Specific Integrated Circuit (ASIC) chips are now being designed specifically for biomedical applications.

1.1 Motivation

Since Federal Communications Commission (FCC) released the 3.1-10.6GHz frequency band for UWB applications in 2002 [1], numerous researches have concentrated on the UWB technology and its applications. The UWB is defined as a modulated transmission with more than 20% fractional bandwidth, or at least 500MHz of bandwidth [1]. Among a few currently available UWB technologies such as direct sequence orthogonal frequency-division multiplexing (DS-OFDM) and frequency hopping spread spectrum (FHSS), the impulse radio based UWB (IR-UWB) technique uses extremely short Gaussian monocycle pulses as signal. This technology opens a new era of practical applications in medical sensing, one of which is the human heart motion detection [2].

Ultra-wideband (UWB) has received significant attention for applications in target positioning and wireless communications recently. The very fundamental character that

differentiates IR-UWB from the conventional wireless communications is the absence of carrier signals. IR-UWB employs extremely narrow Gaussian monocycle pulses or any other forms of short RF pulses to represent information. The extremely short pulses in turn generate a very wide bandwidth and offer several advantages, such as large throughput, covertness, robustness to jamming, lower power, and coexistence with current radio services [3]. IR-UWB not only can transmit a huge amount of data over a short distance at very low power, but also has the capability to pass through physical objects that tend to reflect signals with narrow bandwidth.

Ultra-wideband communications is not a new technology; in fact, it was first employed by Guglielmo Marconi in 1901 to transmit Morse code sequences across the Atlantic Ocean using spark gap radio transmitters [4]. From the 1960s to the 1990s, this technology was restricted to military and the United States Department of Defense applications under classified programs such as highly secure communications. However, the recent advancement in micro-processing and fast switching in semiconductor technology has made IR-UWB ready for commercial applications. Therefore, it is more appropriate to consider UWB as a new name for the long-existing technology [3]. Figure 1.1 shows the IR-UWB development history.

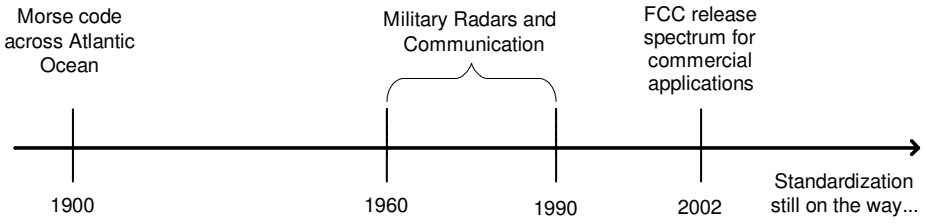


Figure 1.1 IR-UWB development timeline [3]

The idea of monitoring physiologic functions in humans using radars started as early as the 1970s [5], but further development was hindered by the clumsy and expensive technology of those years until the commercially affordable low-power CMOS technology became mature in the 1990s. An UWB radar biomedical application was first proposed in 1998 [6], and a few years later, several U.S. patents describing its medical applications were claimed [7,8,9]. One of the most cited work is done by Thomas McEwan at U.S. Lawrence Livermore National Laboratory [5]. McEvan described

promising medical applications, and emphasized that the "device is medically harmless, as the average emission level used (about 1μW) is about three orders of magnitude lower than most international standards for continuous human exposure to microwaves" [9]. The most recent progress has been made by Wireless2000, and their first UWB commercial product, the PAM 3000, which detects heart and respiration rate is released in the middle of 2007 [10].

Recently, there is a new trend of demand for a biomedical device that can monitor patient's vital life index such as heart rate variability (HRV) and respiration rate [11]. To be useful, the device must be small, wearable, and wirelessly networkable. This small comfortably wearable device would enable proactive home monitoring of vital signs, which in an aging population could decrease the cost of healthcare by moving an amount of eligible patients from hospital to homecare. This device could also provide prevention or early diagnostics for pathological patients. The networkability enables the device to transmit and share the monitored data with other systems or even the hospital monitoring center. This requires a communication link from the wearable sensor to a base station. This device should have a radar sensor portion and a wireless communication link all integrated in one small set. The technology that can fulfill these requirements is the impulse UWB technology. The physical characteristics of UWB short pulse make it possible to achieve both high data rate transmission and accurate radar sensing. Because of the wide frequency content of the UWB signal, it can penetrate biological materials such as skin, fat, and other organic tissues, and the reflection from the internal organs provides means to monitor vital signs, etc. [5,8,11]. Also, researches showed that the ultrawide band pulses are harmless to human tissues [3,11].

Unlike ultrasound device, which is being widely used at the present time that requires direct skin contact, the IR-UWB makes imaging internal organ movements without invasive surgical or direct skin contact possible. Another advantage in using IR-UWB technology is that the UWB transceiver is simple and occupies a very small chip area as it does not require complex frequency recovery system as in the narrow bandwidth transceiver. In addition, power consumption of the impulse based UWB systems is extremely low because the power is consumed only during pulse transmitting period. This is an asset for battery-driven device.

A few examples of UWB radar systems for biomedical sensing applications are in [12,13,14] and the PAM 3000 made by Wireless2000. The system in [14] uses discrete electronic components on PCB, and the large physical dimension and high power-consumption (compared to the low power expectation of the UWB) drawn by the discrete components makes this device not the best candidate specifically for wearable sensor, not mention the networkability. The PAM 3000 is designed to be placed underneath the patient's mattress for stationary monitoring; again, it is not for wearable sensor. The IR-UWB based sensor proposed in this project is so far an appropriate approach to the wearable heart motion detection solution due to the non-invasive detection, very low product cost, low power consumption for battery-powered device, high miniaturization capability and the environmental friendliness due to its very low electromagnetic energy emission.

1.2 Project Overview and Objectives

The proposed UWB sensor in this project is a wearable heart motion sensor that is non-invasive, contactless and wirelessly connected to a base station data processor. The overall sensor, as shown in Figure 1.2, consists of three parts: an UWB radar unit, a control and DSP unit, and a communication unit.

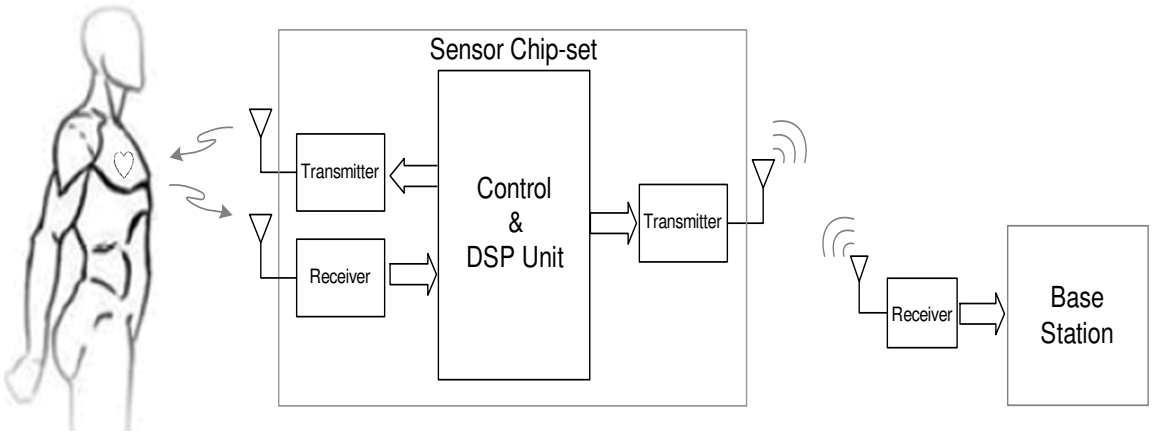


Figure 1.2 Overall system view of UWB bio-sensor

Both the UWB radar unit and UWB communication unit are coordinated by the control and DSP unit. The radar has one transmitter and one receiver. Once the control unit sends a digital control signal to the transmitter in the UWB radar unit, a short pulse is sent from this transmitter toward the human heart, and the radar receiver detects the reflected pulse and converts the received analog pulse into a digital bit, and then this digital bit is sent back to the control and DSP unit. This completes one sensing period. Instead of using only one pulse for each sensing period, many pulses (five pulses in this project) are used to make the reflected signal detection in the receiver easier by increasing the signal SNR. By measuring the time interval between the control signal and the reconstructed digital bit, a distance between the heart and the transceiver can be calculated in the control and DSP unit. More details on radar sensing will be introduced in Chapter 2. The DSP unit can either send the calculated heart rate to a base station nearby or the raw data to the same base station for more complicated processing, through the communication unit. Similarly to the radar sensing unit, the communication unit includes a transmitter and a receiver. The transmitter and the receiver for communications are on the same chip as the ones for radar sensing, but with different tune-ups for communication purpose. The communication unit is specifically tuned to achieve high data transmission with very short pulse period, where as the radar sensing unit is tuned to send more pulses in one sensing period but the sensing period is very long.

The overall goal of this project is to design and simulate an UWB wireless Radar/Communication transceiver biosensor device for human heart motion detection. The design objectives for this sensor system are as follows:

- Modulation Schemes: On-Off Keying (OOK).
- The radar sensor and communication transceiver functions as proposed.
- Verify the circuit design at schematic simulation and post-layout simulation.
- Transceiver layout in 0.18µm CMOS ready for fabrication.
- Data transmission rate of 200 Mbps for the communication unit

1.3 Thesis Outline

There are four primary topics of interest discussed in this thesis, including IR-UWB radar and IR-UWB communication background, IR-UWB based transceiver design, transceiver layout in 0.18µm CMOS technology, and simulation performances of the overall system. The thesis work begins with Chapter 2 which describes the background of UWB communications and radar technology as it is the foundation for the design of the heart motion sensor. Chapter 3 presents the heart motion detecting methodology and architecture of the impulse-based UWB transceiver followed by circuit design of each individual radar transceiver blocks. UWB antenna and some other design issues are also discussed. In Chapter 4, circuit layout consideration and transceiver layout design in 0.18µm CMOS are presented. This will lead into Chapter 5 where the design simulations are analyzed. Finally, the conclusion and suggestions for future work are given in Chapter 6.

Chapter 2 Impulse Radio UWB Background

The goal of this chapter is to provide a brief background of the basic concepts of IR - UWB radar and IR-UWB communication in a simple and easy-to-understood language. It covers the fundamentals of short pulse characteristics, modulations, and concepts behind sensing and communication application considerations as well as IR-UWB's advantages and challenges.

2.1 UWB Concepts

In conventional communication systems, transmitter employs specific carrier frequency to carry information. The signal carrier is a continuous wave (usually a sinusoidal wave) with well-defined energy spectrum in a narrow band, which is very easy to detect. In the IR-UWB case, the transmitter uses very short pulses with a very low duty cycle to represent the information bits. The pulse itself contains the information and is sent directly to the receiver for detection and translation. The very low duty cycle results in a very low average transmission power and since frequency is inversely related to pulse width, the short pulse spread their energy across a wide range of frequencies, which in turn results in a very low power spectral density. Figure 2.1 illustrates the differences between conventional communication system and IR-UWB system in a more interpretative way.

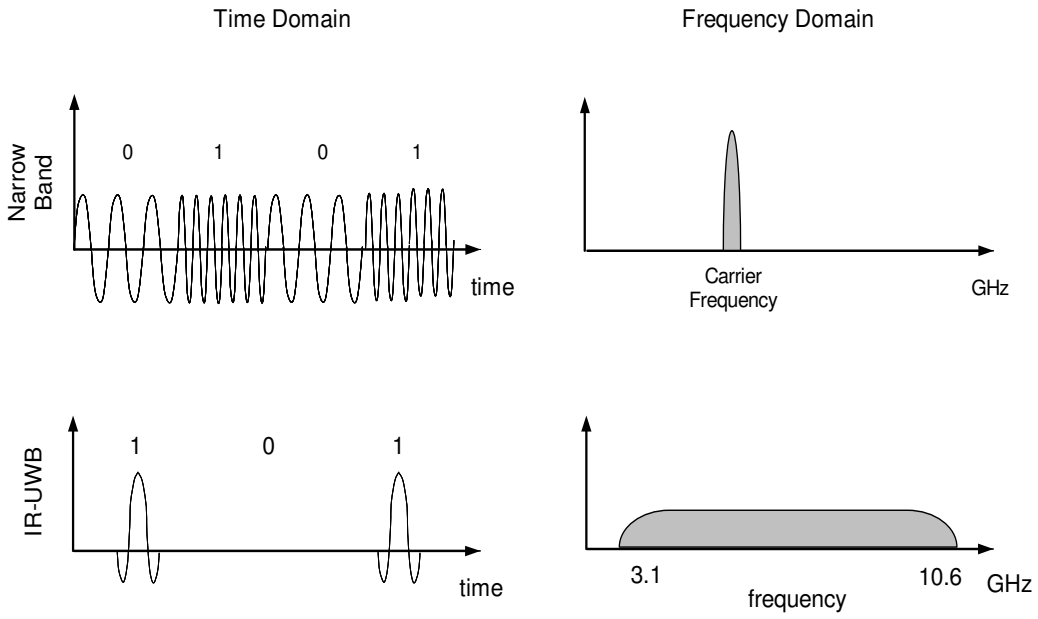


Figure 2.1 Narrowband signal and IR-UWB signal representations

The time-scaling property of the Fourier transforms, shown in Equation 2.1, can provide some insight for the very large bandwidth of the short pulses [3,4].

$$x(at) \leftrightarrow \frac{1}{|a|} X\left[\frac{f}{a}\right] \tag{2.1}$$

Scaling signal by a factor of a in time domain corresponds to the inversely scaling the frequency domain signal by a factor of a. For example, if the pulse has duration of 200 picoseconds, in frequency domain the center frequency f_c is calculated in Equation 2.2.

$$f_c = \frac{1}{T} = \frac{1}{200 \times 10^{-12}} = 5 \times 10^9 \, Hz = 5 \text{ GHz} \tag{2.2}$$

2.2 Impulse UWB Signals

A UWB signal can be any form of short pulse with wideband frequency spectrum such as Gaussian pulse, Gaussian monocycle pulse, wavelet, or chirp pulse. The Gaussian

monocycle pulse, which is the first derivative of Gaussian pulse, has been widely used in current UWB researches. The Gaussian monocycle pulse has the mathematical expression as shown in Equation 2.3 [3]

$$P(t) = \frac{t}{\tau} e^{-(\frac{t}{\tau})^2} \tag{2.3}$$

where t represents time and τ represents a time delay constant that determines the width of the pulse in time domain. The following figures show examples of Gaussian pulse and Gaussian monocycle pulse with a pulse width of 0.2ns and its frequency spectrum. The pulse type in most cases generated from a pulse generator at the transmitter is a Gaussian pulse. However, since after pulse-shaping effects and derivation by antenna, the actual pulse shape in transmission is Gaussian monocycle pulse, that's the reason the Gaussian monocycle pulse receives more attention in UWB communications and channel modeling.

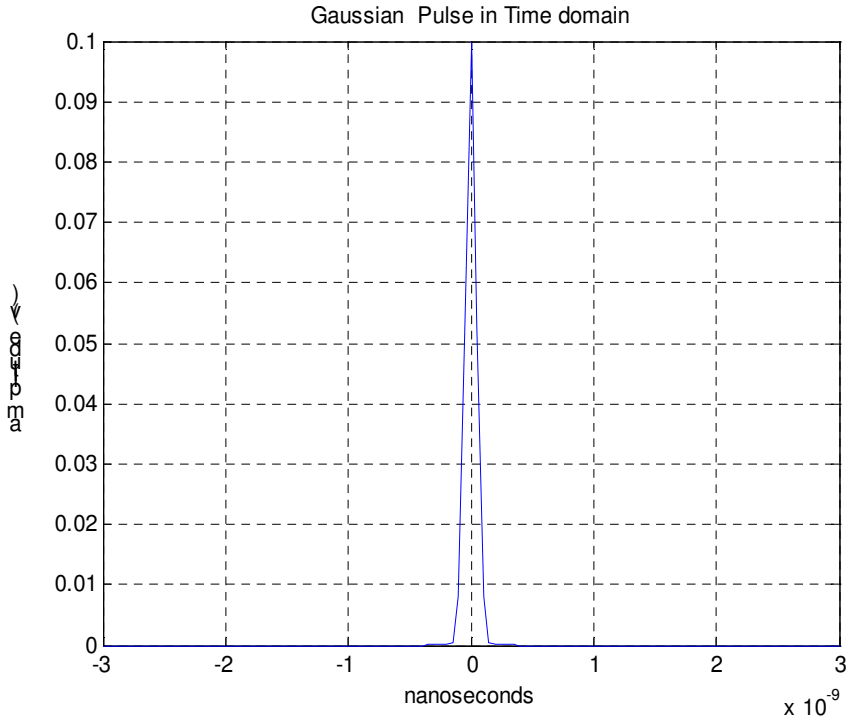


Figure 2.2 An example of Gaussian pulse

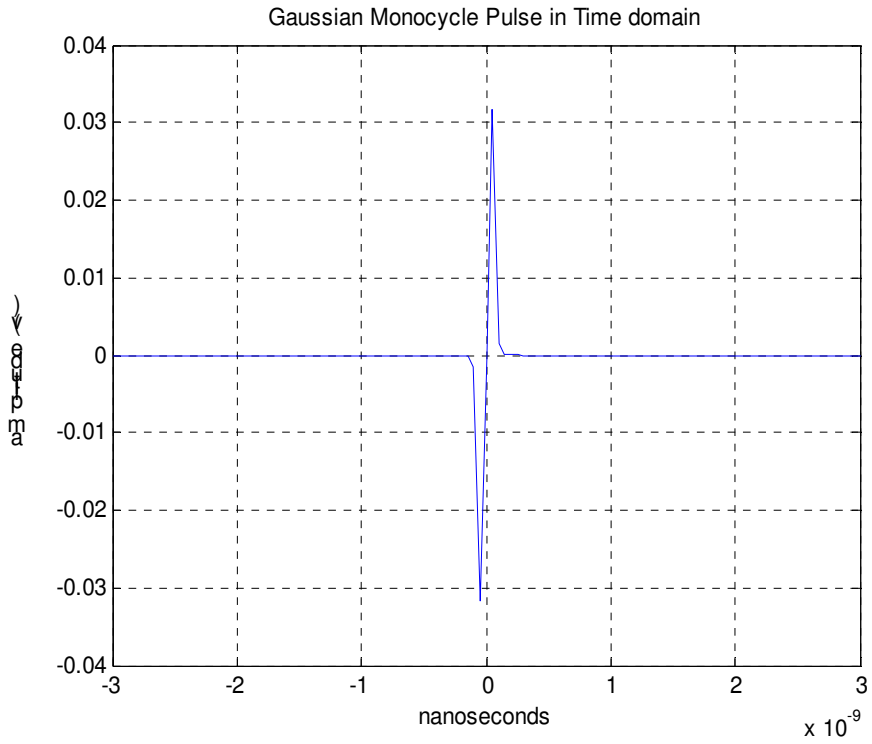


Figure 2.3 An example of Gaussian monocycle pulse

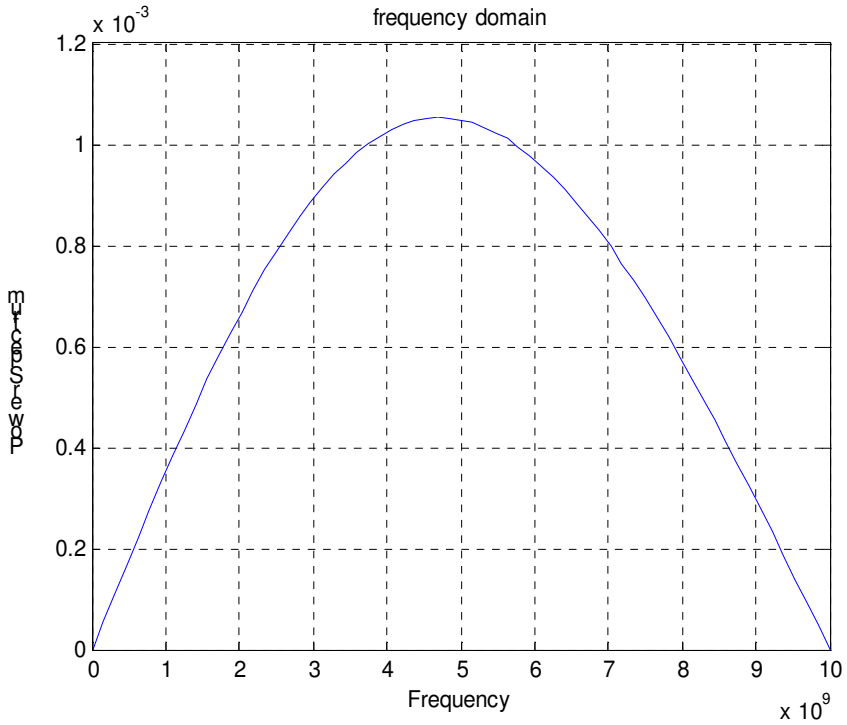


Figure 2.4 Frequency spectrum of a Gaussian monocycle pulse

2.3 FCC Emission Mask

In order to protect the conventional communication systems from interference, the Federal Communication Commission (FCC) assigned a frequency spectrum mask for UWB applications in the 3.1GHz to 10.6GHz frequency band. There are four masks for indoor UWB applications, outdoor UWB applications, through-wall UWB imaging applications, and vehicular radar systems respectively [1,3]. Since this project falls in the category of indoor UWB applications, the first type of emission is considered in the design. Figure 2.5 shows the FCC's emission mask for indoor UWB applications.

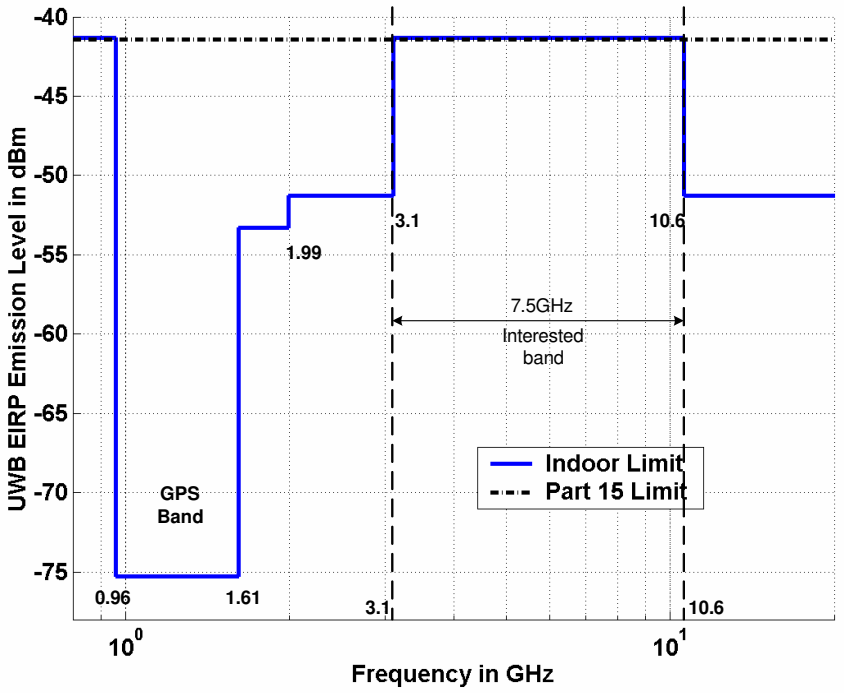


Figure 2.5 FCC indoor UWB applications emission mask [1]

For indoor applications, the average output power spectrum density is limited to -41.3 dBm/MHz between 3.1GHz and 10.6GHz and limited to -53dBm/MHz between 1.99GHz and 3.1GHz. This limitation coexists with the long standing FCC Part 15 general emission limits to controlled radio interference [4]. In this project, the short pulse

frequency content falls in the 3.1GHz to 10.6GHz band. Therefore, the transmitting power spectrum density level in this 7.5GHz frequency band is limited to -41.3dBm/MHz.

It is worth to mention that even the FCC regulated the UWB spectrum, the industrial standardization still remains unfinalized. The FCC masks are guidelines for forming the template for regulations in other countries including Canada.

2.4 Modulation and Detection

In IR-UWB system, the short pulses are directly modulated in time domain to carry the information bits before they are sent out for transmission. A few commonly used pulse-modulation techniques are discussed in this section. They are on-off keying (OOK), pulse-amplitude modulation (PAM), pulse-position modulation (PPM), and biphase modulation. Different modulation technique has different drawbacks and advantages affecting the system design parameters such as resistance to interference and noise, data rate, circuit complexity, and overall system cost.

2.4.1 Pulse-Amplitude Modulation

Pulse-amplitude modulation (PAM) is a one-dimensional signal modulation that modulates the narrow pulse amplitude to two amplitude levels corresponding to bit 1 or bit 0 [4]. By convention, the pulse with high amplitude represents data 1 and the low amplitude represents data 0. The modulated signal can be expressed in by Equation 2.4:

$$s(t) = \sum_{m=1}^{\infty} a_m \cdot P(t - mT) \qquad (2.4)$$

In this expression, ∞ shows the data bits are transmitting continuously, $P(t)$ represents the extremely narrow energy pulse, a_m stands for the two possible amplitudes for information bit, 1 or 0. T is the pulse period (pulse duration and the rest in one cycle). Figure 2.6 shows an example of the output signals by PAM.

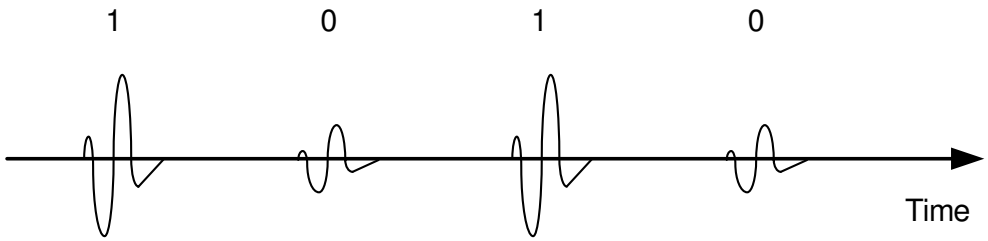


Figure 2.6 Pulse-amplitude modulation

PAM implementation is relatively simple since it requires only single polarity to represent data. PAM-type demodulator relies on energy detector to recover data. However, PAM is sensitive to noise and attenuation can make '1' and '0' undistinguishable.

2.4.2 On-Off Keying

The OOK pulse modulation is a special case of PAM. This modulation transmits a pulse if the information bit is 1, and transmits nothing if the information bit is 0. The modulated signals can be represented in time domain by

$$s(t) = \sum_{m=1}^{\infty} b_m \cdot P(t - mT) \tag{2.5}$$

where in this expression, ∞ shows the infinite number of transmitted bits, $P(t)$ is the extremely narrow pulse, b_m stands for the information bit, either 1 or 0. T is the pulse period (pulse duration and the rest in one cycle). Figure 2.7 shows how the OOK modulation scheme works.

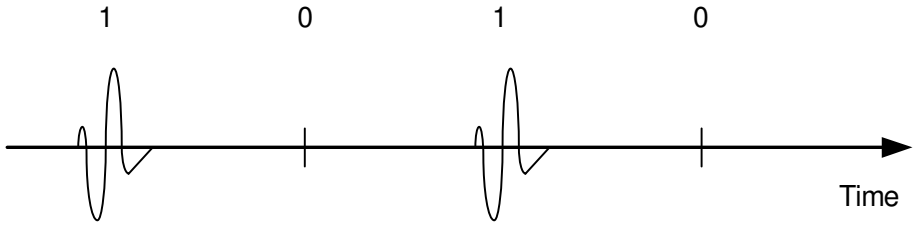


Figure 2.7 On-off keying modulation

This modulation technique is applied in this project design due to its low circuit complexity required for both modulation and demodulation. Multiple pulses are used to represent a single bit, this helps to combat noise and attenuation and makes the energy detection at the receiver side easier.

2.4.3 Pulse-Position Modulation

Pulse-position modulation (PPM) modulates signals by shifting the pulses in a predefined window in time. A data bit 1 can be represented by the original signal pulse and data bit 0 by position-shifted pulse with respect to a specific reference point in time domain. The signals after modulation are in a form as follows [15]:

$$s(t) = \sum_{m=1}^{\infty} P(t - mT - b_m \delta) \tag{2.6}$$

where δ is a time delay, and b_m is the data bit '1' or '0'. $P(t)$ is the energy signal and m is the numbers of bits that modulated. For a particular case of PPM transmission, as shown in Figure 2.8, data bit '1' is sent at the nominal time and data bit '0' is send delayed by a time interval δ. PPM signals are less sensitive to channel noise compared to PAM or OOK signals. However, they are vulnerable to catastrophic collisions that are caused by multiple-access channels [15]. The higher circuit complexity is another issue when considering PPM physical implementation.

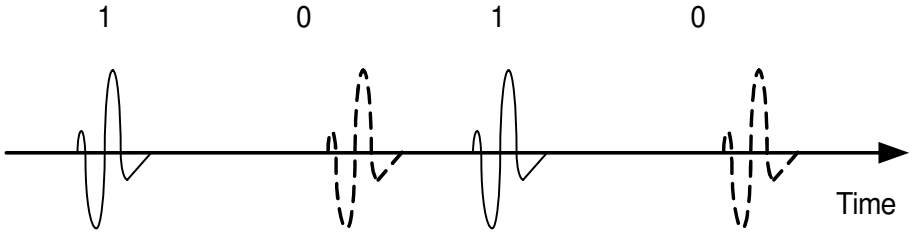


Figure 2.8 Pulse-position modulation

2.4.4 Biphase Modulation

The biphase modulation changes the polarity of the signal pulse to represent information bits 1 or 0. Usually, positive polarity carries the data bit 1 and negative polarity carries the data bit 0. The mathematical representation of the modulated signals is shown as follows [15]:

$$s(t) = \sum_{m=1}^{\infty} b_m \cdot P(t - mT) \qquad (2.7)$$

where b_m stands for the positive or negative polarities 1 or -1 with respect to the data bits 1 or 0. $P(t)$ is the short energy pulse. T is the full pulse cycle time. Figure 2.9 demonstrates signal modulation using biphase scheme.

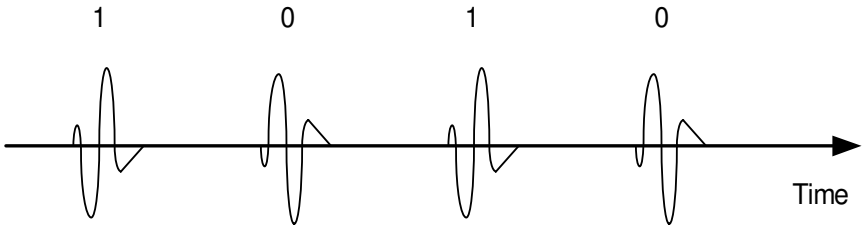


Figure 2.9 Biphase modulation scheme

The advantage of biphase modulation is the less susceptibility to distortion because the signals are detected based on the polarity not on the amplitude [3]. But on the other hand, both the transmitter and the receiver need complex circuit implementation.

2.5 UWB Communications and UWB Radar

Both UWB communications and radar sensing utilize IR-Ultra Wideband techniques and electromagnetic properties of pulses to convey information and sense targets. However, completing wireless communications and sensing tasks are not just all about the UWB but a successful integration of all the parts including design methodologies,

physical implementation, wireless channel estimation, and UWB technology. This section focuses on how the UWB technology can be applied for communicating and sensing.

2.5.1 UWB Communications

Wireless UWB communications is regarded as the future technology for high data rate and short range communications. Impulse radio is a UWB digital data communication system for low power, low range applications. The carrier-less transmission eliminates the use of frequency mixer, local oscillator at the transmitter and frequency down-converter at the receiver since the digital input bits are not modulated on a continuous waveform of a fixed carrier frequency. As a result, the transceiver, as shown in Figure 2.10, is much less complex than the conventional narrow-band transceiver architecture [3,16,17].

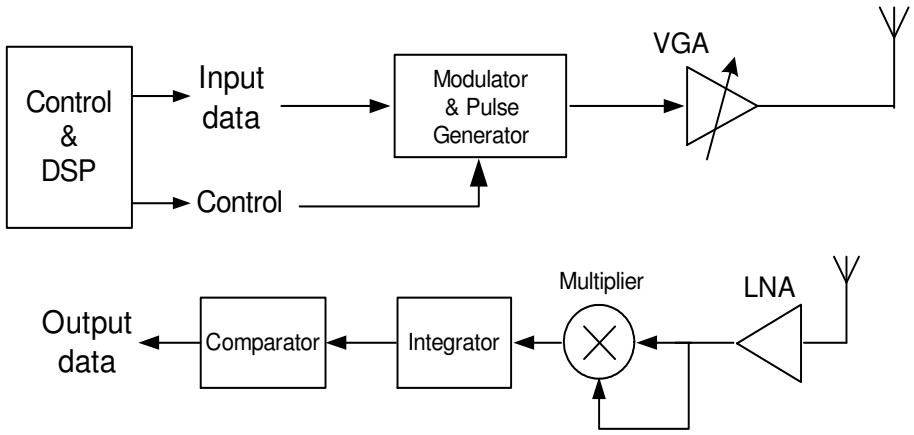


Figure 2.10 IR-UWB transceiver architecture

At the block level, the transmitter is very simple. It consists of a pulse generator and an OOK modulator, and a variable gain amplifier (VGA) to control the output pulse amplitude level. The pulse repetition rate is determined by a control signal from the DSP unit. The receiver for signals transmitted over an additive white Gaussian noise (AWGN) channel is a correlation-type receiver which calculate the correlation between received signals and template signals and maximize the signal to noise ratio (SNR) [18]. The receiver proposed in this thesis is a non-coherent receiver that includes a low-noise

amplifier (LNA), a multiplier functioning as a correlation circuit, an energy integrator, and a 1-bit voltage comparator. To maximize the processing gain and SNR, the template signals should be the same as that of the received signal. Usually very coarse approximations are generated as template due to the difficulty of making the replica of the transmitted signal. Here in the proposed design, the template for correlation is the received signal itself. This eliminates the use of signal template generator and complex coherent synchronization techniques. After a received signal is amplified and squared, the result is integrated over one bit duration to maximize the received signal power and to minimize the noise. Having multiple pulses representing one bit raises the correlated signal from the noise and the possible signals of other sources. This comes to a conclusion that the more pulses representing a bit, the better SNR is attained since more energy is put into the symbol.

2.5.2 UWB Radar for Biomedical Use

As mentioned before, the extremely narrow pulse (usually in order of few hundreds picoseconds) makes it possible to build radar with much better spatial resolution and very short-range capability compared to other conventional radars. Also, the large bandwidth allows the UWB radar to get more information about the possible surrounding targets and detect, identify, and locate only the most desired target among others. The fine resolution makes the ultra wideband radar beneficial for medical applications. The properties of short pulse indicate that the UWB signal can penetrate a great variety of biological materials such as organic tissues, fat, blood, and bone. Experiment results show that the signals with low center frequencies achieve better material penetration [17]. Compared to a radar system with a pulse-length of one microsecond, a short Gaussian or Gaussian monopole pulse of 200ps in width has a wavelength in free space of only 60 mm, compared to 300m. Since the pulse length in conventional radar is significantly longer than the size of the target of interest, the majority of the duration of the returned signal is an exact replica of the radiated signal as the reflection process is at quasi steady-state.

Thus, the returned signal provides little information about the nature of the target. However, since the UWB pulse length is in the same order of magnitude with the potential targets, UWB radar reflected pulses are changed by the target structure and electrical characteristics. Those changes in pulse waveform provide valuable information such as shape and material properties about the targets. Discrimination of target using higher order signal processing of impulse signals can distinguish between materials that would not be otherwise distinguishable by the narrowband signals, at the cost of complex signal processing [19].

To work as an impulse radar, the UWB transmitter sends a narrow pulse toward a target and a UWB receiver detects the reflected signal. This is the very simple algorithm of radar sensing which has been widely used. For biomedical sensor in this project, the target is a human heart. To further explore how the heart movement can be detected and measured, it is useful to take a close look at what is measured and analyzed in the sensing process.

When electromagnetic wave in propagation encounter an boundary of two types of medium with different dielectric properties, a portion of the incident electromagnetic energy is reflected back to the original medium with reflection angle θ_r (zero reflection angle if the incident wave path is parallel to the normal line), while the other portion continues propagating through the next medium. The transmission of UWB pulse has the same analogy, as shown in Figure 2.11.

The reflection coefficient is Γ and transmission coefficient is represented by γ. The reflected and transmitted signals are expressed in Equation 2.8 and 2.9

$$E_t = \gamma \cdot E_i \tag{2.8}$$

$$E_r = \Gamma \cdot E_i \tag{2.9}$$

where E_i is the incident wave, E_r and E_t are the reflected wave and transmitted wave respectively. The reflection coefficient can be represented by Equation 2.10

$$\Gamma = \frac{\frac{Z_1}{Z_2} - 1}{\frac{Z_1}{Z_2} + 1} \tag{2.10}$$

where $Z_1 = \sqrt{\frac{\varepsilon_0}{\varepsilon_1}}$ and $Z_2 = \sqrt{\frac{\varepsilon_0}{\varepsilon_2}}$ are the characteristic impedances of medium one and medium two, respectively. ε_1 and ε_2 are the relative permittivities of the two mediums. ε_0 is the permittivity of free space. Studies and researches show that there is a noticeable difference in dielectric properties between human heart muscle and the blood it pushes into the vascular tree [5,20]. Therefore, when a pulse reaches the interface between the heart muscle and the blood inside, partial reflection occurs. According to McEwan's patent, rough estimation of the characteristic impedance of the cardiac muscle is about 60 ohms and the impedance of cardiac blood is about 50 ohms [8]. Given all the impedance data, the reflection coefficient can be estimated using Equation 2.10 which yields a 10% return fraction of the radiated pulse.

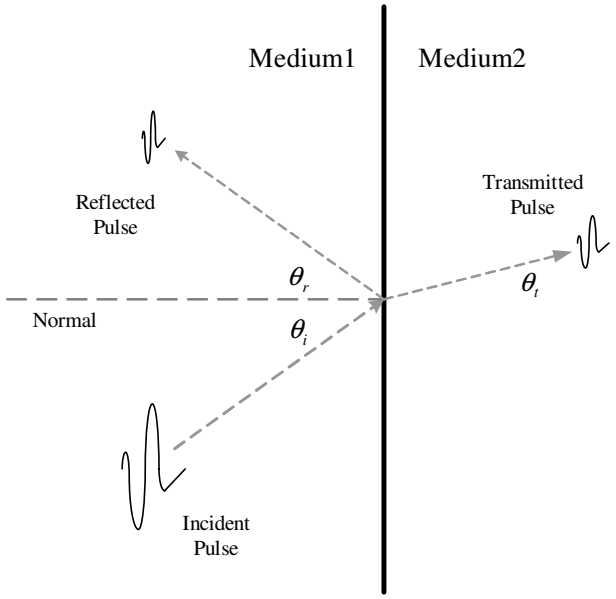


Figure 2.11 Pulse reflection and transmission diagram

The primary components of an IR-UWB sensor radar consist of a transmitter and a receiver. These two parts can be either implemented in a same chip or separately. The transmitter sends out a pulse to the thorax and sends a timing signal to processor. As the pulse propagates through skin (including epidermis, dermis, and subcutaneous layer), fat, pectorals muscle, cardiac muscle and heart blood, several reflections occur at each interface. At this moment it is believed that the energy reflection from the interface between cardiac muscle and heart blood is the highest among these reflections. This is

because the dielectric properties between cardiac muscle which belongs to soft tissue category and heart blood differ noticeably while the differences of dielectric properties between other similar soft tissues are minor since they are formed by similar types of carbohydrate macromolecules. For the above reason, the receiver only detects the reflected pulse and sends another timing signal to the processor. The time interval between two timing signals is the pulse round trip time. The distance is then computed using the equation, *distance*=*time*×*velocity* where the velocity can be expressed by Equation 2.11 as

$$velocity = \frac{2.99752458 \times 10^8 \, m/s}{\sqrt{\varepsilon_r}} \tag{2.11}$$

The velocity is material dependent and different propagation velocities are estimated based on tissues' relative permittivity ε_r. The movements of heart muscle are analyzed based on the computed distance. After repeating sending pulses and receiving pulses, a pattern for measured distances can be plotted and heart beating rate can be obtained. An example of the distance measurement plot is shown in Figure 2.12.

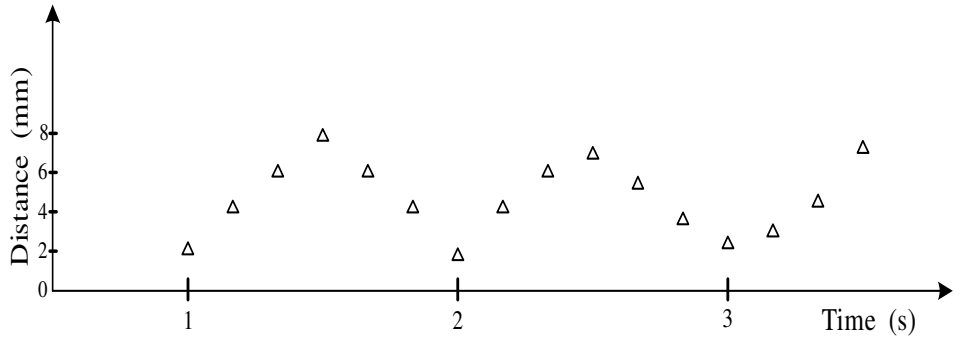


Figure 2.12 Distance plot for heart motion with a heart rate of 60 beats/second

Models of organic tissues in the thorax over typical UWB pulse of width 200 ns are shown in Table 2-1, these data are obtained from the Visible Human Project [21] and the Gabriel's data book of dielectric properties of tissues [22]. Figure 2.13 illustrates the cross-section diagram of different organ locations.

Table 2-1 Models of different organic tissues in human thorax [21,22]

	Impedance	Attenuation	Speed	Tissue Thickness
	Ohms	m^{-1}	10^7 m/s	mm
Free air	376.7	0	29.98	1
fat	112.6	8.96	8.958	0.96
muscle	49.99	31.67	3.978	1.35
lung	52.86	29.62	4.206	5.78
heart	49.17	38.71	3.912	N/A

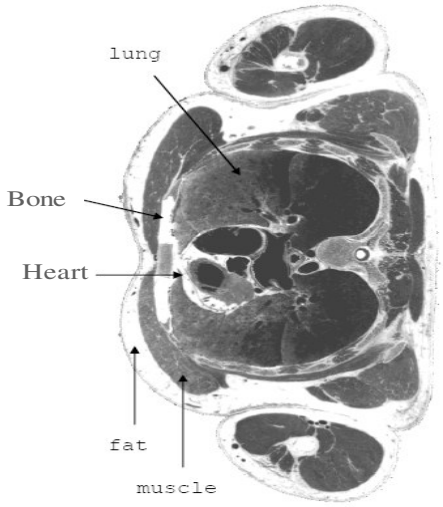


Figure 2.13 Cross-section of thorax [2]

These data help to develop and build an accurate propagation analysis. However, this project focuses rather on the overall physical sensor system realization and implementation than the detailed pulse transmission analysis. The construction of accurate model for pulse propagation will be carried out in the future work. The next chapter will talk about the circuit implementation of the UWB transceiver.

Chapter 3 UWB Transceiver Design

As machine computation is getting cheaper and cheaper, the analysis of system no longer presents much of a problem. Therefore, developing the design insight is more interested than getting the actual circuit parameters. The goal of this chapter is to provide a detailed design approach and design insight to the UWB transceiver with design methods that are reasonably simple to apply yet convey the desired insight and yield a good start for computer analysis. Also, a description of the proposed UWB antenna and a Control & DSP Unit are discussed for the full transceiver design completeness. Before further exploration of the UWB transceiver circuitry, a formal review of the basic concepts of radio frequency (RF) circuits and MOSFET design considerations are reviewed.

3.1 Design Considerations

In a CMOS RF system, the matching, noise, power gain, and speed are the most concerns that can affect the overall system performance. This section briefly overviews some general design techniques and considerations behind these concerns.

3.1.1 Impedance Matching

To achieve maximum power transfer in radio frequency circuit design, the matching is necessary between the load and the source impedance. Figure 3.1 illustrates a typical situation in which an amplifier, in order to deliver maximum power to the $50\,\Omega$ load, must have the $50\,\Omega$ equivalent terminations Z_S and Z_L. The input matching network is designed to transform the $50\,\Omega$ voltage source impedance (could be an antenna or a communication front-end) to the source impedance Z_S, and the output matching network transforms the $50\,\Omega$ termination to the load impedance Z_L.

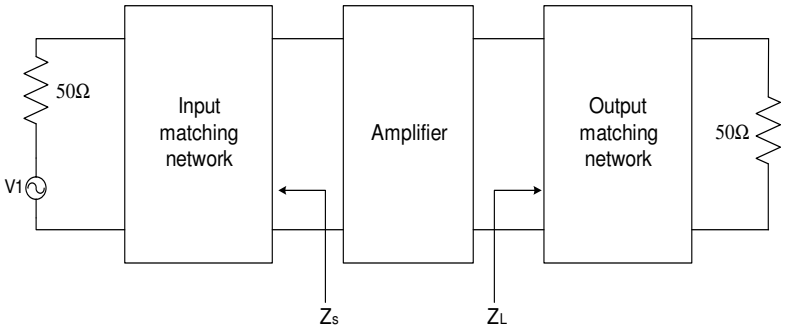


Figure 3.1 Block diagram of a microwave matching

The basic idea of the matching comes from the maximum power theorem which states that, for DC circuits, maximum power will be transferred from the source to the load if the load resistance equals the source resistance [23]. However in the case of time-varying wave forms, this theorem states that the maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance [23]. If the source impedance is described, by $Z_S = R + jX$, then the load impedance should be $Z_L = R - jX$. Therefore as shown in the Figure 3.2, for example, the inductive and capacitive reactance compensates for each other, and the equivalent circuit is shown on the right side of Figure 3.2.

Simple real impedance matching is very rare in the real world. For most devices such as transistor, transmission lines, LNAs, mixers, and antenna systems, the source and load

impedances are almost always complex because devices either contain reactive components or the parasitic effects.

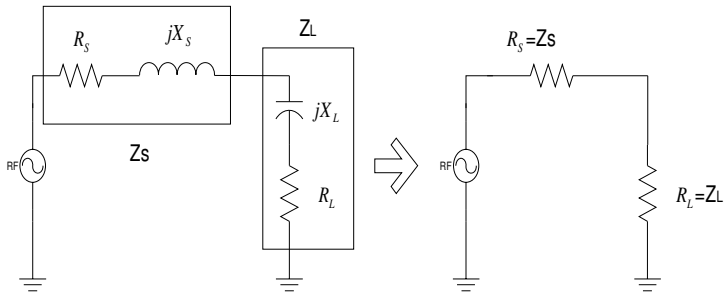


Figure 3.2 Impedance matching circuit and its equivalent circuit [24]

There are many different types of matching techniques, the L-match network, shown in Figure 3.3, is most commonly used not only because it is simple to design but quite practical. The quality factor analysis (Q analysis) is usually applied to construct the L matching network [24]. The basic definition of the quality factor of a circuit is

$$Q = 2\pi \frac{W_S}{W_P} \tag{3.1}$$

where W_S is the energy stored in reactive components and W_P is the average power dissipated in every frequency period. In Figure 3.3, from the definition of Q, the serial network Q_S and the parallel network Q_P can be described as

$$Q_S = \frac{X_S}{R_S}, \tag{3.2}$$

$$Q_P = \frac{R_P}{X_P}. \tag{3.3}$$

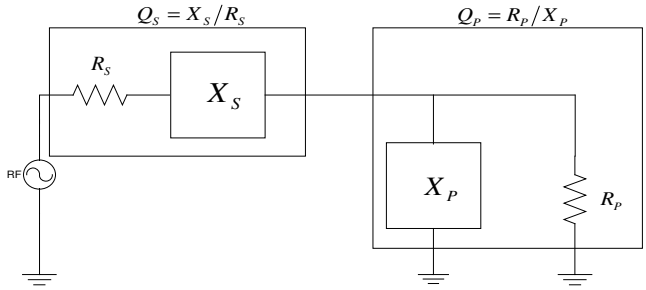


Figure 3.3 A simple L-matching network [24]

To match the source to the load, $R_S + jX_S$ and $R_P \parallel jX_P$ should be the same. Therefore,

$$R_S + jX_S = \frac{jX_P R_P}{R_P + jX_P} = \frac{jX_P R_P^2 + X_P^2 R_P}{R_P^2 + X_P^2}. \tag{3.4}$$

The real part is

$$R_S = \frac{X_P^2 R_P}{R_P^2 + X_P^2} = \frac{R_P}{Q_P^2 + 1}. \tag{3.5}$$

This leads to a Q_P described with resistive components only

$$Q_P = \sqrt{\frac{R_P}{R_S} - 1} \tag{3.6}$$

This Q analysis can be applied to other basic matching networks such as π match (a matching circuit with the π shape) and T match (a matching circuit with T shape) networks. Since they are not relevant to the project design, the review on impedance matching is not required to discuss further.

3.1.2 Shunt-Peaked Cascode Amplifier with Inductance Degeneration

The shunt-peaked cascade amplifier topology with inductance degeneration, shown in Figure 3.4, is a very good choice to start with the design of a driver amplifier at the transmitter and the front-end LNA at the receiver in this project because it has very low inverse interference, good noise figure, and high stability and gain [25]. The load impedance Z_L in the Figure 3.4 is replaced by a series connection of a shunt-peaking inductor L_L and a load resistance R_L to further enhance the frequency bandwidth as mentioned in the later sections.

The amplifier small signal gain can be analyzed by using the amplifier's small signal model shown in Figure 3.5. The transistor's body effect and gate-drain capacitance are ignored in analysis for simplicity and to provide more intuition for behavioral understanding.

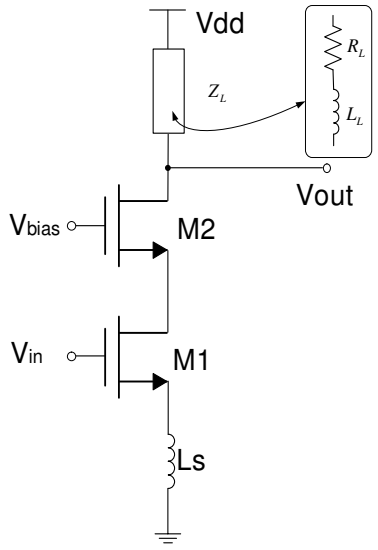


Figure 3.4 Cascode amplifier with inductance degeneration

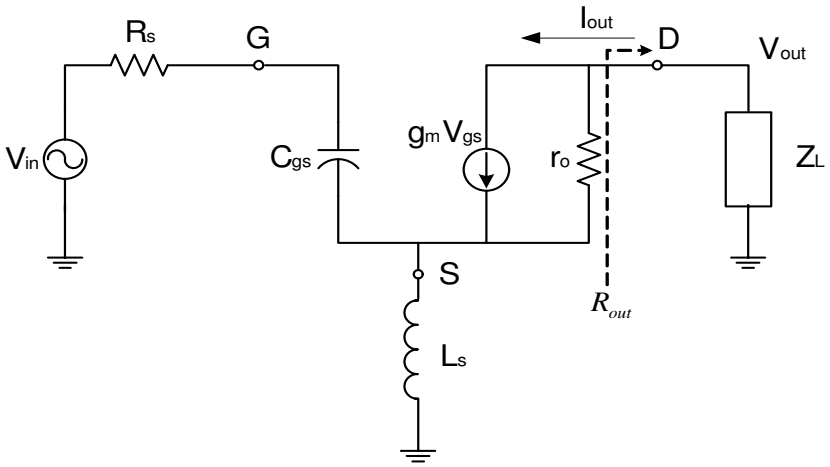


Figure 3.5 Small signal model of inductance degenerated amplifier

Consider the inductive degenerated output stage in Figure 3.5, the output impedance looking into the drain is R_{out}. To find an expression for R_{out}, the Thévenin's theorem is applied. The V_{in} is shorted to ground:

$$I_{out} = g_m V_{gs} + \frac{V_{out}}{r_o} \tag{3.7}$$

$$V_{out} = (I_{out} - g_m V_{gs}) r_o + V_S \tag{3.8}$$

At the source S:

$$I_{out} = \frac{V_S}{Z_S} \tag{3.9}$$

$$I_{out} = \frac{-V_{gs} + V_G}{Z_S} \tag{3.10}$$

$$V_{gs} = -I_{out} Z_S \tag{3.11}$$

Therefore, V_{out} can be expressed as:

$$V_{out} = (I_{out} - (-g_m I_{out} Z_S)) r_o + V_S \tag{3.12}$$

$$V_{out} = (1 + g_m Z_S) r_o I_{out} + V_S \tag{3.13}$$

$$V_{out} = (1 + g_m Z_S) r_o I_{out} - V_{gs} \tag{3.14}$$

$$V_{out} = (1 + g_m Z_S) r_o I_{out} + I_{out} Z_S \tag{3.15}$$

Therefore,

$$R_{out} = \frac{V_{out}}{I_{out}} = (1 + g_m Z_S) r_o + Z_S \tag{3.16}$$

$$R_{out} = r_o + g_m Z_S r_o + Z_S \tag{3.17}$$

Since

$$I_{out} = g_m V_{gs} \tag{3.18}$$

$$I_{out} = g_m (V_{in} - I_{out} Z_S) \tag{3.19}$$

$$I_{out} = \frac{g_m V_{in}}{1 + g_m Z_S} \tag{3.20}$$

Substitute:

$$V_{gs} = V_{in} - g_m V_{gs} Z_S \tag{3.21}$$

$$V_{in} = V_{gs} (1 + g_m Z_S) \tag{3.22}$$

$$V_{gs} = \frac{V_{in}}{1 + g_m Z_S} \tag{3.23}$$

Substitute:

$$V_{out} = -g_m V_{gs} (R_{out} \parallel Z_L) \tag{3.24}$$

$$V_{out} = -g_m \frac{V_{in}}{1 + g_m Z_S} (R_{out} \parallel Z_L) \tag{3.25}$$

$$V_{out} = -g_m \frac{V_{in}}{1 + g_m Z_S}(Z_S + r_o + Z_S r_o g_m) \parallel Z_L \tag{3.26}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-g_m}{1 + g_m Z_S} \cdot \frac{r_o Z_L + Z_S r_o g_m Z_L + Z_S Z_L}{r_o + Z_S + Z_L + Z_S r_o g_m} \tag{3.27}$$

For a very large r_o, the high frequency gain can be simplified to

$$A_v \approx \frac{-g_m Z_L}{1 + g_m Z_S} \tag{3.29}$$

The last equation shows that the gain of an amplifier is mainly determined by the load impedance Z_L and the source impedance Z_S.

3.1.3 MOSFET Design Considerations

Proper CMOS transistor sizing is critical for realizing high gain, high speed, and low noise circuits for Giga Hertz analog design. Among various transistor parameters, two figures of merit used to indicate transistor performance are particularly important, i.e., ω_T and $\omega_{\max}$, shown in equations 3.30 and 3.31, in which ω_T is the frequency at which the current gain equals to unity, and $\omega_{\max}$ is the frequency at which the power gain drops to unity [26]. These two figures define the maximum speed at which a transistor can operate.

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{3.30}$$

$$\omega_{\max} = \frac{1}{2}\sqrt{\frac{\omega_T}{r_g C_{gd}}} \tag{3.31}$$

where r_g is the series transistor gate resistance. It is clear that ω_T depends on gate-source capacitance and gate-drain capacitance (mostly on gate-source), and $\omega_{\max}$ not only on ω_T, but also on the gate resistance. Further derivation of ω_T with assumption that the gate-drain capacitance is very small compared to the gate-source capacitance shows that

$$\omega_T \approx \frac{g_m}{C_{gs}} \approx \frac{\mu_n C_{OX} \frac{W}{L}(V_{gs} - V_t)}{\frac{2}{3} WLC_{OX}}. \quad (3.32)$$

Therefore, ω_T depends on the inverse square of the transistor length *L*, and *W* if the gate-drain capacitance is taken into consideration. So small CMOS transistor length *L* is required to increase ω_T and $\omega_{\max}$ and therefore, the speed of the circuit. Large transistor width *W* leads to a large g_m, which in turn increases transistor gain and reduces noise, as the minimum noise figure of a CMOS transistor is inversely proportional to the g_m as shown in Equation 3.33 [26], where K_2 is the constant dependent on temperature and r_S is the source resistance.

$$F_{\min} = 1 + K_2 C_{gs} \sqrt{\frac{r_g + r_S}{g_m}} \quad (3.33)$$

The gate and source resistance r_g and r_S should be kept small in order to maintain a low noise figure and high $\omega_{\max}$. However, large transistor width *W* is sometimes unavoidable in the design, thus some layout techniques are applied to reduce the gate and source resistance. These layout techniques will be discussed in Chapter 4.

3.2 The Transmitter

Figure 3.6 shows the architecture of the UWB transmitter. The very simple transmitter structure includes a modulator, a pulse generator and a driver amplifier. The input clock signal and control signal are modulated to a sequence of clock pulse, and this square pulse train then goes into the pulse generator to produce a short Gaussian voltage pulse. The output of the pulse generator is passed onto a driver amplifier and then transmitted by an UWB antenna. The output pulse amplitude is adjustable through the variable gain amplifier (VGA) driver. This driver also shapes the pulse to meet the FCC spectral mask [27].

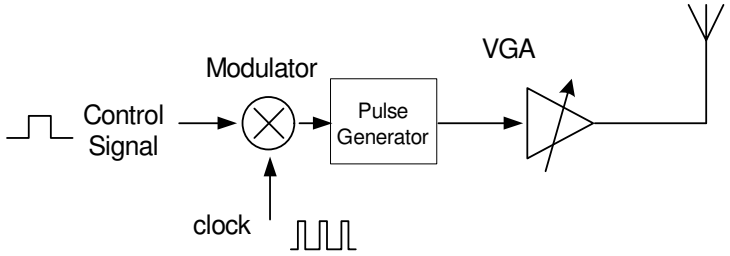


Figure 3.6 The block diagram of the transmitter

In the following sections, each component of the transmitter is presented and design issues are discussed from an intuitive design perspective.

3.2.1 The Modulator and Pulse Generator

Figure 3.7 shows two main components of the transmitter: the modulator and the pulse generator. The data modulator and the pulse generator are designed using low power digital circuits. The modulation scheme is OOK modulation. The inputs to the OOK modulator are a digital periodical clock signal Clk, and a binary control signal data. The control signal, as shown in Figure 3.8(a), decides how many pulses to be sent while the clock decides the pulse frequency. Whenever the input data goes high, the modulated output V_{mod} is represented by a sequence of clock signal as shown in Figure 3.8(b). V_{mod} is logic low when the data goes low. In Figure 3.8(c), V_{pulse} is the waveform at the output of the pulse generator. The clock rate must be higher than the data rate to ensure reliable modulation and demodulation.

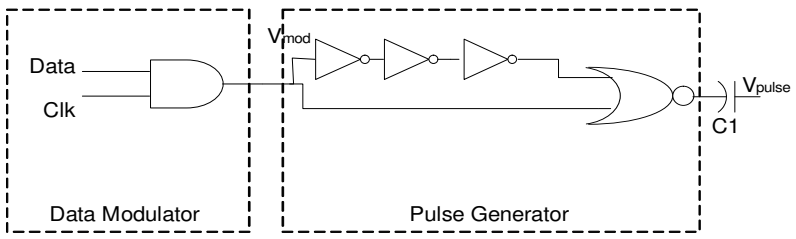


Figure 3.7 Circuit diagram of data modulator and pulse generator

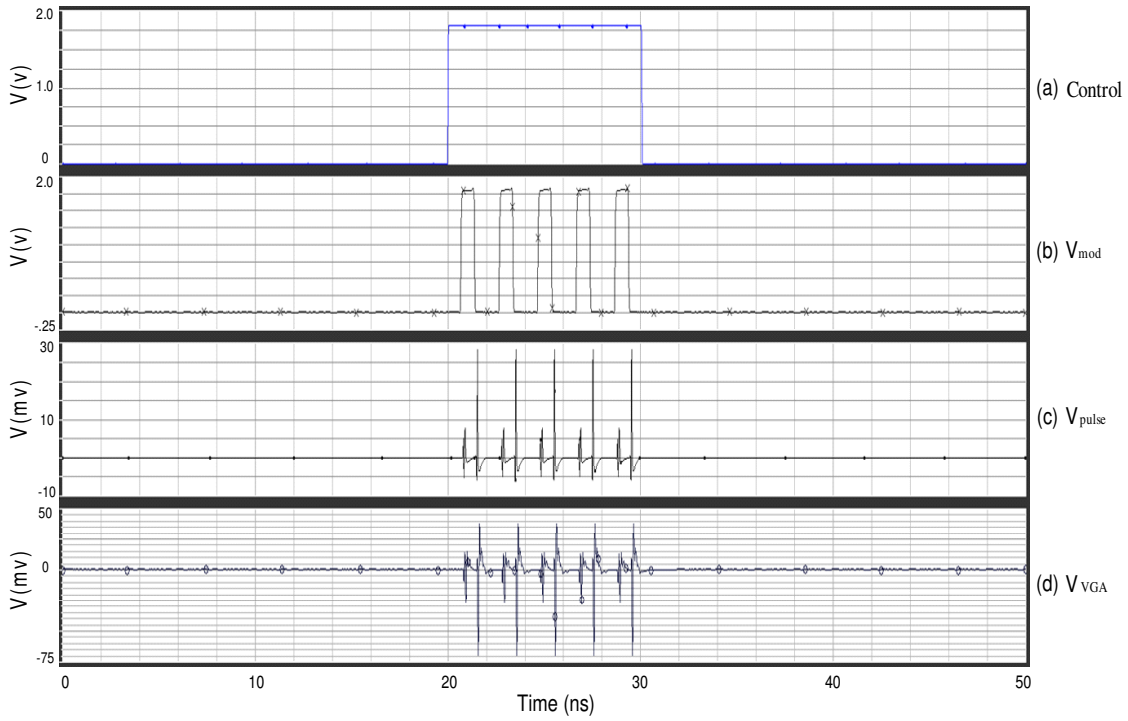


Figure 3.8 Signal-flow in the modulator and pulse generator

The input signal to the pulse generator is the modulated clock signal. Each falling edge of the clock triggers a positively-peaked Gaussian pulse through a NOR gate since one input of the NOR gate is delayed and inverted by a series of inverters and two NOR inputs are both low only when the clock is at the falling edge. The momentary logic low for both inputs produces a momentary logic high pulse. The width of the pulse is determined by the time of the inputs are momentary low, which is set by the total delay time of the inverters. Figure 3.8(a) shows the modulated clock in which the control signal is long enough to allow five pulses to be sent and the Gaussian pulses produced by the pulse generator. The modulator can be set so that three pulses are sent instead of five pulses. The circuit is in idle state without dynamic power dissipation unless the control signal is turned on. In Figure 3.8(d), V_{VGA} shows the waveform at the output of the transmitter. The next section will discuss how the amplifier waveform can be adjusted.

3.2.2 The Driver Amplifier with Variable Gain

The driver amplifier is used to adjust the transmitting pulse amplitude, and to drive a $50\,\Omega$ antenna. There are two stages in the driver amplifier: the first stage is a cascaded common-source common-gate shunt-peaked structure with an inductive degeneration, and the second stage is a source-follower with an active load. By analyzing the high frequency operation of a cascaded common-source amplifier, a voltage gain can be shown as:

$$A_V = -G_m Z_L \tag{3.34}$$

$$\text{or} \qquad A_V = \frac{-g_m Z_L}{1 + g_m Z_S} \tag{3.35}$$

For a MOS transistor biased in the linear region, the current can be described by the relationship of the following equation:

$$i_D = \mu_n C_{OX} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{3.36}$$

If the value v_{DS} is very small, the last term $\frac{1}{2}v_{DS}^2$ can be neglected, and the above equation is turned into a linear function between v_{DS} and i_D. Rearrange this representation, a linear resistance r_{DS} is shown:

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(v_{GS} - V_t)} \tag{3.37}$$

The value of the resistance r_{DS} is controlled by varying the value of v_{GS}.

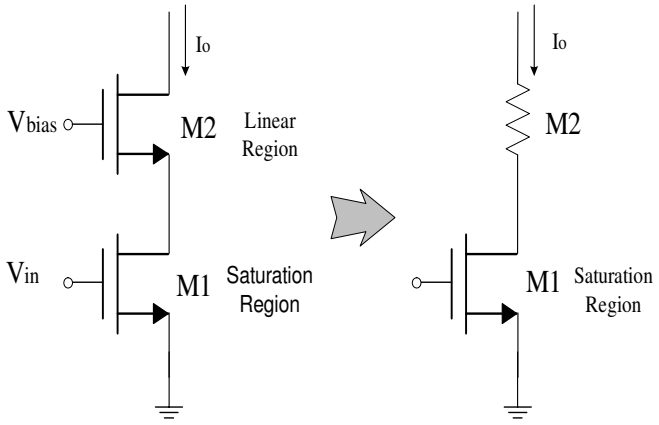


Figure 3.9 Equivalent circuits of a simple VGA

As shown in Figure 3.9, M1 is biased to operate in the saturation region while M2 operates in the linear region. V_{in}, the gate voltage of M1, is the signal input. V_{bias}, the gate voltage of M2, controls the resistance r_{DS}. The gain of the amplifier with M2 in the linear region is

$$A_V = -r_{DS}\mu_n C_{OX}\frac{W}{L}(V_{in} - V_t)$$

$$= -g_m r_{DS} \tag{3.38}$$

$$= -g_m \frac{1}{\mu_n C_{OX}\frac{W}{L}(v_{GS} - V_t)} \tag{3.39}$$

r_{DS} is in series with the shunt-peaked components Z_L. Therefore, the total gain of this simple VGA can be expressed as:

$$A_V = \frac{-g_m Z_L - g_m r_{DS}}{1 + g_m Z_S}$$

$$= \frac{-g_m Z_L - g_m\left(\mu_n C_{OX}\frac{W}{L}(v_{GS} - V_t)\right)^{-1}}{1 + g_m Z_S} \tag{3.41}$$

Simulation shows that a change from 0.6V to 1.4V corresponds to a signal pulse level from 6mV to 75mV. There is a linear relationship between the control voltage and the amplifier gain. The second stage is an output buffer which is used to match the $50\,\Omega$

output resistance from 0.9GHz to 6GHz. The driver amplifier VGA circuit is shown in Figure 3.10.

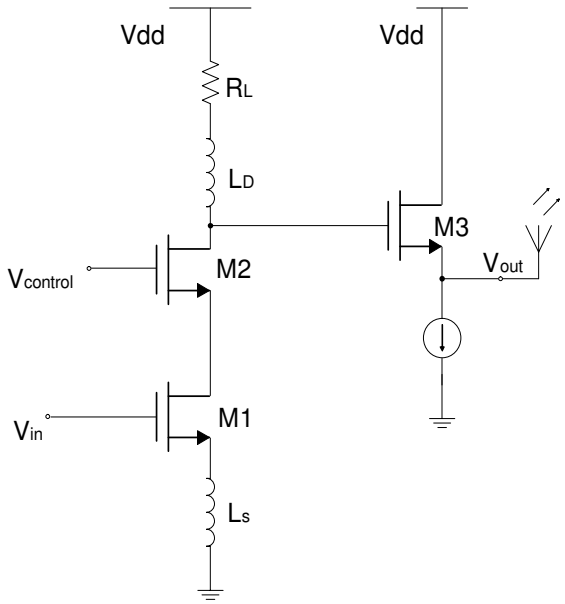


Figure 3.10 Driver amplifier with variable gain

3.3 The Receiver

The UWB receiver's structure is shown in Figure 3.11. In this receiver topology, The UWB pulses are detected by the receiver antenna and amplified by an ultra wideband LNA. The amplified pulse is then self-multiplied by a multiplier which behaves as a correlation-type demodulator since it maximizes the SNR [18,29]. The squared output is then fed into an integrator to further improve SNR of the signals by collecting energy over one pulses repetition period. The signal output of the integrator is compared with a reference voltage to decide whether there is a pulse received. In the following sections, each component of the receiver is presented and design issues are discussed.

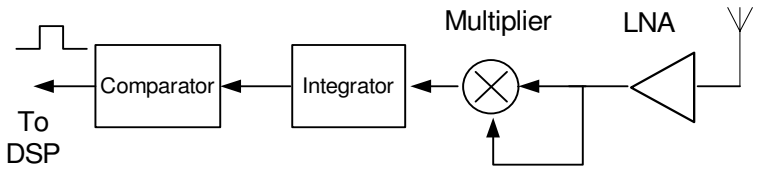


Figure 3.11 The UWB receiver structure

3.3.1 The Low Noise Amplifier

The wireless receiver requires input impedance matching to 50 Ω source impedance (RF front end, antennas). This 50 Ω input matching maximizes the power received in the receiver. In UWB circuit design, conventional narrow band matching techniques can not be employed for matching over a wideband of frequency. It is quite challenging to match over the 7.5 GHz bandwidth in the case of UWB.

Classic shunt feedback amplifiers for wideband input match is a possible approach, but the higher 3dB frequency is limited by the parasitic input capacitance. The proposed circuit is based on a common-source amplifier with inductance degeneration, shown in Figure 3.4 in previous section, a technique widely used in narrow-band designs by embedding the input network of the LNA in a multi-section reactive network so that the overall input reactance is resonated over a wider bandwidth [26,29]. At high frequency, the power matching and noise matching is very similar. Here, the LC-ladder matching, a technique for ultra-wideband input matching is applied in the LNA. This technique uses a second-order low-pass ladder filter as shown in Figure 3.12.

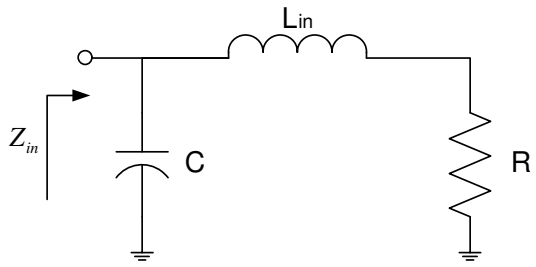


Figure 3.12 LC-ladder matching network

The values of L_{in} and C are chosen that

$$L_{in} = \frac{R}{\omega_0} \tag{3.42}$$

$$C = \frac{1}{\omega_0 R} \tag{3.43}$$

The overall input impedance is equal to R to up to ω_0, the low-pass cut-off frequency. Using the low-pass to band-pass transformation, the series inductor is transformed to a series LC and the shunt capacitor to a parallel LC [30,31]. The transformation is conducted by replacing s/ω_0 by $(s/\omega_0)+(\omega_0/s)$ and adding a zero in the second-order filter transfer function

$$T = \frac{\omega_0^2}{s^2 + s\left(\frac{\omega_0}{Q}\right) + \omega_0^2}, \tag{3.44}$$

where $\omega_0 = 1/\sqrt{LC}$ and $Q = \omega_0 CR$.

In Figure 3.13, the transformed band-pass ladder matching network is shown. The right side of Z_{in} resembles the input impedance of an inductively generated common-source transistor.

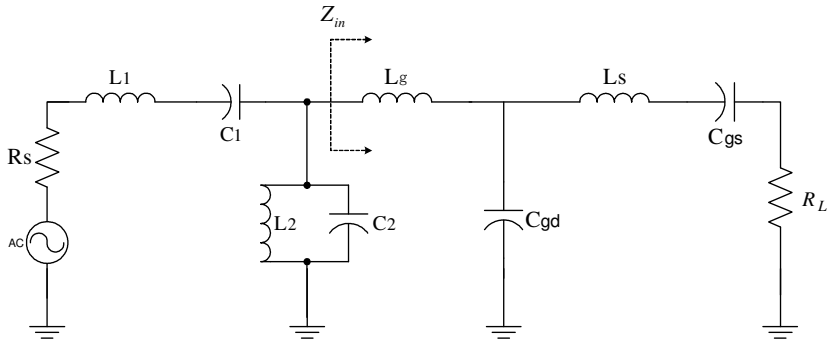


Figure 3.13 The LNA input matching network

The input impedance can be expressed as

$$Z_{in} = sL_g + (\frac{1}{sC_{gs}} + R_L + sL_S) \| \frac{1}{sC_{gd}} \tag{3.45}$$

$$= sL_g + \frac{1 + sR_L C_{gs} + s^2 C_{gs} L_S}{s[C_{gs} + C_{gd} + sR_L C_{gs} C_{gd} + s^2 C_{gs} L_S C_{gd}]} \quad (3.46)$$

$$\approx \frac{1 + sR_L C_{gs} + sR_L C_{gd} + s^2 (L_S + L_g) C_{gs} + s^2 (L_S + L_g) C_{gd}}{s(C_{gs} + C_{gd})} \quad (3.47)$$

R_L, the real part of input impedance Z_{in}, is chosen to be equal to the source resistance R_S, which is $50\ \Omega$. From the principle of inductance degeneration analysis, the input impedance model of the inductive source degeneration can be simplified as

$$Z_{in} = sL_{ind} + \frac{1}{sC_{gs}} + \omega_T L_{ind} \quad (3.48)$$

where $\omega_T = g_m / (C_{gs} + C_{gd})$. Therefore, R_L in Figure 3.13 is replaced by $R_L = \omega_T L_S$. It is clear that the value of the real part of input impedance can be controlled over through the choice of the inductance. The approximated equations for choosing the matching inductors and capacitors are shown in Equation 3.49 to 3.52.

$$L_2 \approx \frac{R_S}{\omega_L} \quad \text{and} \quad C_{gs} \approx \frac{1}{\omega_L R_S} \quad (3.49 \text{ and } 3.50)$$

$$L_g + L_S \approx \frac{R_S}{\omega_H} \quad \text{and} \quad C_2 \approx \frac{1}{\omega_H R_S} \quad (3.51 \text{ and } 3.52)$$

The complete LNA circuit is shown in Figure 3.14. The LNA gain analysis is very similar to the gain analysis of the driver amplifier in the transmitter since both circuits utilize the same circuit topology: the shunt-peaked cascade structure with inductance degeneration. A similar derivation can lead to a rough approximation for gain transfer function shown in Equation 3.53.

$$A_V = \frac{V_{out}}{V_{in}} \approx \frac{-g_{m1}}{sC_1 R_S} \cdot \frac{R_1 (1 + \frac{sL_3}{R_1})}{s^2 L_3 C_{db2} + sR_1 C_{db2} + 1} \quad (3.53)$$

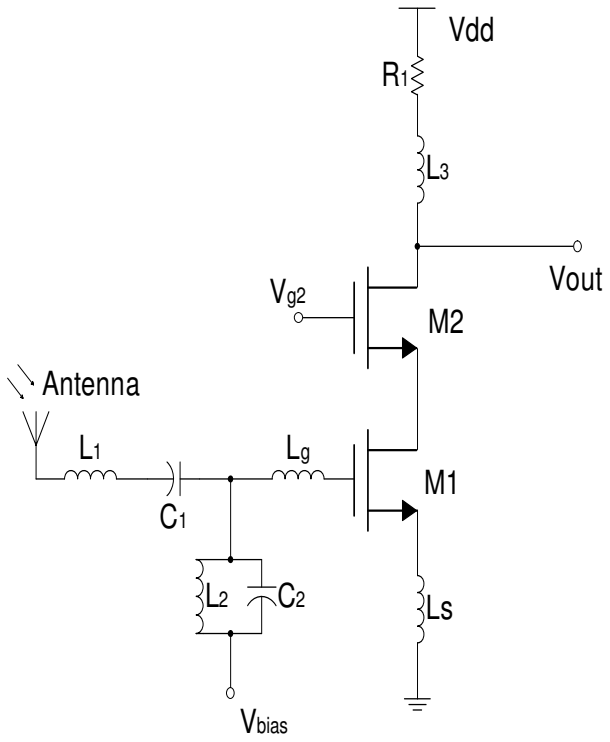


Figure 3.14 The LNA

The size of the transistors and operating currents are chosen by the constraint of maximizing gain while maintaining low-power consumption. Through simulations, the LNA provides a power gain of 7 dB, as plotted in Figure 3.15, a relatively good impedance match and the bandwidth is from 2GHz to 11.2GHz, as plotted in Figure 3.16. The maximum impedance matching is achieved at 5GHz. The dip at 5GHz in Figure 3.16 shows the minimum signal reflection occurs at this frequency. Figure 3.19 (a) shows the LNA output pulse train waveform.

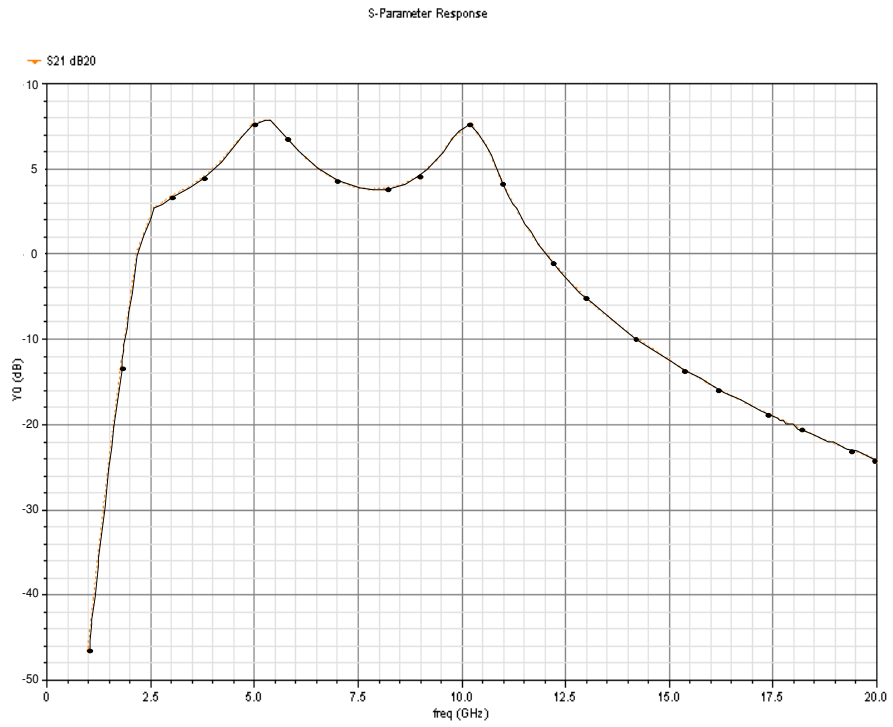


Figure 3.15 Simulated power gain for the LNA

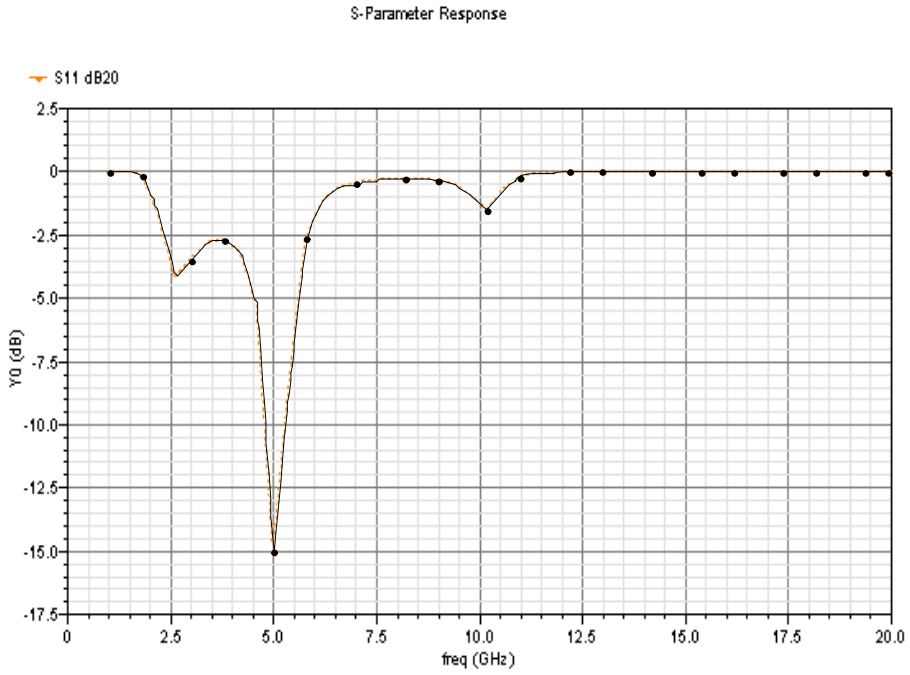


Figure 3.16 Simulated input matching for the LNA

3.3.2 The Multiplier

A Gilbert cell, the most common differential amplifier structure used in integrated telecommunication circuits today, is applied to implement the multiplication function in the UWB receiver, as shown in Figure 3.17.

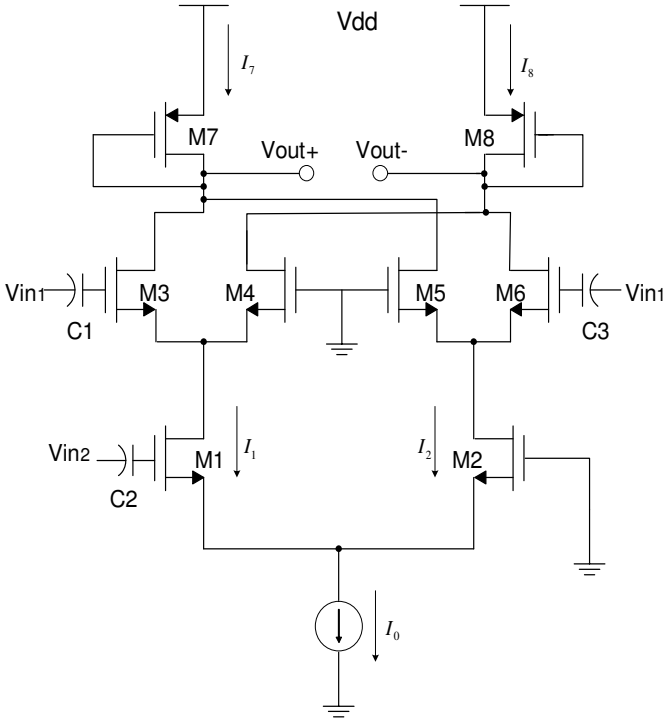


Figure 3.17 The multiplier

The Gilbert multiplier consists of two differential pairs with variable gain control in each tails. The differential output voltage and output current can be expressed as

$$V_{out} = V_{out}^{+} - V_{out}^{-} \tag{3.54}$$

$$I_{out} = I_7 - I_8 \tag{3.55}$$

With the diode connected active load on both V_{out}^{+} and V_{out}^{-},

$$V_{out} = \frac{1}{g_{m7}} I_7 - \frac{1}{g_{m8}} I_8 \tag{3.56}$$

Since

$$I_7 - I_8 = (I_3 + I_5) - (I_4 + I_6) \tag{3.57}$$

$$= (I_3 - I_4) - (I_6 - I_5) \tag{3.58}$$

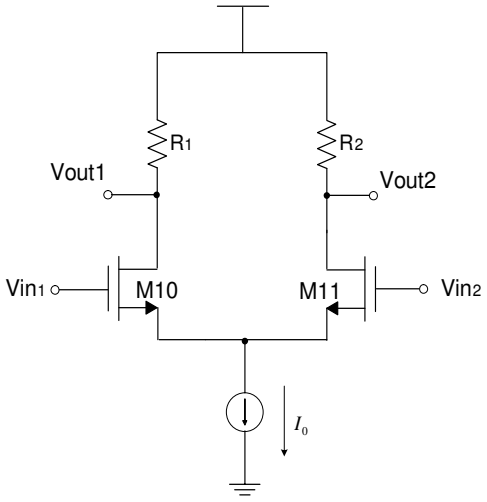


Figure 3.18 A differential pair

In a single differential pair shown in Figure 3.18, it can be proved by MOS square law in the saturation that

$$(I_{10} - I_{11})^2 = -\frac{1}{4}\left(\mu_n C_{OX}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_0 \mu_n C_{OX}\frac{W}{L}(V_{in1} - V_{in2})^2 \qquad (3.59)$$

Rearrange the above equation

$$I_{10} - I_{11} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_0}{\mu_n C_{OX}\frac{W}{L}} - (V_{in1} - V_{in2})^2} \qquad (3.60)$$

Similarly, $I_3 - I_4$ and $I_6 - I_5$ can be expressed as

$$I_3 - I_4 = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}V_{in1}\sqrt{\frac{4I_1}{\mu_n C_{OX}\frac{W}{L}} - V_{in1}^2} \qquad (3.61)$$

$$I_6 - I_5 = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}V_{in1}\sqrt{\frac{4I_2}{\mu_n C_{OX}\frac{W}{L}} - V_{in1}^2} \qquad (3.62)$$

Let $\alpha = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}$ as the transistor sizes from M3 to M6 are the same.

$$I_7 - I_8 = \alpha V_{in1}\sqrt{\frac{2I_1}{\alpha} - V_{in1}^2} - \alpha V_{in1}\sqrt{\frac{2I_2}{\alpha} - V_{in1}^2} \qquad (3.63)$$

Substitute into equation 3.57:

$$V_{out} = \frac{1}{g_{m7}} \alpha V_{in} \cdot (\sqrt{\frac{2I_1}{\alpha} - V_{in}^2} - \sqrt{\frac{2I_2}{\alpha} - V_{in}^2}) \tag{3.64}$$

Since M1 and M2 in Figure 3.17 form a lower differential pair

$$I_1 = \frac{1}{2}\alpha\left(\sqrt{\frac{I_0}{\alpha} - \frac{V_{in2}^2}{2}} + \frac{V_{in2}}{\sqrt{2}}\right)^2 \tag{3.65}$$

$$I_2 = \frac{1}{2}\alpha\left(\sqrt{\frac{I_0}{\alpha} - \frac{V_{in2}^2}{2}} - \frac{V_{in2}}{\sqrt{2}}\right)^2 \tag{3.66}$$

The output voltage V_{out} can be further simplified to

$$V_{out} = \frac{1}{g_{m7}} \alpha V_{in1} \cdot \left(\sqrt{\left(\sqrt{\frac{I_0}{\alpha} - \frac{V_{in2}^2}{2}} + \frac{V_{in2}}{\sqrt{2}}\right)^2} - \sqrt{\left(\sqrt{\frac{I_2}{\alpha} - \frac{V_{in2}^2}{2}} - \frac{V_{in2}}{\sqrt{2}}\right)^2}\right) \tag{3.67}$$

$$V_{out} = \frac{\sqrt{2}}{g_{m7}} \alpha V_{in1} \cdot V_{in2} \tag{3.68}$$

In the non-coherent UWB receiver design, the signal template for correlation detection is the received signal itself. Therefore, $V_{in1} = V_{in2} = V_{in}$, and the output of the multiplier is the square of the signal represented by Equation 3.69.

$$V_{out} = \frac{\sqrt{2}}{g_{m7}} \alpha V_{in}^2 \tag{3.69}$$

The output pulse waveform is shown in Figure 3.19 (b) below. The correlated pulses are squared and random noise is depressed. Figure 3.19(c) shows the waveform at the output of the integrator. This will be discussed in the following section.

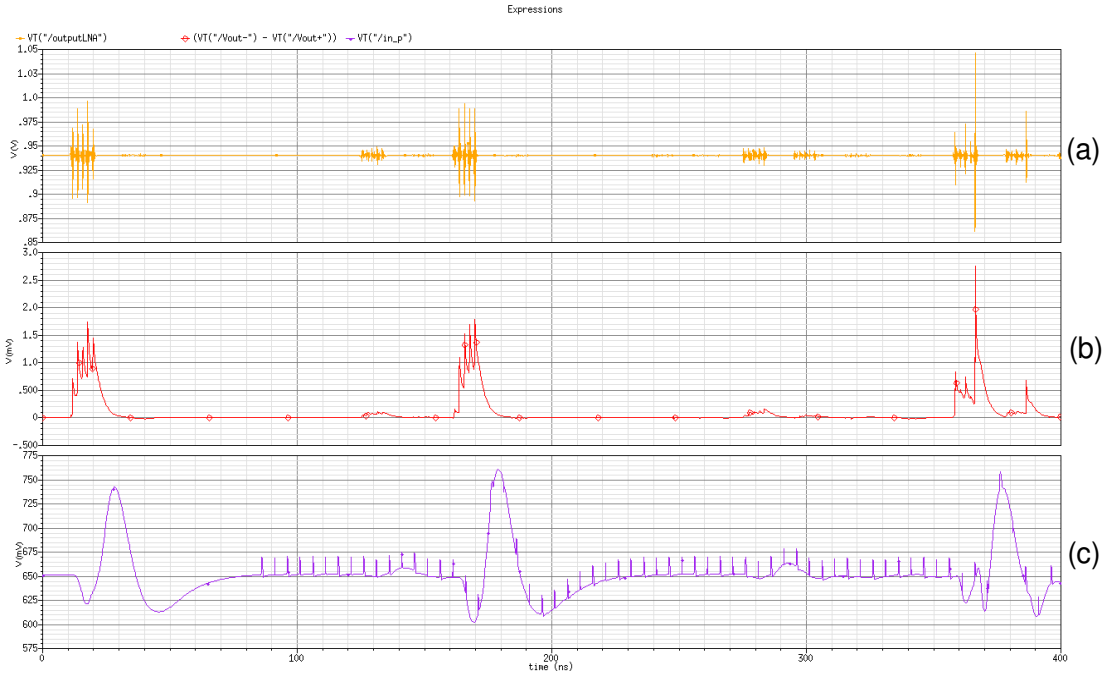


Figure 3.19 (a) LNA output pulse train, (b) multiplier output, (c) integrator output

3.3.3 The Integrator

An inverting operation amplifier configuration is employed in the implementation of the charge integrator. As shown in Figure 3.20, this configuration has a capacitor in the feedback path and a resistor at the input.

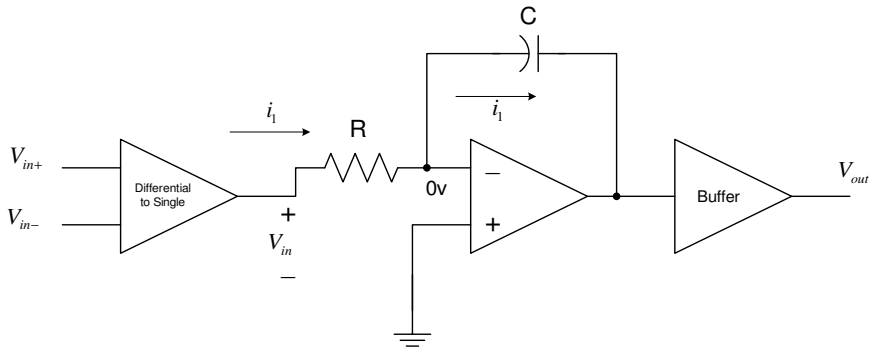


Figure 3.20 The integrator configuration

The first stage of the integrator is a differential-to-single amplifier to convert the differential signal to single-ended signal to achieve a signal gain, as shown in Figure 3.21. The signal voltage gain can be derived similarly to the differential pair as shown in the previous section. The gain can be approximated as

$$A_V = G_m R_{out} = g_{m1,2} \cdot (r_{o2} \parallel r_{o4}) \tag{3.70}$$

The second stage is an inverting operational amplifier with feedback [32]. The inverting op-amp input causes V_{in} to appear in effect across R, and therefore, the current i_1 flowing from the last stage will be V_{in}/R. This current flows through the capacitor C, which causes charge to accumulate on C. If the circuit begins to collect charges at time t=0, then, at time t, the current i_1 will have deposited on the capacitor C a charge equal to $\int_0^t i_1(t)dt$. The voltage across the capacitor C will change by $\frac{1}{C}\int_0^t i_1(t)dt$. The op-amp output voltage is the negative of the capacitor voltage, therefore,

$$V_{out}(t) = -\frac{1}{RC}\int_0^t V_{in}(t)dt - V_{Cinitial} \tag{3.71}$$

where $V_{Cinitial}$ is the initial voltage across the capacitor C before time 0. Then output voltage is proportional to the time-integral of the input, and CR is the integrator time-constant. The input signal is the pulse trains with a period T, and T is set to allow the integrator have enough time to collect the incoming pulse train charges and discharge the integrator before a new pulse train coming. The integrator frequency, ω_{int}, is the inverse of the integrator time constant

$$\omega_{\text{int}} = \frac{1}{RC} \tag{3.72}$$

For a very short pulse train duration time, the integrator constant RC must be very small as well in order to achieve an acceptable gain. The desirable op-amp must have a very large gain to overcome the ultra-wideband mismatching and high frequency attenuation.

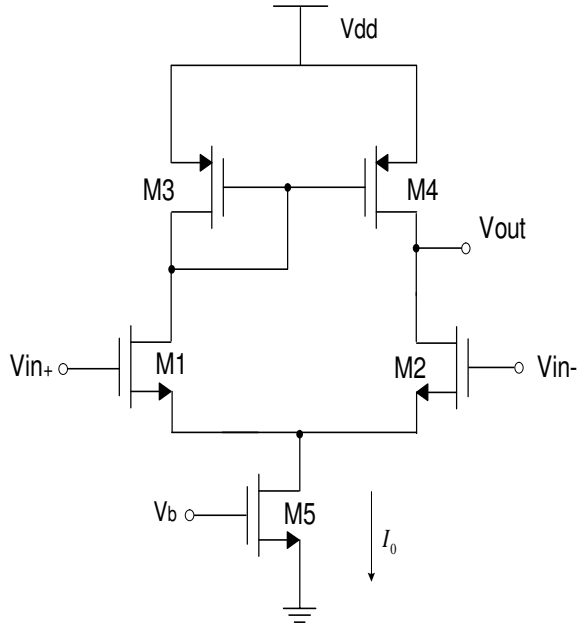


Figure 3.21 The differential-to-single converter circuitry

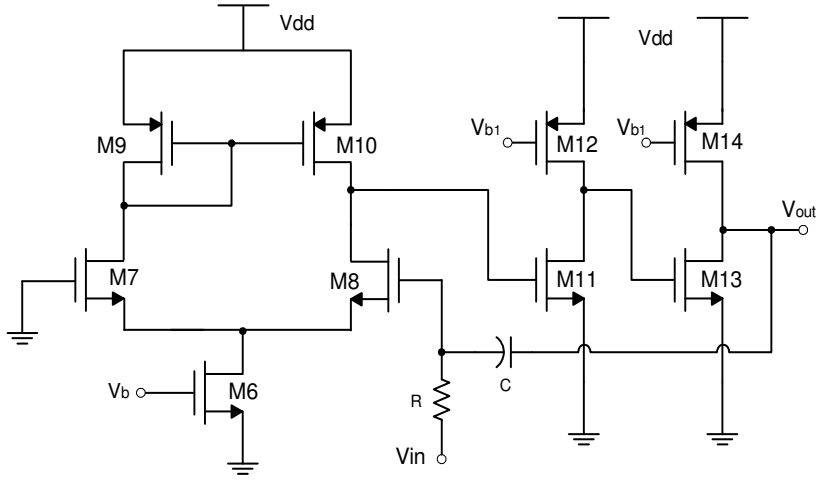


Figure 3.22 Inverting operational amplifier

Figure 3.22 shows the detail circuit for the inverting operation amplifier in the second stage. A rough estimation of the voltage gain is

$$A_{V1} = G_m R_{out1} = g_{m8} \cdot (r_{o8} \parallel r_{o10}) \tag{3.73}$$

$$A_{V2} = g_{m11} \cdot (r_{o11} \parallel r_{o12}) \tag{3.74}$$

$$A_{V3} = g_{m13} \cdot (r_{o13} \parallel r_{o14}) \tag{3.75}$$

$$A_{VTotal} = A_{V1} \times A_{V2} \times A_{V3} = g_{m8} g_{m11} g_{m13} \cdot (r_{o8} \parallel r_{o10})(r_{o11} \parallel r_{o12})(r_{o13} \parallel r_{o14}) \qquad (3.76)$$

The last stage is a series of common source amplifiers to further amplify the signal before it reaches the voltage comparator. Simulation shows this charge integrator is fast enough for the input signals. The final integrator output is shown in Figure 3.19 (c). The small voltage spikes in the integrator output are the clock feedthrough from the comparator at the next stage. The integrator output signals are high enough to overcome the clock feedthrough.

3.3.4 The Comparator

A voltage comparator is the last stage in the UWB receiver. A sense amplifier is used as comparator because of its high sensitivity and low circuit complexity [33,34]. Figure 3.24 shows a schematic diagram of the comparator. For a better understanding of how the circuit works, a simplified form is presented on the right side of the Figure 3.24. In the circuit, M3 – M6 form a flow-through latch (a cross coupled inverter shown in Figure 3.23).

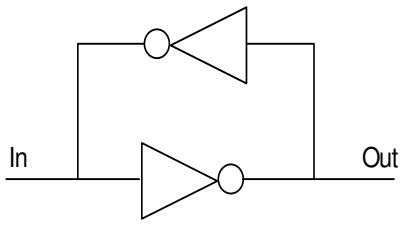


Figure 3.23 A latch formed by M3-M6

As shown in Figure 3.24, when the clock is set to a logic high, M5 and M6 are closed switch and M7 and M10 are open switch. When input voltage is rising higher than the reference voltage, the voltage at the drain of M1 is going down and therefore the voltage at the drain of M3 is going down. This leads to a smaller gate voltage of M4. Since the reference voltage is virtually going down relative to the input voltage (keep in mind that it is a differential amplifier topology), the voltage at the drain of M2 is going up, and so does the drain voltage at M4 (remember that the gate voltage of M4 is smaller now). This

process is keeping running until the drain of M4 reach the logic high level (Vdd). All this happens in a very short time and then the drain of M4 is stabilized at Vdd. This finishes one comparison. The signal diagram in Figure 3.25 illustrates the comparison process. It should be noted that the input signal must be greater than Vth (threshold voltage) for M1 and M2 to work properly (they are turned on to provide a path to ground). Kickback noise is minimized since the input signals are isolated from the latch by M1 and M2. Another important undesired noise is clock feedthrough which is large glitch seen in the input waveform when the clock goes high or low. It is because the clock has a direct capacitive path to the input signals. To reduce this feedthrough, one can use a cascade input configuration. In our design, the clock feedthrough noise is around 15 mV (much higher than the sensitivity of the comparator which is 7mV). A NAND SR latch at the end is used to provide the outputs of the circuit change on the rising edge of the clock signal.

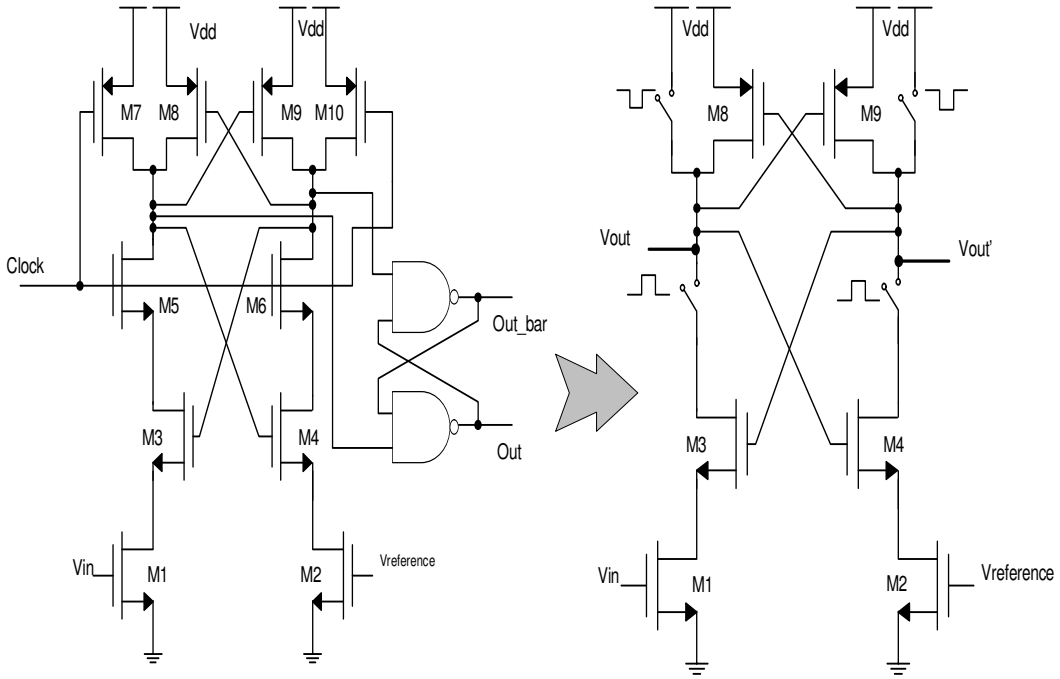


Figure 3.24 The comparator

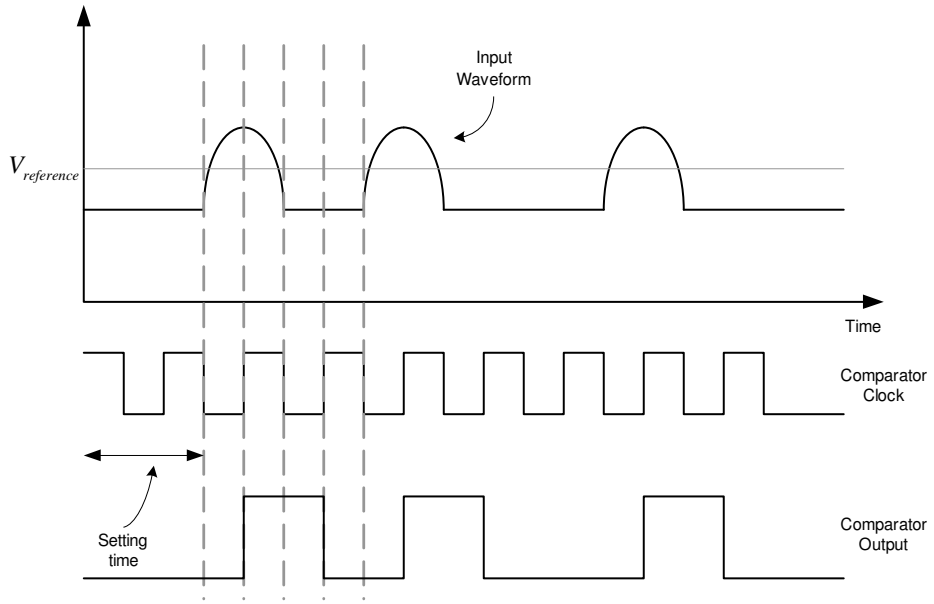


Figure 3.25 The operation of the comparator

3.4 The Bandgap Reference and Current Biasing

To make the circuits work properly, fixed voltages and currents must be generated to provide accurate biasing that is most independent of temperature, small voltage source swing, and technology parameters variations. The voltage reference bias circuits that widely used in PCB circuit is no longer suitable for CMOS that are to be fabricated using integrated-circuit technology since they make extensive use of resistors. Instead, knowing that the diode-connected MOS transistor behaves as an active resistor with the resistance of $R = \frac{1}{g_m}$, a voltage reference bias circuit can be constructed using MOS transistors replacing conventional resistors. Such a simple and practical circuit used in the industry is shown in Figure 3.26.

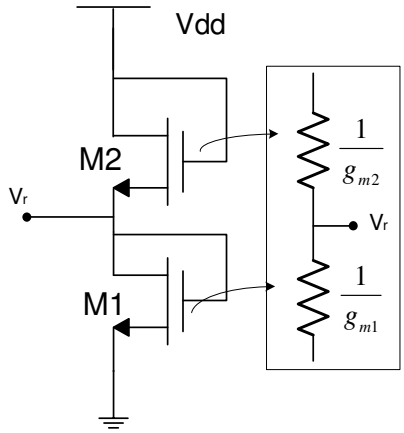


Figure 3.26 Voltage reference circuit

Recall that in a saturation region (diode-connected), the transconductance g_m depends on the sizing of the transistor W and L. Hence, the reference voltage V_r can be set by controlling the width and length of the transistor.

A cascade Wilson current mirror, as shown in Figure 3.27, is employed for independent current biasing as this type of current mirror provides large output impedance [25]. The transistor M5 and M6 have the same W/L ratio, which yield the same current in both sides of the circuit, i.e., $I_1 = I_2$. Also it can be seen that

$$V_{gs2} = V_{gs1} + I_1 R \tag{3.77}$$

Hence $V_{eff\,2} = V_{gs1} + I_1 R$, and an expression for the tail resistor R can be derived as in Equation 3.79.

$$R = \frac{2}{\sqrt{2\mu_n C_{OX} (W/L)_2 I_2}} \left[1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}} \right] \tag{3.78}$$

It is shown further that

$$g_{m2} = \frac{2\left[1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}} \right]}{R} \tag{3.79}$$

Equation 3.79 demonstrates that the transconductance of M2 is determined only by geometric ratio of M1 and M2, and is independent of the power supply voltage. In the design, the value of R is set to $10\text{K}\Omega$ so that the current I_1 equals to 0.1mA. The ratios of transistors W/L are shown in Figure 3.27. The ratios of the actually biasing current and

biasing voltages in the project design are obtained by optimizing the transistor sizing using CAD tools.

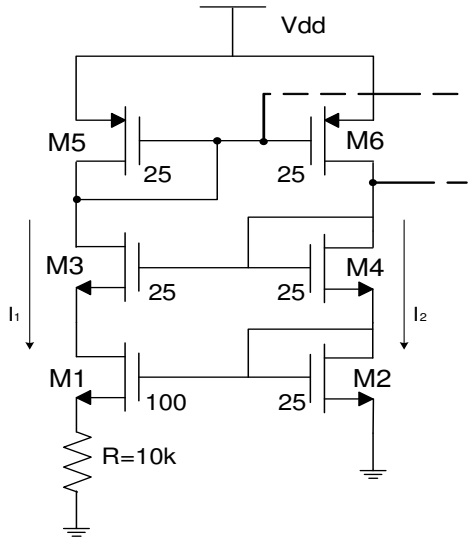


Figure 3.27 The current biasing circuit

The overall transceiver circuit is shown in the following figures. Figure 2.28 illustrates the whole transmitter circuit schematic (the exact biasing circuits are not shown due to the space limited). Figure 2.29 presents the overall receiver circuit schematic (the exact biasing circuits are not shown for simplicity). Table 3-1 presents the parameter values for the circuit components.

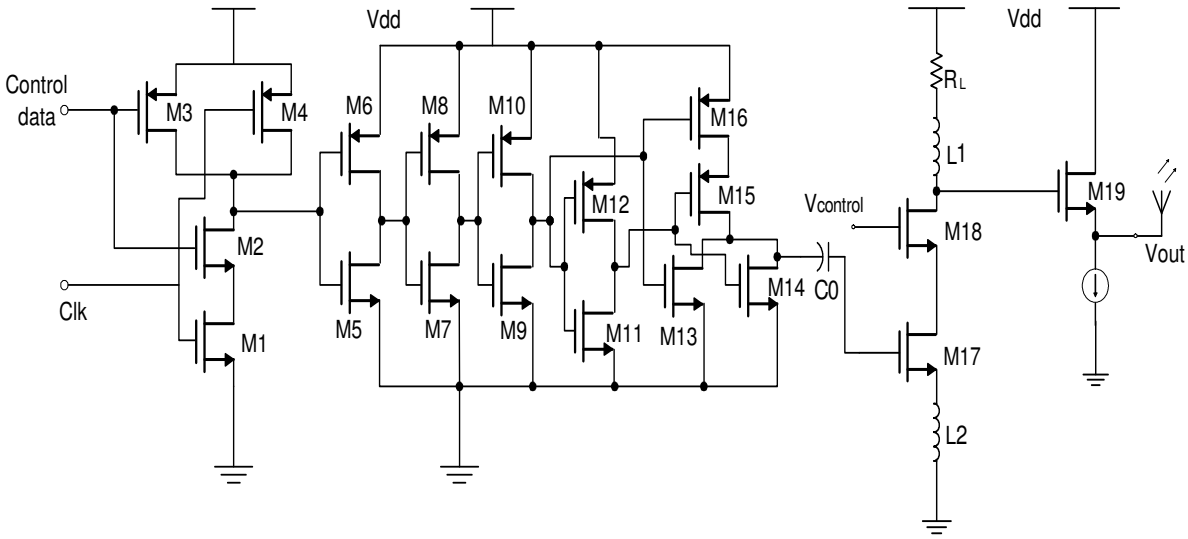


Figure 3.28 The transmitter circuit schematic

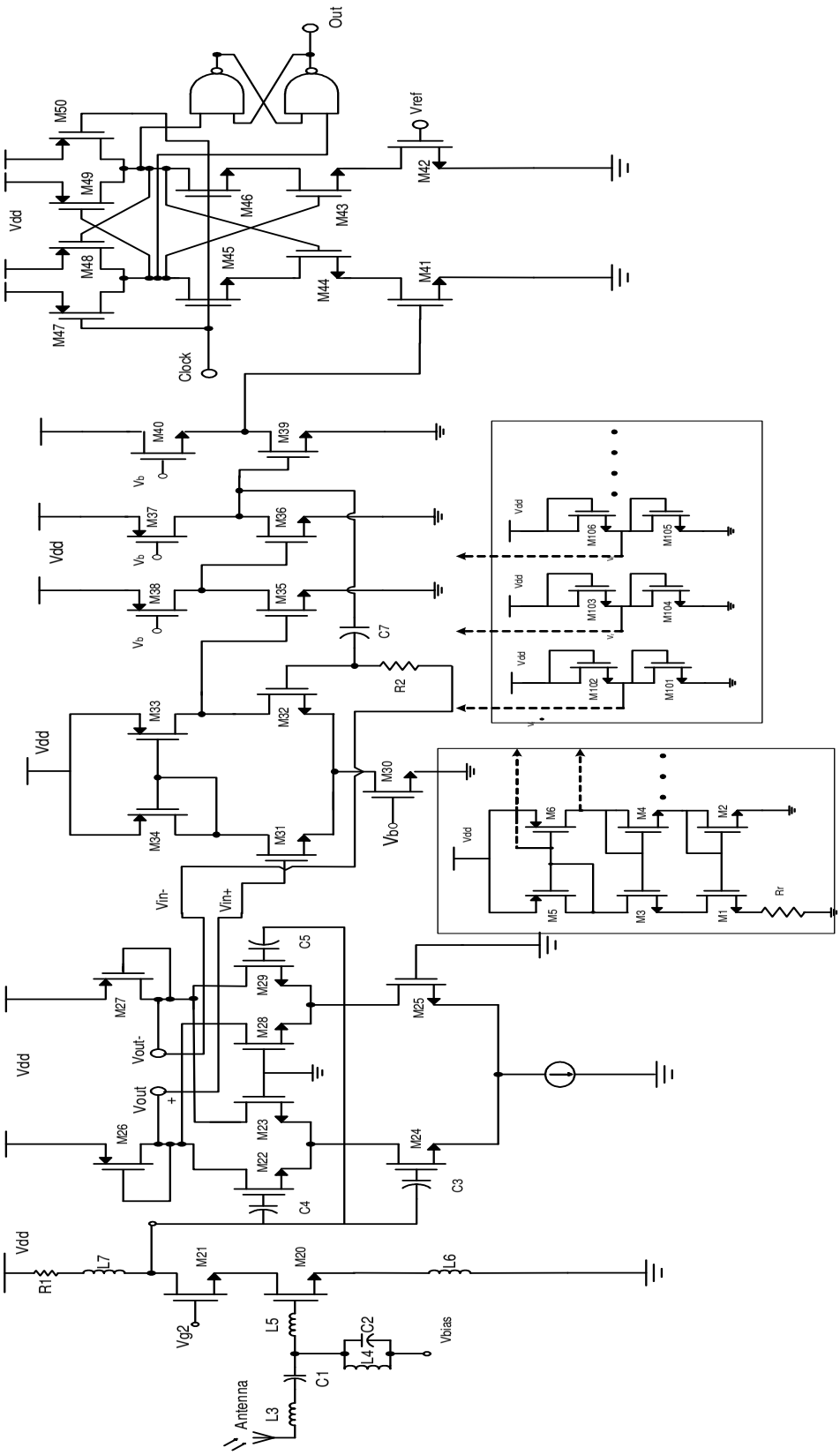


Figure 3.29 The receiver circuit schematic

Table 3-1 Circuit component parameters

Components	**Parameters**		**Components**	**Parameters**	
Capacitors	Capacitance (pF)		MOSFET	Width (μm)	Length (μm)
C0	0.5		M17	100	0.18
C1	1.2		M18	100	0.18
C2	0.49		M19	100	0.18
C3	5		M20	100	0.18
C4	5		M21	100	0.18
C5	5		M22	27	0.18
C6	5		M23	27	0.18
C7	0.8		M24	54	0.18
Resistors	Resistance (Ω)		M25	54	0.18
R_L	60		M26	54	0.18
R1	90		M27	54	0.18
R2	5k		M28	27	0.18
Rr	10K		M29	27	0.18
Inductors	Inductance (nH)		M30	54	0.18
L1	1.84		M31	27	0.18
L2	3.6		M32	27	0.18
L3	0.8		M33	54	0.18
L4	1.6		M34	54	0.18
L5	1.4		M35	54	0.18
L6	2.6		M36	54	0.18
L7	0.68		M37	54	0.18
MOSFET	Width (μm)	Length (μm)	M38	54	0.18
			M39	90	0.18
M1	1.8	0.18	M40	90	0.18
M2	1.8	0.18	M41	9	0.18
M3	3.6	0.18	M42	9	0.18
M4	3.6	0.18	M43	9	0.18
M5	1.8	0.18	M44	9	0.18
M6	5.4	0.18	M45	9	0.18
M7	1.8	0.18	M46	9	0.18
M8	5.4	0.18	M47	18	0.18
M9	1.8	0.18	M48	18	0.18
M10	5.4	0.18	M49	18	0.18
M11	1.8	0.18	M50	18	0.18
M12	5.4	0.18	M101	4	0.18
M13	1.8	0.18	M102	21	0.18
M14	1.8	0.18	M103	0.8	0.18
M15	5.4	0.18	M104	50	0.18
M16	5.4	0.18			

3.5 The UWB Antenna

The purpose of this section is to explore suitable UWB antenna for use in the UWB radar sensing and communication system. UWB antennas differ from other narrowband antennas in one basic concept: the narrowband antennas, especially in the telecommunication applications, are resonant elements that are tuned to particular centre frequencies and have relatively narrow bandwidths, with the contrast of that, the UWB antenna has much broader bandwidths and require non-resonating operation [35]. Antenna is a critical component in UWB transceiver system and is often approximated as a differentiator both at the transmitter and receiver because it yields the derivative of the transmitted or the received pulse waveform [36]. If a short Gaussian pulse is produced by the pulse generator, it becomes a monocycle pulse after the transmitter's antenna, and becomes the 2^{nd} derivative of Gaussian pulse after the receiver's antenna. The antenna also effects in extending the duration of the transmitted and received pulse [32]. Another problem when a very short time domain pulse is used to excite the antenna is the ringing effect, that is, the received pulse is spread in the time domain. Shown in Figure 3.30, this ringing effect can be seen from the received pulse by the UWB receiver. The receiver's antenna is modeled using a resistive capacitance dominated RLC circuit.

In this project, the desirable antenna is a portable antenna that must be small and low cost. The radiation efficiency is not a critical measure here so a resistive antenna can be used to suppress the ringing effect. There are a few types of antennas, such as TEM Horn, arrays antennas, that is with a good gain and can be applied for UWB applications. However, the physical size of these antennas eliminates the possibility of the applications in this thesis project. Recent researches [31,32,33,37] suggest two types of UWB antennas that are best suitable for the project applications: bowtie antenna and short Meander dipole antenna, as shown in Figure 3.31.

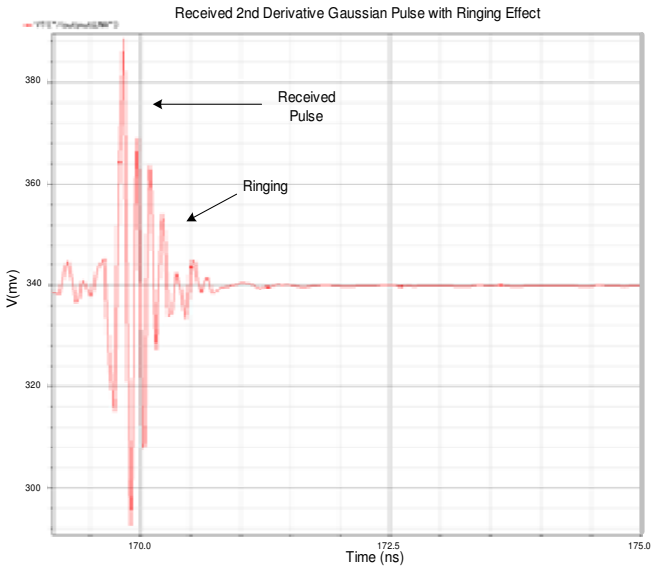


Figure 3.30 Received pulse waveform simulated in Cadence

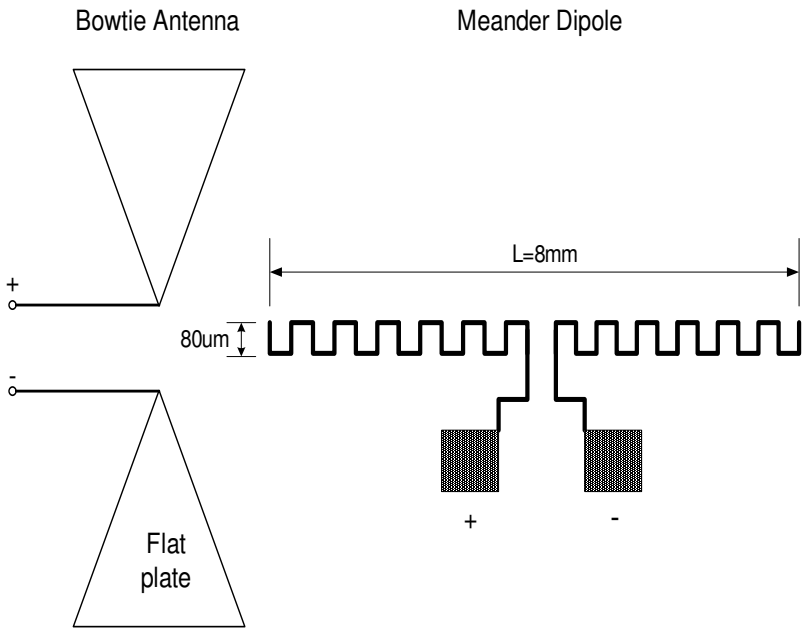


Figure 3.31 Bowtie antenna and meander dipole antenna

The beamwidth and input impedance of the bowtie antenna depend directly on its geometry, and they are nearly constant over the desired frequency bandwidth [36,37]. The bowtie antenna structure can be applied to build the textile wearable antenna using fleece fabric (a special garment material) and such textile antenna has been built and analyzed in the reference [38]. The other very attractive design is using the Meander

dipole antenna since it is very small and can be integrated in a silicon chip. Authors in [32] have successfully constructed a Meander dipole antenna of the physical size shown in Figure 3.31. This antenna was integrated with an UWB transceiver and successfully transmitted and received UWB pulse at a center frequency of 4 GHz [32].

Chapter 4 Transceiver Layout

Analog integrated circuit layout is a subject of art rather than science. It is the blueprints for implementing the circuit-level design in microscopic physical reality and it reveals the true appearance of the electronic world. Successful layout of the transceiver is a vital step leading to the successful functioning of the fabricated IC chip. It is more often the malfunctions of an analog chip are credited to the circuit layout failure rather than circuit design mistakes. After more than 30 years of IC layout study and research, thorough understanding of analog layout is still far beyond human's capability. However, IC designers need to understand the basic principle behind the commonly used device in order to develop by intuition an efficient approach of the time-economic manner for IC layout. This chapter introduces such design principles and approach for the UWB transceiver layout design in the thesis project.

4.1 Integrated Passive Device

Integrated passive devices, consisting of resistors, capacitors, and inductors, are the backbone in analog circuits. Integration of these devices into a CMOS process can provide significant performance, cost, and size advantages. Before these CMOS integrated passive devices are discussed, a cross section of the particular $0.18\,\mu m$ CMOS technology used in the design are illustrated in Figure 4.1. Six metal layers are stacked and separated by interlevel oxide (ILO), with the topmost layer of a protective overcoat (PO) made of a compressive nitride film [39]. A NMOS and a PMOS lie inside the P

epitaxial substrate at the bottom. All the circuit components, including passive devices, are integrated using the materials in Figure 4.1.

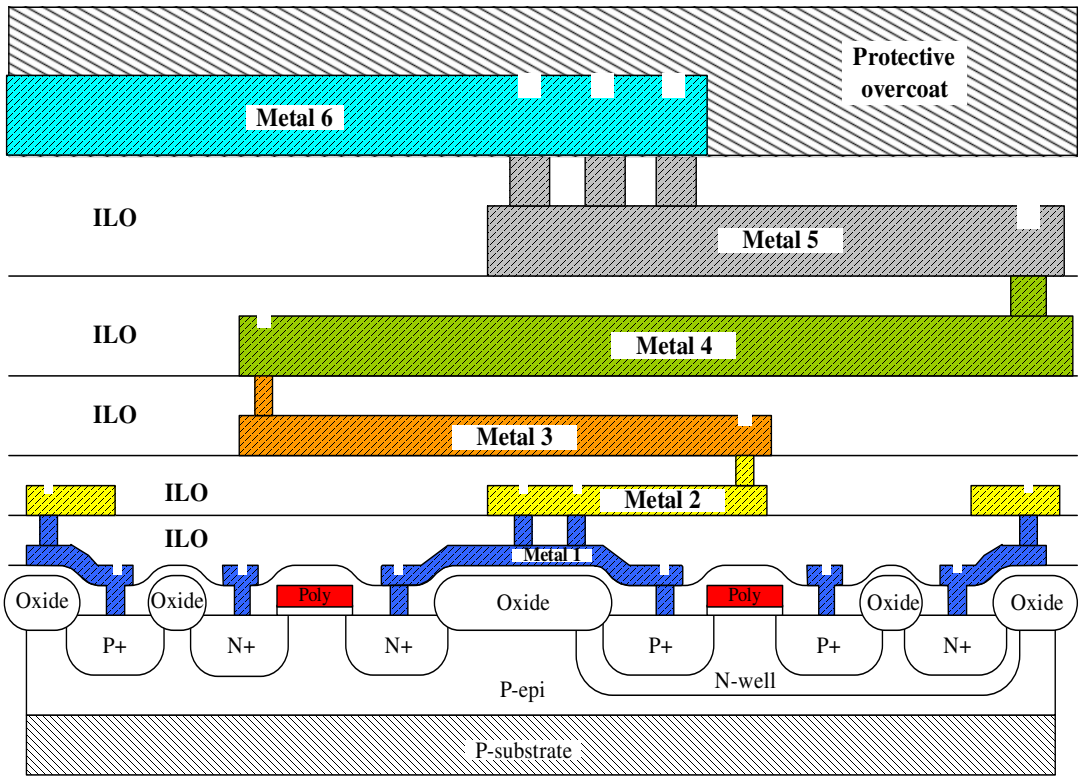


Figure 4.1 Cross section of a 0.18 μm CMOS integrated circuit

4.1.1 The Resistor Layout

In integrated circuits, resistors provide specific and controlled amounts of electrical resistance that are useful in a variety of applications, ranging from current biasing to AC higher frequency choke. There are many types of resistors such as base resistor, emitter resister, N-well resistor, high-sheet resistor, and metal resistor. However, polysilicon resistors are the most popular type of resistors in the 0.18µm CMOS process due to the high resistive density of the poly. The poly used for constructing MOS gates is heavily doped to improve conductivity and has a sheet resistance of about 25 to 50 Ω/square. Lightly doped polysilicon can have sheet resistances of hundreds or even thousands of Ohms per square [39].

The resistance value of poly resistor can be computed, given its dimensions and the poly's characteristic resistivity ρ, as shown in Equation 4.1.

$$R = \rho \frac{L}{Wt} \tag{4.1}$$

In IC manufacturing, the thickness of the poly is a constant only varying with technology; therefore, it is customary to combine resistivity and thickness into a single term called the sheet resistance R_S, where $R_S = \rho / t$, and the nominal value of R_S is 20-30 Ω/square for the TSMC 0.18µm CMOS technology. The reformed resistance is shown in Equation 4.2.

$$R = R_S \frac{L}{W} \tag{4.2}$$

By making the poly narrow, a large resistance value can be realized. The parameterized poly resistor cell can create a resistor user-defined. For example, a 5KΩ resistor is shown in Figure 4.2. Poly resistors should reside on top of field oxide to reduce the parasitic capacitance between the resistor and the substrate and ensure that the oxidation process does not cause unexpected resistance variations.

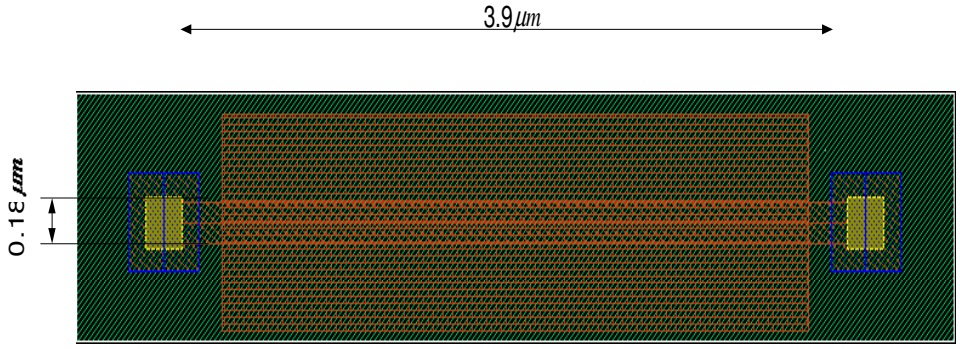


Figure 4.2 A 5K ohms poly resistor

Normally big resistors such as 5K ohms or 10K ohms do not require high accuracy. Thus, for big resistors, the tolerance is not very important, especially for the big resistors used in the voltage reference and current biasing circuit. But still, one way to improve the tolerance of a resistor is trying to make the resistor wider and longer to reduce the influence of the process variation during fabrication. However, it is more efficient to take

25% of resistance variation into account when design the circuit, and leave more headroom for resistor values.

4.1.2 The Capacitor Layout

Capacitors are a class of passive elements useful for coupling AC signals and for constructing RLC circuits. They are relatively bulky devices that store energy in electrostatic fields. Therefore, the microscopic dimensions of the die area limit the value of capacitors within a few hundred pico farads of capacitance. Most of the capacitors used in integrated circuits are parallel-plate capacitors, which consist of two conductive plates and an insulating material. Most processes offer only a limited selection of capacitors, and a few types of capacitors used in integrated circuits include Metal-insulator-metal (MIM) capacitor, Oxide-nitride-oxide (ONO) capacitor, Poly-poly capacitor, and MOS capacitor. An MIM capacitor employs silicon dioxide as its dielectric insulator, and the electrode plates are usually the metal5 layer. An ONO capacitor resembles an MIM capacitor except that it employs an oxide-nitride-oxide dielectric material to obtain a higher capacitance, but this requires more complex processing steps. Poly-poly capacitors employ two polysilicon electrodes in combination with an oxide dielectric insulator. MOS capacitors consist of a thin layer of grown oxide formed on a silicon diffusion that serves as one of the electrodes while the other electrode consists of either metal or doped polysilicon [39].

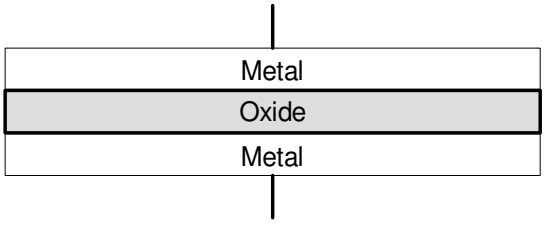
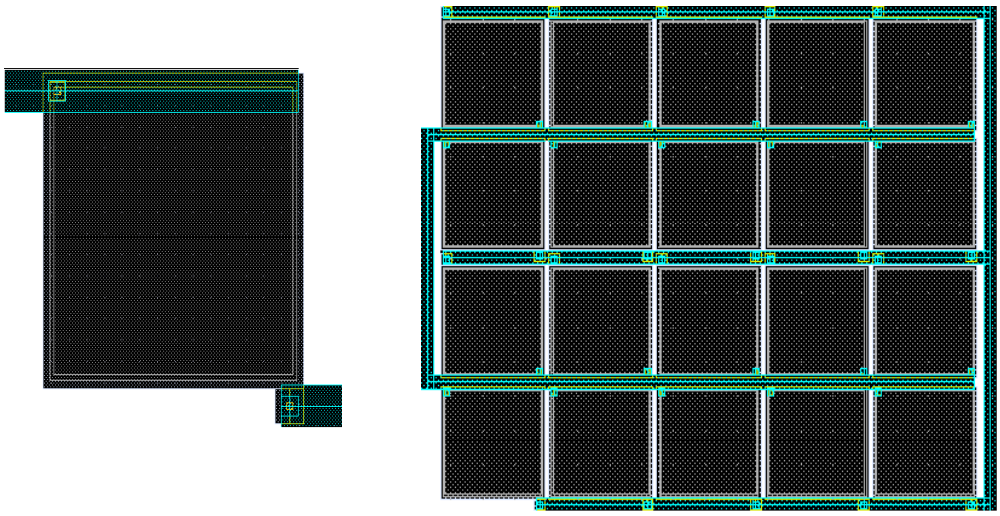


Figure 4.3 A MIM capacitor

Taking into account the trade-offs between area, capacitance tolerance, design and technology complexities, the MIM capacitor, as shown in Figure 4.3, is the most popular choice for the CMOS process. A layout of MIM capacitor is shown in Figure 4.4. The

capacitor in Figure 4.4(a) has a capacitance of 200fF with a dimension of 14.76µm by 14.76µm. Figure 4.4(b) shows a large capacitor array of 5pF total capacitance. It consists of 20 small capacitor blocks all connected in parallel. Each small capacitor block has a capacitance of 250fF with a dimension of 16.37µm×16.37µm. And the total array of 5pF capacitor has a dimension of 69.96µm×84.19µm.



(a) (b)

Figure 4.4 (a) 200fF capacitor; (b) 5pF capacitor array

4.1.3 The Inductor Layout

Inductors are another class of passive elements that store energy in the form of electromagnetic fields and they are extremely bulky devices. Normally, only a few tens of nano Henries of inductance can be integrated on a practical integrated circuit. These tiny inductors are useful only at frequencies higher than a few hundred MHz.

The simplest inductor consists of a circular loop of wire as shown in Figure 4.5. The inductance of the loop in Henry [39] is

$$L = \mu_r \mu_0 r \left[\ln\left(\frac{8r}{a}\right) - 2 \right] \tag{4.3}$$

where r is the radius of the loop and a is the radius of the wire. The constant μ_r varies depending upon the material surrounding the inductor, but in most case in integrated circuit design μ_r =1; μ_0 is the permeability of free space constant of the value 1.26μm/m.

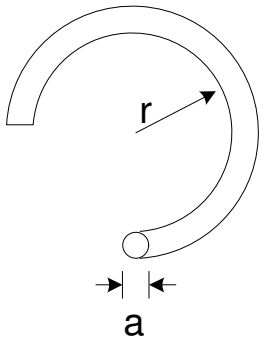


Figure 4.5 Geometries of circular loop inductor

Since a circular loop does not provide much inductance, multiple loops of wire on top of one another (called a solenoid) are used to produce the desired large inductance [40]. Each loop of wire in the solenoid is a turn, and the total inductance equals the product of the inductance of one loop multiplied by the total number of turns. In reality, solenoids are very difficult to integrate into micro-scale circuits, alternative structures called planar inductors are used in integrated circuit designs. Figure 4.6 shows a few popular types of planar inductors having square, octagonal, and circular turns. Circular planar inductors are difficult to analyze by CAD programs, square and octagonal layout geometries are more commonly used. These planar inductors are constructed in the top metal layer (metal6) in a CMOS process as the top layer is the thickest metal layer with lowest sheet resistance. The use of top metal layer for inductor construction maximizes the distance between inductors and the substrate and minimizes the parasitic capacitance. Metal 5 is used to provide the exit from the inner side of the spiral.

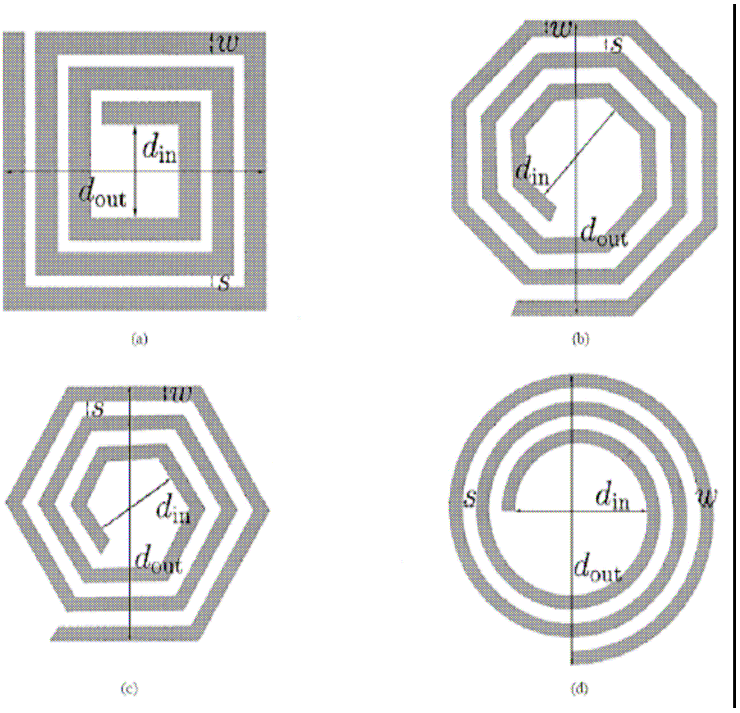


Figure 4.6 On-Chip planar spiral inductors [39]

The integrated inductor is inherent with parasitic effects and losses. Among them, eddy current losses are the most troublesome inductor parasitic. The fluctuating magnetic fields generated by an inductor set up circulating currents within nearby conductors. The total effect resembles a heat loss caused by a resistor in series. The magnitude of eddy losses depends upon the resistivity of the underlying silicon. The simplest way to avoid eddy losses is to construct the inductor over lightly doped silicon [39]. Figure 4.7 shows a Pi model of planar spiral inductor with substrate effects. The Pi model splits the parasitic capacitance and resistance between the inductor metal layer and the underlying silicon into two equal halves. L is the desired inductance and Rs represents the associated series resistance of the inductor metallization. The capacitance Cs represents the capacitive coupling between the two terminals due to overlapping, and C_{s1} and C_{s2} model the oxide capacitance between the inductor and the substrate.

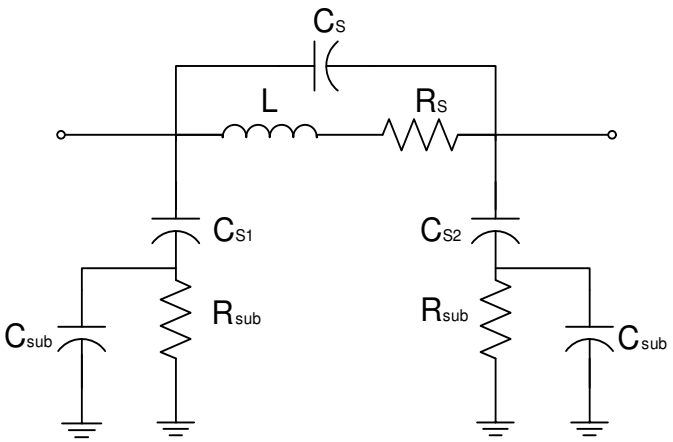


Figure 4.7 A layout model of the inductor

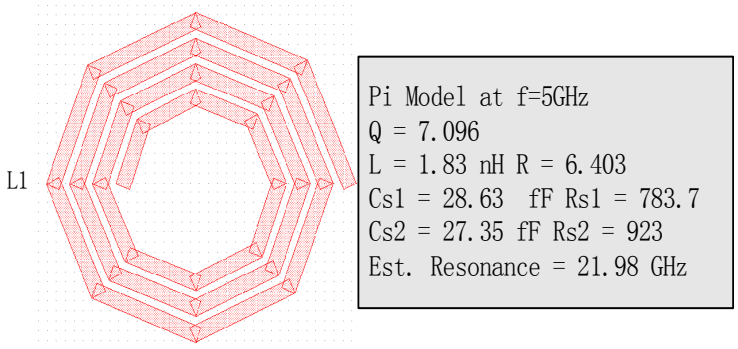
The effect of the series resistance Rs is the dominant parasitic as frequency increase because the skin effect increases dramatically at high frequency. One way to reduce the eddy losses is to heavily dope the substrate; unfortunately this reduces Q of the inductor because the parasitics are largely increased. Another way is to create a deep air cavity by etching away the silicon beneath the inductor [40]. But these techniques are not compatible with the standard IC processing.

Most of the geometric parameters of the integrated inductors nowadays are designed, optimized, and computed by computer programs. A few points must be kept in mind when laying out an inductor [39]:

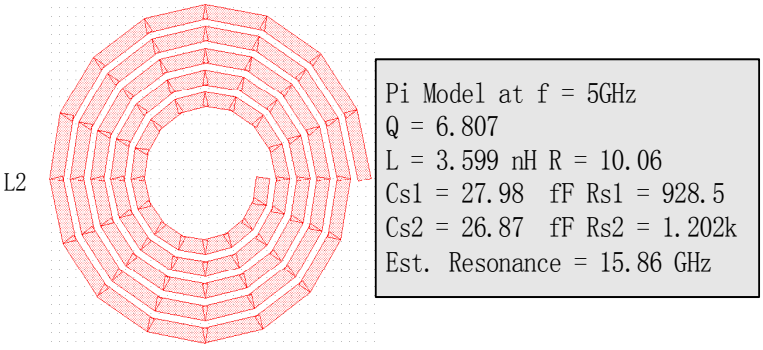
- Place inductors on the highest possible metal layers to minimize parasitic capacitance and skin effect;
- Keep away irrelevant circuit blocks from inductors to minimize eddy current losses;
- Avoid excessively wide or narrow metallization (6-15µm is optimal);
- Use the narrowest possible spacing between turns to enhance magnetic coupling and produce larger inductance;
- Do not fill the inductor center with turn (strong eddy current losses will occur in the center of the inductor);
- keep inductor leads short and straight to avoid any possible parasitic capacitance relative to the substrate.

Integrated inductors design is tedious and time-consuming. Fortunately, designing an inductor now can be aided by a tool called ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits) [41]. ASITIC analyzes and optimizes the inductors based on programmed computation on the inductor's electromagnetic behavior and possible current that flows through the inductors using the famous Maxwell's equations. By including CMOS 0.18µm technology file, this tool customizes the inductors for CMOS 0.18µm technology.

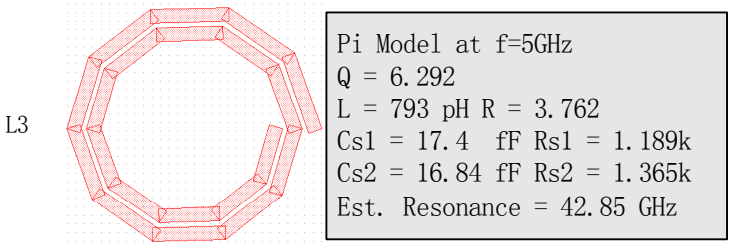
The inductor layouts as a part of this project are designed and optimized by ASITIC at 5GHz, the center frequency of the UWB pulse. Figure 4.8 shows the seven inductor layouts in the transceiver with their Pi model parameters.



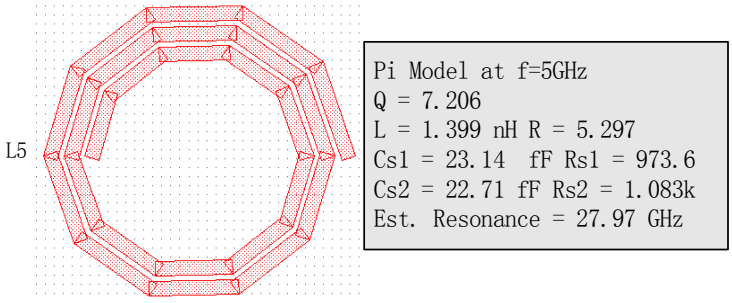
(a) The Layout of 1.83nH Inductor L1 in the transceiver circuit



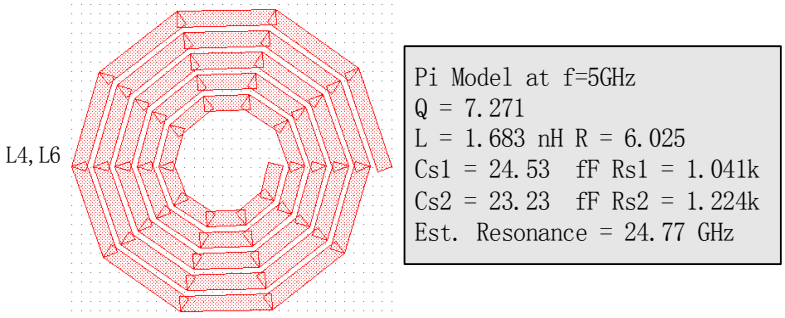
(b) The Layout of 3.6nH Inductor L2 in the transceiver circuit



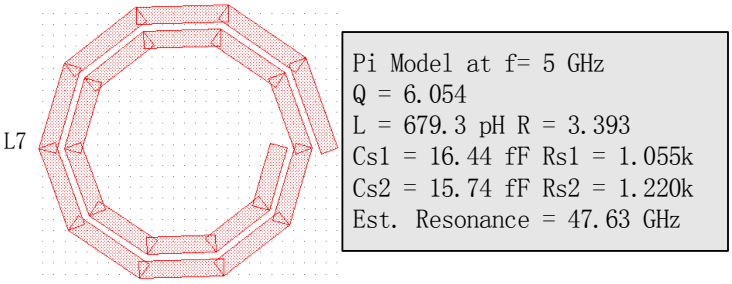
(c) The Layout of 793pH Inductor L3 in the transceiver circuit



(d) The Layout of 1.4nH Inductor L5 in the transceiver circuit



(e) The Layout of 1.683nH Inductor L4 and L6 in the transceiver circuit



(f) The Layout of 680pH Inductor L7 in the transceiver circuit

Figure 4.8 Inductor layouts by ASITIC

The dimensional parameters of inductors provided by ASITIC are shown in Table 4-1. All the inductors, as labeled with the respect to the circuit schematic as shown in Chapter 3, page 50 and 51, are designed using metal6 layer. The inductor parasitic parameters and Q values are included in Figure 4.8.

Table 4-1 Inductor dimensional parameters

Inductor	Inductance (nH)	Width (μm)	Spacing (μm)	Outer diameter (μm)	Turns
L1	1.83	8	3	90	3.5
L2	3.6	8	3	97	5
L3	0.793	8	3	78	2
L4	1.683	8	3	89	5
L5	1.4	8	3	90	2.5
L6	1.683	8	3	89	5
L7	0.68	8	3	71	2

4.2 Integrated Active Device

In the previous sections, the layouts of the passive components used in the transceiver design are introduced. In this section, the layout of the integrated active device is presented, and several issues that could affect the quality of the circuit in laying out the transistor are discussed.

4.2.1 The Layout of Large-Size Transistors

In analog circuit, the widths of transistors are usually very large (sometimes a few hundred micrometers). Putting such a wide transistor in the layout would cause a lot of problems. The first problem is the parasitic capacitance aroused by the long and thin poly gate, as shown in Figure 4.9. For a very thin and wide transistor, the long poly not only

introduces a large capacitance, but also a large parasitic resistance. These undesired parasitics consume power and delay the signal responses.

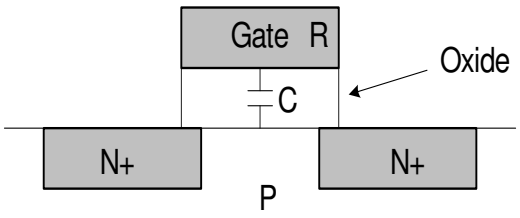


Figure 4.9 Parasitic capacitance in a large NMOS

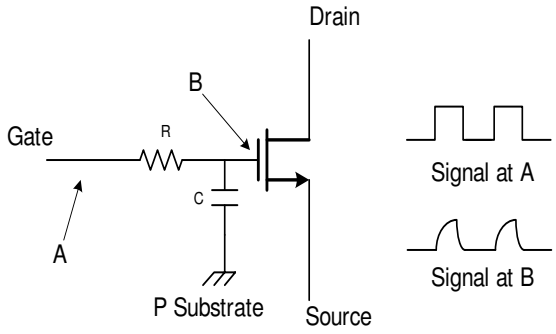


Figure 4.10 The effects of transistor parasitics

As demonstrated in Figure 4.10, the parasitic capacitance and resistance of a large transistor can be modeled by a RC circuit at the gate of the transistor (keep in mind that in reality, the parasitic capacitance and resistance are evenly spread across the poly gate). For a squared digital input signal at point A, the actual waveform that received by the transistor is the signal at point B. The actual voltage rises and falls at a slower rate than the ideal input signal at point A. It is clear that the parasitic effects slow down the signal by a time constant RC. The width of the poly gate is determined by circuit specifications and is not easy to change without changing the circuit performances. However, one wide transistor can be split into several narrow transistors in parallel geometry in order to reduce the parasitic resistance of the poly gate. This arrangement calls finger structure as shown in Figure 4.11. Figure 4.11(a) is the single transistor with a large width; this long transistor is split into four small transistors of equal size, as shown in Figure 4.11(b). The drains, sources and gates of these four transistors can be connected, respectively, to be equivalent to the transistor in Figure 4.11(a). However, space is expensive in integrated

circuit. Thus, to save space, a more efficient way to connect these four transistors is to flip horizontally the second and the fourth transistors and let the first two and last two transistors share a same source. The second and third transistors can share a same drain. In this way, the spacing between each transistor is eliminated and the resistance of the overall gate is highly reduced. Once all the drains, sources, and gates are connected by metal and poly, the new structure, shown in Figure 4.11(c), is equivalent to the original large transistor in Figure 4.11(a), but with much less parasitic resistance.

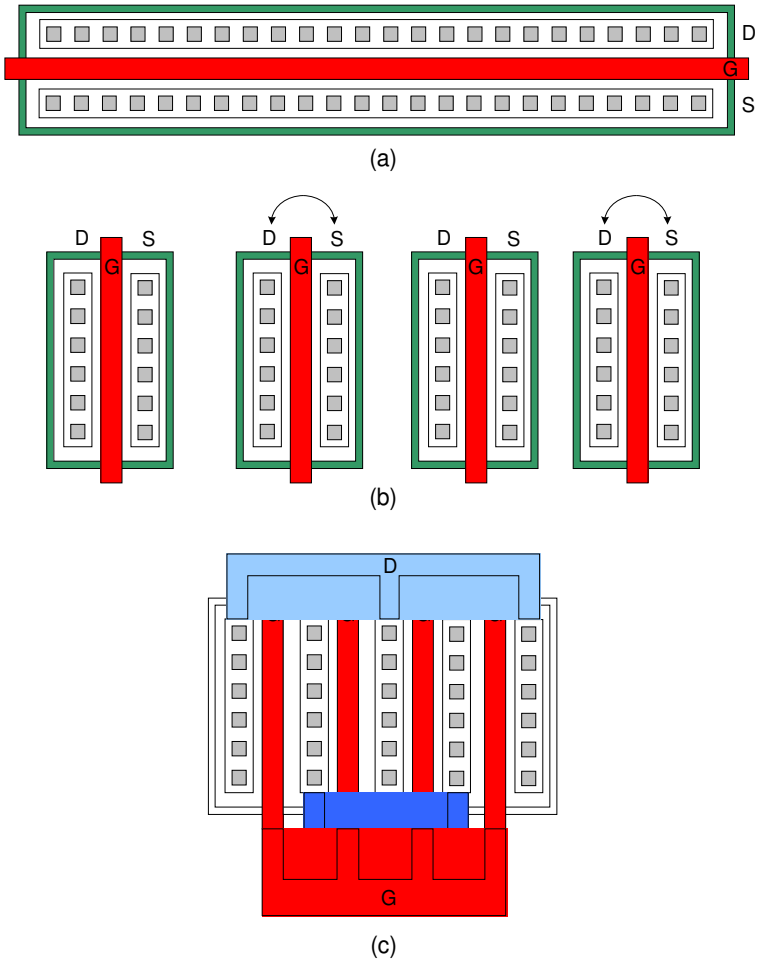


Figure 4.11 Rearrangement of the CMOS transistor geometry

Since the poly is a highly-resistive material, it is a good practice not to use long poly as the signal path for connecting other transistors. As discussed in section 4.1.1, the poly resistance is proportional to its length and inversely proportional to its width. Hence, the

poly used to connect gates in a finger structure, or any other similar cases, should be made thicker to reduce any undesired poly resistance.

4.2.2 Compact Layout

The integrated circuit design is carried out by putting small, single functional CMOS units together to form a complex circuit. The goal is to make the overall layout small. This can be optimized by arranging each individual CMOS unit within a rectangular outline. Polygon shape is easier to be coordinated than the irregular shapes. For instance, two layout examples of a differential amplifier are illustrated in Figure 4.12. The first layout has two large CMOS transistors with one on each side. Employing such transistor structure would be very space-consuming because putting together couples of this differential amplifier would result in the occupation of an enormous die area. If the large transistor can be redesigned with small transistors, the second layout is obviously a better choice for compact integration.

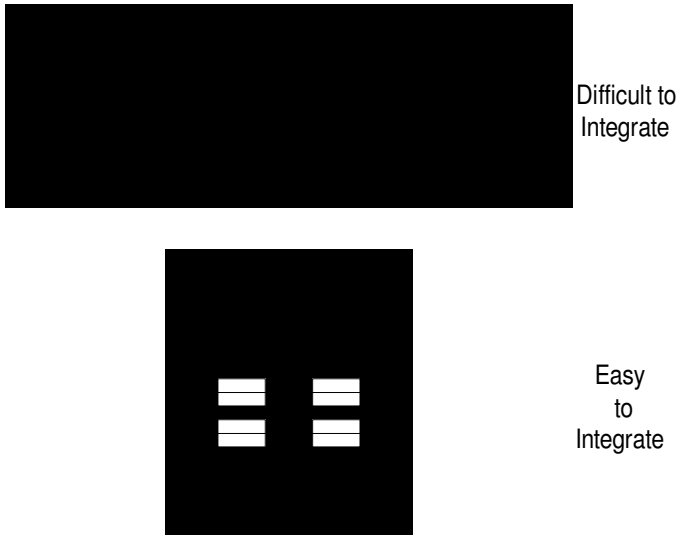


Figure 4.12 Integratabilities of different transistor layouts

4.3 Other Issues in Layout

The layout of an integrated circuit can have numerous potential weaknesses that may lead to circuit failures. Thus, it is beneficial for the circuit designer to know the safeguards against layout flaws. This section discusses a few common issues in layout that are important for designing a successful circuit layout.

4.3.1 Mismatch

In an analog integrated circuit design, mismatches are caused by microscopic fluctuations in dimensions, dopings, oxide thicknesses, and other parameters that influence circuit component values [39]. One of the layout design goals is to minimize the mismatch impact so that the overall circuitry can maintain precision and performance. The MOS transistor matching is closely related to its size, shape, and orientation. In general, large transistors match more precisely than small transistors since large poly gate helps to minimize the impact of process fluctuations; the large transistors usually have longer channel which match more precisely than the small size transistors with short channels because longer transistors have less channel-length modulation effect [39].

An expression for transistor mismatches can be represented by Equation 4.4, where S_{Vt} is the standard deviation of the threshold voltage mismatch, and C_{Vt} is a constant as expressed in Equation 4.5.

$$S_{Vt} = \frac{C_{Vt}}{\sqrt{W_{eff} L_{eff}}} \tag{4.4}$$

$$C_{Vt} = a t_{ox} \sqrt{N_b} \tag{4.5}$$

where a is the standard deviation constant, t_{ox} is the transistor gate oxide thickness, and N_b is substrate doping concentration. From the above equations, one can draw a rough conclusion that besides the size of transistor, the mismatches also relate to the thickness of the gate oxide and doping, which in turn relate to the carrier mobility that varies the transistor's transconductances. The gate oxide thickness of the MOS transistor is technology dependent and the designers do not have control over it. However, the

transconductances of the MOS transistor is affected by the orientation of the transistors since crystal axes in different directions present different transconductances under stress [40]. Transistors aligned in the same direction exhibit same transconductance than the transistors aligned in different directions with each other, as shown in Figure 4.13 below.

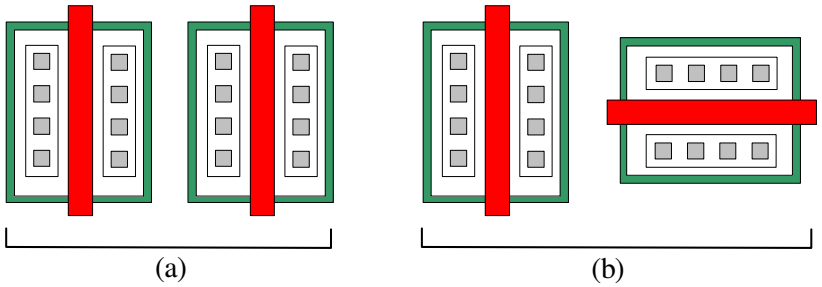


Figure 4.13 Different device orientations

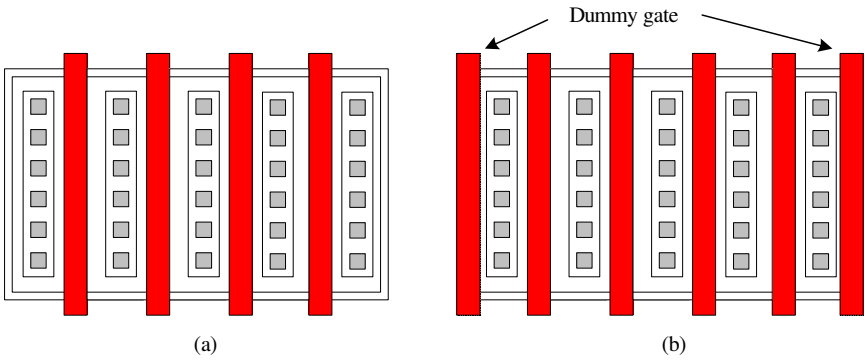


Figure 4.14 MOS transistor (a) without dummy gates, (b) with dummy gates

Photo mask misalignment during etching and non-uniform etching also causes common mismatch problems especially at the edges of poly. To minimize these causes, dummy poly added at each sides of the MOS transistor array can combat the polysilicon etch rate variations. This can be shown in Figure 4.14. The left transistor array is more vulnerable to erosion at the edges of outside poly gate. In comparison, the transistor array at the right side experiences much less problem.

The device matching not only depends on MOS transistor layout geometry, but also depends on the effective gate voltages applied to the MOS transistor. In the analog circuit, the differential amplifier and mixer require gate-source voltage matching and current biasing circuits require current matching. The ways the effective gate voltage affects

voltage matching and current matching are expressed by Equation 4.6 and 4.7, respectively [35].

$$\Delta V_{GS} \cong \Delta V_t - V_{gst1}\left(\frac{\Delta k}{2k_2}\right) \tag{4.6}$$

$$\frac{I_{D2}}{I_{D1}} \cong \frac{k_2}{k_1}\left(1+\frac{2\Delta V_t}{V_{gst1}}\right) \tag{4.7}$$

In Equation 4.6, two transistors are assumed to have the same drain current. The bias voltage difference ΔV_{GS} between two transistors is caused by mismatch, ΔV_t is the threshold voltage difference, and Δk is the difference of device transconductances and k_1 is the transconductance of the first transistor while k_2 is the transconductance of the second. V_{gst1} is the effective gate voltage of the first transistor. To minimize ΔV_{GS}, the effective voltage V_{gst} of the matched transistors should be low. To minimize the difference between currents I_{D1} and I_{D2}, V_{gst} should be kept high. Usually in analog design, a V_{gst} of less than 0.1V is applied for transistors in differential amplifier and differential pairs, and a V_{gst} of higher than 0.3V is applied at current biasing circuits.

Many other advanced matching techniques are not discussed in this thesis since they are not employed in the transceiver layout. Also, still a lot of causes of device mismatches remain mystery and wait for researchers to explore. Experiences in analogy circuit layout sometimes play a more important role when producing a successful layout.

4.3.2 Symmetry

In analog circuit layout, two circuit units are designed to be identical to achieve same functional performance. Unit matching requires symmetric layout design. The symmetric design is extremely important for sensitive digital blocks and analog circuit blocks using differential signals such as the differential amplifier that detects and amplifies the difference of the two signals. Figure 4.15 illustrates a symmetric layout for the differential amplifier used in the UWB transceiver circuit. The right half of the layout is

the exact replica of the left half in this layout. Such arrangement minimizes the gradient-induced temperature, stress, and oxide thickness mismatches between two sides. It also yields, at its greatest capability, the same electrical properties for both halves of the amplifier. From the circuitry point of view, the differential off-set voltages are minimized.

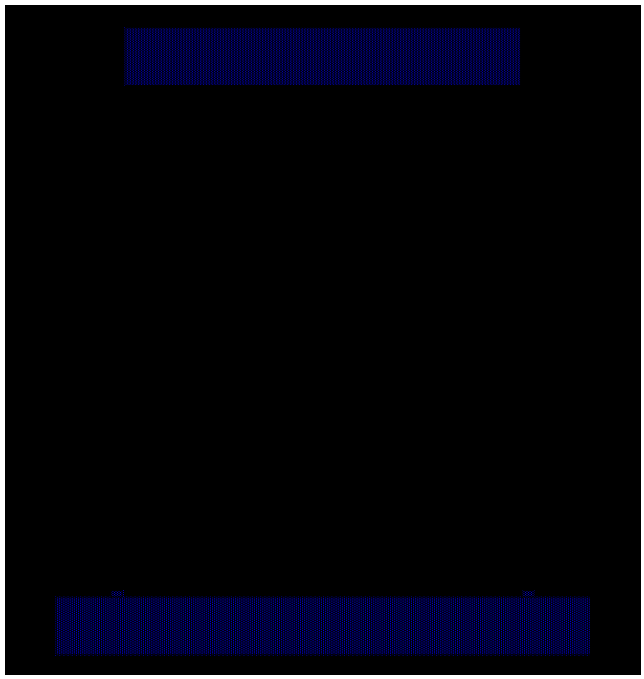


Figure 4.15 Symmetric differential amplifier layout

4.3.2 Guard Ring

The latch-up and minority charge injection problems becomes more severe in a mixed signal integrated circuit layout. Deep sub-micron CMOS makes this problem even worse. A technique to reduce this problem is the use of guard rings either around the analog blocks that are sensitive to interference or around the noisy blocks. A popular way is to place an N-well ring in the P-epi on top of P substrate surrounding the source of injected electrons [40]. Figure 4.16 shows an example application of an N-well guard ring used to isolate a sensitive circuit from other noisy circuits experiencing large voltage transients. The cross section of a guard ring is shown in Figure 4.16(b). The guard ring is connected to the positive voltage supply to enhance the electrons collection mechanism. In the

UWB transceiver, an N-well guard ring is employed to isolate the transmitter from the receiver. Another N-well guard ring is placed around the comparator to reduce the negative charge injection from the clock switching.

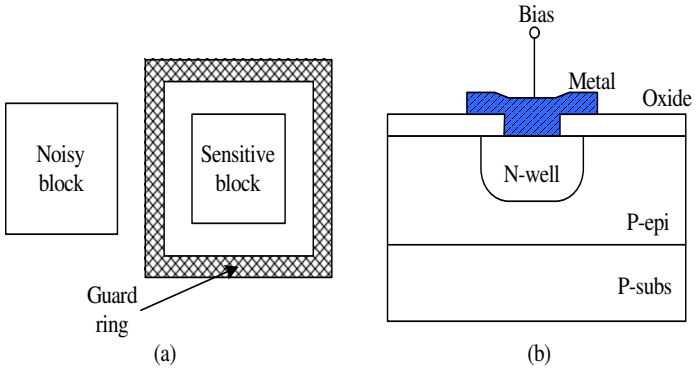


Figure 4.16 (a) Sample guard ring, (b) Cross section of a popular guard ring

4.3.3 The Antenna Effect

The antenna effect is the damage of thin gate dielectrics by the overstress of the electrical charges collected by either metal conductors or poly from surface of the wafer after those charges are deposited by the process of dry etching [39]. This effect can generate a large leakage current that can break down the normal transistor operations. Figure 4.17 shows an example of antenna effect by an antenna-shape long poly connected to the gate poly.

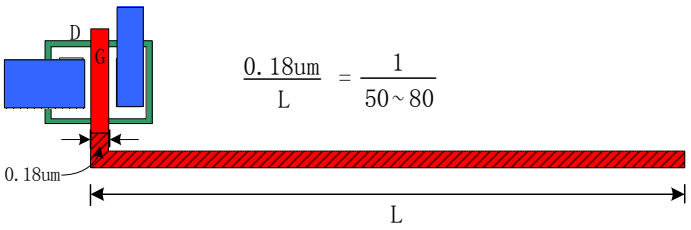


Figure 4.17 The antenna effect caused by long poly

The vulnerability of a given geometry to the antenna effect depends upon the ratio of the total length to the active gate length of a transistor [41]. The poly geometry ratio of larger than 50 to 80 is considered to have very high risk of collecting electrical charges.

The maximum allowable geometry ratios for metal layers are smaller than poly since the metal is more sensitive to electrical field variations. Any layers whose antenna ratios exceed the maximum allowable ratios should be rerouted to reduce the antenna effects. Different layer involves different techniques. In the case of Figure 4.17, the long poly path can be broken by a metal jumper, as shown in Figure 4.18. The long poly now becomes two separate geometries. The poly connecting to the gate of the transistor on the left has a very small antenna ratio. The poly on the right has zero antenna ratios if it is not connected to any gates of transistors. Therefore, by putting a metal1 layer to separate a long poly, the antenna effects are greatly reduced, if still exist. Similar techniques can be applied to reduce the antenna effects in metal layers.

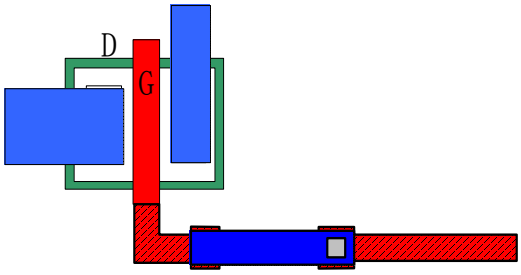


Figure 4.18 A layout susceptible to the antenna effect

Another method to reduce the antenna effect is to place a diode near the transistor that could possibly be affected by the antenna effect caused by any long metal connected to the gate poly. Once the long metal path collects electrical charges high enough, the diode will transfer these charges to the P substrate.

4.3.4 Signal Interconnection

Signal routes are used to connect different circuit blocks in a layout. TSMC 0.18 μm CMOS technology provides six levels of metallization. Therefore, the placement of circuit blocks is only constrained by matching and packing area. Signal routing in most cases will not present a problem as long as the designer leaves a little space between circuit blocks. However, in RF circuit layout design, the signal's electromagnetic energy

propagation must be considered. The metal wire resembles a waveguide for high frequency signals as the fiber to optical waves. The 90-degree wire corners cause signals partial reflection, as illustrated in Figure 4.19(a). Thus, a good compensation is to make the wire turning at 45-degree, as shown in Figure 4.19(b). By applying a 45-degree corner, the signal is reflected to the next adjacent wire segment, like a submarine telescope. This same technique is applied when routing the very wide power line with very large current flowing. The 45-degree corners also help to reduce heat loss.

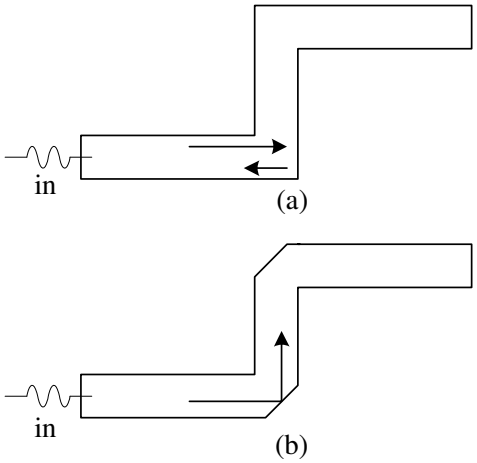


Figure 4.19 Signal path in high frequency

Another thing worth to mention is the via connections between two wide routes of different metal layers. Evenly distribution of as many as possible vias in the overlap area between two metal wires helps to reduce parasitic resistance and current congestion in term of heat loss.

4.4 Die Floor Planning and Final Layout

The final layout of an analog integrated circuit needs good planning and forethought. Before the actual layout begins, a sketch of the layout, or floor plan in another name, should be created to guide for constructing the pad ring and the top level layout. The

floor plan indicates the component locations and estimated areas of each blocks and total area. Figure 4.20 shows the die floor plan of the designed UWB transceiver.

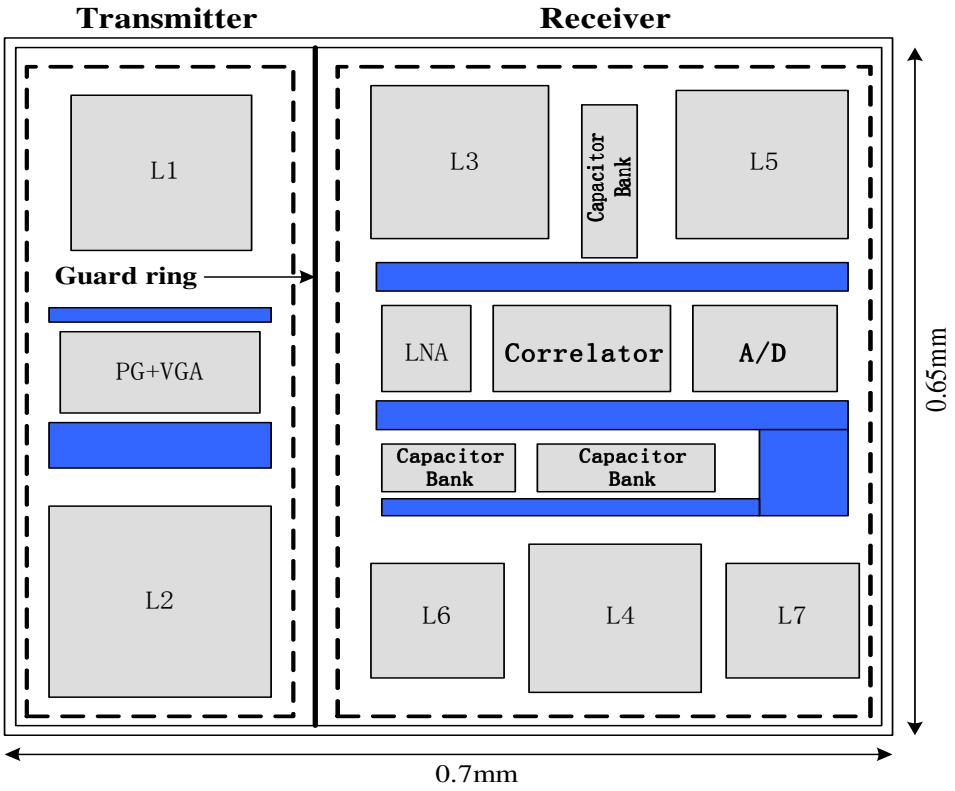


Figure 4.20 Die floor plan

In this floor plan, the seven inductors occupy most of the die area. About 20% of the empty space is reserved for power wires and signal wires routing. The estimated die area without pad frame is 700μm×650μm.

The final layout using the 0.18μm CMOS process of the UWB transceiver is presented in Figure 4.21. The die with pad ring occupies an area of 1.026mm×1.242mm. The input and output pads are separated by power and ground pads to limit the signal interferences among pads and other power-related issues. More Vdd and Gnd pads can limit the parasitic inductance effects of the bond wires on the transceiver [31].

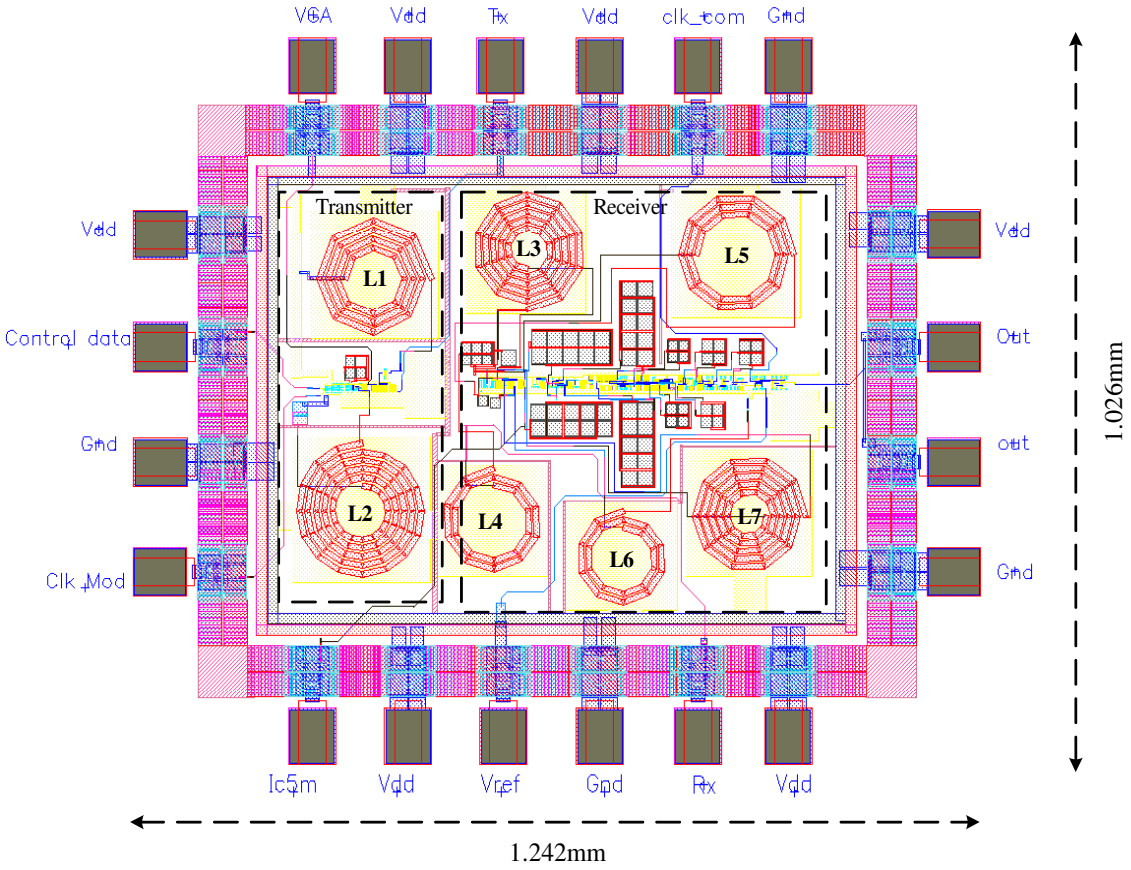


Figure 4.21 The UWB transceiver layout

The transmitter and receiver are separated by a guard ring to reduce interference between them. The transmitter and receiver both use 1.8V power supply. The transmitter's antenna will be connected to the output pin Tx, and the antenna at the receiver side will be connected to the output pin Rx. The input data comes in from the input pin Control_data. The transmitter pulse level is adjusted through pin VGA. The transceiver output is connected to the output pin Out. The input/output pins are $65\mu m \times 75\mu m$ metal pads with electrostatic discharge (ESD) protection. The layout passed the TSMC 0.18µm CMOS design rule check (DRC) and passed the pre-tape-out checks with no errors to ensure a successful design after fabrication.

Chapter 5 Results and Analysis

The UWB transceiver designed in this project is used for the UWB radar unit in a UWB bio-sensor network. With minor circuit modifications, the transceiver can also be employed for the communicating between the Control and DSP unit, and the base station, as proposed in Chapter one. The UWB transceiver was designed and simulated using Cadence for TSMC 0.18µm CMOS process. Functions of the circuits for both for radar sensing and communications were simulated.

5.1 Radar Sensing Verification

The performances of radar sensing were simulated in this section to verify the transceiver design. Parasitic effects from layout were included in the post-layout simulation. Since physical extractions of inductors were not possible, their accurate models at 5GHz were used.

5.1.1 Radar Sensing Simulation Setup

The UWB transceiver was simulated using Cadence Analog Environment for the TSMC 0.18µm CMOS process. A 1.8V DC supplied to both the transmitter and receiver. The transmitted pulse width was 0.2ns, with a repetition period of 2ns. The control signal frequency was set at 6.7Mbps (depends on how frequently the Control and DSP unit sent pulses to a target) and the control signal bit width was 10ns, allowing five pulses in one

pulse bundle to increase level of delectability at the receiver. The comparator was clocked at 100MHz, which means that it samples the waveform every 10ns. The reference voltage of the comparator was set to 670mV. The antennas were modeled as a capacitive-dominant RLC circuit and the radiation resistance is 50Ω [8,15,35]. However, RLC circuit produces resonant, and in an ultrawide band system, the resonant-type antenna is not desired. Therefore, the inductance and capacitance values in this model are extremely small, and the R of 50Ω dominates. For simplicity, only white noise and signal attenuation were assumed in the simulation. Hence, a 50Ω lossy transmission line model was used to represent the free space and signal path through human body. This path reflects the simplest scenario of the pulse propagation. In this scenario, only the power attenuation and environment white noise are considered both in building the transmission path and the circuit design. This is not a true reflection in reality. Therefore, a more accurate transmission and scattering model for UWB signal through different human organic tissues with various dielectric properties must be developed and analyzed. To create a moving target equivalent, two transmission lines with different lengths were employed to represent different target locations: the transmission line 1 has a short length and it represents the target at a closer position; the transmission line 2 has a longer length and therefore it takes longer signal propagation time, and thus represents the target at farther location. Switching between the two transmission lines were controlled by a clocked voltage switch. Figure 5.1 shows the system simulation setup.

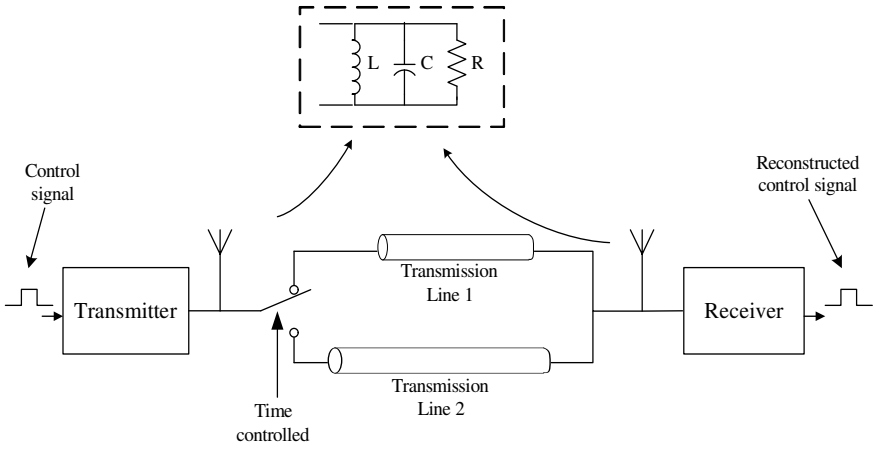


Figure 5.1 Simulation setup for radar sensing

5.1.2 Simulation Results and Analysis

The distance between the transmitter and the target is the key consideration to decide the pulse repetition rate. The rate should be in a range so that the first transmitted pulses bundle is able to reflect back to the receiver before the second pulses bundle is sent out. This setting avoids the signal distortion caused by the direct collisions between the reflected signals and the transmitted signals. Figure 5.2 shows the circuit schematic simulation results, and Figure 5.3 shows the post-layout simulation results. Figure 5.2(a) is the control signal from the Control and DSP unit. Figure 5.2(b) is the successfully reconstructed control signal that reflected from human heart. Figure 5.2(c) shows the pulse trains sent out by the transmitter, and Figure 5.2(d) illustrates the reflected pulse train received at the receiver front-end. The slight distortions in the received pulses occur because the transmitter and receiver are not perfectly matched to the 50Ω transmission lines. The transceiver reached the steady state within the first 20ns, thus the comparator ignored the first pulse bundle sent by the transmitter. To reduce the simulation time, a target with much faster moving rate than the heart wall was assumed here. T1 is the first time interval between output and reflected signals at the time when the target is close to the transceiver. T2 is longer than T1, indicating that the target moved further away from the transceiver. Different channel lengths were used to represent different target positions in the simulation, as mentioned before. There were small bursts of pulses between the transmitted and received pulse bundles, as shown in Figure 5.2(d). These bursts were signal reflection from the input of the receiver caused by imperfect match between the transmission line and the LNA.

As shown in Figure 5.3, the parasitics has little effects on the overall circuit functioning. The post-layout schematic view was extracted both with parasitic capacitance and parasitic resistance. The physical extractions of inductor are not possible by the Cadence tools. The pi models of inductors accurate at 5GHz were built at the test bench for post-layout simulations.

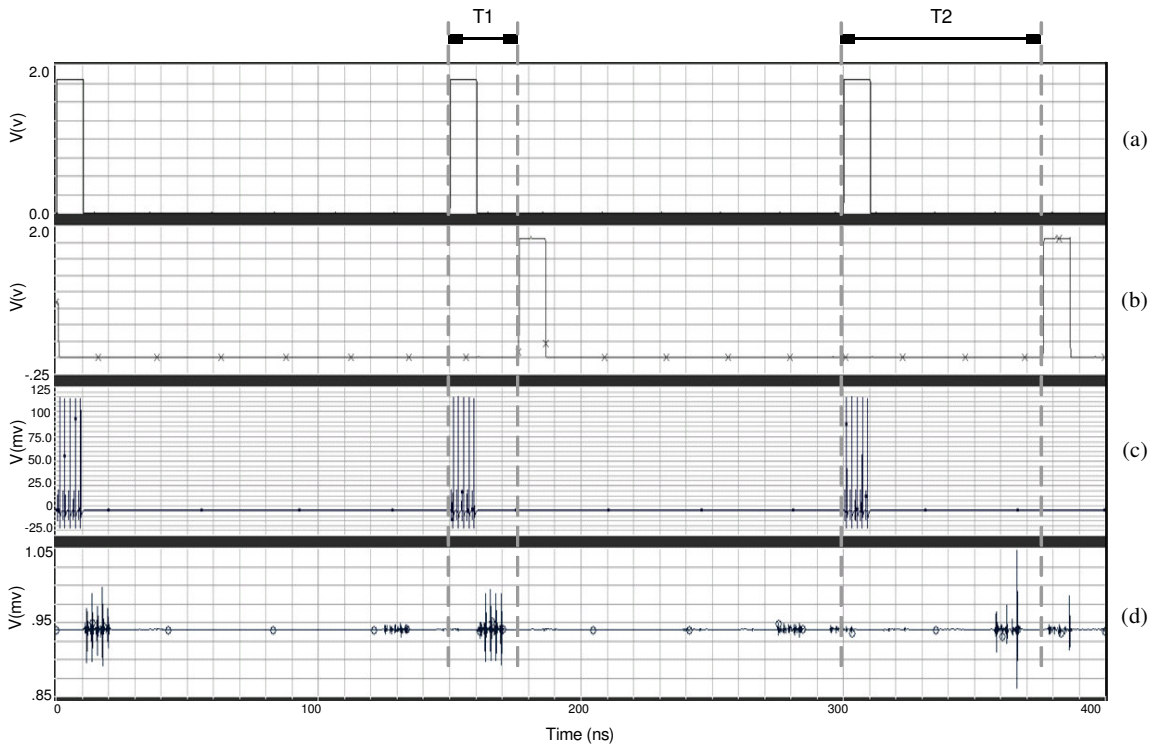


Figure 5.2 Simulated waveforms of data patterns: (a) input data, (b) the detected pulse in binary form at the receiver side, (c) the transmitted pulse bundle waveform, (d) the reflected pulse bundle waveform.

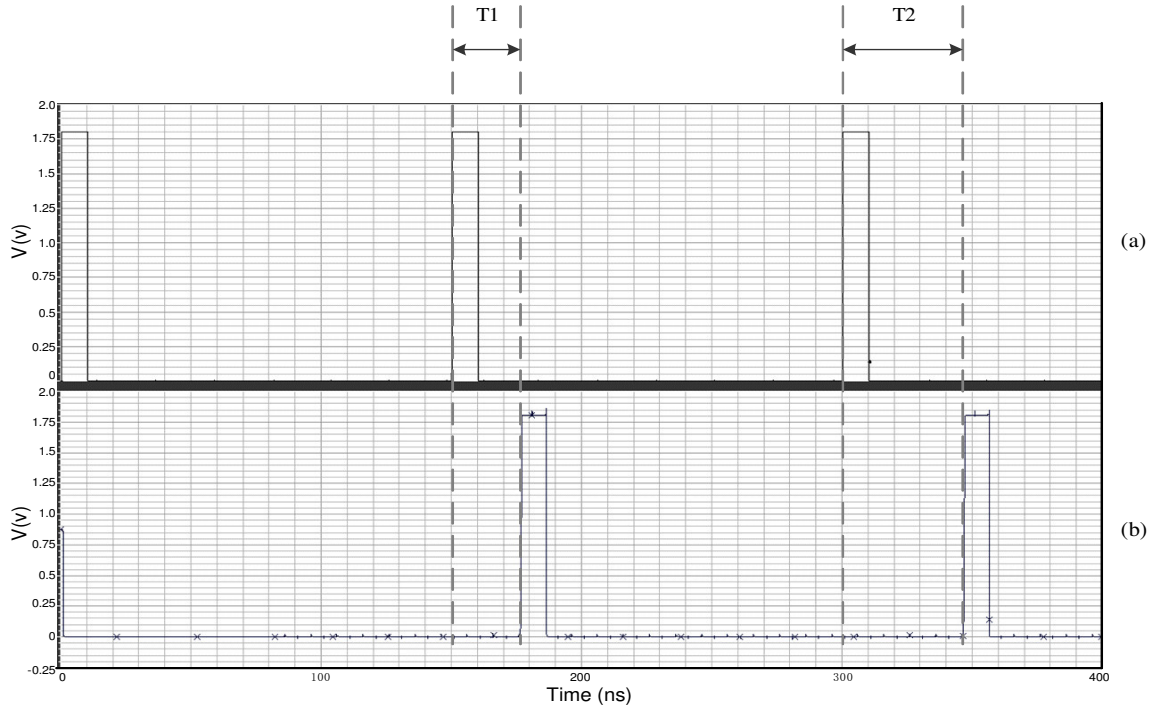


Figure 5.3 Post-Layout Simulation: (a) input control signal into transmitter, (b) the reconstructed control signal at the receiver

A single transmitted pulse has maximum amplitude of 70mV and a duty cycle of 0.1. The maximum possible average power of each pulse was estimated to be $9.8\,\mu W$ by Equation 5.1.

$$P_{ave} = \frac{1}{T}\int_0^T \varepsilon(t)\,dt \tag{5.1}$$

where T is the pulse period 2ns and $\varepsilon(t)$ is the pulse energy function of time. The pulse bandwidth was estimated as 5GHz (wider bandwidth possesses a lower power). The pulse power spectrum density was calculated to be -57.077dBm/MHz. This power level is well below the FCC UWB spectrum limit of -41.3dBm/MHz. Many studies on the evaluations of the effects of human exposure to UWB signal showed that the pulses in ultrawide band were not posing any harm to human tissues [3,11,15]. Furthermore, the studies by [42] demonstrated that the FCC UWB power limitation is far below the international Specific Absorption Rate (SAR) standard of maximum 2W/kg of human absorption in UWB frequency range. The UWB transceiver only sends pulses toward a very small area on human chest, and the power emission just under -41.3dBm/MHz over 10 grams human tissues yielded absorption level of 70.8pJ/kg [43]. The receiver sensitivity is achieved with the lowest power of -73.01dBm. The total transceiver power consumption in the post-layout simulations is 40mW. The driver amplifier at the transmitter and the LNA and the integrator at the receiver consumed most of the power.

5.2 UWB Communication Simulations

The performances of short range UWB communication were simulated in this section to verify the transceiver design. Parasitic effects from layout were included in the post-layout simulation. The accurate models of inductors at 5GHz were used in the post-layout simulation.

5.2.1 Communication Simulations setup

Similarly, the transceiver circuit schematic and layout for UWB communications were simulated under Cadence Analog Environment for TSMC 0.18 μm CMOS process. The power supply voltage is 1.8V. For communication purpose, the data rate is much higher than the sensing applications. Therefore, the transmitter clock frequency was set at 500MHz and the input test data was set at 200Mbps. The comparator is clocked at 200MHz. The transmitted pulse has a width of 0.2ns with a repetition period of 1.8ns. Each single input data bit has the width of 5ns, which is represented by three pulses. Less pulses in one data bit increases the difficulty to reconstruct the data information with a reward of ultra fast data rate. The integrator time constant RC at the receiver was modified accordingly to integrate the charges of three pulses instead of five pulses in the sensing case. The comparator sampled the waveform every 5ns, and the comparator reference voltage was set at 670mV by simulations. The antennas were modeled using the same capacitive-dominant RLC circuit. Since RLC circuit produces resonance, and in an ultrawide band system, the resonant-type antenna is not desired. Therefore, the L and C value in this model were set extremely small. Only the R dominated with the radiation resistance of 50Ω. A 50Ω transmission line model was used here to represent the free space channel. Figure 5.4 shows the system simulation model.

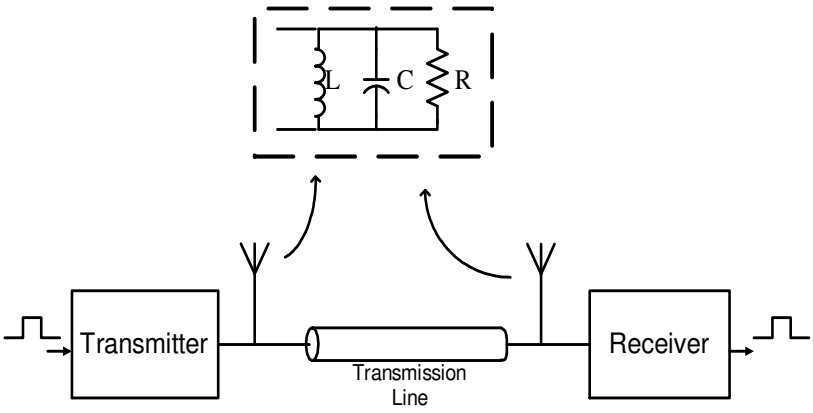


Figure 5.4 Simulation setup for UWB communications

5.2.2 Simulation Results and Analysis

Figure 5.5 shows the simulated waveforms from binary data into the transmitter to reconstructed data coming out of the receiver. Figure 5.5(a) is the input data, and Figure 5.5(b) is the pulses sent from the transmitter. Three pulses represent one bit, as shown in the plot. Figure 5.5(c) shows the waveform after the multiplication function at the receiver. Figure 5.5(d) is the comparator clock signal. The voltage comparison was made every time when the clock signal was on the rising edge. Since the comparator clock enables and disables the data reconstruction as shown in the waveforms, this clock signal can be used as enable signal to define the system initialization time and disable the system, if needed. Figure 5.5(e) is the reconstructed data that resembles the input data after the enable signal. The clock signal at the comparator has 30ns delay, resulting in same time delay for the data reconstruction at the receiver. Figure 5.6 shows the results of the transceiver simulation using different input data sequence. The signal latency, without considering the channel delay, is 5ns. Data transmission rate is 200Mbps, and data is successfully reconstructed at receiver. Figure 5.7 shows the post-layout simulations for UWB communications. The post-layout schematic view was extracted both with parasitic capacitance and parasitic resistance. The physical extractions of inductor are not possible by the Cadence tools. The pi models of inductors accurate at 5GHz were built at the test bench for post-layout simulations. Total power consumption in the post-layout simulations is 57mW. The higher power consumption was due to the faster clock switching both at the pulse generator of the transmitter and at the comparator of the receiver. Increased clock switching rate causes large switching currents, which in turn, increasing the power dissipation. Simulations of 150Mbps data transmission rate yielded an average power consumption of 55mW, and 100Mbps data transmission rate yielded an average power consumption of 52mW. Increasing the length of the transmission line increases the data reconstruction errors. Simulations showed that the first data error appeared when the length of the transmission line was increased to 15 meters. More data errors occurred when the length was increased further.

The signal reconstruction was delayed by 60ns as shown in Figure 5.7(d). The parasitic effects have increased the integrator circuit setting time. The parasitic

capacitance and resistance affected the dumping ratio of the integrating circuit and the circuit was under damped.

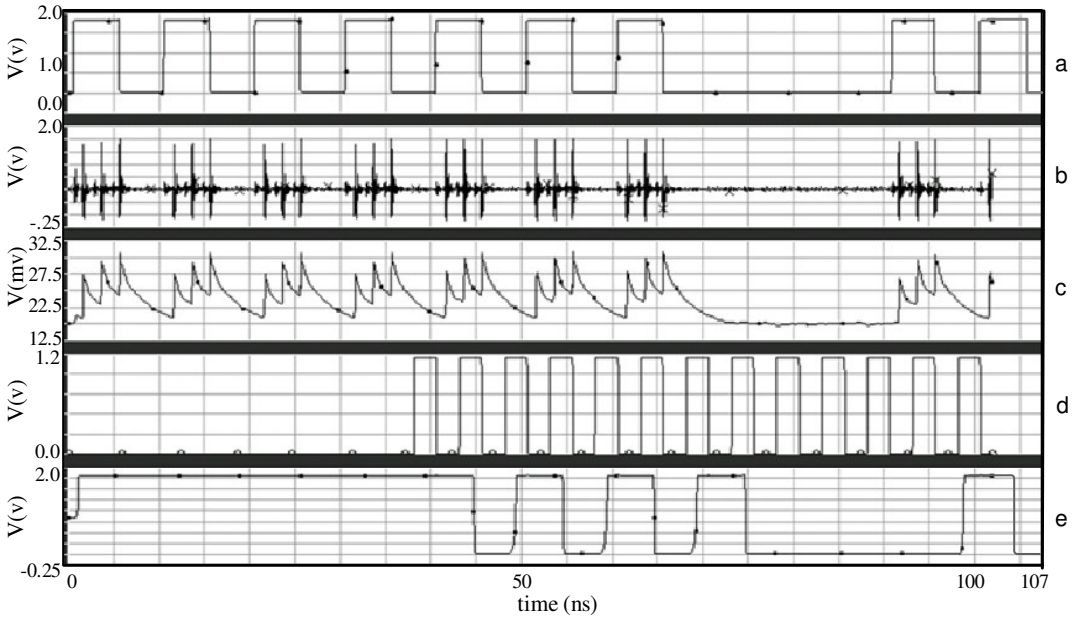


Figure 5.5 Simulated waveforms of data patterns: (a) input data, (b) pulse sequence at the input of receiver, (c) output at the correlator, (d) the comparator clock, (e) reconstructed data.

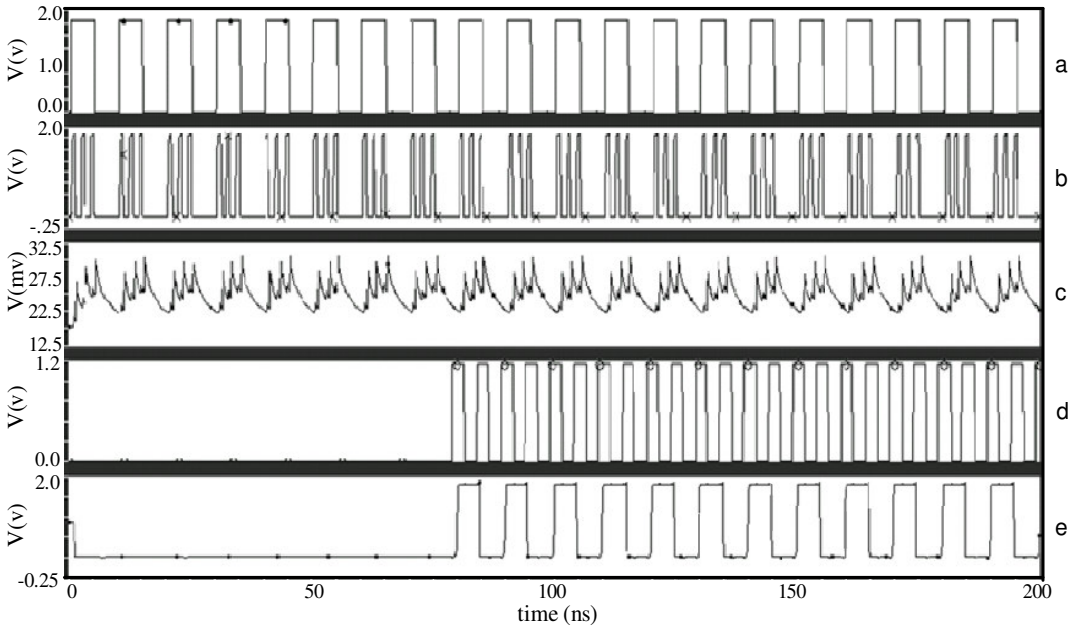


Figure 5.6 Simulated waveforms of data patterns: (a) input data, (b) modulated clock signal, (c) waveform after the correlator, d) the comparator clock, (e) reconstructed data

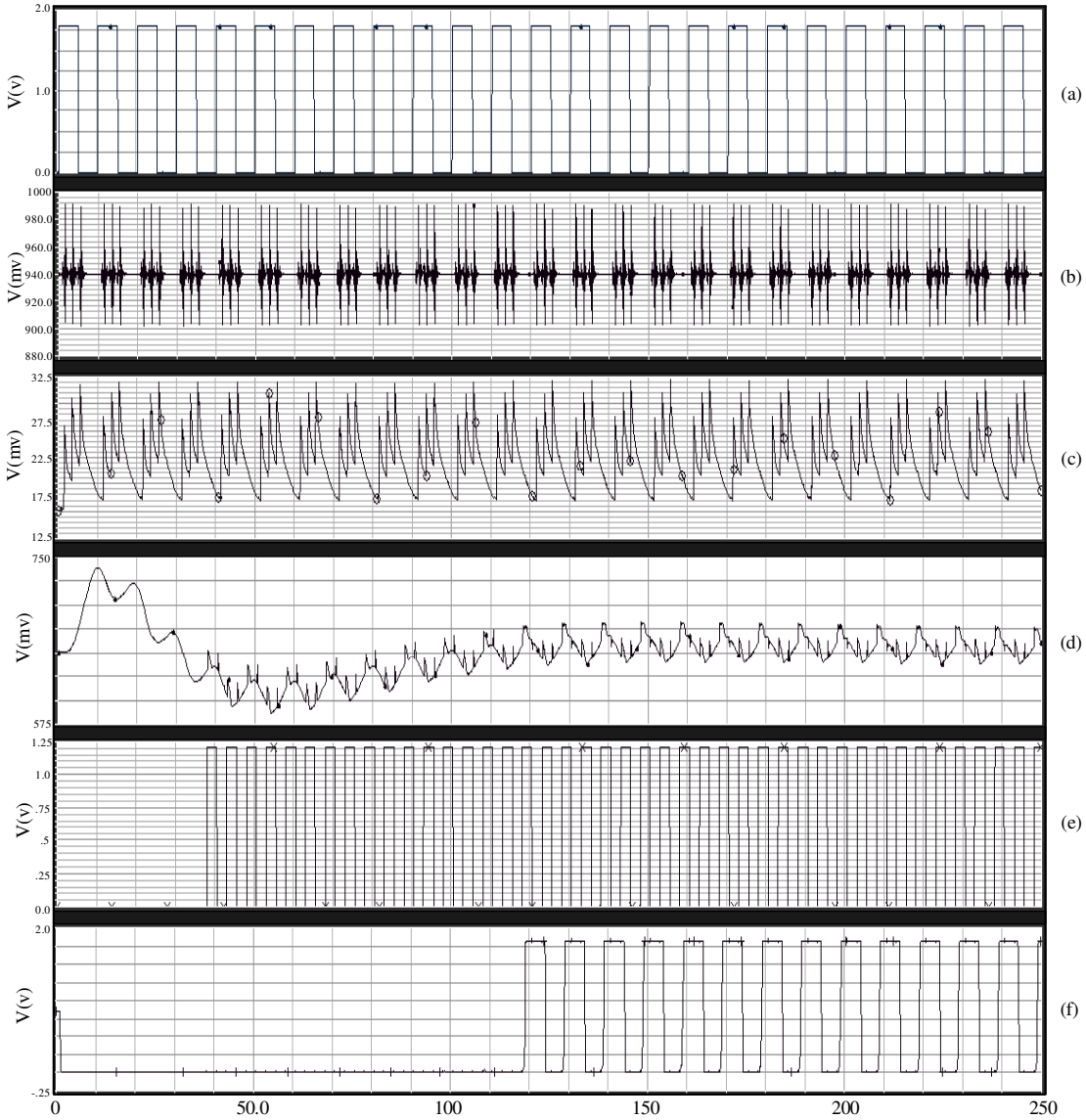


Figure 5.7 Post-layout simulation: (a) input data, (b) pulse sequence at the input of receiver, (c) waveform after the correlator, (d) waveform after the integrator, (e) the comparator clock, (f) reconstructed signal

5.3 Power Analysis

Power consumption is an important index for the performance of the battery-powered devices. Battery lifetime is critical factor in the design of the wearable UWB wireless transceiver. While determining the battery running life of the transceiver, several battery

parameters are considered: battery capacity in mAh, and battery voltage in V [44]. When a battery discharges to a load, the battery voltage drops from the initial supply voltage to a cut-off voltage, where the battery no longer operates. The battery operating time is defined as the time the battery takes from the initial voltage to the cut-off voltage. For example, one commercially available Duracell Lithium 1.8V AAA battery has a standard capacity of 1100mAh. This type of battery is used for estimating the battery lifetime for the wearable sensor node as shown in Figure 5.8. In this battery lifetime estimation, the Control and DSP unit is excluded as it consumes very little power compared with the wireless transceiver circuit.

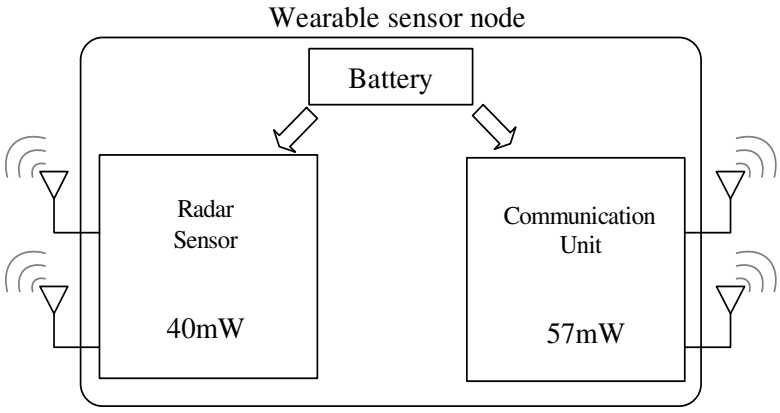


Figure 5.8 The battery lifetime estimation

In this design, the maximum overall average power consumption is 40mW for the UWB radar sensing and 57mW for the UWB communications. The radar sensing transceiver current drain is 22.2mA and the UWB transceiver for communications consumes a current of 31.7mA. Assuming two transceivers, supplied by one Lithium 1.8V AAA battery, are operating at the same time, a total current of 53.9mA is consumed. The battery lifetime of this single Lithium 1.8V AAA battery for simultaneous operation of two transceivers is estimated in Equation 5.2 below.

$$\text{Battery lifetime} = \frac{Capacity}{Current} = \frac{1100mAh}{53.9mA} = 20.41 \text{ hours} \qquad (5.2)$$

This estimation is based on the assumption that the pulses are sent out uninterruptedly during the lifetime of the battery. In a real application, at least 95% of the time the transceivers are in an idling status and consume very little power. In this case, the battery

lifetime for a single Lithium 1.8V AAA battery is 408.2 hours, or 17 days. Adding another AAA battery doubles the battery lifetime.

The power consumption of the transceivers can be greatly reduced by slowing down the transmission speed. Current radar sensing unit sends out pulses in every 150ns. This frequency is much higher than the heart moving rate. Sending the pulses in every micro second would achieve the heart motion detection performance while consuming lower power. The UWB communication unit also has a large room to reduce the data transmission speed to save power. The current data rate of 200Mbps is way beyond the need for communications between the wireless sensor node and the base station. The sensor node only needs to send and receive a small amount of data to and from the base station at a time. Thus, a data transmission rate of few mega bytes per second, or even few hundred thousand bytes per second would satisfy the communication requirement, and greatly reduce the overall power consumption and increase the battery lifetime.

Chapter 6 Conclusions and Future Exploration

6.1 Conclusions

In this project, a fully integrated, non-coherent CMOS wireless UWB transceiver for the 3.1GHz-10.6GHz IR-UWB medical sensor was developed. The transmitter uses the OOK modulation scheme to transmit extremely short Gaussian pulse signals. In the OOK modulation scheme, five pulses are used to represent one data bit. The amplitude of the output pulse can be adjusted within the range from 6mV to 75mV by the shunt-peaking driver amplifier with inductance degeneration for different level of power emitting to fit particular application. In the receiver, the LNA using cascade inductor peaking and inductance degeneration topology provides a power gain of 7 dB and a good impedance matching from 2GHz to 11.2GHz. The signal achieves a good SNR after multiplication by the signal correlator and integration by the charge integrator. A series of amplifier buffer is followed to provide further voltage gain. A sense amplifier is employed in the voltage comparator, which is the last stage in the UWB receiver. The sense amplifier compares the signal waveform with the reference voltage set presumably, and outputs digital level data bit.

The integrated UWB transceiver occupies a core area of $0.752\,mm^2$ and the total die area of $1.274\,mm^2$ when the pad ring is taken into account. The transceiver was simulated with overall power consumption of 40mW for radar sensing. The receiver sensitivity is -73.01dBm. The average power of a single pulse is 9.8μW. The sensing resolution and the target positioning precision are presumably sufficient for heart movement detection

purpose in medical applications. This transceiver can also be used for high speed wireless data communications after minor setup modifications. The transceiver for this purpose was simulated. The data transmission rate of 200 Mbps was achieved with overall power consumption of 57mW. A combination of sensing and communications can be used to build a low power sensor, as proposed in Chapter 1. The goals of this thesis project are accomplished. The remained works and further improvements of the design will be introduced in the next section.

The transceiver simulation results can be used to compare with other recent works in UWB wireless transceivers as shown in Table 6-1. Each design has different circuit implementation. In [32], the UWB transmitter achieves a transmission rate of 1.4G bps (receiver rate unknown). The overall average power consumption is 79mW. The transceiver does include a gain-adjustable amplifier and occupies a chip area of $0.4\,mm^2$. In [28], the OOK-modulated transceiver achieves a maximum transmission rate of 50M and a sensitivity of -72dBm. The transceiver consumes an average power of 41.4mW and occupies a total die area of $4.672\,mm^2$.

Table 6-1 Performance comparison with recent UWB Transceiver

Parameter	2005[32]	2005[28]	2007[16]	This design
Type	UWB Comm.	UWB Comm.	UWB Comm.	Radar sensing & UWB comm.
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Modulation	OOK	OOK	OOK	OOK
Frequency (GHz)	3.1 - 5	3.1 - 5	3 - 5	3.1 – 10.6
Sensitivity (dBm)	N/A	-72	-70	-73.01
Tx Rate (bps)	1.4G at Transmitter	50M	100M (Max. 200M)	200M
Avg. Power consump-tion (mW)	79	41.4	N/A	57
Core chip size (mm^2)	0.4	N/A	1.3	0.752
Total Die Area (mm^2)	N/A	4.672	N/A	1.274

In [16], the UWB transceiver employing the OOK modulation scheme achieves a sensitivity of -70dBm and a maximum pulse rate of 200M bps. However, the transceiver does not include an A/D device that converts the received waveform into digital signals. The transceiver die area is $1.3\,mm^2$ excluding the pad ring. In the design in this thesis, the transceiver is a digital-input digital-output transceiver specifically designed for both radar sensing and communication purposes. The transceiver signal occupies the frequency bandwidth of 3.1GHz to 10.6GHz. The transceiver achieves a very low sensitivity and high data rate with a moderate power consumption.

6.2 Future Exploration

The implementation of the proposed UWB sensor for heart motion detection remains for future work. The UWB wireless transceiver design will be sent to TSMC foundry for chip fabrication. The chip will be tested in the later stage. A more accurate transmission and scattering model based on different lumped components for UWB signal through different human organic tissues with various dielectric properties will be developed and analyzed. Another area that needs a fair amount of future work is the design and implementation of the UWB antenna model for transmitting and receiving UWB pulses. Current researches on UWB antennas suggest a few types of UWB antennas that are suitable for the sensor. The power budget will be computed to assess the feasibility of each option. In the next stage, the antennas of the transceiver will be built and tested based on those existing UWB antenna designs. The antennas will be integrated on the transceiver circuit chip to minimize space. Also, the transceiver will be integrated with the DSP and control units for overall sensor performance testing and evaluation.

The design of the UWB transceiver can be modified in several ways to improve the performances. The current design is based on the assumption that the system will only experience the white Gaussian noise with a constant noise level. However, in a more complicated application environment such that the noise may come from other radio systems nearby, the OOK modulation scheme could experience a difficult time to

distinguish between a received pulse and a burst of noise. In this case, the receiver's bit error rate can be greatly reduced by employing biphase modulation scheme at a cost of increased circuit complexity and die area, which are sometimes not a first priority in analog integrated circuit design.

Future work on the design can also be expanded to the redesigning of the integrated inductors using multi-layer stacked structure to largely reduce the die area and winding loss. As analyzed by ASITIC, this inductor structure, however, has higher parasitic capacitance as it lies closer to the substrate and higher inter-winding capacitance which lowers the frequency of self-resonance. This is a trade-off between area and speed. But there is no absolute right or wrong in this type of issues, as designing of analog circuit is all about making decisions between all kinds of trade-offs.

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