PROGRAMMED SPEECH OUTPUT SYSTEM FOR THE HANDICAPPED

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"PROGRAMMED SPEECH OUTPUT SYSTEM

FOR THE HANDICAPPED"

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ABSTRACT

This thesis describes the design criteria and the resulting construction of an audio output communication device for the physically handicapped. The operator is able to select, via his particular input transducer, one from a possible 400 pre-recorded words and have it appear as a "spoken" word of audio. Also included in this thesis are proposals for further study which would reduce the size, cost, and weight of the unit as well as offer greater flexibility in output format and a much larger vocabulary.

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TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	iv
ABSTRACT	iii
TABLE OF CONTENTS	v
LIST OF FIGURES	vii
1. INTRODUCTION	1
2. GENERAL DESCRIPTION OF PROPOSED SYSTEM	7
2.1 Input Transducers	7
2.2 Principle of Operation	11
3. PROTOTYPE VOCABULARY TAPE DECK	13
3.1 Design Requirements and Resultant Prototype	13
4. IMPROVED VOCABULARY TAPE DECK	18
4.1 Description of Improved Vocabulary Tape Deck	18
4.2 Operation of Improved Vocabulary Tape Deck	21
4.2.1 Tape positioning	21
4.2.2 Head positioning	22
5. DETAILED OPERATION OF CONTROL LOGIC	24
5.1 Tape Drive	24
5.2 Head Drive	28
5.3 General Discussion	29
6. LOGIC ELECTRONICS CIRCUITRY	31
6.1 Vertical Buffer and Vertical OR	31
6.2 Decimal to Binary Converter and Inverter	34
6.3 Coincidence Detector and Binary Counter	38
6.4 Enable AND	40
6.5 Horizontal and Level Buffers and OR	43
6.6 Step Motor Drive and Buffer Shifting Logic	45

TABLE OF CONTENTS (cont'd)

		Page
	6.7 Shift and Reset Driver	48
	6.8 Selector Gate	48
	6.9 Head State and Reset Flip-Flop	51
	6.10 Step Motor Drive and Clutch Drive	51
	6.11 Summary of Operation	53
7.	CONCLUSIONS	54
	7.1 View of System Performance	54
	7.2 Proposals for Further Study	55
8.	REFERENCES	58
9.	APPENDICES	60
	A. Prototype Logic Electronics	60
	B. Audio Electronics	84
	C. Photographs of System	87

LIST OF FIGURES

Figure		Page
1.	Word board input format	10
2.	General block diagram of system	10
3.	Prototype vocabulary tape deck	14
4.	Improved tape deck	19
5.	Block diagram of control logic	25
6.	Physical layout of integrated circuit logic'	32
7.	Vertical buffer	33
8.	Vertical OR	35
9(a)	Decimal to binary converter	36
9(b)	Inverter for decimal to binary converter	37
10.	Coincidence detector	39
11.	Binary counter	41
12.	Enable AND	42
13.	Horizontal and level buffers and OR	44
14.	Step motor drive and buffer shifting logic	46
15.	Shift and reset driver	49
16.	Selector gate	50
17.	Head state and reset flip-flop	50
18.	Step motor drivers	52
19.	Block diagram of prototype logic	61
20.	Input buffer bistable multivibrator	62
21.	Horizontal and level selection	64
22.	Level and horizontal relay drivers	65
23.	Horizontal and level OR gate	67
24.	Decimal to binary converter	68
25(a)	Count and reset schmitt trigger circuit diagram	69
25(b)	Reset pulse amplifier	69
26.	Block diagram of coincidence Detector	72
27.	Coincidence detector	73
28.	Enable AND gate	76
29.	Clutch pulse gate	78
30.	Clutch flip-flop and clutch enable gate	80
31.	Buffer reset pulse amplifier	83
32.	Record electronics circuitry	85
33.	Playback electronics circuitry	86
34.	Word board input transducer	88
35.	Prototype tape deck	88
36.	Prototype logic electronics	89
37.	Complete prototype system	89
38.	Top view of improved tape deck	90
39.	Front view of improved tape deck	90
40.	Integrated circuit logic electronics	91
41.	Audio electronics	91

1. INTRODUCTION

In many cases, people who suffer from a communication deficiency are fully aware of their environment and are able to understand messages directed to them. This deficiency is often due to motor incoordination as a result of brain damage and frequently manifests itself in varying degrees of ataxic aphasia and paralysis or spasticity of the limbs. As a result, in the more severe cases, communication is slow, inefficient and frustrating. Medical treatment can occasionally reduce the severity of the handicap but can rarely remove it completely. Consequently, at present, if these disabled are to have the ability to "speak", devices must be constructed that will allow the operator to communicate by utilizing voluntary actions over which he has reasonably good control.

In the most general case, an artificial communication device should possess the characteristics listed as follows. All of these requirements are intended to describe a system which would most closely approach the properties of natural communication techniques.

(a) Input adaptable to the operator's particular skill.

(b) Information transfer rate limited by the operator's speed.

(c) A large enough vocabulary to satisfy the operator's requirements. Provisions should be made to allow rapid and easy changing of part or all of the vocabulary.

(d) Output to appear in convenient form.

(e) Small size, light weight and quiet operation.

(f) Inexpensive.

There have been a few systems[1-5] constructed in an attempt to alleviate the communication difficulties of the handicapped. All of these were based on the controlled illumination of a display board or the operation of an electric typewriter - none have attempted to provide an artificial audio voice. It is the purpose of this thesis to investigate the feasibility of and propose a system to provide audio communication for the handicapped.

The success in controlling an artificial voice for communication will depend heavily on the limitations of the memory in which is stored the working vocabulary. The memory is by far the most critical and probably the most expensive element of the system and therefore should be selected or designed with utmost care.

The Radio Corporation of America[6] has done considerable work in the fields of analysis and synthesis of speech and

music. The memory in their speech synthesis device consists of a drum recording of 2000 syllables and a digital memory which stores information dictating what syllables are to be used and their order of occurrence. RCA quotes that 2000 syllables allows the reproduction of 98% of the words in the English language. This study was made by Dewey on what he considered to be a reasonable cross section of 100,000 words.

For the application under consideration, a device of this nature has several serious shortcomings. Either the two memories must have very fast access times or there must be a third memory in which the words are constructed in order that the output possesses the syllable to syllable continuity of natural speech. The switching requirements for rapid random access of 2000 syllables will also obviously be large and costly.

A similar system developed by IBM[7] is the IBM 7770 Audio Response Unit (ARU). The 7770 ARU was designed for a telephone intercept system where routine-reply intercepts can easily be handled by a computer. It has a vocabulary of 128 words, phrases, or syllables which are magnetically recorded on a drum. The ARU can supply 48 different messages simultaneously under the direction of computer control.

A second IBM system is the voice output for the IBM System 360. This ARU is the IBM 7772. In this unit, the audio is generated by appropriately energizing 15 tone

filters and combining the outputs to form words. In addition to the 7772, one requires approximately 2400 binary bits of information storage capacity for 1 second of speech. The binary bits are stored external to the 7772 which only generates speech in response to binary data excitation.

A commercial device which most closely approaches the requirements of a communication system is called the Edison Responsive Environment. The audio communication memory portion of the Edison Responsive Environment is a cylinder about 1 inch in diameter and 8 inches long. This cylinder is surfaced with a magnetic recording medium and offers about 125 prerecorded tracks with one word per track. The required track is selected by moving one head under the control of a feedback analogue control system to the appropriate track. It was determined that this audio memory unit was commercially unavailable, and an attempt at obtaining a more detailed description of the system met with little success. The complete unit is, however, a teaching machine worth several thousand dollars and has a number of capabilities not required by a device intended solely for audio-communication.

In conclusion, the existing systems are generally characterized by high cost, large size, and a high degree of complexity due to the nature of their very specialized applications. In addition to this, an artificial voice for communication purposes can tolerate the absence of a great

deal of the sophistication possessed by most of the available systems.

In view of the fact that there could not be found a commercial analogue memory compatible with the specifications outlined in the sub-section on design criteria, it was proposed to construct a memory and its associated electronics to suit the requirements.

The Programmed Speech Output System for the Handicapped is designed to deal with the condition of ataxic aphasia. More precisely, the system is designed for aphasics who are also incapable of satisfactory communication in any natural form due to poor definitive control and muscular co-ordination.

The following list enumerates the design criteria finally settled upon for the Programmed Speech Output System for the Handicapped.

(a) Input circuitry flexible enough to handle a variety of input methods.

(b) Output to take form of the spoken word. In this system, ultimately, the operator should have the option of speaking only one word or being able to construct whole sentences.

(c) An access time of 1 second. An average access time of 1 second should be suitable and sufficiently short for most applications.

(d) The device should be conveniently wheel chair portable.

(e) The vocabulary should be at least a few hundred words. It was decided that 400 words would yield a rather minimal but reasonably good working vocabulary.

In its proposed form one could not completely justify the use of the system for someone with a relatively normal ability to write. However, if the system was refined sufficiently to allow a much larger vocabulary, a rapid and convenient input transducer, and small size, the unit would then more nearly approach natural audio communication which would be sufficient justification for its use in the case of a limited ability to communicate.

2. GENERAL DESCRIPTION OF PROPOSED SYSTEM

It is the purpose of this chapter to describe, in very general terms, the principle of operation of the Programmed Speech Output System. This account is, however, preceded by a section concerned with man-machine interface considerations with the hope that this will lead to a more complete understanding of the situation. Even though the philosophy and design of interfaces is of paramount importance, it is not dealt with in detail here.

2.1 Input Transducers

The most important and most difficult aspect concerning the successful utilization of a communication device of this nature is the operator-machine interface.

The general design philosophy for a transducer to cope with this problem can be summarized quite briefly. In order that the rate of information transfer be as fast as possible, an input device must be constructed which allows the largest number of parallel input channels consistent with the operator's abilities. Another important consideration is physical strength. Many disabilities render the individual incapable of exerting a force of more than a few ounces on

the input transducer and therefore much care should be exercised in selecting a suitable sensor. Frequently poor definitive control is accompanied by poor temporal control and therefore input devices for this condition should avoid timing requirements on the operator's part.

In general it is usually required that the transducer be custom built for anyone with spastic or paralyzed limbs; however, standardization may be possible where individuals can execute a similar degree of control over the same parts of their anatomy. The problems associated with input transducers most certainly warrant further investigation and research since they will ultimately limit the system's speed and usable vocabulary size.

There has been some work[5] done at the University of Saskatchewan on transducer design; however, the results were in some aspects crude and inadequate. Three types of transducers were investigated. The first was a switch fastened to the forehead and activated by raising the eyebrows. The operation of this device was hampered by operator fatigue and unintentional brow motions. The second device studied was a foot switch that took the form of a shoe-shaped trolley confined in motion by rails and stop blocks. This trolley was capable of motion forwards and backwards as well as pitching about an axis through the instep. For the cerebral palsy athetoids who first used the device, it met with reason-

able success; however, the information transfer rate was quite slow.

The most successful input transducer investigated was the "word board" input. The diagram of Figure 1 shows a word board with only three rows and three columns, whereas the actual board used contained ten rows and ten columns. Nevertheless, the essential features can be demonstrated with the board of Figure 1. Each square contains four dashed lines which correspond to the four words in that square. At the centre of each square is a circle. This represents a switch, a photo-cell or other sensor. To select a word, the sensor in the square encompassing the desired word is actuated and one of the four possible level sensors is actuated in order to uniquely define one of the four possible words in the square selected.

This type of input transducer is being used most often in the investigations of communication systems at the University of Saskatchewan. The Physical Rehabilitation Centre in Saskatoon has been very co-operative in allowing tests to be carried out on cerebral palsied children who are accustomed to this type of input. The author recommends Reference 5 if a more complete discussion of input transducer philosophy and design is desired.

Even though the word board type input is used in the system to be described, an attempt was made to make the input

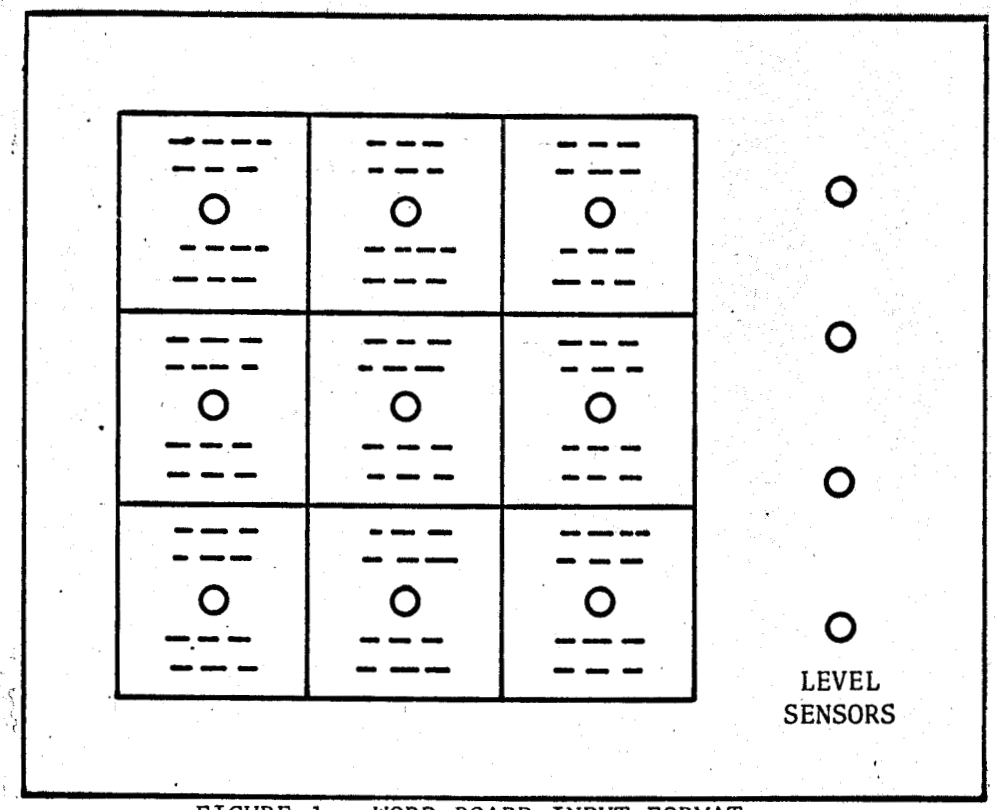

FIGURE 1: WORD BOARD INPUT FORMAT
The dashed lines indicate words of vocabulary.

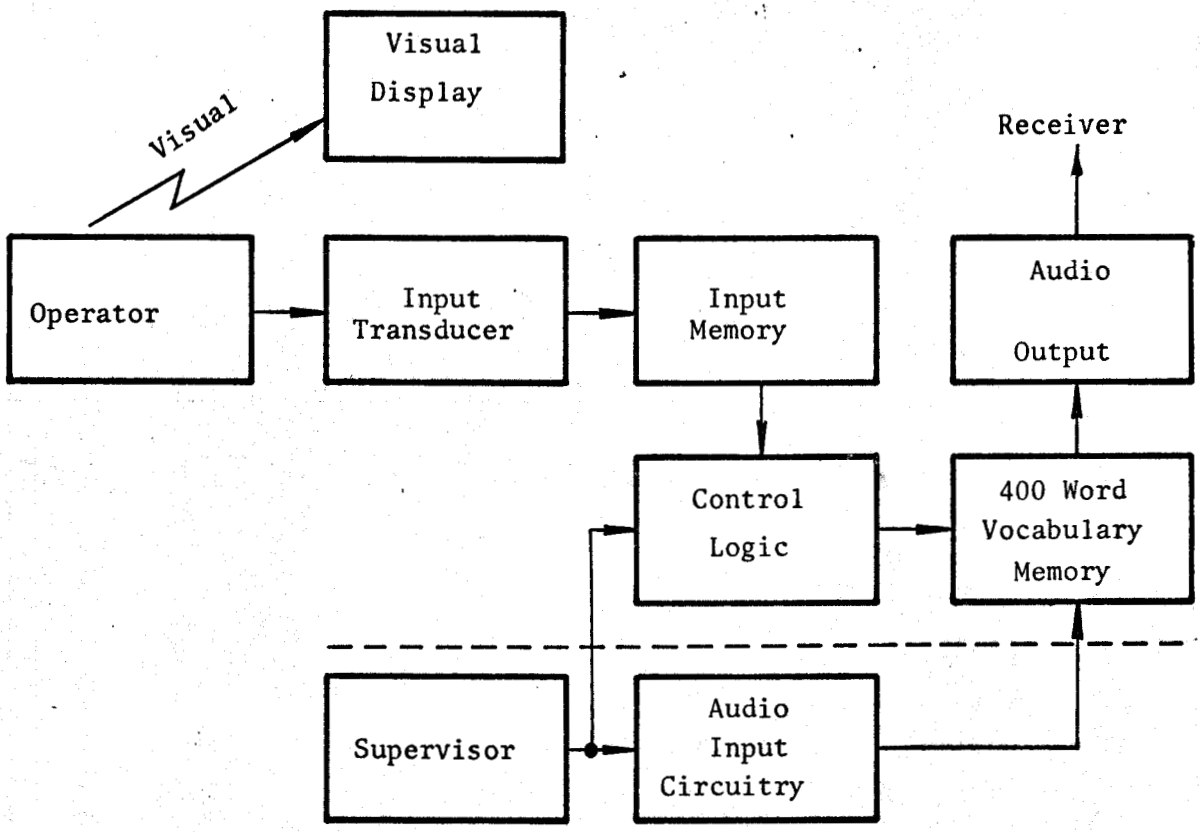

FIGURE 2: GENERAL BLOCK DIAGRAM OF SYSTEM

circuitry sufficiently flexible in order to handle a variety of input modes.

2.2 Principle of Operation

The fundamental ideas concerning the system's operation will now be explained with the aid of Figure 2.

The system is basically a sophisticated tape recorder - the 400 WORD VOCABULARY MEMORY - under the supervision of suitable logic circuitry - CONTROL LOGIC.

Before the system can be used as an aid to communication, the 400 WORD VOCABULARY MEMORY must contain information useful to the OPERATOR. The SUPERVISOR's purpose in this system is to programme the memory with the required words and prepare a VISUAL DISPLAY indicating the words in memory and their locations. During the course of operation, the SUPERVISOR may also be required to change, a portion of, or, all of the memory. The SUPERVISOR can therefore take command of the CONTROL LOGIC and the INPUT CIRCUITRY for programming purposes.

Once programmed, the system is ready to serve the OPERATOR. In order to "speak" a word of audio, the OPERATOR consults his VISUAL DISPLAY to determine the word's location in memory. He then activates the required input sensor(s) on the INPUT TRANSDUCER and the message is delivered to the RECEIVER about 1 second later.

It is necessary to have an INPUT MEMORY to buffer the system and thus permit a large number of different transducers to be used. It will also eliminate some of the input ambiguity due to poorly executed actions on the operator's part.

The AUDIO INPUT and AUDIO OUTPUT circuits are conventional tape recorder record/playback amplifiers, respectively. They are gleaned from Reference 8 and modified slightly. Circuit diagrams for these are shown in Appendix B.

3. PROTOTYPE VOCABULARY TAPE DECK

The main memory or the vocabulary tape deck is the heart of the Programmed Speech Output System. Most of the overall system requirements outlined in Chapter 1 will ultimately be a function of the tape deck parameters. This section of the text will describe the prototype tape deck's design, as well as discussing the results of tests which demonstrate the feasibility of meeting the design requirements. The overall operation of the prototype will be outlined along with some of the problems associated with its operation. For an understanding of the physical construction of the tape deck, reference should be made to Figure 3 throughout this chapter.

3.1 Design Requirements and Resultant Prototype

In order to realize an access time of about 1 second, it was decided to drive the tape at a high scanning speed until the required location was reached, at which time the tape would be slowed to its playback speed. This two-speed drive was to be achieved by engaging either the high speed synchronous motor and its friction wheel reduction system or the low speed synchronous motor and its associated friction

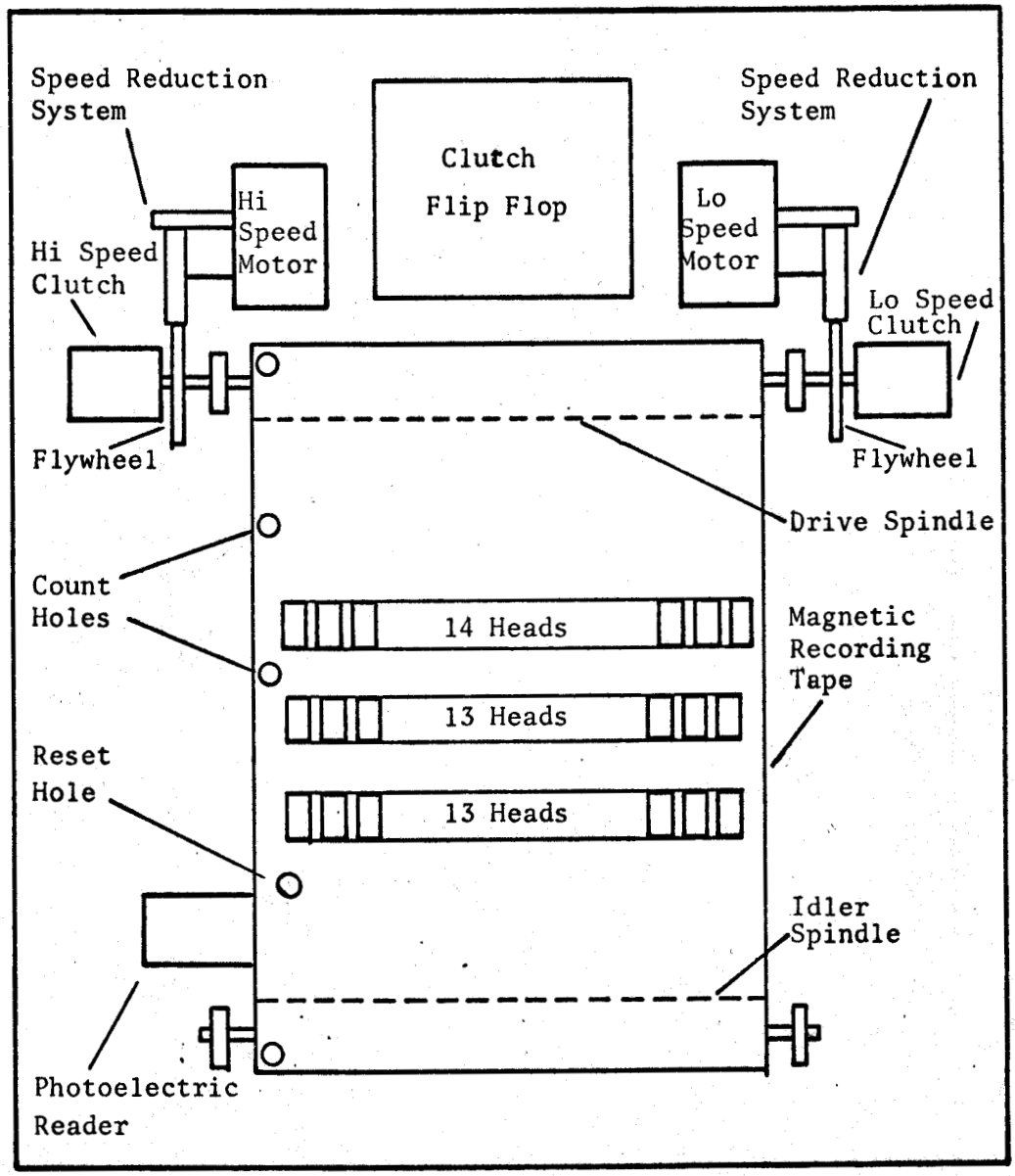

FIGURE 3: PROTOTYPE VOCABULARY TAPE DECK

wheel reduction system to the drive spindle via magnetic clutches.

Pulses derived from the COUNT and RESET holes in the edge of the tape - via the photo-electric reader - keep the LOGIC ELECTRONICS "informed" of the tape's position. On the basis of this address information, the state of the magnetic clutches can be established to suit the requirements of that particular instant.

This type of tape drive caused small speed variations due to intermittent fluctuations in mechanical loading and irregularities in the friction wheel reduction system.

This problem was overcome by using a belt-pulley reduction system driving masses with large moments of rotational inertia.

In order that the tape be as small as possible, the playback speed must be selected to be as low as possible. Tests were performed using an inexpensive record/playback head - of the type proposed for the prototype - on a conventional tape recorder. It was found that a tape speed of 1.5 inches/second yielded good results. The high speed scan was then established at 15 inches/second so as to achieve a maximum access time of 1 second. The 400 words of vocabulary were to be recorded on 40 tracks at 10 words/track, with each word standardized to occupy a maximum of 1 second of tape when operating at the playback speed. Due to the very low

price of the heads - about one dollar each - it was decided to use 40 heads with the hope of keeping the mechanical complexity of the system to a minimum. The heads were arranged in three rows as depicted by Figure 3. Initially pressure pads were not used. The tape was simply drawn taut over the heads' surface.

It was found very difficult to maintain an intimate head to tape contact since the 13 or 14 heads in a row could not be aligned in the horizontal plane with sufficient accuracy. Consequently, the quality of audio output deteriorated. The inclusion of small pressure pads improved the audio response but on occasion increased the drag to the point of stopping the tape. This occurred especially when the splice was passing over the heads.

In addition to this, the bulky inflexible nature of the splice caused rapid loading and as a result speed changes when it passed over the spindles since it would not conform exactly to the curved face of the spindles. Even though the spindle size was increased, there were still minor speed fluctuations.

The combined effects of the above problems led to speed fluctuations and a reduction in the frequency response. This resulted in a generally unacceptable fidelity of audio reproduction. Even though the quality of reproduction was low, the prototype tape deck did indicate that a vocabulary

of 400 words could be randomly selected in an average access time of 1/2 second per word. The improved vocabulary tape deck, which overcomes the deficiencies of the prototype, is described in Chapter 4.

4. IMPROVED VOCABULARY TAPE DECK

Because of the problems outlined in Chapter 3 concerning the PROTOTYPE TAPE DECK, it was proposed to construct an improved model which overcame these. the IMPROVED VOCABULARY TAPE DECK, shown in Figure 4, not only surmounted the difficulties of the prototype but also realized some additional desirable features.

4.1 Description of Improved Vocabulary Tape Deck

Most of the difficulties associated with the prototype's operation were due to the large number (40) of record/playback heads required. In order to overcome this, a single record/playback head, affixed to a type of carriage is driven by means of an incremental stepping motor and lead screw assembly. One head can then "read" all locations on tape without causing excessive drag. An additional benefit results from the use of only one head. The requirement for bulky and expensive head selection circuitry no longer exists. With this technique it is also economical to use a more expensive type of head having a smaller track width thus increasing the information density across the tape and consequently reducing the tape width.

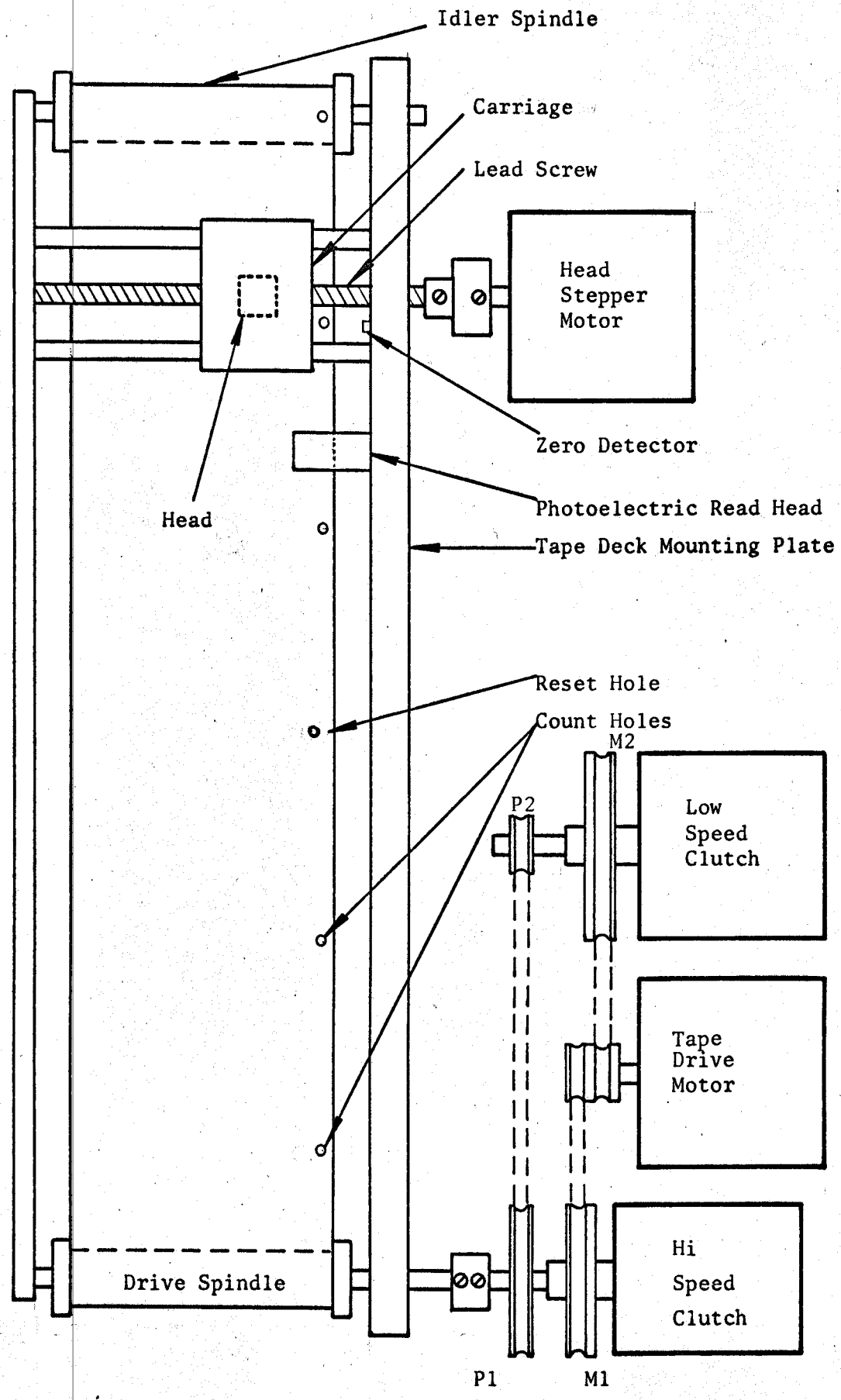

FIGURE 4: IMPROVED TAPE DECK

With the miniature type of head used, having a track width of .024 inches, 40 tracks can easily be put on a 2 inch wide tape. With such a narrow tape, the DRIVE and IDLER spindles could be cantilevered to facilitate easy tape changing - a process in the prototype which required complete dismantling of the tape deck.

The clutch type drive scheme was maintained. However, a different physical layout was incorporated to allow the tape to be driven from one side of the drive spindle only. The two speeds were kept at 15 inches/second for scanning and 1.5 inches/second for recording and playing back.

During the construction of the IMPROVED VOCABULARY TAPE DECK, the author was informed of a company that specialized in the ultrasonic welding of mylar belts. Some tape samples were sent to this company for welding evaluation. On return of the samples, it was found that their resultant weld was only 0.050 inches in length and 20% thicker than the original tape sample. The company claimed that the yield strength of the weld is at least equal to that of the original material. This type of splice would fill the requirements precisely and it was decided to incorporate this into the new deck.

The IMPROVED VOCABULARY TAPE DECK, which embodied all the features just described, has performed very satisfactorily since completion.

4.2 Operation of Improved Vocabulary Tape Deck

The tape deck operation will be explained by describing positioning of the tape and positioning of the head, respectively.

4.2.1 Tape positioning

The tape drive motor continuously drives the two large masses M1 and M2 at an angular velocity of 600 RPM. From experience gained in the PROTOTYPE TAPE DECK, it was deemed advisable to maintain the rotational inertia of the drive to help damp out small speed variations.

Operation of the tape positioning mechanism is as follows. If the system is observed during a time between selections, both clutches will be disengaged and consequently the drive spindle will be at rest. Upon selection of a word, the high speed clutch will engage, effectively locking M1 to pulley P1. The drive spindle will then begin rotation at 600 RPM. Photoelectrically detected holes on the edge of the tape will eventually indicate to the logic electronics that the required position on tape has been reached. The logic electronics will then disengage the HI-speed clutch. Once the playback head has been properly positioned, the LOW-speed clutch will be engaged.

On engaging the low-speed clutch, M2 will be rigidly attached to P2 and will consequently drive it at 600 RPM.

However, since P2 is smaller in diameter than P1 to which it is coupled, P1 will then rotate at a slower speed - the playback speed. On completion of playback the low-speed clutch is disengaged and the drive spindle again comes to rest.

4.2.2 Head positioning

The carriage, on which the head is mounted, is driven across the surface of the tape by the lead screw. A track width of 0.025 inch and an intertrack spacing of 0.025 inch were selected. It is therefore required to have a 0.050 inch movement of the carriage to advance one track. With the 20 threads per inch lead screw used, one revolution per track is required. The lead screw is driven by a bidirectional D.C. stepper motor employing a permanent magnet armature surrounded by stator coils. Sequential energization of the coils by square waves of current results in a stepwise advancement of the resultant magnetic field within the motor. Interaction between this rotating field and the permanent magnet armature causes the armature to rotate in a stepwise fashion. The number of steps experienced per revolution depends on the physical arrangement and number of stator coils as well as the number of poles on the armature. The particular motor used has 16 steps per revolution.

Some logic electronics are required to insure that the stator coils are energized in the proper sequence. Integrated

circuits are used for this and the control of tape positioning. This aspect will be described when the integrated circuit logic of the system is dealt with in Chapter 6.

In order that the head can be positioned over the proper track, its initial position must be known. It is the purpose of the zero detector to perform this function. The zero detector is a conducting lug fastened to, but insulated from, the tape deck mounting plate. It makes electrical contact with the carriage when it returns after each selection. This electrical contact is used to reset the system in preparation for its next selection.

Upon receiving an input, the logic electronics supplies pulses to step the D.C. stepper motor a sufficient number of times to drive the head and carriage out to the required track. When audio output has been completed, the motor is stepped in the reverse direction until the zero detector makes contact with the carriage and resets the system.

Photographs of the prototype tape deck and the improved vocabulary tape deck are shown in the Appendix C.

5. DETAILED OPERATION OF CONTROL LOGIC

The functioning of the CONTROL LOGIC circuitry is now described using the block diagram presentation of Figure 5. This will not only illustrate the action of each section of the logic but will also demonstrate the important inter-relationships without resorting to detailed circuit analysis techniques.

The discussion to follow will be divided into two sections - positioning of the tape and positioning of the head. Let it be assumed that the system has been operating for some time and that it is presently in its normal quiescent state having just completed the selection of a word.

5.1 Tape Drive

The VERTICAL, HORIZONTAL and LEVEL buffers provide the INPUT MEMORY feature discussed in Chapter 2. While awaiting an input these buffers will be set to "0". During the following discussion a "1" will be interpreted as an output and a "0" as no output.

In its quiescent state, the tape drive motor will be operating, but as both clutches will be disengaged, the tape will not be in motion. This is necessary since the heads,

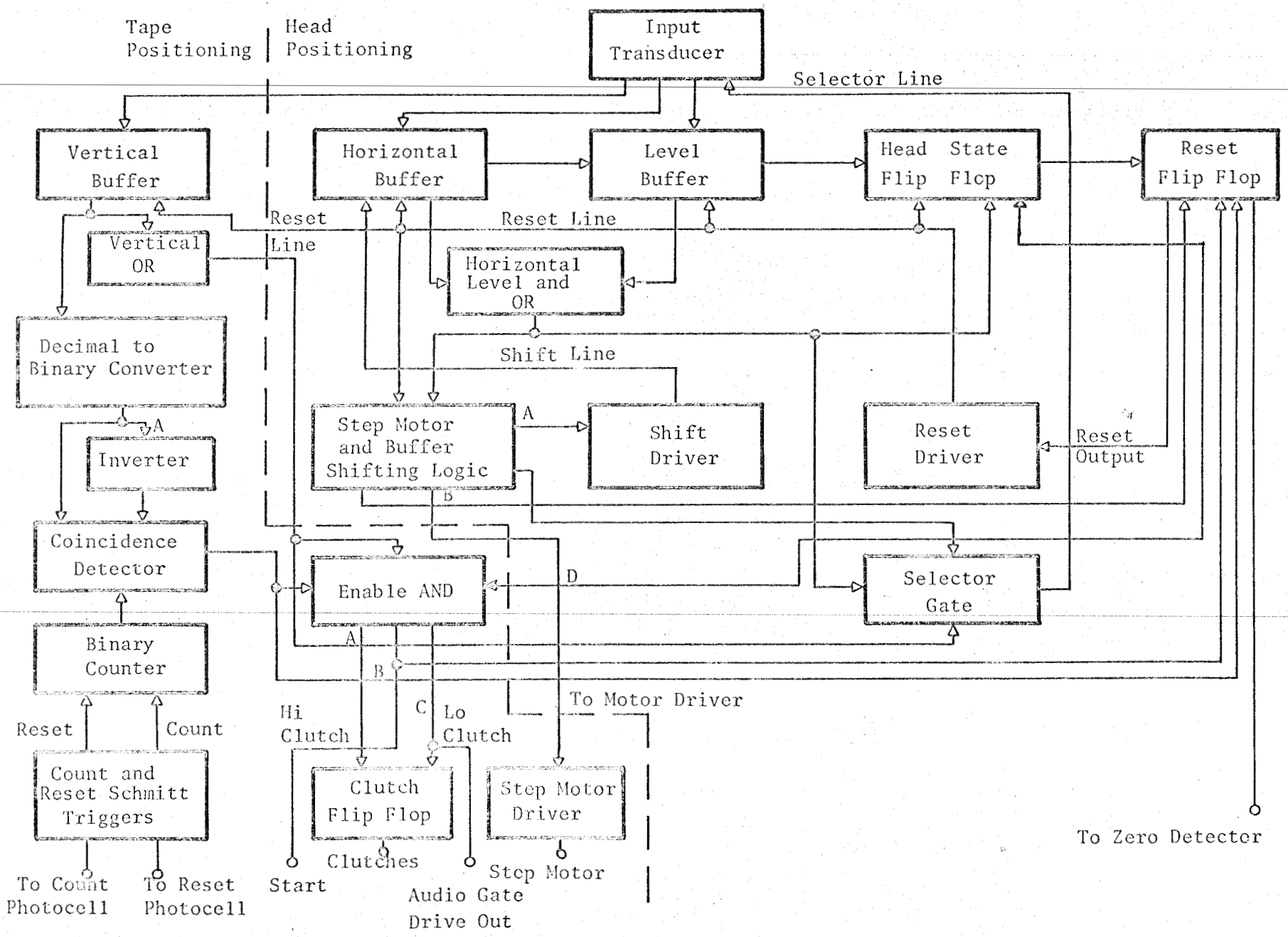

FIGURE 5: BLOCK DIAGRAM OF CONTROL LOGIC

under the condition of continuous tape rotation, would soon abrade the oxide coating from the mylar backing material and render the tape useless.

The BINARY COUNTER, in the TAPE POSITIONING portion of the diagram of Figure 5, will contain the address corresponding to the last hole that passed under the PHOTO-ELECTRIC READ HEAD and will therefore be precisely informed of the tape's present static position.

To initiate the selection process, 1 of the 10 VERTICAL BUFFERS is set to the "1's" state via the input transducer. Assume that the number 7 buffer is set. The output line of the number 7 buffer, which is connected to the DECIMAL TO BINARY CONVERTER, then rises to "1" offering 7_{10} to the DECIMAL TO BINARY CONVERTER. Output A of the converter now carries the binary equivalent of the decimal number applied at the input - in this case, the binary number 7. This binary number, in addition to being applied directly to the COINCIDENCE DETECTOR, is complemented by an INVERTER. This manoeuvre is necessary since the technique for detecting coincidence, the reason for which will be described presently, requires that both the original binary number and its complement be present.

The VERTICAL OR gate, which is coupled to the VERTICAL BUFFER, will generate an output whenever any one of the VERTICAL buffers is in the "1's" state. This output is applied

to the ENABLE AND gate where it causes the HI-SPEED CLUTCH to engage and thus drive the tape at high speed.

The BINARY COUNTER is now set in motion by pulses derived from the photo-electrically "read" holes in the edge of the tape. The RESET and COUNT SCHMITT TRIGGERS shape and amplify these pulses. There are 9 COUNT holes and 1 RESET hole. The RESET hole resets the counter to 1 and the 9 count holes advance the count sequentially to 10 when one count later it is again reset to 1.

Thus, if the tape was not sitting on vertical location 7 when the number 7 VERTICAL BUFFER was set, it would begin rotating at high speed.

Each time the count contained in the BINARY COUNTER is equal to the number at the output of the DECIMAL TO BINARY CONVERTER, the output of the COINCIDENCE DETECTOR rises to "1". This output of "1" is then applied to the ENABLE AND gate where it disables the HI-SPEED CLUTCH. In this case, tape rotation will continue until location 7 is reached at which time the tape will stop. Had the tape been at location 7 when the number 7 buffer was energized, none of the above operations would have taken place. The tape would have simply remained stationary since it was already at the proper location.

After HORIZONTAL and LEVEL inputs have been made and the HEAD is positioned over the required track, input line D of

the ENABLE AND gate will rise to 1. This will cause the LO-SPEED CLUTCH to engage and drive the tape at its low speed for recording or playing back. At the end of the word, the BINARY COUNTER will be advanced to 8 in the assumed case - destroying coincidence. The output of the COINCIDENCE DETECTOR at this time triggers the RESET FLIP FLOP which is responsible for returning the system to its resting state after a selection has been made. The system now awaits its next selection.

5.2 Head Drive

The 10 HORIZONTAL and 4 LEVEL buffers store input information concerning the required track. By energizing 1 HORIZONTAL and 1 LEVEL buffer, a unique definition of 1 from 40 tracks is possible.

The HORIZONTAL buffer is connected as a ring counter and the LEVEL buffer is a conventional shift register. LEVEL shifting is accomplished from the last stage (10) of the Horizontal Buffer.

Suppose now that 1 HORIZONTAL and 1 LEVEL buffer have been set by the INPUT TRANSDUCER. The output of the HORIZONTAL and LEVEL OR gate will rise to "1" and start the STEP MOTOR AND BUFFER SHIFTING LOGIC. Pulses derived from here on line A will be amplified by the SHIFT DRIVER and used to shift the HORIZONTAL BUFFER. Pulses on line B will drive the STEP MOTOR which moves the HEAD from its ZERO position

across the tape. When the bit originally loaded into the LEVEL BUFFER is shifted into the HEAD STATE FLIP FLOP, the STEP MOTOR AND BUFFER SHIFTING LOGIC is disabled and the HEAD stops over the required track. At this time the tape plays back the required word.

At the termination of playback, anticoincidence triggers the RESET FLIP FLOP. It then, via the RESET DRIVER, resets all input buffers and commences the reverse driving of the STEP MOTOR. When the HEAD returns to zero, the ZERO DETECTOR switch clears the RESET FLIP FLOP and the system awaits another input.

5.3 General Discussion

The SELECTOR GATE is so connected that it keeps the INPUT TRANSDUCER disabled during the selection of a word. This precludes the possibility of the INPUT TRANSDUCER's causing an error during the selection operation.

It was assumed, in the description of operation, that the system had been in service for some time. When the unit is first "turned on", certain unpredictable states could be present. The START line of Figure 5 is used to overcome this difficulty. This line is taken to ground for about 1 second after "turn on" allowing the BINARY COUNTER to register itself and forcing all the input buffers to reset. The system is then ready for operation.

Line C from the ENABLE AND gate, the LO-SPEED CLUTCH line or the AUDIO GATE DRIVE OUT line, is used to close a reed relay which connects the record/playback head to the AUDIO ELECTRONICS for the purpose of recording or playing back.

In summary, the entire operation is as follows. The INPUT TRANSDUCER loads one bit of information into each of the input buffers. When the tape and the head have been properly positioned, the AUDIO GATE DRIVE OUT line rises to "1" enabling the audio electronics for one word length on tape. At the termination of selection, the system is reset and awaits further inputs.

6. LOGIC ELECTRONICS CIRCUITRY

A discrete component version of the logic electronics was constructed concurrently with the prototype tape deck. This circuitry worked very well; however, proposals for further study indicated that great savings in system size and cost could be achieved by adopting integrated circuits. This chapter will describe the integrated circuit logic which is nearly identical in operation to the prototype electronics. Appendix A contains circuit diagrams for and descriptions of the prototype circuitry.

Figure 6 shows the physical layout of the integrated circuits used. It is intended that Figures 5 and 6 be considered together in this chapter to facilitate the analysis. The system operation will be explained in terms of the functional groups shown in Figure 6. With one exception, all of the integrated circuits shown are Texas Instrument series SN7400N circuits. The head stepper motor oscillator is a Motorola MC724P gate.

6.1 Vertical Buffer and Vertical OR

Figure 7 shows the detailed diagram for the VERTICAL BUFFER. It is composed of five SN7474N dual type D flip-flops.

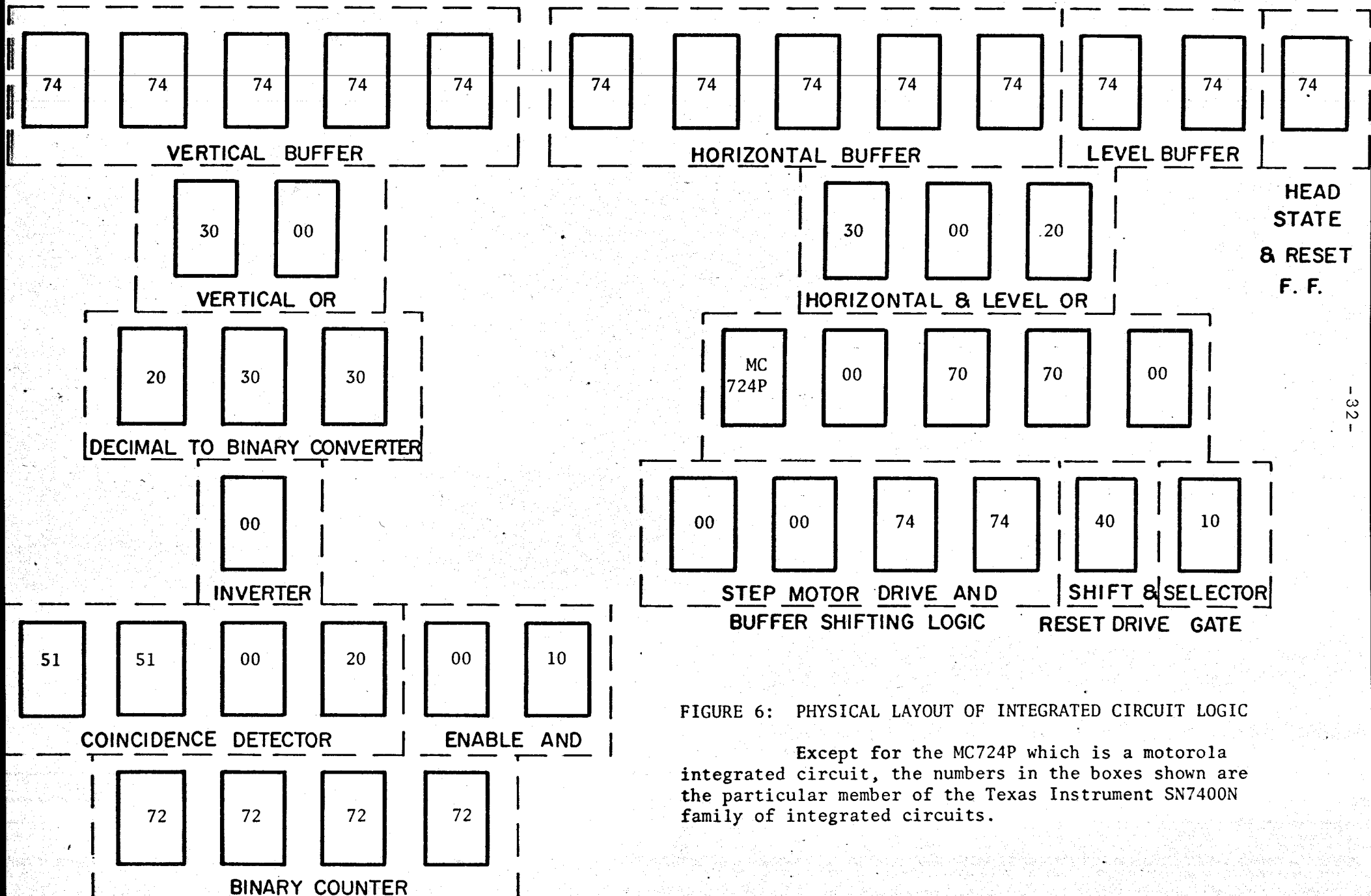

FIGURE 6: PHYSICAL LAYOUT OF INTEGRATED CIRCUIT LOGIC

Except for the MC724P which is a motorola integrated circuit, the numbers in the boxes shown are the particular member of the Texas Instrument SN7400N family of integrated circuits.

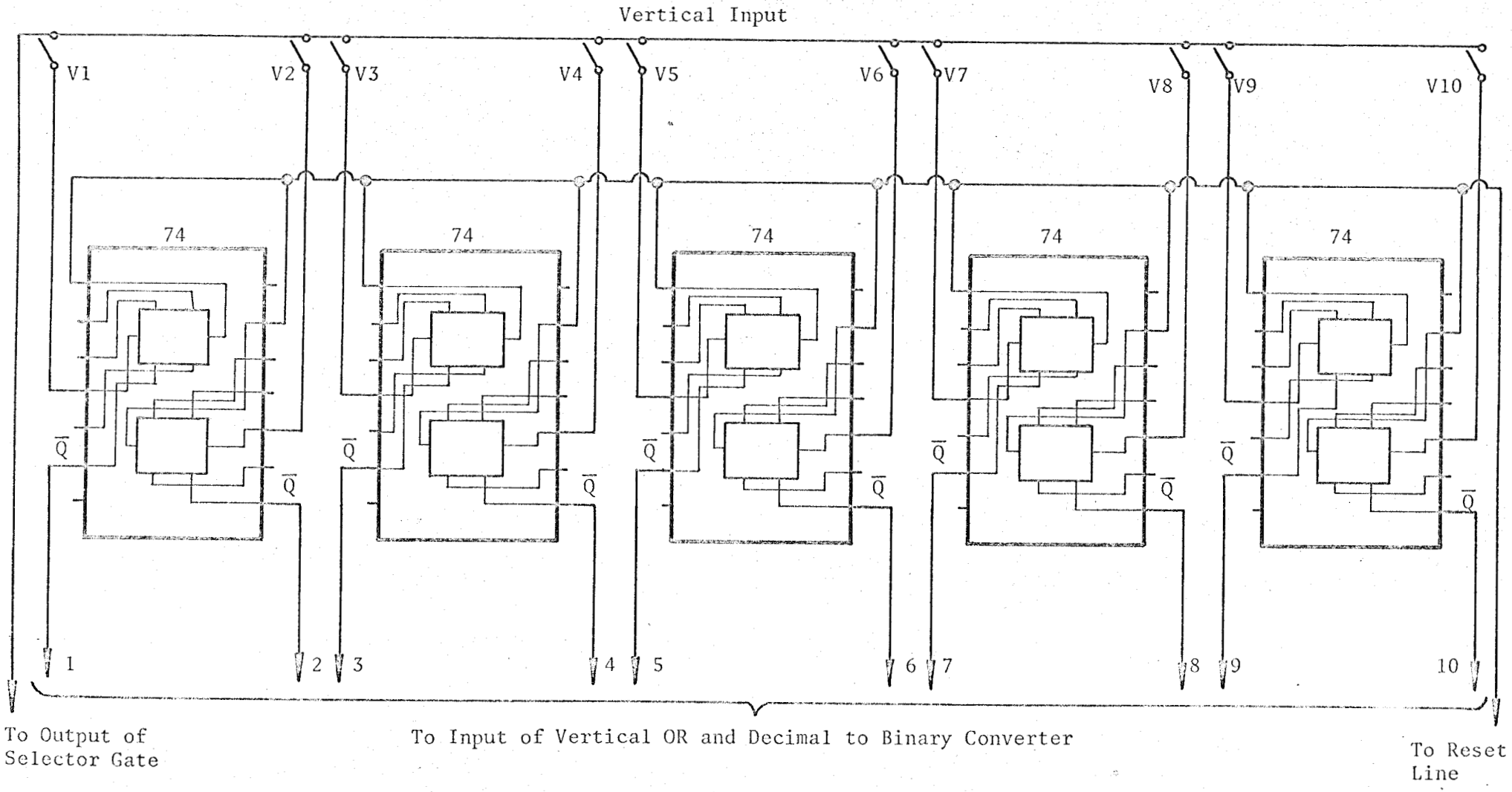

FIGURE 7: VERTICAL BUFFER

Throughout the description of the logic electronics the $+V_{cc}$ supply lines and the negative supply lines will not be shown.

The VERTICAL BUFFER operation is as follows. Prior to making a selection, all of the input switches - V1 through to V10 - are open and the common line for all the switches, which goes to the output of the SELECTOR GATE, is low - 400 mV maximum in this logic family. A vertical input is made by momentarily closing one of the VERTICAL INPUT switches. This loads a "1" into the appropriate buffer.

The output lines of the VERTICAL BUFFER are applied, as shown in Figure 8, to the VERTICAL OR. If any one of the outputs from the $\overline{Q}$ sides of the VERTICAL BUFFER should go to "0", indicating that a selection has been made, the 2Y output of the SN7400N will rise to "1" which will be applied to the COINCIDENCE DETECTOR indicating that a VERTICAL INPUT has been made.

6.2 Decimal to Binary Converter and Inverter

The output lines from the VERTICAL BUFFER, in addition to being applied to the VERTICAL OR, are also applied to the DECIMAL TO BINARY CONVERTER shown along with its INVERTER in Figures 9a and 9b respectively.

Numbers are used to indicate connections between the outputs of the VERTICAL BUFFERS and the circuits, since the

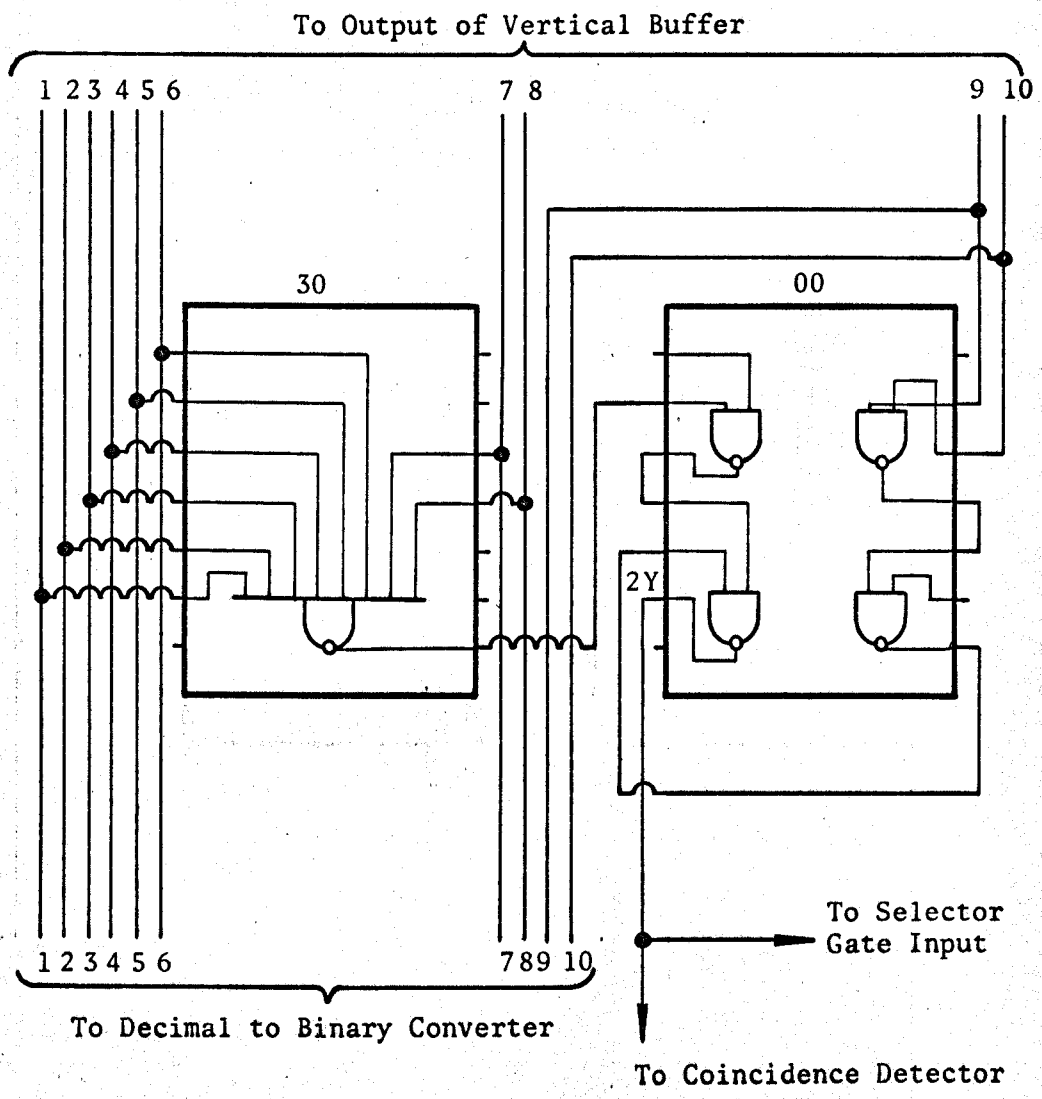

FIGURE 8: VERTICAL OR

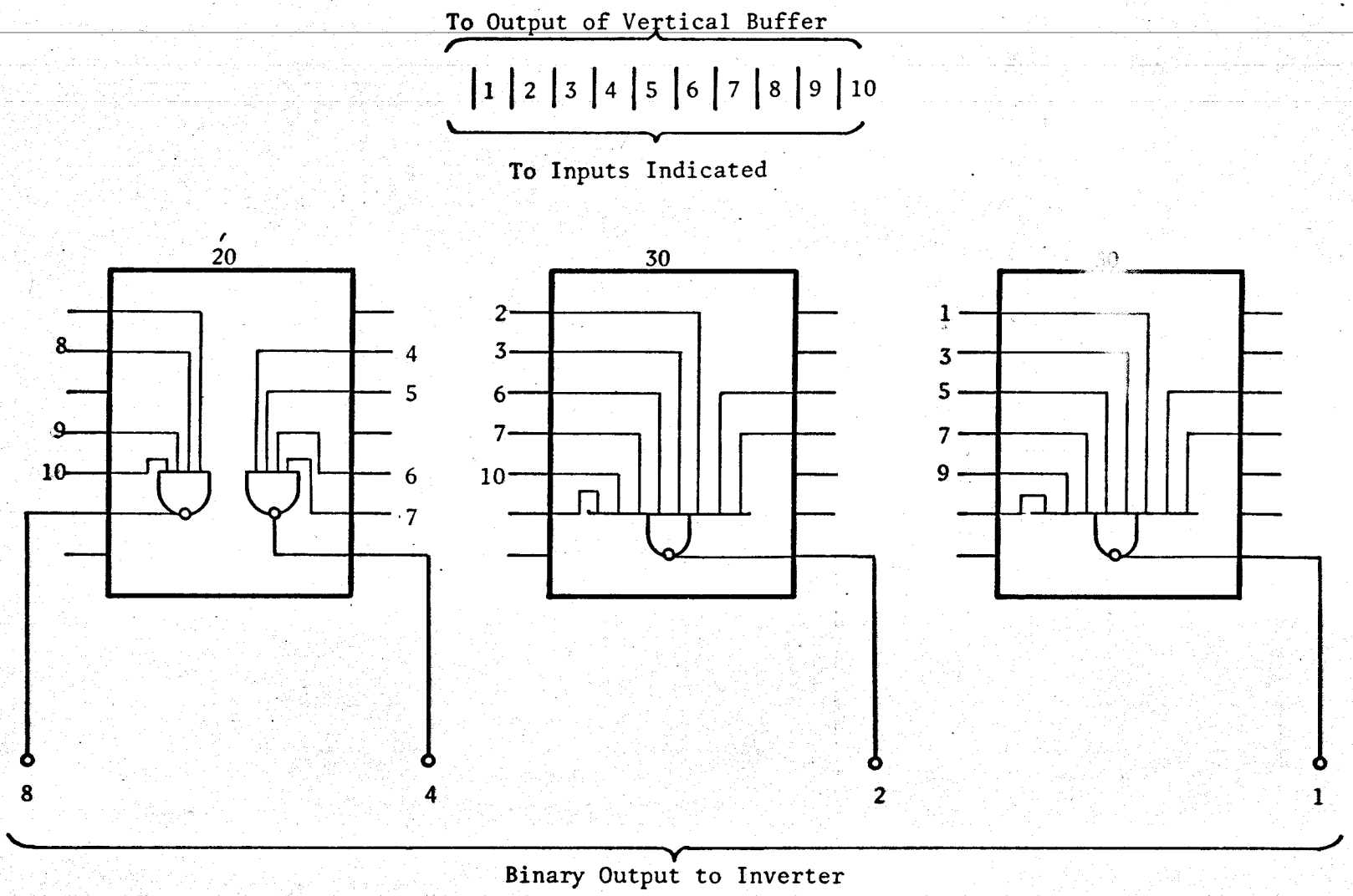

FIGURE 9(a): DECIMAL TO BINARY CONVERTER

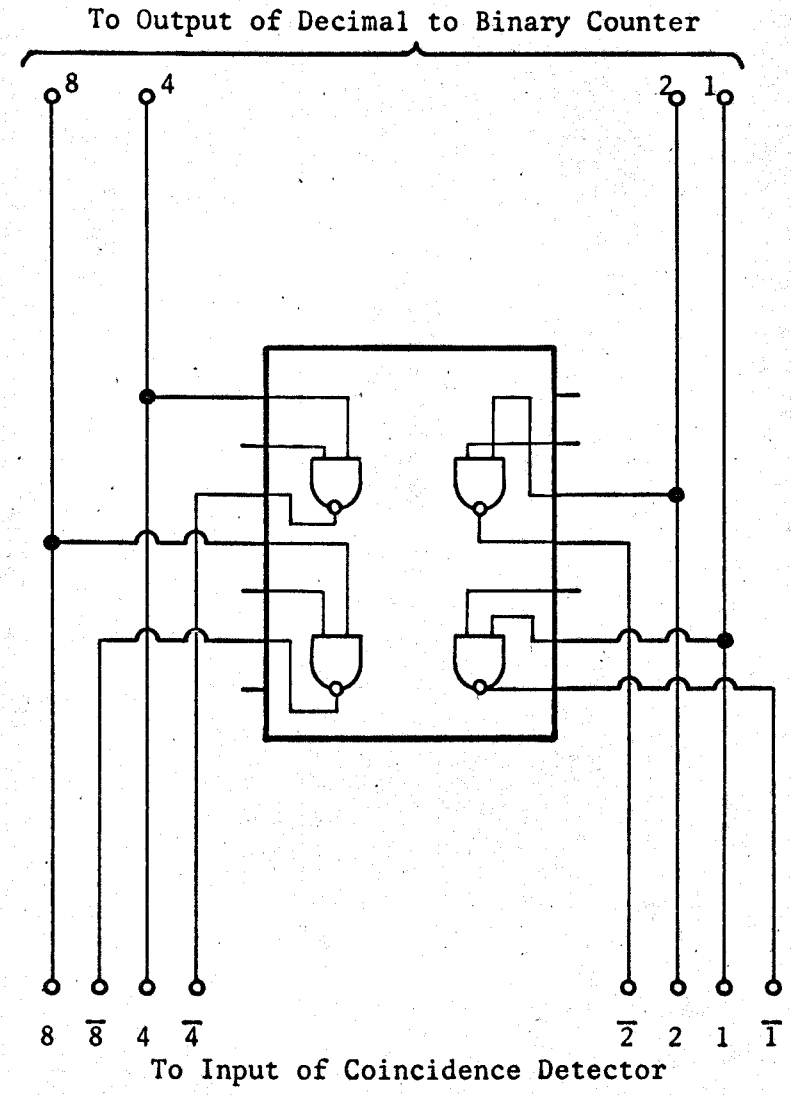

FIGURE 9(b): INVERTER FOR DECIMAL TO BINARY CONVERTER

wiring diagram is difficult to follow due to the large number of cross-overs.

The three integrated circuits shown perform the OR function on the 10 input lines from the VERTICAL BUFFER and yield the binary equivalent as shown.

This 4 bit binary number is applied to the SN7400N INVERTER. The overall output is the original binary number and its complement which are applied to the coincidence detector of Figure 10.

6.3 Coincidence Detector and Binary Counter

The heart of the COINCIDENCE DETECTOR is the SN7451N dual exclusive OR gate which bears a close resemblance to the COINCIDENCE DETECTOR used in the prototype. The truth tables for the two are identical.

Let us consider the detection of coincidence on only the binary 8's place. The operation on all other digits is identical. The 8 input from the INVERTER is connected to 2A and the 8 input from the BINARY COUNTER to 2B. From the specification sheet 2Y will be low only when both 2A and 2B are high in this case. This allows coincidence detection of a "1" in the 8's place of the INVERTER and BINARY COUNTER. If now the $\overline{8}$'s are connected to 2C and 2D, coincident "1's" in the $\overline{8}$'s place can be detected. In short, since 8 and $\overline{8}$ are binary complements, 2Y will be low if both 8's or both

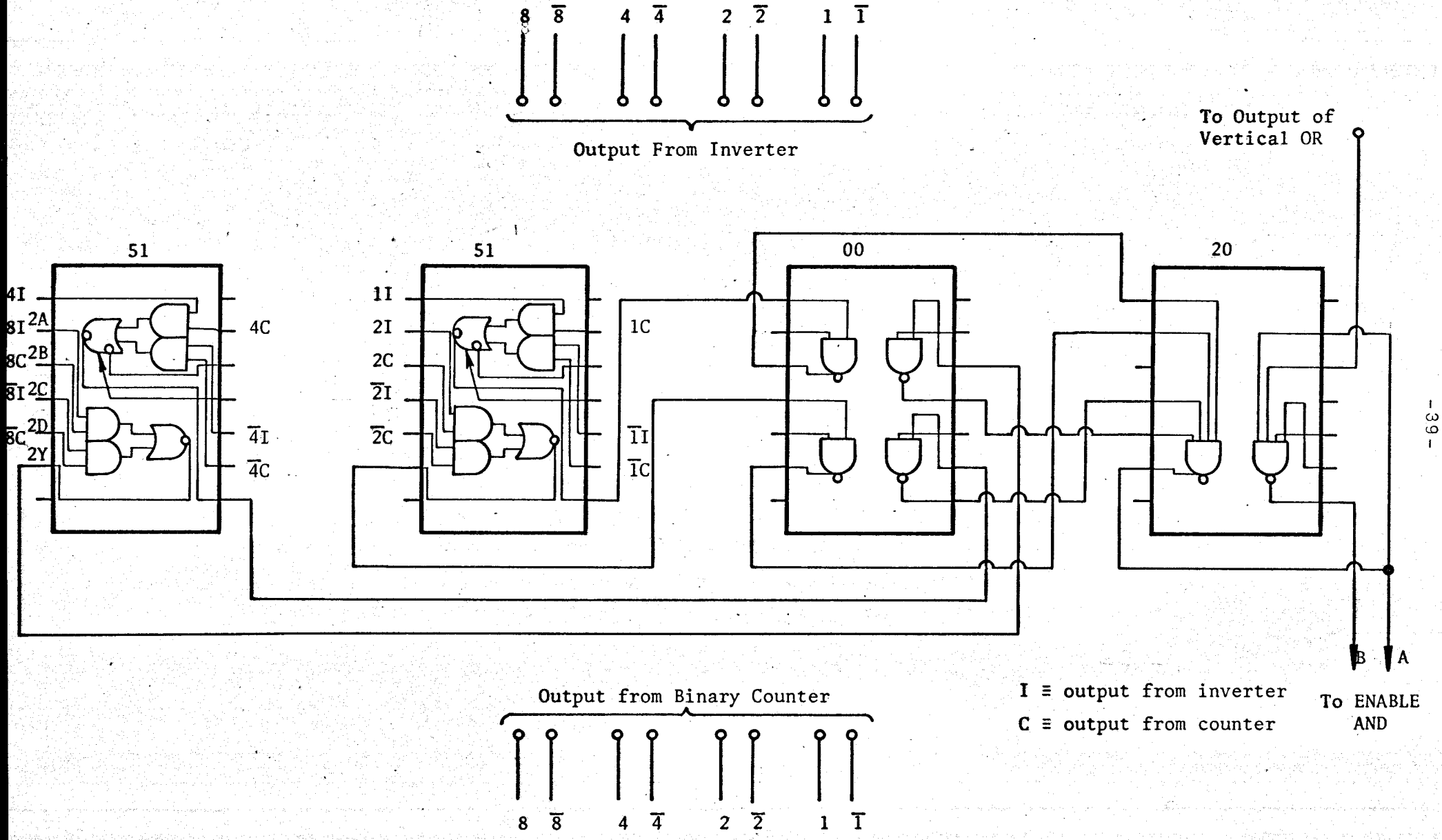

FIGURE 10: COINCIDENCE DETECTOR

$\overline{8}$'s are high - indicating coincidence.

The 4 outputs from the SN7451N's are all applied to the SN7400N gate for inversion in order that the AND function can be performed in the SN7420N. The resultant output is applied to the ENABLE AND gate via lines A and B.

Line A to the ENABLE AND gate from the COINCIDENCE DETECTOR is low or at "0" only during coincidence. At all other times it is at "1".

The BINARY COUNTER of Figure 11 is composed of integrated circuit type D flip-flops, connected to form the conventional ripple carry binary counter. The COUNT line is connected to the output of the COUNT SCHMITT TRIGGER and the RESET line to the output of the RESET SCHMITT TRIGGER. The operation of the COUNT and RESET SCHMITT TRIGGERS here is identical to that of the prototype. Pulses derived from the count holes sequentially advance the counter towards 10. The next pulse to arrive at the counter will be a reset pulse which resets the counter to 1.

6.4 Enable And

The purpose of the ENABLE AND shown in Figure 12 is to determine when and at what speed the tape drive motor is to run. It makes its decision on the basis of the output of the COINCIDENCE DETECTOR and the output of the HEAD STATE and RESET flip-flop.

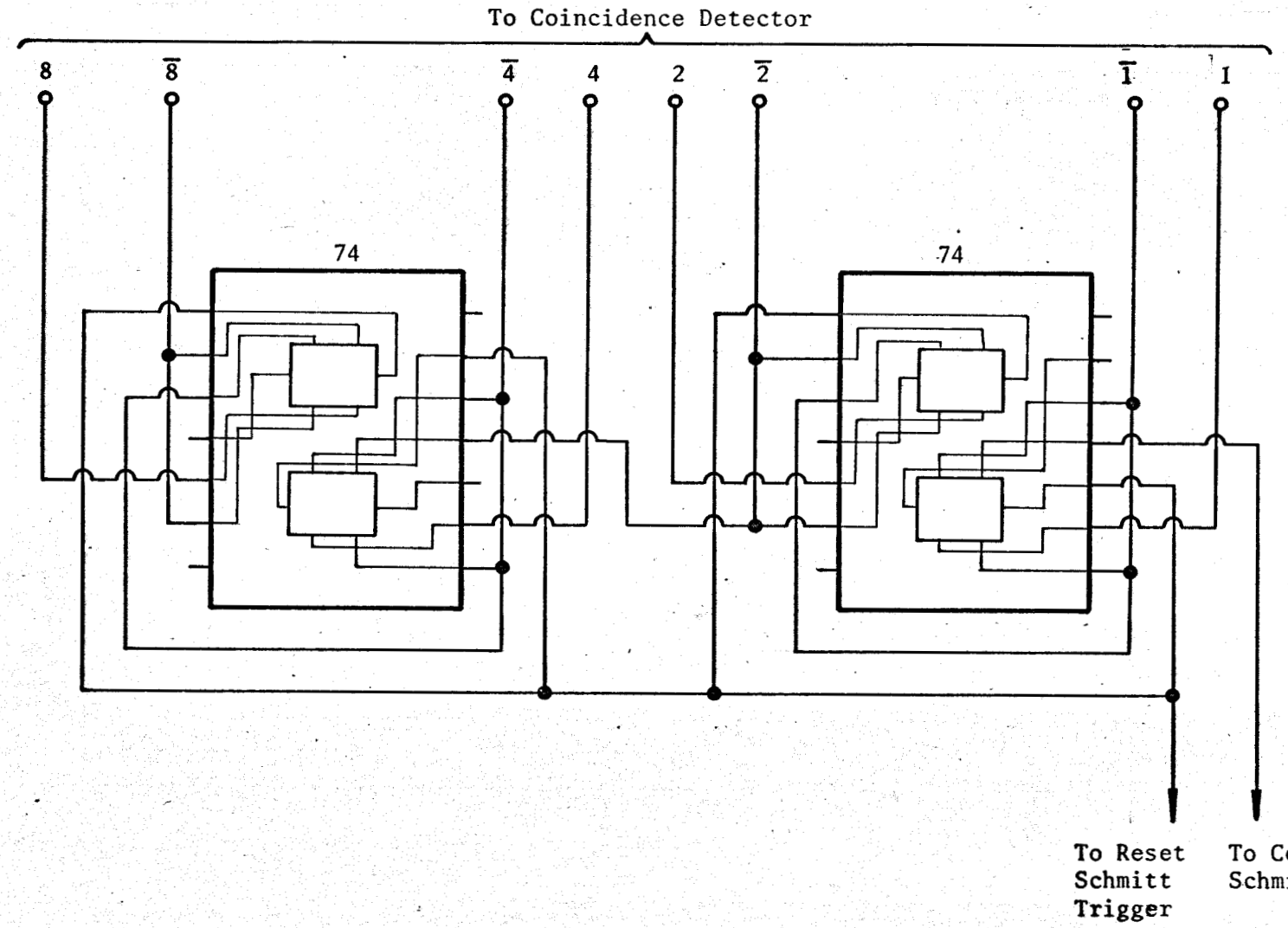

FIGURE 11: BINARY COUNTER

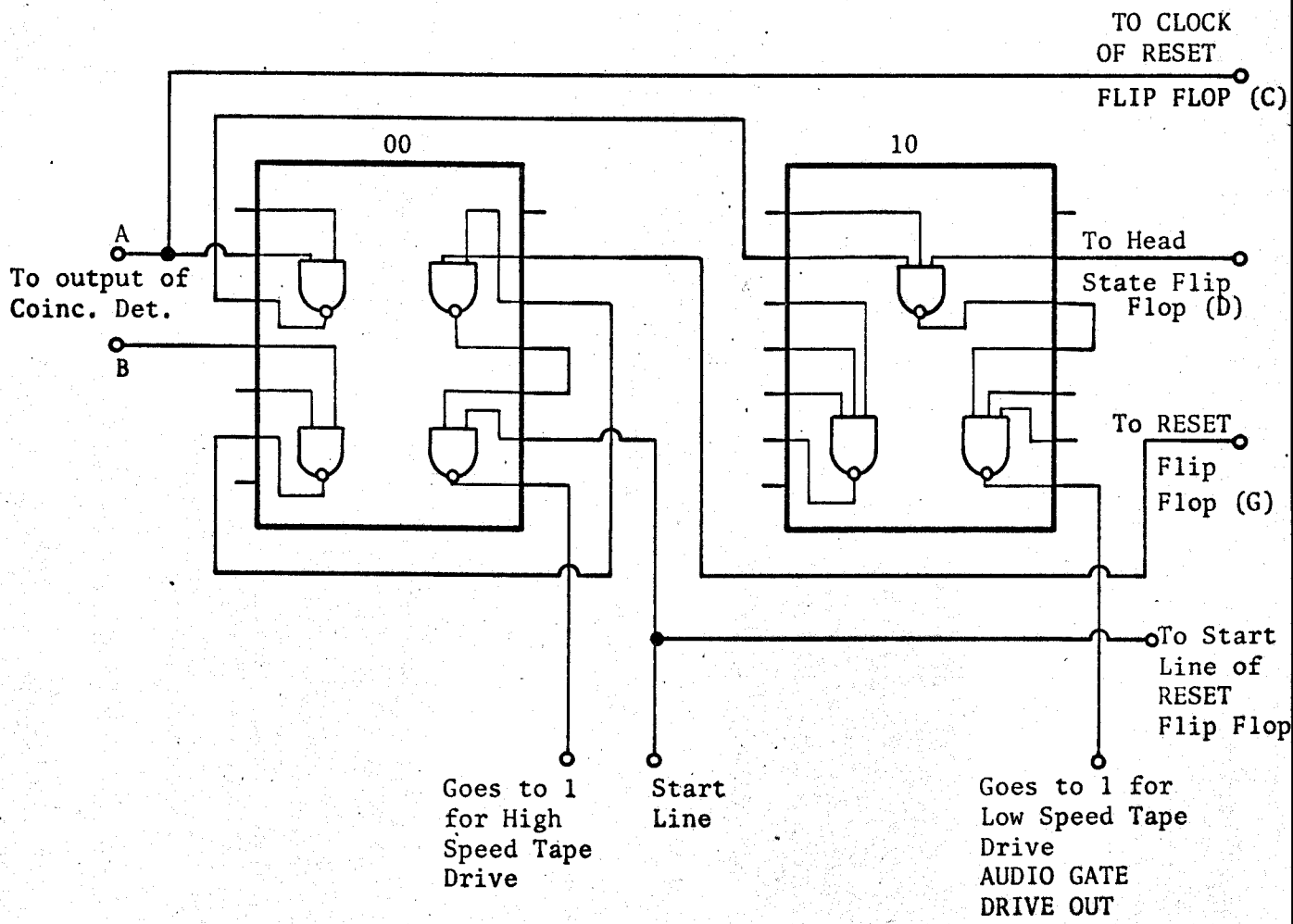

FIGURE 12: ENABLE AND

It also initiates the reset cycle at the termination of a selection via line C.

Upon the application of a vertical input, line B of Figure 12 goes high if coincidence does not exist. This causes the HIGH SPEED tape drive line to rise to a "1" and the tape then advances at its high scanning speed until coincidence is achieved. At this time, the input line B falls to a "0" and the tape drive stops. When line D goes to a "1", indicating that the head is non zero and stationary, it is at the required track and the tape deck starts its slow speed playback. At the termination of playback, the binary counter is advanced by one count and coincidence no longer exists. At this time C rises from zero to "1" and starts the reset cycle.

Line G goes to "0" when the head is returning to zero to prevent the tape deck from running while the head is returning to zero.

The START LINE is held negative a few seconds after the system is turned on to allow the photo reader at least one pass at the reset hole in order that the BINARY COUNTER can be registered.

6.5 Horizontal and Level Buffers and OR

The HORIZONTAL and LEVEL BUFFERS are shown in Figure 13. The HORIZONTAL BUFFER is connected as a 10 bit shift register

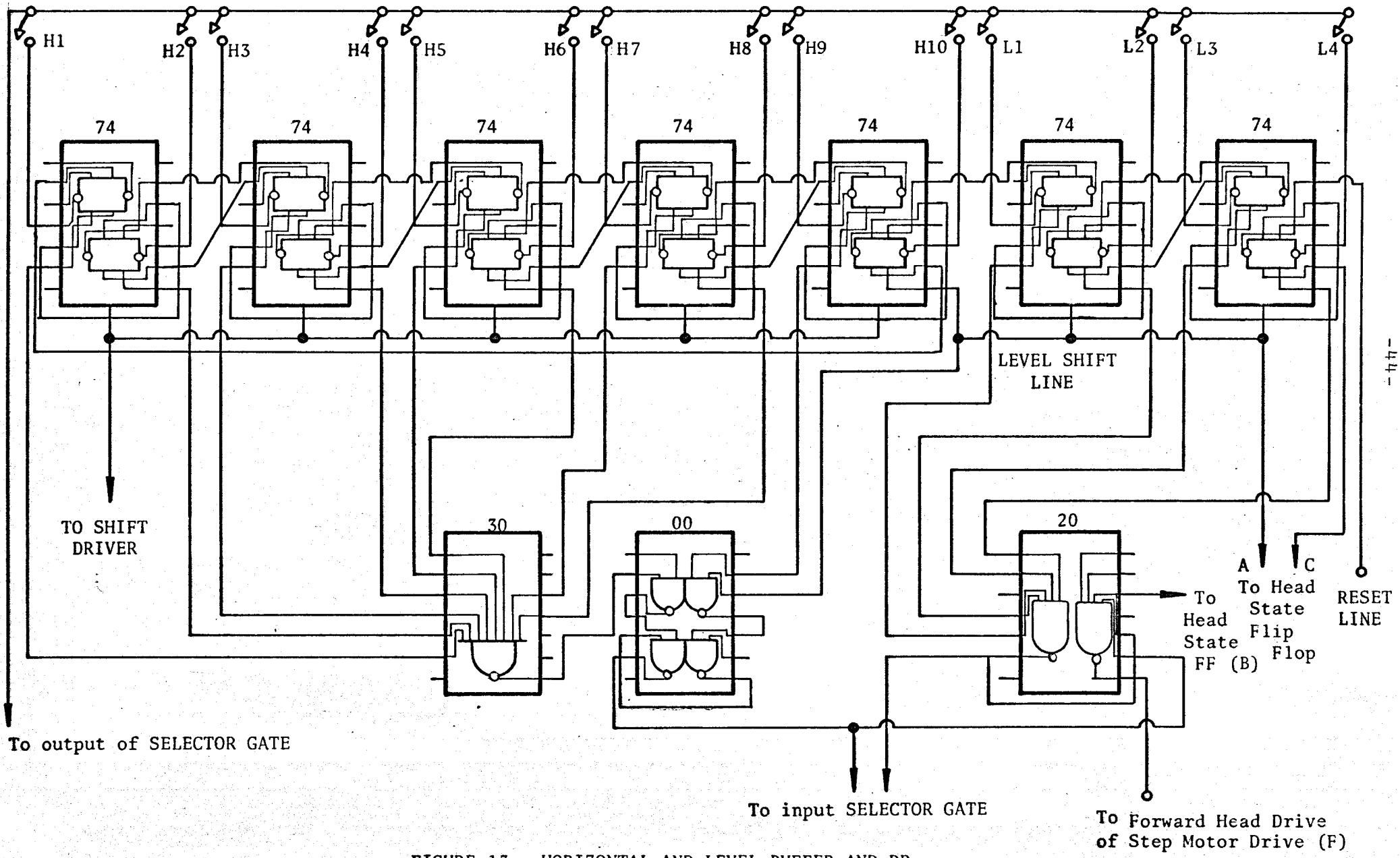

FIGURE 13: HORIZONTAL AND LEVEL BUFFER AND DR.

passing its carry to the LEVEL BUFFER which is connected as a 4 bit shift register. The overflow from the LEVEL BUFFER is loaded into the HEAD STATE flip-flop.

The ultimate purpose of the HORIZONTAL and LEVEL BUFFERS is to position the head over the required track. This is achieved according to the following. One bit of information is loaded into each group of buffers. At this time, pulses derived from the head drive logic simultaneously advance the head and drive the shift register. When the last stage of the LEVEL BUFFER loads the HEAD STATE flip-flop, the step motor drive is terminated and the head is at the proper location. A unique definition of 1 track in 40 is achieved by loading one bit into one stage of the HORIZONTAL BUFFER and one bit into one stage of the LEVEL BUFFER.

The HORIZONTAL and LEVEL OR operates in the same fashion as does the VERTICAL OR.

6.6 Step Motor Drive and Buffer Shifting Logic

It is the purpose of the logic in Figure 14 to control the operation of the stepper motor and to generate shift pulses for the HORIZONTAL and LEVEL BUFFERS. The MC724P is run as a conventional astable multivibrator under control of the SN7400N(A). Suppose that a selection has just been made. Line F goes low and the MC724P oscillator starts. Its output drives the two SN7470N flip-flops which are connected as a

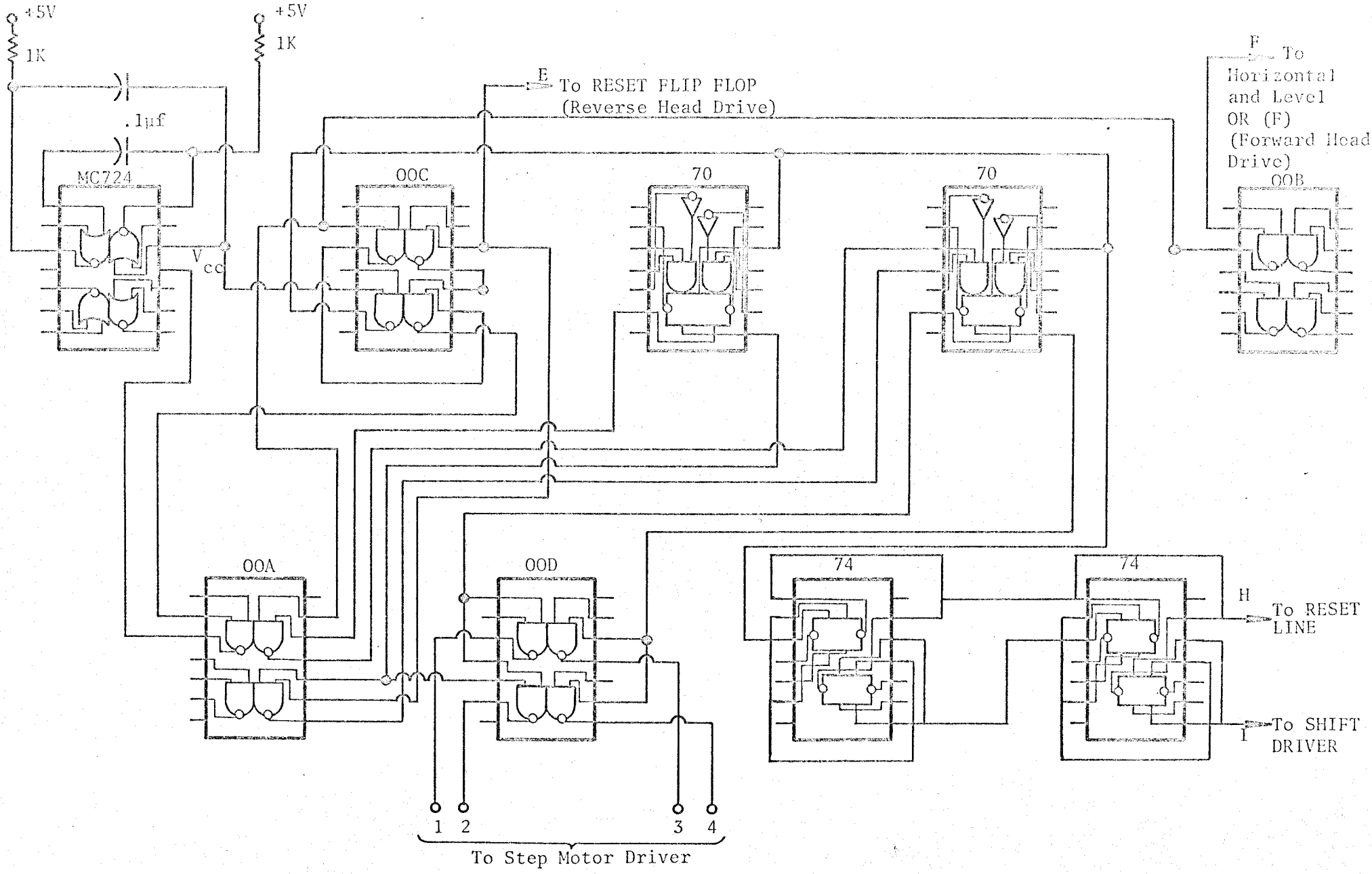

FIGURE 14: STEP MOTOR DRIVE AND BUFFER SHIFTING LOGIC

synchronous binary counter. The outputs of this counter are decoded by the SN7400N(C) and SN7400N(D) into sequential energization of the 1, 2, 3, and 4 lines going to the stepper motor. This causes the stepper motor to rotate in such a direction as to move the head from its zero position across the tape.

At this time, the output of the oscillator is also being divided by 16 in the two SN7474N's interconnected as a ripple carry counter. This is necessary since the motor requires 16 steps to make one complete revolution and the HORIZONTAL BUFFER must be shifted only once per revolution.

When the head reaches its destination, line F goes high since the last bit in the LEVEL BUFFER has been shifted into the HEAD STATE flip-flop. The step motor and head now come to rest.

On the completion of playback, line E, which is connected to the RESET flip-flop, goes high. The oscillator again starts, however, at this time the SN7400N(C) and SN7400N(D) are gated so as to cause the pulse sequence at their outputs to be 4, 3, 2, and 1. This causes the head stepper motor to rotate in the reverse direction. This will continue until the zero detector pulls the clear line of the RESET flip-flop low, resetting it and stopping the head stepper motor. When line E goes high, all input buffers are reset.

This completes the description of the track selection and head resetting.

6.7 Shift and Reset Driver

The SHIFT and RESET DRIVER of Figure 15 is required since the fan out of the series SN7400N gates is only 10. In the resetting application, a fan out of 29 is required and therefore the SN7440N is used since it has a maximum fan out of 30.

Pulses derived from the SHIFTING LOGIC are inverted and amplified by the SN7440N and applied to the shifting line. The positive going level from the RESET flip-flop is inverted and amplified by the SN7440N and applied to all reset lines in the system.

6.8 Selector Gate

The purpose of the SELECTOR GATE of Figure 16 is to preclude the possibility of loading information into the input buffers until such time as a complete selection cycle has been performed.

The output to the SELECTOR LINE remains low until one bit has been loaded into each buffer. At this time it rises to "1" and remains there until the completion of a selection. Then and only then can information for the next selection be loaded into the input buffers.

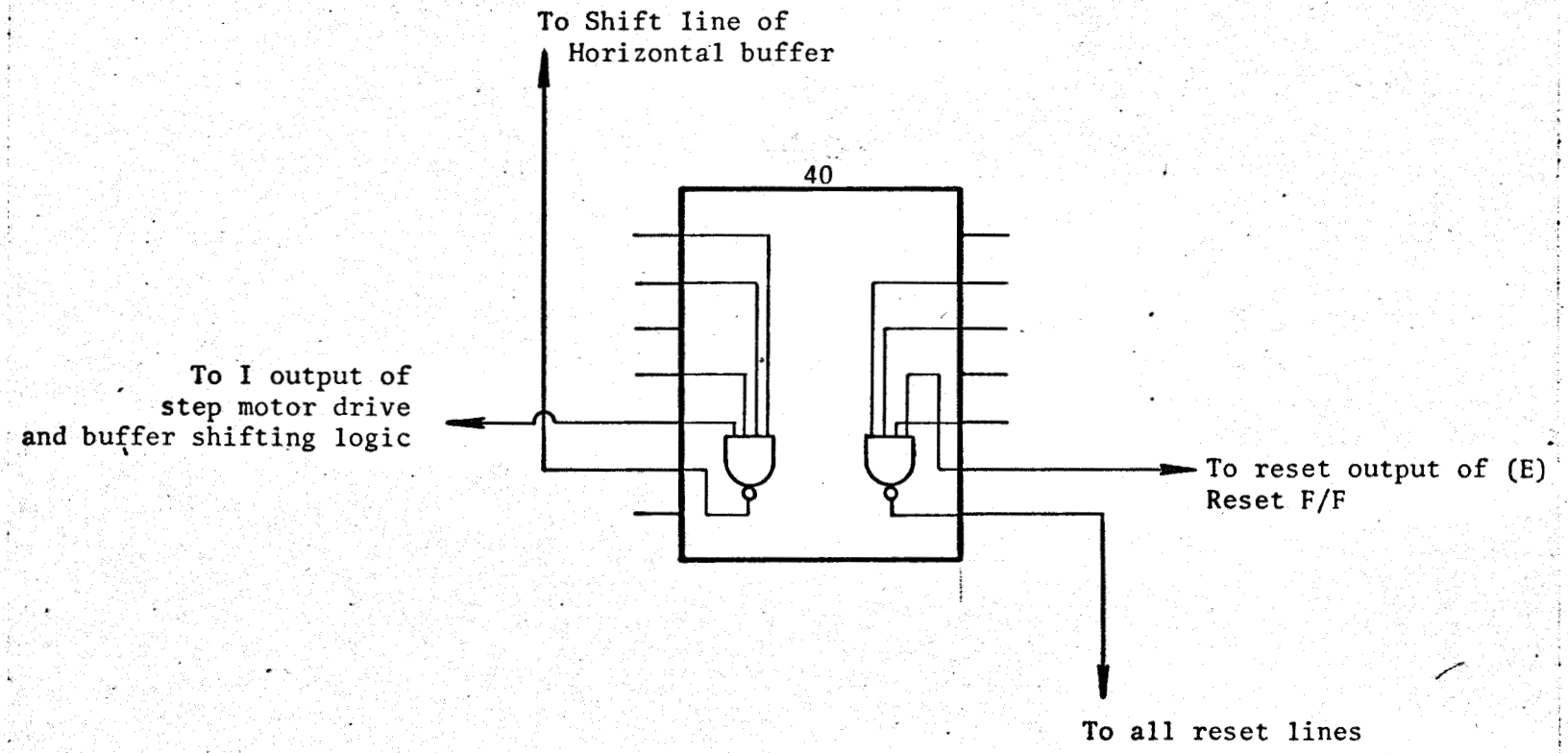

FIGURE 15: SHIFT AND RESET DRIVER

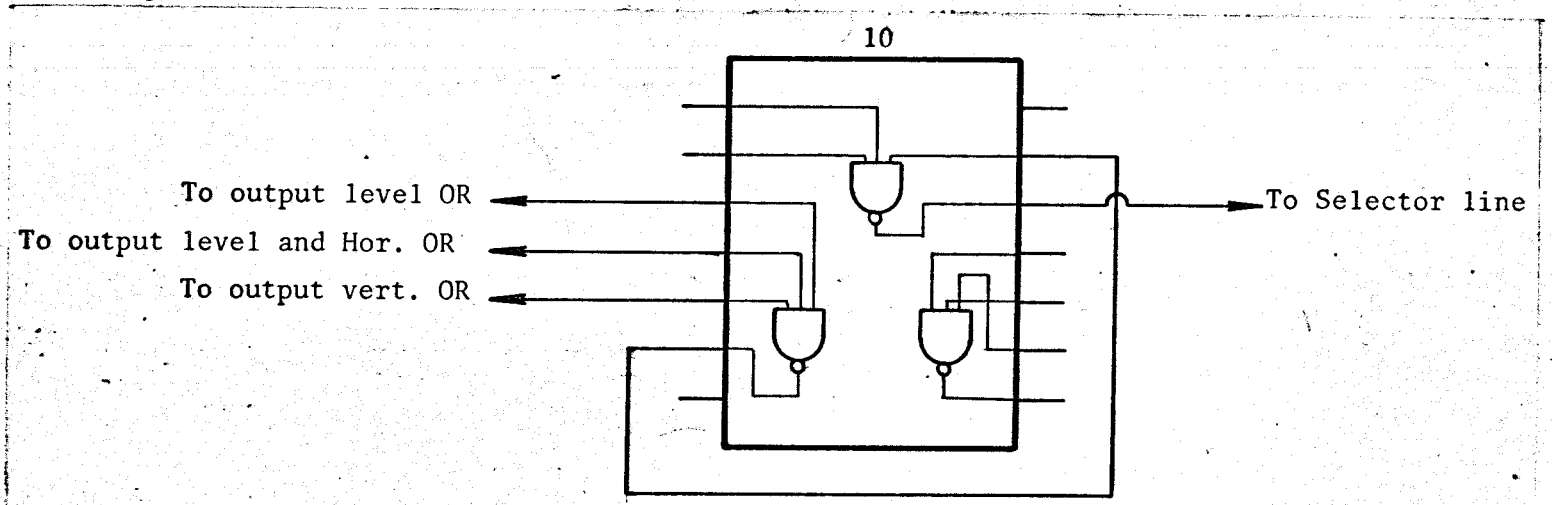

FIGURE 16: SELECTOR GATE

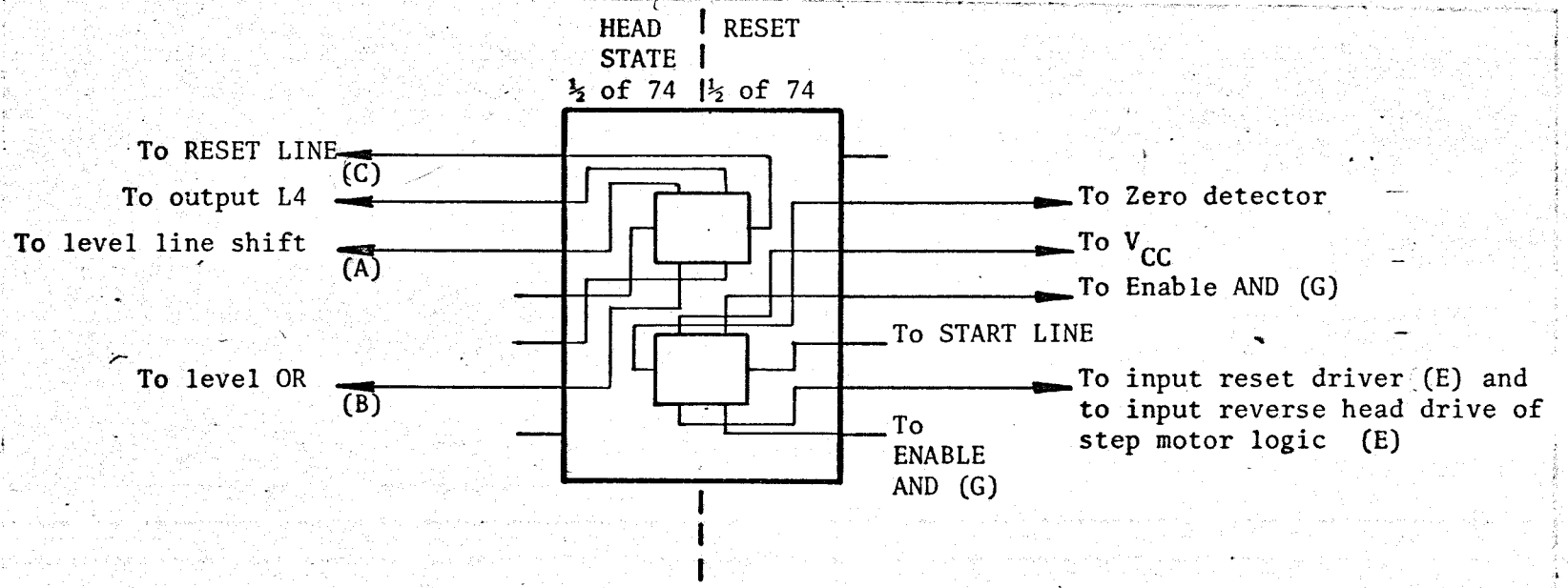

FIGURE 17: HEAD STATE AND RESET FLIP FLOP

6.9 Head State and Reset Flip-Flop

Figure 17 shows the SN7474N dual D HEAD STATE and RESET flip-flop. It is a multipurpose unit. It informs the ENABLE AND concerning the position of the head as well as resetting all flip-flops and buffers at the termination of a selection.

Suppose that a HORIZONTAL and LEVEL selection have just been made and that the LEVEL input has been shifted to L_4. One shift pulse later it will be shifted out into the HEAD STATE flip-flop leaving the LEVEL BUFFER empty. This will stop the head over its required track. At the termination of playback, the RESET flip-flop will receive a signal from the ENABLE AND indicating anti-coincidence and will reset all buffers and flip-flops in the system. Simultaneously this output will also drive the head toward zero. When the head strikes zero, the zero detector clears the RESET flip-flop and the entire system comes to rest awaiting the next input.

6.10 Step Motor Drive and Clutch Drive

Integrated circuits were used for all the logic functions with the exception of the clutch and step motor drivers. The clutch drivers are similar to the ones used in the prototype - described on page 79 - and consequently will not be dealt with further. The step motor drivers are shown in Figure 18.

The STEP MOTOR DRIVE sequentially takes points 1, 2, 3,

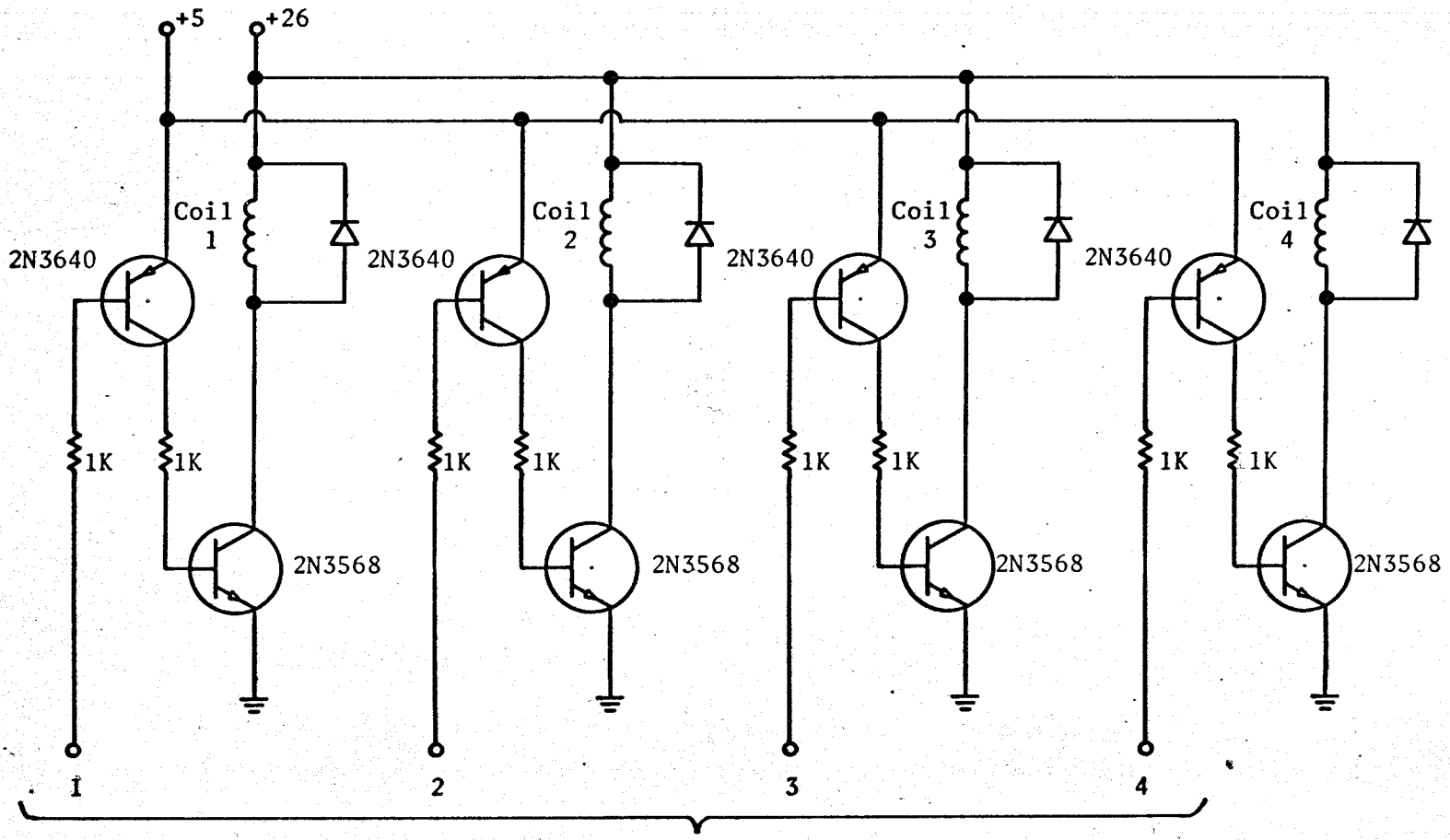

FIGURE 18: STEP MOTOR DRIVERS

and 4 negative - one at a time. This saturates the corresponding 2N3640 and the 2N3568 and energizes the motor field coils in the collector circuits of the 2N3568's. Sequential energization of these coils cause the motor to rotate in a stepwise fashion. The pulse sequence 1, 2, 3, 4 causes forward rotation and 4, 3, 2, 1 causes reverse rotation.

6.11 Summary of Operation

The only difference in principle of operation between the prototype and the improved model just described lies in the selection of the track on tape. The prototype utilized 40 heads whereas the improved model positions one head over the required one of 40 tracks. The net result of the operation of both systems is the same. In response to the loading of three input buffers the system selects the proper location on tape and allows the recording or playing back of one word of audio information.

7. CONCLUSIONS

7.1 View of Systems Performance

Due to delivery time limitations on the welded continuous loops of magnetic recording tape, it has not been possible to test and evaluate the entire system as a unit. Nevertheless the tape deck, the logic electronics and the audio electronics have been evaluated separately and were found to meet and in some cases potentially exceed the minimum design criteria.

The integrated circuit logic electronics and the improved vocabulary tape deck constitute a communication device with a maximum average information transfer rate of 30 words per minute. The input section of the logic electronics possess sufficient flexibility to accommodate a number of different input transducers and therefore will allow this unit to be used in the evaluation of studies currently being carried out in the design, construction, and optimization of input transducers.

Vocabulary content can be changed in one of two ways at the operator's or his attendant's discretion. Single words can be changed by simply recording the desired word in the desired location. On the other hand, the entire vocabulary can be changed by placing a memory tape with the desired words on the tape deck.

In conclusion, this system provides a useful audio communication facility with reasonable specifications for people suffering from ataxic aphasia.

7.2 Proposals for Further Study

Even though the clutch type drive system in principle works very well, an alternate scheme would be desirable since the clutch drive contributes about half of the total cost of the system as well as a good proportion of the overall weight. It should be possible to achieve the two speeds - scan and playback - by using a stepper motor operating at two different frequencies. The velocity perturbations in the output would of course have to be damped out. The total tape drive mechanism would then require only one motor in contrast to the one motor, two reduction systems and two clutches, now in use.

A reduction could be realized in the access time by further sophistication of the logic electronics. If the horizontal and level buffers were made bidirectional shift registers, the head positioning time could be reduced by a factor of 2.

With the audio electronics used, it was found in a test setup that tape speeds as low as 1 inch per second gave very good reproduction. This coupled with the use of a .012 inch track width head would allow a total vocabulary of 2400 words with an average access time of 1/2 second. By judicious

selection of the head stepper motor and tape drive stepper motor, and more sophisticated logic electronics, one should be able to reduce the access time still further. By shaping the transfer characteristic of the audio amplifier, playback speeds less than 1 inch per second could be utilized and still retain acceptable fidelity.

By incorporating the aforementioned modifications, it is felt that a system could be constructed with about the same size and for about the same cost as the present system, but with a much faster access time and a much larger vocabulary.

In many cases a permanent hard copy output is required. For this application, the audio electronics could be replaced by digital logic to handle the recording and playing back of binary data for a teleprinter.

The inclusion of a sentence recorder in the audio output version would be a valuable asset. This would allow the operator to form continuous messages from individual selections.

For further study it is also proposed to investigate the possibility of coupling a number of operators to a small computing system. For purposes of audio communication, the system described in this thesis would be an integral part of the overall system. In addition to simple communication, a computing system would allow programmed learning for the

handicapped student as well as vocational training in computer programming and its allied fields.

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9. APPENDICES

Appendix A

Prototype Logic Electronics

This section contains a description of the prototype logic electronics. The tape positioning technique used here is very similar to that used in the integrated circuit version. On the other hand, the track selection in the prototype required specifying 1 of 40 record/playback heads that were positioned over the tape.

Figure 19 shows a block diagram of the prototype logic. The circuit descriptions will be executed in terms of the units shown in Figure 19.

Input Buffers

The input electronics consists of 24 one bit buffers. These buffers take the form of conventional bistable multivibrators. Figure 20 shows the circuit diagram for the buffer bistable multivibrator. The design procedure and requirements for this circuit and all subsequent logic electronics are outlined in the References.

Setting the BUFFER is accomplished by taking the collector of the $\overline{Q}$ side to logic "0". Throughout this system

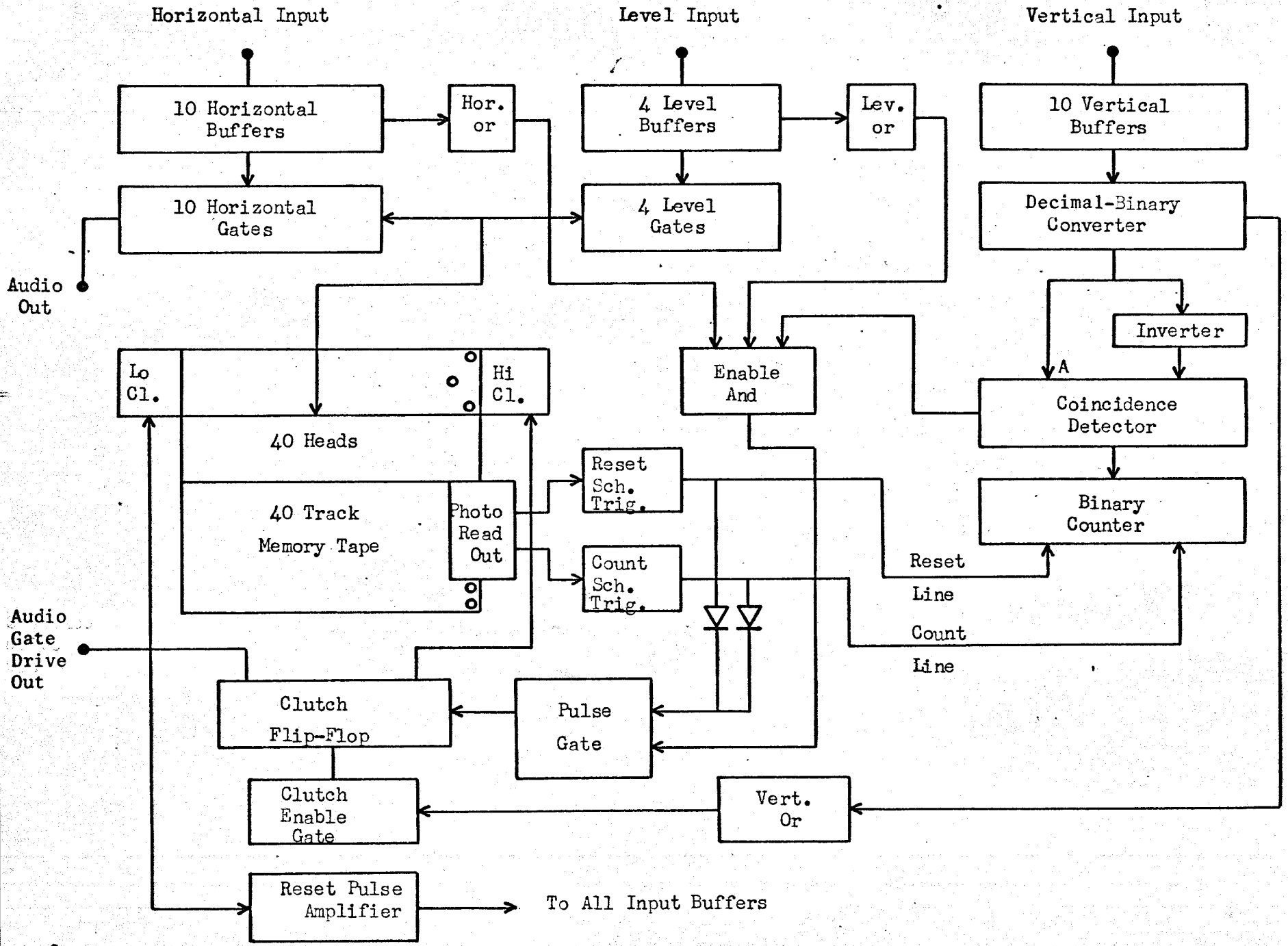


FIGURE 19: BLOCK DIAGRAM OF PROTOTYPE LOGIC

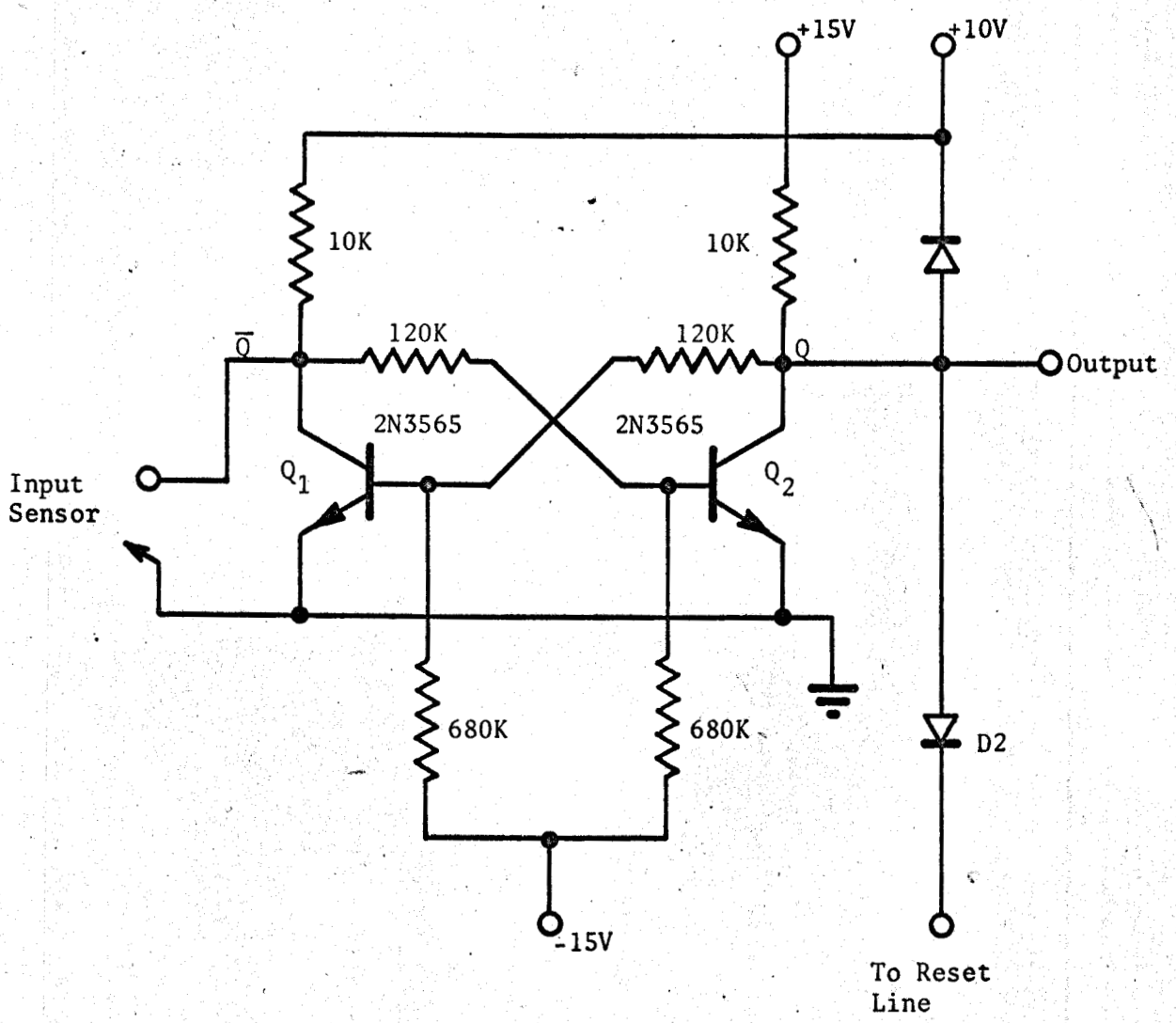


FIGURE 20: INPUT BUFFER BISTABLE MULTIVIBRATOR

a logic "1" output is defined as +10v and a logic "0" output by 0v. Resetting the BUFFER is accomplished by taking the cathode of D_2 to logic "0". The resetting action results in the collector of Q_2 residing at 0v.

Horizontal and Level Selection

The selection process requires the unique definition of 1 head from a group of 40 by making 2 selections - 1 from a group of 10 and 1 from a group of 4. By referring to Figure 21, if the heads are arranged into 4 groups of 10 each, we need only select the proper group and then the desired head from that group. The first head in the first group is connected to the first head in the second group and so on to the fourth group. This also applies to the 2nd, 3rd, 4th, etc. through to the 10th head of each group. We can now select any desired head by first closing the LEVEL GATE which grounds the group containing the desired head and then the HORIZONTAL GATE which is directly connected to the required head. This makes available one and only one head to the AUDIO OUT LINE for the purpose of recording or playing back.

The HORIZONTAL and LEVEL gates are actually electromechanical relays. Operation of these relays is accomplished by connecting the relay driver transistors to the output

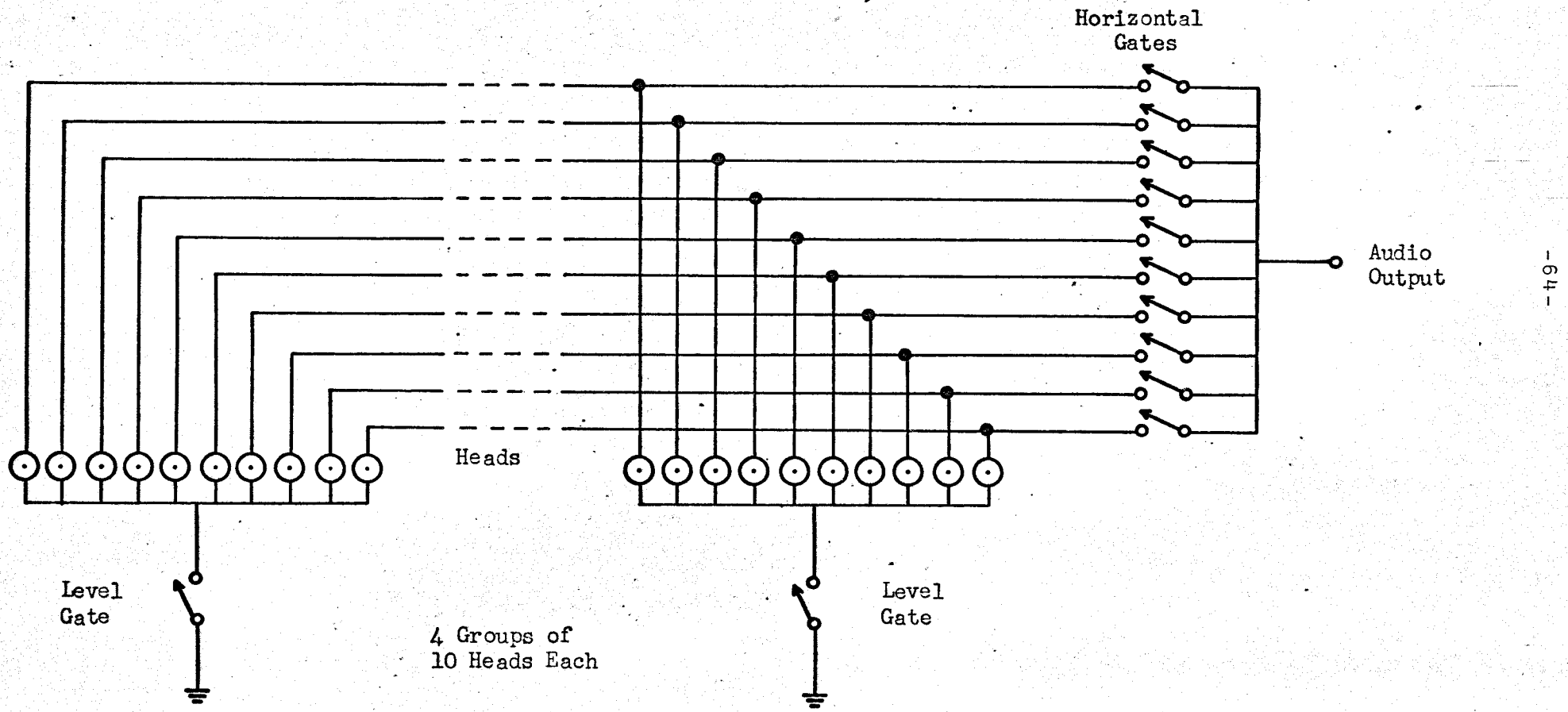
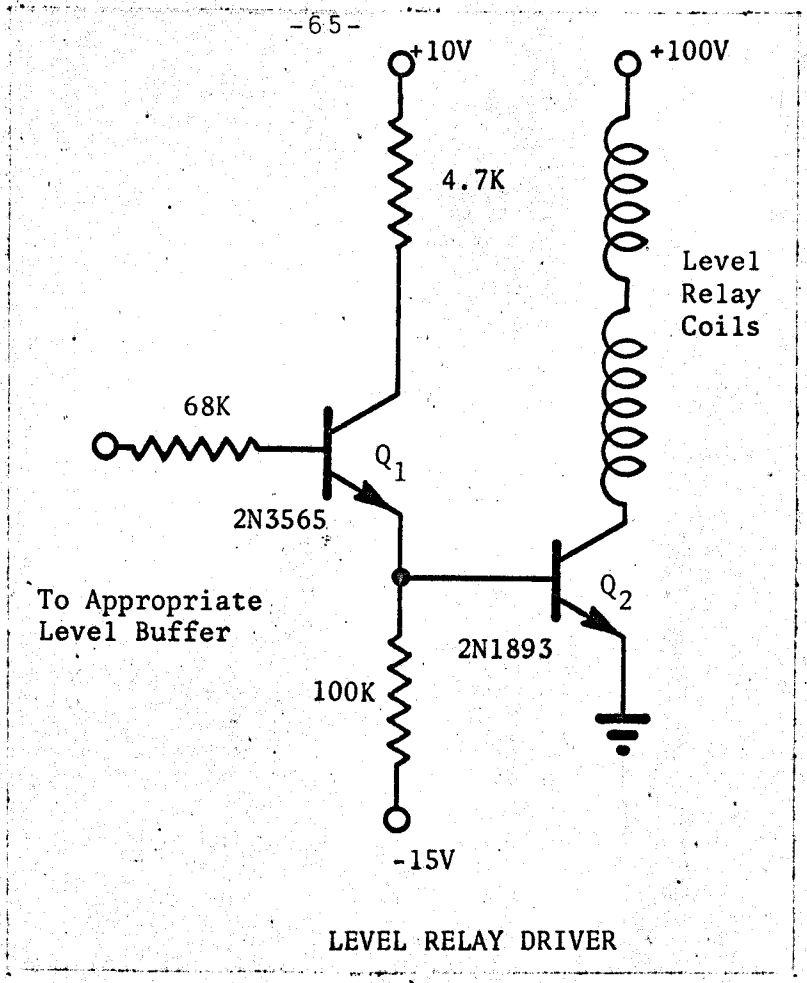
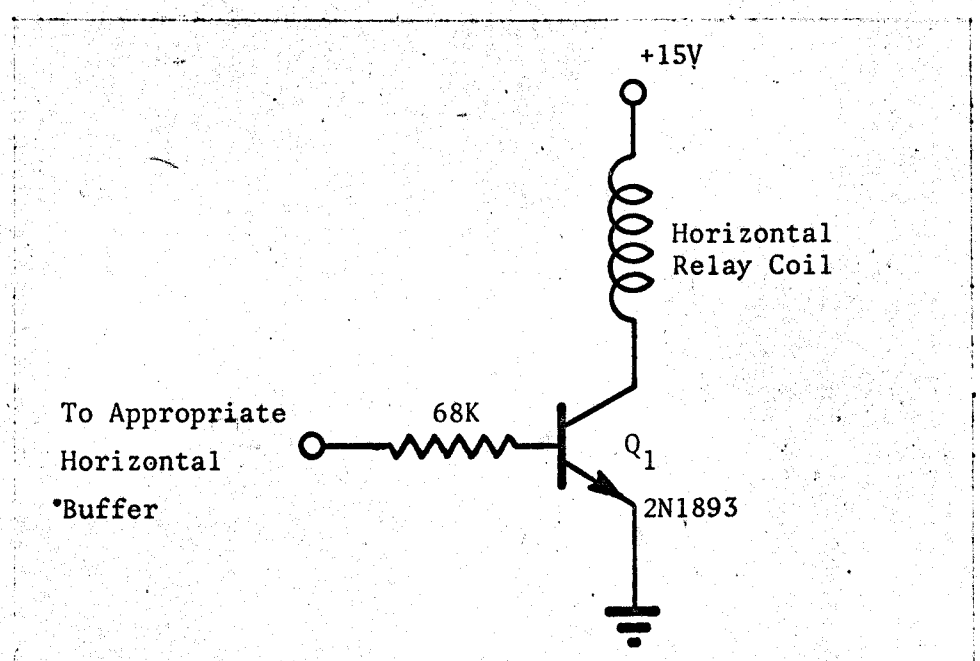


FIGURE 21: HORIZONTAL AND LEVEL SELECTION



LEVEL RELAY DRIVER



HORIZONTAL RELAY DRIVER

FIGURE 22: LEVEL AND HORIZONTAL RELAY DRIVERS

collectors of the corresponding input buffers. Circuit diagrams for the relay drive stages are shown in Figure 22.

Horizontal and Level OR Gates

These OR gates in Figure 23 inform the logic electronics when horizontal and level inputs have been made.

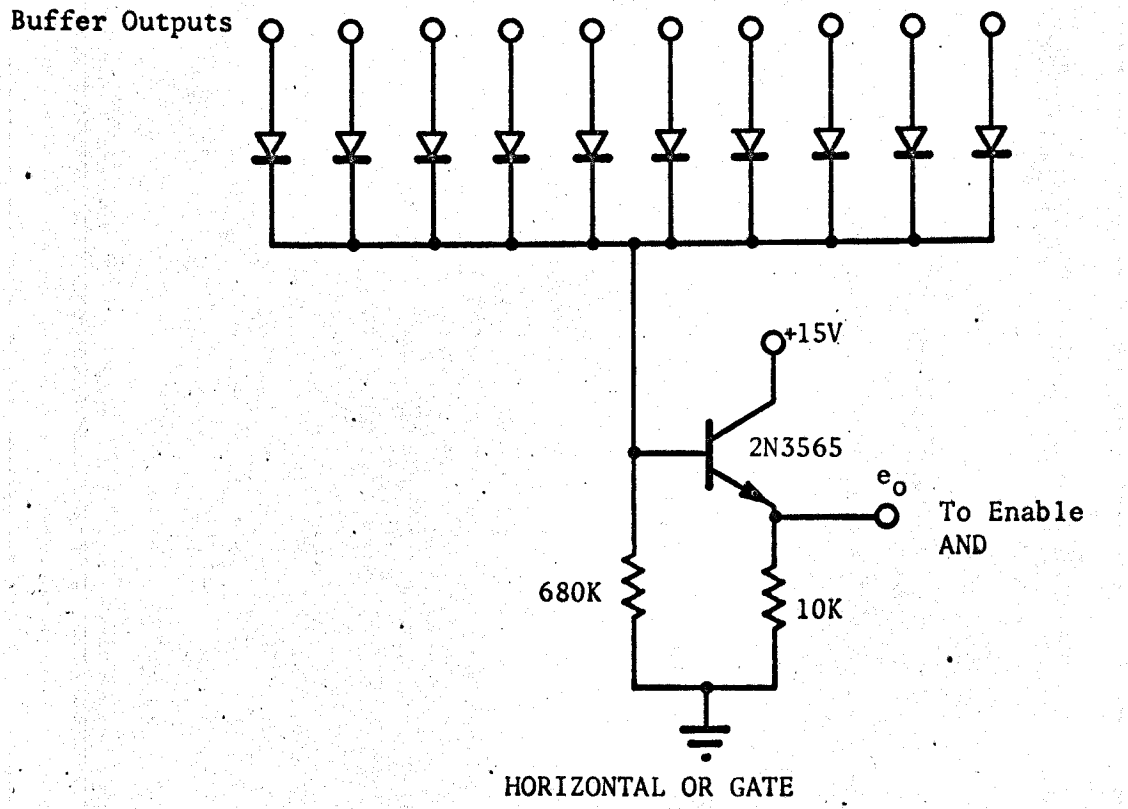
Decimal to Binary Converter

This circuit performs the same function as its counterpart in the integrated circuit version of the logic. It is shown in Figure 24.

Photo Readout and Schmitt Trigger

In order that the electronics be accurately informed of the tape's present position, there must be an address on the side of the tape defining its position. The type of addressing used in this system is a series of holes along one edge of the tape. There are 9 count holes very close to the edge and 1 reset hole indented slightly.

Optical pulses derived from these holes are detected and shaped by the circuits of Figure 25a and 25b. The photoreadout electronics consists of 2 of the circuits shown in Figure 25a and one of the circuits shown in Figure 25b. One of the circuits of Figure 25a is used to detect the count holes and the other is used to detect the reset hole. The



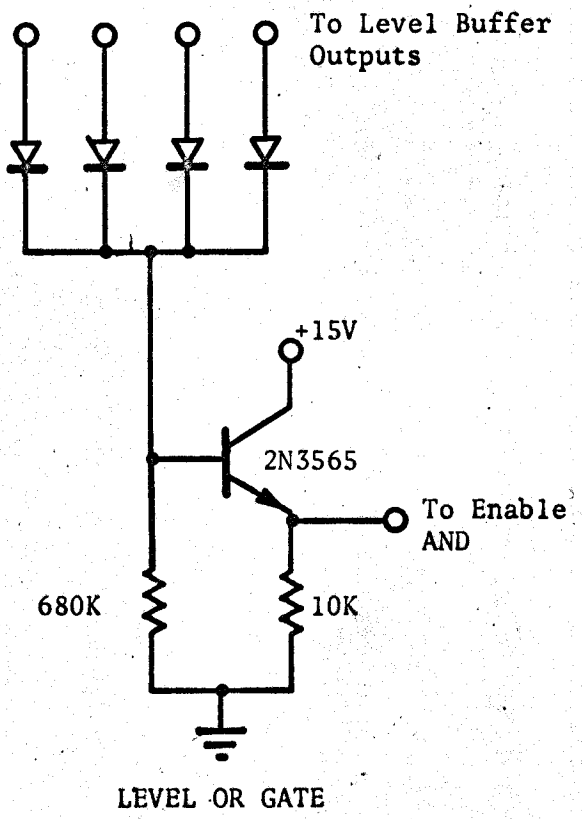


FIGURE 23: HORIZONTAL AND LEVEL OR GATE

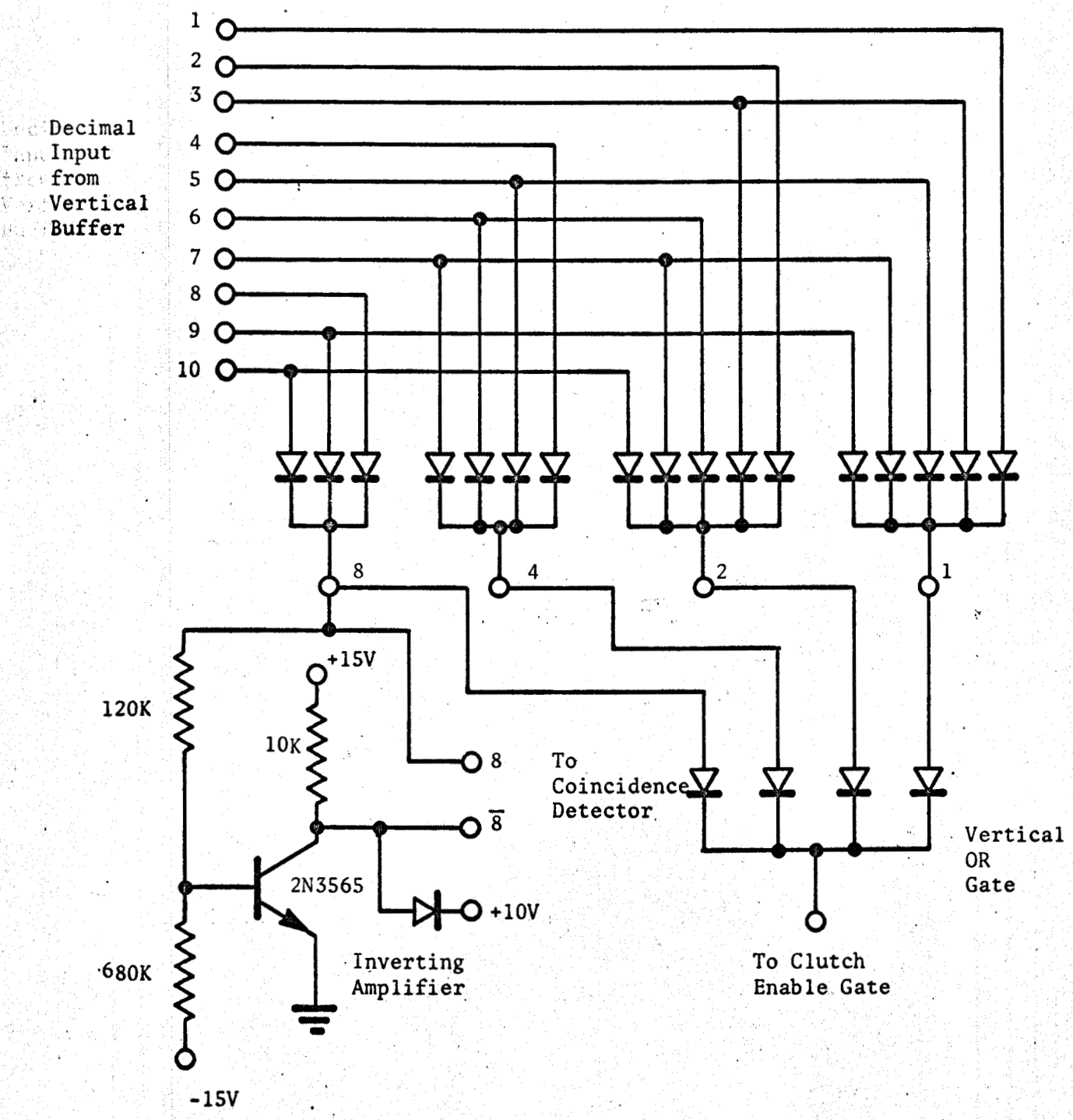
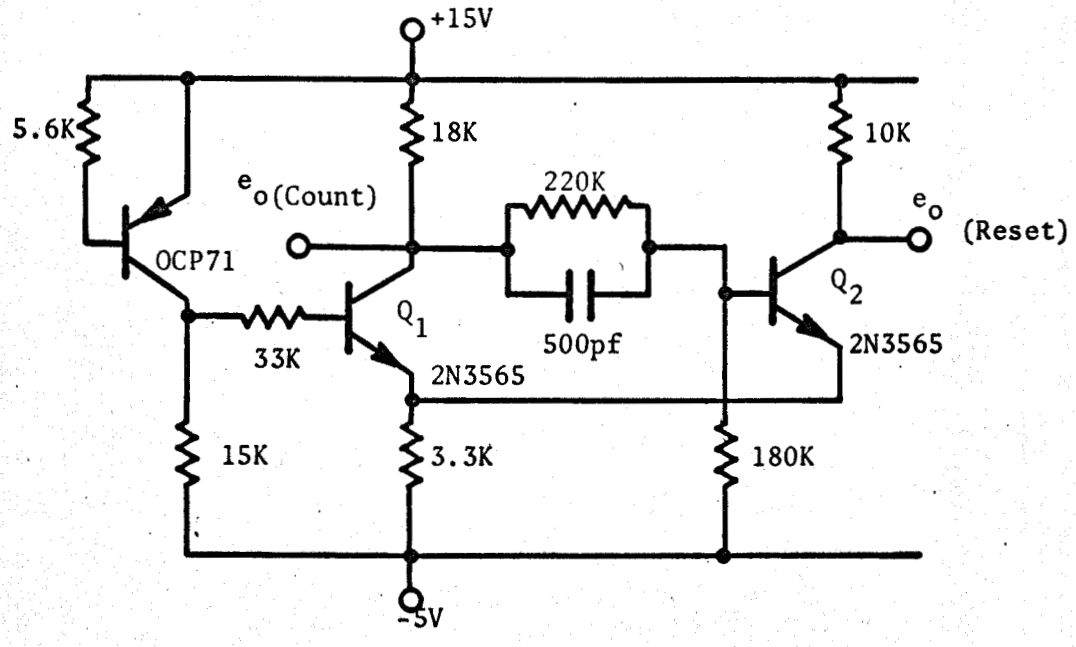
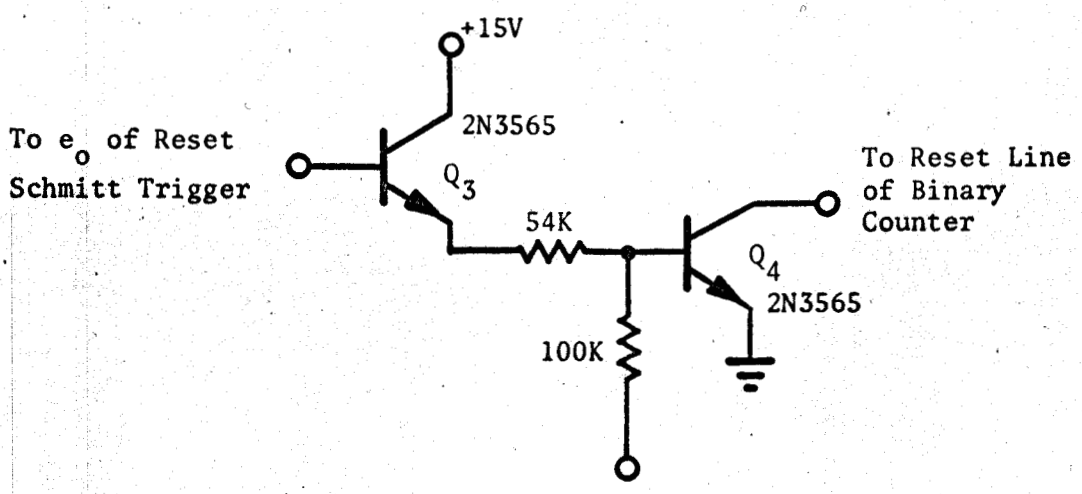


FIGURE 24: DECIMAL TO BINARY CONVERTER



COUNT AND RESET SCHMITT TRIGGER CIRCUIT DIAGRAM



RESET PULSE AMPLIFIER

FIGURE 25: COUNT AND RESET SCHMITT TRIGGER AND RESET AMPLIFIER

circuit of Figure 25a is a photo transistor (OCP71) operating in common emitter followed by a conventional SCHMITT TRIGGER. Figure 25b is the RESET PULSE AMPLIFIER.

In addition to the previously mentioned purpose, the collector of Q_2, in both the COUNT and RESET SCHMITT TRIGGERS is applied to the CLUTCH FLIP-FLOP PULSE GATE. This supplies the required trigger pulses to switch from high to low and low to high tape speed at the correct point in the playback cycle.

Binary Counter

The BINARY COUNTER, constructed from four flip-flops interconnected to form a ripple carry counter, accepts and responds to the pulses derived from the photoelectric read holes via the appropriate SCHMITT TRIGGERS. By counting the holes in the side of the tape, the counter acts as a dynamic memory storing the tape's instantaneous position at all times.

Coincidence Detector

The VERTICAL INPUT specifies the required position on tape in a straight forward decimal representation. This decimal number is converted to a binary number and its complement and applied to the COINCIDENCE DETECTOR. The BINARY COUNTER which holds the actual or instantaneous tape position also outputs this information in the form of a binary

number and its complement to the COINCIDENCE DETECTOR. When the output of the BINARY COUNTER is exactly the same as the output of the DECIMAL TO BINARY CONVERTER we have coincidence and require that the COINCIDENCE DETECTOR indicate this by an appropriate change in its output. The block diagram of a circuit which performs this is shown in Figure 26.

Reducing the process of coincidence detection to its essentials, we find two basic functions. Firstly, coincidence between digits of the same power must be detected and finally the condition when all digits are identical must be sensed. The process of coincidence detection will be explained according to this division of functions.

For the purposes of explanation, consider only the two AND gates and the OR gate concerned with the 8's place input from the COUNTER and the DECIMAL TO BINARY CONVERTER in the top part of Figure 26. The circuitry required for the detection of coincidence for the other digits is identical to that required for the 8's place and therefore the same discussion would apply. Suppose that the 8's place in the BINARY COUNTER is in the "1's" state and the 8's place in the DECIMAL TO BINARY CONVERTER is in the "0's" state. In this case, the upper AND gate would have a "1" and an "0" as inputs. Therefore, the output will be "0". Since the lower AND gate also has an "0" and a "1" for input,

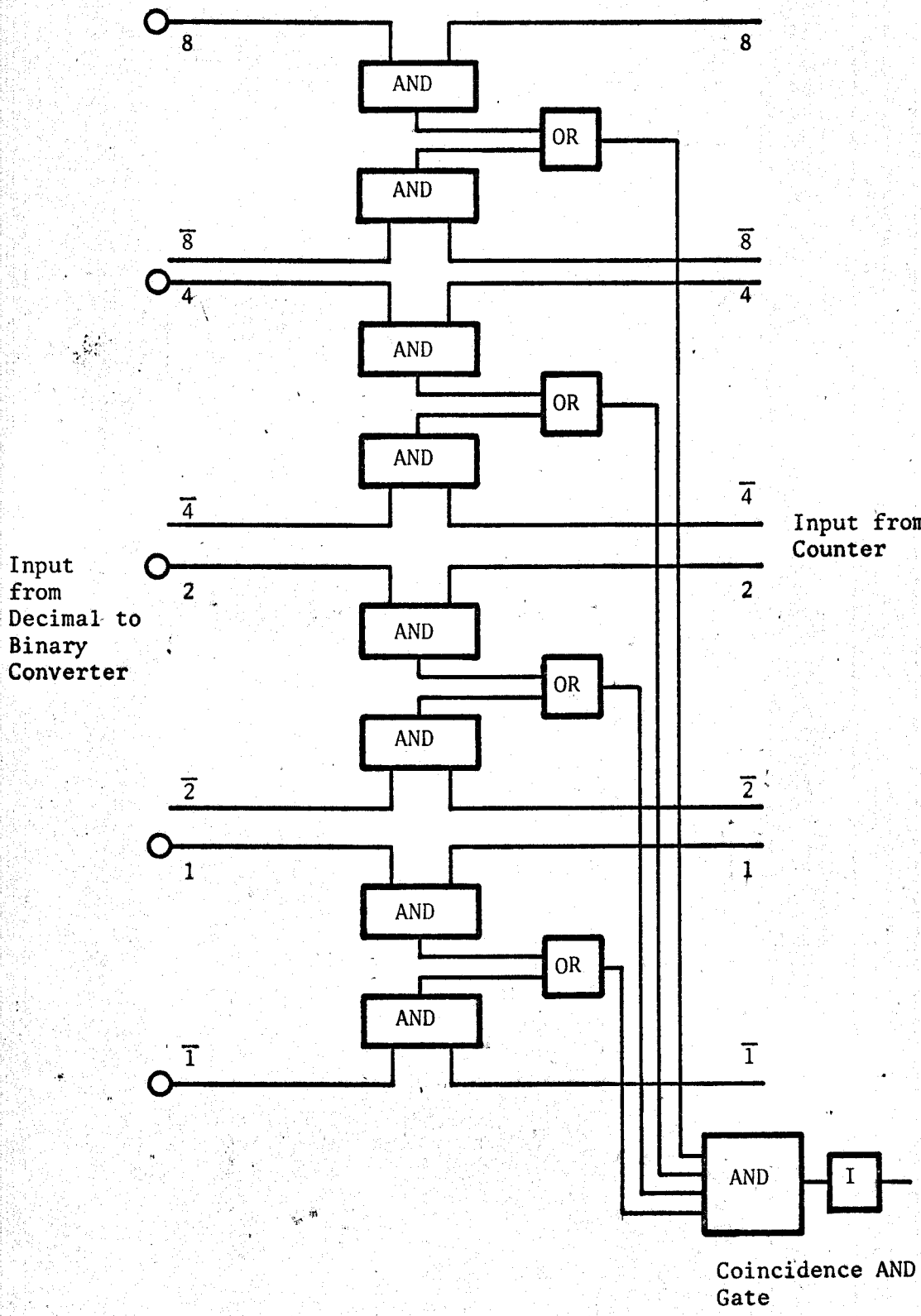


FIGURE 26: BLOCK DIAGRAM OF COINCIDENCE DETECTOR

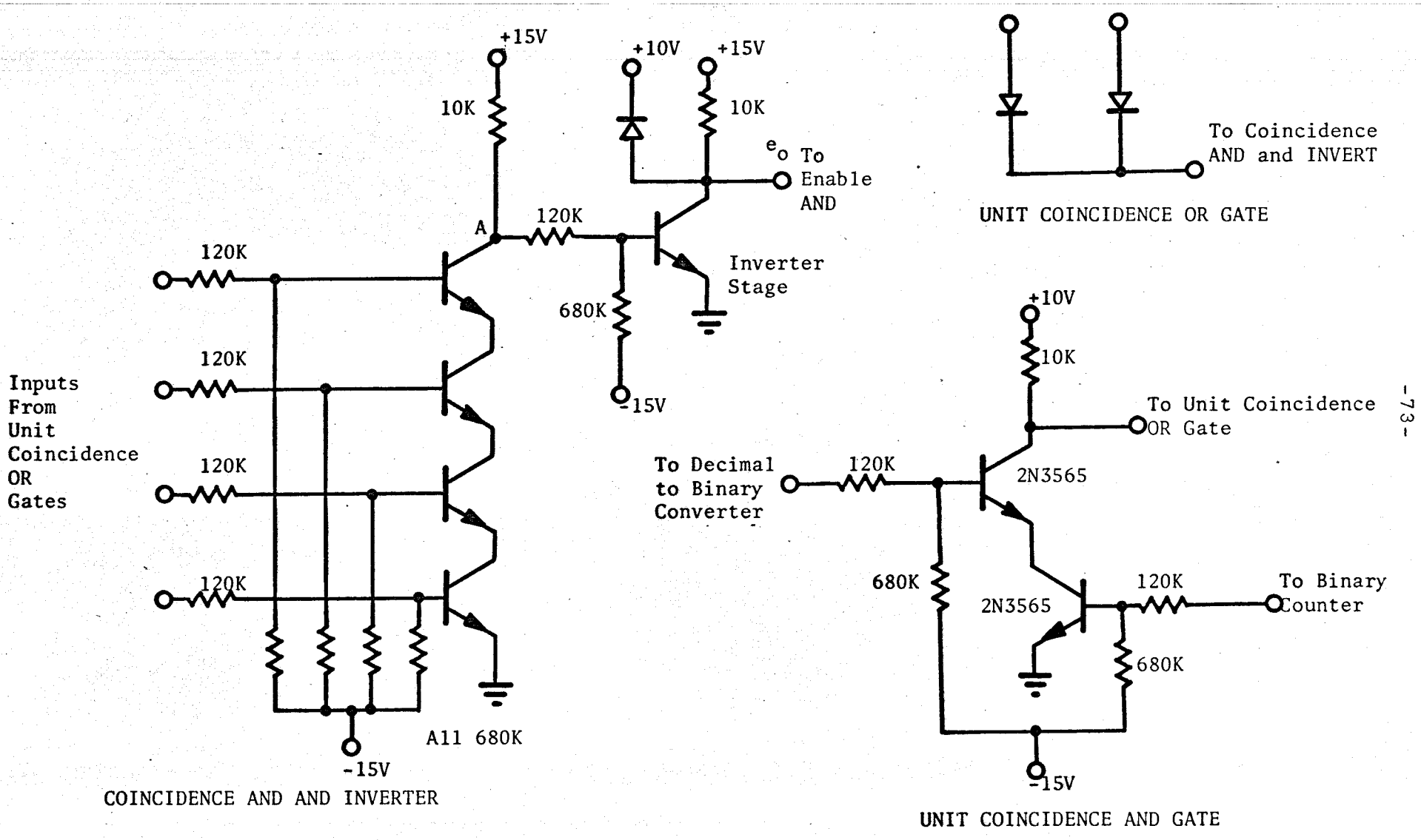


FIGURE 27: COINCIDENCE DETECTOR

it will also have an output of "0". The two AND gates are connected to a common OR gate. Here the OR gate will also be in the "0's" state. By following this line of reasoning for the case where the COUNTER output is "0" and the DECIMAL TO BINARY CONVERTER output is "1", it can be shown that the output of the OR gate will also be "0". This covers the only two possibilities of anti-coincidence. Suppose now that both the binary output of the COUNTER and the DIGITAL TO BINARY CONVERTER are in the "1's" state. The upper AND gate will have two "1's" as input and will therefore have an output to the OR gate of "1". As a result the OR gate will offer a "1" to the COINCIDENCE AND GATE at the bottom of Figure 26. Had the two inputs been "0" on the upper AND gate, the inputs to the lower AND gate would have been "1" since all the inputs to the lower AND of each pair are the binary complement of the inputs to the upper gate. In this case the lower AND gate would output a "1" to the OR gate and the OR will have had a "1's" output to the COINCIDENCE AND GATE.

This process of coincidence detection, on a per digit level, applies equally well to all of the 4 input digits. As each digit achieves coincidence, its appropriate OR gate applies a "1" to the corresponding input of the COINCIDENCE AND GATE. When all the inputs of this AND gate are "1" its output will also go to "1"

The inverter in the COINCIDENCE AND GATE is required to condition the signal to be compatible with the electronics to follow.

In conclusion, e_o from the COINCIDENCE AND GATE will rise to "1" when and only when there is coincidence between the BINARY COUNTER and the DECIMAL TO BINARY CONVERTER.

The circuit diagrams for the gates in Figure 26 are shown in Figure 27.

Enable AND Gate

The purpose of the ENABLE AND GATE is to prevent the commencement of the high speed scan, for the required word, until all inputs - HORIZONTAL, LEVEL and VERTICAL have been made. When the output of the HORIZONTAL OR, LEVEL OR, and the COINCIDENCE DETECTOR are all in the "1's" state - indicating that the location of the required word has been completed - the output of the ENABLE AND GATE will also be in the "1's" state. Here, as in a few other places in the circuit, the logic "1" is 0 volts and the logic "0" is 10 volts. This was done for additional convenience and economy of components.

The output of the ENABLE AND GATE, if in the "1's" state, allows the pulse gate to pass trigger pulses to the CLUTCH FLIP-FLOP in order to accurately commence and control playback.

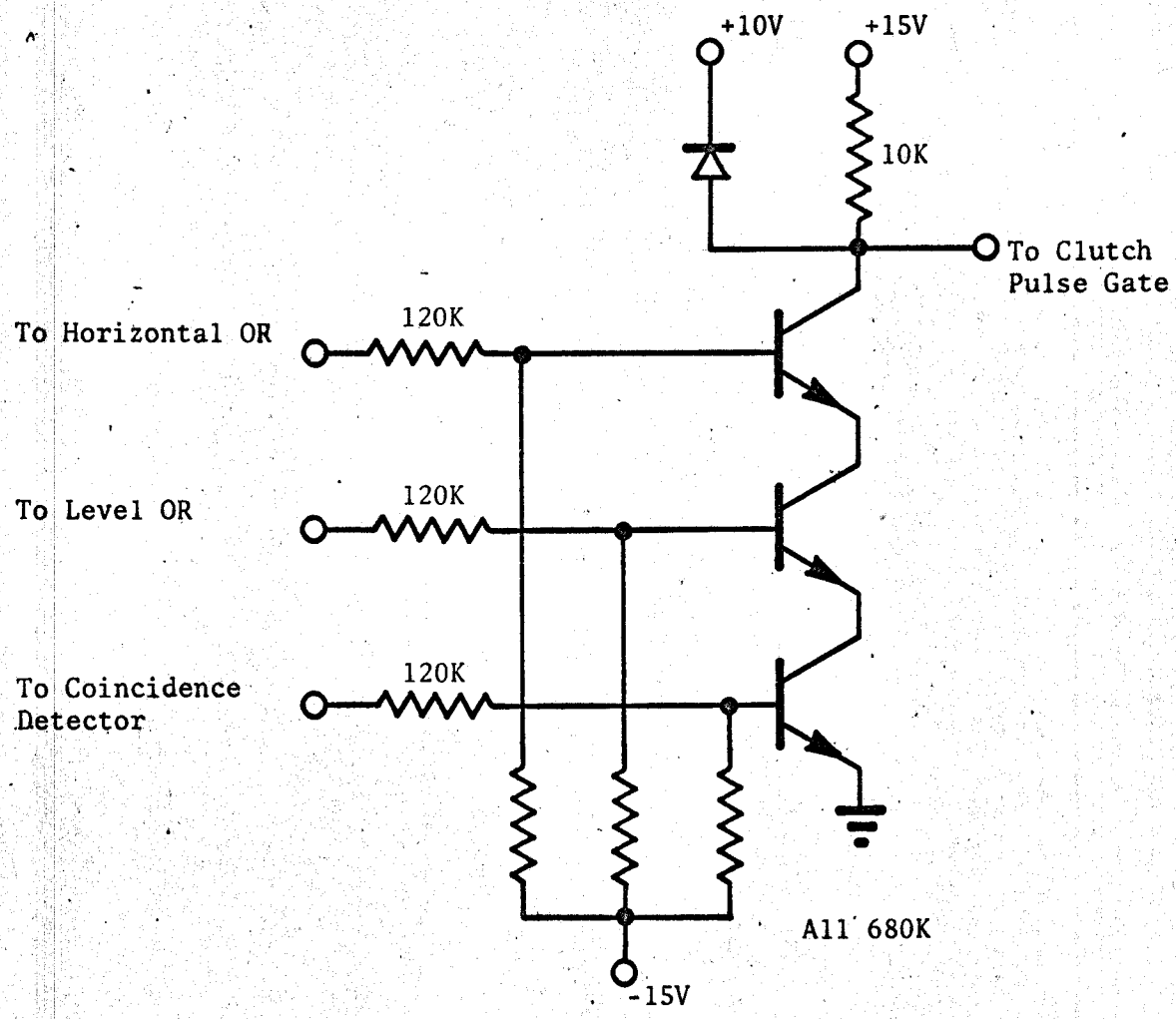


FIGURE 28: ENABLE AND GATE

Clutch Pulse Gate

The CLUTCH PULSE GATE shown in Figure 29 is a multi-purpose circuit. It accepts and conditions pulses from the SCHMITT TRIGGERS to be used for clutch speed control during playback cycle. It also insures that playback or "slow-down" pulses cannot trigger the clutch logic until the required position on tape is reached.

The requirement for two inputs from the SCHMITT TRIGGERS can be explained as follows. The input pulses, after modification, are responsible for initiating slow-down of the tape for playback purposes. Pulses are available on the count line for vertical positions 2 through 10 inclusive. However, there is no count pulse for position 1, since it is reset to position 1. The reset pulse must therefore also be made available to the clutch logic.

The positive output pulses derived from Q_2 are coupled to e_o via D_1. Initiation of playback will occur when a positive pulse appears at e_o. Since this should only happen at the moment of coincidence, Q_1 is utilized to insure this. The output of the ENABLE AND GATE, which resides at +10v during anti-coincidence, saturates Q_1 thus shorting e_o to ground and preventing it from going positive in response to the train of pulses from Q_2. Since counting is achieved on the leading edges of the photoelectric holes and clutch triggering is coincident with the trailing edges of

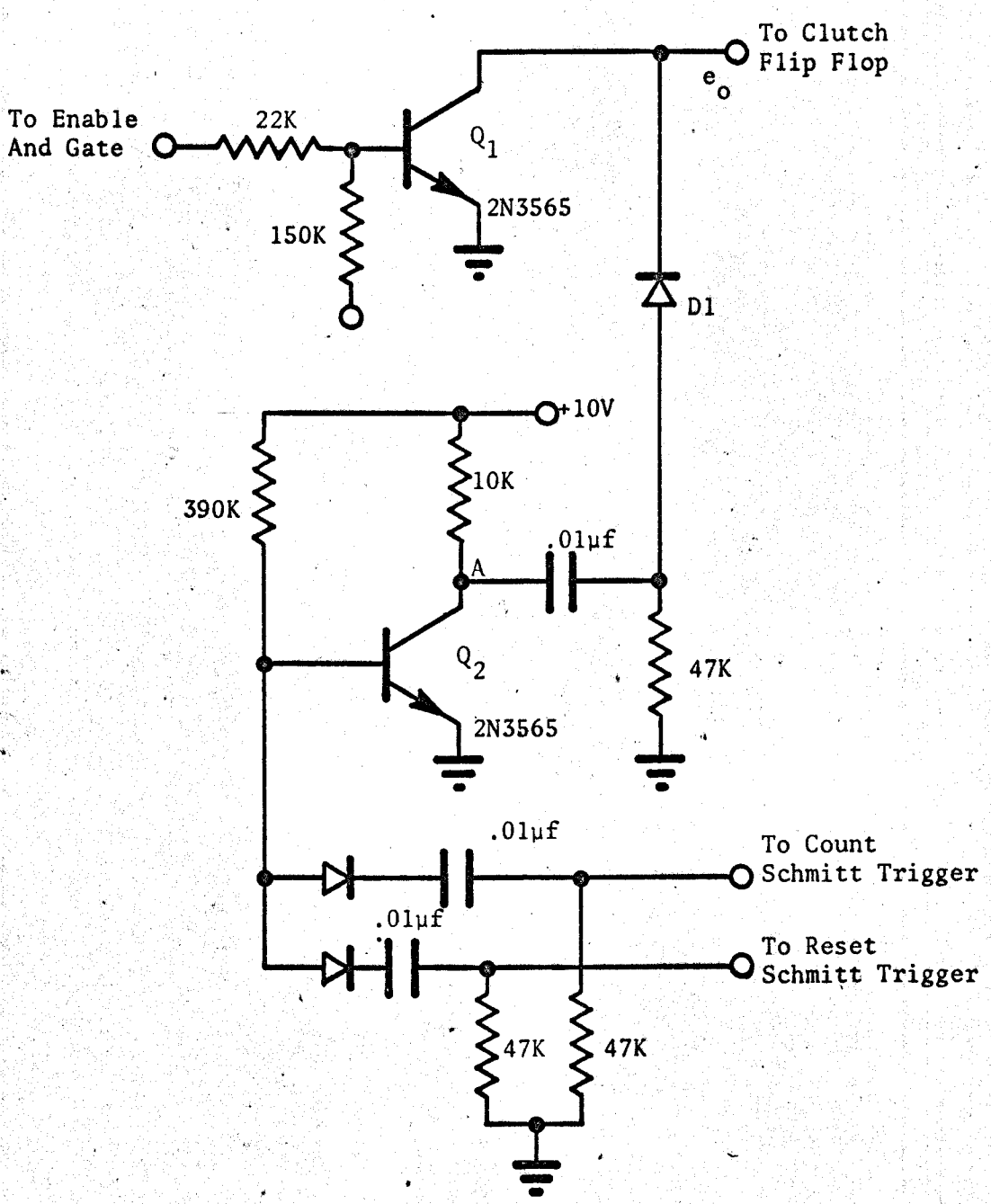


FIGURE 29: CLUTCH PULSE GATE

the holes, the desired address hole on the tape will first advance the COUNTER into coincidence thus cutting off Q_1 and allowing the positive pulse from the trailing edge of the same hole to trigger the slow speed clutch into operation.

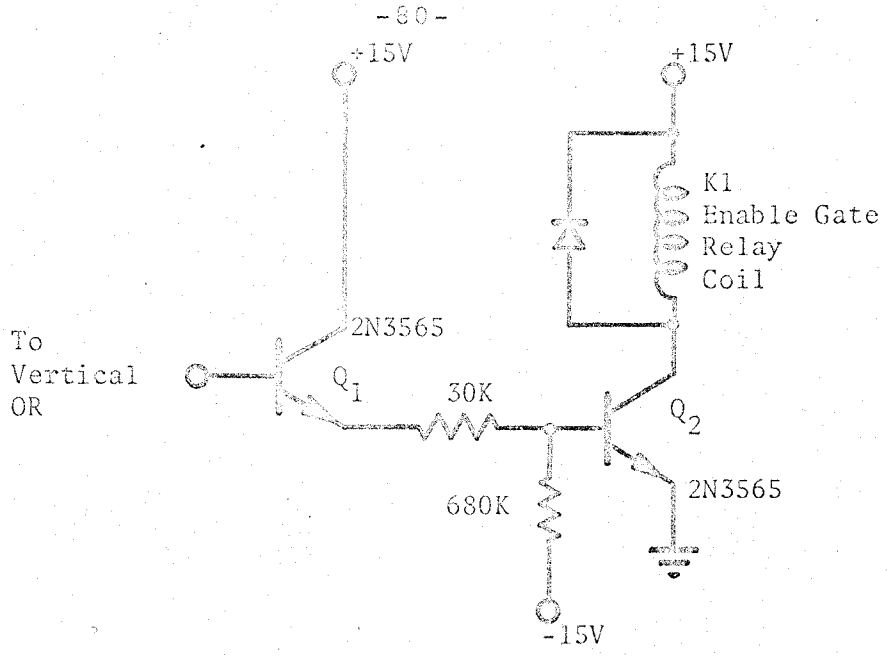
Q_1 is D.C. coupled to the low speed side of the CLUTCH FLIP-FLOP to insure that at the end of a word the low speed clutch is positively disabled long enough to obtain a positive going reset output for buffer reset purposes.

In conclusion, the CLUTCH PULSE GATE and the ENABLE AND GATE allow only the correct trigger pulse to switch the tape from its high speed scan mode to its playback mode.

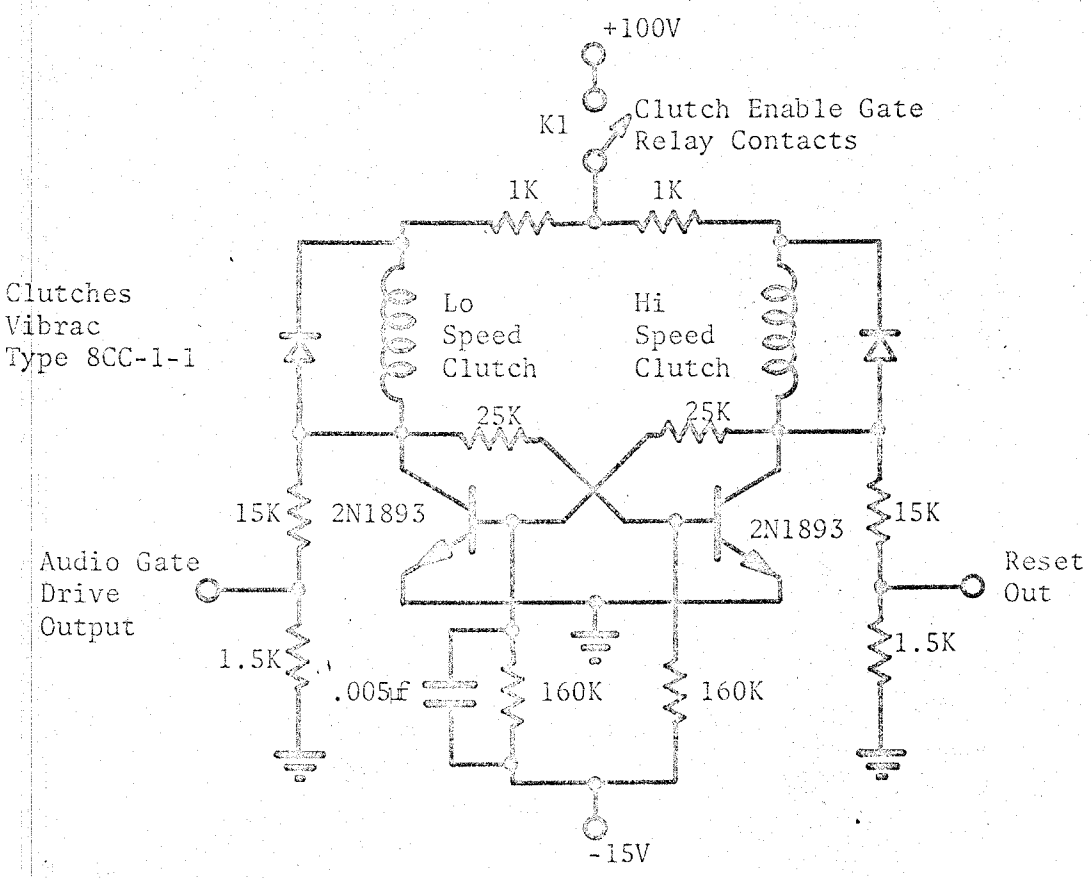
Clutch Flip-Flop and Clutch Enable Gate

It is the purpose of the circuits in Figure 30, the CLUTCH FLIP-FLOP and CLUTCH ENABLE GATE, to actually control the tape speed via the clutches in response to information derived from the selection logic electronics.

The CLUTCH FLIP-FLOP configuration itself is quite conventional. The collector load, however, is not only the clutch but also a 1k series resitor. This technique was used in order to more nearly approach a current source drive for the clutch thus enhancing the operating speed. In a flip-flop, with power applied, either one side or the other mst be conducting. The tape would, in this case, be continually passing ove the heads. Even at very slow speeds, a few days of con-



CLUTCH ENABLE GATE



CLUTCH FLIP FLOP

FIGURE 30: CLUTCH FLIP FLOP AND CLUTCH ENABLE GATE

tinuous running would be sufficient to abrade the oxide coating on the tape beyond usefulness. It is therefore necessary to have the tape at rest when not making an actual selection. This is the purpose of the CLUTCH ENABLE GATE.

The OR gate which samples the DECIMAL TO BINARY CONVERTER controls this gate. If a VERTICAL INPUT is not present both transistors in the gate are cut off and as a result, the ENABLE GATE relay coil is de-energized. Thus, k_1, the ENABLE relay gate is open and both clutches are deactivated and the tape is at rest. However, when a VERTICAL input is applied, the ENABLE relay gate is closed. The flip-flop collector supply of +100 volts is thus applied. When this happens it will always be required that the high speed clutch be engaged. The .005 f capacitor adds sufficient assymetry to the flip-flop to insure that this condition is fulfilled on starting.

It can be seen that two identical voltage dividers are connected from the collectors of the flip-flop to ground. The positive pulse derived from the RESET OUT, during switching from low to high speed at the end of the play out cycle, is used to reset all the input buffers to zero. The AUDIO GATE DRIVE OUTPUT line enables the audio electronics only when required during the record or playback cycle.

Buffer Reset Pulse Amplifier

Since at the termination of a word, in order to avoid "speaking" the same word several times, the input buffers must be set to zero. The BUFFER RESET PULSE AMPLIFIER in Figure 31 does this.

At the termination of a word, the RESET OUTPUT of the CLUTCH FLIP-FLOP goes positive for a brief interval since at this time anti-coincidence exists and the CLUTCH PULSE GATE disables the low speed clutch. This positive going excursion is used to saturate Q_1, thereby dragging all the input buffer collectors to 0v resetting them to the logic "0" state.

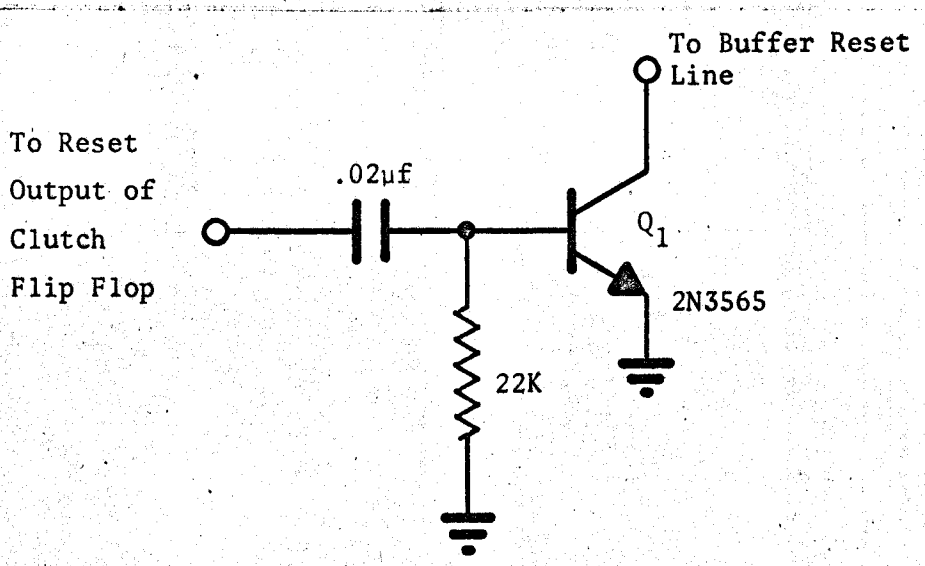
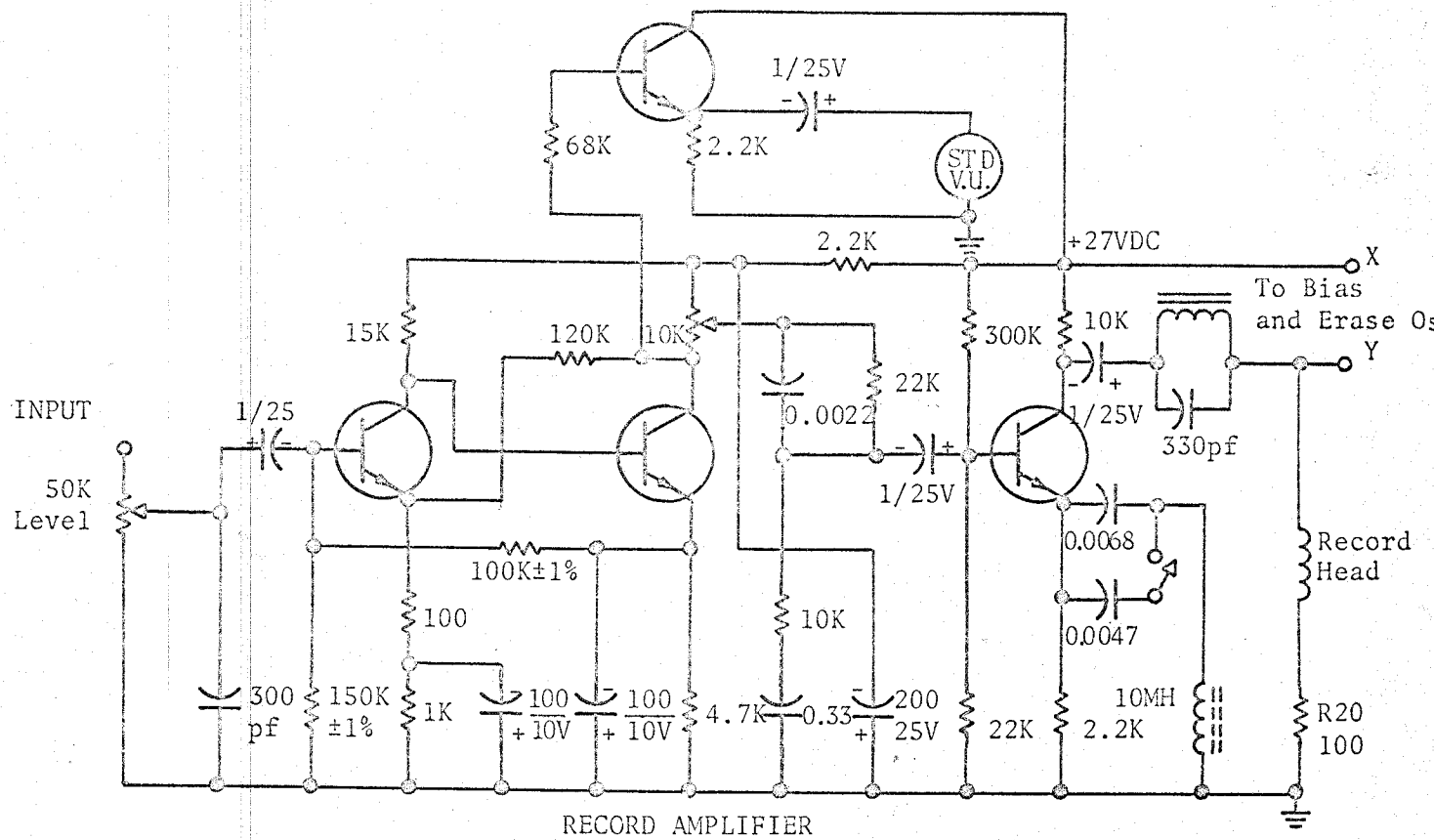


FIGURE 31: BUFFER RESET PULSE AMPLIFIER

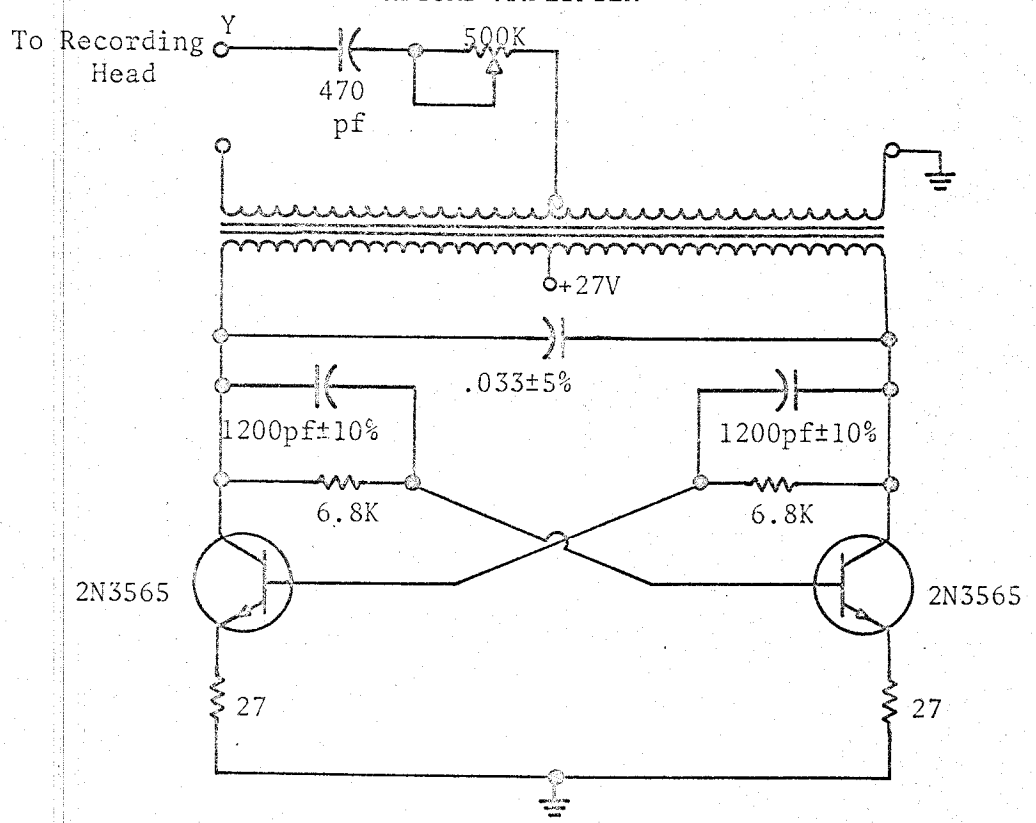
Appendix B

Audio Electronics

Figures 32 and 33 show the record and playback amplifiers, respectively. They were gleaned with little modification from Reference 8.

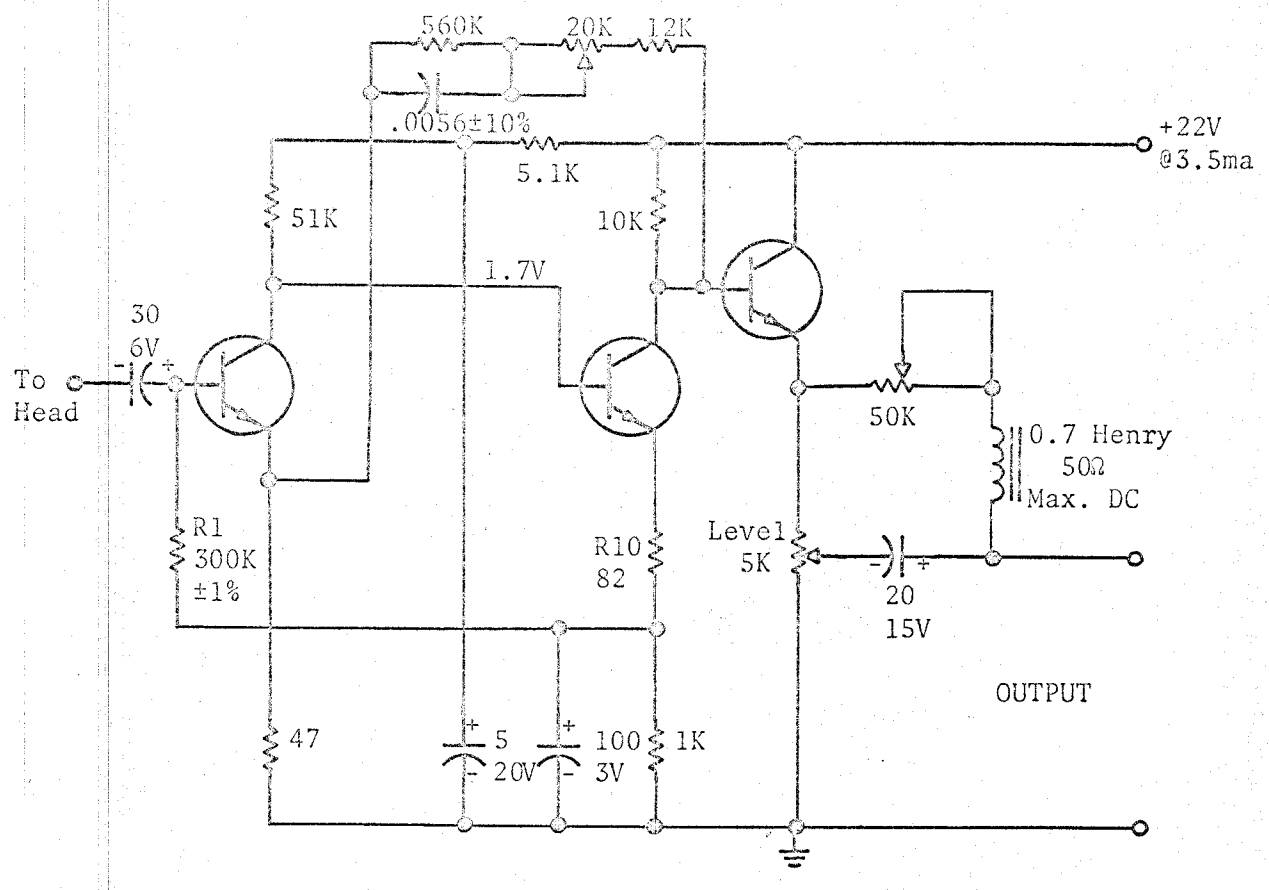


RECORD AMPLIFIER

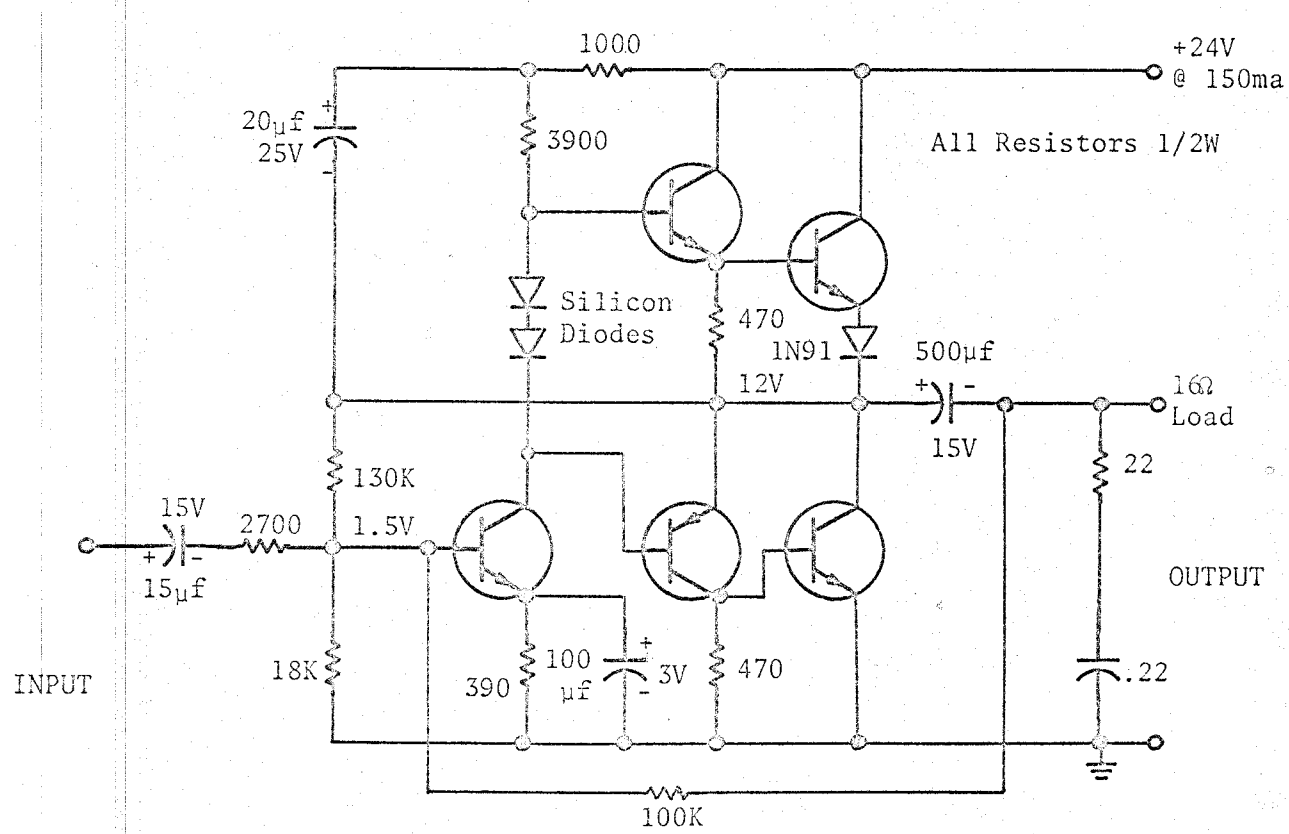


BIAS OSCILLATOR

FIGURE 32: RECORD ELECTRONICS



PREAMPLIFIER



AMPLIFIER

FIGURE 33: PLAYBACK ELECTRONICS

Appendix C

Photographs of System

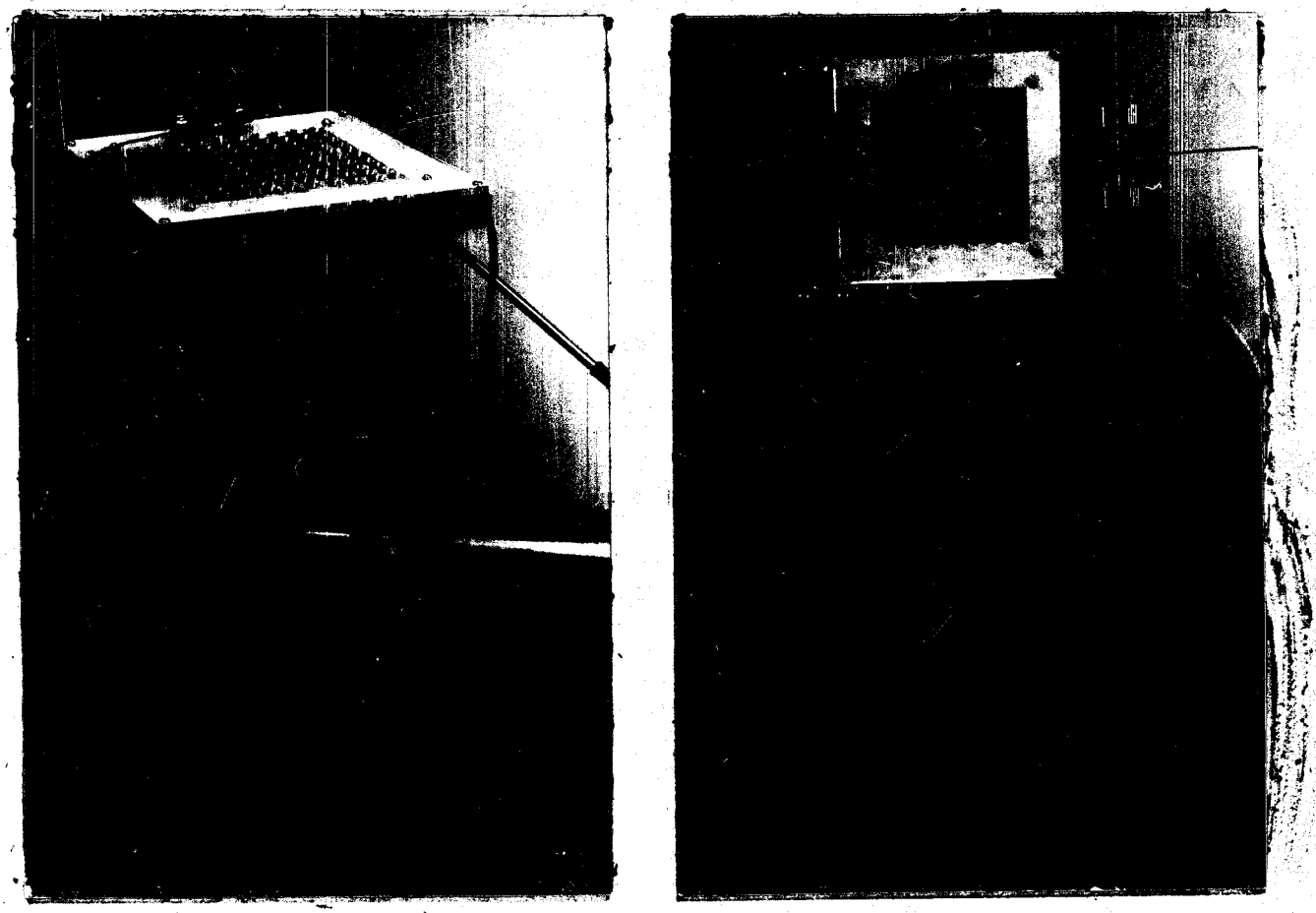


FIGURE 34: WORD BOARD INPUT TRANSDUCER

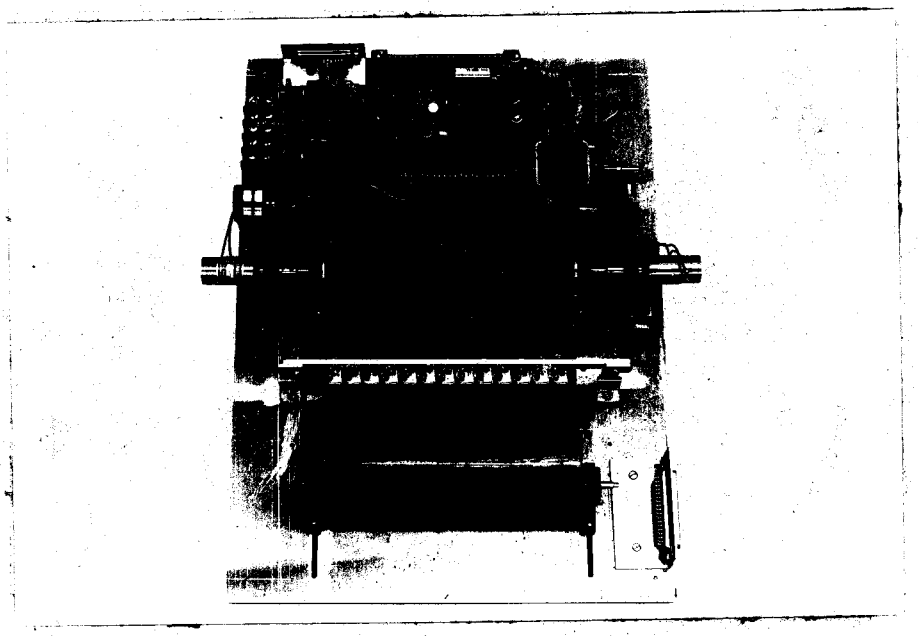


FIGURE 35: PROTOTYPE TAPE DECK

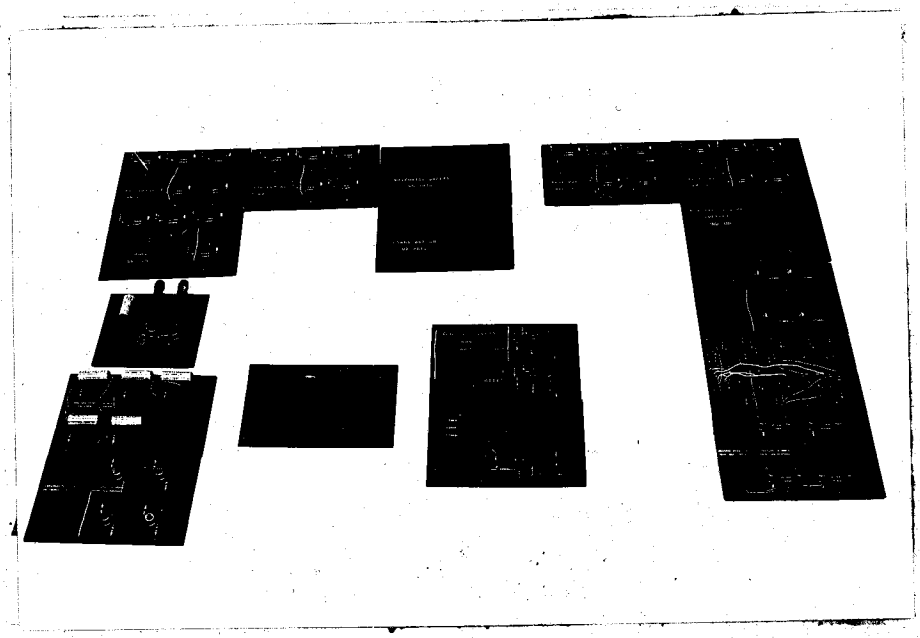


FIGURE 36: PROTOTYPE LOGIC ELECTRONICS

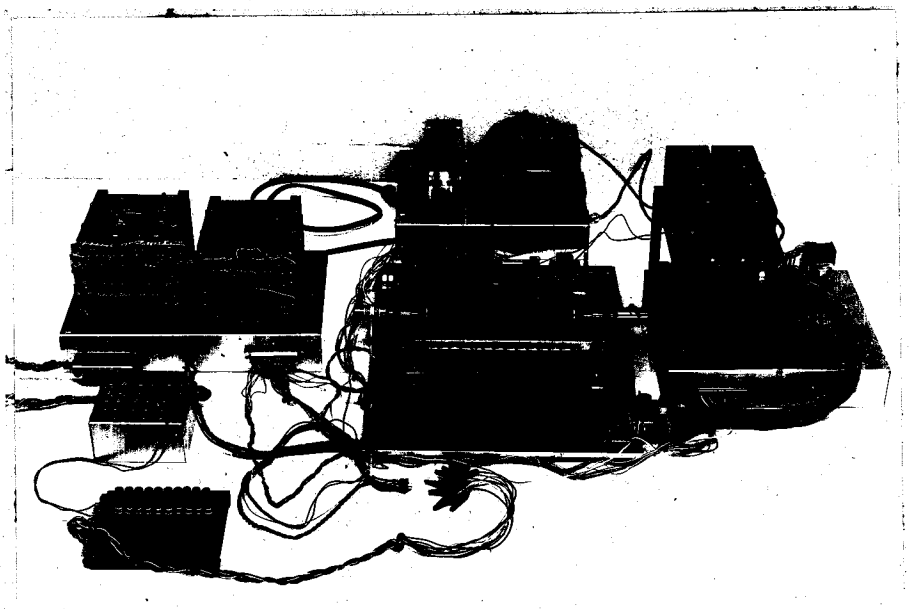


FIGURE 37: COMPLETE PROTOTYPE SYSTEM

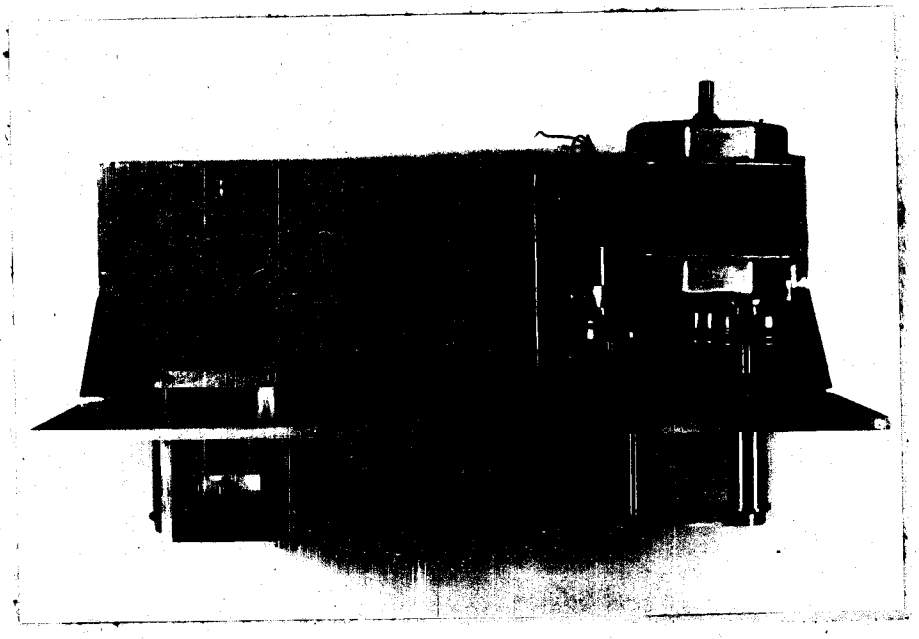
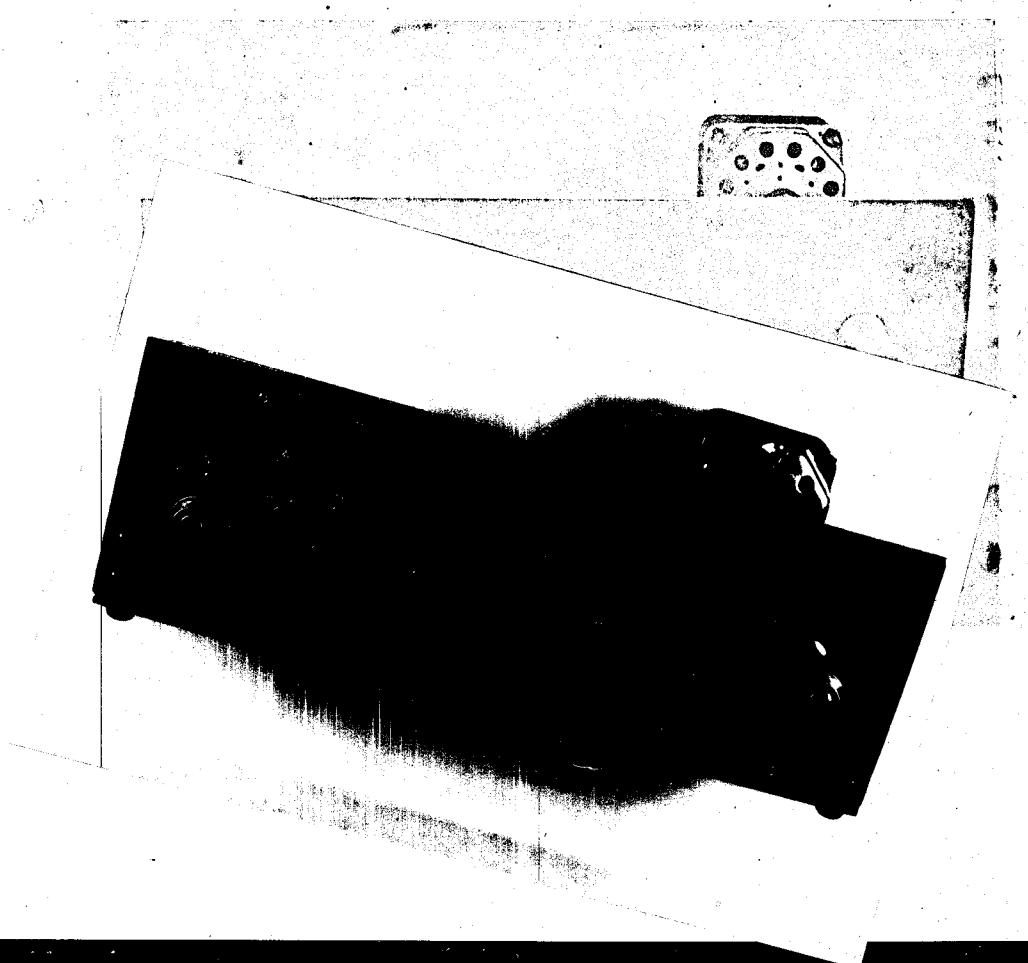


FIGURE 38: TOP VIEW OF IMPROVED TAPE DECK



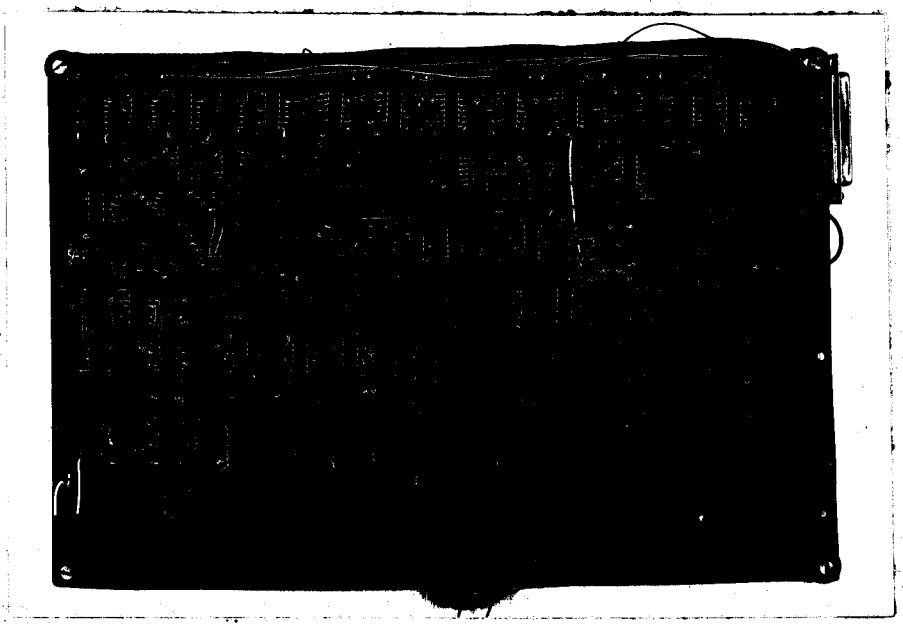


FIGURE 40: INTEGRATED CIRCUIT LOGIC ELECTRONICS

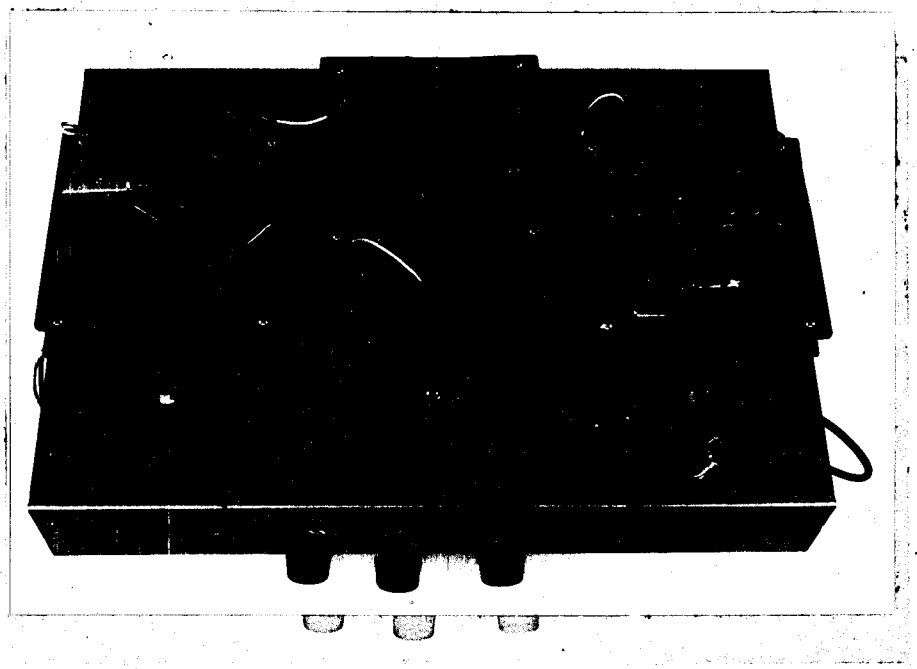


FIGURE 41: AUDIO ELECTRONICS