Single Event Evaluation on 28nm Fully Depleted Silicon-On-Insulator SRAM and Commercial Solid-State Drives

A Thesis Submitted to the
College of Graduate and Postdoctoral Studies
In Partial Fulfillment of the Requirements
For the Degree of Master of Science
In the Department of Electrical and Computer Engineering
University of Saskatchewan
Saskatoon

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ABSTRACT

With the decreasing feature size of ICs, it tends to be more and more sensitive to Single Event Effect (SEE) due to the correspondingly decreasing critical charge. It is significant to evaluate the SEE performance of new technologies and commercial devices, which can provide reference data for the application or hardening design. In this work, the SEE of a common kind of commercial device, SSD and that of a kind of new technology, ST 28nm FDSOI, will be evaluated.

Solid-state drives (SSDs) are widely used in servers, desktops, and portables as storage devices due to their high accessing speed and the anti-vibration performance. Since all of these computing systems carry out critical tasks on a routine basis, it is important to evaluate their single-event (SE) performance to ensure reliability specifications are met by the final product. In this work, two vendors of SSDs were evaluated using alpha particle, pulsed laser, collimated protons and white light neutrons in TRIUMF. The results showed that the micro-controller chip is the most sensitive IC on both vendors of the SSDs. The FIT (Failure In Time. It means 1 error in 10^9 hours. It has no unit) rate of the micro-controller dominated the FIT rate of the whole SSD. The buffer IC is also sensitive to protons but the FIT rate is much lower than that for the controller. The flash and voltage regulator ICs are also sensitive to protons, but the FIT rates are the lowest amongst the components in the SSDs.

ST Microelectronics' (STM) 28-nm Ultra-Thin Body and BOX FDSOI technology has shown robust SEE hardening performance compared to those of 28-nm bulk technologies due to the buried oxide layer (SiO2) between the top transistors and substrate. A triple-modular-redundancy (TMR) SRAM was designed as the embedded high-speed memory for radiation-tolerant ARM processors with STM 28nm FDSOI technology. The single event upset cross-section of the SRAM was tested by using heavy ions with LET=15.0 MeV.cm^2.mg^{-1} in both non-TMR and TMR modes with different accumulated fluence. The SRAM cell was also simulated by using the Cogenda TCAD simulation suite and the cross-section was calculated by using the analytic method. The results showed the cross-section is around 2E-10 cm^2/bit in non-TMR mode, and in TMR mode it varied from one to several orders lower than the non-TMR mode according to the specifically accumulated fluence. As a scrubbing circuit was designed to reduce the accumulated number of SEUs in the SRAM, the cross-section could be low to 5E-17 cm^2/bit, which contributes only negligible errors to the whole system.

ACKNOWLEDGEMENTS

This thesis can't be finished without some other people's help. I appreciate them and would like to say thank you so much!

Firstly, I would like to say thank you to my wife and my kids. When I was busying on studying, preparing experiments or doing other jobs in the University, she always supported me. She did all the housework and took care of the kids. I also want to say thank you for your understanding my kids. Sometime I went home so late and the kids could not see me before they went to bed, which caused they upset. However, after I explained what I was busy on my studying, they said they can understand me and would support me. Thank you so much and I will love you forever.

Secondly, I would like to say thank you Dr. Chen, who is the nicest teacher I have ever seen. Dr. Chen is very rigorous on researching and very patient on teaching us knowledge. Dr. Chen also worked together with me to experiment and gave me important guidance on the data analysis. Without Dr. Chen's help, I could not publish the papers and finish my studying.

Thirdly, I also like to say thank you to Dr. Ko and Dr. Zhang. I attended their classes in different terms and learned lots new knowledge, which opened my eyes.

Finally, I want to say thank you to my class mates and friends who have helped me during my duration in the lab. Without your help, I could not experiment so successfully.

Thank you for all your help and encouragement.

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LIST OF ABBREVIATIONS

DRAM	Dynamic Random Access Memory
DUT	Device Under Test
FDSOI	Fully Depleted Silicon On Insulator
FIT	Failure In Time
FPGA	Field Programmable Gate Array
GCR	Galactic Cosmic Rays
HISEEIF	Heavy Ion Single Event Effect Irradiation Facility
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LET	Linear Energy Transfer
MBU	Multiple Bit Upset
NSREC	Nuclear & Space Radiation Effects Conference
OS	Operating System
PIF	Proton Irradiation Facility
RADECS	RADiations Effects on Components and Systems
SE	Single Event
SEE	Single Event Effect
SEFI	Single Event Function Interruption
SET	Single Event Transient
SEU	Single Event Upset
SHE	Single Hard Error
SOI	Silicon On Insulator
SPE	Solar Particle Event
SRAM	Static Random Access Memory
SSD	Solid State Drive
TCAD	Technology computer-aided design
TID	Total Ionizing Dose
UART	Universal Asynchronous Receiver/Transmitter

1. INTRODUCTION

1.1 Introduction

The development of aerospace technology has not only made mankind out of the earth, but also provided effective tools for mankind to explore and utilize the vast universe. The full development and application of space technology is of great significance to the world's future development.

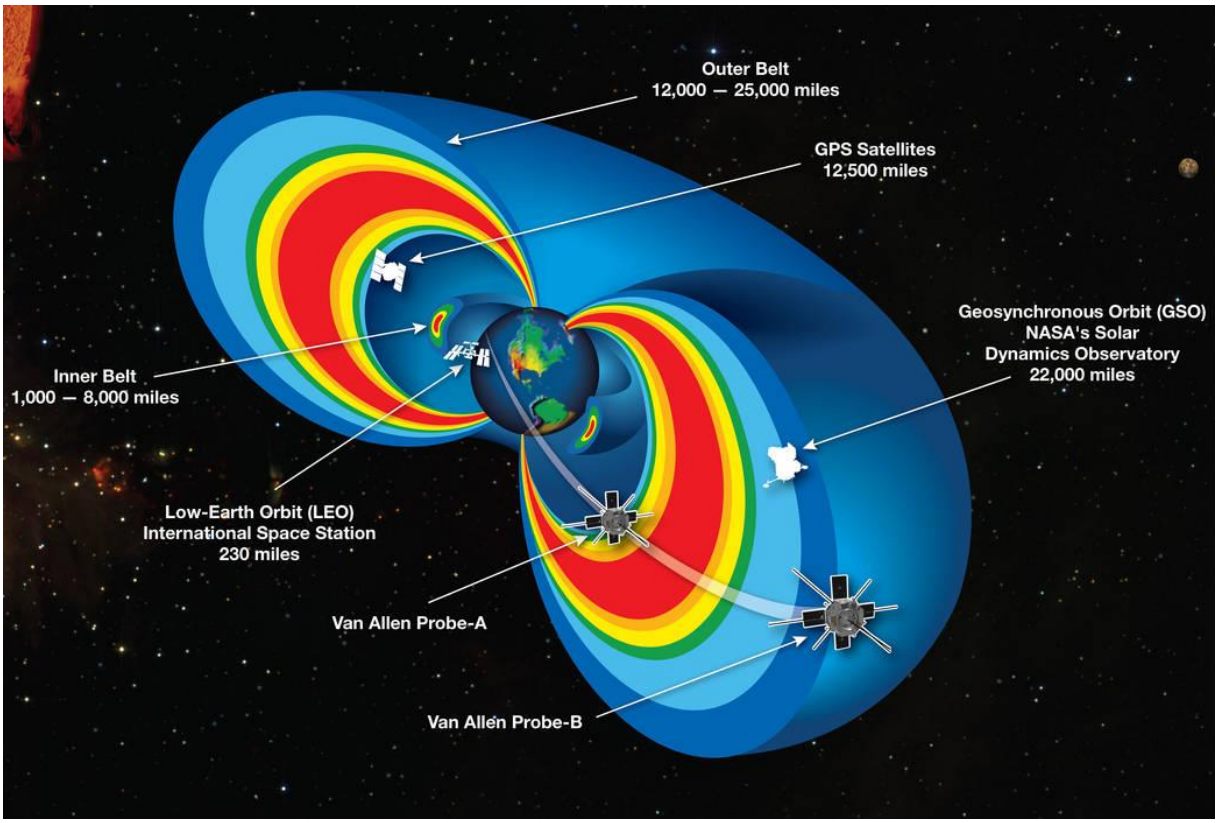


Figure 1.1 The radiation belts outside the earth [1] Copyright © NASA.

However, in the orbit of spacecraft such as satellites, due to the lack of protection of the atmosphere, various high-energy charged particles are likely to cause radiation effect to them. Radiation(shown in Figure 1.1 [1]) in near-Earth cosmic space is mainly composed of three parts: galactic cosmic rays (GCRs), solar particle events (SPEs), and trapped radiation [2]. These rays are mainly composed of electrons, protons, various heavy ions from lithium to uranium, and X-rays

and γ-rays. The composition and energy are different according to the source and orbital level. The intensity of the solar cosmic rays varies with the solar cycle.

The above-mentioned high-energy charged particles can penetrate the bulkhead of the spacecraft, which will not only cause deterioration of material properties but also cause radiation effects of semiconductor devices [3]-[5]. When high-energy heavy ions are incident on the sensitive area of the device, if the charge generated by ionization reaches the device threshold, the logic state of the device will change, forming a Single Event Effect(SEE), which may cause soft or hard errors. Soft errors can cause error in stored data or instructions, and hard errors can permanently damage semiconductor devices. The charge generated by ionization may also be trapped inside the device oxide or the interface between the oxide and the semiconductor material, which causes the device operating voltage to drift. When the amount of charge reaches a certain value, the device permanently fails, which is the Total Ionizing Dose (TID) effects [6], [7] of the semiconductor device. These radiation effects can cause devastating blows to spacecraft with unpredictable consequences.

According to the World Data Center's 40 satellite data from 1971 to 1986 [8], 70% of the 1589 anomaly records were caused by the space environment, and there were 621 Single Event Effects, accounting for 39% of the total 55% of radiation effect failures.

Therefore, one of the important reliable performances that need to be considered before the launch of a spacecraft is the radiation mitigation of the integrated circuits (ICs). In manned spaceflights, it is also necessary to consider the dose absorbed by the astronauts in order to take certain radiation protection measures. In order to ensure the reliable operation of the spacecraft and the health of the astronauts, foolproof when performing missions at critical moments, it is necessary to fully consider the radiation effects after the orbit before the launch of the aircraft and pre-evaluate the error rate of the effects.

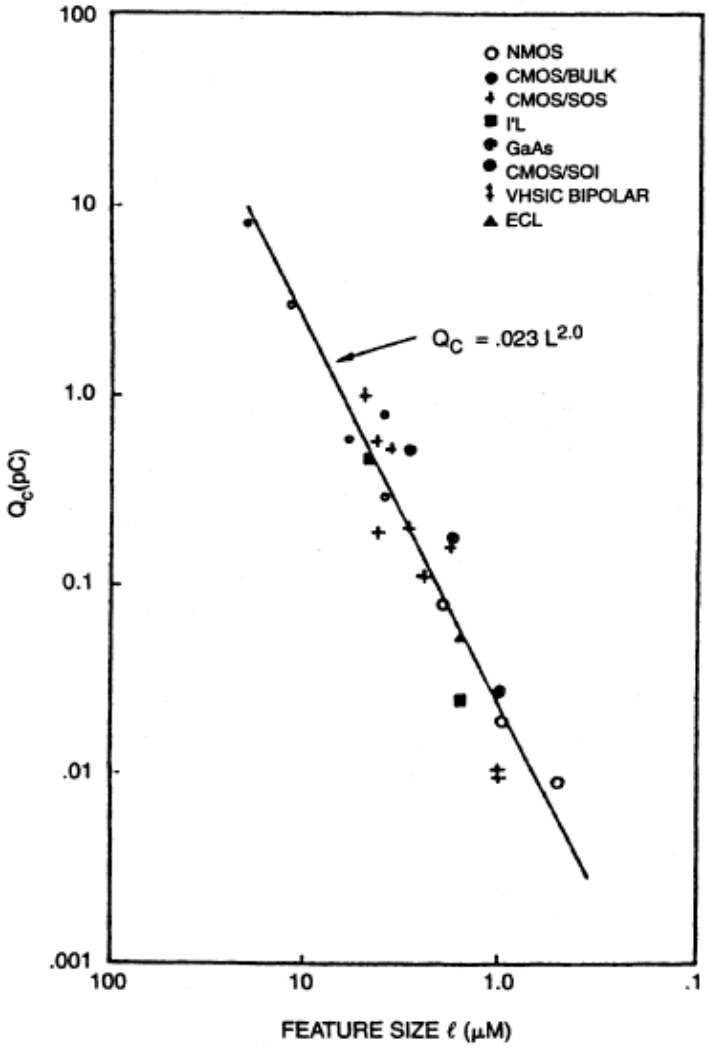


Figure 1.2 Relationship between critical charge and feature size [9] Copyright © 1989 IEEE.

With the development of IC technologies, while new devices are developing towards the trend of low power consumption, high integration, and high processing speed, they have brought even greater challenges to the problem of SEE radiation hardening. The small power consumption trend causes the amount of charge required to store data in the device becoming less and less, which makes the critical charge of the device undergoing SEE continuously decreases, as shown in Figure 1.2 [9]; the increasing integration trend makes the feature size smaller and smaller, which the single ion incidence can cause the SEE probability of multiple sensitive nodes in the circuit to increase significantly, as shown in Figure 1.3 [10]; the requirements of fast processing speed and high operating frequency make the rising and falling edges of the device read and write signals faster

and faster This greatly increases the probability that the SET signal triggers a single-particle inversion or a single-particle function interruption in the circuit, as shown in Figure 1.4 [11]. In nano-scale devices, the above effects are particularly harmful to devices. At present, SEE is not only harmful to electronic equipment in space satellites, but also to aircraft and even ground electronic equipment in the atmosphere.

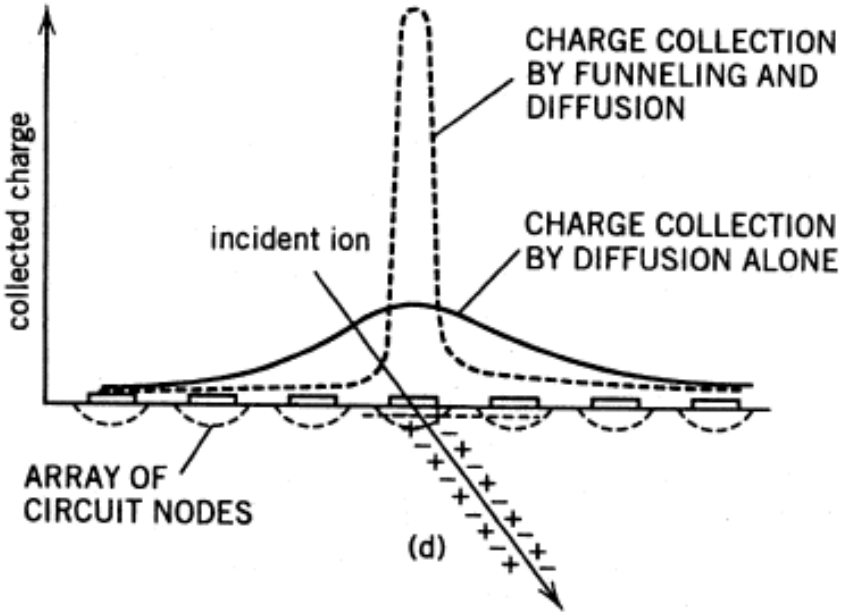


Figure 1.3 Multi-node charge collection in small feature size device [10] Copyright © 1982 IEEE.

Therefore, in order to ensure the safe operation of satellites, aircraft, and even ground electronic equipment, it is necessary to take necessary countermeasures based on in-depth research on the SEE mechanism of semiconductor devices, i.e., radiation hardening. The research on the SEE mechanism of ICs can be carried out by means of space launch and ground simulation tests. Space-borne testing can obtain the chip's SEE data in the real radiation environment of space, but it is limited by the conditions of a long cycle, expensive, a limited number of tests, etc., and it can only conduct a comprehensive inspection of some electronic systems. The ground simulation method can be used to carry out experiments under controlled conditions and investigate various influencing factors, which is conducive to in-depth and systematic research. And combined with the space radiation environment, it can reproduce the SEE situation on the chip. Therefore, ground

simulation is a very cost-effective method, and it is also an indispensable inspection method before the chip is launched into space.

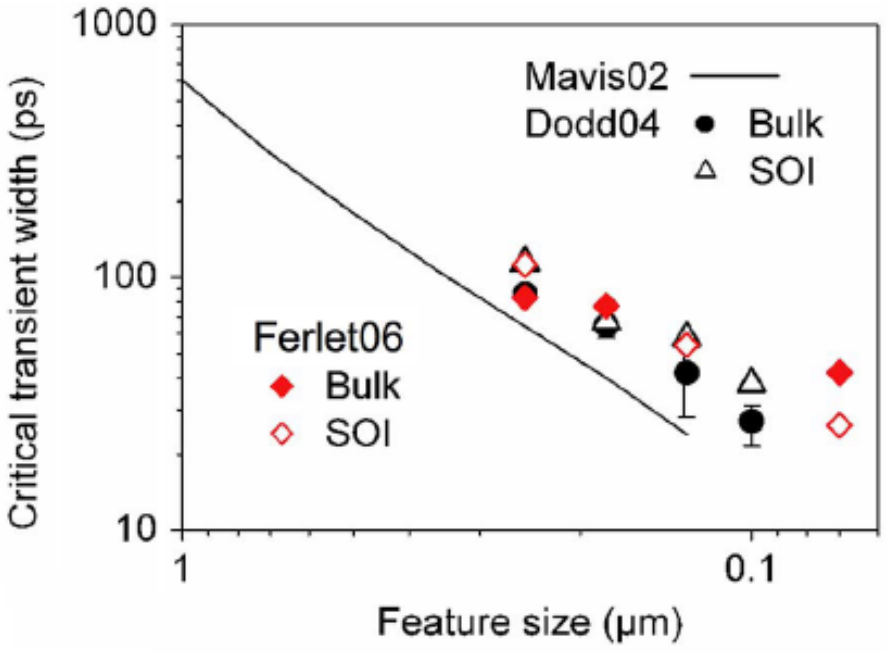


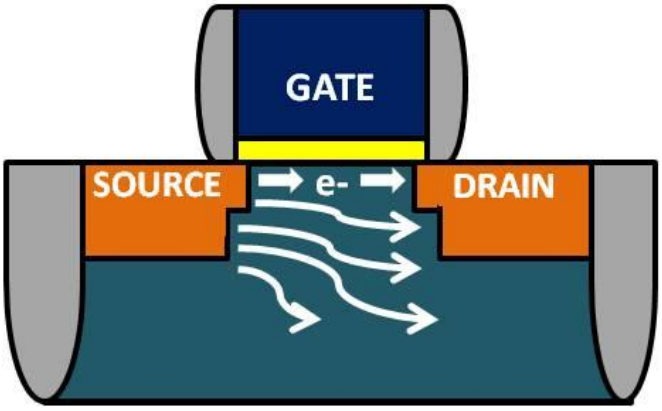
Figure 1.4 Relationship between critical SET pulse width and feature size [11] Copyright © 2010 IEEE.

1.2 Motivation

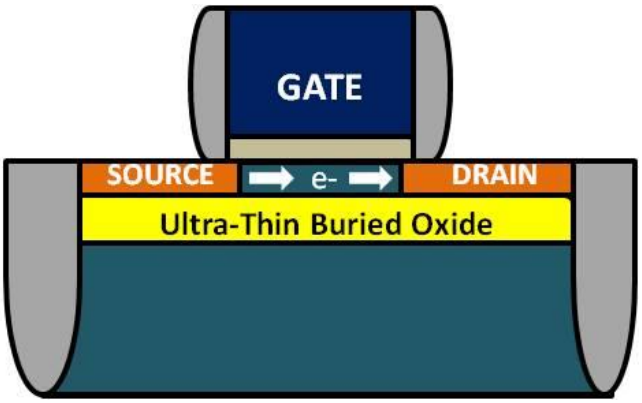
As mentioned above, with the decreasing of the feature size of the ICs, it is becoming more and more sensitive to single ions, such as alpha particles coming from the package material and neutrons in the atmosphere. Some ground level electronic devices begin to be affected by SEE. Such as Solid State Drive(SSD) [12]-[15], which is widely used in portable devices, computers, and cloud storage. Some research results showed it could cause function error or data error once the SEE happened in an SSD, but there is no detailed data for the sensitivity of all kinds of chips on the SSD and how many error modes it has been published. Therefore, it's meaningful to evaluate the SEE error rate and locate the sensitive chip and the sensitive area in it. That kind of data would be significant for hardening design by the designers.

Various SEE mitigation methods have been studied in recent years, such as DICE, TMR, and so on. Some new technology has also been studied, such as Silicon On Insulator(SOI). Nano-meter

technology based on SOI material showed good performance on radiation hardening [16], [17], [18]. The buried oxide between the substrate(shown in Figure 1.5 [19]) and the top layer effectively reduce the charge collection length of the incident ions and also make the devices immune to Single Event Latch-up (SEL) as the parasitic PNPN structure is eliminated [20]. Furthermore the isolation between the transistors is assumed to eradicate the charge sharing between adjacent sensitive nodes. However, some research results showed that some traditional mitigation methods do not work well on the small feature size devices [21], [22]. Triple Modular Redundancy (TMR) has been widely used to mitigate SEE due to its high hardening performance in larger feature size devices in the last few decades. However, references showed the SEU cross-section of the FFs designed with TMR method is only 3.3 times better than those of the regular FFs in 90nm technology [22]. ST Microelectronics' (STM) 28-nm Ultra-Thin Body and BOX FDSOI technology has shown superior performance in terms of SEEs resistance compared to those of 28-nm bulk technologies due to the insolation layer (SiO_2) under the transistors and very thin diffusion layers [11]. To the author's knowledge, there is no data on TMR performance valuation on the FD SOI 28nm technology. Therefore, it's meaningful and necessary to evaluate the performance of TMR in this technology. In this work, an SRAM designed under STM 28nm FD SOI technology and hardened using TMR will be evaluated by using heavy ion beam and simulation.



(a)



(b)

Figure 1.5 Transistor cross-section in a) Bulk technology b) FDSOI technology [19] Copyright © 2018 IEEE.

1.3 Objectives

According to the researching content in this work, the overall goal of the thesis is to study the SEE performance in a kind of commercial device SSDs and SRAM based on ST's FD SOI 28nm technology. The two individual sub-objectives are:

1) study the SEE performance of the SRAM protected with TMR schemes.

Obtaining the cross-section of the presented SRAM chip in both non-TMR and TMR modes by using heavy-ion irradiation experiment and simulation method, then obtaining the effectiveness of TMR in FD SOI 28-nm technology.

2) evaluate the SEE performance of SSDs from different vendors.

Obtaining the error modes and different sensitivity of the components on SSDs by using proton beam, alpha particles, and pulsed laser, and obtaining the difference on SEE phenomenon and sensitivity in different vendors of SSDs using neutron beam. Also try to get the sensitive location distribution in the flipped chips on SSDs using pulsed laser.

1.4 Thesis Organization

This thesis is based on the author's two manuscripts which have been submitted to *RADECS* and *Microelectronics Reliability Journal*. The two manuscripts can demonstrate all the knowledge

that the author has studied during the master studying on SEE mechanism on different integrated circuits (ICs) and SEE testing methods. Each chapter will begin with a brief summary and end with a short conclusion. The main contents and structure of this thesis are shown as follows:

The first chapter gives the introduction of the meaning, motivation, and objectives of the research. Firstly, it gives the endanger of SEE for ICs and it's developing tendency, then presents the meaning of the research contents in this thesis and reports the research status of the contents, finally gives the research objectives of the contents.

The second chapter gives the basic background of the research contents, which includes the nature irradiation source in the atmosphere and its endanger for the ICs. Then introduces the principle of TMR hardening method and mechanism of SEE in SSDs.

Chapter 3 gives the first manuscript on SEE evaluating SSDs. It gives the research status in the world and the innovativeness of this work. Based on the principle of SSDs, different error modes that are caused by the SEEs happened in different chips or working status is analyzed. The testing system and different testing methods were set up to test the SSDs. By using alpha source, pulsed laser, proton beam, and neutron beam, it is found that the most sensitive chip on the SSD is the controller, and the most common error mode in this chip is "hang", which means the SSD system will be stuck once the SEE happened in it. Except that, the firmware could also be damaged and will generate an error mode called "brick", which means the SSD cannot be recovered unless it is refreshed by the factory.

Chapter 4 gives the second manuscript on SEE evaluation for a 28nm FD SOI SRAM. Firstly, it interviews the research status in the world and gives the reason for doing this research. As there is no published data found on the TMR performance under 28nm FD SOI SRAM, and the SRAM is designed as a buffer in a processor chip, so it's important to perform this research to get the data in TMR and get the affection on the processor cores. The SRAM was evaluated by using heavy ions and simulation method. The factors that affect the cross-section were calculated and analyzed. The result shows by using a scrubbing circuit the cross-section of the SRAM can be lower to 10^{-17} cm^2.

In the end, chapter 5 gives the conclusion of the whole thesis, as well as the future research plan.

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2. BACKGROUND

2.1 Basic mechanism of SEE caused by different kinds of ions

When heavy ions get through the sensitive volume of a semiconductor device, they mainly interact with the electrons in the outer layer of the atomic nucleus inside the device, causing them to ionize into free electrons to generate electron-hole pairs [1]. Electron-hole pairs are collected by circuit nodes under the effects of drift and diffusion (shown in figure 2.1 [2]). A current pulse can be generated on the sensitive nodes, which is called Single Event Transient (SET) (shown in figure 2.1 [2]). The charge collected by the nodes via drifting will make the prompt part in the SET curve, while the part via diffusion will make the longer part (shown in figure 2.1 (d) [2]). If the amount of charge collected exceeds the critical charge of the single-particle effect of the device, it will cause a single event effect.

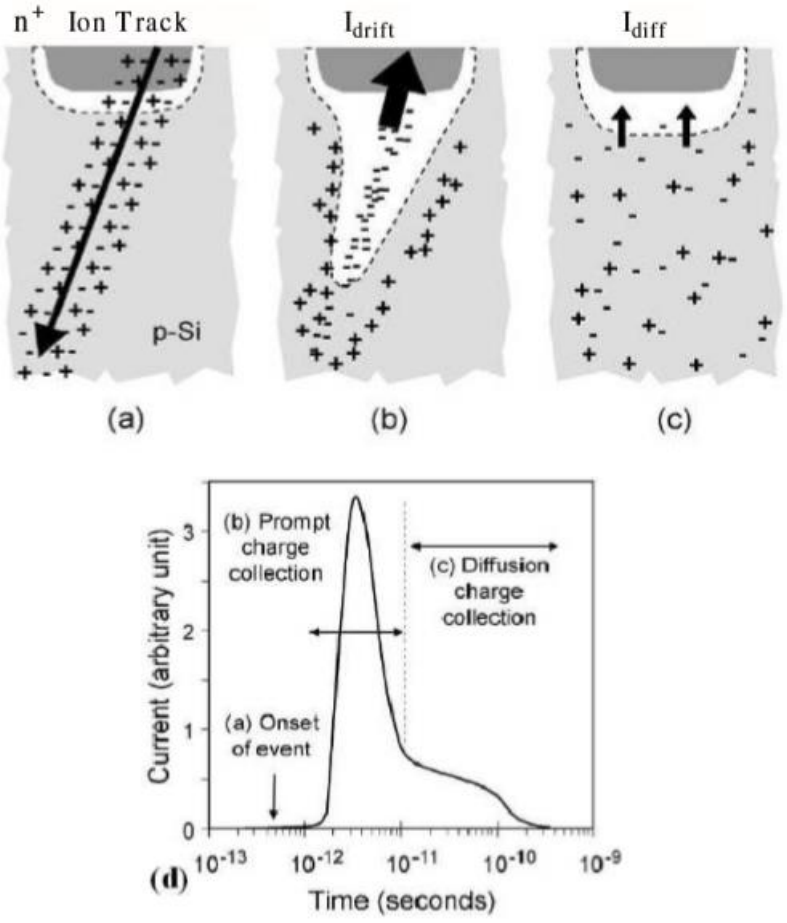

Figure 2.1 Process of (a) charge generation, (b) collection via drifting and (c) diffusion, and the (d) SET generated on the sensitive nodes [2] Copyright © 2005 IEEE.

Since SEE was predicted by Wall market al. [3] in 1962 and confirmed by Binder et al. [4] in 1975, dozens of SEEs have been discovered. Table 2.1 shows several common SEEs.

Table 2.1 Classification of SEEs.

Name	Classification
SET, Single Event Transient [5]	Soft error
SEU,Single Event Upset [6]	Soft error
MBU,Multiple-Bit Upset [7]	Soft error
SES,Single Event Snapback [8]	Soft error
SEFI,Single Event Functional Interrupt [9]	Soft error
SEB,Single Event Burnout [10]	Hard error
SEGR,Single Event Gate Rupture [11]	Hard error
SPDD, Single Particle Displacement Damage [12]	Hard error
SHE,Single Hard Error [13]	Hard error
SEL,Single Event Latch-up [14]	Hard error

When neutrons enter the interior of the device, SEE is triggered mainly by nuclear reactions with target substances, generating secondary heavy ions, which can be a rebound nucleus of the target material or a new nucleus emitted by the compound nucleus [15]. There are two mechanisms for protons caused SEEs: one is through the nuclear reaction with the target material's nucleus to generate secondary heavy ions to ionize and cause SEE [16], and the other is that when the proton energy is located near the Bragg peak, it may ionize the material and deposit enough amount of charge to cause SEE [17]. SEE cross-section is related to the energy of protons or neutrons, while it’s related to the LET for heavy ions.

Lasers mainly interact with the inner layer electrons of the nucleus through the photoelectric effect to generate free electrons to ionize. A single photon can only generate one photoelectron. Usually, a pulse containing a large number of photons is used to simulate the ionization effect of heavy ions [18]. In order to describe the relationship between the ionization ability of a laser pulse and the ionization ability of a heavy ion, the commonly used method is to calculate the equivalent LET value of the laser pulse.

2.2 Irradiation sources commonly used in SEE experiments

2.2.1 Heavy ion irradiation source

Figure 2.2 Heavy Ion Irradiation Facility in China Institute of Atomic Energy [19].

A heavy ion accelerator is used for generating a heavy ion beam. The energy of ions can be high to GeV and the LET is from less than 1 MeV.cm^2.mg^{-1} to around 100 MeV.cm^2.mg^{-1}, which covers the whole range of the LET spectra in the space. The flux of the beam is orders of magnitude higher than that in the space, so it is easy to get a whole cross-section curve in around 10 hours. It's an effective way to evaluate the SEE performance of an IC or get the basic data for on-orbit error rate calculation. In this work, the experiments were carried out in Beijing HI-13 Tandem Van de Graaff Accelerator, which locates in China Institute of Atomic Energy (CIAE) [19]. The irradiation chamber is shown in Figure 2.2.

2.2.2 Proton irradiation source

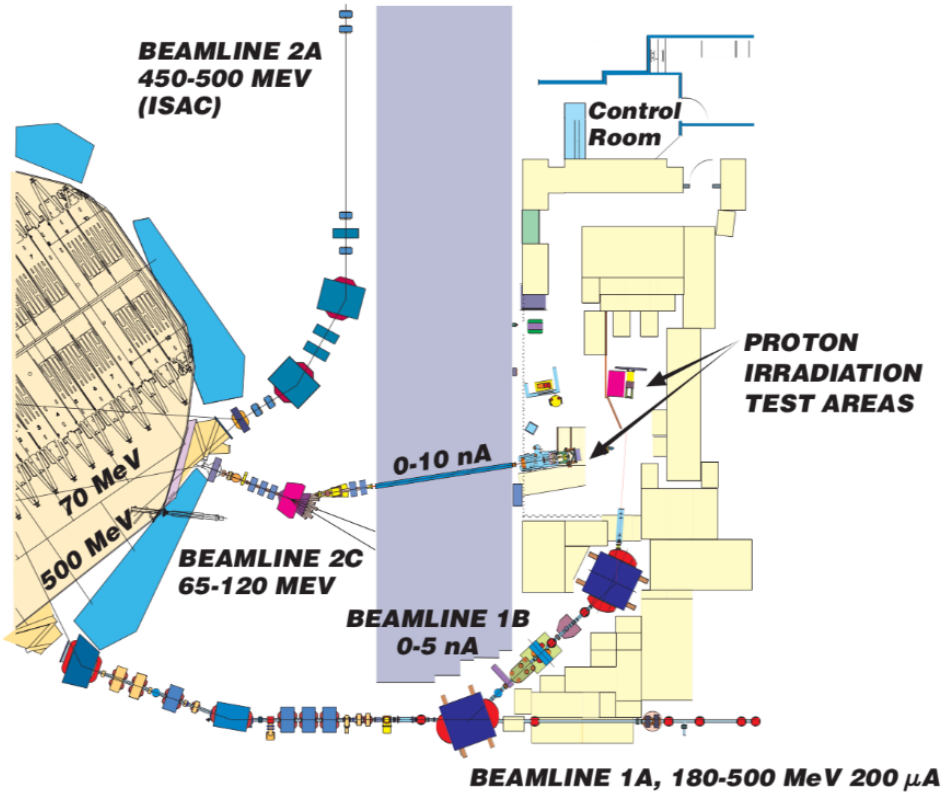

Figure 2.3 Layout of the PIF lab in TRIUMF [20] Copyright © TRIUMF.

Proton beam is also generated by an accelerator. The energy can be from several MeV to hundreds of MeV, which is much lower than the highest energy of protons in the space. However, for most of the ICs, the cross-section will be saturated when the energy is around 100 MeV. The similarity between the proton beam and the heavy ion beam is both of them are monoenergetic, so it's easy to test the cross-section versus LET or energy. In this work, the experiments were carried out in the Proton Irradiation Facility (PIF) of TRIUMF in Vancouver [20]. The layout of the lab is shown in Figure 2.3 [20].

2.2.3 Neutron irradiation source

A neutron beam can be generated by nuclear reactors (fast neutrons), spallation neutron source (white light neutron) or accelerators(wide energy range). However, as there is no charge on neutron, it cannot be accelerated directly; it only can be generated by hitting a target by proton beam. Quasi-single energy neutron source can be generated by hitting a thin target, while white light(continuous energy distribution) neutron beam can be generated by hitting a thick target. The energy spectra of

the white light neutron beam is very similar to the atmosphere neutrons. As when the energy is higher than 50 MeV, the cross-section of neutron and proton can be looked equivalent, people usually use a monoenergetic proton beam to measure the cross-section for specific energies and use a white light beam to verify the total cross-section under various energies neutrons. In this work, the neutron experiment is also carried out in the PIF of TRIUMF. Bl1B was used in the experiment. Figure 2.4 shows the neutron energy spectra of BL1B, BL2C and three JEDEC (Joint Electron Device Engineering Council) models [21].

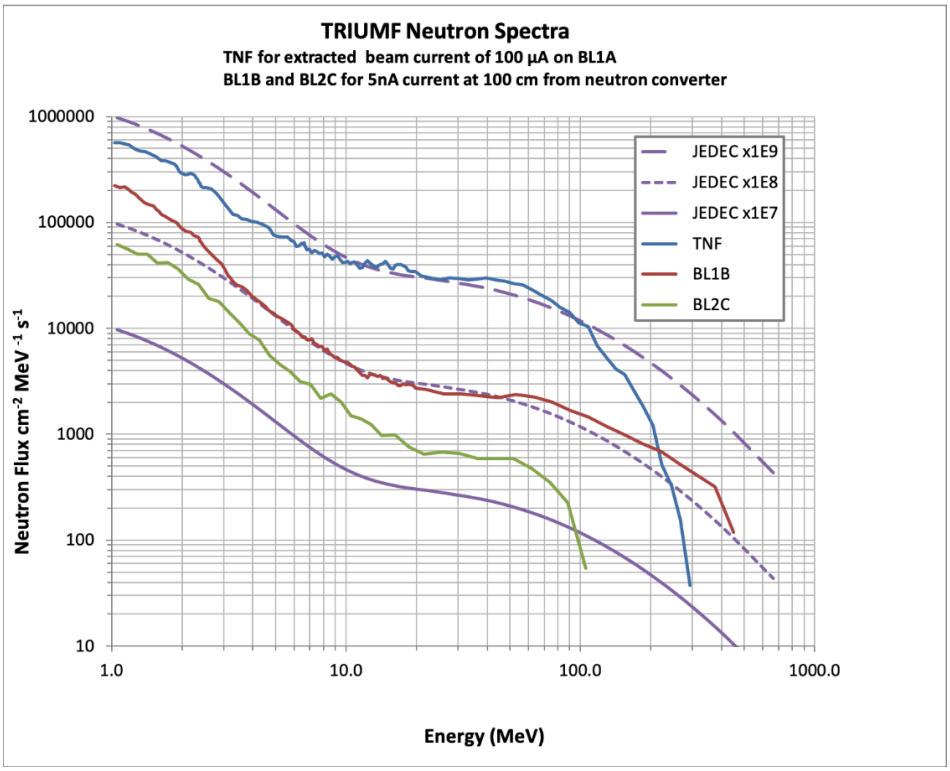

Figure 2.4 TRIUMF neutron spectra [21] Copyright © TRIUMF.

2.2.4 Alpha source

Alpha particle is nuclear of Helium. Some natural material can decay and emit alpha particles, such as Americium 241. The biggest energy peak of the alpha particles is 5.486 MeV, which takes up 85.2%. The range in silicon of the alpha particles is around 27.9 µm, while the thickness of the dead layer of the ICs is around 10~20 µm. Therefore, in most case, it can penetrate the dead layer and get through the sensitive layer. The LET of the alpha particle with 5.486 MeV energy is 0.5 $MeV.cm^2.mg^{-1}$. In addition, the main advantage of the alpha source is it needn't accelerator and no beam time limitation. The dose rate of the alpha source can be realized by painting different

concentration of Americium 241 in a copper plate. We have two kinds of alpha sources. They are shown in Figure 2.5.

Figure 2.5 Alpha sources with different dose rate

2.3 SEE mechanism and testing method for SRAMs and SSDs

2.3.1 SEE mechanism and testing method for SRAMs

The SRAM presented in this work was designed as an embedded buffer in a chip with several processor cores (shown in Figure 2.6). The cores were designed with different mitigation methods. To evaluate the cores accurately, the SRAM was mitigated using TMR to reduce the effect on evaluation of the cores. As there was no published data found on the performance of TMR in STM 28-nm FDSOI technology, it's necessary to test and evaluate the SEE performance of the SRAM.

An SRAM contains storage circuits, address decoding circuits and I/O circuits. As the area of storage is much larger than the other two kinds of circuits, most SEUs happens in the storage. However, it can also generate lots of SEUs if the SEU happens in the peripheral circuit. For the standard circuit of the storage cell, it includes six transistors, as shown in Figure 2.7 [22]. If a heavy ion hits the OFF transistor in either invertor, it may cause SEU, which can cause the storage data to become 1 from 0 or become 0 from 1. Therefore, to test if there is any SEU happening in the storage circuits, a specific data, such as 00, 11 or 01, need to be written into the SRAM first and

then read it back and compare it with the original data. If there is any error, that means SEU happens. For SRAM testing, there are two ways of testing, dynamic and static. The previous one means keeping on writing and reading cycle during the irradiation process, while the latter one means writing specific data into the SRAM before the irradiation, then irradiate it, and read back the data after the irradiation is finished. In this testing mode, the effect of the peripheral circuit is excluded.

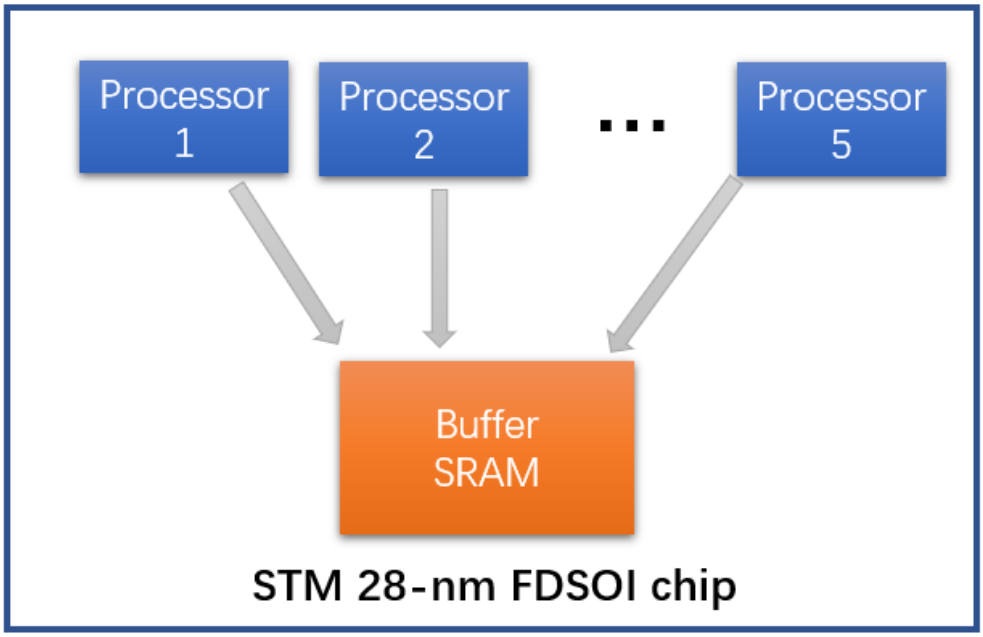

Figure 2.6 The schematic of relationship between the SRAM and the processors

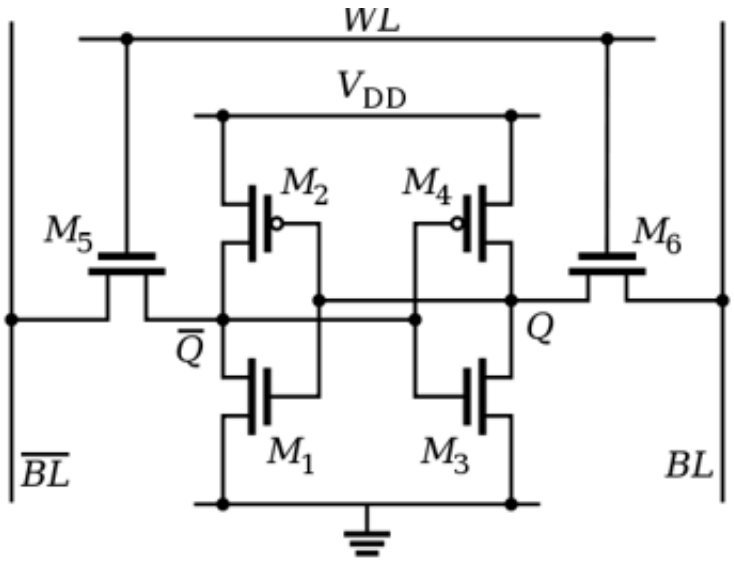

Figure 2.7 Circuit of standard 6-transistor SRAM cell [22]

2.3.2 SEE mechanism and testing method for SSDs

SSD now is a kind of popular commercial device which is widely used in portable devices, communication devices, and computers. The mechanism of SEE for SSDs is much more complex than SRAMs as it is a system that contains storage chip (FLASH), processer (controller), buffer (DRAM) and power related chips. There were very few published papers on the irradiation effects of SSDs. To the author's knowledge, only one conference presentation [23],one published paper [24], one conference paper [25] and one report [26] were found. In reference [23], they found the main effect for SSDs is no-responding, i.e. hang. The uncorrectable data errors were less frequent. In reference [24], the effect on data error of hang was evaluated. A large number of errors were found after the hang and the SSD was rebooted, which is the so called silent error. In reference [25], different kinds of error modes were tested based on the controller chip. The results showed SEE in the controller can not only cause hang but also can cause brick, which means the firmware was damaged and it still did not work after reboot. However, in all the above works, the cross-section (or FIT rate) of different chips on SSDs, such as controller, buffer, flash, and voltage regulator chips, were not provided, so it's difficult to evaluate the contribution of each chip on the total cross-section. In this work, we will test each of them separately and evaluate the FIT rate of each of them.

An SSD mainly consists of controller chip, buffer chip (DRAM), storage chips (flash) and voltage regulator chips. It was supposed that the flash chips were sensitive to irradiation. However, previous research showed that the FIT rate of the flash chip for alpha particles and neutrons was very small [27], [28]. The reason for that is an Error Correction Code (ECC) is designed in the SSD to solve the wearing out the problem for the FLASH. That also works effectively for SEU correction. The function of the controller chip is to control all the behaviors, such as data reading/writing, firmware loading and so on. It's very sensitive to radiation and the most possible error is Single Event Functional Interrupt (SEFI) [25]. The function of the buffer chip is to store data or firmware temporally. It was supposed to be very sensitive to irradiation and may cause SEU. However, from our results, it is less sensitive than the controller and there is only SEFI observed. The power related chips are even less sensitive than the buffer. There are also power related chips on SSDs. According to our previous research, the SET generated in power related chips can cause system function error, such as reboot. Therefore, the voltage regulator chips were also tested in this

work. The result showed they are also sensitive to irradiation although the cross-section is lower than other chips on SSDs.

According to the error modes analyzed above, there should be SEFI and SEU testing functions in the SSD SEE testing system. As most of the SSD testing software only can test the performance, such as reading speed or writing speed, rather than data error testing, a dedicated program was developed to test the SEE for SSDs. The main principle of the program is writing specific binary data, such as 00, 11 or 01, into the SSD, then read it back and compare it with the original data to check if there is any SEU. It can write named specific binary data into the SSD and test SEUs in either reading only, writing only or both reading and writing mode. It can also show the error if there is any function error. The interface of the testing program is shown in Figure 2.8.

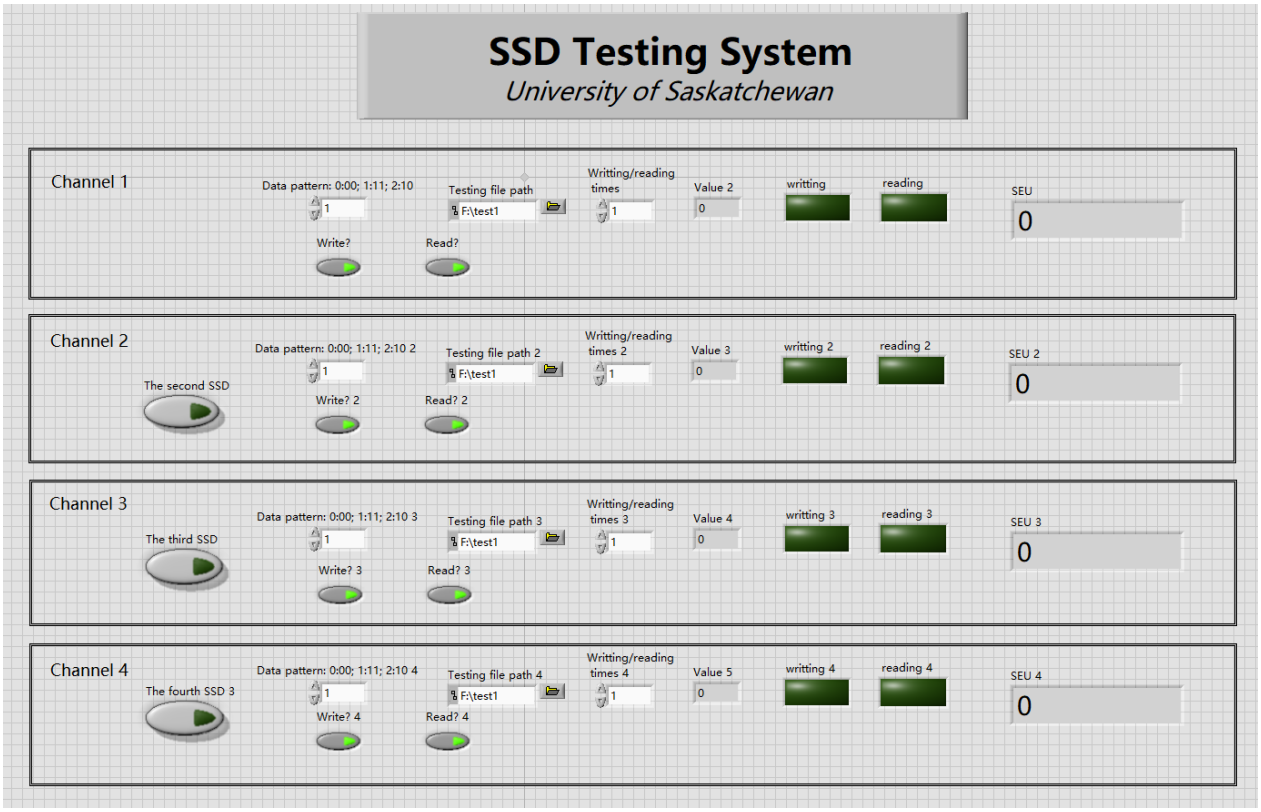

Figure 2.8 Interface of the SSD SEE testing program

To compare the testing data obtained by different programs, another open source program named Fio [29] was also used to test the SSDs. Fio is a professional testing program on the performance of I/O testing of hard drives in different operation modes. It can write and read data into/out an SSD in assigned file size, buffer size, writing/reading speed, and so on. As we were

only interested in the irradiation effects of SSDs rather than the performance of the hardware, we only used the function of data writing and data reading and the related functions.

This program runs better in Linux OS and the user interface is command line mode. As Labview runs only in Windows OS and we need to switch the OS remotely during the experiment, a VMware program was used to make a virtual Linux OS under Windows OS, thus the two OSs can be switched easily. The interface and one of the examples of the command line is shown in Figure 2.9 and one of the sample output is shown in Figure 2.10.

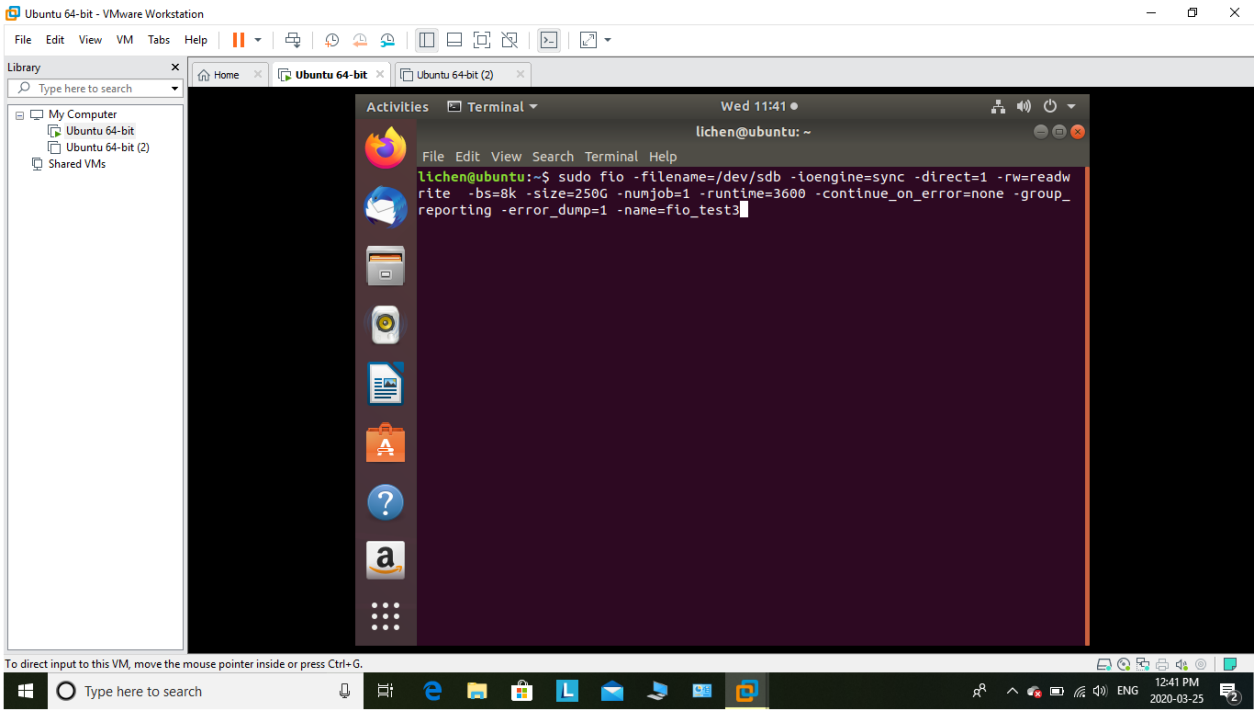

Figure 2.9 Interface and sample command line of the Fio

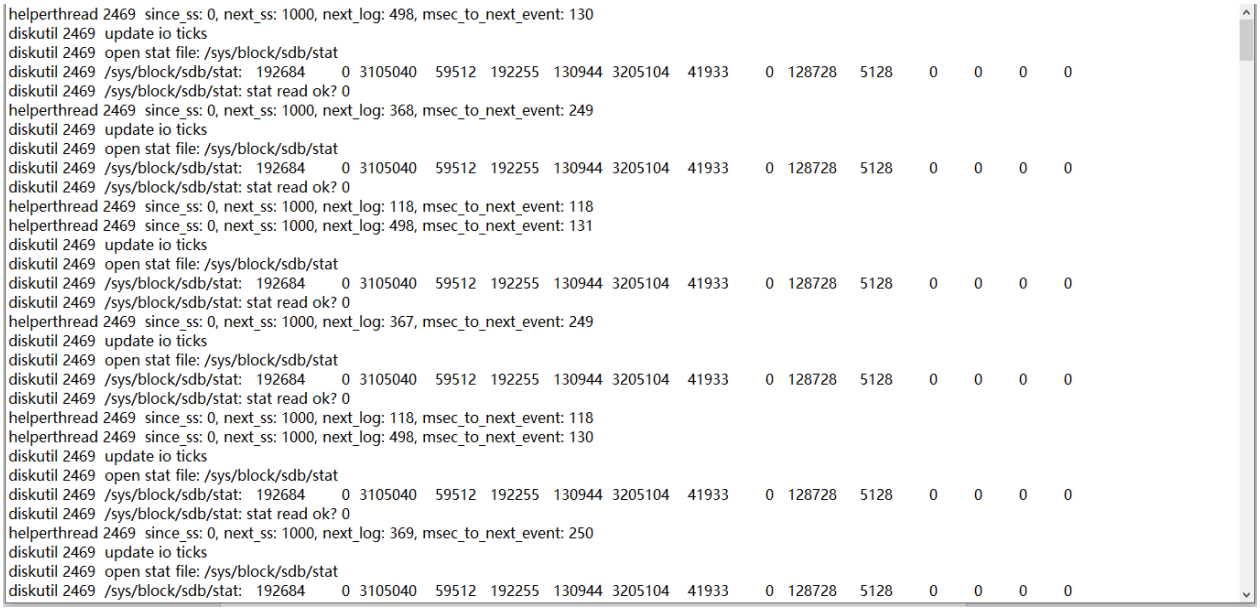

Figure 2.10 Sample output of the Fio program

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3. SINGLE-EVENT EVALUATION OF SSDS WITH ALPHA PARTICLES, PULSED LASER, PROTONS AND NEUTRONS

S. Shi, C. Jin, C. Gu, C. Yeo, R. Fung, S.-J. Wen, R. Tonari, B. L. Bhuva and L. Chen, "Single-event Evaluation of SSDs with Alpha Particles, Pulsed laser, Protons and Neutrons," submitted to *IEEE RADiations Effects on Components and Systems Conference*, 2020.

The background related to SEEs caused by different kinds of ions, SEEs in commercial SSDs and its testing method was presented in the previous chapter. Research showed that SSDs were sensitive to irradiation, such as atmosphere neutrons and alpha particles emitted by the packaging material. As well, it was found the controllers on SSDs were very sensitive to protons. However, to the author's knowledge, there was no published data found about the sensitivity of each chip on SSDs and their contribution to the total SEE cross-section of the SSDs.

In this chapter, alpha particles, protons, neutrons, and laser beams were used for evaluating the SEE sensitivity of each component on SSDs from two vendors. The SSDs experienced Soft Hang (system hang and recovered after power cycling) or Brick (system hang and could not be recovered after power cycling). As there is an ECC code embedded in the NAND flash chip to correct SEUs, none SEU was found in the testing. The results confirm that, amid the brands of SSDs we have tested, the controller chips are still the most sensitive one on the SSD. The buffer chip (DRAM) is also sensitive to irradiation, but the cross-section is much lower than the controller. As expected, the voltage regulator chips are also sensitive to irradiation although the cross-section is even lower than the buffer chip.

The mainly research steps are as follows:

(1) Set up an SSD SEE testing system, which includes hardware and software.

The system should be able to test Single Event Upset (SEU), Single Event Function Interruption (SEFI) and so on, and it should be easily updated to test the new found error modes.

(2) Evaluating the sensitivity using alpha particles, verifying the function of the testing system and obtain the basic error mode in the chips that can be irradiated by using alpha particles.

As we have the alpha sources with high and low dose rate, it's very convenient to do irradiation testing experiment without any beamtime limitation. It's effective and economic way to verify the function of the testing system and obtain the basic error mode. We will use the two alpha sources to irradiate the chips which are wire-bonding packaged on the SSD, to get the important information mentioned above.

(3) Locating the sensitive node in the chips by using a pulsed laser.

A pulsed laser is a more effective and economic way to locate the sensitive position than heavy ion microbeam facilities. We will use our pulsed laser facility to scan and locate the sensitive position in the flip packaged chips on the SSD and get the sensitive circuit and relevant threshold energy.

(4) Locating the sensitive chip on the SSD by using collimated proton beam.

High energy monoenergetic proton beam as it's high penetrating ability and accurate energy is widely used to evaluate the SEE performance of ICs. We will the collimated proton beam in TRIUMF to test different chips on the SSD to evaluate the sensitivity of them and obtain the different error modes caused by SEE happened in different chips.

(5) Evaluating the SEE performance and error modes of the whole SSD by using a white light neutron beam.

The spectra of the white light neutron beam are very similar to that of neutrons in the atmosphere but with much higher flux, so it's an efficient way to evaluate the SEE performance of

a whole electronic device which will be used in the atmosphere. We will use the neutron irradiation facility in TRIUMF to evaluate verify the SEE in the SSD and compare it with the data obtained from other kinds of irradiations.

Single-event Evaluation of SSDs with Alpha Particles, Pulsed laser, Protons and Neutrons

S. Shi, C. Jin, C. Gu, C. Yeo, R. Fung, S.-J. Wen, R. Tonari, B. L. Bhuva and L. Chen

Abstract

SEE sensitivity of major components on the SSD was evaluated using alpha particles, pulsed laser, protons, and neutrons. Results show that the micro-controller is the major contributor to single-event errors.

Index Terms

solid state drive (SSD), single event effect (SEE), single event upset (SEU), alpha, proton, neutron, failure in time (FIT)

3.1 Introduction

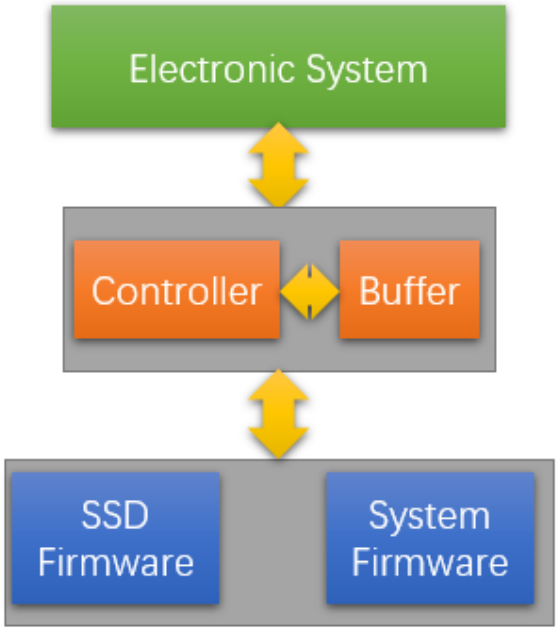


Figure 3.1 Internal parts of a solid state drive (SSD).

Solid state drives (SSDs) are widely used in servers, desktops, and portables as storage devices due to their high accessing speed and the anti-vibration performance [1], [2]. Since all of these computing systems carry out critical tasks on a routine basis, it is important to evaluate their single-event (SE) performance to ensure reliability specifications are met by the final product.

In the terrestrial environment, atmospheric neutrons or alpha particles emitted from the packaging materials are the main cause of single-event upsets (SEU) [3], [4]. These SEUs result in data error or functional interrupt for SSDs [5], [6]. Normally an SSD is composed of non-volatile memory, micro-controller, DRAM, voltage regulators, and other passive components [7].Shown in Figure 3.1. Non-volatile memories, and subsequently SSDs, are shown to become more sensitive to the Single Event Effects (SEE) with the decreasing feature size as shown in Figure 3.2 [6]. Furthermore, components on an SSD are usually made from older technologies to reduce cost without sacrificing performance. These components (micro-controller, voltage, DRAM memory, etc.) from old technologies do not need to be high performance parts because of the slow read/write speeds of non-volatile memories.

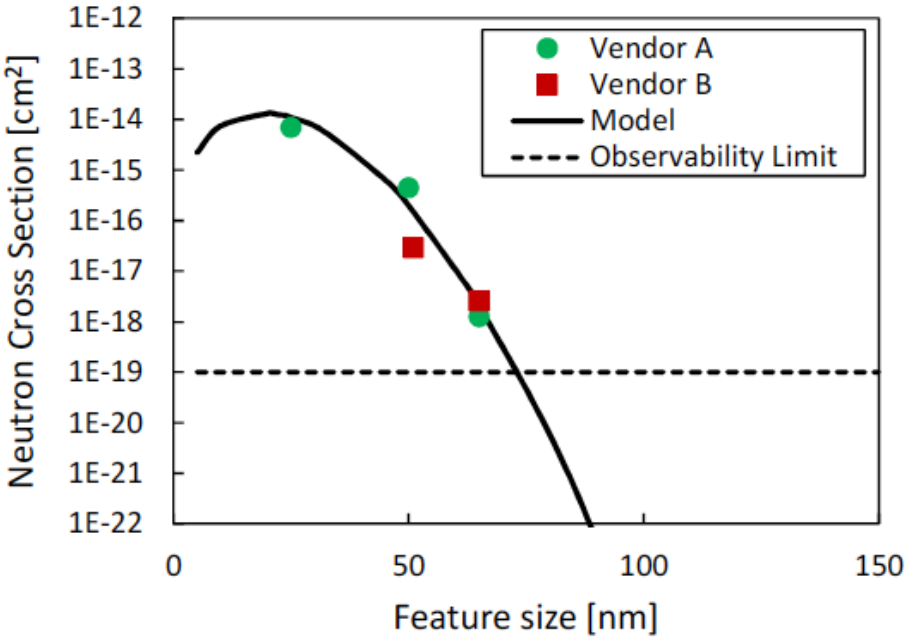


Figure 3.2 Neutron cross-section for non-volatile memories as a function of feature size [6]

Copyright © 2015 IEEE.

Since most SSD manufacturers are focused on reducing cost (the fact that SEE reliability specifications for computing systems are unknown at the time of the manufacturing SSD), most SSDs show high vulnerability to SEE [5]. Because the manufacturers for each of the components on an SSD are different, it is difficult to improve the overall SEE response of SSDs. A study that focuses on SEE vulnerability of individual components on an SSD is needed to identify the weakest link of the SSD so manufacturers can improve the overall SEE performance. This work evaluates

the SEE sensitivity of SSD and major components on the SSDs, including the flash memory, micro-controller, DRAM and voltage regulator chips, using pulsed laser, alpha particles, protons, and neutrons. Results show that micro-controllers in the SSDs are the major contributor to SE errors.

3.2 Error Types and Locations

An SSD is mainly composed of NAND Flash, buffer (DRAM), micro-controller, voltage regulator and some passive components. NAND flash is used for storing data, micro-controller handles all data movements, DRAM memory holds temporary data, and the voltage regulator generates necessary voltages for flash memory operation. NAND flash is very vulnerable to SE errors [8]-[11]. However, the presence of error checking and correction (ECC) algorithm improves the error rate significantly [5], [6]. The main function of the controller of an SSD is loading the firmware from the flash to the DRAM at startup and implement different communication functions, including (i) data I/O and communication between host and SSD, (ii) implementing the wear out an algorithm to improve lifetime, (iii) garbage data collection and bad block management, and (iv) ECC management. All of these functions are critical for the proper operation of SSD. DRAM IC is loaded with firmware at the startup for quick access (accessing firmware in NAND flash will be slow) and acts as a data buffer for data transfer between host and SSD. DRAM may also hold other system-level information necessary for performance evaluation and debugging. It is supposed to be sensitive to irradiation [12].

Single-event upsets in each of these components will affect overall SSD differently. For example, errors in NAND flash may corrupt firmware or stored data. The presence of ECC mostly results in preventing such errors from affecting NAND (and subsequently SSD) operation significantly. SE errors in power regulators will result in NAND operational errors (yielding incorrect data read/write). SE errors in DRAM memory may result in system hang (SSD stops responding) if errors are in firmware. Similarly, SE errors in micro-controllers may result in functional interrupts causing malfunction. For all of these SE errors, SSD may respond in one of three ways; (a) error is in the data and can be easily corrected through ECC or through a retransmit of the data, (b) error causes the system to hang which can be recovered after a power cycle (referred to as Soft Hang error), (c) error causes the system to hang and irrecoverable even after a power cycle (referred to as Brick error).

Brick errors are the most severe errors for SSDs because a power cycle doesn't result in a recovery. The brick error may result from two different ways; (a) firmware in the non-volatile memory is corrupted, (b) firmware may be moved to buffers for relocation to address wear out issues and gets corrupted during transfer. If SE errors occur in micro-controller during such a read/write process for firmware, it may cause a Single Event Function Interruption (SEFI) which leads to the Soft Hang errors. SSD will be able to recover from Soft Hang errors after a power cycle. In the Brick error case, SSD can only be recovered by refreshing the firmware by the manufacture because the golden copy of the firmware is corrupted.

3.3 Experimental Setup

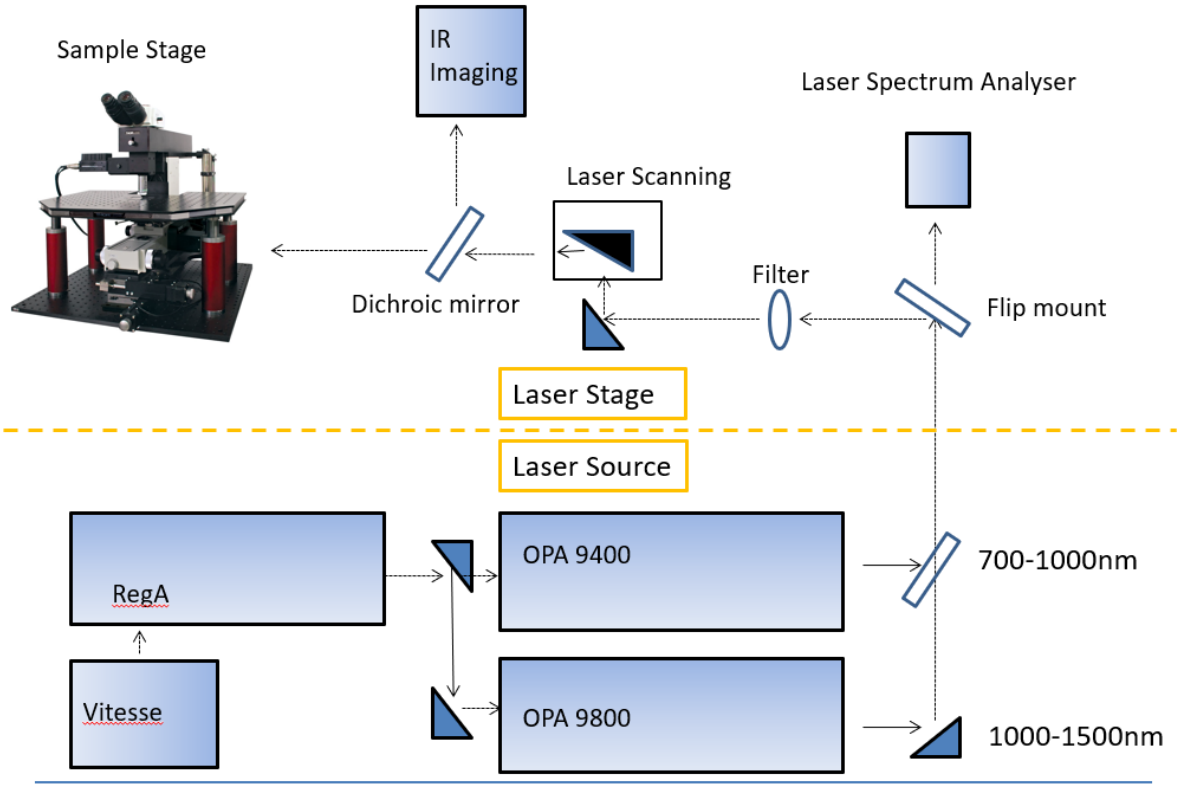


Figure 3.3 Two Photon Absorption optical layout at University of Saskatchewan

Most test software for SSD available in the market focus on performance testing, such as read/write speed. This software is not designed to detect and/or report on single-event errors. In order to detect SEUs occurring in SSD testing during irradiations, specialized test software was developed. The software is designed to write data with a specific pattern (00, 11 or 01) into the SSD and read it back to the testing computer, then compare it with the original data bit by bit to

check if there are any SEU's. The program can run in different modes to check SE errors in different components, for example, one of the read modes allows for direct reading of data from the micro-controller memory or DRAM.

Two alpha sources (shown in Figure 2.4) with different activities were used in the testing at the University of Saskatchewan [13]. The radioactive material of the two sources is ^{241}Am and the energy of the majority alpha particles is 5.486 MeV (85.2%) and 5.443 MeV (12.8%), whose range in silicon is 27.9 μm and 27.59 μm. Wire-bonding chips can be tested with the alpha particles. The activities of the two alpha sources are 92.5 kBq and 30 kBq.

Laser experiments were conducted at the Pulsed Laser facility at the University of Saskatchewan (shown in Figure 3.3). The laser facility can provide femto second laser pulses which are used for two photon excitation in the experiments [14]-[16].

Figure 3.4 The SSDs were fixed at the 1B beam line.

The proton and neutron tests were carried out at the 1B beamline of the Proton Irradiation Facility (PIF) in the TRIUMF laboratory [17]. The photo is shown in Figure 3.4. The energy of the protons was 480 MeV, and the beam is collimated by a collimator with the size of 5 mm × 5 mm at the backside of the room. The neutrons were generated by hitting a thick lead target by the proton beam and the energy spectrum is continuous and very similar to the energy spectrum of neutrons in the atmosphere.

For particle (alpha, proton, and neutron) tests, a specific data pattern (check board) and reading/writing mode for the SSD were chosen and the part was exposed to the beam. Flowchart for the test protocol is shown in Figure 3.5. Whenever a Soft Hang or Brick errors were observed, the beam was turned off and SSD was power cycled for recovery. The SSD was monitored by a laptop computer for proper operation through a USB connection. The SSD power was provided by a standalone power supply to monitor possible single-event latch-up events. For the neutron testing, 4 SSD cards in parallel were placed in the beamline to improve error statistics. Each SSD was powered separately to monitor individual current levels.

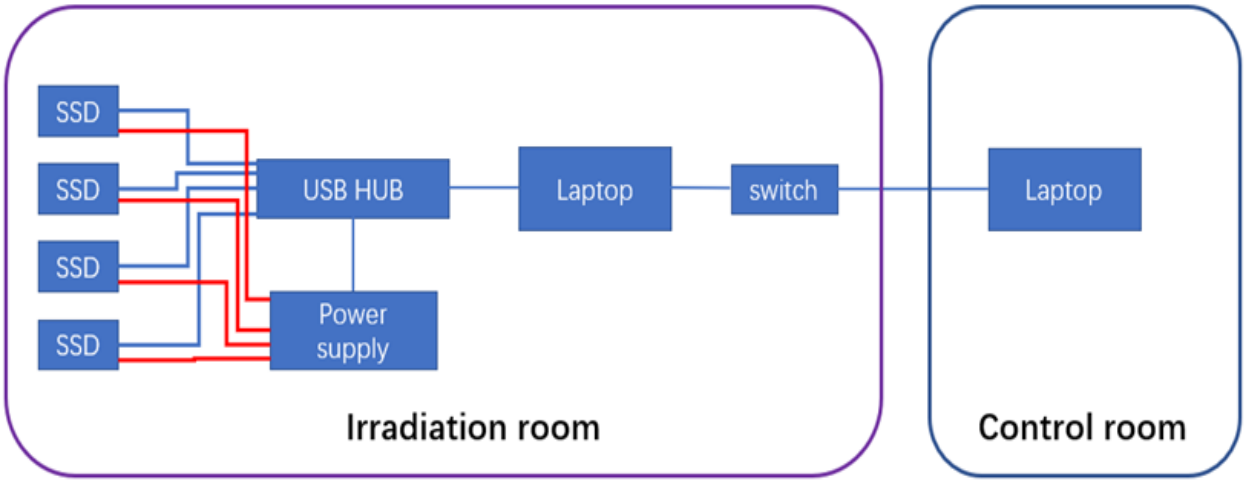


Figure 3.5 The schematic of the testing system for particle exposures.

3.4 Testing Results and Analysis

3.4.1 Alpha source testing results

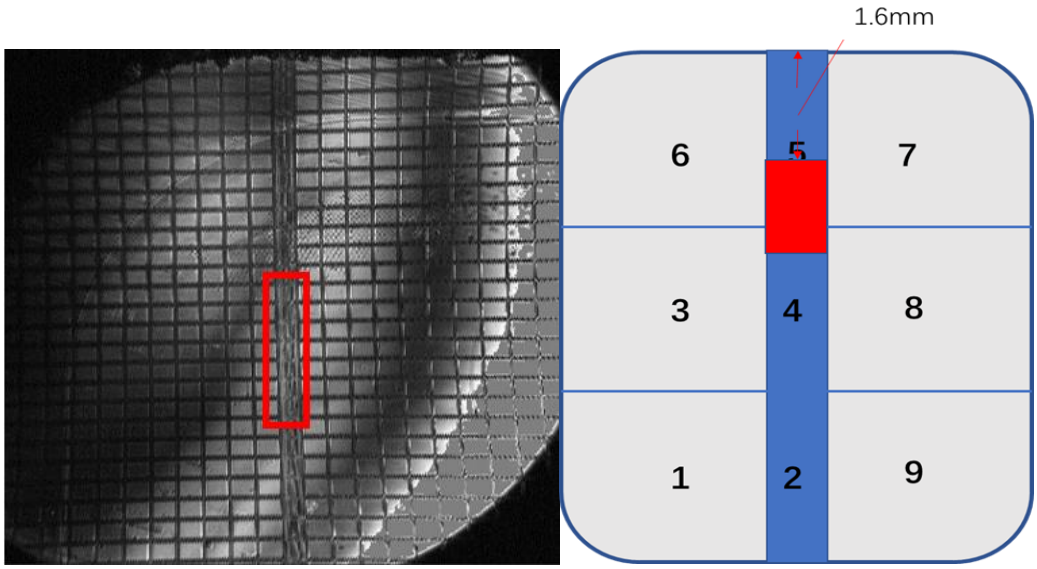
The micro-controller IC and the NAND flash memory IC are wire-bonded chips. They were decapped and tested with alpha sources. Each component was tested separately. As expected, the alpha source caused zero errors when NAND flash memory was exposed to it. During this exposure, ECC was also running, resulting an extremely low probability for an error. The micro-controller, on the other hand, showed sensitivity to alpha irradiation. The dominant failure signature was an unresponsive micro-controller when the alpha source was placed above it. For these errors, the SSD became operational after power cycling. All errors from alpha source for micro-controller resulted in similar Soft Hand errors. The number of errors observed was approximately 10 errors in 5 minutes. The cross section for this type of error was calculated to be 3×10^{-7} cm^2. The similar cross section was observed for both the alpha sources.

3.4.2 Laser testing results

Of all the components on the SSD, only the buffer (DRAM) IC was in a flip-chip package, making it testable using a two-photon laser. The micro image of part of the DRAM is shown in Figure 3.6 (a). The die was classified into 9 areas as shown in Figure 3.6 (b) and scanned using the laser. Areas 2, 4, 5, in the center, are the peripheral circuits while other areas are cell arrays. No errors were observed for laser energies less than 3nJ. Brick errors were observed with 3 nJ energy when the red area was scanned by the laser. After the laser exposure, the SSD couldn't be accessed by the laptop, even after power cycling. The SSD was sent to the manufacturer for Failure Analysis. FA results showed parity bit errors in the DRAM causing Brick errors.

3.4.3 Proton testing results

The components on the SSDs were irradiated separately using the collimated proton beam (5 mm × 5 mm). The results are shown in Table 3.1. From the table, it may be concluded that: (1) the controller is the most sensitive IC on SSDs; (2) When the controller was irradiated, it may cause Soft Hang and Brick errors; (3) the sensitivity of the buffer (DRAM) is lower than the controller; (4) FIT (Failure in Time) rates for errors in NAND flash memory IC and voltage regulators are very low.



(a) (b)

Figure 3.6 Test results for DRAM IC. (a) Image of the buffer IC under infrared microscope showing the sensitive area inside the red rectangle. (b) Sensitive area on the die.

The components on the SSDs were irradiated separately using the collimated proton beam (5 mm × 5 mm). The results are shown in Table 3.1. From the table, it may be concluded that: (1) the controller is the most sensitive IC on SSDs; (2) When the controller was irradiated, it may cause Soft Hang and Brick errors; (3) the sensitivity of the buffer (DRAM) is lower than the controller; (4) FIT rates for errors in NAND flash memory IC and voltage regulators are very low.

3.4.4 Neutron testing results

Four SSDs from Vendor I were tested simultaneously using the white light neutron beam. The results are shown in Table 3.2. It shows that (1) neutron can also cause Soft Hang and Brick errors; (2) the FIT rate is similar to that of the micro-controller IC in the proton testing, indicating that the micro-controller is the most sensitive IC on the SSD.

Table 3.1 Proton Testing Results

Brand	Testing chip	Fluence ($p.cm^{-2}$)	FIT (with 95% confidence)	Effect type
Vendor I	NAND	2.68E+10	1.6±1.4	Hang
	DRAM	5.14E+10	2.1±1.2	Hang
	Controller	3.05E+9	35.0±21.0	Hang
		1.61E+9	19.4±18.9	Brick
	Voltage regulator 1	5.87E+9	5.3±5.2	Hang
	Voltage regulator 2 & 3	1.64E+10	2.6±2.4	Hang
	Voltage regulator 4	6.17E+09	<3.2	Hang
Vendor II	NAND	6.30E+09	<3.1	Hang
	DRAM	7.63E+09	<2.6	Hang
	Controller	4.06E+09	7.7±7.5	Brick
	PWR Management	7.18E+09	<3.1	Hang
	Voltage regulator	6.35E+09	0	hang

Table 3.2 Neutron Testing Results

Error type	Total Fluence ($n.cm^{-2}$)	FIT (with 95% confidence)	Recoverable after power cycle
Soft hang	1.95E+9	48.3±30.8	Yes
Brick error	3.18E+08	98.0±95.9	No

3.4.5 Discussions

From the proton, neutron and laser testing results, it is clear that the Soft Hang errors mainly originated in the buffer (DRAM) IC, the power regulators, and the micro-controller. However, the Brick errors were all from the micro-controller. Brick errors were believed to be caused by errors in the firmware and were written into the NAND flash, as the errors cannot be removed after power cycle.

3.5 Conclusions

The SSDs from two vendors were evaluated using alpha particle, pulsed laser, collimated protons, and white light neutrons. The results showed that the micro-controller IC is the most sensitive IC on the SSD. The FIT rate of the micro-controller dominated the FIT rate of the whole SSD. The DRAM buffer IC is sensitive to protons but the FIT rate is much lower than that for the controller. NAND flash and voltage regulator ICs are also sensitive to protons, but the FIT rates are the lowest amongst the components in the SSDs.

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4. SINGLE EVENT UPSET EVALUATION FOR A 28NM FD SOI SRAM TYPE BUFFER IN AN ARM PROCESSOR

S.-T. Shi, R. Chen, R. Liu, M. Chen, C. Shen, L. Chen, "Single event upset evaluation for a 28nm FD SOI SRAM type buffer in an ARM processor," submitted to *Microelectronics Reliability*, 2020.

In the previous chapter, SSDs were evaluated by using alpha particles, protons, and neutrons. In this chapter, another type of storage device, an SRAM is studied with heavy ions to evaluate its SEE performance. The SRAM was designed and fabricated with STM 28-nm FDSOI technology. It was used as a buffer for a microprocessor test chip in which different mitigation methods were used. In order to minimize the SEU error contribution of the SRAM to the whole test chip, the TMR hardening method was used in the design. To evaluate the cross-section of the SRAM, both simulation and experiment testing approaches were adopted to evaluate the SEU cross-section in both TMR mode and non-TMR mode. The results showed the SRAM is robust enough for the evaluation for the processors.

The mainly research steps are as follows:

(1) Evaluating the SRAM in non-TMR mode by using heavy ions and get the cross-section in non-TMR mode.

Using Heavy ions with different Linear Energy Transfer(LET) to irradiate the chips is an effective way to get the cross-section curve of ICs. We will use the heavy ion facility in Beijing HI-13 Tandem Accelerator to irradiate the SRAM and test the cross-section in non-TMR mode, which will be used as a comparison to TMR mode.

(2) Evaluating the SRAM in TMR mode by using heavy ions and get the cross-section in TMR mode.

Getting the cross-section in TMR mode, comparing it with the data in non-TMR mode and analyzing the reason for the difference.

(3) Simulate the cross-section in non-TMR mode.

According to our design, simulating the cross-section in non-TMR mode, which will be used as a reference to analyze the difference between non-TMR and TMR.

(4) Calculating the cross-section in TMR and analyzing the factors that affect the cross-section in TMR mode.

As we can't get the cross-section in TMR mode by using the simulation method, the calculation method will be used to calculate it. Also, the affection factors, such as accumulated fluence, will be analyzed.

Single event upset evaluation for a 28nm FD SOI SRAM type buffer in an ARM processor

S.-T. Shi, R. Chen, R. Liu, M. Chen, C. Shen, L. Chen

Abstract

A triple-modular-redundancy (TMR) SRAM was designed as the embedded high-speed memory for radiation-tolerant ARM processors with STM 28nm FDSOI technology. The single event upset cross-section of the SRAM was tested by using heavy ions with LET=15.0 MeV.cm^2.mg^{-1} in both non-TMR and TMR modes with different accumulated fluence. The SRAM cell was also simulated by using the Cogenda TCAD simulation suite and the cross section was calculated by using the analytic method. The results showed the cross-section is around 2E-10 cm^2/bit in non-TMR mode, and in TMR mode it varied from one to several orders lower than the non-TMR mode according to the specifically accumulated fluence. As a scrubbing circuit was designed to reduce the accumulated number of SEUs in the SRAM, the cross-section could be low to 5E-17 cm^2/bit, which is robust enough for the whole circuit.

Keywords

single event upset, SRAM, FDSOI, 28nm, TMR, accumulated fluence, MBU

4.1 Introduction

With the decrease in feature size of integrated circuits (ICs), the effect of single event upset (SEU) [1]-[3] caused by neutrons or alpha particles at ground level is becoming more and more severe [4]-[6]. Static Random Access Memory (SRAM) is widely used as high-speed buffers in digital systems for storing the data and instructions to increase the system processing speed. However, single events induced by energetic particles in an SRAM could cause single cell upset or multiple bits upset and result in data errors or system function failures [7]. Single event multiple bit upsets in a word are especially troublesome since simple error correcting code (ECC) could not correct them, and interleaving techniques have to be applied to prevent them [8]. Therefore, it is important to evaluate its upset rates before it's applied in electronic systems.

ST Microelectronics' (STM) 28-nm Ultra-Thin Body and BOX FDSOI technology has shown superior performance in terms of SEEs resistance compared to those of 28-nm bulk technologies due to the insolation layer (SiO_2) under the transistors and very thin diffusion layers [9]. It has

shown that the SEU rates of SRAMs and flip-flops with this technology could be up to two orders of magnitude lower than those with 28-nm bulk technologies [10]-[12].

Triple Modular Redundancy (TMR) techniques have been widely used in designing storage cells for commercial and space electronics where high reliability is required [13], [14]. As the circuits are duplicated with three modules, the flip flop (FF) tolerance to SEEs is generally better than dual modular redundancy methods, such as DICE [15], Guard Gate [16], Quatro [17]. However, the resilience on SEUs for radiation-hardened FFs is remarkably reduced in the 90 nm process and beyond [18]. Jagannathan et al. reported that the SEU cross section of the FFs designed with TMR method is only 3.3 times better than those of the regular FFs [19]. This is due to the distance between the sensitive nodes is becoming smaller and smaller with the decreasing of feature size, and it leads to multiple node charge collection. In addition, the effectiveness of TMR is related to the accumulated numbers of errors in three individual units [20], so the scrubbing frequency is significant for obtaining the lower cross-section in TMR. To the authors' knowledge, there is no data published on the soft error performance of the SRAM designed in TMR based on 28 nm FDSOI technology. Therefore, it is necessary to evaluate the performance of TMR SRAM in this technology.

In this work, a TMR protected SRAM has been designed as an embedded memory for radiation tolerant ARM M0 processors. The SRAM module was tested in heavy ions experiments, and the SEU cross-sections of the SRAM cells in both non-TMR and TMR modes at different accumulated fluence were provided. The single event multiple bit upset (MBU) rates were also provided. The SEU cross-section of the SRAM cells was also simulated by using a TCAD simulation suite and the relationship between the SEU cross-section in TMR mode and accumulated fluence was analyzed.

4.2 Test Chip Design

The SRAM (32k-bits organized as 1024 entries of 32-bit words) was designed as the buffer for the radiation tolerant ARM M0 micro-processors on the same die [21]. The SRAM cells used standard 6-T structure, and the size is about 0.5 μm^2. The floorplan diagram of the test chip is shown in Figure 4.1. TMR instead of the ECC approach was adopted to protect the SRAM from SEUs, to minimize the additional latency for read/write accesses to the SRAM and achieve the

maximum clock frequency. A classical majority voter from the standard cell library was used, which is composed of three AND gates and one OR gate.

The on-chip SRAM is highly configurable and accessible through a configuration and status interface, which was also protected with TMR style. The SRAM can be configured as the embedded memory for the ARM cores, and it could also be configured as independent memories and accessed from external. Also the SRAM can be configured as three standalone 32k bit memories (non-TMR mode), or single 32k bit memory (TMR mode).

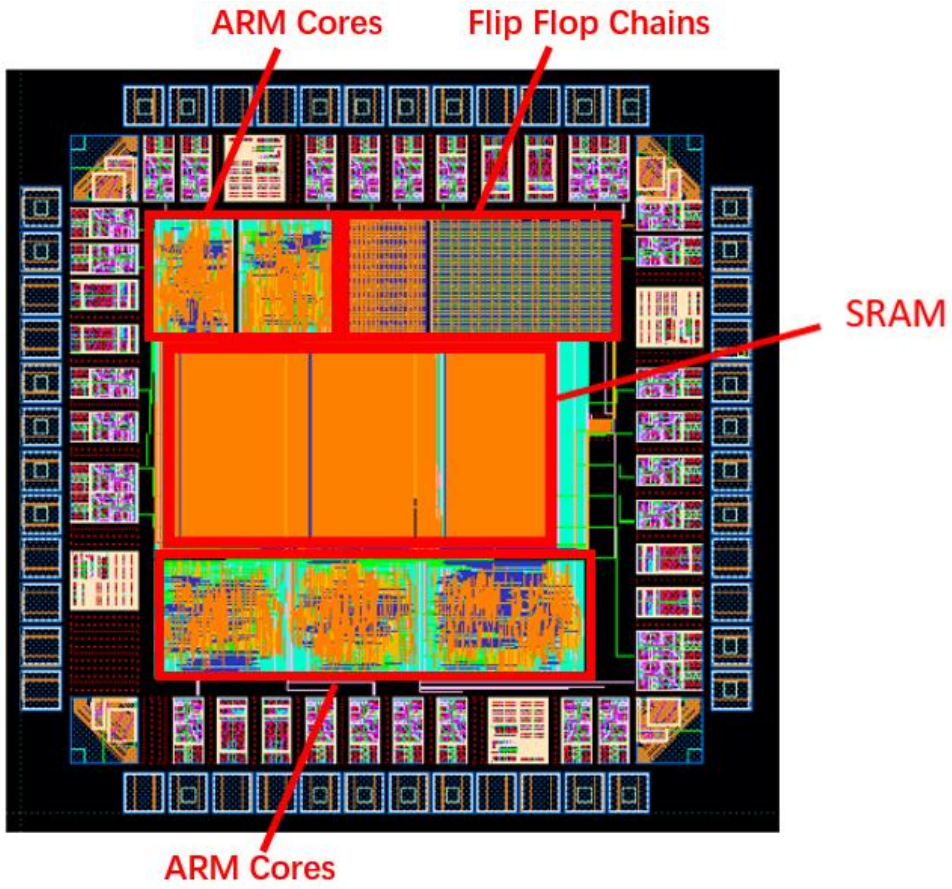

Figure 4.1 The whole layout of the SRAM.

4.3 Experimental Setup

The heavy ion irradiation experiment was carried out at HISEEIF which is located at the Beijing HI-13 Tandem Accelerator, the China Institute of Atomic Energy (CIAE) [22].

The SEU testing system consists of three main parts, including a Raspberry Pi, a Virtex 5 FPGA, and the DUT board as shown in Figure 4.2 and Figure 4.3. The Raspberry Pi is the main

control unit for the entire system and communicates with the FPGA via a UART. The configuration information is sent from the Raspberry Pi to the FPGA. Based on the commands, the FPGA issues 128-bit frames to the DUT through the TMR serial interface. The test chip was irradiated with 110MeV Cl (Chlorine) ions, with LET of 15.0 MeV.cm^{-1}.mg^{-2}.

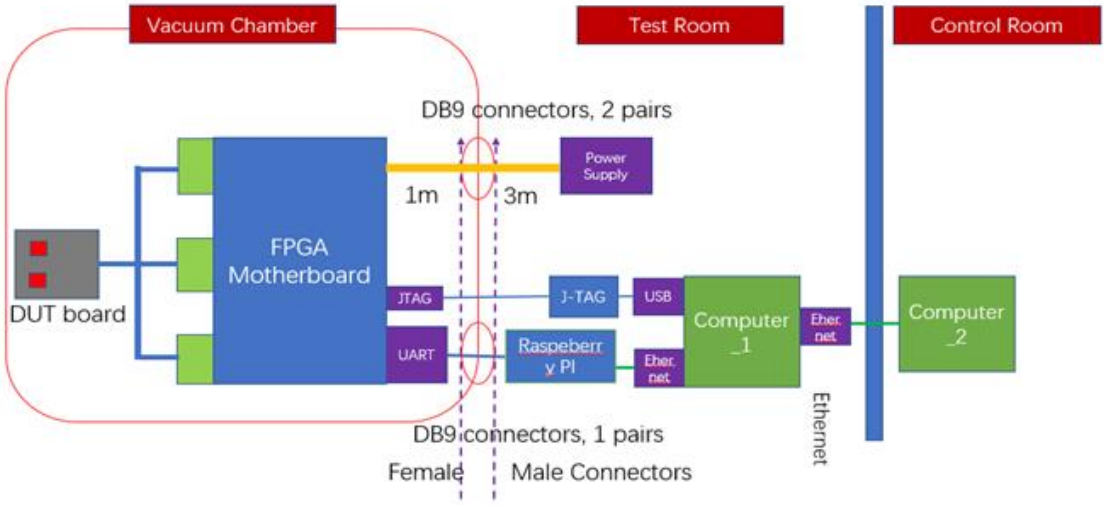

Figure 4.2 The diagram for the heavy ion test setup.

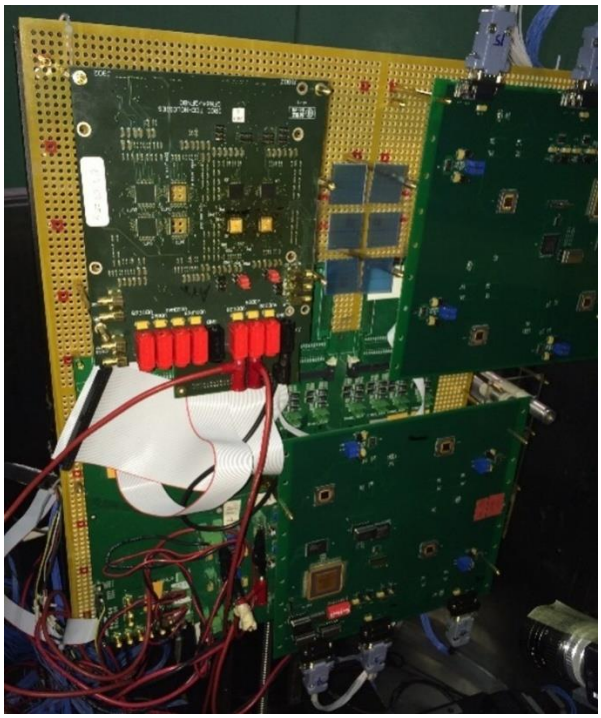

Figure 4.3 The testing board in the vacuum chamber.

To eliminate the unnecessary contribution from other circuits, the SRAM was tested statically when the beam was on. The testing procedure is as following: write the data into the SRAM, turn on the ion beam, turn off the beam when the total scheduled fluence is reached, read out the data from the SRAM and compare it with the initial data. The fluence for each run is selected to keep the SEU numbers relatively low.

The data in the SRAM can be read out in either TMR mode from the embedded voters or non-TMR mode directly from the three parallel separated SRAM modules. In the testing software, an external virtual voter is also designed. It is used as a "software TMR" to obtain the SEU errors when all the data is read out from the three separate modules. This function is designed for comparing the difference between the "hardware TMR", which is generated by the built-in voters, and the "software TMR", which is generated by the software.

4.4 Heavy Ion Experiment Results

4.4.1 Non-TMR Mode

In non-TMR, both 11 and 00 data patterns were tested. The result is shown in Table 4.1. It shows that the average cross-section for the SRAM is around 2.2E-10 cm^2 and the SEU cross-sections of 00 and 11 data patterns are very similar.

Table 4.1 SEU cross-sections of the SRAM in non-TMR and TMR modes, the statistical errors were calculated with a confidence level of 95%

Testing mode	**Fluence ($ions.cm^{-2}$)**	**Data pattern**	**SEUs**	**Cross-section (cm^2/bit)**
Non-TMR	1.0E+07	11	216	(2.20±0.30)E-10
	1.0E+07	00	221	(2.25±0.30)E-10
TMR	1.0E+8	00	34	(1.08±0.36)E-11
TMR (Exterior voter)	5.0E+7	11	11	(7.66±4.36)E-12

4.4.2 TMR Mode

In TMR mode, the voters inside the SRAM test chip were used to vote from the three separate SRAM modules. The result is listed in Table 4.1, which shows that the cross-section for TMR mode is approximate one magnitude lower than that of non-TMR mode, which is mainly determined by the accumulated fluence. The relationship between the cross section and accumulated fluence will be further analyzed in Section 4.5.

Table 4.2 Results for MBU

Fluence (ions.cm^{-1})	**Single bit upsets**	**Two bits upsets**	**Three bits upsets**
5.00E+07	973	30	2

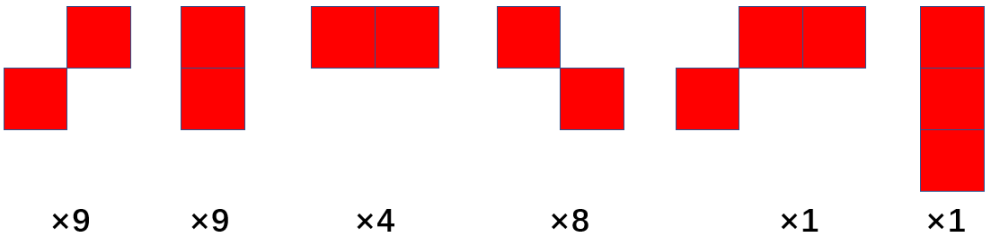

Figure 4.4 SEU mapping for the SRAM modules

4.4.3 MBU Testing

Multi-bit upset is also analyzed from the experiments by recording the addresses of the SEUs during the testing. Therefore, the SEU mapping can be obtained after data processing. The MBU upset rates are listed in Table 4.2 and the upset patterns are shown in Figure 4.4.

From Table 4.2 and Figure 4.4, we can see that the cross-section of MBU is much lower than that in [23]. The possible reasons for this are that the distance between the sensitive nodes in the present design is larger than that in the reference, besides the lower LET used in this experiment.

4.5 Simulation, Calculation and Discussion

4.5.1 Cross-section in non-TMR mode simulation

The SRAM in non-TMR mode was simulated first with the Heavy-Ion module of the Cogenda's Visual TCAD simulation suite, which has been used for SEU simulation in 28nm FDSOI SRAM and other feature size devices in previous work [24], [25]. Figure 4.5 shows the illustrative layout view of the 6T-cell SRAM with the size of 630 nm×793 nm and Figure 4.6 shows the sensitive area in the cell. Five different types of heavy ions were used in the SEE simulation and the SEU cross-sections as the function of LET are listed in Table 4.3. It shows that there is no SEU when the LET is 3.64 and 5.84 MeV.cm^2.mg^{-1}, and the SEU cross-sections of bit-errors increases with LET from 30.6 to 55.3 MeV.cm^2.mg^{-1}. The simulated SEU cross-section at LET of 15 MeV.cm^2.mg^{-1} is slightly smaller than the heavy ion results, it could be that the multiple bit upsets generated by heavy ions were not included in the simulations.

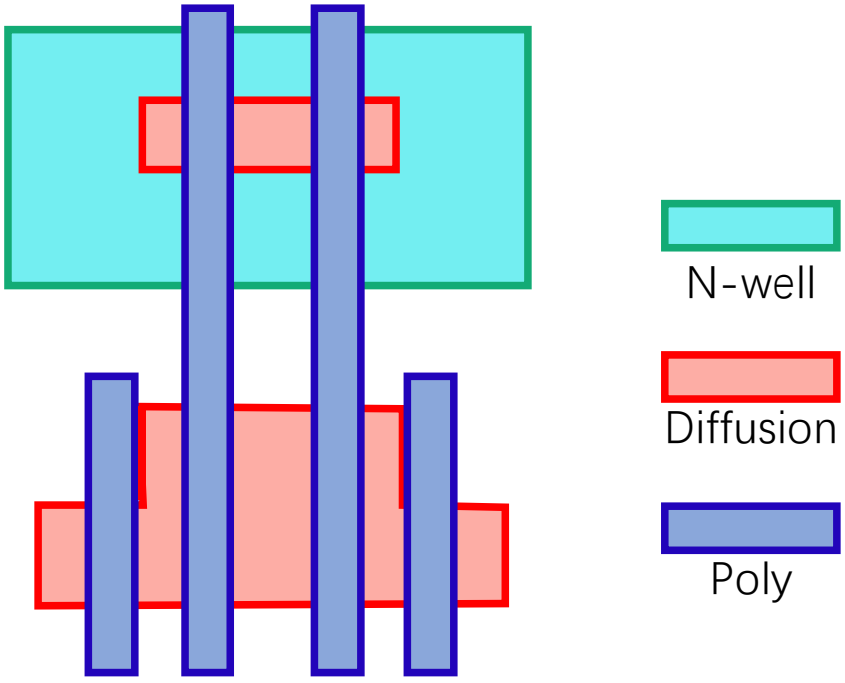

Figure 4.5 The top view of the layout of the SRAM Cell

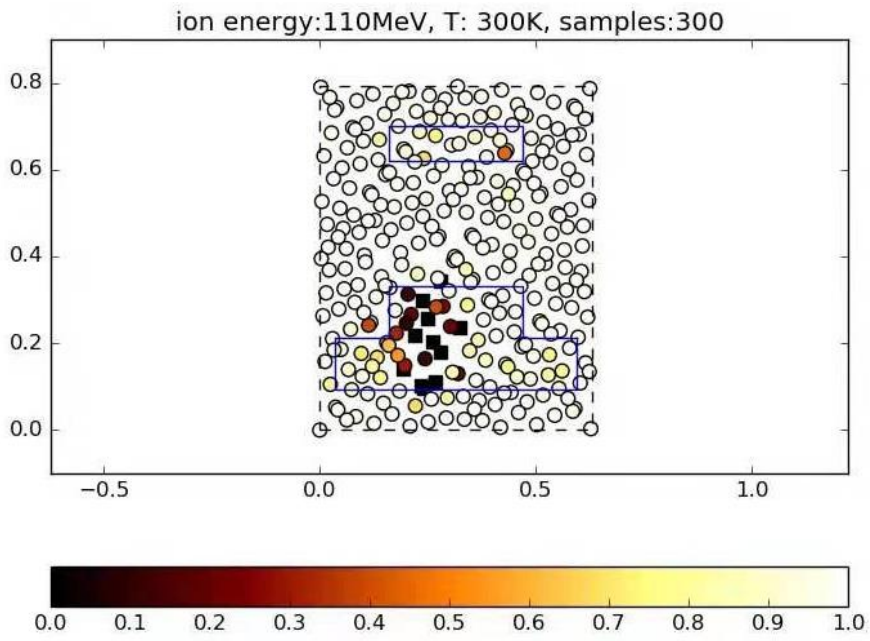

Figure 4.6 The layout of the SRAM Cell and the Sensitive Map

The cross-section data from previous measurements [23] as well as our results are plotted together in Figure 4.7. It can be seen that the simulated cross-section in our work agrees well with the experimental data at the LET of 15 MeV.cm^2.mg^{-1}. The cross-section of the presented 6T cell is approximately 2 orders magnitude lower than that of 28 nm bulk SRAM in previous work.

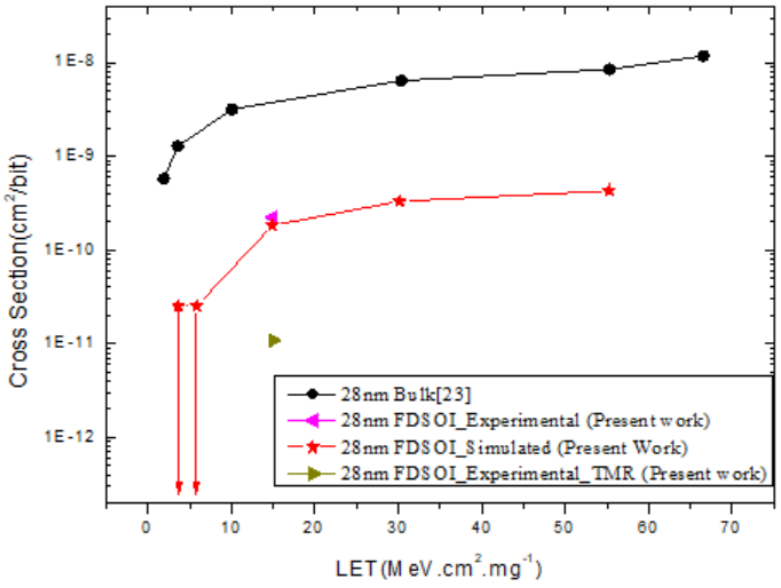

Figure 4.7 Comparing between present work and other data

Table 4.3 Ion Information for the Simulation

Ion	Energy (MeV)	Range in Silicon (μm)	LET in Silicon ($MeV.cm^2.mg^{-1}$)	Cross-section (cm^2/bit)
Ne	185	144.7	3.6	<2.51E-11
Si	301	150.8	5.8	<2.50E-11
Cl	110	30.6	15.0	1.83e-10
Kr	910	113.7	30.2	3.31e-10
Xe	1570	115.3	55.3	4.27e-10

4.5.2 TMR mode results analysis and calculation

Besides the TMR mode, the data in the three separate SRAM modules was also read out directly and analyzed in a "soft TMR mode". The data was voted by the testing software. The voting logic is: assuming the data from the three SRAM modules in the same address is A, B, and C, if A=B, output B; if A≠B, output C. The result is shown in Table 4.1. In this mode, the storage is normalized to one-third of non-TMR mode. From the results, we can see although the two values overlap in the statistical error range, the cross-section in TMR (exterior) is a little lower than the other. The reason for that is that the total fluence for the TMR (exterior) is lower than the TMR, which caused less accumulated errors in the SRAM.

The SEU cross-section of the SRAM in TMR mode is calculated based on the simulated cross-section in non-TMR mode. Supposing σ_d is cross-section for the whole SRAM in non-TMR static mode, and S is the total storage of the three SRAM modules. The probability of a bit flipped in fluence F is

$$P = \frac{3F \cdot \sigma_d}{S} \quad (1)$$

Then the real number of flipped bits is

$$N = F \cdot \sigma_d \quad (2)$$

The probability of a bit flipping is

$$P = \frac{3N}{S} \quad (3)$$

For a given specific address in the three separate modules of SRAM, the probability of 2 errors occurring is

$$P_{TMR2} = P \cdot P \cdot (1 - P) \cdot C_3^2 \quad (4)$$

For a given specific address in the three separate modules of SRAM, the probability of 3 errors is

$$P_{TMR3} = P^3 \quad (5)$$

The total probability of TMR upset is

$$P_{TMR} = P_{TMR2} + P_{TMR3} \quad (6)$$

The total upset number in TMR mode is

$$N_{TMR} = \frac{S \cdot P_{TMR}}{3} \quad (7)$$

Then,

$$N_{TMR} = \frac{(1-S)N^3 + S^2N^2}{3S^3} \quad (8)$$

$$N_{TMR} = \frac{(1-S)\sigma_d^2 \cdot F^2 + S^2 \cdot \sigma_d^2 \cdot F^2}{3S^2} \quad (9)$$

From equation (1), it is noted that the relationship between the number of upsets in TMR mode (N_{TMR}) and total upsets (N) in the SRAM is in an exponential relationship instead of a linear relationship, and as $N=F \bullet \sigma_d$, N_{TMR} also has a linear relationship with the fluence (F), which is shown in equation (9) and plotted in Figure 4.8. According to equation (2), if the refresh time is equal to the irradiation time, i.e. the SRAM is not refreshed during the irradiation, which is the same to the condition of the experimental testing. The cross-section data of LET=15 MeV.cm^2.mg^{-1} and fluence of 1.0E+8 ions.cm^{-2} is used to calculate the cross-section, then cross-section is 3.7E-11 cm^2/bit. This is close to the experimental value (1.1E-11 cm^2/bit).

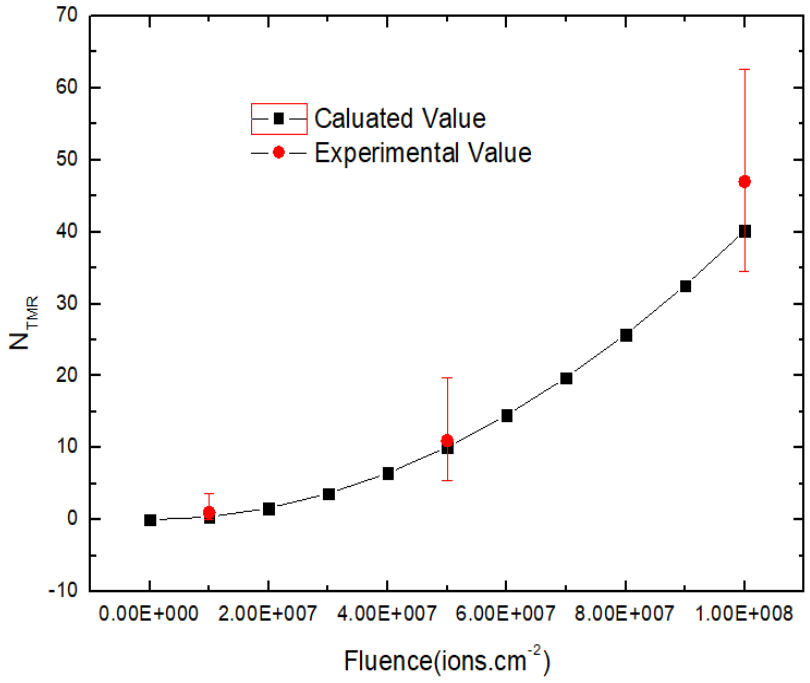

Figure 4.8 Relationship between N_{TMR} and N

Several experimental data were also plotted in Figure 4.8. We can see from the figure, the experimental data fit well with the calculated data, and the shape of the curve is para-curve rather than a straight line. Thus, if we want to lower the SEU rate in TMR mode, the number of SEUs accumulated in each SRAM module should be controlled as low as possible. In another word, the content of the SRAM should be refreshed frequently to reduce the SEUs, this is even true for the TMR protected SRAM.

4.5.3 Discussions on the effect of error rate of the SRAM in the whole chip

As mentioned in the previous part, it is better to keep the lowest SEUs in each separated SRAM module to reduce the SEUs in the TMR mode. A CRC checking and refresh circuit was designed in the test chip. The data in the SRAM are checked continuously and the content will be refreshed once any error is found.

The arm processor can run at a frequency of 600MHz, with the minimum refresh time of around 11ms. Substituting the simulated cross-section data, if the flux Φ is 1.2E+5 ions.cm^{-2}.s^{-1} and the total fluence F is 1.0E+8 ions.cm^{-2}, the cross-section is estimated close to 5e-17 cm^2/bit. It

is around 7 orders lower than the cross-section in non-TMR mode. Therefore, the SEU contribution from the TMR SRAM to the overall microprocessor circuits is low.

4.6 Conclusions

An embedded SRAM was developed for ARM M0 processors with the STM 28nm FDSOI technology. The SEU cross-sections of the SRAM were evaluated in both TMR and non-TMR modes.

Heavy ion testing results showed that the cross-section in non-TMR mode is 2E-10 cm^2/bit with LET of 15 $MeV.cm^2.mg^{-1}$, which matches well with the simulated data. The relationship between the number of errors and accumulated fluence in TMR was calculated and verified by the heavy ion experiment. The results showed that the relationship is parabolic, and based on our scrubbing circuits; the cross-section can be 7 orders lower than the non-TMR mode. Therefore, the effect of the SEUs that happened in the SRAM on the whole chip can be neglected.

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5. SUMMARY, CONCLUSIONS, CONTRIBUTIONS AND FUTURE WORK

5.1 Summary

This work examines the SEE performance in a TMR SRAM based on ST Microelectronics 28-nm Ultra-Thin Body and BOX FDSOI technology and SEE mechanism of two vendors of commercial SSDs.

The SRAM was developed as a buffer for ARM M0 processors with the STM 28nm FDSOI technology. To reduce the effect of SEU happened in the SRAM on the processors, TMR was used in the SRAM. The SEU cross-sections of the SRAM were evaluated in both TMR and non-TMR modes. Heavy ion testing results showed that the cross-section in non-TMR mode is very similar to the simulated value, and TMR is still working well in presented 28-nm FDSOI technology. However, the cross-section is closely related to the number of errors accumulated in the SRAM, the relationship was calculated and verified by experiment result. As a scrubbing circuit was designed in the chip, the effect of the SEE happened in the SRAM to the processors is extremely low. Multiple Bits Upsets was observed in the SRAM, but the cross-section is lower than the existing data, the reason may be the distance between the sensitive nodes is farther than that or the LET of heavy ions used in the experiment is lower than that in the reference.

As commercial SSDs are widely used in computers, portable devices, communication devices and so on. The harm of SEE happened in SSDs has caused people's attention. In this work, the sensitivity of different chips on two vendors of SSDs was envaulted using alpha particle, pulsed laser, collimated protons, and white light neutrons. The results showed that the micro-controller IC is the most sensitive IC on the SSD. The FIT rate of the micro-controller dominated the FIT rate of the whole SSD. The DRAM buffer IC is sensitive to protons but the FIT rate is much lower than that for the controller. NAND flash and voltage regulator ICs are also sensitive to protons, but the FIT rates are the lowest amongst the components in the SSDs.

5.2 Conclusions

The SSDs from two vendors were evaluated using alpha particle, pulsed laser, collimated protons, and white light neutrons. The results showed that the micro-controller IC is the most sensitive IC on the SSD. The FIT rate of the micro-controller dominated the FIT rate of the whole SSD. The DRAM buffer IC is sensitive to protons but the FIT rate is much lower than that for the

controller. NAND flash and voltage regulator ICs are also sensitive to protons, but the FIT rates are the lowest amongst the components in the SSDs.

An embedded SRAM was developed for ARM M0 processors with the STM 28nm FDSOI technology. The SEU cross-sections of the SRAM were evaluated in both TMR and non-TMR modes. Heavy ion testing results showed that the cross-section in non-TMR mode is 2E-10 cm2/bit with LET of 15 MeV.cm2.mg-1, which matches well with the simulated data. The relationship between the number of errors and accumulated fluence in TMR was calculated and verified by the heavy ion experiment. The results showed that the relationship is parabolic, and based on our scrubbing circuits; the cross-section can be 7 orders lower than the non-TMR mode. Therefore, the effect of the SEUs that happened in the SRAM on the whole chip can be neglected.

5.3 Contributions

The main contributions of this work can be divided into two aspects. Firstly, the research results on the FDSOI technology SRAM provided the data on TMR protection method of this technology and its error contribution on the microprocessors. It shows that the impact could be neglected if the refresh rate is high enough. Secondly, this is the first time to obtain the sensitivity of different components on the SSDs and the relevant FIT rates. This provided important data for SSD vendors and users to improve the SSDs performance in terms of SEEs.

5.4 Future Work

For the STM 28-nm FDSOI SRAM chip, it would be ideal that if more data could be obtained from other LET values to provide more information about the hardness of this design. Also only static testing method was used in the heavy ion testing, it would be helpful if the data could be collected at dynamic testing condition so that the impact of other devices like voters can be taken into account.

For SSDs, most testing could be done in the future, such as (1) locate the sensitive position in the controller chip and buffer chip using pulsed laser or alpha source; (2) test and analyze more error modes using alpha source; (3) test more vendors of SSD to check the difference on the SEE sensitivity. Those testing could enhance the understanding of failure mechanisms in the SSDs.