MICROCOMPUTER-BASED REAL-TIME
TWO-PHASE EXCITATION SYSTEM
FOR A
VARIABLE-SPEED DUAL-EXCITED
SYNCHRONOUS GENERATOR

A Thesis
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by

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Dedicated to my father, Mr. Yonah M. Makallah, who instilled in me the dream to get this far with education; and to the young engineers who are learning to convert the feasible into the practical.
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ABSTRACT

Recent studies have demonstrated that a dual-excited synchronous generator (DESG) can be applied as a variable-speed constant-frequency (VSCF) generating system. In such an application, this machine, which has two excitation windings, requires two-phase slip frequency excitation voltages. Thus, the practical application of this DESG for VSCF operation depends on the ability to generate and control these two-phase excitation voltages.

In this thesis, the problem of developing an excitation system for a variable-speed DESG is investigated as a signal generation problem. The problem is to generate a two-phase excitation supply which satisfies, in real time, the excitation requirements of the variable-speed DESG. The proposed solution to this excitation problem has a frequency regulation (FR) scheme and a voltage regulation (VR) scheme. Based on these regulation schemes, a computer-based, real-time, two-phase excitation system for a variable-speed DESG has been developed, implemented and tested. The excitation system uses a novel and flexible signal generation scheme to meet the excitation requirements of the variable-speed DESG. The development, the implementation, and the testing of the excitation system are described in the thesis. The implemented FR and VR schemes control the two excitation voltages simultaneously, but act independently. Experimental results showing the real-time performance of the excitation system and the response of a laboratory DESG driven at variable speeds are presented. These results show that the excitation system is flexible, fast acting, and accurate. The excitation system is flexible in that, the amplitude, the frequency, the frequency-range, and the phase sequence of the two generated excitation voltages can all be controlled dynamically (on-line). In addition, the waveform distortion of the excitation voltage signals can be specified on-line and, once specified, this distortion is independent of the frequency of the generated signals. With the FR and VR schemes both acting automatically, the DESG can supply power at any desired frequency and terminal voltage while its rotor is driven at a variable speed.
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Table 6.1: Values of the parameters $\alpha_0$ and $\alpha_1$ of the dynamic model of the DESG operating at constant speed. ........................................ 120
LIST OF SYMBOLS

\( \alpha_0, \alpha_1 \)  
parameters of the dynamic model of the DESG operating at constant speed:  
\( \alpha_0 = \frac{2\pi p L_s}{R_n}, \alpha_1 = \left(2\pi L_m/R_i\right)^2 \)

\( \beta \)  
sensitivity of analog signal to \( a \) in \( mV \ per \ unit \) of measured quantity

\( \varepsilon_{C_p} \)  
relative error in the count of pulses from the shaft encoder, \( C_p \)

\( \varepsilon_{\phi_m} \)  
relative error in the incremental angle \( \phi_m \)

\( \varepsilon_{C_t} \)  
relative error in the count representing the constant elapsed time (CET), \( T_m \)

\( \varepsilon_{C_s} \)  
relative error in calculation of speed.

\( \varepsilon_{C_p} \)  
relative error in the spacing of pulses from the shaft encoder.

\( \phi_m, \Delta\phi \)  
incremental rotational angle

\( \Phi \)  
resultant stator linkage magnetic field riding on the rotor.

\( \Phi_d \)  
stator linkage flux along the direct-axis (d-axis).

\( \Phi_m \)  
peak amplitude of the rotating magnetic field \( \Phi \).

\( \Phi_q \)  
stator linkage flux along the quadrature-axis (q-axis).

\( \gamma \)  
phase angle, a function of the parameters of the field windings of the DESG.

\( \eta \)  
control factor for a specified DAC, \( \eta = \sum S_i 2^i \), where \( i = 1, \ldots, 12 \) for a 12-bit DAC, and \( S_i \) denotes the setting of the bits, i.e. either 0 or 1.

\( \varphi \)  
control function, law or algorithm, e.g. P, PI, PID algorithms.

\( \lambda_0, \lambda_1 \)  
parameters of the dynamic model of the DESG operating at constant slip.

\( \mu \)  
number of pulses per revolution that will be generated by a shaft encoder.
\[ \theta, \theta_a \]  phase angle defined as \( \theta = 2\pi s f_0 t, \ \theta_a = 2\pi s f_0 t_a. \]

\[ \rho \]  saliency factor, defined as the ratio \( i_{ol}/i_{lq}. \)

\[ \sigma \]  filter coefficient

\[ \tau_{iv} \]  time constant of the \( i^b \) block of the VR loop.

\[ \tau_{if} \]  time constant of the speed transducer block of the FR loop.

\[ \omega_0 \]  synchronous speed in rad./sec., i.e. \( \omega_0 = 2\pi f_0 \)

\[ A \]  amplitude of the digitized pattern waveforms.

\[ b \]  number of \textit{bits} in the DAC data format.

\[ C_t \]  count representing the time \( T_m \), also called the constant elapsed time (CET)

\[ C_p \]  a count of the encoder pulses accumulated during the time interval \( T_m \).

\[ C_{en} \]  a count of the encoder pulses during the negative half cycle of the timing signal.

\[ C_{ep} \]  a count of the encoder pulses during the positive half cycle of the timing signal.

\[ C_{en} \]  a count of the pulses of the measurement clock frequency \( f_c \) during the negative half cycle of the timing signal.

\[ C_{ep} \]  a count of the pulses of the measurement clock frequency \( f_c \) during the positive half cycle of the timing signal.

\[ D, D_i \]  counter divider, integer data

\textbf{DRIVER}  a software program which \textit{controls or drives} a computer peripheral device.

\[ e, e(t) \]  terminal voltage error signal

\[ e_n \]  \( n^\text{th} \) sample of the terminal voltage error signal, \( e(t) \).

\[ f \]  frequency in Hz.

\[ f_0 \]  the frequency corresponding to \( n_o \).

\[ f_{ck} \]  clock frequency, output frequency from a counter.
$f_{da}$ frequency of the generated excitation voltage signals.

$f_{dcz}$ frequency that defines the \textit{dc-zone} for excitation control.

$f_m$ the frequency of the measurement timing signal, $f_m = 1/T_m$.

$f_{out}$ frequency of the terminal voltage of the DESG.

$f_r$ the frequency corresponding to $n_r$.

$f_s$ the slip frequency defined as $f_s = |s_r|f_0 = s_nf_0$

$G$ amplifier gain

$G_{sr}(s)$ transfer function of the speed transducer block of the FR loop.

$G_{ir}(s)$ transfer function of the $i^\text{th}$ block of the VR loop.

$G_{cv}(s)$ transfer function of the controller block of the VR loop.

$G_{gv}(s)$ transfer function of the DESG block of the VR loop.

$\text{INT}$ integerization function by truncation.

$J$ jump index, takes integer values only.

$k, nn, x, z$ integer, sample index

$K_{sv}$ gain factors of the transfer functions of VR blocks $i = 1, 2, \ldots, 5$.

$K_{cv}$ gain factor of the controller block of the VR loop.

$K_d$ derivative gain of the PID controller.

$K_{gv}$ gain factor of the transfer function of the DESG.

$K_i$ integral gain of the PID controller.

$K_{sf}$ gain factor of the speed transducer block of the FR loop.

$K_p$ proportional gain of the PID controller.

$L_a$ d- and q-axis magnetizing inductance between the stator phases and the field windings of the DESG
self-inductance of the d- and q-axis field windings of the DESG

number of samples per cycle of each waveform pattern.

maximum number of samples per cycle of each waveform pattern.

maximum number of samples per quarter cycle of each waveform pattern.

an integer; denotes a sampled form of a variable if used as a subscript.

the desired synchronous speed of the DESG, in rpm or rev./sec.

rotor speed, in rpm or rev./sec.

speed of the rotating magnetic field relative to the rotor.

number of pole pairs of the synchronous machine.

the differential operator $d/dt$.

takes the values 0, 1, 2, and 3 to denote the 1st, 2nd, 3rd and 4th quadrant of a cycle.

resistance of the field windings of the DESG

Laplace operator

slip defined as $s_r = (n_0 - n_r)/n_0$, $s_r(t)$ represents $s_r$ as an analog signal

the magnitude of the dimensionless slip, $s_r$.

the sign of the slip, $s_r$.

period of the FM clock, intersample time for each generated signal.

period of the generated excitation signals.

measurement time interval, also called the constant elapsed time (CET).

time, in seconds, $t_n$ corresponds to the $n$th clock pulse.

time increment.

an analog voltage signal.
\( U_{AM} \)  amplitude control signal.

\( U_I \)  bias excitation voltage, bias amplitude of the excitation voltage signals.

\( U_{ir} \)  instantaneous amplitude of the generated voltages, \( V_d \) and \( V_q \).

\( U_{\text{REF}} \)  reference supply voltage for a DAC

\( V_{\text{CK}} \)  clock voltage signal with frequency \( f_{\text{CK}} \).

\( v_d = V_{d}(t) \)  generated voltage signal for the direct-axis field winding

\( v_{id} = Gv_d \)  excitation voltage signal for supplying the direct-axis field winding

\( v_{iq} = Gv_q \)  excitation voltage signal for supplying the quadrature-axis field winding.

\( v_q = V_{q}(t) \)  generated voltage signal for the quadrature-axis field winding.

\( V_{ir} \)  instantaneous amplitude of the excitation voltages, \( V_{d} \) and \( V_{q} \).

\( V_{\text{REF}} \)  desired or reference terminal voltage of the variable-speed DESG.

\( V_t \)  terminal voltage of the variable-speed DESG.

\( w \)  physical quantity measurable by a digital computer.

\( W \)  filter window size, in number of sample points processed per update.

\( X_a \)  d- and q-axis magnetizing reactance between the stator phases and the field windings of the DESG, \( X_a = \omega L_a \)

\( X_{ir} \)  reactance of the d- and q-axis field windings of the DESG, \( X_{ir} = \omega L_{ir} \)
LIST OF ABBREVIATIONS

ADC  analog-to-digital converter
AVR  automatic voltage regulator
CET  constant elapsed time
CSCF constant-speed constant-frequency
D/A  digital-to-analog
DAC  digital-to-analog converter
DESG dual-excited synchronous generator
ETF  event-trigger-flag
FR   frequency regulation
LPF  low pass filter
MFF  measure-frequency-flag
MPU  microprocessor unit
PC   personal computer, microcomputer
RAM  random-access memory
VAVF variable-amplitude variable-frequency
VSCF variable-speed constant-frequency
VR   voltage regulation
1. INTRODUCTION

1.1 General

In conventional power systems, electrical power is generated and supplied to customers at constant frequency and constant voltage. Since a power system consists of several generators operating in parallel, the quality of the supplied power in the system depends on the quality of the control of the frequency and the regulation of the magnitude of the terminal voltages of these individual generators of the system. Most conventional generating systems are constant-speed constant-frequency (CSCF) systems. In these CSCF generating systems, the generators are driven at constant speed which is regulated to control the frequency of the supplied power. Typical CSCF generating systems include diesel-, hydro-, and thermal-power plants. The latter type includes nuclear plants and those that use fossil fuels, e.g. coal, oil, and natural gas, as energy sources. These CSCF generating systems use energy sources which are physically controllable and, thus, the speed of the generating units can be regulated by controlling the input power to their prime movers.

However, there are cases in which the energy sources can not be easily governed for power generation and, thus, they cannot be utilized through the use of CSCF generating systems. One example of such cases is that of power generation from wind [1 - 5]. Wind energy captured by a wind-turbine is intermittent, highly variable, and weather dependent. Due to the fluctuations in the captured wind energy, the wind-turbine runs at variable speed. This randomness of the turbine speed makes it difficult to use a wind-turbine as a prime mover in a CSCF generating system. A second example of these cases is that of using an aircraft engine to generate power for air-borne applications [6 - 9]. In this case, the engine runs at variable speed which depends on the flight conditions. Again, the use of a CSCF generating system may not be easy in this case. Also, tidal and storage pumped hydro
plants which operate at water-heads that change widely [3, 10] present a third example. In such hydro plants, the wide variation in the water-heads results in that the hydraulic turbines, and hence the hydrogenerators, run at variable speed. This makes it difficult to use the hydrogenerators in this case as CSCF generating units. In all these examples of power generation, it is still desirable to operate the generating units at variable speed while supplying electrical power at constant frequency and constant voltage. This could be possible by the application of one of the variable-speed constant-frequency (VSCF) generating systems [1, 8]. Although the goal in such VSCF generating systems is to generate power at constant frequency and constant voltage as in the case of the CSCF generating systems, the control techniques for achieving this goal in the VSCF systems differ greatly from the techniques used in the CSCF systems.

Overall, three main issues have to be considered when designing a generating system, its controllers and its interface with the power system [1]. These issues can be summarized as follows.

1. The **Frequency Stability**: This satisfies that the generating system will supply electrical power at constant frequency.

2. The **Voltage Stability**: This satisfies that the generating system will keep the terminal voltage constant.

3. The **Power Quality**: This satisfies that the generating system will supply power with no appreciable harmonics [11, 12].

It is the role of the controllers of a generating unit to maintain the frequency stability, voltage stability, and the power quality during both the transient and steady-state operating conditions of the generating unit. These three issues will be discussed in detail in the subsequent sections for both the cases of CSCF and VSCF generating systems.
1.2 Power Generating Systems

1.2.1 Constant-Speed Constant-Frequency Generating Systems

In all the CSCF generating systems used nowadays, synchronous machines are used as the generating units. Automatic speed governing systems and automatic voltage (excitation) regulators (AVRs) are used together with such machines to generate electrical energy at constant frequency and voltage with the desired frequency stability, voltage stability, and power quality. A conventional synchronous generator in a CSCF system uses d.c. excitation current which produces an air gap flux that is rotating together with the rotor. In this case, only the speed of the prime mover determines the frequency of the generated voltage. For a generator connected to an infinite bus, the operating speed should correspond to the frequency at which the infinite bus operates and this speed must be regulated accordingly. The speed control is accomplished by mechanical devices which regulate the flow of the energy source, e.g. water, steam, gas, or diesel fuel to the prime mover as shown in Fig. 1.1 [13 - 17]. In the case of a hydro power plant, the water flow to the hydraulic turbines is regulated by either a gate control scheme, a turbine blade-pitch control scheme or a combination of both. In the case of a thermal power plant, steam input flow to the steam-turbine is regulated by governor controlled valves and a combustion control scheme of the boiler. In a diesel-power plant, speed control is achieved by using a speed governor to regulate the fuel input to each diesel engine.

On the other hand, the d.c. excitation current of a synchronous generator is regulated by a voltage regulator (AVR) to keep the magnitude of the terminal voltage, \( V_t \), constant and to meet the reactive power requirement of the system. When a generator operates in an isolated network, the excitation is controlled to maintain the steady-state voltage within the specified limits, and to prevent unacceptable variations of the voltage during transient conditions (i.e. when large and sudden changes of load occur). Generators running in parallel in larger systems usually need additional control signals to share the total reactive load correctly between them. A schematic diagram of a typical voltage regulation scheme employing an AVR is shown in Fig. 1.2.
Figure 1.1: Speed control in conventional CSCF generating schemes utilizing controllable energy sources.

Figure 1.2: A conventional CSCF system utilizing an AVR to regulate the terminal voltage of the generator.
1.2.2 Variable-Speed Constant-Frequency Generating Systems

Accurate frequency control by regulating the speed of the prime mover is possible in a CSCF generating system because the energy sources used, such as water, steam, and diesel fuel, are physically controllable. However, such a frequency control scheme is not feasible when the energy source used is random in nature and uncontrollable, as it is in the case of wind energy. A conventional, d.c.-excited, synchronous generator driven at variable-speed will supply electrical power at variable frequency and variable voltage. Such a variable frequency power is not acceptable and will not allow the connection of the generating unit to a constant-frequency electrical grid. To overcome such restrictions, numerous variable-speed constant-frequency (VSCF) generating systems have been developed [6 - 10, 18 - 32]. These VSCF generating systems can be classified into three main categories:

1. Systems which use mechanical devices to convert a variable-speed drive to a constant-speed drive.
2. Systems which use static power converters to obtain constant-frequency power from variable-frequency power.
3. Systems which use variable-frequency excitation systems to obtain constant frequency output from the variable-speed generator.

These three categories of VSCF generating systems are illustrated in Fig. 1.3. A brief review of these generating systems follows.

1.2.2.1 Speed Control by Mechanical Techniques

In the VSCF generating schemes of this category, Fig. 3.1(a), the speed of the prime mover is regulated by mechanical devices. Then, a synchronous or an induction generator is driven at this regulated speed [8, 18]. Variable-gear ratio units together with variable blade-pitch wind-turbines are widely used in wind powered generating units to obtain almost constant speed drives. Such drives are ideal for driving induction generators. The control approach for regulating the turbine speed is to change the aerodynamic characteristics of
Figure 1.3: Block diagrams of various variable-speed constant-frequency (VSCF) systems.
the turbine blades in response to changing wind speed. Usually, the variable-gear units are used to select the speed range for operating the turbine. Such a control is known to minimize the effect of the fluctuations of the wind speed on the magnitude of the generated voltage and its frequency. In the case when a synchronous generator is used, the control of the field voltage of the generator allows the regulation of the magnitude of the terminal voltage [18]. The frequency stability and power quality mainly depends on the speed regulation which must take place in the presence of random variations of the wind speed and electrical disturbances. However, such VSCF generating systems require complex mechanical speed control schemes, and need frequent maintenance of the mechanical parts.

1.2.2.2 Use of Power Converters

A. Use of AC/DC/AC link systems

This method employs AC/DC/AC link systems which use static power converters for regulating the desired frequency. In these link systems, Fig. 1.3(b), a generator is driven at variable speed and rectifiers are used to convert the variable-frequency a.c. power to d.c. power. Then, this d.c. power is inverted to constant frequency a.c. power [1, 3, 4, 19-23]. These link systems are widely used in wind energy conversion systems. They have increased the possibility of capturing a larger fraction of the energy incident on the wind turbines. In general, an AC/DC/AC link decouples the variable-speed generator from the rest of the power system. This offers the advantage of eliminating any direct interaction between this variable-speed generator and the other generators in the system. However, rectifiers and inverters generate unwanted harmonics and, thus, the acceptability of the inverted a.c. power depends on the utility-specified maximum acceptable level of the harmonic content of the inverted power [11, 12]. The other disadvantages of this scheme are its relatively high cost, the requirement of an inverter control scheme which is usually complicated, and the need to supply reactive power to these power converters [23].
B. Slip-Power Recovery Systems

A slip power recovery system [24 - 27] employs an induction generator. The generator operates at speeds above the synchronous speed. In such a system, both the stator and the rotor windings of the generator are connected to the power network as shown in Fig. 1.3(c). Since the rotor power is at slip frequency, the rotor winding has to be connected to the network via a static frequency changer which is usually an AC/DC/AC link of lower rating than that used in the system represented by Fig. 1.3(b). In this setup, the mechanical power is converted to electrical power and fed to the network partly through the stator winding and partly through the rotor winding. The power output from the rotor is proportional to the slip. This double output feature makes it possible to feed more than the rated power of the generator to the network without overheating the machine. This system absorbs reactive power from the network and thus compensation may be needed [23].

C. Rotor Resistance Control Technique

This technique employs an induction generator with variable resistance in the rotor circuit [6, 7, 28, 29]. It is a special case of the slip-power recovery system of Fig. 1.3(c) in that, the slip power is not fed to the power network. Instead, this slip power is dissipated in the rotor circuit resistance. In some cases, the heat dissipation in the rotor circuit requires special cooling systems [28, 29]. In this technique, the speed-torque characteristic of the induction generator is adjusted to match the input power by adjusting the external resistance connected in the rotor circuit of the generator. The operation of this scheme is also limited to a range of speeds above the synchronous speed of the induction machine. Overall, the power loss in the rotor reduces the efficiency of the generator setup.

1.2.2.3 Variable-Frequency Excitation Systems

The generator setups used with this method are designed to generate voltage at constant frequency in spite of the variation in the prime mover speed, as long as the speed varies within a specified range. This is achieved by electrical means which result in the production of a synchronous flux in the generators used. The term synchronous flux refers to the
magnetic field in the generator that rotates at synchronous speed relative to the armature of the generator. This synchronous flux will induce in the armature a voltage of constant frequency. Such machines are usually called asynchronized synchronous generators [6-10, 30-37].

The basic control approach in this technique involves supplying variable frequency excitation currents to the rotor of the generator as illustrated in Fig. 1.3 (d). The frequency of these excitation currents should be equal to the slip frequency, \( f_s \), which is defined as the magnitude of the difference between the desired synchronous frequency of the machine, \( f_0 \), and the frequency corresponding to the speed of the rotor of the generator, \( f_r \), i.e. \( f_s = |f_0 - f_r| \). The sign of the quantity \( f_0 - f_r \), which is equal to the sign of the rotor slip, determines the phase sequence of the excitation currents. These excitation currents can be supplied as three- or two-phase currents depending on the number of the field windings in the rotor of the generator [30-33]. The field windings are usually identical and only electrically phase shifted from each other. The phase shift is 120 electrical degrees in a rotor with three field windings [30, 31], and 90 electrical degrees in a rotor with two field windings [32-37]. For the case of a rotor having two field windings, the generator is usually referred to as a dual-excited synchronous generator (DESG) and its excitation scheme is also known as the two-axis rotor excitation technique [32-37]. In this thesis, a DESG has been chosen to implement a computer-controlled VSCF generating system. Since the three-phase rotor winding can be replaced analytically by an equivalent two-phase winding, the use of a DESG in the study represents all asynchronized synchronous machines. These machines have been recognized as the most versatile and economical VSCF schemes. Their reactive power can be controlled by the excitation system. In addition, these machines, when operated as synchronous generators, have higher stability limits compared to the conventional synchronous generators [10, 34, 37]. However, in order to utilize the DESG as a VSCF generating system, controlled two-phase excitation currents should be supplied to its rotor.
1.3 Excitation System for A Variable-Speed Dual-Excited Synchronous Generator

The underlying principle of operation of a DESG is that the two-phase (a.c.) excitation currents fed into its rotor produce a magnetic field that rotates relative to the rotor. This relative rotation of the field is at such a speed and in such a direction that the frequency of the generated voltage is always constant. In other words, the magnetic field rotates at slip frequency relative to the rotor and at synchronous speed relative to the stator of the DESG. Based on this principle, the realization of the VSCF operation of the DESG depends on the ability to generate and control these two-phase excitation currents. Due to this fact, the excitation problem becomes a problem of generating and controlling low-frequency (0-100 Hz), two-phase, variable-amplitude variable-frequency (VAVF) voltage signals. The frequency of these signals should be equal to the slip frequency. Their phase sequence should be determined by the sign of the rotor slip. These excitation voltage signals should then supply the required rotor currents. The generation of such excitation signals could be done by various techniques [34, 38 - 54]. These techniques are either based on the frequency-converter method in which a fixed frequency from a local oscillator is mixed together with frequencies from a variable frequency source [48] or on the method of frequency division by digital combinational circuits.

In the frequency-converter method, the local oscillator supplies a fixed reference frequency to the mixing device (mixer). Then, another controllable variable-frequency source is used to supply frequencies for mixing with the fixed reference frequency. The mixer output is generally characterized by harmonic components having frequencies consisting of sums and differences of multiples of the variable input frequencies and the fixed reference frequency. Most of these frequency components are unwanted and, hence, low pass filters are used to obtain the desired low frequency output from the mixer. This scheme of frequency synthesis applies to every phase generated. In this method, the phase information of each generated signal is expected to be preserved in the frequency mixers. In addition, control signals are needed for the control of the magnitude, the frequency, and the phase sequence of the generated signals.
In the frequency division method, output frequencies are synthesized by dividing a reference frequency by integer dividers which are programmed on digital counters [49-54]. The desired waveforms are obtained by using sampled data of the sine wave which are converted into analog values by clocked digital-to-analog converters (DACs). These frequency synthesis methods can be implemented by using different design techniques which can be classified into (a) analog designs, (b) digital designs, (c) hybrid designs, (d) designs that use power converters as frequency changers, (e) designs that use analog computers, and (f) microcomputer-based designs. Brief reviews of these design techniques are given in the following subsections.

1.3.1 Analog Designs

Analog designs use analog circuitry to generate the variable-frequency voltage signals [38, 40]. In these schemes, passive phase shifting networks are used to realize the required phase relationship between the output signals and for filtering the outputs of the mixers. The serious drawback of these analog designs is that the signals generated in the low-frequency range (0 - 100 Hz) are accompanied with a drift problem. This drift problem is caused by the sensitivity of the designs to the instability of the reference oscillators used. This sensitivity problem is solely due to mixing frequencies of comparable order of magnitudes. The performance of these analog circuits suffers from errors due to aging of components and the environmental factors, e.g. temperature. Hence, the design of the analog circuits requires careful component selection to achieve the desired accuracy in the phase relationships and in the frequency of the generated signals. Also, the harmonic distortion of the output signals depends on the output frequency. In fact, it is difficult to realize frequencies close to zero (0 - 5 Hz) due to the filtering problems. Lastly, there is no easy way for generating different types of multiphase waveforms.

1.3.2 Digital Designs

Digital designs use digital logic circuits to synthesize signal waveforms. An example of these digital designs is the scheme reported in Reference 39. This method makes use of
a programmable-read-only-memory (PROM) containing coded numerical values of the sine wave for 32 steps between 0° and 90° per phase. During the signal generation process, these coded reference data are loaded from the PROM into the output buffer at predetermined time intervals. Then, these output buffers drive a set of DACs, one per phase. The DACs convert the digital values into analog values to produce the desired sine waves. The timing for the sampling process is controlled by up/down counters. About a decade ago, this scheme was assessed as expensive and complicated [45]. At that time, many of the components used in the scheme were expensive and limited in capability, e.g. the PROMs used have limited storage capacity for the pattern tables. These parts are primitive by today’s standards. As it will be discussed later in this thesis, this design technique, when implemented on a microcomputer, offers many advantages that overcome most of the drawbacks of the other methods. One main cause of waveform distortion in digital designs is the integerization procedure to obtain the sample values. This procedure can be done either by roundoff or truncation. The other main cause of waveform distortion is the integration of these samples by the DACs to produce stepped analog outputs.

1.3.3 Hybrid Designs

Hybrid designs use both analog and digital circuits for synthesizing variable-frequency waveforms [41, 45, 46]. In these designs, digital logic is used to determine the output frequency and the phase sequence of the output signals. On the other hand, hybrid circuitry is used to determine the output amplitude and the waveform shape of the generated signals. In Reference 41, the three-phase sine waves are produced by DACs as in Reference 39. The difference between these two schemes is that, in Reference 41, the sine pattern data are hardwired into the 6-bit DACs used. This is achieved by using normalized resistor values which are selected to be equal to the value of the sine function for every 15° from 0° to 90°. Hybrid designs share the same disadvantages as the analog designs. Relatively, these schemes are more expensive and complicated when compared to their analog counterparts.
1.3.4 Designs Which Use Analog Computers

A programmable method using analog computer simulation method for generating sine wave signals is described in Reference 42. Although, the method appears to be elegant and programmable, the main disadvantage of the scheme is the large number of components used which have to be selected carefully.

1.3.5 Use of Power Converters

The use of power converters as frequency changers is another technique for sine wave synthesis. A power converter is an array of static power switches (e.g. thyristors and triacs) arranged to close and open the supply voltage to a load at controlled time intervals. This switching process constitutes the mixing of an input fixed frequency of the supply voltage and a variable frequency from the switching controller to generate an output frequency. An example of such power converters is the cycloconverter [48, 55, 56]. This static device is capable of directly converting single or polyphase a.c. power of a given frequency to a single or polyphase a.c. power of a chosen output frequency. The output frequency is lower than the input supply frequency. In fact, cycloconverters are dominantly used for supplying variable frequency excitation power to generators in VSCF generating systems [9, 10, 30 - 32, 36]. Of course, the main disadvantage of these frequency changers is that they are harmonic generators [11, 12]. The other drawback is that, in general, good quality output waveforms can be produced from a cycloconverter only over a narrow frequency range, usually up to one fourth of the input supply frequency. This gives a frequency range of 0 - 15 Hz for a 60 Hz supply. These power converters also require complex switching control circuits. Naturally, increasing the number of switches used or/and the input supply frequency would reduce the harmonic distortion of the synthesized waveforms. Essentially, this is expensive.
1.3.6 Microcomputer-Based Method

An earlier study by the author [57, 58] demonstrated that it is feasible to use a digital computer to generate the excitation voltage signals and to eliminate the drawbacks of the other previous techniques mentioned above. In the feasibility study, a computer-based digital-to-analog (D/A) conversion process which uses numerically generated pattern data of sinusoidal waveforms was used to synthesize variable-amplitude variable-frequency voltage signals. The results of the feasibility study demonstrate that the digital signal generation technique is suitable for generating and controlling the two-phase excitation voltage signals for the variable-speed DESG. This computer-based technique offers four main advantages. Firstly, the technique is a software-based approach for generating variable-amplitude variable-frequency sinusoidal waveforms of acceptable quality. Secondly, the technique gives total control on the distortion of the waveforms generated, i.e., the waveform distortion can be specified on-line and, once specified, this distortion is independent of the excitation frequency. Thirdly, the technique allows for on-line control of the range of the excitation frequencies, i.e., the frequency range can be changed dynamically. Lastly, the technique has a software-based flexibility for (a) generating multiphase waveforms which can be specified as mathematical functions, and (b) for varying the number of control options.

1.4 Objectives of the Research Project

The main objective of this thesis is to develop, implement and test a flexible, computer-based, real-time, two-phase, excitation system for a variable-speed dual-excited synchronous generator (DESG). This objective translates into the development of a computer-controlled VSCF generating system using a DESG which can supply power at constant voltage and constant frequency over a variable speed range. Based on the experience of the feasibility study [57 - 58], it is proposed to implement the excitation system on a distributed computing hardware. Use of a distributed computing approach gives modularity to the research. Modularity is expected to simplify the development, implementation and the testing of the excitation system. In order to meet the research objective, it is proposed to carry out the following investigations:
1. To develop a computer-based, real-time, two-phase excitation algorithm based on the excitation requirements of a variable-speed DESG.

2. To investigate the interface requirements, the timing and sampling requirements, and the measurements and signal processing requirements for solving the excitation problem. These investigations become necessary following the decision to use a distributed computing hardware for the study. Such a multi-process hardware should be provided with the means to exchange information, i.e. data and control commands, among the excitation system modules. The need to study the timing and sampling requirements reflects the awareness that real-time control requires critical timing to respond to real time responses. Also, synchronization of all the measurement and control processes is essential. Usually, such critical timing requires special signal interfaces between modules. The plan is to use dedicated plug-in cards to meet the signal interface requirements.

3. To develop and test all the required real-time application programs. It is intended that the developed programs should allow on-line and interactive experimentation. The goal is to take into account the findings from the investigations of stage 2 above to develop coordinated real-time application programs for the excitation system.

4. To implement the excitation algorithm on a microcomputer distributed platform which will be configured based on the results of the investigations of the first three stages.

5. To test the resulting excitation system and to evaluate its performance on a laboratory variable-speed DESG in the Rotating Machines Research Laboratory, University of Saskatchewan.
2. A DUAL-EXCITED SYNCHRONOUS MACHINE AND ITS EXCITATION REQUIREMENTS

2.1 Introduction

As discussed in Chapter 1, a dual-excited synchronous generator (DESG) can be used as a variable-speed constant-frequency (VSCF) generating system. This chapter describes in details the basic principles of such a generator and its excitation requirements when employed as a VSCF generating system. A structure of a computer-based system that can meet the excitation requirements of the DESG in real time is proposed. Finally, the main blocks which characterize the functional relationships in the proposed excitation system are identified and discussed.

2.2 Basic Principles of A Dual-Excited Synchronous Machine

A DESG has a three-phase armature winding on the stator and a laminated rotor which is constructed such that, for each pole, it has two sets of identical excitation windings [32 - 37]. One winding is on the pole-axis (direct- or d-axis) and the other winding is on the interpole-axis (quadrature- or q-axis). As a result of this construction, the two field windings are in quadrature with each other, i.e. 90 electrical degrees from each other. These two field windings are externally accessible via slip rings and both windings are usually capable of carrying the full-load excitation current. Figure 2.1 shows a typical schematic diagram of a DESG.
2.2.1 Excitation Requirements of A Dual-Excited Synchronous Machine

To operate a DESG in a VSCF generating setup, its two field windings should be supplied with two-phase variable-amplitude variable-frequency (VAVF) excitation voltages, identified as $v_{fa}$ and $v_{fq}$ in Fig. 2.1. These two excitation voltage signals should be sinusoidal and must meet, in real time, the following set of five requirements:

1. The two excitation voltage signals must have equal frequencies.
2. The frequency of these signals must be equal to the slip frequency, \( f_s \). This frequency is defined by \( f_s = |s| f_0 = s_m f_0 \), where \( s \) is the rotor slip defined as the ratio \( s = (n_0 - n_r)/n_0 = (f_0 - f_r)/f_0 \) and \( s_m \) is the magnitude of the rotor slip. In this definition, \( n_0 \) (rev./sec.) is the required synchronous speed of the DESG, \( n_r \) (rev./sec.) is the rotor speed, \( f_0 = pn_0 \) (Hz), is the synchronous frequency, \( f_r = pn_r \) (Hz) is the frequency corresponding to the rotor speed, and \( p \) is the number of pole pairs of the DESG.

3. The two excitation voltages must be orthogonal, i.e. 90 degrees phase shifted from each other.

4. The phase sequence of the two voltages should be controlled by the sign of the rotor slip, \( \text{sign}[s] = \text{sign}[n_0 - n_r] = \text{sign}[f_0 - f_r] \), in such a way to compensate for the difference between the rotor speed, \( n_r \), and the synchronous speed, \( n_0 \), of the generator.

5. The amplitude of these excitation voltages, \( V_{fr} \), should be controlled by the terminal voltage error, \( e = e(t) \), in a way to nullify the deviations of the magnitude of the terminal voltage, \( V_t \), from the required magnitude, \( V_{REF} \).

Practically, the sources of the voltage signals \( v_{id} \) and \( v_{iq} \) should be capable of supplying the required excitation power to the DESG. But, the use of a microcomputer to generate voltage signals will only produce signals at digital logic current levels. Thus, the generation of the excitation voltage signals should have two stages, firstly, to generate the two-phase voltage signals at low current levels, \( v_d \) and \( v_q \), and secondly, to amplify these signals to obtain the required high current signals \( V_{id} \) and \( V_{iq} \). If \( G \) is the gain of the amplifiers that have to be used to obtain the required excitation power, then, the waveforms of the excitation signals can be described as follows:
\[ v_d = U_r \cos(\text{sign}[s_r]2\pi f_s t) \]  
\[ v_q = U_r \sin(\text{sign}[s_r]2\pi f_s t) \]  
\[ U_r = U_f(1 - \varphi(e)) \]  
\[ v_{fd} = G v_d \]  
\[ v_{fq} = G v_q \]  
\[ V_{ff} = GU_{ff} \]  

where \( U_r \) is the amplitude of the signals \( v_d \) and \( v_q \), \( U_f \) is the bias amplitude of the two voltage signals (value of \( U_r \) when \( \varphi(e) = 0 \)), and \( \varphi \) is a control algorithm which is a function of the voltage error \( e(t) \).

2.2.2 The Concept of a Rotating Magnetic Field

The two excitation voltages \( v_{fd} \) and \( v_{fq} \), Fig. 2.1, supply the required excitation currents \( i_{fd} \) and \( i_{fq} \) to the d- and q-axis excitation windings, respectively. At no load, the current \( i_{fd} \) in the d-axis excitation winding produces a flux \( \Phi_d \) along the d-axis, and the current \( i_{fq} \) in the q-axis excitation winding produces a flux \( \Phi_q \) along the q-axis. These two orthogonal fluxes, \( \Phi_d \) and \( \Phi_q \), produce a resultant rotating flux \( \Phi \) (Fig. 2.2) which has a constant amplitude. To generate constant-frequency constant-magnitude voltage from a variable-speed DESG, the flux \( \Phi \) should have the appropriate magnitude and should rotate at the synchronous speed (corresponding to the desired output frequency) with respect to the stator. Such a behaviour of the resultant flux \( \Phi \) requires that the excitation voltages \( v_{fd} \) and \( v_{fq} \) be generated and controlled dynamically in real time.

With the assumption that the two field windings are electrically identical, the fluxes \( \Phi_d \) and \( \Phi_q \) produced by the two orthogonal excitation voltages \( v_{fd} \) and \( v_{fq} \) respectively, and the resultant flux \( \Phi \) can be described as follows.
\[ \Phi_d = \Phi_m \cos(\text{sign}[s_r]2\pi f_st + \gamma) \]  
\[ \Phi_q = \Phi_m \sin(\text{sign}[s_r]2\pi f_st + \gamma) \]  
\[ \Phi = \Phi_d + j\Phi_q = \Phi_m \left(\text{sign}[s_r]2\pi f_st + \gamma\right) \]  
\[ \Phi_m = \sqrt{\Phi_d^2 + \Phi_q^2} \]

where \( j \) is the complex plane notation, \( \gamma \) is an angle which depends on the parameters of the field windings, and \( \Phi_m \) is the magnitude of \( \Phi \) which is a function of the voltage error \( e \).

![Phasor diagram](image)

**Figure 2.2:** The phasor representation of the two orthogonal fluxes \( \Phi_d \) and \( \Phi_q \) in a d-q frame in a dual-excited synchronous generator.

Equation (2.9) clearly shows that this resultant flux \( \Phi \) rotates at a relative speed \( n_r = f_s/p \) with respect to the rotor. The direction of rotation of \( \Phi \) should be in the same direction as the rotor if \( \text{sign}[s_r] = +1 \), or should be in the opposite direction to that of the rotor if \( \text{sign}[s_r] = -1 \). For \( f_s = 0 \), the flux \( \Phi \) will rotate together with the rotor, i.e. stationary with respect to the rotor, and this corresponds to the case of conventional d.c. excitation currents. Also, Eqns. (2.7) to (2.9) show that the control of the direction of rotation of \( \Phi \)
is possible by dynamically controlling the phase sequence of the excitation voltages \( v_{d} \) and \( v_{q} \). The slip sign, therefore, is a sufficient control parameter for dynamically selecting the appropriate phase sequence of the two-phase excitation voltages. Reversal in the direction of rotation of the flux \( \Phi \) can be observed by reversing the polarity of one of the excitation voltage signals or by interchanging the two voltage signals of the two field windings. With this type of excitation control, the speed of the rotating flux \( \Phi \) with respect to the rotor, \( n_r \), can be dynamically superimposed on the rotor rotation, \( n_r \), to realize a regulated speed of \( \Phi \) relative to the stator, i.e. \( n_0 = n_r + \text{sign}(s) n_r \). The flux \( \Phi \) rotating at this regulated relative speed will induce a constant armature frequency, \( f_a \). This is the basic strategy for controlling the excitation of a DESG operating as a VSCF generating system. In this thesis, this strategy of superimposing the flux rotation on the rotor rotation is referred to as the frequency regulation (FR) scheme [57 - 60]. The FR scheme is, in essence, a frequency modulation scheme, where the desired synchronous frequency, \( f_0 \), is modulated by the rotor slip such that \( \text{sign}(s) f_s = s f_0 \). The result of this modulation is then added to the frequency \( f_r \) that corresponds to the rotor speed, \( n_r \), to give the output \( f_{out} = f_0 \).

On the other hand, the magnitude of the resultant flux, \( \Phi_m \), should be controlled such that the terminal voltage of the DESG is kept constant. This can be accomplished by adjusting the amplitudes of the excitation voltages, \( V_{fr} \), as a function of the terminal voltage error \( e(t) \), i.e. \( V_{fr} = GU_{fr} = U_f(1 - \varphi(e))G \) (Eqns. (2.3) and (2.6)). This amplitude adjustment has the form of a negative amplitude modulation scheme, where the voltage error signal, \( e(t) \), processed according to some control function \( \varphi \), is the modulating signal. The effect of this amplitude modulation is to keep the terminal voltage constant. In this thesis, this amplitude control is referred to as the voltage regulation (VR) scheme [60].

### 2.3 The Excitation Control Problem

Equations (2.1) through (2.6) describe the excitation voltage signals which, when used to excite a variable-speed DESG, will result in the regulation of the output frequency, \( f_{out} \), and the regulation of the magnitude of the generator terminal voltage, \( V_f \). These two
regulation schemes, FR and VR schemes, can both be accomplished by controlling specific parameters of the excitation voltages. These two schemes should act simultaneously, but independently. Figure 2.3 shows a schematic diagram which illustrates a conceptual excitation system with such FR and VR schemes.

2.3.1 The Frequency Regulation Control Loop

The frequency regulation (FR) scheme is a feed forward scheme which uses the rotor slip (frequency) as the error information [31, 59, 60]. The block diagram for this scheme is shown in Fig. 2.4. In this figure, s denotes the Laplace operator as used in expressing transfer functions. The transfer function \( G_{fr}(s) \) represents the speed transducer. The variable speed operation of the DESG controlled by the FR loop is such that:

\[
f_{out} = \{f_0 - G_{fr}(s)n_r\} + pn_r \tag{2.11}
\]

Theoretically, \( G_{fr}(s) = p \) (the number of pole pairs of the DESG) so that the output of the FR loop is an algebraic summation of the slip frequency and the frequency \( f_r \) to give \( f_{out} = f_0 \).

Proper operation of this loop requires that \( f_s = f_s(t) \) and \( sign[s_r] \) be measured continuously in real time. Due to this measurement process, the transfer function \( G_{fr}(s) \) may introduce some delay in the FR loop. The accuracy of this loop in regulating \( f_{out} \) will depend on the accuracy in measuring or specifying the reference/system frequency, \( f_0 \), and on the accuracy of measuring the rotor speed, \( n_r \). There is no stability problem within the FR loop because this loop is a feed forward scheme.

2.3.2 The Voltage Regulation Control Loop

The main blocks that characterize the voltage regulation (VR) scheme are shown in Fig. 2.5. This VR control loop is a feedback scheme which uses the terminal voltage error signal \( e(t) \) to adjust the amplitude of the excitation voltages [61]. The task of this VR
Figure 2.3: A two-phase excitation scheme for a variable-speed dual-excited synchronous generator (DESG).

Figure 2.4: A block diagram showing the structure of the frequency regulation (FR) scheme of the proposed excitation system.
Figure 2.5: A block diagram showing the structure of the voltage regulation (VR) scheme of the proposed excitation system.
scheme is to keep the terminal voltage $V_t$ constant. In real-time operation, the VR will regulate $V_t$ by adjusting $V_{se} = GU_{se}$. However, the VR loop may have the tendency toward instability because it is a feedback control system. In Fig. 2.5, the tuning of the VR loop to achieve the voltage stability can be dealt with by selecting, by design and/or synthesis, suitable transfer functions for the controller $G_c(s)$, stabilizer $G_s(s)$, limiters $G_n(s)$ and the filter $G_{sv}(s)$. This filter, $G_{sv}(s)$, is for conditioning the measured terminal voltage for feedback purposes.

### 2.3.3 Overview of the Basic Hardware Requirements for the Study

As stated in the objectives of the thesis in Chapter 1, a distributed computing hardware will be used to investigate the excitation problem. Therefore, such a computing hardware will form the major part of the computing platform for implementing the excitation system. Figure 2.6 shows a conceptual layout of the platform. This layout has a multi-process structure. In a multi-process system, several processes take place simultaneously in real time. Then, there is the concern of the interfacing of the computing platform to the real world, both for input and output purposes. Plug-in cards have been identified as suitable for meeting this interface need [66]. In addition, power amplifiers are needed for amplifying the generated excitation signals. In Fig. 2.6, the layout of the computing platform has three main stages. The first stage consists of the transducers required for real-time signal measurement. Tracking of $V_o$, $V_{REF}$, $n_r$, and $n_0$ has to be done continuously and in a synchronized fashion. From these measurements, the control signals $e(t)$ and $s_i(t)$ or $sign[s_i(t)]f_i(t)$ can be derived and conditioned for computer processing and control.

The second stage of the layout of Fig. 2.6 is the computer-based signal generator. This stage has three main blocks, namely, the input, processing and control, and the output blocks. To allow for maximum flexibility and modularity each of these blocks is a personal microcomputer (PC). This approach was verified during the feasibility study [57] as appropriate for this type of research. There are several ways to input to and output data from a PC. Figure 2.7 shows some of these interfaces. Data can be input to a PC via analog-
Figure 2.6: Hardware layout of a conceptual computer-based excitation system for a variable-speed DESG.
Figure 2.7: Typical system I/O support of a personal computer.
to-digital converters (ADCs), timers, digital I/O data lines, the keyboard or loaded from mass storage devices such as floppy diskettes and hard drives. On the other hand, data can be output from a PC via digital-to-analog converters (DACs), timers, digital I/O data lines, or displayed on the computer video monitor (at programmable precision) or stored on mass storage devices. However, the process of inputting data to or outputting data from a PC requires proper timing. A dedicated programmable clock is required to provide this timing. This clock may be an internal component of the PC or external from the PC.

The third stage consists of the amplifiers. Since two-phase voltage supply is to be generated, a dual power amplifier setup is required. The type of amplifiers suitable for this study should be able to amplify both a.c. and d.c. voltage signals. Thus, operational power amplifiers are the best candidate for this application. The ability to amplify both a.c. and d.c. signals will allow the DESG to operate at subsynchronous, synchronous, as well as supersynchronous speeds. Furthermore, since the phase sequence of the excitation signals is controllable, the flow of the excitation power will be always into the generator.

2.4 Dynamic Model of A Variable-Speed Dual-Excited Synchronous Generator Operating at No-Load

Figure 2.8 illustrates the proposed structure of an input-output dynamic model of the variable-speed DESG. The inputs to the model, Fig. 2.8(a), are the two-phase excitation voltage signals, \( v_{rd} \) and \( v_{rq} \), and the speed of rotation \( n_r \) of the generator rotor. The outputs of the model are the magnitude of the terminal voltage, \( V_t \), and the frequency of the terminal voltage, \( f_{out} \). Figure 2.8(b) and (c) reinforces the fact that the regulation of \( f_{out} \) and \( V_t \) can be accomplished separately. In Fig. 2.8(c), for the purpose of regulating the magnitude of the terminal voltage, the DESG can be treated as having one equivalent field winding which is supplied with the voltage \( V_{ff} \). Thus, if saturation effects are neglected, the DESG operating at no-load can be modelled as a first order system [31, 37, 62 - 64].
Figure 2.8: Proposed structure of the dynamic model of the variable-speed DESG.

The dynamic behaviour of the DESG will depend mainly on the behaviour of the gain factor $K_{gv}$, Fig. 2.8(c). It is therefore important to know how this gain factor varies with the different operating conditions of the variable-speed DESG. The general behaviour of $K_{gv}$ can be deduced from the steady-state performance of the DESG (operation at constant slip). Such an operation of a DESG is investigated in Reference 59. The reported analysis shows that, when the effect of saturation is neglected and there is no armature current, the magnitude of the terminal voltage, $V_t$, is linearly related to the magnitude, $V_{ff}$, of the excitation voltages. If $L_a$ is the stator magnetizing inductance in both the d- and q-axis, $L_f$ is the self inductance of each field winding, and $R_f$ is the resistance of each field winding, the linear relationship between $V_t$ and $V_{ff}$ at constant slip, $s_r$, can be shown to be:

$$V_t = X_a V_{ff} / \sqrt{(R_f^2 + s_r^2 X_f^2)} \quad (2.12)$$
where $X_a = 2\pi f_0 L_a$ is the magnetizing reactance in both the d- and q-axis of the DESG, $X_{ff} = 2\pi f_0 L_{ff}$ is the reactance of each field winding, and $f_0$ is the synchronous frequency. Equation (2.12) is derived in Appendix A. From this equation, the gain factor $K_{gv} = \Delta V/\Delta V_{ff}$ is obtained as:

$$K_{gv} = \frac{X_a}{\sqrt{R_f^2 + s_r^2 X_{ff}^2}} \quad (2.13)$$

Since $s_r = \text{sign}[s_j] f_s / f_0$, where $f_0 = p(n_r + \text{sign}[s_j] f_s / p)$, Eqn. (2.13) can be rewritten to take the form:

$$K_{gv}(f_s, n_r) = \alpha_0 (n_r + \text{sign}[s_j] f_s / p) / \sqrt{1 + \alpha_1 f_s^2} \quad (2.14)$$

where $\alpha_0 = 2\pi p L_s / R_r$, and $\alpha_1 = (2\pi L_a / R_f)^2$.

The numerator of Eqn. (2.14) clearly shows that the dynamic behaviour of $K_{gv}$ is a linear function of the regulated synchronous speed $n_0$. This speed $n_0$ is a function of the rotor speed, $n_r$, the excitation frequency, $f_s$, and the sign of the slip, $\text{sign}[s_j]$. In fact, the factor $(n_r + \text{sign}[s_j] f_s / p)$ in the numerator describes the operation of the FR scheme. On the other hand, the gain $K_{gv}$ is inversely proportional to the impedance of the field windings and this is accounted for by the denominator of Eqn. (2.14). Since the excitation frequency will vary when the DESG will be operating at variable speed, the impedance of the excitation windings will also vary and, thus, there will be a coupling effect between the FR and the VR control loops. Due to this coupling, the gain factor will not be a constant. In the following sections, three cases of Eqn. (2.14) are investigated for $L_a = 71.9539 \, mH$, $L_{ff} = 77.4262 \, mH$, $R_r = 1.538 \, \Omega$, $p = 2$, and $n_o = 1800 \, rpm$ (rated speed) for operation at $f_0 = 60 \, Hz [59]$. The three cases are (a) variable $f_s$ at constant speed $n_r$, (b) constant $f_s$ at variable speed $n_r$, and (c) when both $f_s$ and $n_r$ are variable but $n_0$ is constant.
2.4.1 Constant Rotor Speed Gain Curves at Variable Excitation Frequency

Figure 2.9 shows a sample of the gain curves as a function of the excitation frequency for different rotor speeds. One aspect of these curves is that, for each value of \( f_s \), the value of \( K_{gv} \) for \( \text{sign}[s_j] = -1 \) is smaller than that for \( \text{sign}[s_j] = +1 \). This is attributed to the fact that the corresponding value of \( n_0 \) for \( \text{sign}[s_j] = -1 \) is smaller than that for \( \text{sign}[s_j] = +1 \). This shows the effect of changing the phase sequence of the excitation voltages at constant rotor speed.

The other aspect of the curves of Fig. 2.9 is that each curve gives only one operating point at which the DESG will generate voltage at a constant output frequency, \( f_0 \). This aspect can be illustrated by the following example. Suppose that the generator is running at \( n_r = 2250 \text{ rpm} \). At this speed the generator should be excited with \( f_s = 15 \text{ Hz} \) and \( \text{sign}[s_j] = -1 \) to generate power at 60 Hz. In this case, the 2250 rpm-gain curve (Fig. 2.9) has to be used to determine the value of \( K_{gv} \). From Fig 2.9, this value is 3.6. Now, consider that the generator speed is changed to 1350 rpm. In this case, \( f_s = 15 \text{ Hz} \) and \( \text{sign}[s_j] = +1 \), and now the 1350 rpm-gain curve has to be used to obtain the value of \( K_{gv} \), which is equal to 3.6. The striking fact of these two operating cases is that the two gains from the two curves are equal. This is due to the fact that the synchronous frequency of the magnetic field \( \Phi \) is equal to 60 Hz for both cases, i.e. \( n_0 = 1800 \text{ rpm} \).

2.4.2 Constant Excitation Frequency Gain Curves at Variable Rotor Speed

From Eqn. (2.14), the behaviour of the gain \( K_{gv} \) at constant \( f_s \) and \( \text{sign}[s_j] \) can be described by a model of the form:

\[
K_{gv}(n_r, f_s) = \lambda_0 + \lambda_1 n_r
\]  

(2.15)
Figure 2.9: Constant speed gain curves showing the variation of $K_{gv}$ with excitation frequency.
where \( \lambda_0 = (\alpha_0 \text{sign}[s_J] f_s/p) / \sqrt{1 + \alpha_1 f_s^2} \) and \( \lambda_1 = \alpha_1 / \sqrt{1 + \alpha_1 f_s^2} \) are parameters of the model. Equation (2.15) is linear in \( n_r \) as it is illustrated in Fig. 2.10. This figure shows a sample of the curves of \( K_{gv} \) plotted against the rotor speed, \( n_r \), for different excitation frequencies. Thus, allowing for a speed deviation of say \( \pm 25\% \) from \( n_0 = 1800 \text{ rpm} \) will also cause the gain \( K_{gv} \) to vary by \( \pm 25\% \) of its gain \( K_{gv,0} \) at \( n_r = 1800 \text{ rpm} \).

### 2.4.3 Constant Generating Frequency Operation Gain Curve

For the desired operation of the dual-excited synchronous generator (DESG) in a VSCF generating system, i.e. with the rotor driven at variable speed, \( n_r \), and the excitation frequency, \( f_s \), and the slip sign, \( \text{sign}[s_J] \) (i.e. the phase sequence), adjusted such that the relative speed, \( n_o \), of the field \( \Phi \) with respect to the stator is kept constant, i.e. \( n_o = n_r + \text{sign}[s_J] f_s/p \), there is an operating gain curve for each desired value of \( n_o \). This operating gain curve can be obtained from Eqn. (2.14) by specifying a constant value of \( n_o \).

Figure 2.11 shows the DESG gain operating curves for \( f_o = 50 \text{ Hz} \) and \( 60 \text{ Hz} \). These two curves correspond to synchronous speeds of \( n_0 = 25 \text{ rev/sec} \) and \( 30 \text{ rev/sec} \), respectively. It can be seen from this figure that the shape of the operating curve is symmetrical about the line \( f_s = 0 \). Also, the gain \( K_{gv} \) is very sensitive to the change in the slip frequency, \( f_s \). This behaviour of the gain can be described by:

\[
K_{gv}(f_s) = K_{gv,0} / \sqrt{1 + \alpha_1 f_s^2} \tag{2.16}
\]

where \( K_{gv,0} = \alpha_1 n_o \). For a \( \pm 25\% \) speed deviation from the synchronous speed of \( 1800 \text{ rpm} \), which corresponds to \( f_s = 15 \text{ Hz} \), the gain \( K_{gv} \) decreases by about \( 80\% \) of the maximum value \( K_{gv,0} \) corresponding to \( f_s = 0 \). This means that, if the terminal voltage of the DESG is regulated by a closed loop system, the \( \pm 25\% \) speed deviation will cause the effective open loop gain of the regulator system to vary from \( 100\% \) to \( 20\% \) of its value at \( f_s = 0 \). Thus, the terminal voltage regulator should be capable of compensating such a wide range of parameter variation.
Figure 2.10: Constant excitation frequency gain curves showing the variation of $K_{ge}$ with the rotor speed.
Figure 2.11: Constant generating frequency operation gain curve of the DESG for $f_0 = 50 \text{ Hz}$ and $60 \text{ Hz}$. 

\[ f_0 - f_r = \text{sign}[s_\text{r}] f_s \ (\text{Hz}) \]
2.5 Summary

This chapter has described the basic principles and the excitation requirements of a variable-speed dual-excited synchronous generator (DESG). The solution to the excitation problem has a frequency regulation (FR) scheme and a voltage regulation (VR) scheme. It has been shown that the excitation control of a DESG operating in a VSCF generating system can be achieved by generating the excitation voltages $v_d$ and $v_q$, described by Eqns. (2.1) through (2.6), amplifying them, and exciting the rotor of the DESG with the amplified signals, $v_{d'}$ and $v_{q'}$. In this way, the excitation problem becomes a signal generation problem in which a two-phase excitation supply is generated to satisfy, in real time, the excitation requirements of a variable-speed DESG. The computer-based technique used to generate the two-phase excitation supply is described in the next chapter. The software-based implementation of the signal generation technique is described in Chapter 5. The foregoing analysis of the variation of the gain factor $K_{gv}$ of the DESG operating at no-load has been presented as a background for the qualitative interpretation of the performance of the excitation system in Chapter 6.
3. THE MICROCOMPUTER-BASED REAL-TIME TWO-PHASE EXCITATION ALGORITHM

3.1 The Excitation Methodology

This chapter describes the microcomputer-based real-time two-phase excitation algorithm for realizing the frequency regulation (FR) and the voltage regulation (VR) schemes discussed in Chapter 2. The excitation algorithm deals with the real-time programmability of the excitation requirements of the dual-excited synchronous generator (DESG). In the work reported in References 57 and 58, the author describes the feasibility of a computer-based excitation control algorithm implementable on a multi-buffered computing environment. In such computing systems, data is accessed from memory only in units of buffers. This accessibility of data does not allow the processing of one data point at a time for real-time control. This chapter extends the buffer-based data processing approach to accommodate a point-based data processing approach. This point-based approach has proved to have more flexibility than the buffer-based approach [59]. The discussion in this chapter treats the excitation problem as a signal generation problem as discussed in Chapter 2.

The computer-based excitation algorithm employs a dedicated digital-to-analog (D/A) conversion process, which is driven by a real-time programmable clock, as a technique for generating the variable-amplitude variable-frequency (VAVF) excitation voltage signals for the variable-speed DESG. This signal generation approach is illustrated in Fig. 3.1. In this figure, DRIVERs A, B, and C denote real-time clocked software programs. These drivers control the two-channel digital-to-analog converter (DAC), whose channels are identified as DAC #1 and DAC #2. The timing of DRIVER A is controlled by CLOCK A and the timing of DRIVERs B and C is controlled by CLOCK B.
Figure 3.1: The block diagram showing the structure of the computer-based two-phase signal generation scheme.
The algorithm uses numerically computed samples of cosine and sine waves of specified amplitude, \( A \) (Fig. 3.1), as reference (pattern) data. The choice of these two orthogonal sinusoidal functions fulfils two of the excitation conditions of the variable speed DESG, i.e. the signals are sinusoidal and 90° phase shifted from each other. These reference samples are fed to the two-channel DAC, Fig. 3.1, during the D/A conversion process. These samples are sent to the DAC in a predetermined sequence and at controlled time intervals to generate the excitation voltages described by Eqns (2.1) - (2.6) of Chapter 2. Practically, the amplification of the excitation signals can be done after the low current signals are generated. For this reason, the gain \( G \) in Fig. 3.1 is placed outside the signal generator.

In the following derivations, \( f_{\text{CK}} \) denotes the sampling frequency of the clock (DRIVER A in Fig. 3.1) at which samples are sent to the DAC and \( f_{\text{sa}} \) denotes the frequency of the signal(s) to be generated. The reciprocal of \( f_{\text{CK}} \) gives the D/A intersample time \( T_{\text{CK}} \) (= the clock period) and the reciprocal of \( f_{\text{sa}} \) gives the period \( T_{\text{sa}} \) of the required generated voltage signal(s), as illustrated in Fig. 3.2. The real time \( t_n \) at the \( n \)th clock tick is equal to \( \Sigma (T_{\text{CK}}) \), where \( i = 1, \ldots, n \), and for a constant \( f_{\text{CK}} \), \( t_n = nT_{\text{CK}} \). A subscript \( n \) attached to a variable denotes the sampled form of the variable corresponding to the time \( t_n \). In Fig. 3.1, \( f_{\text{sa}} \) denotes the sample rate at which data is acquired by DRIVER B and DRIVER C, i.e. the rate of CLOCK B.

### 3.2 Synthesis and Control of the Frequency of the Excitation Voltage Signals

The DRIVER A in Fig. 3.1 is a clocked process for synthesizing and controlling the frequency of the excitation voltages. This driver is the major component of the frequency regulation (FR) scheme. Figure 3.2 shows a typical periodic, stepped, sinusoidal waveform of the output voltage generated by a continuous D/A conversion process synchronized by a real-time clock (e.g. CLOCK A in Fig. 3.1) of constant rate \( f_{\text{CK}} \). By inspecting Fig. 3.2, an angle \( \theta_n \) in radians can be associated with the stepped periodic signal at any
Figure 3.2: A periodic-stepped output voltage from a digital-to-analog converter driven by a clocked software driver.

Instant of time $t_n$ such that $\theta_n = 2\pi f_{da} n T_{CK}$. In terms of $\theta_n$, the excitation voltages described by Eqns. (2.1) and (2.2), for $G = 1$, can also take the form:

\[
\begin{align*}
  v_{dn} &= U_{th} \cos (2\pi f_{da} n T_{CK}) \\
  v_{qn} &= U_{th} \sin (2\pi f_{da} n T_{CK}) \\
  U_{th} &= A U_{AMn} \\
  U_{AMn} &= U_I (1 - \varphi(e_n))
\end{align*}
\]

where $e_n$ denotes the processed sample of the terminal voltage error signal, $e(t)$, at the $n^{th}$ clock tick, $U_{AMn}$ is an amplitude control update (Fig. 3.1), and $A$ is the amplitude of the digitized pattern waves.
If \( N \) is the number of samples per cycle in the D/A conversion process, the periodic output voltage will have \( N \) steps of equal width and thus, \( T_{da} = NT_{ck} \), from which \( f_{da} = f_{ck}/N \). This gives \( \theta_n = 2\pi n/N \) and Eqns. (3.1) and (3.2) can be rewritten as:

\[
\begin{align*}
\nu_{\text{dn}} &= U_{\text{in}} \cos (2\pi n/N) \\
\nu_{\text{qn}} &= U_{\text{in}} \sin (2\pi n/N)
\end{align*}
\]

(3.5) (3.6)

It can be deduced from Eqns. (3.5) and (3.6) that the \( N \) paired ordinates, \((\nu_{\text{dn}}, \nu_{\text{qn}}), n = 0, 1, 2, ..., N-1\), of the two sinusoidal functions are independent of the frequency to be generated. Thus, these values can be computed off-line and stored in the computer memory as a pattern lookup table. Also, it can be deduced from \( f_{da} = f_{ck}/N \) that the frequency of the output signals can be varied by dynamically varying either the number of samples per cycle, \( N \), the sampling frequency \( f_{ck} \) of the DAC driver (DRIVER A), or both. These two deductions constitute the main function of the FR scheme, which is performed by Driver A in Fig. 3.1.

In the application described in this thesis, the variable \( N \) represents contiguous memory locations where the pattern data are stored. For this reason, the values of \( N \) can be only integer values. Consequently, the major source of error in the signal generation technique is the round-off errors or quantization noise due to the finite number of steps (= \( N \)) within a cycle of each output waveform [49, 50, 57]. The number of samples per cycle \( N \) should be chosen such that the total waveform distortion of the stepped signals will not exceed the maximum specified level. Given a value of \( N \), the value of the voltage distortion factor (VDF) for such stepped waveforms can be determined by \( \text{VDF\%} = 180.01N/\pi \) [57, 58].

The harmonics responsible for the waveform distortion are integer multiples of the fundamental \( f_{da} \) and can be identified by the expression \((mN \pm 1)f_{da} \) [49, 50, 57] where \( m \) is a positive integer. It is therefore preferable to select and keep the value of \( N \) larger than a certain minimum value. For example, choosing \( N > 180 \) samples per cycle, gives a
distortion factor of less than one percent. Thus, the requirement for the amount of low-pass filtering to remove unwanted harmonics is greatly reduced. In fact, the excitation windings of the DESG may be a sufficient filter to smooth the excitation signals.

### 3.2.1 Slip Frequency Control Function

Accurate synthesis of the frequency $f_{da}$ of the two-phase excitation voltages requires continuous measurement of the slip frequency $f_s = |f_0 - f_r|$. This requires continuous measurement of the desired reference (system) frequency $f_0$ and the frequency $f_r$ which corresponds to the rotor speed $n_r$. Clearly, the FR scheme has four main tasks:

1. To measure the rotor speed, $n_r$, and the system (reference) frequency, $f_0$. From these measurements, the actual slip frequency, $f_s$, and the slip sign, $\text{sign}[s_r]$, can be determined (Fig. 2.4).

2. To select the appropriate value of $N$ and to synthesize the correct value of $f_{CK}$.

3. To generate $f_{da}$ by using $N$ and $f_{CK}$ from task (2).

4. To select the appropriate phase sequence of the excitation voltages based on the value of $\text{sign}[s_r]$.

The above four tasks have to be executed continuously in real time. To vary $f_{da}$ (the above first three steps) for variable speed operation of a DESG, either the clock frequency $f_{CK}$ or the number of samples per cycle $N$, or both, should be dynamically adjusted as functions of the processed absolute values of the slip signal, $s_r$, or the slip frequency, $f_s$. This can be accomplished by using the following slip frequency control functions.

\[
\begin{align*}
  f_{CK} &= NF_s = NF_{da} \quad (3.7) \\
  N &= \text{INT}(f_{CK}/f_s) = \text{INT}(f_{CK}/f_{da}) \quad (3.8)
\end{align*}
\]
Equation (3.7) is applied in the case when the value of $N$ is fixed and the clock frequency $f_{\text{CK}}$ is varied to control $f_{\text{da}}$. This equation describes a frequency modulation scheme of varying $f_{\text{CK}}$, which in turn varies $f_{\text{da}}$, with the slip $s_r$ as the modulating variable. The value of $N$ can be selected and fixed by using either known or directly computed set of $N$ samples per cycle of the cosine and the sine functions. On the other hand, Eqn. (3.8) is a frequency division scheme which is applied in the case when the clock frequency $f_{\text{CK}}$ is fixed and $N$ is varied to synthesize $f_{\text{da}}$. Overall, these two options, varying $f_{\text{CK}}$ and $N$ dynamically, enable the generation of the variable-frequency excitation voltage signals.

3.2.2 Timing Requirements and Frequency Synthesis by Clock Rate Control

The timing requirements for the signal generation (D/A conversion) process is critical because the generation of the variable-frequency voltage signals is achieved by both the variation of the clock rate $f_{\text{CK}}$ and the division of the clock rate by $N$. This requires manual or dynamic (on-line) programming of the clock rate, $f_{\text{CK}}$. This task could be accomplished by a separate clock driver, DRIVER C in Fig. 3.1. In addition, the D/A conversion process reconstructs the real time $t_n = \sum(T_{\text{ck}})_i$, where $i = 1, \ldots, n$ ($= nT_{\text{ck}}$ for constant $f_{\text{CK}}$) using the clock (CLOCK A). Therefore, for this application, it is desirable to select and use a reference clock of high rate (> 100 kHz) to allow for a wide variation of $f_{\text{CK}}$ and also for realizing fine quantization units of time. A quantization unit of time of the order of milliseconds allows for a relatively fine approximation and adjustments of the frequency $f_{\text{da}}$ of the generated excitation signals. Multi-stage timers can be used as clocks to meet such a requirement. Examples of such timers include the 8254 three-counter programmable interval timer and the 9513 five-counter integrated system timing controller, both having 16-bit counters [68]. The counters of these timers can be cascaded as shown in Fig. 3.3 to provide a flexible software-based programmable frequency synthesis setup. Each counter has to be loaded with an appropriate integer divider $D_i$ ($i = 1, 2, \ldots, N$) such that

$$D_i = \text{INT}(f_i / f_{i+1})$$  \hspace{1cm} (3.9)
where \( f_i \) is the input frequency to the counter stage and \( f_{i+1} \) is the desired output frequency from the counter. The determination of the values of these integer dividers \( D_i \) requires that \( f_i \) and \( f_{i+1} \) for each counter stage be known or specified in advance. The theoretical permissible range of values of each divider \( D_i \) (for a 16-bit counter) is \( 1 \leq D_i \leq 65535 \). The value \( D_i = 1 \) gives the maximum output frequency for a stage and the value \( D_i = 65535 \) gives the minimum output frequency for the stage.

![COUNTERS](image)

**Figure 3.3:** A block diagram of a multi-counter programmable timer.

The fine tuning of the output frequency of a particular timer stage depends on the reference frequency, \( f_C \) (e.g. the MPU clock or bus speed of the computer used) and the number of stages preceding it. The higher the reference frequency \( f_C \) is, the wider is the range of the clock sampling frequencies, \( f_{\text{CK}} \). Also, more counter stages cascaded can provide more flexibility for frequency variation. However, in practice, the minimum value of each divider (hence the maximum output frequency of each stage) will be determined by the efficiency and the speed of execution of the DAC software driver (DRIVER A in Fig. 3.1).
3.2.3 Dynamic Control of the Waveform Distortion, the Number of Samples per Cycle, and the Phase Sequence

Figure 3.4 shows a two-dimensional pattern lookup table which holds a specified maximum number of equispaced samples per cycle, $N_m$, for both the cosine and the sine waves of specified amplitude, $A$. In Fig. 3.1, the value of $A$ is set to unity for convenience. The angular spacing between the consecutive samples for each waveform is $2\pi/N_m$. A sample index $k$ ($= 0, 1, 2, \ldots, N_m-1$) points to a pair of these reference samples, i.e $v_d[k] = \cos(2\pi k/N_m)$, $v_q[k] = \sin(2\pi k/N_m)$. The values of $N$ can be dynamically derived from a dedicated software pointer control process. This software pointer will scan the pattern lookup table containing the $N_m$ coordinates such that $N = N_m/J$, where $J = 1, 2, \ldots, N_m-1$. The integer $J$ is a jump index. For example, $J = 1$ will give $N = N_m$. In this case, every sample in the pattern will be used for the signal generation. When $J = 2$, every other sample in the pattern sequence will be used. This will give $N = N_m/2$. Since the waveform distortion of the generated voltage signals is a function of $N$, the pointer
control process can be used not only to vary the frequency, but also to control the distortion of the waveforms dynamically. In the case when the clock frequency $f_{CK}$ is varied to control the output frequency $f_{a}$, this pointer control process can be used to change the frequency range of the output frequencies by varying $J$ dynamically.

During the signal generation process, the pointer scanning process should update the sample index $k$ such that:

1. the value of $N$ remains fixed as specified,
2. the phase sequence of the two-phase signals correctly corresponds to the sign of the slip according to the excitation requirements of the DESG, and
3. continuous signal waveforms are generated, i.e. no discontinuities.

Conditions (1) and (2) of the pointer scanning process can be achieved if the sample index $k$ is updated at every clock tick to:

$$k \leftarrow k + \text{sign}[s_{j}] \cdot J$$

(3.10)

In order to realize continuous signal waveforms (condition (3) of the pointer scanning process), the sample index $k$ should be reset to a new value when it reaches a value greater than $N_{M} - 1$ or less than zero. The pseudo code for resetting $k$ is:

$$k \leftarrow k - \text{sign}[s_{j}] \cdot N_{M}$$

(3.11)

The pseudo codes (3.10) and (3.11) describe the pointer scanning process as a complex, clocked, resettable, software-based digital oscillator [52, 53], as illustrated in
In this figure, the software-based switch will be simply a boolean logic that compares the value of the index \( k \) with that of \( N_m \) and selects the appropriate bias addend for the oscillator. The output of the oscillator is the updated index \( k \).

Figure 3.5: The block diagram of the software-based digital oscillator for controlling the pointer which scans the pattern lookup table.

Several ways can be used to control the pointer activity of scanning and fetching the pattern coordinates for a specified jump index, \( J \). The following four examples of pseudo codes for updating the sample index \( k \) on successive clock ticks will dynamically vary the number of samples per cycle, \( N \), and the direction in which the pointer scans the pattern lookup table depending on the slip sign.

\[
k \leftarrow k + \text{sign}[s_r].\text{INT}(N_m/N) \quad (3.12)
\]

\[
k \leftarrow k + \text{sign}[s_r].N_m2^R \quad (3.13)
\]

\[
k \leftarrow k + \text{sign}[s_r].\text{JMP}[x] \quad (3.14)
\]

\[
k \leftarrow k + \text{sign}[s_r].F(z) \quad (3.15)
\]
where $R$ is a positive integer less than or equal to $\log_2 N_M$, $x$ is a sample index for another lookup table containing predetermined choices for $N$ denoted as $JMP[x]$, and $F(z)$ is a polynomial function of an integer variable $z$. All these pseudo codes use the sign of the slip, $\text{sign}[s]$, to select the direction of scanning, i.e., incrementing $k$ for $\text{sign}[s] = +1$, decrementing $k$ for $\text{sign}[s] = -1$, and keeping $k$ a constant for $\text{sign}[s] = 0$. Effectively, this is equivalent to controlling the phase sequence of the excitation voltages. It should be noted that the condition $\text{sign}[s] = 0$, which corresponds to $f_s = 0$, is a valid programmable condition.

Given the values of $N_M$ and $N$, the pseudo code (3.12) will approximate a frequency range by using the integer ($\text{INT}$) function. In the case of $N_M$ being a power of 2, the pseudo code (3.13) will switch the frequency ranges using jumps which are also powers of 2 indexed by $-R$. In addition, it may be convenient all along to specify and select (in off-line) the values of $N$ for desired frequency ranges. These choices of $N$ can be stored also as a lookup table, e.g. $JMP[x]$. The software pointer only needs to use an index, such as $x$, to locate and fetch the specified value of $N$ from the lookup table as in the case of the pseudo code (3.14). Further, the jump index $J$ can be defined as an integer function $F(z)$ as in the pseudo code (3.15). For example, $F(z) = J + \text{adjust} \cdot z$ will increment ($\text{adjust} = +1$) or decrement ($\text{adjust} = -1$) $J$ in steps specified by $z$. For $\text{adjust} = 0$, the value of $J$ will remain unchanged. Such a function is suitable for on-line adjustment of $N$ manually from the keyboard of the computer.

The control of both the phase sequence and $N$ can be accomplished at any of the $N_M$ points. This flexibility is a powerful and desirable feature of this point-based data processing approach. Such a flexibility is not possible with the buffer-based data processing approach. The reason is that, in the buffer-based data processing approach, the pattern data are accessible only in units of buffers. However, with this point-based data processing scheme, there is a possibility of the two excitation windings carrying direct current with unequal excitation power. The worst case will occur when one of the excitation winding is contributing all the required excitation and the other winding is carrying no current at all. Therefore, there may be a need to specify off-line or dynamically the loading ratio of the excitation windings.
when the DESG is operating at or near its synchronous speed. This need is not a serious constraint in the case where both the excitation windings of the DESG are capable of carrying the full load excitation currents.

3.3 Real-Time Constraints

It has been discussed earlier that the variation of the clock rate $f_{ck}$ and/or the variation of the number of samples per cycle, $N$, are dynamic control options for synthesizing the variable-frequency of the excitation voltage signals. However, it is typical for any real-time clock or timer to have a fixed number of combinations of the clock frequency, $f_c$, and the values of the counter preset dividers $D_i$. These finite combinations allow only a subset of possible frequencies $f_{ck}$ and, thus, $f_{ca}$.

On the other hand, the value of $N$ is limited by the number of quantization levels of the DACs used in the signal generation which is equal to $2^b$ where $b$ is the bit-size of the DACs used. For this signal generation application, one value of $N$ and one range of dividers $D_i$ are not adequate to provide control flexibility [57]. Therefore, different combinations of $N$ and $D_i$ are required. There are four limitations in selecting the counter presets ($D_i$) as per Eqns. (3.7) and (3.9), and in selecting the values of $N$ as per Eqn (3.8). These limitations are:

1. Low sensitivity of the counter divider range to variation in $f_{ck}$. This applies to the counters used to synthesize $f_{ck}$,

2. The problem of generating very low frequencies, $f_{ca}$, when the DESG is operating near zero slip,

3. The limited range of the values of $N$, and

4. The limited speed of the execution of the DAC software driver (DRIVER A in Fig. 3.1).

These four limitations and ways to overcome them are discussed in the following sections.
3.3.1 Low Sensitivity of Counter Dividers to Clock Frequency

Equation (3.8) uses the integerization process (\(\text{INT}\)) by truncation. The curve \(D \text{ vs } f_{\text{ck}}\) for a specified input frequency to a counter stage is a hyperbola which changes from a curve with smaller steps for small values of \(f_{\text{ck}}\) to a curve with larger steps for high values of \(f_{\text{ck}}\). This problem arises from the fact that, for small values of \(f_{\text{ck}}\), the values of \(D\) are practically distinct and the sensitivity is high, while for high values of \(f_{\text{ck}}\), sub-ranges of \(f_{\text{ck}}\) will give the same value of \(D\). This gives steps on the \(D \text{ vs } f_{\text{ck}}\) hyperbola. This provides a poor sensitivity for dynamic control.

This problem can be illustrated by an example. Suppose that the DAC driver (DRIVER A in Fig.3.1) is to be driven at clock rates in the range \(50 \text{ Hz} \leq f_{\text{ck}} \leq 600 \text{ Hz}\). Let these rates be synthesized by loading appropriate dividers, i.e. \(D = \text{INT}(f_c / f_{\text{ck}})\), into a one-stage (counter) timer. The corresponding \(D \text{ vs } f_{\text{ck}}\) curves for \(N = 64, 128,\) and 256 samples per cycle are shown in Figs. 3.6 to 3.9 for input clock rates, \(f_c\), of 100 kHz, 500 kHz, 1.0 MHz, and 10.0 MHz, respectively. These figures show that, to have a high sensitivity and to avoid the more stepped parts of the hyperbola, there must be an ability to change both the values of \(N\) and the input clock rate dynamically. Otherwise, it is necessary to use extremely high clock rates (> 1.0 MHz) to guarantee a high sensitivity. Clocks of such high rates may not be available. Also, it may become necessary to use small values of \(N\) to synthesize \(f_{\text{ck}}\). This is not desirable since low values of \(N\) correspond to high waveform distortion.

3.3.2 Generation of Very Low Excitation Frequencies for Operation Near Zero Slip

The values of \(s_r\) near or equal to zero require approximately zero sampling frequencies if the option of varying \(f_{\text{ck}}\) (to vary \(f_{\text{sa}}\)) is used. Such low sampling rates are a problem because the DAC software driver, at such low rates, will be slow in reacting to changes in the slip-sign and, thus, the phase-sequence control will be slowed down.
Figure 3.6: Variation of the counter divider \( (D) \) with clock rate, \( f_{CK} \), for a counter input frequency \( f_c = 100 \text{ kHz} \).
Master Clock = 500 kHz

\[ D = \frac{f_c}{f_{ck}} \]

\[ D = \text{INT}\left(\frac{f_c}{f_{ck}}\right) \]

Figure 3.7: Variation of the counter divider \((D)\) with clock rate, \(f_{ck}\), for a counter input frequency \(f_c = 500 \text{kHz}\).
Figure 3.8: Variation of the counter divider ($D$) with clock rate, $f_{ck}$, for a counter input frequency $f_c = 1.0$ MHz.
Master Clock = 10.0 MHz

\[ D = \frac{f_c}{f_{ck}} \]
\[ D = \text{INT}(\frac{f_c}{f_{ck}}) \]

**NOTE:** In this figure, the solid-line curve and the dashed-dotted line curve for each case of \( N \) coincide. This coincidence depends on the graph scale.

**Figure 3.9:** Variation of the counter divider \( (D) \) with clock rate, \( f_{ck} \), for a counter input frequency \( f_c = 10 \text{ MHz} \).
The best way to generate low frequencies, \( f_{da} \), is to increase \( N \). In addition, zero sampling rate could be accomplished by virtually stopping the sampling process, e.g. by setting \( \text{sign}(s_a) = 0 \), when a specified \( \text{dc-zone} \) is reached. This \( \text{dc-zone} \) is a range of slip frequencies, \( 0 \leq f_{da} < f_{dcz} \), for which it can be assumed that the rotor slip is equal to zero. The excitation power will be a minimum within this \( \text{dc-zone} \). This concept of the \( \text{dc-zone} \) corresponds to the idea of a deadband in frequency regulation schemes for constant-speed constant-frequency (CSCF) generating schemes [14]. In this case, the frequency regulation curve is defined by:

\[
\begin{align*}
    f_{da} &= f_s; \quad f_{dcz} < f_s \leq f_{sM} \\
    f_{da} &= 0; \quad 0 \leq f_s < f_{dcz}
\end{align*}
\]  

(3.16)

where \( f_{sM} \) is the maximum slip frequency allowed for the operation of the DESG. This \( f_{sM} \) corresponds to the frequency regulation setting in conventional CSCF systems.

If \( (f_{CD})_{min} \) is the minimum rate at which the DAC driver should operate, and the specified maximum value of \( N \) is \( N_{M} \), then the possible minimum value of \( f_{dcz} \) will be:

\[
f_{dcz} = \frac{(f_{CD})_{min}}{N_{M}}
\]

(3.17)

For example, if \( (f_{CD})_{min} = 50 \text{ Hz} \) and \( N_{M} = 4096 \), then, \( f_{dcz} = 0.0122 \text{ Hz} \). This corresponds to a slip range of \( \pm 0.02\% \) for \( f_0 = 60 \text{ Hz} \).

There is an objection to this idea of a \( \text{dc-zone} \), since this \( \text{dc-zone} \) requires the DESG be operated with a d.c. excitation. There is thus no frequency correction in this case \((s_r = 0 \text{ for the FR})\). As a result, a DESG synchronized to a power system may fall out of synchronism. This is not desirable. Practically, operation in a \( \text{dc-zone} \) can be avoided by operating the DESG at higher slips. However, the value of \( f_{dcz} = 0.0122 \text{ Hz} \), of the example
discussed above is about ten times smaller than what is considered normal in conventional systems. Normal deadband settings in CSCF systems are about \( \pm 3 \text{ rpm} \) (fossil) and \( \pm 2 \text{ rpm} \) (nuclear) [14]. For the case of \( f_0 = 60 \text{ Hz} \) and \( p = 2 \), these values translate to \( f_{ac} = 0.1 \text{ Hz} \) and \( 0.07 \text{ Hz} \), respectively. Thus, this dc-zone problem is not a serious issue. Since, the excitation control is programmable, the value of \( f_{ac} \) can be adjusted on demand. The only foreseeable limitation to adjusting this zone is the finite resolution of the shaft encoder used to measure the speed of the generator.

3.3.3 The Maximum Number of Samples per Cycle

The maximum number of the equal-spaced samples per cycle, \( N_M \), of the sinusoidal patterns used in the signal generation process is a function of the bit-size \((b-bits)\) of the DACs used. In this application, quarter-cycles are used as building blocks of the sinusoidal waveforms to maximize the value of \( N_M \). A quarter of a cycle \((\pi/2 \text{ radians})\) is the smallest detailed part of a cycle of a sinusoidal wave from which the full cycle of a sinusoidal wave could be reconstructed [53]. If \( N_Q \) is the maximum number of samples per quarter cycle, then, the maximum number of samples per cycle will be four times as much, i.e. \( N_M = 4N_Q \). The value of \( N_Q \) is \( 2^b \) for \( b\)-bits DACs. Thus, the size of the lookup table in memory (for a complete cycle) per each pattern need to be no longer than \( N_M = 4(2^b) = 2^{b+2} \). For \( b = 12\)-bits, \( N_M = 16384 \) samples per cycle. In addition, this \textit{bit} size of the DACs determines the quantization noise of the signal generation (sampling) process. The signal-to-noise ratio at the output of the converter is given by \( 20\log_{10}(2^b) \) decibels.

On the other hand, at run time, the waveform pattern values have to be loaded into the dynamic program memory of the computer, RAM (Random Access Memory), which is accessed by the microcomputer. Some microcomputer hardware architecture may restrict the size of the lookup tables, especially if single-chip microcomputers (microprocessors) are used [52 - 54]. The reason for this is that such microcomputers generally have limited memory pointers. Thus, the value of \( N_M \) may be limited by the available memory for loading
the waveform pattern lookup table during run time. However, the RAM problem is not a serious limitation if personal computers are used. Such microcomputers have much larger memory pointers. For example, the 8086-, 80286-, 80386- and 80486-MPU-based PCs have motherboards with expandable RAM. This expansion depends on the addressing capability of the computer system, e.g. RAM can be expanded to 1.0 Megabytes (1.0 Mb) for the 8086-based PCs and up to 4 Gigabytes (4 Gb) for the 80486-based PCs [69].

Since the value of $N_M$ is limited to some finite value, there is a problem of sensitivity in the use of Eqn. (3.8) for synthesizing $f_{in}$ by varying $N$. Also, there is the problem of waveform distortion control. In general, the waveform distortion will increase with increasing excitation frequency, $f_{in}$, because fewer pattern samples are used per wave signal at higher frequencies. Figures 3.10 and 3.11 show the variation of $N$ vs $f_{in}$ for a DAC-software driver rate of 500 Hz. From these figures, it is clear that Eqn. (3.8) has a good sensitivity for synthesizing frequencies $f_{in}$ $\leq 5$Hz. Using $f_{CK} = 500$ Hz and $N_M = 16384$ in a 60 Hz system, the minimum value of $f_{in}$ is $\approx 0.03$ Hz. This gives a slip range of $\pm 0.05\%$ for the dc-zone. This dc-zone can be reduced by reducing $f_{CK}$. For example, selecting $f_{CK} = 50$ Hz gives a minimum value of $f_{in} \approx 0.003$ Hz, which gives a slip range of $\pm 0.005\%$ for the dc-zone.

3.3.4 Execution Speed of the Signal Generator (DAC) Software Driver

The DAC software driver, DRIVER A in Fig. 3.1, is a real-time application program. Real-time means that the time it takes the program to fetch and process the waveform pattern data, to monitor all external signals, and to drive (write to) the DACs for every clock period ($T_{CK}$) must be negligible when compared to the period of the maximum clock frequency, ($f_{CK}$)$_M$, the driver can track. Thus, the ultimate sophistication of the DACs driver, i.e. how many tasks to be performed per clock period, is limited by how long it takes to execute the program. In fact, this speed of execution of the driver determines the maximum clock frequency ($f_{CK}$)$_M$ in the frequency synthesis process (Eqn. (3.7)). It is therefore important that the program be carefully structured and written to minimize execution time. Three ways can be used to increase this execution speed.
Figure 3.10: Variation of the number of samples per cycle \( N \) with the desired output frequency \( f_{da} \) for a constant clock rate of \( f_{CK} = 500 \) Hz. The range of \( f_{da} \) in this case is 0 - 1.0 Hz.
Figure 3.11: Variation of the number of samples per cycle ($N$) with the desired output frequency ($f_{da}$) for a constant clock rate of $f_{CK} = 500$ Hz. The range of $f_{da}$ in this case is $0 - 20$ Hz.
Firstly, the execution speed depends on the type of the program compiler and the computing hardware used. Compilers that can optimize program code for speed, e.g. C, C++ compilers, are most suitable for developing the DAC driver. Secondly, the use of fast hardware computing processors, e.g. Maths Co-processors, can also greatly increase the speed of the execution of the DAC driver. The third way to increase the execution speed is to reduce the background computational load in the driver and only perform tasks directly relevant to the signal generation. This third approach has been extensively used in this work by distributing tasks to three computers (three PCs), i.e. the use of a distributed computing hardware. For example, the variation of the clock rate $f_{ck}$ from CLOCK A can be performed by an independent driver, e.g. DRIVER C in Fig. 3.1, implemented in a separate computer.

3.4 Modified Dynamic Control of the Lookup Table Scanning Process Based on the Quarter-Cycle Patterns

The procedure described in section 3.2.3 for scanning the pattern lookup table is only applicable for the case that all $N_M$ samples of complete cycles of the cosine and sine waves are stored in memory. In the case when only quarter cycles are used, i.e. $N_Q$ samples per wave are stored, a different procedure is required for scanning the lookup tables to achieve smooth joining of the quadrants at the boundaries and to eliminate discontinuities.

The modified procedure requires quadrant information (be stored in memory or determined in real time) for reconstructing the full cycles of each wave from the pattern table of quarter-cycles stored in memory. In this research work, the real-time approach is used to determine the quadrant information for the scanning process. Two sample indices, $nn$ and $k$ are used. The index $nn$ is used to point at virtual samples in the range 0 to $N_M - 1$ such that:

$$nn \leftarrow nn + \text{sign}[s]. J$$

(3.18)
where \( nn \) is incremented or decremented after every clock tick depending on the value of \( \text{sign}[s] \), and \( J \) is the jump index. If codes \( \text{Quad} = 0,1,2, \) and \( 3 \) are used to denote the \( 1^{\text{st}} \), \( 2^{\text{nd}} \), \( 3^{\text{rd}} \), and the \( 4^{\text{th}} \) quadrants, \( \text{Quad} \) can then be determined from the index \( nn \) in real-time from:

\[
\text{Quad} = \text{INT}( nn / N_Q )
\]  

(3.19)

The sample index \( k = (0, 1, 2, \ldots, N_Q - 1) \) is then used to point at the actual samples stored in the lookup tables. The pseudo code for updating \( k \) in terms of \( nn \) and \( \text{Quad} \) is:

\[
k < \quad nn - \text{Quad} \cdot N_Q
\]  

(3.20)

The full waves of each signal can be reconstructed from the quarter-cycle patterns by performing simple arithmetic operations on the pattern data before they are converted into analog values. Denoting \((v_{\text{da}}, v_{\text{qa}})\) as the processed samples corresponding to the pair \((v_{\text{d}}[k], v_{\text{q}}[k])\) indexed by \( k \), the operations are as shown in Fig. 3.12. This figure also shows the corresponding processed pattern values of the pointer index \( k \) (marked by *) for the case when 12-bit DACs are used in the signal generation process.

The modified scanning process also requires a reset pseudo code when the value of \( nn \) is less than zero or is greater than \( N_M - 1 \) in order to guarantee continuous waveforms in real time. The reset pseudo code is:

\[
nn < \quad nn - \text{sign}[s] \cdot N_M
\]  

(3.21)
<table>
<thead>
<tr>
<th>Quad</th>
<th>Sample Pointer (k)</th>
<th>Data to be Used</th>
<th>Range of Index nn</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>k ← nn</td>
<td>(v_{dn} = v_d[k]) (v_{qn} = v_q[k])</td>
<td>([0, N_Q - 1])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>([0, 4095])*</td>
</tr>
<tr>
<td>1</td>
<td>k ← nn - N_Q</td>
<td>(v_{dn} = -v_q[k]) (v_{qn} = v_d[k])</td>
<td>([N_Q, 2N_Q - 1])</td>
</tr>
<tr>
<td></td>
<td>k ← nn - 4096*</td>
<td>(v_{dn} = -v_q[k]) (v_{qn} = v_d[k])</td>
<td>([4096, 8191])*</td>
</tr>
<tr>
<td>2</td>
<td>k ← nn - 2N_Q</td>
<td>(v_{dn} = -v_q[k]) (v_{qn} = -v_q[k])</td>
<td>([2N_Q, 3N_Q - 1])</td>
</tr>
<tr>
<td></td>
<td>k ← nn - 8192*</td>
<td>(v_{dn} = -v_q[k]) (v_{qn} = -v_q[k])</td>
<td>([8192, 12287])*</td>
</tr>
<tr>
<td>3</td>
<td>k ← nn - 3N_Q</td>
<td>(v_{dn} = v_q[k]) (v_{qn} = -v_d[k])</td>
<td>([3N_Q, 4N_Q - 1])</td>
</tr>
<tr>
<td></td>
<td>k ← nn - 12288*</td>
<td>(v_{dn} = v_q[k]) (v_{qn} = -v_d[k])</td>
<td>([12288, 16383])*</td>
</tr>
</tbody>
</table>

* for 12-bit DACs

Figure 3.12: Quadrant information and pseudo codes for the pointer scanning process based on the quarter-cycle pattern.

3.5 Control of the Amplitude of the Excitation Voltages

The voltage regulation (VR) loop must adjust the amplitude of the excitation voltages \(v_d\) and \(v_q\) to maintain the terminal voltage of the variable speed DESG constant. This adjustment of the amplitude of \(v_d\) and \(v_q\) is a task of another clocked process identified as Driver B in Fig. 3.1. This driver generates a signal, \(U_{AM} = U_{AM}(t)\), which may be digital or analog, proportional to the term \(U_f(1- \varphi(e))\) in Eqn. (3.4). Then, this signal is multiplied by the outputs of Driver A such that \(U_{ff} = AU_{AM}\). The realization of the VR control scheme in terms of the operations of Driver A and B is as follows:

1. After every clock tick, Driver A fetches from the pattern lookup table a predetermined pair of reference data, \((v_d[k], v_q[k])\), processes them to obtain \((v_{dn}, v_{qn})\) according to the pointer scanning process described in Section 3.4.
2. Before these values of the reference cosine and sine functions are released for conversion to analog values or while in the process of being converted to analog values, the values are processed such that:

\[
\begin{align*}
U_{AMa} & \leftarrow U_i (1 - \varphi(e_a)) \quad (3.22) \\
v_{\text{sls}} & \leftarrow U_{AMa} * v_{\text{u}} \quad (3.23) \\
v_{\text{qs}} & \leftarrow U_{AMa} * v_{\text{q}} \quad (3.24)
\end{align*}
\]

where \(U_{AMa}\) is the amplitude update, \(e_a\) is the processed sample of the terminal voltage error signal, \(e(t)\), corresponding to the \(n\)th clock tick, and \(\varphi\) is a control function. It can be observed that Eqns. (3.22) to (3.24) describe a negative-amplitude modulation scheme which uses the errors \(e_a\) derived from the terminal voltage error signal as the modulating signal. Such a scheme, in real time, can keep the magnitude of the generator terminal voltage constant. The phrase *keep the magnitude of the terminal voltage constant* is a performance objective for the VR scheme. This objective, once specified, e.g. as a steady-state error, can be achieved by the use of a suitable control function, \(\varphi\).

The control function \(\varphi\) is either a compensator or a digital filter. A class of conventional control functions which can be used include the P, PI, PD, and PID controllers [70 - 74]. However, the use of computer-based control greatly increases the class of control laws that can be used. For example, it is easy to use nonlinear calculations, to incorporate logic and to perform substantial calculations (iteratively or otherwise) in the controller. Further, lookup tables can be used to store data in order to accumulate knowledge about the properties of the system as it is the case in self-tuning or adaptive controllers [70].
In general, the design of a suitable digital control function, such as $\varphi$, will depend on several aspects of the control system on which the function is to apply. These aspects include:

1. **Sensors, sensor interfaces and computational delays** - These give rise to additional dynamics (delays) into the system.

2. **Numerics** - e.g. the accuracy of the ADCs and DACs used, and the precision of computation chosen must be considered in the controller design.

3. **Actuators** - These also introduce extra dynamics and may also introduce nonlinear dynamics into the system.

4. **Operational aspects** - e.g. switching from MANUAL to AUTOMATIC control.

5. **Programming aspects** - e.g. code optimization for speed, available computing power and the timing of the real-time tasks.

6. **Knowledge about the system or plant to be controlled** - in this case the DESG. To acquire the necessary knowledge about the system requires system modelling and identification.

Effects due to these aspects of real-time control should be considered and accounted for in the controller design. Altogether, these aspects show that the selection of transfer functions of the blocks of the excitation system (Fig. 2.5) discussed in Chapter 2 is a complex issue. In fact, the controller design problem requires an independent study of its own and, thus, is beyond the scope of this thesis. However, the proposed VR scheme has a software-based provision for implementing a desirable control function, $\varphi$. Figure 2.5 shows the blocks that form the structure of the VR scheme. This structure has been used to test the VR scheme. Of course, the proposed structure can be changed or modified as may be deemed necessary. After all, the structure is software-based and hence flexible.
3.6 Summary

This chapter has described the development of a real-time algorithm for controlling the excitation of a variable speed dual-excited synchronous generator (DESG) operating as a VSCF generating system. The algorithm has a frequency synthesis scheme (which is also a waveform distortion control scheme), frequency and amplitude modulation schemes, and a phase-sequence control scheme, all designed to run concurrently in real time. The algorithm employs a dedicated, clocked, D/A conversion process to generate the two-phase excitation voltages that meet the excitation requirements of a variable speed DESG. The frequency synthesis and the frequency modulation schemes of the excitation algorithm are used to realize the frequency regulation (FR) scheme for the DESG. The amplitude modulation scheme is used to realize the voltage regulation (VR) scheme for the DESG. These two regulation schemes are designed to control the excitation voltages simultaneously while acting independently. Such a concurrent control by the FR and the VR schemes will enable the variable speed DESG to supply electrical power at constant frequency and constant terminal voltage.
4. EXCITATION SYSTEM SIGNAL INSTRUMENTATION

4.1 Introduction

The various variables of the dual-excited synchronous generator (DESG) in a variable speed generating system must be synchronously monitored continuously and simultaneously. In the frequency regulation (FR) loop, the speed of the generator rotor, \( n_r \), and the desired (system) frequency, \( f_0 \), must be monitored continuously. From these two measured signals, the slip frequency, \( f_s \), and the slip sign, \( \text{sign}[s] \), could be obtained for feed forward control from \( f_s = |f_0 - f_r| \) and \( \text{sign}[s] = \text{sign}[f_0 - f_r] \). The voltage regulation (VR) loop requires the terminal voltage error, \( e(t) \), to be available continuously. In turn, the generation of \( e(t) (= V_{\text{REF}} - V_t) \) in real time requires the measurement of the magnitude of the terminal voltage of the generator, \( V_t \), continuously (Fig. 2.3). In addition, it was decided that the excitation system should generate analog signals proportional to \( n_r \), \( \text{sign}[s]f_s \), the frequency of the generator terminal voltage, \( f_{\text{out}} \), and the magnitude of the terminal voltage, \( V_t \). These analog signals have been identified and found useful for monitoring the performance of the excitation system. This chapter describes the instrumentation employed to perform these measurements in a microcomputer environment.

4.2 Terminal Voltage Transducer and the Voltage Error Formulation [75]

Figure 4.1 shows the arrangement used to derive the terminal voltage feedback for the VR loop. The important component of this arrangement is the RMS-to-DC AD536AJ device. This device, an RMS-to-DC converter, is a complete monolithic integrated circuit which performs true rms-to-dc conversion (rms stands for root mean square value) [46]. The
converter will accept both d.c. and a.c. input voltage signals. This device performs an averaging operation to generate a d.c. voltage signal proportional to the rms-value of the input voltage signal. In Fig. 4.1, the terminal voltage of the DESG is attenuated by a factor of 100 before it is fed to the RMS-to-DC converter. Figure 4.2 shows the isolation and attenuator circuit employed to interface the RMS-to-DC converter to the generator terminals.

![Block diagram of the VR control loop](image)

**Figure 4.1:** (a) Part of the block diagram of the VR control loop showing the components that make up the terminal voltage transducer. (b) Equivalent transfer function of (a).

The rms-to-dc transducer requires an external capacitor to set the averaging time constant. In addition, a low-pass prefilter (LPF in Fig. 4.1) with a cut-off frequency of 60 Hz is used to limit the effect of noise and unwanted high frequency harmonics (> 60 Hz) to the rms-to-dc conversion process. Due to the added averaging capacitor and
the LPF block, the arrangement of Fig. 4.1 has unavoidable delays. The transfer function
of the prefilter plus the RMS-to-DC converter arrangement has been determined
experimentally to be of the form:

\[ G_{4v}(s) = \frac{K_{4v}}{[(1 + s\tau_{4v1})(1 + s\tau_{4v2})]} \]  \hspace{1cm} (4.1)

where \( K_{4v} = 0.01 \), \( \tau_{4v1} = 0.0067 \text{ sec.} \) and \( \tau_{4v2} = 0.06 \text{ sec.} \). These values depend on the
selected components of the isolation stage, the prefilter and the averaging capacitor of the
RMS-to-DC converter.

\[ \text{Figure 4.2: The circuit diagram of the differential amplifier stage used as an} \]
\[ \text{isolation and attenuator unit for metering the terminal voltage of} \]
\[ \text{the DESG. \{Specification for the 1 MΩ resistors: 5%, 1kV, 3W \}.} \]
The d.c. output from the RMS-to-DC converter is then sampled by an analog-to-digital converter (ADC) into the computer, as illustrated in Fig. 4.3. The voltage samples from the ADC are passed (processed) through another low-pass filter of the form:

\[ G_{sv}(s) = \frac{K_{sv}}{1 + s\tau_{sv}} \]  \hspace{2cm} (4.2)

The parameters of this filter can be varied or adjusted on-line. The gain \( K_{sv} \) is a software-based multiplier which provides a means for adjusting the error formulation, in Fig. 4.3, such that \( V_{REF} = V_t \) (\( e(t) = 0 \)) before closing the VR loop (i.e. engaging the automatic mode). The value of this gain \( K_{sv} \) will vary with the desired \( V_{REF} \) and the on-line adjustment of the gain is such that:

\[ K_{sv} \leftarrow \frac{V_{REF}}{V_t} \]  \hspace{2cm} (4.3)

![Figure 4.3: Part of the block diagram of the VR loop showing the details of the software-based error formulator for deriving the terminal voltage error signal, \( e(t) \).]
In essence, the programmable gain $K_{sv}$ allows for the VR loop to optimize the scaling of the generator terminal voltage so that this voltage can be compared with the reference voltage (software-based) for generating the error signal, $e(t)$. Additional processing of the error signal by the computer is discussed in Chapter 5.

4.3 Speed and Frequency Measurements

For the proper operation of the proposed excitation system, four frequency signals must be metered continuously and simultaneously in a synchronized multi-process sampling scheme. These four signals are the rotor speed, $n_r$ (or $f_r$), the reference frequency (or the system frequency) $f_0$, the slip frequency, $f_s$, and the frequency of the terminal voltage of the DESG, $f_{out}$. The slip frequency is calculated from $f_0$ and $f_r$ as $f_s = |f_0 - f_r|$. In the case that the generator is supplying power to a constant-frequency power system, the DESG will be synchronized to the system and, thus, $f_{out} = f_0$. In such a case, there will be no need to monitor $f_{out}$ and $f_0$ separately. On the other hand, if the DESG is operating in the island mode (i.e. not synchronized to a constant-frequency power system), there must be an accurate means of specifying the desired output frequency $f_0$. In a microcomputer environment, this reference frequency may be either specified as a theoretical number or generated (internally) using programmable counters.

In the case that the DESG is isolated, the range of $f_0$ has been chosen to be between 40 Hz and 70 Hz. Once $f_0$ is chosen, it remains fixed until changed manually (on-line). In the second case, when the DESG is connected to a grid, the reference frequency will always have a known nominal value, e.g. 50 Hz or 60 Hz. For both cases, the deviation of $f_0$ from the specified value should be negligible. These deviations of $f_0$ should be measured continuously in real time.

Also, it has been established that data acquisition rates between 20 Hz and 35 Hz are sufficient to track the dynamics of the DESG. These dynamics have been investigated and found to be not faster than 2 Hz. Thus, such low sample rates can be derived from the
reference frequency $f_0$ by dividing it by two. A shaft encoder, mounted on the rotor of the DESG, is used as a speed transducer. The output of the shaft encoder provides asynchronous electric pulses whose frequency is proportional to the rotational speed $n_r$, (and hence $f_r$). The speed signal is obtained by computer processing of these encoder pulses. With these pulses available, the problem of speed measurement also becomes a frequency measurement problem.

### 4.3.1 Selection of the Method of Frequency and Speed Evaluation

The following requirements were considered in the selection of the method for metering the frequencies $f_0$, $f_{out}$, $f_s$, and the speed $n_r$.

1. Both the frequency and the speed evaluation schemes should be implementable and programmable in a microcomputer-based multi-process environment.

2. Both the frequency and the speed metering (or sampling) operations should be amenable to being synchronized to other metering operations within the excitation system.

3. Since the excitation system is a real-time multi-process system, the speed and frequency evaluation schemes used should be real-time processes and must not be computational intensive. The range of the response time of the frequency and speed metering schemes should be less than 60 ms so that they can work with the low sample rates between 20 Hz and 35 Hz.

4. The frequency metering schemes should be able to measure accurately frequencies at least between 30 Hz and 80 Hz. This range covers the range of the output frequency, $f_{out}$, particularly when the FR scheme is operating in the MANUAL mode.

5. The digital speed metering scheme should be able to measure accurately speeds within $\pm 30\%$ deviation from the specified nominal operating speed, $n_0$, of the
DESG. For a 60-Hz, 4-pole DESG, the corresponding speed range will be \( 1260 \leq n_r \leq 2340 \text{ rpm} \), where the nominal speed \( n_0 \) is equal to 1800 rpm. However, the actual operating speed range may be limited to either the subsynchronous range \( (n_r < n_0) \) or the supersynchronous range \( (n_r > n_0) \).

Different methods for designing speed and frequency measurement systems were considered for implementation in the excitation system. The first group of these methods consists of those schemes that use data acquired from waveform sampling [77 - 80]. These methods use high sample rates of up to 10 kHz and require relatively extensive processing to obtain the frequency updates. Thus, such schemes are not appropriate for implementation in the excitation system. The other group of methods considered are those that are counter-based (i.e. based on processes that count pulses) [81 - 88]. These methods differ mainly in the approach for timing the measurement processes and in the method of speed or frequency evaluation. Of these methods, the constant elapsed time (CET) method for designing digital tachometers [81, 84, 86] has been studied and found capable of meeting the above five requirements of the excitation system. In general, this CET method requires a short measurement time which varies little throughout the speed range. In addition, the CET method provides an optimal compromise between resolution and measurement time (response time) [84]. With this CET method, it is possible to measure both speed and frequency simultaneously.

4.3.2 Programmable Constant Elapsed Time Method

The constant elapsed time (CET) method involves the counting of shaft encoder pulses and a time measurement simultaneously and continuously. The encoder pulses are counted for a specified time interval, \( \Delta t = T_m \), to obtain an incremental rotational angle, \( \Delta \phi = \phi_m \). The time \( T_m \) gives the period of the measurement cycle and \( f_m = 1/T_m \) gives the sample rate. In a separate counting process, the time interval \( \Delta t = T_m \) is measured by counting cycles of a high frequency clock, \( f_c \), over this period of time. An update of the rotational speed, \( n_r \), is then calculated from the quotient [81, 84]:

\[ n_r = \frac{f_m}{T_m} \]
The CET method is made programmable by providing a software-based way to specify both $T_m$, which is the CET, and the frequency $f_C$ for the time measurement. Such a provision makes the CET independent of the speed to be measured. If an integer $C_p$ is the count of the encoder pulses accumulated in time $T_m$ and $C_t$ is the count representing $T_m$, then, the rotational speed $n_r$ in rev/sec. can be calculated from Eqn. (4.4) as:

$$
n_r = \frac{\Delta \phi}{\Delta t} = \frac{\phi_m}{T_m} \tag{4.4}
$$

$$
n_r = \frac{(f_C \cdot C_p)}{(\mu C_t)} \tag{4.5}
$$

where $\mu$ is the number of encoder pulses per revolution of the shaft. It can be reasoned out from Eqn. (4.4) that the relative error of the speed measurement scheme is determined by the error in the measurement of the increment of the rotational angle $\phi_m$, the error in measuring $T_m$, and the calculation error. These errors are denoted as $\varepsilon_{\phi m}$, $\varepsilon_{Ct}$, and $\varepsilon_{Ca}$, respectively.

The calculation error, $\varepsilon_{Ca}$, depends on the computing platform used to evaluate Eqn. (4.4) expressed as in Eqn. (4.5). Microcomputer platforms are so advanced that they can offer up to 64-bit floating point arithmetic. Thus, the calculation error, $\varepsilon_{Ca}$, can be considered negligible.

The maximum relative error $\varepsilon_{Ca}$ for the $T_m$, based on one missing count ($\Delta C_t = 1$), is given by $|f_m/f_C|$. This error can be specified and fixed by specifying appropriate values of $f_m$ and $f_C$. For example, if $f_m = 60$ Hz, and $f_C = 2.5$ MHz, then, $\varepsilon_{Ca} = 0.0024 \%$.

The maximum relative error in $\phi_m$, i.e. $\varepsilon_{\phi m}$, is a sum of the error due to the non-equispaced encoder pulses, denoted as $\varepsilon_{ep}$, and the error in accumulating the count $C_p$ of the encoder pulses, denoted as $\varepsilon_{Cp}$. The value of $\varepsilon_{ep}$ is usually specified by the encoder...
manufacturer and is small of the order of 0.01%. The value of $\varepsilon_{cp}$ (based on $\Delta C_p = 1$) increases with the decrease in speed according to:

$$\varepsilon_{cp} = 1/C_p = 1/\mu n_T T_m$$

(4.6)

As a result, the measurement of $\phi_m$ becomes less accurate at low speeds. The accuracy can be improved by using a high resolution encoder, i.e. a high value of $\mu$, and/or a longer CET period ($T_m$). This error $\varepsilon_{cp}$ can be eliminated by using a fixed integer value of $C_p$. This requires a continuous adjustment of the CET ($T_m$) such that $C_p$ is always constant. This is the case when an integer number of encoder pulses is used to specify the CET asynchronously [81, 84]. However, such a control gives a variable sample rate and, thus, this control is not easy to synchronize with other sampling operations. For speeds in the range $1260 \leq n_r \leq 2340$ rpm, sample rates $(1/T_m)$ in the range between 25 Hz and 35 Hz, and $\mu = 360 ppr$, the error $\varepsilon_{cp}$ will vary from a minimum of 0.14% (at 2340 rpm, sample rate of 25 Hz) to 0.46% (at 1260 rpm, sample rate of 35 Hz). Correspondingly, $\varepsilon_{\phi_m} = \varepsilon_{cp} + \varepsilon_{cr}$ will be less than 0.5%. This accuracy of the speed measurement scheme using a fixed value of CET ($T_m$) was considered adequate. The accuracy can be improved by using a shaft encoder with higher resolution.

4.3.3 Speed Metering Counter Scheme

Figure 4.4 shows the configuration of the computer-based tachometer which utilizes programmable multi-counter timers. All the signals shown in this figure are digital signals, i.e. a HIGH signal level gives a LOGIC = 1 level and a LOW signal gives a LOGIC = 0 level. In this figure, counters #1 and #3 are used to count the encoder pulses and counters #2 and #4 are used to count the cycles of the high frequency, $f_r$. The gate signal $Q$ controls the counting processes in counters #1 and #2. The gate signal $Q^C$ (compliment of Q) controls the counting processes in counters #3 and #4. These two gate signals, Q and $Q^C$, are also
Figure 4.4: The block diagram of the counter scheme for implementing the programmable CET technique for computer-based frequency and speed metering.
fed to the computer as digital inputs IP1 and IP2. A HIGH (LOGIC = 1) digital input IP1 indicates that the counting processes in counters #1 and #2 are still in progress. A LOW (LOGIC = 0) input IP1 indicates that these two counters are ready to be latched for reading.

The timing of the counting processes in the counters is illustrated in Fig. 4.5. A similar set of events takes place to counters #3 and #4 when the digital input IP2 is HIGH and when it becomes LOW.

On detecting a LOW level of Q, counter #1 will register a count \( C_{pP} \) and counter #2 will register a count \( C_{pP} \). These two readings are updates that correspond to the positive half cycle of Q. The corresponding update of the rotational speed \( n_{rP} \) is obtained from Eqn. (4.5) as:

\[
 n_{rP} = \frac{(f_c \cdot C_{pP})}{(\mu \cdot C_{pP})} \quad (4.7)
\]

Similarly, on detecting a LOW level of \( Q^c \), there will be counts \( C_{pN} \) and \( C_{pN} \) registered by counters #3 and #4, respectively. These two readings correspond to the negative half cycle of Q (which corresponds to the positive half cycle of \( Q^c \)). The update of the rotational speed after the negative half period is thus:

\[
 n_{rN} = \frac{(f_c \cdot C_{pN})}{(\mu \cdot C_{pN})} \quad (4.8)
\]

The updates \( n_{rP} \) and \( n_{rN} \) are two consecutive updates within a cycle of the signal Q (frequency = \( f_m/2 \) or \( f_0/2 \)). Therefore, the arrangement of the counters #1 through #4 provide continuous updates of the rotational speed at a sample rate equal to \( f_m \) or \( f_0 \). Using only \( n_{rP} \) or \( n_{rN} \) as a speed update will give a sample rate equal to \( f_m/2 \) or \( f_0/2 \).
1. Read appropriate counters and initialize them for next cycle,
2. process the data,
3. perform some filtering, then
4. update speed and output results either to the screen, DAC or disk drive.

Figure 4.5: The timing diagram of the counters' operation of frequency and speed metering.
Counters #5 and #6 of Fig. 4.4 are for synthesizing the sample rate $f_m$ from another reference (Master) frequency $f_{m\text{ST}}$. The synthesis of $f_m$ is accomplished by loading into counters #5 and #6 appropriate dividers $D_{m1}$ and $D_{m2}$, respectively, such that:

\[
D_{m1} = \text{INT}(f_{m\text{ST}}/f_1) \quad (4.9)
\]
\[
D_{m2} = \text{INT}(f_1/f_m) \quad (4.10)
\]

where $\text{INT}$ denotes an integerization operation by truncation. Counter #7 is used to synthesize the frequency $f_c$. This is accomplished by loading into this counter an appropriate integer divider, $D_c$, such that:

\[
D_c = \text{INT}(f_{m\text{ST}}/f_c) \quad (4.11)
\]

The multiplexer circuit, identified as $MUX$ in Fig. 4.4, allows for the use of either $f_m$ or the power system line frequency $f_0$ as reference frequencies. These two can be chosen by using the digital output signals OP1 and OP2. This switching arrangement provides not only programmable CET but also a way to measure $f_0$.

In Fig. 4.4, the counts $C_{IP}$ and $C_{IN}$ are proportional to the time periods corresponding to the positive and negative half-cycles of the signal $Q$, whose frequency is $f_m/2$ (or $f_0/2$). These measurements give two consecutive updates of the full period corresponding to the frequency $f_m$ (or $f_0$). That is:

\[
f_{mP} = f_c/C_{IP} \quad (4.12)
\]
\[
f_{mN} = f_c/C_{IN} \quad (4.13)
\]
Equations (4.12) and (4.13) describe the measurement of the frequency by first measuring the period of a signal and then taking the reciprocal of the period to obtain the frequency [35]. The maximum relative error in this measurement can be shown to be 
\[ |\Delta f_m/f_m| = 1/C_t = f_m/f_C. \]
For \( f_C = 2.5 \text{ MHz} \), this maximum error is equal to 0.0024\% for tracking a steady 60 Hz, and the error is equal to 0.002\% for tracking a steady 50 Hz. A worst case deviation of ± 2 Hz from the 60 Hz or 50 Hz nominal values will cause the respective maximum errors to change by ± 0.00008\%. Thus, the method is sufficiently accurate for the excitation control. This frequency measurement method is also used to measure \( f_{\text{out}} \) in another (separate) two counter setup such as counters #2 and #4.

4.4 Digital-to-Analog Signal Instrumentation

The excitation control scheme uses several digital-to-analog (D/A) conversion processes, which employ 12-bit, bipolar and inverting, multiplying digital-to-analog converters (DAC's) to generate the required analog signals. These devices provide an interface between the digital words (binary codes) of the PCs and the continuous analog world within the excitation system. Under software control, each DAC takes the assigned digital words as inputs and generates a stepped output voltage. Figure 4-6(a) shows the block diagram of a single-channel of the DACs used interfaced to a computer data-bus via an output (Latch) register. The corresponding 12-bit data format of the DAC channel is shown in Fig. 4.6(b).

The waveform of the output voltage, \( u(t) \), of the DAC of Fig. 4.6 can be controlled by the pattern of the digital words applied to the output register, the rate of application of the digital words and the DAC reference supply \( U_{\text{REF}}(t) \), which can be an output of another DAC [59 - 62]. Essentially, the DAC performs a programmable hardware multiplication as it combines each digital word with the reference signal to generate an output. This provides a fast way to accomplish the multiplication arithmetic as compared to the relatively slower software multiplication. The bipolar output \( u(t) \) of the DAC of Fig. 4.6 can be described as:
where $\eta = \sum S_i 2^i$, where $i = 1, 2, \ldots, 12$. The value of each bit $S_i$ can be either 0 or 1. The value of $\eta$ is minimum and equal to zero when all bits are at logic zero ($S_i = 0$), and the maximum value is approximately unity when all the bits $S_i$ are set to 1. For each value of $\eta$, the bit sequence $S_i$ ($i = 1, 2, \ldots, 12$), corresponds to an integer, $D$. For $\eta = 0$, $D$ is equal to zero and, for $\eta = 1$, $D$ is equal to 4095 ($2^b - 1$, where $b$ is the number of bits

\[ u(t) = -U_{\text{REF}} (1 - 2\eta) \]  

(4.14)

Figure 4.6: (a) A block diagram of a DAC interfaced to a digital computer via an output register. (b) The data format of the 12-bit DACs used in the excitation system.
in the data format of the DAC). Since $\eta$ cannot be negative, the variation of this factor suggests that the pattern data should be binary offset. In the case of a 12-bit data format, the offset value is $2^{b-1} = 2048$.

Under software control, the digital values of any variable $w$ (within the computer) can be mapped to the DAC analog values so as to optimize the sensitivity of the analog signal, $u(t)$. In the case where the measurement range for $w$ is $-w_M < w < w_M$, the mapping of such $w$ bipolar values into 12-bit digital numbers, $D_w$, can be defined by:

$$D_w = INT[2048(1 - w/w_M)]$$  \hspace{1cm} (4.15)

$$\beta_w = U_{REF} / w_M$$  \hspace{1cm} (4.16)

where $w_M$ is the maximum value of $w$, and $\beta_w$ is the sensitivity of the DAC output voltage signal in volts per unit of the variable $w$. Equation (4.15) is suitable for metering bipolar signals such as bipolar voltages, slip, and frequency deviations from a reference value. Sometimes, a variable such as the rotor speed $n_r$ and the output frequency $f_{out}$ may not be assigned a negative value. These are unipolar variables. A typical measurement range of such variables would be $0 \leq w < w_M$. In this case, Eqn. (4.15) can be modified for sensitivity optimization to:

$$D_w = INT[2048(2 - w/w_M)]$$  \hspace{1cm} (4.17)

On-line programmability of $\beta_w$ can be accomplished by having a lookup table $L_w[x]$ containing different values of $w_M$ indexed by an integer $x$. This integer $x$ can be chosen and entered from the keyboard of the computer dynamically such that:
\[ \beta_w = \frac{U_{\text{REF}}}{L_w[x]} \]  
\[ D_w = \text{INT}\{2048*(1 - w/L_w[x])\}; \text{ if } -w_m < w < w_m \]  
\[ \text{or} \quad D_w = \text{INT}\{2048*(2 - w/L_w[x])\}; \text{ if } 0 < w < w_m \]

4.5 Digital Filtering for Data Smoothing

Preliminary studies on the excitation problem [60, 61] have shown that the performance of the variable-speed DESG is characterized by slow dynamics, much less than 2 Hz. Such slow dynamics allow the use of low sampling rates (20 Hz - 35 Hz) in the excitation system. However, the use of a computerized excitation system near high current machines, such as the DESG, makes high-frequency noise (> 60 Hz) due to electromagnetic interference unavoidable [92]. Even if anti-aliasing analog-low-pass prefiltering is applied on all signals before digitizing them, still some of the high frequency noise will contaminate the acquired data. Smoothing of this data is therefore necessary.

The Least Squares (LS) digital filters have been found to be suitable for smoothing the acquired data within the excitation system modules. These LS filters have a linear phase, cause no distortion to passband signals, and introduce minimum error in the filtering process. As a result of these properties, the LS, non-recursive, smoothing filters can discriminate against the rapid fluctuations in the data while preserving the slowly changing dynamics [93]. This feature of the low-pass filters is illustrated by their frequency response, \( H(\Omega = f / f_m) \), shown in Fig. 4.7 (for LS quadratic filters with data window sizes of \( W = 5 \) and 9 points).

Real-time filtering in the excitation system uses a filter block consisting of five LS quadratic filters of data windows \( W = 5, 7, 9, 11, \) and 13 points. Each of these filters can be chosen and engaged dynamically. The structure of these five filters and the software procedure used to implement them as causal filters are detailed in Appendix B.
4.6 Summary

In this chapter, the signal instrumentation schemes employed in the excitation system are presented. The RMS-to-DC converter (AD536AJ) is used as a terminal voltage transducer. A software-based error-formulator is used for deriving the terminal voltage error signal, $e(t)$. Also, the frequency and speed metering scheme used in the excitation system is presented. The programmable CET method is investigated for implementation on a microcomputer platform. It is shown that this CET method can be synchronized to other sampling operations when the sample rate (i.e. the CET) is fixed. Furthermore, 12-bit, bipolar and inverting, multiplying DACs are investigated for generating the required analog signals within the excitation system. Finally, Least Squares quadratic filters are discussed as suitable for smoothing the data acquired within the excitation system modules.
5. IMPLEMENTATION OF THE REAL-TIME TWO-PHASE EXCITATION SYSTEM

5.1 Introduction

A prototype of the computer-based two-phase excitation system for the variable-speed dual-excited synchronous generator, based on the excitation algorithm described in Chapter 3, has been implemented. The excitation system is implemented on a real-time distributed computing hardware consisting of three personal computers (PCs). Such a hardware gives sufficient flexibility to implement the excitation algorithm. Also, the PCs give enough resources and computation power for implementing the required measurement and signal processing schemes. This prototype excitation system has a frequency regulation (FR) scheme and a voltage regulation (VR) scheme. These two regulation schemes are designed to control the excitation voltages simultaneously, but always acting independently. This chapter describes the hardware of the excitation system prototype, the components of the excitation system software and the operation of the excitation system. Also, the details of the intermodular interactions among the modules of the excitation system software are presented. The FR and the VR control schemes are realized through such interprocess interactions.

5.2 Hardware Description

Figure 5.1 shows the block diagram of the prototype of the computer-based two-phase excitation system. In this figure, PC1, PC2, and PC3 are 8086 AT&T/10 MHz microcomputers with bus speeds of 5 MHz. These three microcomputers are programmed as dedicated modules for amplitude control, signal generation, and frequency control, respectively.
Figure 5.1: A block diagram of the prototype of the computer-based two-phase excitation system supplying a DESG.
Each PC has a computer-interfaced two-channel, 12-bit, multiplying digital-to-analog converter (DAC). In Fig. 5.1, the channels are identified as DAC_{x1} and DAC_{x2}, where x is the PC number, i.e. x = 1, 2 or 3. The voltage outputs of these DACs can best be described by using Eqn. (4.14), i.e. in terms of the factors \( \eta_{x1} \) and \( \eta_{x2} \), and the reference supply, \( U_{\text{REF}} \), of these DACs. The PCs have a set of electronic programmable real-time timers built around the 8254 timer chip [94]. These timers are used for frequency synthesis and frequency or pulse-width measurements as discussed in Chapters 3 and 4. In addition, each PC has an 8-channel analog-to-digital converter (ADC) (DAS-8 cards) for data acquisition. Most important in the excitation control is the ADC of PC1 and, thus, is the only one shown in Fig. 5.1. The microcomputer PC1 uses this ADC to measure the output terminal voltage of the generator via the voltage transducer block. The amplifiers BOPA1 and BOPA2 (KEPCO - BOP15V-20A (M)) are used to amplify the control signals \( v_d \) and \( v_q \). The dual-excited synchronous generator is identified as DESG. A shaft encoder capable of producing 360 ppr is used to monitor the speed of the rotor. The generator is driven by a d.c. motor which is labelled as the prime mover.

Furthermore, Fig. 5.1 shows a bidirectional, programmable, 24-bit parallel data line connecting PC2 and PC3. This data line is configured using two PIO-12 plug-in cards, one on each of these two PCs. The 8255 programmable peripheral interface chip [94] on each of the PIO-12 cards controls the 24 bits of the digital I/O data line. These 24 bits are accessible via three 8-bit ports identified as ports A, B, and C in Fig. 5.2. In this figure, these ports on the PIO-12 cards are hardwired in pairs, i.e. A-A, B-B, and C-C. For each pair of ports, eight bits as parallel data can be transmitted between PC2 and PC3 along the eight lines connecting the two ports, simultaneously.

The functional configuration of the 24-bit data line is software-controlled partly from PC2 and partly from PC3. In fact, the data line can be configured to operate in either a unidirectional or bidirectional mode. The choice between the two modes is accomplished under software control. The microcomputer PC2 receives coded data containing the status of PC3, phase sequence and the value of the jump index, J, from PC3 via this data line. The value of J is used in PC2 to select a pattern of data that defines one cycle of each sinusoidal
wave (sine and cosine), i.e. the number of samples per cycle, \( N \). The selected patterns are then used to generate the excitation voltage signals using DAC_{21} and DAC_{22}. The sample rate of application of the pattern data to these DACs is controlled by a square wave (FM) signal from PC3 which is fed through a digital I/O port in PC2. This FM signal is generated using programmable counters in PC3. The frequency of this FM signal can be adjusted automatically according to Eqn. (3.7) when the clock rate \( f_{CK} \) is used to vary \( f_{sa} \). Also, the frequency of this signal can be manually set to be constant when \( f_{sa} \) is varied by using \( N \) (Eqn. (3.8)). Another square wave signal generated in PC1, which has a frequency of \( f_{sa} = f_0 / 2 \), is used to synchronize the sampling operations in PC1 and PC3.

Equations (3.1) and (3.2) have two parts, i.e. \( U_{A_{sa}} = U_f (1 - \phi(e_n)) \) and \( A \cos(2 \pi f_{sa} n T_{CK}) \) or \( A \sin(2 \pi f_{sa} n T_{CK}) \). The amplitude of the excitation voltage signals is done by adjusting the first part, \( U_{A_{sa}} = U_f (1 - \phi(e_n)) \). The frequency of the signals is

---

**Figure 5.2:** Hardware connection between the ports of the PIO-12 cards for realizing the 24-bit data line between PC2 and PC3.
controlled by adjusting the frequency of the second part of each of the equations. These two parts should be multiplied in real time on a continuous basis to generate variable-amplitude variable-frequency (VAVF) excitation voltages, \( v_d \) and \( v_q \). This multiplication can be accomplished fast by using numeric coprocessors or multiplying DACs. However, the sampling processes in PC1 and PC3 are mainly data acquisition processes which are driven at the constant sample rate \( f_{sa} \). On the other hand, the sampling process in PC2 is driven at a variable sample rate, \( f_{ck} \), which is controlled by the FM-signal from PC3. For this reason, the multiplication of the two factors in Eqns. (3.1) and (3.2) may not be done in one PC and, thus, only the use of multiplying DACs is feasible. In Fig. 5.1, the hardware multiplication is implemented by having the reference supply, \( U_{\text{REF}} \), of DAC\(_{21}\) and DAC\(_{22}\) in PC2 controlled by the output of DAC\(_{12}\) of PC1, \( U_{\text{AM}} \). This reference supply is controlled such that \( U_{\text{AM}} = -U_{\text{REF}} \) (Eqn. (4.14)).

### 5.3 Software Description

The excitation system software consists of three real-time application programs namely, AMMODULE in PC1, SIGGEN in PC2, and FMODULE in PC3. These three programs are time critical modules. Each of them must perform a set of activities and produce responses at times dictated by external real-time event triggers. These event triggers specify time-windows during which the programs sample designated sensors, compute the required control responses and output the processed values to output devices for control or signal visualization purposes, or to mass storage devices for off-line processing. These features qualify the excitation system for use as a personal instrument [56, 95]. The novelty of the excitation system is based on the structure of these three program modules. The structure allows the programs to run continuously in real time. In addition, the structure permits the control variables and parameters of the excitation system to be adjusted on-line either manually or automatically.

Data can be acquired by means of ADCs, programmable timers, peripheral interface parallel I/O, and also can be keyed into the PCs via the keyboards of the PCs. These programs output processed data to the outside world as binary data via parallel I/O interfaces, as
alphanumeric text to the computer monitors, as analog signals for control or strip chart recording via DACs, and as floating point or integer data to mass storage devices of the computers. Appendix C presents some guidelines for programming the plug-in cards of the excitation system. Details of each of the three programs are presented in the following sections. The excitation control is achieved through the intermodular interactions of these three programs as illustrated in Figs. 5.3 and 5.4.

The three programs of the excitation system software are designed to run continuously with a "do while the user request from the keyboard, if there is any, is not to wind-up and quit" structure. This structure is illustrated by the flow chart of Fig. 5.5. In this structure, all assigned tasks of a module are grouped into blocks of code. Then, these blocks of code are organized into a main loop so that, on event trigger, each block is executed once per pass through the loop.

Each module has a Keypress Event/Keyboard Hit Event trigger. This trigger causes the module to respond dynamically to the user requests entered via the keyboard of the respective microcomputer. In addition to the Keypress Event trigger, the program AMMODULE has two more event triggers and the programs FMMODULE and SIGGEN each have one more event trigger. In this application, these event triggers are digital signals which are scanned by the excitation system software continuously. The program AMMODULE has a Measure-Frequency-Flag (MFF) and an Event-Trigger-Flag (ETF). The MFF trigger initiates the measurement of the frequency of the terminal voltage, $f_{\text{out}}$. The ETF is a general trigger that controls all the other activities of the program AMMODULE. This ETF trigger also controls the activities of the program FMMODULE in synchronism with the activities of the program AMMODULE. When the ETF goes HIGH (Logic = 1), a sampling event occurs in both PCI and PC3. A LOW ETF (Logic = 0) indicates a waiting state. During this state, the two programs are structured to perform background tasks, e.g. responding to the requests from the keyboards of these PCs. The operations of AMMODULE and FMMODULE programs are synchronized to run at a rate $f_{\text{m}} = f_{0}/2$. The activities of the program SIGGEN are triggered by an FM-Flag which is controlled by the FM signal at the rate $f_{\text{ck}}$. 
Figure 5.3: Intermodular interactions among the modules of the excitation system software to realize the VR scheme.
5.3.1 The Amplitude Modulation Module (AMMODULE)

The program AMMODULE in PC1 is structured to measure both the magnitude, $V_t$, and the frequency, $f_{out}$, of the terminal voltage. It also produces an analog signal proportional to the measured output frequency using DAC_{II} (Fig 5.1) by controlling the factor $n_{II}$ of this DAC (Eqn. (4.14)). The integer data that controls $n_{II}$ is generated in real time for every MFF cycle according to:

$$D_{out} = INT\left\{2048 \left(2 - \frac{f_{out}}{f_{outm}}\right) \right\}; \quad 0 \leq f_{out} < f_{outm}$$ (5.1)
Figure 5.5: A flow chart showing the general structure of the application programs of the excitation system software.
where \( f_{\text{outM}} \) indicates the range value of \( f_{\text{out}} \). This program, AMMODULE, is a control module for setting parameters of the software-based blocks of the VR loop (Fig. 5.3). The flow chart of the program AMMODULE is shown in Fig. 5.6. The details of the flow chart are presented in Appendix D. The VR control is achieved by controlling the factor \( \eta_{12} \) of DAC12 (PC1) using the terminal voltage error signal \( e(t) \) such that:

\[
U_{\text{REF}} = -U_0(1 - \varphi(e(t))) = -U_0(1 - 2\eta_{12}) = -U_{\text{AM}} \tag{5.2}
\]

where \( U_0 \) is fixed at -10V and \( \varphi \) is the programmable control function which is a function of the voltage error signal, \( e(t) \). Consequently, the outputs of DAC21 and DAC22 in terms of their factors \( \eta_{21} \) and \( \eta_{22} \), respectively, become:

\[
\begin{align*}
\nu_q &= U_0(1 - 2\eta_{12})(1 - 2\eta_{21}) = U_{\text{AM}}(1 - 2\eta_{21}) \tag{5.3} \\
\nu_d &= U_0(1 - 2\eta_{12})(1 - 2\eta_{22}) = U_{\text{AM}}(1 - 2\eta_{22}) \tag{5.4}
\end{align*}
\]

There are many control functions that could be used to implement the function \( \varphi(e) \). The most popular are the proportional (P), integral (I) and the derivative (D) control functions. In the literature, the term control function is also referred to as control law, control mode or control algorithm [70, 96 - 98]. A PID control law is a parallel combination of the proportional, the integral, and the derivative control modes. Figure 5.7 shows a structure of the PID control law. This PID control law is usually used where complete knowledge of the controlled plant is lacking [96] as it is the case with the excitation system controlling the DESG.

The use of the PID control law in the excitation system requires the tuning of the three parameters \( K_p, K_i, \) and \( K_d \) of the controller algorithm to the DESG. For testing the voltage regulation (VR) loop of the excitation system, the PID control law with an open structure
Figure 5.6: The flow chart of the program AMMODULE.
Proportional Control

\[ K_p \]

\[ e(t) \]

From the Error Formulator

\[ K_i / s \]

Integral Control

\[ K_d \times s \]

Derivative Control

\[ m(t) \]

Total control action

\[ G_{cv}(s) \]

**Figure 5.7:** The structure of the proportional plus integral plus derivative (PID) control law as employed in the excitation system.

has been implemented in the program AMMODULE. The implementation is such that one or more of the individual control modes (P, I, or D) can be engaged or disengaged dynamically, if necessary. In Fig. 5.7, a smoothing low-pass filter (LPF) is used to reduce the differentiation noise in the derivative control. In the program AMMODULE, the parameters of the PID control law and those of the smoothing filter can be adjusted on-line. The details of the implementation of the PID control law for the VR scheme are presented in Appendix E.

5.3.2 Frequency Modulation Module (FMMODULE)

The microcomputer PC3 executes FMMODULE to measure \( f_o, n_e \), and to calculate the slip frequency, \( f_s \) and \( \text{sign}[s] \). In addition, it produces analog signals \( n_e(t) \) and \( \text{sign}[s], f_s(t) \) proportional to the rotor speed and the slip frequency via DAC_{31} and DAC_{32}, respectively. The voltage outputs of these two DACs are programmable in terms of their factors \( \eta_{31} \) and \( \eta_{32} \), respectively. These factors \( \eta_{31} \) and \( \eta_{32} \) are generated in real time for every ETF cycle according to the following mappings:
\[ D_{ur} = \text{INT}\{2048(2 - n_t / n_{m})\}; \quad 0 \leq n_t < n_{m} \]  
\[ D_{ub} = \text{INT}\{2048(1 - \text{sign}(s_f / f_{m})\}; \quad 0 \leq f_s < f_{m} \]  

(5.5)  

(5.6)

where \( n_{m} \) and \( f_{m} \) are the range values for \( n_t \) and \( f_s \), respectively.

The program FMMODULE is a control module for performing functions that tune the FR control loop. The flow chart of the program FMMODULE is shown in Fig. 5.8. The details of the flow chart are given in Appendix D. After processing the acquired data for each ETF cycle, the program FMMODULE first determines the appropriate value of \( N \). Then, it updates the frequency of the FM signal, \( f_{ckr} \), if necessary. It also updates the jump index \( J \) from the calculated value of \( N \). This jump index \( J \) is required in PC2 for dynamic control of the pointer that scans the pattern lookup table. There are two options for determining the value of the jump index \( J \). In the first option, \( J \) is accessed from a lookup table, \( \text{JMP}[x] \) (Fig. 5.8). This option corresponds to the case that Eqn. (3.7) is used as the slip-frequency control function. In the second option, the value of \( J \) is determined in real time as \( J = \text{INT}(N_{m} / N) \), where \( N_{m} \) is the maximum number of samples per cycle in the pattern lookup table. This case applies when Eqn. (3.8) is used as the slip-frequency control function. After this, the values of \( \text{sign}(s_f) \) and \( J \) are conveniently packaged and then transmitted to PC2 via the 24-bit data line. This process is repeated for every ETF cycle.

5.3.3 The Signal Generator Module (SIGGEN)

Figure 5.9 shows the flow chart of the program SIGGEN and its details are given in Appendix D. The operation of this program is such that the factors \( \eta_{21} \) and \( \eta_{22} \) (of \( \text{DAC}_{21} \) and \( \text{DAC}_{22} \) in Fig. 5.1) are controlled to follow the cosine and sine waveform patterns described by Eqns. (3.1) and (3.2). These pattern data are generated during the initialization stage of the signal generation program, SIGGEN, according to the scheme described in section 3.2.3 and 3.4. The pairs of the pattern data are processed and stored as reference
Figure 5.8: The flow chart of the program FMODULE.
Figure 5.9: The flow chart of the program SIGGEN.
integer numbers, $D_{co}(k)$ and $D_{si}(k)$, ready for digital-to-analog conversion according to:

$$D_{co}(k) = INT\{2048 - 409.6\times A \times \cos(2\pi k / N)\} \quad (5.7)$$

$$D_{si}(k) = INT\{2048 - 409.6\times A \times \sin(2\pi k / N)\} \quad (5.8)$$

for $k = 0, 1, 2, \ldots, N - 1$, where $N = 4096$. These pattern data are calculated based on $U_{REF} = -5V$, which has been selected to give signals with the specified amplitude $A$. This parameter, $A$, is used to control the range of the factors $\eta_{21}$ and $\eta_{22}$ of DAC$_{21}$ and DAC$_{22}$, respectively. For example, if $A = 1.0$ V then $0.4 \leq \eta_{2x} \leq 0.6$, and for $A = 2.0$ V, the range becomes $0.3 \leq \eta_{2x} \leq 0.7$, where $x = 1$ or $2$. This control is very useful for limiting and optimizing the outputs of the amplifiers BOPA1 and BOPA2. The gain factor of the limiter block (Figs. 2.5 and 5.3) $G_{2y}(a) = K_{2y}$ is given by:

$$K_{2y} = |1 - 2\eta_{2xM}| \quad (5.9)$$

where $\eta_{2xM}$ is the maximum value of $\eta_{2x}$ for a chosen value of $A$. Thus, if $A = 1.0$ V, $K_{2y} = 0.2$, and for $A = 2.0$ V, $K_{2y} = 0.4$. These values of $K_{2y}$ correspond to limited ranges of $\pm 2V$ and $\pm 4V$ of input voltages to the amplifiers, respectively. The output from DAC$_{y}$, i.e. $U_{AM} = -U_{REF}$, has a range of $\pm 10V$.

For every cycle of the FM-Flag, the program SIGGEN in PC2 will scan the PIO-12 ports A, B, and C for new data. The program has a set of procedures for decoding the data received from PC3 via the 24-bit data line. The device check data received from port C allows the program SIGGEN to recognize whether or not PC3 is talking [96] to PC2. Also, the same device status data will inform PC2 to select the appropriate procedure for decoding the data sent from PC3 to obtain the jump index $J$ and the slip sign, $sign[J]$. The program SIGGEN utilizes these values of $J$ and $sign[J]$ from PC3 to control the pointer that scans
the pattern lookup table. Details of programming the 24-bit data line to realize the talk-listen [96] link between PC3 and PC2 are discussed in Appendix C.

The FM signal, fed to PC2 as a digital input FM-Flag (Fig. 5.9) is scanned continuously by SIGGEN. The frequency of this FM signal, $f_{CK}$, controls the speed of execution of SIGGEN. Execution speeds of the other two programs, AMMODULE and FMMODULE, are controlled such that the program SIGGEN runs at least twice as fast. In this way, data from PC3 is received by PC2 on time without introducing delays in the FR and the VR control loops.

5.4 Operation of the Excitation System

The three real-time application programs of the excitation system software, i.e. AMMODULE, FMMODULE, and SIGGEN, are designed to run continuously and independently in separate PCs. All three programs can run under MANUAL or AUTOMATIC modes of control, and these modes can be engaged dynamically. The programs are equipped with user interfaces that are based on the command line approach [99]. The user interfaces are protocols consisting of single alphanumeric characters. These protocols use keyboard key codes as on-line software potentiometers, switches and tokens for choosing and adjusting the values of the different parameters and variables in the excitation system. These command line user interfaces are fast and flexible. Details of the command protocols of the three programs of the excitation system are presented in Reference 100.

Under the MANUAL control mode, the programs will perform hardware initialization, and will set the default control parameters and variables. These variables are set via the keyboards of the respective PCs. The MANUAL mode is also useful for setting the desired operating conditions for the excitation system, i.e. specifying the reference voltage, $V_{REF}$, the reference frequency, $f_0$, and the sampling rate for the data acquisition processes in PC1 and PC3. The AUTOMATIC control mode refers to the operation of all the three programs when the control variables in the modules are adjusted automatically.
The program SIGGEN is critical to the operation of both the FR and the VR control schemes. It is this program that performs the signal generation. Without the FM control signal, the data packages containing $J$ and $sign[s_i]$ from PC3, and without the amplitude control from PC1, the program SIGGEN will generate constant-amplitude, constant-frequency, excitation voltages ($V_q$ and $V_d$) out of DAC$_{21}$ and DAC$_{22}$. The amplitudes of the signals will depend on the factor $A$ in Eqns. (5.7) and (5.8), and the default value of $U_{AM} = U_{REF}$ from PC1. The frequency of the output signals will depend on the default values of the jump index $J$, the slip sign $sign[s_i]$, and the speed ($f_{CK}$) at which the program SIGGEN will be running in PC2.

5.5 Summary

This chapter has described a prototype of the computer-based two-phase excitation system for a variable speed dual-excited synchronous generator. The excitation system is implemented on a distributed computing hardware consisting of three personal computers (PCs). The signal and data interfaces in this hardware are realized by the use of specialized plug-in cards (peripherals). The software of the excitation system has three real-time application programs dedicated for amplitude modulation (AMMODULE), signal generation (SIGGEN), and for frequency modulation control (FMMODULE). These three programs are dedicated to the three PCs such that each of the PCs executes one of these programs. The frequency regulation (FR) and the voltage regulation (VR) schemes of the excitation system are realized from the intermodular interactions of the three programs. The programs can operate either under MANUAL or AUTOMATIC control modes and these two control modes can be engaged dynamically.
6. EXPERIMENTS, RESULTS AND DISCUSSION

6.1 Introduction

The implemented excitation system has been tested on a 3-phase, 3000-VA, 208-V, 60-Hz, 1800-rpm, star-connected dual-excited synchronous generator (DESG). The power amplifiers BOPA1 and BOPA2 (Fig. 5.1) are rated for 300 VA each. Several signals were used to monitor the performance of the excitation system and the generator response to different tests. These signals are \( n_r, \text{sign}(s_r)f_n, U_{\text{REF}} = -U_{AM}, v_q, i_6, i_8, f_{\text{OUT}}, \) and \( V_r \). Fig. 5.1 In this chapter, the experiments conducted on the excitation system and the experimental results obtained are presented and discussed.

The experiments conducted fall into two categories. The first category is a set of experiments for the validation of the two-phase signal generation scheme of the excitation system as implemented on the distributed microcomputer setup. The second category consists of experiments on the real time performance of the excitation system while supplying excitation currents to the variable-speed DESG.

6.2 Performance of the Computer-Based Signal Generation Scheme

One of the objectives of the experiments in this group was to test the ability of the signal generation scheme of the excitation system to track and respond to the slip signal, \( s_r = s_r(t) \), and the terminal voltage error signal, \( e = e(t) \), in real time. The other objective was to obtain results for comparing the point-based data processing approach with the buffer-based data processing approach used in the feasibility study of the excitation problem.
There are six experiments in this group. These experiments were designed to study the response of the signal generation scheme to the following commands:

1. Step changes in the clock rate $f_{CK}$ (i.e. the frequency of the FM signal in Fig. 5.1) for constant number of samples per cycle, $N$.

2. Step changes in the number of samples per cycle, $N$, at constant clock frequency.

3. Changes in the slip sign, $\text{sign}[s]$. 

4. Frequency modulation at constant amplitude.

5. Amplitude modulation at constant frequency.

6. Frequency modulation and amplitude modulation, both acting simultaneously.

For these experiments, two signal generators were used to supply the slip signal $s(t)$ and the voltage error signal $e(t)$ as test signals. The signal $e(t)$ was sampled by using the analog-to-digital converter (ADC) of PC1 in Fig. 5.1. The signal $s(t)$ was sampled by using the ADC of PC3. Both test signals were sampled at 30 Hz. The two amplifiers BOPA1 and BOPA2 and the variable-speed DESEG (Fig. 5.1) were in the OFF mode. Effectively, the results presented in this section correspond to the case where $G = 1$ in Eqns (2.1) to (2.3). The chart sensitivities for all figures in this chapter are given per smallest scale division of both the horizontal and vertical axes.

### 6.2.1 Frequency Synthesis by Clock Control

Frequency synthesis by using a programmable real-time clock is illustrated in Fig. 6.1. In this figure, low clock frequencies ($\leq 10$ Hz) were selected so that the clock signal, $V_{CK}$, could be recorded. Evident from this figure is that increasing the clock rate $f_{CK}$ for constant number of samples per cycle, $N$, increases the frequency $f_a$ of the generated voltage signals (Eqn. (3.7)). With this frequency synthesis scheme, low excitation frequencies ($< 100$ Hz) can be generated with extremely high accuracy.
Figure 6.1: Response to changes in the clock rate $f_{ck}$ for constant number of samples per cycle ($N = 32$).

Chart sensitivities: Horizontal, $0.2$ sec/div.; Vertical, $200$ mV/div. for the clock signal $V_{ck}$ and $100$ mV/div. for $V_g$. 
6.2.2 Response to Changes in the Number of Samples per Cycle

Figure 6.2 shows the effects of changing the number of samples per cycle, \( N \), at a constant clock frequency, on the generated voltage signals, \( v_q \) and \( v_{dq} \). One of these effects is that the size of the steps of the waveforms of the two signals decreases as \( N \) increases. The other effect is that the waveforms become more smooth with increasing \( N \). The third effect is that increasing \( N \) at a constant clock frequency decreases the frequency of the generated signals, \( f_{dc} \) (Eqn. (3.8)). All these effects do not affect the phase shift of 90° between the generated signals.

Also, Fig. 6.2 shows that the signal generation scheme can respond to changes in \( N \) dynamically and, thus, the waveform distortion of the generated signals can be controlled dynamically. This ability to respond to changes in \( N \) on-line illustrates the effectiveness of the pointer control process that scans the pattern lookup table. Changes in \( N \) are a result of effective tracking of the changes in the jump index, \( J \). This type of control is one of the advantages of the point-based data processing approach compared to the buffer-based data processing approach. In the latter case, the change in \( N \) requires a fresh initialization of the buffers containing the pattern data. This may be done only off-line [57, 58].

6.2.3 Response to Changes in the Slip Sign

The dynamic phase sequence setting using the sign of the slip values, \( sign[s_i] \), is illustrated in Fig. 6.3, for \( N = 256 \) and \( f_{ck} = 64 \text{ Hz} \). This figure shows the effectiveness of the pointer control process in changing the direction of scanning the pattern lookup table as the value of \( sign[s_i] \) is changed dynamically (Fig. 3.12, Eqns. (3.18) and (3.21)). This phase sequence control is required by the excitation system to satisfy the excitation requirement (4) of the variable-speed DESG, i.e. to control the phase sequence in such a way to compensate for the slip frequency, \( f_s \).
Figure 6.2: Response to changes in the number of samples per cycle, $N$, at a constant clock frequency ($f_{CLK} = 64$ Hz).

Chart sensitivity: Horizontal - 0.2 sec/div., Vertical - 100 mV/div.
Figure 6.3: Response to changes in the slip sign, $\text{sign}(s_r)$.

*Chart sensitivity:* Horizontal- 0.2 sec./div.,
Vertical- 100 mV/div. for both plots.
6.2.4 Frequency Modulation at Constant Amplitude

The frequency modulation scheme is implemented according to Eqns. (3.7) and (3.8) for the purpose of controlling the frequency $f_{da}$ of the excitation voltage signals, $v_d$ and $v_q$. The frequency $f_{da}$ should be equal to $f_s$ in order to satisfy the excitation requirements (2) and (4) simultaneously. Figure 6.4 shows the effect of the frequency modulation at constant amplitude. In this figure, the instantaneous values of the signal $s_r(t)$ are proportional to the slip values. This slip signal is used as the modulating signal. The sign of this slip signal should trigger the change of the phase sequence of the two excitation voltage signals, $v_d$ and $v_q$. This change in the phase sequence can be observed on the waveforms of these signals at the instants of the zero crossings of the slip signal.

The other aspect of this frequency modulation scheme is the flexibility in choosing the modulated frequency, $f_0$. This frequency $f_0$ is the desired frequency of the terminal voltage, $V_t$, of the variable-speed DESG. This frequency may be different from the rated synchronous frequency of the generator. Such a flexibility indicates that the frequency modulation scheme will allow the DESG to supply power at frequencies different from the rated value.

6.2.5 Amplitude Modulation at Constant Frequency

The amplitude of the excitation voltages, $U_{fr}$, should be adjusted so as to satisfy the excitation requirement (5) of the variable-speed DESG. The result of the amplitude adjustment is to keep the terminal voltage, $V_t$, constant. A negative amplitude modulation scheme is used to meet this requirement. This modulation scheme is implemented according to Eqns. (2.3), and (3.22) to (3.24). For testing this modulation scheme, the control function $\varphi(e)$ was set to be equal to $e(t)$, i.e. $U_{fr} = U_t(1 - e)$. The results of this test are shown in Fig. 6.5 for $U_t = 1.0$ V. The results of this figure show that the signal generation scheme can modulate the amplitude of the excitation signals accurately.
Figure 6.4: Frequency modulation at constant amplitude ($N = 128, f_s = 60$ Hz).

*Chart sensitivity:* Horizontal- $0.2$ sec./div., Vertical- $1\%$/div. for the slip signal $s_f(t)$ and $100$ mV/div. for $v_d$ and $v_q$. 
Figure 6.5: Amplitude modulation at constant frequency ($f_m = 4$ Hz).

*Chart sensitivity:* Horizontal- 0.2 sec./div., Vertical- 100 mV/div.

for both (a) and (b).
Figure 6.5 shows the results obtained by using the point-based data processing approach with multiplying DACs. For comparison purposes, Fig. 6.6 shows similar results obtained by using the buffer-based data processing approach. By a close observation of these two figures, it can be seen that the delay between $e(t)$ and $v_d(t)$ in Fig. 6.5 is negligible compared to the delay between the two signals in Fig. 6.6. Thus, the use of the multiplying DACs with the point-based data processing approach provides a faster and more accurate way to track the voltage error signal, $e(t)$, for regulating the terminal voltage $V_t$ of the DESG.

6.2.6 Frequency Modulation and Amplitude Modulation, Both Acting Simultaneously

Figure 6.7 shows the variable-amplitude variable-frequency (VAVF) two-phase excitation voltage signals, $v_d$ and $v_q'$ as a result of having the frequency modulation and the negative amplitude modulation, both acting simultaneously in real time. The results of this figure correspond to the point-based data processing approach. From this figure, it can be noticed that the tracking of the test signals $e(t)$ and $s_r(t)$ is fast and accurate. The change in the phase sequence takes place at the zero crossings of the slip signal $s_r(t)$. With the VAVF signal format of Fig. 6.7, the two phase excitation voltage signals will satisfy all the five excitation requirements of the variable-speed DESG.

Figure 6.8 shows the results obtained using the buffer-based data processing approach. In this figure, the modulating signal is used as $e(t)$ as well as $s_r(t)$. The effectiveness of the amplitude modulation in Fig. 6.7 and Fig. 6.8 can be compared for slip values close to zero, which corresponds to low values of $f_{ck}$. In Fig. 6.8, due to slow sampling clock rates, $f_{ck}$, it takes a relatively longer time to empty a buffer of pattern data to the DACs. This slows down the amplitude modulation scheme. Thus, it is clear that the point-based data processing approach is a better way to implement the modulation schemes than the buffer-based data processing approach.
Figure 6.6: Amplitude modulation for different waveforms of the voltage error signal $e(t)$ - using the buffer-based data processing approach. Frequency of modulated signal is $f_d = 4$ Hz.

*Chart sensitivity:* Horizontal- 0.2 sec./div., Vertical- 100 mV/div. for both $e(t)$ and $v_d$. 
Figure 6.7: Response to frequency modulation and amplitude modulation, both acting simultaneously ($N = 128$). Chart sensitivity: Horizontal- 0.2 sec./div., Vertical- (a) 50 mV/div., (b) $1\%$/div., (c) and (d) 100 mV/div.
In this interval the amplitude modulation is slower than the frequency modulation. This affects the symmetry of the amplitudes.

Figure 6.8: Response to frequency modulation and amplitude modulation, both acting simultaneously, for the case of buffer-based data processing approach. ($f_o = 3.0 \text{ Hz}$, $U_p = 1.0 \text{ V}$).

*Chart sensitivity:* Horizontal- 0.2 sec./div., Vertical- 1%/div. for $s(t)$, and 50 mV/div. for $e(t)$ and $v_d$.

*Note:* same signal is used as $s_i(t)$ as well as $e(t)$.
6.3 Operating Characteristics of The Variable-Speed Dual-Excited Synchronous Generator

As discussed in Chapter 2, the dynamic behaviour of a dual-excited synchronous generator (DESG) operating at variable speed will depend mainly on the behaviour of the gain factor $K_{gv}$ (Eqn. (2.13)). The behaviour of this gain factor can be described by Eqn. (2.14) if the parameters $\alpha_0$ and $\alpha_1$ of this equation are known. However, the validity of Eqn. (2.14) is based on the assumption that the DESG has identical field windings. In practice, the two field windings may not be identical. This means that, for a specified value of $V_{f}$, the excitation currents $i_{f_d}$ and $i_{f_q}$ produced by the excitation voltages $v_{f_d}$ and $v_{f_q}$, respectively, may not be equal. As a result, the corresponding stator linkage fluxes $\Phi_d$ and $\Phi_q$ will not be equal. The result of this is ripples on the generated terminal voltage. The amplitude of these ripples will be highest for values of $f_s$ close to zero. Due to this fact, a saliency factor, $\rho$, defined as the magnitude of the ratio of the excitation currents $i_{f_d}/i_{f_q}$ has been used to quantify the saliency feature of the DESG. The case of identical windings corresponds to $\rho = 1$. For accurate operation of the excitation system, the condition $\rho = 1$ should be satisfied as closely as possible in real time over the entire operating speed range. This section, describes the measurement of $\rho$, $\alpha_0$, and $\alpha_1$ of the laboratory DESG used in the study. The measurement of $\alpha_0$ and $\alpha_1$ is intended to verify the structure and the accuracy of the DESG model given by Eqn. (2.14). A method for minimizing the effect of having non-identical field windings on the performance of the excitation system is discussed. Also, the resulting operating gain curves of the DESG at different operating conditions are presented.

6.3.1 Determination of The Saliency Factor.

The general behaviour of the saliency factor, $\rho$, can be determined from the d- and q-axis open-circuit characteristics of the DESG when the generator is excited by d.c. from the d- and q-axis field windings, respectively. Figure 6.9 shows these two open-circuit characteristics of the DESG used in the investigation. This figure shows that the two curves
do not coincide and, hence, the two field windings are not identical. Figure 6.10 shows the corresponding curve of the saliency factor plotted as a function of the terminal voltage for the case when the DESG is excited by d.c.

![Diagram](image)

**Figure 6.9:** The d- and q-axis open-circuit characteristics of the DESG used in the investigations.

Since the impedances of the field windings vary with \( f_s \), the value of the saliency factor will also depend on the value of \( f_s \). Thus, to each value of \( f_s \), a curve of the saliency factor exists. From Eqns. (2.12) and (2.13), \( V_t = K_{sv} V_a \) when the DESG is unloaded and unsaturated. Under these conditions, the saliency factor could be expressed in terms of the impedances of the field windings, i.e. \( \rho = \left| \frac{i_d}{i_q} \right| = \left| \frac{Z_{qa}}{Z_{ta}} \right| \), where \( Z_{ta} \) and \( Z_{qa} \) are the
impedances of the d- and q-axis field windings, respectively. When \( f_s = 0 \) (d.c. excitation), the saliency factor could be approximated by the ratio of the resistances of the field windings, i.e. \( \rho_{dc} = R_{q}/R_{d} \), where \( R_{d} \) and \( R_{q} \) are the resistances of the d- and q-axis field windings, respectively. In the case that the DESG is excited with a.c. \( (f_s > 0) \), the saliency factor could be approximated by the ratio of the self-inductances of the field windings, i.e. \( \rho_{ac} = L_{q}/L_{d} \), where \( L_{d} \) and \( L_{q} \) are the self-inductances of the d- and q-axis field windings, respectively. For the laboratory DESG used in the study, \( R_{d} = 1.705 \, \Omega \), \( R_{q} = 1.587 \, \Omega \), \( L_{d} = 0.265 \, H \), and \( L_{q} = 0.224 \, H \). Using these values, \( \rho_{dc} = 0.9308 \) and \( \rho_{ac} = 0.8453 \). From these results and those of Figs. 6.9 and 6.10, it can be generalized that, for a practical variable-speed DESG, the saliency factor is neither equal to unity nor is it constant.

Figure 6.10: The variation of the saliency factor \( (I_{q}/I_{d}) \) with the armature line voltage when the DESG is excited by d.c.
The problem of non-identical field windings could be eliminated by a control scheme that adjusts the amplitudes of the excitation voltages $v_{fd}$ and $v_{fq}$ separately such that $\Phi_d = \Phi_q$ over the entire operating speed range. The excitation system would thus regulate the excitation currents $i_{fd}$ and $i_{fq}$ separately. This requires the use of current sources instead of voltage sources to supply the required excitation currents [34]. This approach conflicts with the thesis objective of using voltage sources. However, to minimize the effect of not having $\rho = 1$ on the performance of the implemented excitation system, the amplifiers (Fig. 5.1) were adjusted to have gains $G_d$ (d-axis) and $G_q$ (q-axis) such that $G_d = \rho_v G_q = G$, where $\rho_v = (\rho_{dc} + \rho_{ac})/2 = 0.9$.

6.3.2 Determination of the Parameters $\alpha_0$ and $\alpha_1$

For the determination of the parameters $\alpha_0$ and $\alpha_1$, the excitation system was used as a variable-frequency voltage signal generator and the DESG was operated in its unsaturated region, which corresponds to the terminal voltage range of $0 \leq V_t \leq 180$ V (Fig. 6.9). This experiment has two steps. Firstly, the DESG is operated at a specified constant speed ($n_r$), constant excitation frequency ($f_e$) and a specified phase sequence, i.e. a fixed value of $\text{sign}[s_f]$. Then, $V_n$ is varied in equal steps and then several step responses, $V_t$ vs $V_n$, of the generator are recorded as illustrated in Fig. 6.11. From these step responses, the value of the gain factor $K_{gv}$ corresponding to the operating settings is then calculated from $K_{gv} = \Delta V_t / \Delta V_n$. The average value of the gains from all the step responses gives a point on the constant-rotor speed gain curve. More data points are obtained by repeating this procedure of recording the step responses of the generator at different excitation frequencies without changing the rotor speed. The calculated curves of $K_{gv}$ (Fig. 6.12) are then used to determine the parameters $\alpha_0$ and $\alpha_1$ of Eqn. (2.14) by curve fitting. Different sets of data were obtained by repeating the experiments at different rotor speeds. Table 6.1 shows the values of these parameters for six different speeds of the rotor. Figure 6.12 shows a sample of three gain curves fitted to the measured data (shown by symbols on the figure).
There are 8 step responses in this figure. The values of \( V_i \) are recorded as phase peak values. The values of \( V_f \) are calculated from \( V_f = G K_v U_{AM} - G K_v U_{REF} \) (Eqn. (5.2), Fig. 5.3). In this case, \( K_v = 0.4 \), \( G = 9 \), and \( \Delta V_f = 3.6V \). The average value of \( \Delta V_i \) is given by:

\[
\Delta V_i = \left\{ \frac{4.5 + 4.5 + 5.0 + 4.0 + 4.0 + 5.0 + 4.5 + 4.5}{8} \right\} \text{ div. } \times 8.165V/\text{div.}
\]

\[= 36.7423V\]

Hence, \( K_{gv} = \frac{\Delta V_i}{\Delta V_f} = 10.2062 \).

**Figure 6.11:** Step responses of the laboratory DESG running at \( n_t = 1800 \text{ rpm} \) and excited with a.c. (\( f_s = 2 \text{ Hz} \) and \( \text{sign}[s] = -1 \)).
This figure confirms the accuracy of the model of Eqn. (2.14). This procedure of calculating $K_r$ from the step responses is valid as long as the DESG is not saturated. The average values of $\alpha_0$ and $\alpha_1$ of Table 6.1 were then used to obtain the gain curves (for the three cases discussed in Chapter 2) of the DESG shown in Figs. 6.13 to 6.15.

**Table 6.1:** Values of the parameters $\alpha_0$ and $\alpha_1$ of the dynamic model of the Laboratory DESG operating at constant speed.

<table>
<thead>
<tr>
<th>$n_r$ (rpm)</th>
<th>$\alpha_0$ (sec/rev)</th>
<th>$\alpha_1$ (sec$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1350</td>
<td>0.6507</td>
<td>0.6721</td>
</tr>
<tr>
<td>1500</td>
<td>0.6107</td>
<td>0.5740</td>
</tr>
<tr>
<td>1620</td>
<td>0.6169</td>
<td>0.5740</td>
</tr>
<tr>
<td>1800</td>
<td>0.6752</td>
<td>0.7316</td>
</tr>
<tr>
<td>2040</td>
<td>0.6080</td>
<td>0.6034</td>
</tr>
<tr>
<td>2250</td>
<td>0.5951</td>
<td>0.6116</td>
</tr>
</tbody>
</table>

Average values: $\alpha_0 = 0.6261$ sec/rev., $\alpha_1 = 0.6278$ sec.$^2$
Figure 6.12: Constant speed gain curves of the laboratory DESG showing the variation of \( k \) with excitation frequency. This figure shows the measured data points (shown by symbols) and the fitted curves.
Figure 6.13: Constant speed gain curves of the laboratory DESG showing the variation of $K_{gv}$ with excitation frequency. (Data obtained from the model).
Figure 6.14: Constant excitation frequency gain curves of the laboratory DESG showing the variation of $K_g$ with the rotor speed.
Figure 6.15: Constant generating frequency operation gain curve of the laboratory DESG for $f_0 = 50$ Hz and 60 Hz.
6.4 Real-Time Performance of the Computer-Based Excitation System

The results presented in this section show the real-time performance of the excitation system and the response of the dual-excited synchronous generator (DESG) to the variation in the rotor speed $n_r$. Four main cases of the operation of the excitation system are investigated for an isolated DESG (i.e. not connected to a constant frequency grid). These cases correspond to the following settings of the FR and VR schemes (Fig. 5.3).

1. The FR and VR schemes are both set to the MANUAL control mode.

2. The FR scheme is set to the AUTOMATIC control mode and the VR scheme is set to the MANUAL control mode.

3. The FR scheme is set to the MANUAL control mode and the VR scheme is set to the AUTOMATIC control mode.

4. The FR and the VR schemes are both set to the AUTOMATIC control mode.

A variation to case (2) is included in which the FR scheme is tested with step changes in the desired synchronous frequency, $f_0$. Also, a variation of case (4) is included in which the excitation system is tested to respond to a sudden application and removal of an inductive load. The signals $V_v$, $f_{out}$, $sign(s)$, $f_s$, $n_r$, $U_{ref} = -U_{amp}$ and either $v_d$ and $v_q$ or $i_d$ and $i_q$ were recorded simultaneously to monitor the generator response. The amplifiers BOPA1 and BOPA2, Fig. 5.1., were set to have the gains $G_q = 10.0$ and $G_d = G = 9.0$. These gains were selected based on a saliency factor $\rho_w = 0.9$ (section 6.3.1). The limiters in Fig. 5.3 were set to have the same gain of $K_{sv} = 0.4$. This setting corresponds to a limited amplitude range for $v_d$ and $v_q$ of $\pm 4$ V. All the results correspond to the case where the stabilizer block in Fig. 5.3 is disabled, i.e. $G_{iv}(s) = 0$, and the controller is a proportional (P) controller, i.e. $G_{iv}(s) = K_p$, and $\tau_{sv} = 10.0 \text{ sec}$. These settings were found sufficient for demonstrating the performance of the excitation system without complicating its design.
6.4.1 Response to Speed Variation When the FR and the VR Schemes are Both in Manual Control Mode.

Figures 6.16 to 6.21 illustrate the response of the DESG to the variation in the rotor speed, \( n_r \), for the case that the FR and the VR schemes are both operating in the manual control mode. Each of these figures show the performance of the excitation system at constant excitation frequency, \( f_s \), and a preselected phase sequence, i.e. a value of \( \text{sign}[s_i] \). Since, in this case, there is no frequency regulation and no terminal voltage regulation, the DESG driven at variable speed generates voltage with variable magnitude and variable frequency. The output frequency can be described by \( f_{out} = f_r + \text{sign}[s_i] f_s \), where the term \( \text{sign}[s_i] f_s \) has a different constant value for each of the figures. At a constant value of \( \text{sign}[s_i] f_s \), the variation of the terminal voltage depends on the gain \( K_{mv} \), which is a function of the speed \( n_r \) (Fig. 6.14). It can be seen from the plots (a) and (g) of these figures that the terminal voltage varies more or less linearly with the rotor speed \( n_r \) (Eqn. (2.15)).

Qualitatively, the percentage speed change for all the figures is less than 40% of the initial value of speed. It is therefore expected that the terminal voltage should also change by the same order of percentage. For example, for the results of Fig. 6.16, the rotor speed increases from 1566 rpm to 2034 rpm. This corresponds to 30% increase in the speed from the initial value of 1566 rpm. Correspondingly, the terminal voltage, \( V_r \), increases from 120 V to 150 V, which is 25% increase. Thus, the change in \( n_r \) results in approximately an equal change in the terminal voltage.

The ripples on the terminal voltage waveforms of plots (g) of Figs. 6.16 to 6.21 are caused mainly by having non-identical field windings. The amplitude and the period of these ripples decrease as \( f_s \) increases. This ripple problem may be corrected by adjusting the gains of the amplifiers dynamically such that \( i_{fi} = i_{fi} \) over the entire usable speed range.
Figure 6.16: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating in the manual control mode. (The DESG is unloaded, $f_s = 0.5$ Hz, $\text{sign}[s] = +1$, $f_{\text{out}} = f_r + 0.5$ Hz.)
Figure 6.17: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating in the manual control mode. (The DESG is unloaded, $f_i = 1.0 \text{ Hz}$, $\text{sign}[s] = +1$, $f_{\text{out}} = f_r + 1.0 \text{ Hz}$).
Figure 6.18: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating in the manual control mode. (The DESG is unloaded, $f_r = 1.0 \text{ Hz}$, $\text{sign}[s] = -1$, $f_{\text{OUT}} = f_r - 1.0 \text{ Hz}$).

**Chart Sensitivity**

**Horizontal:**
- 0.5 sec./div. for all plots

**Vertical:**
- (a) 18 rpm/div.,
- (b) 0.6 Hz/div.,
- (c) 200 mV/div.,
- (d) and (e) 100 mV/div.,
- (f) 0.6 Hz/div., and
- (g) 10 V/div. (line)
Figure 6.19: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating in the manual control mode. (The DESG is unloaded, \( f_s = 2.0 \text{ Hz} \), \( \text{sign}[s] = -1 \), \( f_{\text{out}} = f_s \cdot 2.0 \text{ Hz} \) )
Figure 6.20: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating in the manual control mode. (The DESG is unloaded, $f_s = 3.0$ Hz, $\text{sign}[s] = +1$, $f_{out} = f_s + 3.0$ Hz).
Figure 6.21: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating in the manual control mode. (The DESG is loaded, $f_s = 4.0 \text{ Hz}$, $\text{sign}(s) = +1$, $f_{\text{OUT}} = f_t + 4.0 \text{ Hz}$).
6.4.2 Response to Speed Variation When the FR Scheme is Acting Automatically and the VR Scheme is in the Manual Control Mode

The results of this test are shown in Figs. 6.22 to 6.30. For these figures, the desired output frequency is \( f_0 = 60 \) Hz. The frequency regulation for all these figures can be described by \( f_{\text{out}} = f_r + \text{sign}(s) f_s \). In this case, the FR scheme adjusts the term \( \text{sign}(s) f_s \) automatically to keep \( f_{\text{out}} = 60 \) Hz. Plots (d) and (e) of these figures show the effectiveness of the FR scheme in controlling the phase sequence of the two excitation voltages, \( v_d \) and \( v_q \). For these results, the rotor speed deviates within the range of \( \pm 16.67\% \) from 1800 rpm. This corresponds to a range of slip frequencies of \( 0 \leq f_s \leq 10.0 \) Hz.

The plots of the terminal voltage \( V_t \) (plots (g) of the Figs. 6.22 to 6.29) show that the generated voltage follows the gain curve of the VSCF operation at \( f_0 = 60 \) Hz, of Fig. 6.15. Figures 6.22 to 6.25 show the results for the case when the DESG is unloaded. For these results, the model described by Eqn. (2.16) can be used to interpret the variation of the terminal voltage, \( V_t \). Given that there is no automatic voltage regulation by the VR scheme, the gain \( K_{sv} \) will only vary with the excitation frequency, \( f_s \). Hence, the magnitude of the terminal voltage, \( V_t \), will follow the variation of the gain \( K_{sv} \). From the model, the gain is maximum at \( f_s = 0 \). All these figures support this fact. For example, in Fig. 6.23 the speed \( n_r \) varies from 1602 rpm to 1980 rpm. This causes the slip frequency to vary from +6.6 Hz to -6.0 Hz. From Eqn. (2.16), where \( \alpha_0 = 0.6261 \) (sec./rev.) and \( \alpha_1 = 0.6278 \) (sec\(^2\)), the gain \( K_{sv} \) will increase from 3.4193 (16.92\%) to 20.2057 (100\%) at \( f_s = 0 \). Then, the gain will decrease to 3.7499 (18.56\%). In comparison, plot (g) of Fig. 6.23 shows that the terminal voltage varied from 40 V (18.18\%) to 220 V (100\%) at \( f_s = 0 \). It then decreased to 50 V (22.73\%). These changes compare favourably with the changes of the gain \( K_{sv} \) obtained from Eqn. (2.16). Plots (d) and (e) of Fig. 6.25 shows the variation of the excitation currents for constant excitation voltage \( U_{\text{ref}} = -U_{\text{AM}} \), when the FR scheme is acting automatically with the DESG unloaded. As expected, the field currents increase with decreasing values of \( f_s \). Highest currents flow when \( f_s = 0 \).
Figure 6.23: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is unloaded, and $N = 32$ samples per cycle)

**Chart Sensitivity**

**Horizontal:**
0.5 sec./div. for all plots

**Vertical:**
(a) 18 rpm/div.,
(b) 0.6 Hz/div.,
(c) 200 mV/div.,
(d) and (e) 100 mV/div.,
(f) 0.6 Hz/div., and
(g) 10 V/div. (line).
Figure 6.24: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is unloaded, and $N = 64$ samples per cycle).
Figure 6.25: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is unloaded, and N = 64 samples per cycle. Plots (d) and (e) show the variation of the excitation currents $i_m$ and $i_q$, respectively.)
Figures 6.26 to 6.29 show the results for the case when the DESG is loaded. Due to the loading, the overshoot of the terminal voltage near $f_s = 0$ has decreased. This is expected because, under loaded conditions, the terminal voltage should be less than the internal (no-load) generated voltage. The voltage drop depends on the load current and the reactances of the machine at the supply frequency, $f_{\text{out}}$ [59]. Figure 6.29 shows the variation of the field currents when the DESG is loaded.

The use of small values of the number of samples per cycle, $N$, in the signal generation scheme will affect both the FR and the VR schemes. The effects are demonstrated by Figs. 6.22 to 6.24 for unloaded DESG and Figs. 6.26 to 6.29 for a loaded DESG. The effects on the FR scheme are due to the low sensitivity of the counter dividers (calculated using a small value of $N$) to the variation of the clock frequency, $f_{\text{ck}}$ (section 3.3). The performance of the VR is affected in that the terminal voltage becomes distorted (stepped) especially for values near $f_s = 0$.

Figure 6.30 demonstrates a protective scheme in the excitation system software which will not track clock rates $f_{\text{ck}}$ which exceed the specified maximum speed of the software driver for the DAC$_{21}$ and DAC$_{22}$ (PC2 of Fig. 5.1). In this case, the software was set to accept clock rates $f_{\text{ck}} \leq 540$ Hz. In other words, the excitation software will disable the automatic mode of the FR scheme if $f_{\text{ck}}$ exceeds this maximum rate. This protection was tested for $N = 128$ samples per cycle. For this value of $N$, the FR scheme should stop compensating for the slip frequency when $f_s > 4.22$ Hz. This is clearly illustrated by the plot of $f_{\text{out}}$ of Fig. 6.30. Thus, a faster driver (i.e. a faster computer or/and a faster program) will obviously extend the slip frequency control range for the FR scheme. Since excitation power is proportional to $f_s$, this protection will not allow the control scheme to overdrive the power amplifiers by limiting the value of $f_s$. 
Figure 6.26: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is loaded, and $N = 16$ samples per cycle).
Figure 6.27: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is loaded, and $N = 32$ samples per cycle).
Figure 6.28: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is loaded, and $N = 64$ samples per cycle).
Figure 6.29: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is loaded, and $N = 64$ samples per cycle. Plots (d) and (e) show the variation of the excitation currents $i_{d1}$ and $i_{q1}$, respectively).
Figure 6.30: Real-time response of the DESG to speed variation when the FR scheme is acting automatically and the VR scheme is in the manual control mode. (The DESG is loaded, and $N = 128$ samples per cycle.)
6.4.3 Response to Speed Variation When the FR Scheme is Set to Manual Control Mode and the VR Scheme is acting Automatically

The results of this test are illustrated in Figs. 6.31 and 6.32. The desired terminal voltage of the generator is $V_t = 150.0 \, \text{V}$. Figure 6.31 demonstrates the effectiveness of the VR scheme when the DESG is not loaded. Figure 6.32 illustrates the performance of the VR scheme when the DESG is loaded.

From Eqn. (2.15), the gain $K_{g_r}$ should increase with the rotor speed, $n_r$, since the automatic frequency regulation by the FR scheme is disabled. In this case, the amplitude control signal $U_{\text{ref}} = -U_{\text{AM}}$ will decrease as the gain increases with $n_r$ due to the action of the VR scheme. The effect of this action can be seen on plots (c), (d) and (e) of both Figs. 6.31 and 6.32. Both figures show stable responses and the steady state error is less than 2%.

6.4.4 Response to speed Variation When the FR and the VR Schemes are Both Set to Operate Automatically

Figures 6.33 to 6.36 illustrate the performance of the excitation system for the case when the FR and the VR schemes are providing automatic frequency regulation and automatic voltage regulation, simultaneously. For the results of Figs. 6.33 to 6.35, $f_0 = 60.4 \, \text{Hz}$ and $V_t = 150.0 \, \text{V}$ and the DESG is unloaded. In Fig. 6.36, $f_0 = 60.0 \, \text{Hz}$, and plots (d) and (e) show the excitation currents when the DESG is loaded. Qualitatively, these figures show that the frequency, the amplitude, and the phase sequence of the excitation voltages can all be controlled dynamically in real time to effectively regulate the terminal voltage, $V_t$, of a DESG and the frequency $f_{\text{out}}$ of the generated voltage. Also, it can be noted from these figures that the operating speed range decreased due to the fact that the amplifiers used could not supply more excitation power to the windings. This speed range can be increased by using power amplifiers of higher power and voltage ratings.
Figure 6.31: Real-time response of the DESG to speed variation when the FR scheme is in the manual control mode and the VR scheme is acting automatically. (The DESG is unloaded, \( f_s = 3.0 \) Hz, \( \text{sign}[s] = -1 \), \( f_{\text{out}} = f_s - 3.0 \) Hz; \( K_p = 50.0, K_v = 3.3117 \).)
Chart Sensitivity

Horizontal-
0.5 sec./div.
for all plots

Vertical-
(a) 18 rpm/div.,
(b) 0.6 Hz/div.,
(c) 200 mV/div.,
(d) and (e) 100 mV/div.,
(f) 0.6 Hz/div., and
(g) 10 V/div. (line).

Figure 6.32: Real-time response of the DESG to speed variation when the FR scheme is in the manual control mode and the VR scheme is acting automatically. (The DESG is loaded, $f_r = 3.0$ Hz, $\text{sign}[s_r] = +1$, $f_{\text{out}} = f_r + 3.0$ Hz; $K_p = 50.0, K_v = 2.1184$).
Figure 6.33: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating automatically. (The DESG is unloaded, $K_p = 30.0, K_{sv} = 2.1184$).
Figure 6.34: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating automatically. (The DESG is unloaded, $K_r = 40.0$, $K_{sv} = 2.1184$).
**Figure 6.35:** Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating automatically. (The DESG is loaded, $K = 70.0 \ K_{sv} = 2.1184$).
Figure 6.36: Real-time response of the DESG to speed variation when the FR and the VR schemes are both operating automatically. (The DESG is loaded, \( K_p = 50.0, \ K_v = 2.1184 \). Plots (d) and (e) show the variation of the excitation currents.)
6.4.5 Response to Change in the Desired Frequency

For this test, the rotor speed was set at ~1827 rpm and the $U_{\text{ref}}$ at -3.8 V. The reference frequency, $f_0$, was first changed from 60.0 Hz to 54.6 Hz, then from 54.6 Hz to 60.0 Hz. This was followed by a change from 60.0 Hz to 64.6 Hz, and then back to 60.0 Hz from 64.6 Hz. These step changes were easily applied to the excitation system by selecting a different reference frequency from the keyboard of PC1 (Fig. 5.1). The change is instant and it affects the calculation of the slip frequency in PC3 instantly.

The response of the FR scheme to such changes is shown in Fig. 6.37. Plot (a) of this figure shows the changes in $f_{\text{out}}$ and plot (b) shows the slip frequency changes. The slip frequency changes are from +0.9 Hz to -4.8 Hz, then from -4.8 Hz to +0.9 Hz, then from +0.9 Hz to +5.4 Hz and finally, from +5.4 Hz back to +0.9 Hz again. This ability of the excitation system to track the changes in the desired frequency indicates that such an excitation system can be used with the DESG to supply power at different frequencies. This means the ratings of the DESG can be easily customized for a different power system.

6.4.6 Response to Sudden Removal of Load

The frequency regulation (FR) and the voltage regulation (VR) schemes should provide both frequency stability and voltage stability during all types of allowable operating conditions of the DESG. One of these conditions is the sudden application and removal of a load [13, 15]. The computer-based excitation system was tested for this condition using a derated load of 500 VA, 4.8 A. The computer controlled VSCF generating system was set to provide a regulated supply of 100 V, 60.2 Hz.

The results of this test are shown in Figs. 6.38 to 6.40. Since a P-controller is used, it is expected that the voltage dip (on application of the load) and the overshoot of the voltage, $V_v$, (on removal of the load) [13] should increase with $K_p$. This is confirmed by the results of these figures. The voltage dip is about 20% in Fig. 6.38 and 30% in Fig. 6.39. The voltage overshoot varies from 20% in Fig. 6.38 to about 50% in
Figure 6.37: The response of the DESG to step changes in the desired output frequency, $f_0$, for the case when the FR scheme is in the automatic control mode. (Chart sensitivity: horizontal - 0.5 sec./div. for all plots, vertical - (a) 0.6 Hz/div., (b) 0.3 Hz/div., (c) 9 rpm/div., (d) and (e) 100 mV/div.).
Figure 6.38: The response of the DESG to a sudden application and then removal of an inductive load for the case when the FR and the VR schemes are both in the automatic control mode. ($K_p = 30.0$, $K_v = 2.1184$).
Figure 6.39: The response of the DESG to a sudden application and then removal of an inductive load for the case when the FR and the VR schemes are both in the automatic control mode. \((K_p = 40.0, K_{sv} = 2.1184)\).
Figure 6.40: The response of the DESG to a sudden removal of an inductive load for the case when the FR and the VR schemes are both in the automatic control mode. \( (K_p = 50.0, K_v = 2.1184) \).
Fig. 6.40. In all the three figures, the peak time of the transient responses is less than 0.5 sec. The recovery time [13] of the VR scheme for almost zero steady-state error varies from 1 sec. in the case of Fig. 6.38 to about 2 sec. in the case of Fig. 6.40. On the other hand, it is clear from these three figures that the frequency regulation scheme is extremely accurate. For both the application and the removal of load, the frequency dip/overshoot is much less than 0.5% (0.3 Hz), and the recovery time is less than 0.5 sec.

6.5 Summary

In this chapter, two categories of experimental results have been presented and discussed. The first category of results validates the signal generation scheme employed in the computer-based two-phase excitation system for the variable-speed dual-excited synchronous generator (DESG). The signal generation scheme has the flexibility to control the frequency, the amplitude, the waveform distortion, the frequency range, and the phase sequence of the generated two-phase excitation voltages, dynamically. This signal generation scheme meets all the five excitation requirements of the variable-speed DESG.

The second category of results demonstrate the performance of the implemented computer-based, real-time, two-phase excitation system acting on a variable-speed DESG. The results confirm that an unloaded variable-speed DESG can be represented as a first order system with a time varying gain factor. The gain factor is a function of the rotor speed and the excitation frequency. However, the gain factor is more sensitive to the variation of the excitation frequency than to the changes in the rotor speed. The performance results collectively show that the two regulation schemes of the excitation system, i.e. the FR and the VR schemes, are flexible, fast acting, and accurate. These two regulation schemes can control the excitation voltages while acting one at a time or both acting simultaneously.
7. SUMMARY AND CONCLUSIONS

7.1 Summary of Thesis

A dual-excited synchronous generator (DESG) can be applied as a variable-speed constant-frequency (VSCF) generating system. In such an application, this generator, which has two excitation windings, requires two-phase slip frequency excitation voltages. Practically, the application of this DESG for VSCF operation depends on the ability to generate and control these two-phase excitation voltages. In this machine, the regulation of its terminal voltage and the frequency of this voltage can be accomplished simultaneously by controlling specific parameters of the excitation voltages. Based on these facts, the research work reported in this thesis had the following objectives.

1. To develop a computer-based, real-time, two-phase excitation algorithm for controlling the excitation of a variable-speed DESG.

2. To investigate the interface requirements, timing and sampling requirements, and the measurement and signal processing requirements for implementing the excitation algorithm on a microcomputer environment.

3. To develop and test all the required real-time application programs.

4. To implement the excitation algorithm on a microcomputer platform.

5. To test and evaluate the resulting excitation system on a laboratory variable-speed DESG.
In Chapter 1, an overview of the different types of electrical power generating systems is presented. This overview introduces the excitation problem which arises when a DESG is selected for realizing a VSCF generating system. This is followed by a review of the methods that could be used to generate the required excitation voltage signals for such an application. The possibility of using a computer-based technique for generating such excitation voltage signals is introduced and the background of such a technique is presented. Also, the objectives of the research work are discussed.

In Chapter 2, the basic principles and the excitation requirements of the variable-speed DESG are discussed. The excitation problem is described analytically as a signal generation problem in that a two-phase excitation supply should be generated to satisfy, in real time, the excitation requirements of the variable-speed DESG. Furthermore, the solution to the excitation problem is described, using block diagrams, as having a frequency regulation (FR) scheme and a voltage regulation (VR) scheme. An overview of the hardware requirements for such an excitation system is also given.

The development of the real-time algorithm for controlling the excitation of the variable-speed DESG is described in Chapter 3. The technique used to synthesize and control the frequency of the excitation voltages is described as a frequency modulation algorithm. The technique used to control the amplitude of the excitation voltages is described as an amplitude modulation algorithm. The frequency modulation algorithm has been used to realize the frequency regulation scheme for the DESG. The amplitude modulation algorithm has been used to realize the voltage regulation scheme for the DESG. Included in the chapter is a discussion of some real-time constraints that could affect the performance of the FR and the VR schemes. Ways to overcome these constraints are also presented.

In Chapter 4, the signal instrumentation employed in the excitation system for metering the terminal voltage of the DESG, its speed, and the output frequency, is presented. In addition, the filtering scheme that uses Least Squares quadratic filters for smoothing the acquired data in the excitation system is discussed.
The excitation algorithm has been implemented on a distributed computing hardware consisting of three microcomputers (PCs). The hardware and the software of the implemented computer-based, real-time, two-phase excitation system are discussed in Chapter 5. The excitation software has three real-time application programs referred to as AMMODULE, FMMODULE, and SIGGEN. The FR and the VR schemes of the excitation system have been realized from the intermodular interactions of these three programs.

In Chapter 6, experimental results obtained from tests conducted on and using the excitation system are presented and discussed. Two sets of results are presented. The first set of results validates the signal generation scheme used in the excitation system. The second set of results demonstrates the real-time performance of the excitation system while supplying excitation voltages to a laboratory variable-speed DESG. The performance results present the response of the DESG to the variation in the rotor speed for four combinations of the MANUAL/AUTOMATIC settings of the FR and VR schemes. This second set of results includes the response of the excitation system and the DESG to changes in the desired frequency of the terminal voltage and to sudden application and removal of load.

7.2 Conclusions

A computer-based, real-time, two-phase excitation system for a variable-speed dual-excited synchronous generator (DESG) has been developed, implemented, and tested. Thus, the research objectives of the thesis have been met successfully. In this context, several significant conclusions can be drawn from this research work and summarized as follows.

1. The computer-based excitation system is a flexible signal generator that can meet the excitation requirements of the DESG. The excitation system is flexible in that, the frequency, the amplitude, the waveform distortion, the frequency range, and the phase sequence of the two generated excitation voltages can all be controlled dynamically.
2. Since the signal generation scheme uses numerically computed pattern data (of cosine and sine waves) for the signal generation, this data can be changed to generate a different set of voltage waveforms. Also, different multi-phase control signals can be generated by varying the number of the DAC channels used. In addition, more control options may be added to the scheme by increasing the number of control signals. The number of control signals can be increased by adding more ADC-channels, more timer/counter channels, or more parallel I/O data lines into the PCs used.

3. The open structure of the software of the excitation system allows for real-time experiments to be configured dynamically. This makes it easy to perform several real-time experiments in a single experimental session.

4. The excitation system can be implemented by using standard plug-in data acquisition components and standard personal computers (PCs). The use of such plug-in cards together with the open structure of the excitation system software allows for the excitation system to be used as a data acquisition system, a personal instrument, or/and a controller. For example, the excitation system can be used as a digital tachometer for measuring rotational speeds and frequencies or as a metering device to measure voltages.

5. The developed excitation system has a frequency regulation (FR) scheme and a voltage regulation (VR) scheme. With both regulation schemes operating automatically, the DESG can supply power at constant frequency and constant terminal voltage while its rotor is driven at a variable speed. The experimental results show that these two regulation schemes are fast acting and accurate. One of the novel feature of the excitation system is that the FR and the VR schemes control the excitation voltages simultaneously, but act independently and, thus, the system can be easily configured for other applications. For example, the excitation system can be used as a conventional automatic voltage
regulator (AVR) by setting the VR scheme to act alone under d.c. excitation and using only one of the generated excitation signals, $\nu_d$ or $\nu_q$. On the other hand, the excitation system becomes a low frequency generator when the FR scheme is used alone. In both of these cases, the FR and the VR schemes can be set to operate in the manual control mode or in the automatic control mode.

6. The experimental results show that the FR scheme is a *fast acting governing* scheme and it can handle a wide range of fluctuation in the rotor speed. This feature of allowing the randomness in the rotor speed to generate power at constant frequency is very desirable in utilizing the DESG for generation of electrical power from wind. The operating speed range can be freely chosen. However, this speed range should not violate the safety requirements of the mechanical design of the generator rotor.

7. With the FR scheme acting automatically and the rotor running at a variable speed, the DESG can generate electrical energy at constant frequency which can be selected on-line. This feature of the FR scheme gives the excitation system the ability to detect and follow the change in the desired synchronous frequency, $f_0$. Thus, such an excitation system can be used to customize the DESG to supply power at different frequencies. For example, a DESG running at a speed corresponding to $f_r = 55 \text{ Hz}$ can be used to supply power at $60 \text{ Hz}$ by setting $f_s = 5 \text{ Hz}$ and $\text{sign}[s_r] = +1$, or to supply power at $50 \text{ Hz}$ by setting $f_s = 5 \text{ Hz}$ and $\text{sign}[s_r] = -1$. The difference between the two settings is only in the phase sequence of the two-phase excitation voltages.

8. The slip frequency, $f_s$, is a sufficient control variable for regulating the frequency of the terminal voltage of a DESG under disturbances such as changes in the reference (desired) frequency, $f_0$, and the changes in the rotor speed. Changes in the rotor speed can be caused by a change in the input power to the prime mover or due to the loading of the DESG. For the facilities used in the study, up to $\pm 25\%$ change in the speed from the desired speed can be
compensated (when the VR is in its manual control mode). The ability of the excitation system to handle a wider slip range depends mainly on the availability of power amplifiers of higher rating. Also, a wider operating range of the slip frequency may require the use of a faster computer platform (PC2 of Fig. 5.1) to implement the signal generation scheme.

9. The software-based open structure of the FR and VR schemes provides a flexible way to implement these two control schemes. The parameters of the software-based blocks of these regulation schemes can be adjusted on-line to optimize their performance. This flexibility in adjusting the control options of these regulation schemes is very useful and handy for on-line experimentation.

10. When unloaded, a variable-speed DESG can be modelled as a first order system with a time varying gain factor. This gain factor, $K_{gv}$, is a function of the rotor speed, $n_r$, and the excitation frequency, $f_a$. The experimental results show that the gain factor is more sensitive to the variation in $f_a$ than to the variation in $n_r$.

11. Since the two-phase excitation control signals are applied to the DESG via its two field windings, it is necessary to identify accurately the field circuit of the machine and its effects on the dynamic performance of the machine. In this study, the use of the saliency factor, $\rho = i_{id}/i_{iq}$, is suggested as a way of comparing the field circuit of a practical DESG ($\rho < 1$) to that of an ideal DESG with identical field windings ($\rho = 1$)
REFERENCES


Appendix A

VOLTAGE GAIN FACTOR OF UNLOADED DUAL-EXCITED SYNCHRONOUS GENERATOR OPERATING AT CONSTANT SLIP

A.1 Introduction

In Reference 59, the two-axis theory has been applied to model an ideal dual-excited synchronous generator (DESG) when operating at constant slip. In the developed model, the three-phase stator winding of the DESG are replaced by two equivalent fictitious windings stationary with respect to the rotor, one being on the d-axis and the other on the q-axis. These two fictitious winding together with the two field windings on the d- and q-axis represent the model in the two-axis (d- and q-axis) frame. In this appendix, the corresponding voltage-current relationships of an unloaded DESG are used to derive the gain factor, $K_g$, which gives the relationship between the magnitude of the terminal voltage, $V_t$, to the magnitude of the two-phase excitation voltages, $V_{fi}$, of the DESG at a specified operating slip, $s_r$, such that $V_t = K_g V_{fi}$.

A.2 The Voltage Current Equations of Unloaded DESG

The differential equations of the unloaded DESG operating at a slip $s_r$ can be written in the Park's two-axis reference frame as follows [59]:

$$v_{di} = L_s \rho i_{di} - (1 - s_r) \omega_0 L_s i_{dq}$$

(A.1)

$$v_{q} = (1 - s_r) \omega_0 L_s i_{dq} + L_s \rho i_{dq}$$

(A.2)
\[ v_{fd} = R_f i_{fd} + L_{ff} \rho i_{fd} \]  
\[ v_{fq} = R_f i_{fq} + L_{ff} \rho i_{fq} \]  
(A.3)  
(A.4)

where \( v_{fd} \) and \( v_{fq} \) are the d- and q-axis components of the terminal voltage, respectively; \( v_{fd} \) and \( v_{fq} \) are the two-phase excitation voltages applied to the d- and q-axis field windings, respectively; \( i_{fd} \) and \( i_{fq} \) are the field currents produced by \( v_{fd} \) and \( v_{fq} \), respectively; \( L_a \) is the d- and q-axis magnetizing inductance between the stator phases and the field windings, \( L_{ff} \) is the self-inductance of the d- and q-axis field windings of the DESG, \( R_f \) is the resistance of each field winding, \( \omega_0 = 2\pi f_0 \) is the desired angular synchronous speed, and \( \rho \) is the differential operator \( d/dt \). Also, it is assumed that the DESG is unsaturated.

At constant slip, the d- and q-axis voltages and currents of both the rotor and the stator windings are all sinusoids of the slip frequency [59]. Thus, all these components can be represented as phasors of the form \( Y = Ye^{j(\omega_0 t + \phi)} \), where \( Y \) is the magnitude of \( Y \), \( \phi \) is the phase angle and \( j \) is the complex operator. Using this phasor representation in Eqns. (A.1) through (A.4), the following equations can be obtained:

\[ V_{fd} = js_r \omega_0 L_a I_{fd} - (1 - s_r) \omega_0 L_a I_{fq} \]  
(A.5)  
\[ V_{fq} = (1 - s_r) \omega_0 L_a I_{fd} + js_r \omega_0 L_a I_{fq} \]  
(A.6)  
\[ V_{fd} = R_f I_{fd} + js_r \omega_0 L_{ff} I_{fd} \]  
(A.7)  
\[ V_{fq} = R_f I_{fq} + js_r \omega_0 L_{ff} I_{fq} \]  
(A.8)

where \( V_{fd}, V_{fq}, I_{fd}, I_{fq}, \) and \( I_{fd} \) are the phasor representation of \( v_{fd}, v_{fq}, i_{fd}, \) and \( i_{fq} \), respectively. Furthermore, it has been shown in Reference 59 that the d- and q-axis components of the terminal voltage, \( V_{fd} \) and \( V_{fq} \), have the same magnitude, \( V \), and 90° phase shifted from each other, i.e.
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\[ |V_{u}| = |V_{q}| = V_t \quad \text{(A.9)} \]
\[ V_{q} = -jV_{u} \quad \text{(A.10)} \]

On the other hand, the excitation voltages, \(v_{fd}\) and \(v_{fq}\), which are generated and supplied to the rotor of the DESG, have the same magnitude, \(V_{fr}\), and are 90° phase shifted from each other. During steady-state conditions (i.e. at constant slip), these excitation voltages will produce the currents \(i_{fd}\) and \(i_{fq}\) which also have the same magnitude, \(I_{fr}\), and are 90° phase shifted from each other. Accordingly, these phasor relationships can be expressed as follows:

\[ |V_{fd}| = |V_{fq}| = V_{fr} \quad \text{(A.11)} \]
\[ V_{fq} = -jV_{fd} \quad \text{(A.12)} \]
\[ |I_{fd}| = |I_{fq}| = I_{fr} \quad \text{(A.13)} \]
\[ I_{fq} = -jI_{fd} \quad \text{(A.14)} \]

Substituting Eqns. (A.10), (A.12), and (A.14) into Eqns. (A.5) to (A.8), it can be shown that the performance of the unloaded DESG can be represented by a system of only two equations:

\[ V_{u} = js_{r}\omega_0 L_s I_{fd} + j(1 - s_{r})\omega_0 L_s I_{fd} = j\omega_0 L_s I_{fd} \quad \text{(A.15)} \]
\[ V_{fd} = R_{f}I_{fd} + js_{r}\omega_0 L_{fr} I_{fd} \quad \text{(A.16)} \]

Taking the magnitude of both sides of Eqns. (A.15) and (A.16), the following equations can be obtained:

\[ |V_{u}| = V_t = \omega_0 L_s I_{fr} \quad \text{(A.18)} \]
\[ |V_{fd}| = V_{fr} = \sqrt{R_{f}^2 + (s_{r}\omega_0 L_{fr})^2}I_{fr} \quad \text{(A.19)} \]

Consequently, the voltage gain factor of the unloaded DESG, \(K_{v} = \Delta V_t/\Delta V_{fr}\), can be given by:
where $X_a = \omega_L L_a$ and $X_{ff} = \omega_L L_{ff}$. Equation (A.20) relates only the magnitudes of the respective stator and rotor voltage components and, thus, is valid for both the d-q and a-b-c frames.
Appendix B

LEAST SQUARES QUADRATIC SMOOTHING FILTERS

B.1 Determination of Filter Coefficients

A Least Squares (LS) quadratic filter will fit a quadratic function $w(t) = C_0 + C_1t + C_2t^2$ to a specified set of consecutive data points of the time varying signal $w(t)$ [64]. The number of data points, $W$, used in the curve fitting process defines the window size of the filter. Odd window sizes, i.e. $W = 2M + 1$ for some integer $M$, are usually used so that the processed data can be made to correspond to a particular time instant in the window, e.g. at the center or the end of the window (Fig. B.1).

![Diagram](image)

Figure B.1: Data points in a filter window.
In the excitation system software, the smoothing property of these LS filters is exploited. This property naturally removes fast transitions in the data or rapid fluctuations that are caused by high-frequency noise. The smoothed data point $\hat{w}(t_n = 0)$ can be shown to be given by

$$\hat{w}(t_n = 0) = C_0 = \frac{(\Sigma n^4)(\Sigma w_n) - (\Sigma n^2)(\Sigma n^2 w_n)}{(\Sigma 1)(\Sigma n^4) - (\Sigma n^2)^2}$$  \hspace{1cm} (B.1)$$

where $\Sigma$ denotes the summation from $n = -M$ to $M$, i.e. Equation (B.1) can be simplified to the form:

$$\hat{w}(t_n = 0) = \sigma_M(w_{n-M} + w_{n+M}) + \sigma_{M-1}(w_{n-M+1} + w_{n+M-1}) + \ldots + \sigma_i(w_{n-i} + w_{n+i}) + \ldots + \sigma_0 w_n$$  \hspace{1cm} (B.2)$$

where $\sigma_i$, $i = 0, 1, 2, \ldots, M$, are unique coefficients of the smoothing filter which depend on the window size $W$. Equation (B.2) requires future values of $w_n$ and, thus, is only good for off-line processing. The causal form of Eqn. (B.2), i.e. one that does not require future values of $w_n$, is obtained by centering the fitted curve in the window at $t_n = M$:

$$\hat{w}(t_n = M) = \sigma_M(w_n + w_{n-2M}) + \sigma_{M-1}(w_{n-1} + w_{n-2M+1}) + \ldots + \sigma_i(w_{n-i-M} + w_{n+i-M}) + \ldots + \sigma_0 w_{n-M}$$  \hspace{1cm} (B.3)$$

The value of the coefficients $\sigma_i$, $i = 0, 1, \ldots, M$ for $W = 5, 7, 9, 11, \text{ and } 13$ ($M = 2, 3, 4, 5, \text{ and } 6$) can be calculated using Eqn (B.1) and organized into a 7 by 5 matrix $A4[I]$ as follows
Let another array Window[] contain the actual window sizes, i.e. Window[] = [5, 7, 9, 11, 13]. By careful observation of the two arrays AA[] and Window[], it can be seen that an index y (= 0, 1, 2, 3, 4) can be used to select which filter (i.e. value of \(W\)) to use. For example, if \(y = 0\), the value of \(W = \text{Window}[y = 0] = 5\) is selected. Correspondingly, the coefficients of the selected LS quadratic filter can be accessed by using the index \(y = 0\) to select the first column of the coefficient matrix, i.e. \(AA[y = 0]\). Thus, the arrangement of the coefficients in the matrix \(AA[]\) provides a filter block.

### B.2 Implementation

Figure B.2 shows the flow chart of a procedure for configuring the LS filters dynamically. In this figure, the data to be filtered is stored in a filter buffer denoted as Buffer[] and the index \(y\) will select the desired filter. After every filtering cycle data must be reorganized by shifting in a first-in first-out (FIFO) manner. This FIFO approach keeps the correct time history of the sequence of the raw data in the buffer, Buffer[].
Figure B.2: The flow chart of the procedure for configuring the LS quadratic filters dynamically.
Appendix C

PROGRAMMING THE DATA ACQUISITION 
AND SPECIALIZED PLUG-IN CARDS

C.1 Introduction

In the excitation system, the personal computers PC1, PC2, and PC3 of the excitation system (Fig. 5.1) are programmed to acquire data from input devices and send processed and formatted data to output devices efficiently, accurately and continuously. Input devices include analog-to-digital converters (ADCs), interval programmable timers, mass storage devices, keyboard or another computer. Output devices include digital-to-analog converters (DACs), video monitors, storage devices, timers or another computer. These input and output devices are collectively referred to as I/O devices or peripherals (Fig. 2.7). They have to be properly interfaced to the PCs. The I/O support is realized by the use of DAS-8, DAC-02, and PIO-12 plug-in cards.

The function of each device interface is to enable the hardware of the peripheral to be associated with the hardware of the processor section of the respective PC. A typical arrangement is for the interface components to be treated by the processor (CPU) of the PC as sections of memory, i.e., memory mapped I/O or simply I/O ports [69, 94]. In such an I/O arrangement, suitable memory addresses are reserved for the interface components so that the transfer of data is accomplished by means of sets of signals on the normal address and data buses of the computer. This is the case when plug-in cards are used. The reserved memory addresses for each interface form an I/O memory map for the respective plug-in device. In a PC, each memory map, and hence each I/O device, is usually identified by a unique reference address referred to as the base address of the device memory map.

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It therefore follows that any I/O device that is accessed for input or output of data from a PC is selected as an I/O address relative to some base address of the device. An input port accepts electrical signals as data from an output peripheral and places them on the data bus at the appropriate time for the CPU to read. An output port acquires data from the data bus and presents it to an output peripheral.

Since the operation of the modules of the excitation system software are controlled by programmable clocks, these modules should be capable of accessing the appropriate locations of each I/O device at periodic intervals. This appendix presents programming considerations for programming the three types of plug-in cards used in the excitation system, i.e. the DAS-8, DAC-02, and the PIO-12 cards.

C.2 The DAS8: An 8-Channel Analog-to-Digital Converter, Timer and Digital Interface Board

The excitation system uses analog-to-digital converters (ADCs) to track the terminal voltage $V_i$ of the DESG, the voltage error $e(t)$, and, if necessary, the slip signal $s_i(t)$. Programmable timers are used to synthesize the FM clock frequency $f_{CK}$, the reference frequency $f_{0r}$, and for measuring the frequency $f_{OUT}$ of the terminal voltage and the rotor speed $n_r$. Digital I/O signals (HIGH-LOW signals) are used for triggering real-time events and for controlling and synchronizing the processes of the excitation system. All these I/O functions are facilitated by special I/O interfaces provided by a set of standard DAS8 plug-in cards. Each DAS8 plug-in card provides the following [66, 101]:

1. An 8-channel 12-bit successive approximation ADC with sample hold feature. The ADC has a per channel full-scale input of $\pm 5 \text{ Volts}$ and a resolution of 2.44 $\text{mV}$. Typical conversion times of the ADC is 25 $\mu\text{sec}$ (35 $\mu\text{sec}$ max) resulting in data throughput rates in excess of 30 $kHz$. These rates are machine and software dependent.
2. Three separate 16-bit down counters on an 8254 timer device. One of these counters is connected to a submultiple of the systems clock (2.5 MHz) and all I/O functions of the remaining two counters are accessible to the user.

3. The DAS8 has seven (7) bits of TTL digital I/O which are organized into one output port of 4 bits and one input port of 3 bits.

C.2.1 Programming the Analog-to-Digital Converter on the DAS8 Card

Each sampling event by the ADC on the DAS8 board is a sequence of WRITE/READ operations on specific I/O memory addresses of the board. The relevant addresses for programming the ADC on the board are as follows:

<table>
<thead>
<tr>
<th>Memory Address</th>
<th>Read Operation</th>
<th>Write Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAS8-Base + 0</td>
<td>Low byte</td>
<td>Initialize 8-bit A/D conversion</td>
</tr>
<tr>
<td>DAS8-Base + 1</td>
<td>High byte</td>
<td>Initialize 12-bit A/D conversion</td>
</tr>
<tr>
<td>DAS8-Base + 2</td>
<td>Poll digital inputs including the A/D end-of-conversion (EOC) signal.</td>
<td>Select multiplexer channels (0-7) set/clear digital I/O signals</td>
</tr>
</tbody>
</table>

where DAS8-Base is the base address of the I/O memory map of the DAS-8 board. The data format of the ADC is shown below:
After a 12-bit A/D conversion, data from the ADC ports has to be read as two bytes, one of these bytes is the low byte, LoByte, and the other byte is the high byte, HiByte. The low byte has to be read first. For every sampling event, the processing of the two bytes is as follows:

\[ Data = (16 \times HiByte + LoByte/16) \times 10/4096 - 5.0 \]  

(C.1)

The procedure for programming the ADC is illustrated in the flow chart of Figure C.1 and an example of the actual programming of the ADC is in the listing of the function main() of the program AMMODULE of the excitation software reported in page 28 of Reference 100.

C.2.2 Programming the 8254 Timer on the DAS8 Board

The programmable feature of the 8254 interval timer [94, 101] allows the user to program each of its three counters separately. Each counter can be programmed for a specific task or used in multiple modes of operation. In the excitation system, the counters are used mainly as square wave generators and for pulse-width measurements (pulse-counting).

The use of the 8254 timer depends very much on the understanding of how to program the internal registers of this timer chip. For programming purposes, the three counters are located at the I/O addresses DAS8-Base + 4, DAS8-Base + 5 and DAS8-Base + 6; and the counter control register is located at DAS8-Base + 7, where DAS8-Base is the base address of the DAS8 board. Each sequence of programming the counters should begin with the specification of the mode of operation of the selected counter. This mode of operation has to be initialized by writing the appropriate control byte to the control register. After initialization, the application program can either WRITE/LOAD integer data to the counters or READ integer data from the counters.

In the case of a WRITE/LOAD operation, a processed 16-bit integer data \( D \) is first decomposed into two bytes, LoByte and HiByte, and then these bytes are loaded into the
Specify channel scan limits; then initialize first channel: \( \text{Channel} = 0 \)

Set multiplexer channel:
Write to \( ADR+2, \text{Channel} \), then initiate 12-bit A/D conversion by writing to \( ADR+1 \)

Read low and high bytes of data:
read \( Lo \) from \( ADR+0 \)
read \( Hi \) from \( ADR+1 \)

Process data and stamp it for on-line storage:
\[
\text{Data[Channel]} = \frac{(\text{Hi} \times 16 + \text{Lo} / 16)}{409.6} - 5.0
\]

\( \text{Channel} = \text{Channel} + 1 \)

Figure C.1: A flow chart showing the procedure for programming the ADC on the DAS8 board.
selected counter. The decomposition of the data $D$ should be as follows:

$$HiByte = \text{INT}(D/256)$$ \hspace{1cm} (C.2)

$$LoByte = \text{INT}(D - HiByte \times 256)$$ \hspace{1cm} (C.3)

On the other hand, the values of the data bytes, i.e. $LoByte$ and $HiByte$, read from a specified counter should be latched properly. Then, these two bytes should be combined to yield the required data as follows:

$$D = (HiByte \times 256 + LoByte)$$ \hspace{1cm} (C.4)

Functions `CounterRead()` [100, pg. 42] and `LoadCounter()` [100, pg. 43] show the details of how the counters of the 8254 timers are programmed for different tasks in the excitation system.

### C.3 Programming the DACs on the DAC-02 Analog Output Board

The DAC-02 is a two channel analog output board which consists of two separate double buffered 12-bit multiplying DACs plus interface circuitry [66, 102]. The excitation system metering scheme uses several of these DACs to generate the analog signals $v_q$, $v_n$, $V_0$, $f_{OUT}$, $n_f$, $f_f$, and $U_{AM} = -U_{REF}$ (Fig. 5.1). Since these DACs have 12-bit resolution, they can convert only integer data, $D$, in the range $0 \leq D \leq 4095$, decimal.

The basic requirement for programming the DACs on the DAC02 board is to know the I/O memory map of the board. The two DAC channels are mapped as follows:

- **Channel 0 (CH = 0)**: $DAC02$-Base + 0 is the low byte port
- **DAC02-Base + 1** is the high byte port
Channel 1 (CH = 0) \textit{DAC02-Base} + 2 is the low byte port
\textit{DAC02-Base} + 3 is the high byte port

where \textit{DAC02-Base} is the base address of the memory map of the DAC02 board.
The data format for each channel is as follows (Fig. 4.6):

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{data_format}
\caption{Data Format for Each Channel}
\end{figure}

The programming steps are illustrated in the flow chart of Figure C.2. The data \( D \) has to be decomposed into a low byte and a high byte for loading the DACs. It should be noted that the data format is such that the bit sequence is shifted 4 bits to the left. This must be taken into account in the decomposition of the data \( D \). The function \textit{SendDAC02()} of the program \textit{AMMODULE} [100, pg. 43] is an example of programming a DAC02 card.

\section*{C.4 Parallel Data Transfer Between Two Computers Using the PIO-12 Card}

Any connection between two computers, for the purpose of data transfer, must ensure that the two computers can operate together properly. This means that the connection between the two computers must be mechanically, electrically, and functionally sound. Such a connection is usually realized by the use of devices called programmable peripheral interfaces (PPI). These devices are also referred to as I/O digital interface adapters. The mechanical soundness of the connection is done by physically wiring the ports of the PPIs (Fig. 5.2). The electrical soundness is achieved by selecting a PPI with logic signals compatible with
Get the data, $D$
Select channel, $CH = 0$ or $1$

Decompose the data $D$ into a high byte, $HiByte$, and a low byte, $LoByte$ as per the DAC data format:

\[
HiByte = \text{INT}(D/16) \\
LoByte = \text{INT}(D - 16 \times HiByte) \times 16
\]

Output $LoByte$ to low byte address
Output $HiByte$ to high byte address

Write to $DAC02\_Base + 2 \times CH$
Write to $DAC02\_Base + 2 \times CH + 1$

**Figure C.2:** A flow chart showing the procedure for programming the DACs on the DAC02 board.
the PC to which the PPI will be interfaced. The functional soundness of the connection has to be done by software switching, i.e. by programming the ports of the PPI. The general setup for transfer of digital data between two computers in a parallel scheme is illustrated in Fig. C.3.

**Figure C.3:** The general setup for parallel data transfer between two computer systems using two PPIs.

### C.4.1 Choice of suitable PPI

A typical general purpose PPI will have I/O ports which can be individually programmed and used in multiple modes of operation. Four issues have to be investigated when considering the use of a certain PPI. These are:

1. How to program the adapter, i.e. to understand its I/O memory map.

2. How to configure the I/O ports of the PPI as input or output ports. This is done by writing a control byte to the control register of the PPI [94].

3. The possibility of configuring the I/O ports for unidirectional and bidirectional data transfer.
The handshaking capability of the PPI. Handshaking is the electrical/electronic software provision for the verification that a proper data transfer has occurred between two devices. Any handshaking scheme has a data-ready data-received signal scheme that ensures orderly data transfer between the machines involved.

In the excitation system, two PIO-12 plug-in cards are used to realize the data line between PC2 and PC3 in Fig.5.1. A PIO-12 card uses the 8255 PPI. This PPI provides 24-bit parallel digital I/O interface in the form of three 8-bit ports which can be programmed in software to serve as input or output ports [94].

### C.4.2 Packaging Values of Control Variables for Transmission From PC2 to PC3

In the excitation system described in this thesis, it is required to transmit values of three variables, \( J \), \( \text{sign}[s] \), and \( \text{Mode} \) from the module FMMODULE in PC3 to the module SIGGEN in PC2. The value of \( J \) specifies the jump index which corresponds to the required number of samples per cycle, \( N \), of the sinusoidal patterns used in the signal generation. The value of \( \text{sign}[s] \) specifies the phase-sequence, i.e. the direction of rotation of the field flux \( \Phi \) relative to the rotor of the DESG. The value of \( \text{Mode} \), specifies the available/unavailable status of the module FMMODULE. Also, this \( \text{Mode} \) contains the information needed to select which slip-frequency control function should be used for varying the frequency \( f_a \) of the generated excitation voltage signals, \( v_d \) and \( v_q \), i.e. Eqn. (3.7) or Eqn. (3.8). The values of these variables \( J \), \( \text{sign}[s] \) and \( \text{Mode} \), should be formatted and packaged in a suitable manner for transmission to the microcomputer PC2. On receiving this data package, the microcomputer PC2 should decode the values of the control variables from the bytes in the package.

Many formats could be devised for this purpose. In the following discussion, a byte is treated as the smallest unit of data package which can be transferred between the modules. Though the data format may depend on the scheme designed for the transfer, it suffices to aim at a minimum number of bytes that can contain all information and form a complete
package. In the excitation system software, the program FMMODULE of PC3 is programmed as the *sender/talker* and the program SIGGEN of PC2 is programmed as the *receiver/listener*. Flexible data formats for transferring data over the 24-bit data line can be established by following a five-step procedure:

1. Specify the information to be encoded or formatted. The specification may be a range of magnitude of numbers and the required resolution or a number of choices.

2. Decide on how to encode the information into bytes.

3. Determine the optimum number of bits which should be reserved for transmitting each integer number.

4. Determine the total number of bytes required for encoding all data available for transmission.

5. Pack all the data into the minimum number of bytes possible ready for transmission.

This five-step procedure has been applied to develop the data format for the 24-bit data line of the excitation system. The application is elaborated in the following.

**STEP 1:**

The specification of the three variables *J*, *sign[x]*, and *Mode* as programmed in the excitation system are as follows:

1.  
   \[J: 1 \leq J \leq 2048 \text{ and specifically } J = 1, 2, 4, \ldots, 2048.\]  
   These values are coded as \(J = 2^{(11-x)}\), where \(x = 0, 1, 2, \ldots, 11\). These values of *J* correspond to values of *N* in the range \(8 \leq N \leq 16384\), i.e. \(N = 8(2^x) = 2^{(9+x)}\), where \(x = 0, 1, 2, \ldots, 11\).
2. The variable $\text{sign}[s] = \text{sign}[f_0-f_r]$ can take three values, i.e. +1, 0 and -1.

3. The variable $\text{Mode}$ contains the information on whether the module FMMODULE is available (data = 240) and running properly or not available (data $\gg$ 240). This is a diagnostic information. Also, $\text{Mode}$ will indicate whether Eqn.(3.7) (data = 0) or Eqn. (3.8) (data = 15) is being used as the slip control function.

**STEP 2:**

1. If Eqn(3.7) is used as the control function, the value of $J$ is sent to PC2 as a code. There are 12 choices in all to fully represent $J = 2^{11-x}$, $x = 0, 1, 2, \ldots$, 11. For this case, both the programs FMMODULE and SIGGEN have lookup tables of the jump index, $\text{JMP}[x]$. The integer code $x$ points to the desired value of $J$. In the case that Eqn. (3.8) is used as the control function, $J$ has to be sent as an integer value.

2. The variable $\text{sign}[s]$ has three possible values and, thus, the data format should allow for three choices to be transmitted.

3. The variable $\text{Mode}$ has four codes to be sent, i.e. status of FMMODULE: available/unavailable; slip frequency control function: either Eqn.(3.7) or (3.8).

**STEP 3:**

1. To transmit 12 coded choices of $J$, at least four (4) bits (i.e. $2^4 = 16$) need to be reserved. A minimum of 11 bits are needed to send a value of $J$ in the range $1 \leq J \leq 2048$.

2. At least two (2) bits are needed for transmitting three (3) coded choices of $\text{sign}[s]$. 
3. To transmit the status of FMMODULE, at least two bits are needed. Another two bits are required to transmit the choice of the slip frequency control functions. Summing up the bits in all the three cases gives a total of 19 bits. This amounts to at least 3 bytes (8-bits/byte) to fully encode $J$, $\text{sign}[s]$, and mode for transmission.

**STEP 4:**

Within the three bytes, there are 24 bits. With only 19 bits needed, five (5) bits will remain unused. Thus, the manner in which the data is packed into the three bytes is the choice of the programmer. Figure C.4 shows one data format for the case when Eqn. (3.7) is used as the slip frequency control function and Fig. C.5 shows the data format used when Eqn. (3.8) is chosen.

---

**Figure C.4:** Data format corresponding to the first slip frequency control function (Eqn. 3.7).

**Figure C.5:** Data format corresponding to the second slip frequency control function (Eqn. 3.8).
STEP 5:

For the case of the data format of Fig. C.4, packaging of data is easier in that BYTE1 and BYTE2 are assigned to contain the values of J and sign[sJ] separately, and BYTE3 contains the Mode information. In PC3, these three bytes are processed for sending to PC2 as follows:

\[
\begin{align*}
\text{BYTE1} &= J & \text{(C.5)} \\
\text{BYTE2} &= \text{sign}[s_j] + 2 & \text{(C.6)} \\
\text{BYTE3} &= \text{Mode} = \text{Slip-Function-Code} + \text{STATUS} & \text{(C.7)}
\end{align*}
\]

In PC2, the required control data is recovered from the three bytes by the following arithmetic operations:

\[
\begin{align*}
J &= \text{BYTE1} & \text{(C.8)} \\
\text{sign}[s_j] &= \text{BYTE2} - 2 & \text{(C.9)} \\
\text{Slip-Function-Code} &= \text{BYTE3 AND 15} & \text{(C.10)} \\
\text{STATUS} &= \text{BYTE3 AND 240} & \text{(C.11)}
\end{align*}
\]

Equation (C.10) is for decoding information from the low nibble of BYTE3 and Eqn. (C.11) is for decoding information from the high nibble of BYTE3.

For the case of the data format of Fig. C.5, the values of J, sign[sJ] and Mode are processed in PC3 for sending purposes as follows:

\[
\begin{align*}
\text{BYTE1} &= J-\text{LoByte} & \text{(C.12)} \\
\text{BYTE2} &= J-\text{HiByte} + \left(\text{sign}[s_j] + 2\right) \times 16 & \text{(C.13)} \\
\text{BYTE3} &= \text{Mode} = \text{Slip-Function-Code} + \text{STATUS} & \text{(C.14)}
\end{align*}
\]
In PC2, \textit{BYTE3} is processed according to Eqns. (C.10) and (C.11) to recover the values of the variables \textit{Slip-Function-Code} and the \textit{STATUS}, respectively. The values of $J$ and $\text{sign}[s]$ are recovered by performing the following arithmetic operations:

\begin{align*}
J\text{-LoByte} &= \text{BYTE1} \tag{C.15} \\
J\text{-HiByte} &= \text{BYTE2} \text{ AND } 63 \tag{C.16} \\
\text{sign}[s] &= (\text{BYTE2} \text{ AND } 192) - 2 \tag{C.17} \\
J &= J\text{-HiByte} \times 256 + J\text{-LoByte} \tag{C.18}
\end{align*}

The two data formats (Fig. C.4 and C.5) clearly show that all three bytes are presented to PC2 in a "broadside" manner, i.e. in parallel. This provides a fast way to send data from PC3 to PC2. Details of the actual programming of this scheme are reported in pages 61-62 (sender, PC3) and page 89 (receiver, PC2) of Reference 100.
Appendix D

THE FLOW CHARTS OF THE EXCITATION SYSTEM SOFTWARE

D.1 Flow Charts of the Program AMMODULE [100, pp. 17 - 48]

The flow charts of the program AMMODULE are shown in Figures D.1 to D.8. The callable functions of this program are briefly described below.

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>FUNCTION DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>main():</td>
<td>The calling function of the program AMMODULE.</td>
</tr>
<tr>
<td>Set_Display():</td>
<td>Sets the screen for displaying the values of the variables and control settings at run time.</td>
</tr>
<tr>
<td>Protocol():</td>
<td>Provides hot keys for on-line control from the computer keyboard. The hot keys are single alphanumeric characters programmed to trigger certain events interactively as the AMMODULE is running continuously.</td>
</tr>
<tr>
<td>SendDAC02():</td>
<td>Sends integer data in the range 0 to 4095 to the DACs of the DAC02 card.</td>
</tr>
<tr>
<td>LoadCounter():</td>
<td>Loads a selected counter with the control codes or the reference count. Also, initializes the selected counter for event counting.</td>
</tr>
<tr>
<td>CounterRead():</td>
<td>Reads the hardware counters on the 8254 timing device.</td>
</tr>
<tr>
<td>GainSet():</td>
<td>Initializes the reference voltage settings for the manual control of the voltage regulation scheme.</td>
</tr>
<tr>
<td>Display():</td>
<td>Displays alphanumeric data on the screen for signal visualization.</td>
</tr>
</tbody>
</table>
Figure D.1: The flow chart of the main function of the program AMMODULE.
main()

Declare Local Variables and Initialize Arrays

Set the Base Addresses of DAS8 and DAC02 Cards

Open File for Data Logging

Set the Screen for Display: Set_Display()

Initialize The Amplitude of the Excitation Voltages: GainSet(), SendDAC02()

Set the Sampling Rate and The Reference Frequency ($f_0$): LoadCounter()

Initialize The Event Flags: MMF and ETF

Figure D.2: The flow chart of the initialization block.
Figure D.3: The flow chart of the keyboard handler.
MEASURE THE FREQUENCY OF THE TERMINAL VOLTAGE: $f_{out}$

Update the STATUS of the $Measure\_Frequency\_Flag$ (MFF)

Is the MFF Set?

NO

YES

Read Counter #0: CounterRead(0)

Process Data: $f_{out}$

Filter/Smooth the Frequency Data

Figure D.4: The flow chart of the frequency measurement block.
Figure D.5: The flow chart of the voltage regulator block.
Figure D.6: The flow chart of the PID algorithm block.
OUTPUT DATA

7

Output the Voltage Error $e_a$ as an analog signal, $e(t)$:
SendDAC02( )

Is the VR Loop Closed?

NO

YES

Update the Amplitude of the Excitation Signals $(U_{Adc})$: SendDAC02( )

Display Data TOSCREEN?

NO

YES

PRINT to Screen:
Display()

Save Data TODISK?

NO

YES

Save Data to DISK (FILE)

8

Figure D.7: The flow chart of the main output block.
Figure D.8: The flow chart of the main function `Protocol()` of the program AMMODULE.
D.2 Flow Charts of the Program FMMODULE [100, pp. 49 - 77]

The flow charts of the program FMMODULE are shown in Figures D.9 to D.14. The following is a brief description of the callable functions of this program.

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>FUNCTION DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>main()</td>
<td>The calling function of the program FMMODULE</td>
</tr>
<tr>
<td>Set_base()</td>
<td>Initializes the Base addresses of the plug-in cards installed in the microcomputer PC3.</td>
</tr>
<tr>
<td>Set_Display()</td>
<td>Prepares the computer screen for the display of the measurement readings and control settings.</td>
</tr>
<tr>
<td>Display_Reading()</td>
<td>Receives alphanumeric data from the main program, formats the data, and displays the information on the computer screen (for signal visualization).</td>
</tr>
<tr>
<td>Protocol()</td>
<td>Provides hot keys for the on-line control from the keyboard of PC3.</td>
</tr>
<tr>
<td>Send_Dac02()</td>
<td>Sends digital data to the 12-bit DACs on the DAC02 card.</td>
</tr>
<tr>
<td>Counter_Loader()</td>
<td>Loads any of the 16-bit counters of the 8254 timer with a precalculated integer data.</td>
</tr>
<tr>
<td>Read.Counter()</td>
<td>Reads the three 16-bit counters on the 8254 timer and initializes them for the next measurement cycle. Each counter data has a low byte and a high byte. The low byte of data is read first followed by the high byte.</td>
</tr>
<tr>
<td>LevelSetter()</td>
<td>Initializes the timing clocks. This level defines the quantization unit of time for each timer.</td>
</tr>
<tr>
<td>get_f()</td>
<td>Initializes the name of the file to be opened for data logging.</td>
</tr>
<tr>
<td>Load_data()</td>
<td>Initializes the lookup tables for the Jump-Index J and the number of samples per cycle, N. The lookup tables are duplicates of those initialized by the program SIGGEN in PC2.</td>
</tr>
</tbody>
</table>
Figure D.9: The flow chart of the main function of the program FMMODULE.
main()

Declare Local Variables and Initialize Arrays

Open File for Data Logging: get_f()

Set the Base Addresses of Plug-in Cards (DAS8, DAC02, and PIO-12 Cards): Set_base()

Set the Screen for Display of Data and Control Settings: Set_Display()

Initialize the Ports of the Data Line (three ports of the 8255A PPI)

Generate the Lookup Table of the Jump Index J: Load_data()

Set the Default Frequency $f_{CK}$ of the FM Signal: Level_Setter()

Initialize The Event-Trigger-Flag: ETF

Figure D.10: The flow chart of the initialization block.
Update the STATUS of the Event_Trigger_Flag (ETF)

Is the ETF Set?

NO

Measure Speed ($n_i$) and the Reference Frequency ($f_o$)

Filter/Smooth the Measured Data

Slip Frequency Control Function

OUTPUT Processed Data and/or parameters

YES

Figure D.11: The flow chart of the frequency regulator block.
Figure D.12: The flow chart of the slip frequency control function block.
OUTPUT DATA

Send Data to PC2?

Send Data to PC2 via the 24-bit Data line

Where Else to Send Data?

To Screen?

PRINT to Screen: Display_Reading()

As Analog Signals?

Output to Strip Chart Recorder: Send_Dac02()

Save Data TODISK?

Save Data to DISK (FILE)

Figure D.13: The flow chart of the output block.
Figure D.14: The flow chart of the keyboard handler block.
D.3 Flow Charts of the Program SIGGEN [100, pp. 78 - 95]

The flow charts of the program SIGGEN are shown in Figures D.15 to D.19. A brief description of the callable functions of this program is given below.

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>FUNCTION DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>main()</td>
<td>The calling function of the program SIGGEN.</td>
</tr>
<tr>
<td>Protocol()</td>
<td>Provides shortcut keys for dynamic control from the Keyboard. The programmed keys can be used for manual control in the case that the FMMODULE is not available (i.e. not running).</td>
</tr>
<tr>
<td>Set_base()</td>
<td>Initializes the base addresses of the required plug in cards.</td>
</tr>
<tr>
<td>Load_data()</td>
<td>Initializes the pattern and the jump index lookup tables for signal generation.</td>
</tr>
<tr>
<td>Device_check()</td>
<td>Tests the status of the FMMODULE during the initialization stage of the program SIGGEN. Function may be upgraded to provide more diagnostic features.</td>
</tr>
</tbody>
</table>
**Figure D.15:** The flow chart of the main function of the program SIGGEN.
main()

Declare Local Variables

Set the Base Addresses of Plug-in Cards (DAS8, DAC02, and PIO-12 Cards): Set_base()

Check if FMMODULE (PC3) is available and in Operation: Device_Check()

Configure the DACs for 8-bit or 12-bit Operation

Specify the default Amplitude of the Pattern Sine and Cosine Wave

Generate the Pattern and the Jump Index Lookup Tables: Load_data()

Initialize the Jump Index J and the Status of the FM Flag

Figure D.16: The flow chart of the initialization block.
Figure D.17: The flow chart of the keyboard handler.
Figure D.18: The flow chart of the two-phase signal generator.
Figure D.19: The flow chart showing the blocks of data decoders.
Appendix E

DIGITAL IMPLEMENTATION OF SOFTWARE-BASED BLOCKS OF THE EXCITATION SYSTEM

E.1 Introduction

Computer-based control has the potential to greatly increase the class of control laws that can be used [70 - 74]. For example, it is easy to use non-linear calculations to incorporate logic and to perform substantial calculations in the controllers. To take advantage of this potential, both the frequency regulation (FR) and the voltage regulation (VR) schemes of the excitation system are provided with software-based structures for implementing desirable control functions. This appendix describes the implementation of the two transfer functions of the VR control loop, i.e. the controller $G_{cv}(s)$ and the filter $G_{sv}(s)$. The flexibility in implementing these transfer functions is in the choice of their structures and in the method of the digital integration, differentiation, and filtering [93].

E.2 Implementation of the PID Control Algorithm

The proportional plus integral plus derivative (PID) controller structure has been found suitable for implementation in the excitation system. This structure is used for the VR controller transfer function, $G_{cv}(s)$. The choice of this structure is based on the fact that the PID control law can be used where complete knowledge of the controlled plant is lacking [96]. This is the case with the excitation system controlling the variable-speed dual-excited synchronous generator (DESG). The transfer function $G_{cv}(s)$ has the form (Fig. 5.7):
where $K_p$ is the proportional gain, $T_i$ is the reset time, $K_i = K_p/T_i$ is the integral gain, $T_D$ is the derivative time, $K_D = K_pT_D$ is the derivative gain, and $G_f(s)$ is the transfer function of a smoothing filter (LPF in Fig. 5.7). The digital implementation of Eqn. (E.1) is as follows.

$$G_{cy}(s) = K_p(1 + 1/T_i s + T_D s G_f(s)) = K_p + K_i s + K_D s G_f(s) \quad (E.1)$$

Equation (E.2) is a simple multiplication of $K_p$ and the sample $e_n$. Equation (E.3) uses the Simpson's integration rule which fits a parabola to three consecutive sample points. Other integration methods, e.g. the Euler's rectangular (simple accumulation) method, Trapezoidal method, and the 3/8's rule [93, 96] would equally be easily implementable. The choice of integration method will depend on the available computing power and the desired performance. In this study, the choice of Simpson's rule is based on educated intuition for realizing a near ideal integration and to show the flexibility of the excitation system. Equation (E.4) uses the simple backward difference (Euler's method) to approximate the derivative using two sample points. Naturally, this method of differentiation greatly accentuates noise and, thus, the processed values of $e_{Dn}$ will be noisy. To overcome this noise, an 11-point LS quadratic filter is used to smooth out the differentiation noise. The smoothing filter has the form:

$$e_{Pn} = K_p e_n \quad (E.2)$$

$$e_{In} = K_i (0.333333 e_n + 1.333333 e_{n-1} + 0.333333 e_{n-2}) \Delta T \quad (E.3)$$

$$e_{Dn} = K_D (e_n - e_{n-1}) / \Delta T \quad (E.4)$$

where $e_n$, $e_{n-1}$, and $e_{n-2}$ denote the error samples at time instants $t_n = n \Delta T$, $(n-1) \Delta T$, and $(n-2) \Delta T$, respectively; $e_{Pn}$, $e_{In}$, and $e_{Dn}$ are the actuation values due to the P-, I-, and D-control actions on the error information, respectively. The excitation system is designed such that the sample time $\Delta T$ can be specified as $\Delta T = 2T_0 = 2/f_0$, where $f_0$ is the desired synchronous frequency of the DESG.
\( E_{\text{Dnf}} = \sigma_5(e_{\text{Dn}+} + e_{\text{Dn}-10}) + \sigma_4(e_{\text{Dn}-1} + e_{\text{Dn}-9}) + \sigma_3(e_{\text{Dn}-2} + e_{\text{Dn}-8}) + \)
\( \sigma_2(e_{\text{Dn}-3} + e_{\text{Dn}-7}) + \sigma_1(e_{\text{Dn}-4} + e_{\text{Dn}-6}) + \sigma_0 e_{\text{Dn}-5} \)  \hspace{1cm} (E.5)

where \( E_{\text{Dnf}} \) is the smoothed update of \( e_{\text{Dn}} \), and \( \sigma_i, i = 0, 1, \ldots, 5 \) are the filter coefficients. The smoothing filter is part of the filter block described in Appendix B. The total control action \( \varphi(e_n) \) is the sum of all the three actuation values, i.e.

\[ \varphi(e_n) = e_{\text{Pn}} + e_{\text{In}} + E_{\text{Dnf}} \]  \hspace{1cm} (E.6)

In the excitation system software, the PID control law is programmed such that the P-, I-, or D-control actions can be engaged or disengaged on-line, as may be desired. Also, the parameters \( K_p, K_i \) and \( K_d \) can be varied dynamically. This type of programming has been found suitable for on-line experimentation with the excitation system [100].

**E.3 Implementation of the Filter \( G_{5v}(s) \)**

The transfer function \( G_{5v}(s) \) (Fig.5.3) is implemented using the fourth-order Runge-Kutta (RK) integration method [70]. This RK integration method is widely used for simulation of control systems especially when the system is highly nonlinear and/or discontinuous. Also, the RK method is known to perform well in variable sample rate systems of which the excitation system is one of them. The use of the RK method is intended to demonstrate another feature of the excitation system, i.e. it can be used for real-time simulation and control by using the popular techniques used to solve differential equations in off-line. Since the excitation system uses fast and affordable computers, such a use is achievable. After all, the main difference between off-line simulation and real-time simulation is only in the way the test data is obtained. Normally, data is calculated in the case of off-line simulation and data is acquired in the case of real-time simulation.
The filter transfer function has been defined earlier (Eqn. (4.2)) to be of the form:

\[ G_{5v}(s) = \frac{K_{5v}}{s + \tau_{5v}} = b_0(s + a_0) \] (E.7)

where \( a_0 = 1/\tau_{5v} \) and \( b_0 = K_{5v}/\tau_{5v} \). Figure E.2 shows the direct implementation scheme of the filter. This figure can also be described in terms of the state \( V_2 \), the input \( V_1 \) and output \( V_t \) as follows.

\[
\begin{align*}
\dot{V}_2 &= V_1 - a_0 V_2 = F(V_2, t) \quad \text{(E.8)} \\
V_t &= b_0 V_2 \quad \text{(E.9)}
\end{align*}
\]

![Implementation diagram for \( G_{5v}(s) \).](image)

Equation (E.8) defines the function \( F(V_2, t) \) required for implementing the RK integration scheme. Let \( V_1 = V_{10} \) and \( V_2 = V_{20} \) at \( t_n = t_0 \). Using these initial conditions, the RK integration steps to generate the next update of \( V_t \) are as follows [70]:

\[
\begin{align*}
K_1 &= F(V_{20}, t_o) \Delta T = V_{10} \Delta T - a_0 V_{20} \Delta T \quad \text{(E.10)} \\
K_2 &= F(V_{20} + K_1/2, t_0 + \Delta T/2) \Delta T = V_{10} \Delta T - a_0 (V_{20} + K_1/2) \Delta T \quad \text{(E.11)}
\end{align*}
\]
\[ K_3 = F(V_{20} + K_2/2, t_0 + \Delta T/2)\Delta T = V_{10}\Delta T - a_0\{V_{20} + K_2/2\}\Delta T \quad (E.12) \]
\[ K_4 = F(V_{20} + K_3, t_0 + \Delta T)\Delta T = V_{10}\Delta T - a_0\{V_{20} + K_3\}\Delta T \quad (E.13) \]
\[ V_{21} = V_{20} + (K_1 + 2K_2 + 2K_3 + K_4)/6 \quad (E.14) \]
\[ V_{t1} = b_0 V_{21} \quad (E.15) \]
\[ t_1 = t_0 + \Delta T \quad (E.16) \]

It should be noted that Eqn.(E.16) is necessary only for off-line simulations. In real-time simulations or control, the time is automatically incremented by the driving clock and new samples will be acquired in real-time. Equations (E.10) to (E.13) can be reorganized for digital programming as follows.

\[ K_1 = \chi - V_{20}h_1 \quad (E.17) \]
\[ K_2 = \chi - \{2V_{20} + K_1\}h_2 \quad (E.18) \]
\[ K_3 = \chi - \{2V_{20} + K_2\}h_2 \quad (E.19) \]
\[ K_4 = \chi - \{V_{20} + K_3\}h_1 \quad (E.20) \]

where \( \chi = V_{10}\Delta T, h_1 = a_0\Delta T, h_2 = h_1/2 \). The values of \( h_1 \) and \( h_2 \) may be updated only when either \( a_0, \Delta T \) or both are changed. In addition, the initial condition \( (V_{20}, t_0) \) has to be updated for every clock tick. For the above algorithm, the initial value \( V_{20} \) should be updated such that \( V_{20} \leftarrow V_{21} \) before the integration procedure is repeated for the next clock tick.