DESIGN OF THE M.3 COMPUTER

A Thesis
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in Partial Fulfilment of the Requirements
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by
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Abstract

A solid state digital computer, the M.3, has been designed, constructed and partially tested. The computer logic is based on the M.2 computer constructed by A. D. Booth in 1956, but with fundamental changes to the logic associated with the store and the arithmetic section.

The M.3 is a serial, fixed-point computer which uses 32 bit words and two address instructions. The 150 Kc/s clock frequency permits addition or subtraction in 250 microseconds. Division requires 8000 microseconds and multiplication requires 250 to 8000 microseconds. A drum store provides 8192 word storage with an average random access time of 8500 microseconds.

Peripheral equipment consists of an 80 character per second tape reader and a 60 character per second tape punch or a 10 character per second typewriter.
Plate I

Front View of M.3 Computer
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1. HISTORY OF DIGITAL COMPUTERS

The history of computing machines began when man learned to count. The familiar decimal system originated with the use of the fingers (digits) for simple calculations. Later, notched sticks, stones and knotted strings were used to represent quantities in calculations involving larger numbers.

The earliest known mechanical device used for arithmetic calculations is the Abacus. This instrument, which consists of moveable beads strung within a wooden frame, was developed in the Far East about 600 B.C. Addition, subtraction, multiplication and division can be performed with the Abacus, but the earliest users of the Abacus probably used it only for addition and subtraction.

The next step in the development of the automatic calculating machine came in 1642 when a crude, stylus operated, numerical wheel calculator was devised by Pascal. Numbers were represented by the visible figures on a set of rotatable wheels, each wheel being numbered from 0 to 9. Numbers could be added to or subtracted from the instrument by rotation of the wheels. Carry over to the wheel on the left was controlled by a carry mechanism. Later, this calculator was modified by Leibnitz to enable the performance of multiplication and division. However, both modified and unmodified version were unreliable. The early calculators of Pascal and Leibnitz were greatly improved during the late seventeenth century by several people. Morland, Stanhope, and later Troncet, made outstanding improvements to the manually operated calculator. Further improvements, including the addition of an electric drive, transformed the early calculators into the modern desk calculator.

In 1812 Charles Babbage proposed the idea of building a machine which would be capable of performing accurately the simple calculations
required for generating tables of functions. Support for a small model was obtained from the Royal Society and the model was completed in 1822. The instrument was found to perform very well and the government of the day advanced support for the design and construction of a much larger model. This model, the "Difference Engine" was designed to work to 20 decimal places using sixth order differences. Throughout the construction of the machine, the lack of precision lathes and cutting tools caused many engineering difficulties. Finally, this plus the loss of financial support caused the project to be abandoned entirely.

In 1833 Babbage proposed to build a calculating machine which would perform all the arithmetic operations of a universal computer. The computer, the "Analytic Engine" was to have storage facilities for one thousand, fifty digit numbers. To speed up addition, Babbage devised a mechanical method of simultaneous operation of all carries (anticipated carry). This, for example, would allow the machine to automatically zero all 9's when 1 had been added to 899999 and to add 1 to the 8. This technique has been the basis of the adder system of several modern machines.

The Analytic Engine contained many other features which make it the true ancestor of today's computing systems. In the design of his machine, Babbage originated all the logical elements which are used in today's computers. It consisted of two main parts, the mill and the store. The mill was the equivalent of today's arithmetic unit and the store had the same purpose as the memory of modern computers.

The use of punched cards as a computer input was first suggested by Babbage. The card used with the Analytic Engine was a slightly modified version of the punched card which had been in use for many years to control the weaving of complex designs on the Jacquard loom.
The results of calculations were to be printed by a mechanism which would set up a block of type representing the results, check the correctness of this block, and then print it. The faculty of checking the printed output was one advantage which this mechanism had over almost all subsequent models.

The machine was designed in such a way that it could make a choice between two or more alternative operations. This is the so-called "conditional transfer" or "branch" instruction which is present in the structures of all modern computers and is partially responsible for their usefulness.

Thus Babbage conceived the idea of the first universal calculating machine. Prior to his death in 1871, Babbage prepared many detailed drawings from which the analytic engine could have been constructed, had precision tools been available. His son, Major H. P. Babbage, constructed a portion of the mill and print out mechanism between 1880 and 1910. This machine was able to calculate and print out the multiples of \( \pi \) to 20 decimal places as was shown at one demonstration. It has since been placed on display at the South Kensington Science Museum.

The first data sorting system was developed in 1889 by Herman Hollerith to handle information gathered in the American census. As an input to his mechanism, Hollerith used a punched card similar to that suggested by Babbage. This mechanism became the basis of the accounting machines which the predecessors of International Business Machines began to manufacture in 1903.

It was not until a century after Babbage conceived the Analytic Engine that the next universal computer was designed. In 1937, Professor Howard Aiken of Harvard University, assisted by International Business Machines, designed and constructed the Harvard Mark I Automatic Sequence
Controlled Calculator. This computer, which was completed in 1944, used similar logic to that of the Analytic Engine. The mechanical construction was quite different though, as the machine used electromechanical elements instead of the mechanical elements of Babbage's time. The store of the machine was not entirely divorced from the arithmetic unit since seventy-two of the storage registers also acted as adders or subtractors. In order to obtain faster addition rates, the "anticipated carry" system designed by Babbage was used. Sixty other storage registers were also available, but as they were manually controlled, they could be used only for storing constants.

The Harvard Mark I was designed with a central multiplier and divider, plus a number of special units to generate functions such as \( \log x, 10^x, \) and \( \sin x \). Input to the computer was by punched card or by automatic typewriter. There was also an automatic sequence control unit which directed operations from punched paper tape.

The Mark I is still in operation and has been used for many useful tasks over the past nineteen years. Its speed is many times slower than the speed of the most recent computers, but in 1944 it was able to do tasks for which it was designed at a rate many times faster, and with far greater reliability than any alternative method.

An engineer with Bell Telephone Laboratories, G. R. Stibitz, was the first person to design a computing device which used electromagnetic instead of electromechanical operation. This computer, known as the "Complex Number Computer" required some assistance from the human operator and was classed as semi-automatic. Composed entirely of telephone relays, and using teletype equipment for input and output, the computer was capable of performing multiplication or division accurately in a few seconds.

During the war, Bell produced three special purpose relay computers which calculated ballistics' tables to be used in gun sight calibra-
tion and with fire control equipment. Following the war, Bell received a
government contract for the development and construction of two relay
operated general purpose digital computers. The new computers were known
as the Bell Model V Computers. Many new computer design concepts were
apparent in their construction. All arithmetic operations were performed
on floating decimal point numbers. With this notation, the number 594
would be represented by 0.5940000 multiplied by 1000.000,000,000,000.0.
The biquinary system, similar to that used on the Abacus, was used to
represent each decimal number on the relays. Using this code, 7 relays
are needed to represent each decimal number. Assuming an open relay is
represented by 0 and a closed relay by 1, the relay configurations are
as follows:

<table>
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<tr>
<th>DECIMAL DIGIT</th>
<th>RELAYS</th>
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<tbody>
<tr>
<td>00</td>
<td>5</td>
</tr>
<tr>
<td>0 1</td>
<td>0</td>
</tr>
<tr>
<td>1 0</td>
<td>0</td>
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<tr>
<td>2 0</td>
<td>0</td>
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<td>3 0</td>
<td>0</td>
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<td>4 0</td>
<td>0</td>
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<tr>
<td>5 0</td>
<td>0</td>
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<td>6 0</td>
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<td>7 0</td>
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<td>8 0</td>
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<td>9 0</td>
<td>0</td>
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<td>0 1</td>
<td>0</td>
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<td>1 0</td>
<td>0</td>
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<td>2 0</td>
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<td>7 0</td>
<td>0</td>
</tr>
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<td>8 0</td>
<td>0</td>
</tr>
<tr>
<td>9 0</td>
<td>0</td>
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</table>

The machine was very accurate and never proceeded to a new
calculation until the previous one had been checked. Any mistake made
by the computer caused the machine to stop and turn on a lamp, indicat-
ing the trouble spot.

This computer pair has been in operation since 1947 and, due
to its self checking and to the reliability of the telephone relay, the
machines have accomplished a great deal of work with a minimum of errors
and maintenance.
Another large relay computer, the Harvard Mark II, was built by the Harvard University group. Construction was started in 1945 and in 1947 the machine was in operation. The Mark II used floating point numbers similar to those used in the Bell Model V. The use of special high speed relays plus the elimination of the self checking property made the operating speed of this machine considerably faster than that of the Bell computers.

With relay calculators, it was difficult to perform more than fifty additions per second due to the time required to switch a relay. This switching time was dependent upon the inertia of a moveable portion of the relay and also upon the inductance of the coil. By using electronic tubes and diodes as logical elements in a computer, much faster switching times could be obtained.

The possibility of constructing a computer using electronic components as logical elements was first investigated by the Moore School of Electrical Engineering. A computer known as the "ENIAC" (Electronic Numerical Integrator and Calculator) was designed by J.P.Eckert and J.W. Mauchly as a result of this investigation. The computer design was completed in 1945 and the "ENIAC" was working in 1946. Although the machine as was initially designed had limited applications, logical changes during construction caused the final model to be quite versatile. The use of electronic components allowed the machine to operate at a previously impossible speed of 5000 additions per second. The "ENIAC" used a logical structure quite similar to the relay machines of that day.

Modern computers, although performing the same tasks as early machines, are quite different. Calculating speed has been increased by several hundred times, yet physical size and power consumption have been greatly reduced.
Semiconductor developments and new memory devices are primarily responsible for this change. Semiconductor circuits switch many times faster than electronic tube circuits, yet require much less power and virtually no maintenance. They are also compact and require no forced ventilation. Recently developed memory devices using magnetic storage provide fast access time yet require no retaining power and very little recording or emitting power. High speed semiconductor memories are also being developed.

New mathematical techniques have simplified the logic required to perform arithmetic operations within a computer. The use of number systems with a base other than ten has also simplified computer logic.

The following chapters describe how a moderate speed, modern computing system has been developed.
2. THE M.2 COMPUTER

In 1956 a general purpose digital computer, the "M.2", was designed at Birbeck College, University of London by A. D. Booth. The logical operations required for addition, subtraction, multiplication and division are performed in the M.2 by hot-tube electronic circuits. The M.2 logic derives from a series of computers: the "ARC", a stored program relay computer; the "SEC", an electronic computer capable of addition and subtraction with a magnetic drum memory; the "APEXC", a modified SEC with double speed and an automatic multiplier and the "MAC", the prototype of the M.2 which was similar in design to the "APEXC" but contained an automatic divider.

The M.2 is a binary computer working with 32 bit numbers confined to the range $-1 < x < 1$ (a bit is a binary digit). The first digit of a number represents the sign, being 0 for a positive number and 1 for a negative number. Negative numbers are expressed in the complementary form mod. 2. Thus $+\frac{1}{2}$ appears as 0.0100,0000,0000,0000,0000,0000,0000,0000 and $-\frac{1}{2}$ appears as 1.1100,0000,0000,0000,0000,0000,0000,0000 (i.e. $2^{-\frac{1}{2}}$).

Instructions are also represented by 32 bit numbers. To ease program optimization, "two address code" instructions are used. A typical instruction is: Add the number in location "X" into the accumulator and obtain the next instruction from location "Y". The first 10 bits of the instruction contain the "X" address, the next 10 the "Y" address, the next 5 the order to be performed and the next 6 the input to the control counter. The last bit, the "vector record" instruction, when set to unity causes recording of the same number in all word locations of one track.

The M.2 is composed of three main units; the memory which is responsible for storing both instructions and data until required, the
control which is capable of receiving and executing instructions stored in the memory and the arithmetic unit which must on command from the control operate on stored data to produce the combinations of ordinary arithmetic.

2.1 The Memory

The memory of the M.2 consists of a machined aluminum cylinder which is rotated at 3400 R.P.M. by a small induction motor. The surface of the cylinder is coated with a thin homogeneous layer of ferrous oxide and plastic. Thirty-two recording heads are spaced evenly along the drum surface, each on an individual track. The spacing between the drum surface and the head is approximately .00025 inch.

Two clock tracks are engraved on one end of the drum to provide an address for each bit of stored information on the drum. The first track is the "word marker track". It has thirty one single groove markers and one double groove marker spaced evenly around the drum. Electrical impulses induced in a small reading head by this track indicate the beginning of each word. The impulses are amplified and the resulting pulses are counted by a 5 stage binary counter. A special gating network causes the double pulse to set the counter to zero. Successive word markers each advance the counter by one. The binary number contained in the counter while the reading head is between any pair of word markers is known as the "word location" of that particular word.

To complete the location of any particular word on the drum, the recording head used to record information must also be specified. As there are 32 different heads, a five bit "track location" number must accompany the "word location" number. This results in the ten bit "memory location" address used by the M.2.
The second clock track is known as the "bit marker track". This track has 32 slots engraved between each pair of markers on the word marker track. An unmarked recovery space equivalent in length to 4 bit spaces is left at the beginning and end of each set of slots.

The M.2 is a serial machine in which data transferred between the memory and the rest of the computer become available one bit at a time starting with the least significant bit. To transfer information to a memory location, the control addresses the "I" track location and a comparison is made between the "I" word location (stored in the control) and the word location shown by the word marker counter. When these are equal (coincidence), the memory emits 32 bit markers.

If the least significant bit of the word being recorded is a "1", the first bit marker pulse is gated to cause a four microsecond current pulse to pass in one direction through the recording head winding. The resulting magnetic field magnetizes a small spot on the drum surface.

If a bit in the word is a "0", the corresponding bit marker produces a similar current pulse which passes through the recording head winding in the opposite direction. This produces a magnetized spot with opposite polarity to the spot recorded by a "1". The remaining bits in the word are recorded on the drum in a similar manner by their corresponding bit marker pulses.

The memory generates an "operation complete pulse" (op. comp. pulse) after emission of the thirty second bit marker pulse. This indicates to the control and arithmetic unit the completion of any operation in which information is transferred to or from the memory.

Information recorded on the drum induces a small voltage in the recording head as each magnetized element of the drum surface rotates under the recording head. If a "1" has been recorded in a particular bit location, the voltage induced in the head resembles a single cycle of a
sine wave. If a "0" was recorded, the induced voltage resembles a single cycle of a negative sine wave. To determine the identity of a bit, the recording head output is amplified and the signal obtained is sampled during the centre \( \frac{1}{2} \) of the sine wave corresponding to each bit. If the amplifier output during this time is going negative, the sampling circuit recognizes the bit as a "l". If the output is going positive, it is recognized as a "0".

Access time to this type of memory is inherently slow as the drum must rotate to the proper word location before information can be recorded or received from the memory.

Information no longer needed can be erased from the memory by recording new information over the old. If recorded information is not removed in this manner, it will be retained for many years with negligible deterioration.

2.2 The Control

The M.2 control consists of three main sections: the control register which stores an instruction until it is executed, the decoder which interprets the instruction in the control register, and the control counter, which has been incorporated into the control register to control the number of basic operations performed in an instruction. Operation of the computer is controlled by the "Control Flip Flop" (C.F.F.); if in the "l" state the computer must execute the instruction stored in the control register. If it is in the zero state, the memory must shift a new instruction into the control register. The computer must execute three basic instruction types; instructions which shift a single word to or from the memory, instructions which require more than one basic operation and branch instructions.

With instructions requiring transfer of information between memory and arithmetic unit, the C.F.F. change to the "l" state shifts the "X"
Fig. 2.1
M.2 Control Schematic
track location from control register stages 1 to 5 (C.R. 1-5) through the "and" gate, g_4, to the track selector and permits the decoder to issue the order stored in C.R. 21-25 to the arithmetic unit (Figure 2.1). When coincidence occurs between the available word location and the "X" word location (C.R. 6-10), 32 shift pulses from the memory cause the execution of the order. Following the thirty-second shift pulse, the op. comp. pulse generated by the memory passes through the arithmetic unit to zero the C.F.F., shift the "Y" track location (C.R. 11-15) through g_5 to the track selector and shift the "Y" word location (C.R. 16-20) through g_6 into the C.R. 6-10 locations. Zeroing of the C.F.F. instructs the memory to read and opens g_3 to allow the 32 shift pulses emitted by the memory on coincidence to shift the next instruction into the control register. Following the thirty-second pulse, the op. comp. pulse generated by the memory returns the C.F.F. to the "1" state ready to execute the next instruction.

With instructions requiring the completion of more than one basic operation, the C.F.F. change to the "1" state shifts the "X" track location into the track selector and permits the decoder to emit an instruction. As this type of instruction does not require coincidence with a word location, operation starts immediately. Each basic operation performed passes a pulse through g_7 to the control counter (C6). When the required number of operations have been performed, the most significant stage of C6, C.R.26 generates an "operation complete" pulse to zero the C.F.F., shift the "Y" track location into the track selector and shift the "Y" word location into C.R. 6-10.

When coincidence occurs, the zeroed C.F.F. shifts a new instruction into the control register in a manner similar to that described in the previous example. The op. comp. pulse following the shift resets the
C.F.F. to unity, ready to execute the new instruction. With branch instructions, the next instruction shifted into the control register is determined by the sign of a number stored in the arithmetic unit. When the C.F.F. switches to the "1" state, the "X" track location is set into the track selector by $g_4$ and a gating pulse from the decoder tests the sign of the number in question. If the sign bit is a "0" indicating a positive number, the arithmetic unit emits an operation complete pulse which zeros the C.F.F. and opens $g_5$ and $g_6$ to shift the next instruction to the control register from the "X" memory location. However, if the sign bit is a "1", the arithmetic unit emits a pulse on the branch $n < 0$ line which zeros the C.F.F. but does not open $g_5$ or $g_6$. This results in the new instruction being shifted to the control register from the "X" memory location. Following the instruction shift, the operation complete pulse generated by the memory will set the C.F.F. to a "1" ready to execute the new instruction.

2.3 The Arithmetic Unit

Operation of the arithmetic unit is controlled by the control unit. When instructed, the arithmetic unit will perform right shifts, left shifts, additions, subtractions, multiplications and divisions. Provision is made for the emission of an operation complete pulse on completion of an operation, or alternatively, for generation of basic operation complete pulses for the control counter. The arithmetic unit contains two electronic storage registers, the accumulator and the shift register. Both can store a 32 bit word, and have the property that stored digit patterns can be shifted to the right only.

To explain the operation of the arithmetic unit, each order will be considered separately.
2.3.1 Right Shift

In the right shift, the least significant digits of the number "A" stored in the accumulator are shifted into the most significant end of the shift register. The sign digit of "A" is propagated to fill the most significant end of the accumulator. The least significant digits of the number stored in the shift register are lost.

![Diagram of Right Shift Logic]

**Fig. 2.2**
Right Shift Logic

The logical circuits required to perform the right shift are shown in Figure 2.2. The control counter (C6) is advanced by each right shift, allowing control of the total number of shifts. An n-bit right shift is equivalent to dividing "A" by 2^n.

2.3.2 Left Shift

Left shift is similar to the right shift, but the contents of the last register stage are shifted back to the first stage of the accumulator. To obtain a left shift, the decoder activates both right and left shift order lines shown on Figure 2.3.

![Diagram of Left Shift Logic]

**Fig. 2.3**
Left Shift Logic
An n bit left shift is obtained by shifting the stored number to the right 64-n digits. The number of shifts performed is controlled by the G6.

2.3.3 Addition

Addition is achieved by adding the contents of memory location "X" to a number stored in the accumulator. The rules of addition are:

If: Incident digit = carry digit (coincidence)
Send A32 to Al
Leave carry digit unchanged

If: Incident digit ≠ carry digit (anti coincidence)
Send the inverse of A32 to Al
Send A32 to the carry store

The carry digit must initially be set to zero. Here A_n represents the contents of the nth stage of the accumulator.

As addition requires shifting data from the memory, the op. comp. pulse generated by the memory following emission of the thirty-second pulse instructs the control that the addition is finished.
2.3.4 Subtraction

Subtraction is performed in the M.2 by adding the complementary form mod. 2 of the incoming number from memory location "X" to the number stored in the accumulator. To obtain the true complement of a binary number, all "1"s in the number are changed to "0"s; all "0"s are changed to "1"s and "1" is added to the least significant bit of the number. The effect of inverting the incoming digits from the memory is produced by two "and" gates which invert the output of the coincidence sensor. The addition of one to the least significant digit is obtained by setting the carry store to unity prior to the subtraction.

The rules of subtraction for this scheme are:

If: Incident digit = carry digit (coincidence)
    Send the inverse of A32 to A1
    Send A32 to the carry store

If: Incident digit ≠ carry digit (anti coincidence)
    Send A32 to A1
    Leave carry digit unchanged.

The carry digit must initially be set to unity. The op. comp. pulse for this operation is generated by the memory following emission of the thirty-second shift pulse.

2.3.5 Multiplication

A multiplication order in the M.2 multiplies the number stored in the shift register by the number recorded in all word locations of the "X" track in the memory. The product is shown in the accumulator. The multiplier, shown schematically in Figure 2.5, follows the rules:

For basic operations 1 to 31:

If: R32 = R33, shift accumulator and register one place right.
If: \( R32 = "1", R33 = "0" \), subtract the number stored on the memory from the accumulator, then shift accumulator and register one place right.

If: \( R32 = "0", R33 = "1" \), add the number stored on the memory to the accumulator, then shift accumulator and register one place right.

For operation 32:

Exactly the same as above except that the shift is deleted.

Prior to multiplication, \( R33 \) must be set to zero. \( Rn \) indicates the contents of the \( n \)th stage of the shift register.

The multiplication op. comp. pulse is generated by the control counter. Following the thirty-first basic operation, the control counter switches off \( g_4 \) in Figure 2.5, preventing right shift after the thirty-second operation.

Fig. 2.5

M.2 Multiplier Schematic
2.3.6 Division

For division, the dividend is placed in the accumulator and the divisor is recorded on all word locations of one track in the memory. The divisor must be negative for the operation. The divider, shown schematically in Figure 2.6 follows the rules:

Basic operations 1 to 31:
- Send Al to R1
- Store Al in F
- Clear A33
- Shift accumulator and register one stage left.

If \( F = "1" \) Subtract the divisor from the accumulator.
If \( F = "0" \) Add the divisor to the accumulator.

The division op. comp. pulse is generated by the control counter following the thirty-first basic operation. \( 1 + 2^{-31} \) must be added to the resulting quotient which is stored in the shift register to obtain the correct result.

![Diagram of the divider](image)

**Fig. 2.6**

M.2 Divider Schematic
3. REASONS FOR TRANSISTORIZING THE M.2

When the M.2 was designed in 1956, electronic tubes were the best logic element available. Unfortunately, tubes have several disadvantages; they are expensive, they deteriorate with age and they dissipate considerable power as heat. To keep M.2 tube requirements to a minimum, a simplified arithmetic unit is used which replaces a 32 stage immediate access register required for multiplication and division by a system of recording a required number on all word locations of one track.

This reduces cost, power consumption and heat dissipation, but has several disadvantages. Recording a number on all word locations of a track requires one drum revolution, thirty-two times longer than the time required to shift information into an electronic shift register. Programming is also more difficult as the M.2 divider assumes that the divisor, stored on the track of the memory, is negative.

Tube deterioration is also a problem with the M.2 as a twenty minute maintenance period is required each week to prevent machine errors due to changing tube characteristics.

The low priced, fast, switching transistors available today allow many of the M.2 problems to be overcome. The additional cost of a thirty-two stage immediate access register is small. Power supply requirements, heat dissipation and ventilation requirements are reduced. Very little maintenance is required due to the long term stability of transistors. The small size of transistors and the reduced ventilation space allow the transistorized version of the M.2 to occupy a much smaller volume than the original.

3.1 Modifications to the M.2 Structure

The first modification to the M.2 is the addition of an immediate access "cycle" register to the arithmetic unit. Prior to multiplication
or division, the multiplier or divisor is shifted into this register. Then during the arithmetic operation, each time the stored number is required, a group of thirty-two shift pulses are used to cycle the register and to shift data from the thirty-second stage of the register to the arithmetic unit.

The second modification to the M.2 is the replacement of the divider. The original divider, with no direct method to determine the sign of the divisor, assumes it to be negative. However, in the modified M.2 the sign of the divisor can be determined by sampling the most significant stage of the cycle register. This permits the use of the non-restoring process of division which places no restrictions on the signs of numbers involved.

---

**Fig. 3.1**
Non-Restoring Divider Logic
Assuming that the divisor \((C)\) is stored in the cycle register, the dividend \((d)\) appears in the accumulator and the quotient \((b)\) appears in the shift register; this process is as follows:

Operations 1 to 31:
- If \(Cl = Al\)
  - Add \(2^{-31}\) to \((b)\)
  - left shift accumulator and register one place.
  - Subtract \(C\) from \(A\).
- If \(Cl \neq Al\)
  - Add 0 to \((b)\)
  - left shift accumulator and register one place.
  - Add \(C\) to \(A\).

Operation 32:
- Add \(1 + 2^{-31}\) to \((b)\).

In this scheme, \(A_n\) and \(C_n\) represent the \(n\)th digit of \(A\) and \(C\). The logical schematic of this divider is shown in Figure 3.1.

The 1024 word memory capacity of the M.2 is too small to handle a long program in a single run. To provide memory capacity for longer programs as well as space for useful subroutines, a memory with a 8192 word capacity is used in the new computer. The new memory contains 64 word locations per revolution and has 128 tracks. As speed of rotation of the new drum and the M.2 drum are equal, the change in words per revolution increases the basic bit rate from 75 Kc/s to 150 Kc/s. This increases the calculation rate of the new machine by a factor of two over the M.2. However, access time to a memory location chosen at random remains the same. Thus optimized programming is still essential.

The increased number of tracks in the memory necessitates a new method of track selection. As 6 bits of the 10 bit memory location address are used by the word location, only 4 bits remain to specify a track. To avoid increasing the 32 bit word length to allow direct address-
ing of any track, the 128 tracks are divided into 16 blocks, each containing 8 heads. The heads in the first block can be addressed by track numbers from 0 to 7. In the remaining fifteen blocks, to address a particular head, a block must first be switched on by a block switch order. Then heads in the particular block can be addressed by track location numbers from 8 to 15. Once a block is switched on, it will remain on until a different block is addressed by a block switch instruction.

As this transistorized computer uses a similar logical structure in control and arithmetic units to the M.2 logic, it will be referred to in the following chapters as the M.3.
4. DESIGN OF LOGICAL CIRCUITS

A digital computer is composed of electronic circuits interconnected to produce an operational unit. Only a few basic circuit types known as logical elements or logical circuits are required for a computer, though these may be modified to meet special input or output requirements. The overall layout of interconnected logical elements is known as the logic of the computer.

In this chapter, the operating characteristics, design and use of the different logical circuits of the M.3 are described. Variations from the basic circuits are also described and their purpose is shown.

4.1 Design Technique

The primary requirements in logical circuit design are reliability and acceptable speed. Secondary requirements of the circuit are simplicity, low cost and low power consumption. To ensure reliable circuit operation, switching circuits are designed using a "worst case" design procedure. Worst case design implies that a circuit will work when all supply voltages and active and passive components are simultaneously at those extremes of their tolerance limits that will tend most to make the circuit inoperative. Component values and voltage levels are assumed to have ±10% variation. The transistor current gain, which is rated from 60 to 300 by the manufacturer is assumed to be a minimum of 50. Circuits are designed to operate within the ambient temperature range from 40°F to 130°F assuming the greatest semiconductor variations with temperature.

Texas Instruments 2N1306(N.P.N.) and 2N1307(P.N.P.) germanium switching transistors are used in all logical circuits. These transistors, which have a minimum common-base alpha-cutoff frequency of 10 megacycles, allow switching times in the .1 to .2 microsecond range.
The basic building block of many of the logical circuits used with the M.3 is shown in Figure 4.1

![Basic Building Block](image_url)

This circuit design allows the 2N1307 transistor only two stable states, either conducting or non-conducting. When conducting, sufficient current is drawn from the base to ensure that the transistor remains saturated under normal loading. In this state, the emitter to collector voltage drop ($V_{CE}$) varies from .1 to .2 volts depending upon ambient temperature and transistor characteristics. Saturated transistor circuits use fewer components than unsaturated circuits and produce a stable output voltage for a variable load. When switching a transistor off, a .1 microsecond delay is observed which is partially due to the effects of saturation. However, this delay is not large enough to cause difficulty.

In the non-conducting state, sufficient current is passed through $R_3$ from the +1.5 volt supply to ensure that the base voltage is positive with respect to the emitter voltage. In this "cut off" state, the collector voltage is clamped to a level slightly negative of -6 volts by a IN67A clamping diode. The clamping diode causes faster switching speeds
and produces a stable output voltage for a varying load.

A speed up capacitor $C_s$ is placed in parallel with $R_2$ to obtain the fast switching speeds required. The value of $C_s$ varies from 50 pf to 300 pf and is chosen empirically in each circuit to produce maximum operating speed.

4.2 The Basic Flip-Flop

In a digital computer a method must be available to store a digit while another part of the circuit examines it. This logical operation of remembering is performed by the flip-flop, a two element active circuit which has two stable states. A circuit diagram of the basic flip-flop used with the M.3 is shown in Figure 4.2. This circuit is assumed to be in state "1" when $T_1$ is conducting and $T_2$ is non-conducting (cut off). In this state, output $A$ is -6.3v due to the clamping diode and output $B$ is approximately -.2v due to the voltage drop across the saturated transistor. The flip-flop is assumed to be in the "0" state when $T_1$ is cut off and $T_2$ is conducting. In this case the output voltage levels will be reversed.

To be useful, a method must be available to set the flip-flop to either "1" or "0". The diode gating network shown in Figure 4.3 is used to perform this task. To shift a "1" into the flip-flop, $C$ is set to 0 volts, $D$ is set to -6 volts and a 6 volt positive going pulse is applied to $F_1$ and $F_2$ simultaneously. As $D_1$ is initially reverse biased by 6 volts, the pulse has insufficient amplitude to cause current to pass to the base of $T_1$. However, initially $D_2$ has only enough reverse bias to prevent current flow.

The 6 volt pulse causes current flow through $D_2$ to reverse bias the base to emitter junction of $T_2$. This cuts off $T_2$ which in turn causes $T_1$ to conduct. Thus the flip-flop is set to the "1" state.

To set the flip-flop to the "0" state, the voltage levels applied to $C$ and $D$ are reversed and a positive going 6 volt pulse is applied to $F_1$ and $F_2$. 
Fig. 4.2
The Basic Flip Flop

Fig. 4.3
Basic Flip Flop Showing Input Gating

(a) Single Shift Register Stage  
(b) Stage Shift Register

Fig. 4.4
Symbolic Flip Flop Representation

Fig. 4.5
Symbolic Counter Representation
Storage for an n bit number is obtained with an n flip-flop shift register. As data become available from the memory one bit at a time, serial registers which accept one bit at a time are used. This type of register is constructed by attaching the "1" output (A) of stage (m) to the "1" input (D) of stage (m + 1). Similarly, the "0" output (B) of stage (m) is connected to the "0" input (C) of stage (m + 1). All "F" terminals (Figure 4.3) are connected to a common bus. A positive going 6 volt pulse is applied to this bus to shift the contents of the register one stage to the right (from stage (m) to stage (m + 1)).

The schematic representation of a single flip-flop is shown in Figure 4.4(a). The flip-flop terminals A, B, C, D, F₁ and F₂ are shown for clarity, but are normally not shown. The schematic of a three stage shift register is shown in Figure 4.4(b).

A flip-flop can accept data from more than one source if an additional pair of diode gates are added to the flip-flop for each additional source. When more than one source is used, the 1N67A gating diodes are replaced by 1N625 diodes which have a much lower reverse leakage current. The source of information shifted into the flip-flop is determined by the pair of F₁, F₂ terminals which receive the 6v positive pulse.

A binary counter can be made from the flip-flop in figure 4.3 by connecting the terminals A to C, B to D, and F₁ to F₂. When a positive going pulse is applied F₁ and F₂ the flip-flop is caused to change state. To make an n stage binary counter, the "1" output of stage m is corrected to F₁F₂ of stage m + 1. This will cause stage m + 1 to change state each time that stage m changes from the "1" to the "0" state. The schematic representation of a two stage counter is shown in Figure 4.5.

In tests at 500 Kc/s, a four stage shift register constructed with unselected components was found to operate for all voltage and temperature
variations within design range. Bench tests show that this type of counter will operate at frequencies up to 1 megacycle/sec.

The switching time for a flip-flop loaded by one "and" gate and one shift register stage is .2 to .3 microseconds. The flip-flop is designed to supply or accept a 1 milliamp load in either conducting or cut off state, but a large capacitive load results in a definite showing of switching time. In this case, an emitter follower is normally placed between flip-flop and load to retain switching speed.

4.3 Basic "And" Gates

The "and" gate is a logical element which will pass an incident signal only if all control inputs to the gate are at a particular voltage. Any one input signal must not affect the other input signals to the gate. The gate, when open, must allow an incident signal to pass with minimum delay; when closed, the gate must not pass any appreciable noise. The gate output must be sufficient to drive several circuits.

The M.3 uses three different "and" gates; the transistor "and" gate, the inverting "and" gate, and the diode "and" gate. The signal input and the control inputs on any gate are interchangeable. The gate is turned on when all control inputs are -6v, but is turned off if any control input is 0v. Each gate has advantages and disadvantages, and the gate chosen for any logical operation is determined by the characteristics required. The circuit diagrams of the basic gates and their logical characteristics are shown in Figure 4.6.

The transistor "and" gate shown in Figure 4.6(a) has a 50K ohm input impedance and approximately 1K ohm output impedance. This output impedance limits the number of circuits which the gate can drive. Any number of transistors may be placed in parallel with this basic gate to increase the number of control inputs. The circuit is simple and causes no inver-
(a) Transistor "And" Gate

(b) Inverting "And" Gate

(c) Diode "And" Gate

Fig. 4.6
M.3 "And" Gates

Fig. 4.7
Symbolic Representation of an "And" Gate
sion of input signal. The propagation delay due to the turned on gate is less than .05 μ second, but the fall time of the output signal is dependent upon the load capacitance. When the gate is closed, an incident pulse on one input causes a noise output with 1 v peak amplitude. Less than ½v noise is caused on any of the input lines.

The inverting "and" gate shown in Figure 4.6(b) has a low input impedance (8.2 kΩ in parallel with 200 pf.), but it is valuable as its output impedance of 50 to 100 Ω allows the gate to drive several capacitive circuits. Up to four inputs to the gate may be obtained by attaching additional transistors with input biasing circuits in series with the present transistors. The gate is useful in cases where an inverted output is required, but requires more components than the previous gate. Propagation delay and output rise time are each less than .1 microsecond. When turned off, the noise output from an unloaded gate is less than .8 volts for a normal input signal. This signal causes less than .2 volts noise on other input lines.

The diode "and" gate is shown in Figure 4.6(c). As it contains no active elements, the gate output is directly dependent upon the input. A power amplifier is normally required on the output to prevent input circuit loading. Advantages of the diode gate are low cost, small physical size and ease of construction.

The schematic representation of an "and" gate is shown in Figure 4.7. In this figure, the inputs (a) and (b) are represented by arrows pointed into the circle. The output (c) is represented by an arrow coming out of the circle.

### Basic "Or" Gates

The "or" gate is a logical element in which a signal incident upon any input will cause an output regardless of the state of the other
Fig. 4.8
Basic "Or" Gates

Fig. 4.9
Symbolic Representation of "Or" Gate
inputs. However, an input signal does not affect any other input signal. The gate must not cause appreciable delay to the signal and the output from the gate must be capable of driving several circuits. The three "or" gates used in the M.3 are shown in Figure 4.8.

The transistor "or" gate in Figure 4.8(a) is most commonly used in the M.3. This gate has a 50 KΩ input impedance, 50 to 100Ω output impedance, and produces a propagation delay of less than .05 microseconds. The circuit causes very little increase in the fall time of the input signal, but does not speed it up either. A signal into one input of the gate causes negligible noise on any other input.

The inverting "or" gate shown in Figure 4.8(b) is useful if the output requires inversion with respect to the inputs. This gate has input and output characteristics similar to the inverting "and" gate in the on state. An input signal causes negligible noise on the other input lines.

The diode "or" gate shown in Figure 4.8(c) is the simplest gate, but as the gate contains no active elements, the output impedance is determined by the output impedance of the circuits driving the gate. If heavily loaded, this gate normally has a power amplifier between the output and the load.

The number of inputs to any of the "or" gates shown may be increased by adding more transistors or diodes in parallel with those already present. A schematic representation of a two input "or" gate is shown in Figure 4.9.

4.5 One Shot Circuits

The "one shot" or "delay multivibrator" is a logical circuit which has one stable state and one quasi stable state. The output from the
Input Characteristics

(a) Negative Pulse Generating One Shot

Input Characteristics

(b) Positive Pulse Generating One Shot

Input Characteristics

(c) Symbolic Representation of One Shot

Fig. 4.10
Basic One Shots
One shot is normally at the long term steady state level, but when triggered, the output changes to the opposite state where it remains for a length of time determined by the discharge time of an R-C circuit.

One shots are used in the M.3 to provide timing waveforms with consistent pulse amplitude and width and also to provide adjustable delays. The delay consists of a one shot coupled to an A.C. amplifier to produce an output pulse with leading edge coincident with the trailing edge of the one shot output. The time elapsed between input pulse and output pulse can be adjusted by varying the one shot pulse width.

The one shot shown in 4.10(a) is triggered by a negative going signal at approximately -3 volts. The output transistor is normally conducting, producing a steady state output of 0 volts. However, when the input stage is triggered, the output transistor is switched off for a length of time determined by the time constant $R_1C_1$. During this time, known as the pulse width, the output voltage is -6 volts.

The one shot shown in Figure 4.10(b) is triggered by a positive going signal at approximately -8 volts. The output stage of this one shot is a normally conducting transistor with approximately -10 volts collector voltage. When triggered, the output transistor is switched off and the collector voltage changes to approximately -2 volts. The pulse width is determined by $R_2C_2$. As this one shot is normally used for delay applications, the trailing edge switching time is shortened by the use of an oversized speed up capacitor (300 pF) in parallel with the 5.6 KΩ biasing resistor. This has the disadvantage of slowing the leading edge switching, but as this edge is not used, this is of no consequence.

D.C. triggering has been used on the input to both one shots. This produces a fast switching output waveform for a slow input signal.

In order to ensure that the one shot has two stable states, one with the
output transistor conducting, and the other with this transistor switched off, R should be no more than 56 KΩ and C should be no less than 180 pF.

Both one shots have output impedance greater than 1 KΩ. In cases where the one shot is to be loaded by a capacitive load, an emitter follower is usually placed between one shot and load. Otherwise, the switching time of the leading edge would be considerably slower than desirable.

4.6 The Inverter

The purpose of the inverter in a digital computer is to emit the opposite logical voltage level to the incident voltage level. In the M.3 the inverter must emit -6 volts for 0 volts incident and 0 volts for -6 volts incident. A similar circuit to the inverting "and" gate is used to perform this task (Figure 4.11(a)).

![Inverter Circuit](image)

(a) inverter circuit

(b) logical symbol

Fig. 4.11

4.7 D.C. Delay

It is occasionally necessary to delay a D.C. voltage level change by a short time ( < 2 microseconds). In some cases this delay must be obtained without appreciable slowing of the D.C. level switching
speed. The one shot A.C. amplifier delay cannot be used in this application as a D.C. level output is required rather than a pulse. A simple circuit has been designed to perform this task in the M.3. This circuit, which delays a 0v to -6v voltage level change for a length of time variable from .5 to 2 μsec., is shown in Figure 4.12. The delay time can be controlled by varying the size of the capacitor Cτ. A major drawback of the circuit is that a 10% increase in the input voltage change causes the delay time to be decreased by approximately 10%.

Fig. 4.12
Short time D.C. delay element

4.8 A.C. Ampliers

A.C. amplifiers are required in a computer to differentiate waveforms. Normally, the M.3 uses the basic amplifiers shown in Figures 4.13(b) and (c). However, in cases where an inverted output is required and low output power is satisfactory, the amplifier shown in Figure 4.13(a) is used. The input impedance of the amplifiers is approximately 300 pF in series with 3.3KΩ. The output impedance from amplifiers (b) and (c) is approximately 1.5KΩ; thus an emitter follower is required between amplifier and load for capacitive loads. A .2 micro-
(a) Inverting A.C. Amplifier (Negative Trigger)

(b) A.C. Amplifier (Negative Trigger, Negative Output)

(d) A.C. Amplifier (Positive Trigger, Positive Output)

(d) Symbolic Representation of A.C. Amplifier

Fig. 4.13
Basic A.C. Amplifiers
second delay is obtained between input voltage change and output pulse, but this normally is no problem.

4.9 Emitter Followers

The emitter follower is not a logical circuit, but as it has a high input impedance and a low output impedance, it is very important in the construction of a digital computer. The emitter follower is normally placed between circuits required to emit fast pulses and their loads if the load is capacitive or requires a large driving current.

The M.3 uses three types of emitter followers. In applications where both the leading and the trailing edge of a pulse are important, the "complementary pair" emitter follower (Figure 4.14(a)) is used. The output impedance from this circuit, when driven by a logical circuit, is 50 to 100Ω. This low resistance discharges any capacitive load C very quickly, preventing slowing of both leading and trailing edges of a pulse.

In cases where either the positive or the negative going edge of a circuit output is important but the opposite edge is not, the emitter followers shown in Figures 4.14(b) and (c) are used.

The NPN emitter follower has approximately 50Ω output impedance for D.C. conditions and positive going edges. However, when the input to the emitter follower goes negative, the transistor is cut off and the load capacitance C must discharge through the 1kΩ resistor. This results in an exponential voltage decrease. As the leading edge of a pulse is usually important, the NPN emitter follower is normally used with circuits which emit positive going pulses.

The PNP emitter follower has the opposite characteristic and exhibits a 50Ω output impedance for D.C. and negative edges, but approximately 1kΩ output impedance for positive edges. This emitter follower
(a) Complementary-Pair Emitter Follower

(b) N.P.N. Emitter Follower

(c) P.N.P. Emitter Follower

Fig. 4.14
Basic Emitter Followers
is normally used with circuits which emit negative going pulses.

4.10 Neon Driver

In the M.3, neon are used to indicate the contents of the accumulator, the shift register and the control register. The circuit shown in Figure 4.15 is used to drive the neon. The input to the driver is taken directly from the "l" side of a register stage. Input impedance to the driver is approximately 10.5 KΩ. One milliamp D.C. is passed through the turned on neon. When switched off, the transistor leakage current (I_CBO) bypasses the neon through the 270 KΩ resistor in parallel with it.

![Fig. 4.15](image)

Neon Driver Circuit

4.11 Circuit Layout Techniques

All logical circuits are mounted on 3½" x 8", 22 contact, plug in Veroboard. The Veroboard card was chosen as it permits easy circuit assembly, allows considerable freedom in circuit layout and is quite inexpensive. The card size was chosen mainly for economic reasons. A small
card containing one or two logical circuits simplifies construction and testing, but the expense of the large number of cards and sockets required is not economically justifiable. The eight inch long card used allows at least four logical circuits to be mounted per card. Card servicing is simplified by a plug in test jack which permits easy access to all components mounted on the card.

Each card in the M.3 is stamped with a drawing number. This drawing, which is shown in Appendix A, gives the location and description of all components and wires on the card. The destination and color of wires connected to any of the 22 contacts via the plug in socket is also shown. A small logical diagram on the top of each drawing shows the logical circuits and internal connections on the card and also the socket pin numbers of all accessible input and output points of the logical circuits.

The logic cards are mounted in a 76 card rack. The drawing number for each card is stamped on the rack to ease servicing. Card locations are chosen to keep inter-card wiring to a minimum length.
5. **THE STORE**

The M.3 store consists of a magnetic drum and the circuits required to read and write information in a specified location. To definitively locate each position on the magnetic drum, timing pulses are generated from engraved tracks on one end of the drum. The operation of the M.3 store will be described by considering the following constituent units: the magnetic drum, the counter and coincidence sensor, the head switch, the block switch and the read-write circuits.

5.1 **The Magnetic Drum Memory**

The magnetic drum consists of a 9.75 inch diameter aluminum alloy cylinder which is driven by a small induction motor at 3425 r.p.m. The outside surface of the cylinder is precisely machined and is coated with a thin homogeneous layer of ferrous oxide and plastic. One hundred and twenty eight recording heads are spaced on individual tracks along the side of the cylinder. The recording heads are spaced approximately .0005 inch from the magnetic surface of the drum.

Three engraved soft iron timing tracks are mounted on one end of the cylinder. The first track is engraved with a single slot. This slot generates a single "drum marker" pulse in a read head each drum revolution. The second track is engraved with thirty-two equally spaced slots to generate thirty-two "word marker" pulses in a read head for each revolution of the drum. The third track is engraved with 1280 equally spaced slots (40 between each pair of word markers). The output from the read head on this track is amplified to form the basic 75 Kc/s continuous clock of the computer.

In many of the basic M.3 operations, groups of 32 pulses are required. These pulses are gated from the continuous clock and must occur at a constant location in each word, starting approximately 5 microseconds...
after the word marker pulse.

It was initially planned to gate out groups of 32 pulses from the continuous clock by placing two recording heads on the word marker track. With this method, a flip-flop, known as the "emit flip-flop", is set to unity by a delayed pulse from the leading word marker head, when a group of pulses is required. When in this state, the emit flip-flop opens a gate to allow the continuous clock pulses through. The second word marker head is adjusted so that the word marker engraving passes under this head immediately following emission of the thirty-second pulse from the gate. The pulse induced in the head zeros the emit flip-flop and thus turns off the gate after allowing only 32 pulses to pass.

This method could not be used with the M.3 as the word marker engravings were not milled in a constant position with respect to the continuous clock engravings and the spacing between continuous clock engravings is not constant. These variations made it impossible to gate out a set of 32 pulses in each word location.

The system used to generate timing pulses in the M.3 does not use the word marker engravings, but instead obtains word marker pulses by counting the clock pulses. This method has the advantage that the word marker position is always constant with respect to the clock pulses. Another advantage is that, by generating a word marker pulse after every twentieth clock pulse, sixty-four word locations are designated per drum revolution. By doubling the frequency of the clock pulses, the capacity of the memory is increased from 4096 to 8192 words and the calculating speed of the computer is increased by a factor of two. Outputs from the counter control the opening and closing of the gate which emits groups of 32 pulses, thus giving reliable operation yet eliminating delicate head adjustment.
5.2 The Counter and Coincidence Sensor

The counter and coincidence sensor, shown schematically in Figure 5.1, is responsible for addressing all word locations and also for the generation of timing pulses for the computer.

The single pulse per revolution induced in the drum marker head is amplified by \( a_1 \) and is shaped by a one shot to zero the word marker counter and bit counter. This ensures that the counter always gives memory locations on the drum the same address each time the computer is switched on. To ensure reliable operation, the zeroing pulse should occur approximately three microseconds after a clock pulse. This allows approximately ten microseconds for completion of the zeroing operation before the arrival of the next clock pulse.

Pulses induced in the bit marker head are amplified by \( a_2 \) and shaped by \( S_7 \) to form the basic clock, a 75 Kc/s array of negative-going, one microsecond wide pulses.

The clock pulses are inverted to cause the least significant stage of the bit counter to count. This counter could count to thirty-one, but on the arrival of the twentieth pulse, a positive-going word end marker pulse is generated by \( g_4 \) which zeros the counter and advances the word marker counter by one. A delay is placed between the fifth counter stage output and the input to \( g_4 \) to prevent spurious outputs on the sixteenth count.

As the word location counter is advanced one by each word marker pulse, the counter always contains the address of the word location available. The six stage counter counts from zero to sixty-three and is zeroed by the sixty-fourth pulse. In normal operations, the counter is zeroed by this pulse approximately three microseconds before the arrival of the zeroing pulse from the drum marker head. As the counter is already zero, the zeroing pulse has no effect.
Figure 5.1
Counter and Coincidence Sensor (M.3 Unit 1)
The 75 Kc/s clock supplies only one half the number of bit marker pulses required per word location. A frequency doubler composed of $S_5$, $S_8$ and an "or" gate is required to generate the required number of bits per word. Inverted clock pulses trigger $S_5$ to generate a set of positive-going 6.8 microsecond pulses (one half the average period of the 75 Kc/s clock). $S_8$ is triggered by the negative-going edge of these pulses to produce 1 microsecond negative-going pulse similar to the clock but delayed by one half period. This and the clock are merged by an "or" gate to form the 150 Kc/s clock used by the rest of the computer.

In information shifts to or from the store, the address of the word location involved is stored in a portion of the control register. A continuous comparison between this address and the address indicated by the word marker counter is made by the coincidence senser circuit shown in Figure 5.2. This circuit normally emits a 0 volt level which holds $g_1$ in the switched off state. However, when coincidence occurs, the output voltage switches to -6 volts allowing pulses to pass through $g_1$ if an "M.emit" signal is present.

![Diagram of Coincidence Senser Circuit](image)
The one shot $S_1$ and A.C. amplifier $a_3$ produce a test pulse which is delayed from the word marker pulse by a time equal to the output pulse width of $S_1$. The delay is inserted to allow the coincidence sensor input to $g_1$ to settle down after the counting impulse. Otherwise spurious operation might result.

The test pulse tests $g_1$ and $g_2$. If a transfer of information to or from the store is required, the M.emit line is activated. In this case a pulse will pass $g_1$ only if coincidence is sensed. If 32 pulses are required for multiplication or division, the "instantaneous emit" line is activated. In this case, as coincidence is not required, the first test pulse generated will pass through $g_2$. A pulse through either $g_1$ or $g_2$ sets the emit flip-flop to unity.

When the emit flip-flop is set to unity, the double frequency clock pulses are allowed to pass through $g_5$. To ensure that the gate allows only 32 pulses to pass, $g_3$ zeros the emit flip-flop a short time after counting the seventeenth 75 Kc/s clock pulse. The short time delay produced by $S_2$ is required to ensure that $g_5$ will not close before the complete emission of the thirty-second pulse. A delay is placed between the output of the fifth counter stage and the input to $g_3$ to prevent spurious output from $g_3$ when the bit counter changes from fifteen to sixteen.

The set of 32 pulses emitted from $g_5$ is known as the "32 immediate" or "32 IMM" pulses. Their main use is as timing pulses when writing information on the magnetic drum. To read recorded information from the drum, a set of pulses are required which occur approximately three microseconds after the beginning of each of the "32 IMM" pulses. These "strobe" pulses are generated by triggering the delay one shot $S_6$ by the leading edge of each "32 IMM" pulse. The trailing edge of the $S_6$ output triggers the A.C. coupled pulse forming one shot, producing the required set of
Figure 5.3
M.3 Timing Pulses
2.5 microsecond pulses.

To shift information from the read circuit to registers within the arithmetic and control units, a set of 1 microsecond pulses are required which occur 1 microsecond after the trailing edge of each strobe pulse. These pulses, known as the "delayed 32" or "V 32" pulses, are generated by triggering $S_{11}$ from the trailing edge of each strobe pulse and by triggering $S_{12}$ from the trailing edge of the $S_{11}$ output.

An "operation complete" pulse (op. comp. pulse) must be generated by the store following emission of each set of 32 pulses. This pulse informs the control and arithmetic unit that an order or a portion of an order has been completed. Zeroing of the emit flip-flop triggers the delay one shot $S_9$. The trailing edge of the $S_9$ output triggers an A.C. amplifier which produces the required op. comp. pulse. The delay circuit must not emit the op. comp. pulse before emission of the thirty-second $V 32$ pulse. Also the pulse should occur approximately 3 microseconds after a clock pulse.

In manual operation, the operation complete pulse is generated by operating a lever key switch. Contact bounce on the output from the switch is removed by a 10 millisecond one shot. The trailing edge of the one shot output triggers an A.C. amplifier to produce the manual pulse. The outputs from the manual and automatic op. comp. pulse sources are merged by an "or" gate which passes the pulse to the rest of the computer.

5.3 The Head Switch

The magnetic drum used with the M.3 has 128 recording heads. The computer must be able to address any one of these heads to store or receive information. To do this, the heads are divided into 16 blocks, each containing 8 heads.
Heads in the first block are assigned track numbers from 0000 to 0111. A head in this block may be switched on by placing the track number of the head in either the "X" or "Y" address of an instruction. Heads in this block are continuously available, and are independent of the block switch.

In the remaining fifteen blocks, the heads in each block are assigned track numbers from 1000 to 1111. To address a head in this group, the block containing the required head is first switched on by a block switch instruction. The head can then be addressed by placing the track number in either the "X" or the "Y" address of the instruction as usual.

The head switch is composed of three main sections; a storage register which holds a track number as long as information is required from that track, a diode matrix which produces a single output for each combination in the storage register and a transformer-symmetrical transistor gate array which is controlled by the output from the diode matrix and which turns on the head or set of heads required.

The storage register must accept information from either the "X" or the "Y" track location in the Control Register. The "X" track location, stored in Control Register stages 1 to 4 (C.R. 1-4), is shifted into the storage register by a positive pulse from a4 (Figure 5.4). This A.C. amplifier is triggered by the negative change in output voltage of the control flip-flop (C.F.F.) when the C.F.F. is set to unity. The "Y" track location, stored in C.R. 11-14 is shifted into the storage register by a "Y" diode pulse from the control.

Complementary pair emitter followers are placed on each storage register output to prevent register loading by the diode matrix and to preserve the fast switching time of the register flip-flops.
Figure 5.4
Head Switch Circuit for Head 0000
A diode matrix decoder translates the four bit track address into a single output from the sixteen possible. Each output from the matrix is generated by a four input diode "and" gate similar to that shown in Figure 5.4. The output voltage from the "and" gate is normally 0 volts. However, when all inputs to the "and" gate are -6 volts, a -6 volt output is produced.

Each output from the matrix is directly connected to an inverting amplifier whose output drives the transformer-symmetrical transistor gates. A 0 volt input to the amplifier holds the 2N1307 transistor in the switched-off state, producing a -12 volt output. However, when the input to the amplifier is -6v, the transistor is saturated, causing the output voltage to switch to approximately 0 volts.

The amplifier outputs are directly connected to the inputs of the transformer-symmetrical transistor gates. The gates consist of a Ferroxcube 3C pot core transformer with an eight turn primary winding connected to a memory head output and a twenty-six turn centre tapped secondary with the terminals of the centre tap connected to the collector and emitter of a 2N594 NPN symmetrical transistor. The secondary outputs from all gates in a block are connected in parallel to the primary winding of the block switch. When a block is turned on, a -1.5v level is applied to the centre tap of the block switch primary winding. To turn on a particular gate in the block, a 0 volt level is applied to the base of the symmetrical transistor through a 56Ω resistor. This causes the transistor to be forward biased and current passes through the transistor and transformer windings to the -1.5v level. When in this state, an A.C. signal input to the gate from either direction finds a low impedance path (approximately .75Ω for signals from the head) due to the saturated common base amplifier, and passes through the gate with very
little attenuation.

The remaining seven inputs to the gates in a particular block are held at -12v by the diode matrix decoder. This reverse biases the symmetrical transistors in the gates by approximately 10.5 volts. In this state, the transistors appear as approximately a 200 KΩ resistance in parallel with a 26 pf capacity. The impedance ratio of a switched off to switched on transistor at operating frequencies is approximately $5 \times 10^4$: 1. This results in a gate having a very good signal to noise ratio.

5.4 The Block Switch

The block switch must switch on one from a total of fifteen available blocks. The block switch instruction triggers a₁ (Figure 5.5) to shift the block address stored in C.R. 1-4 into the block switch storage register. A three microsecond delay on the switch instruction allows the positive shift pulse from a₁ to also be used as an op. comp. pulse. The delay allows the C.F.F. to settle to unity state before being reset by the op. comp. pulse.

To prevent storage register loading, emitter followers are placed on all outputs to the block selector diode matrix.

The diode matrix consists of fifteen 4 input "and" gates. The output from each gate drives an inverting amplifier similar to that used in the head switch. Incorrect combinations into an "and" gate cause an amplifier output of -12 volts. As this voltage is applied to the base of a symmetrical transistor with emitter and collector held at approximately -1.5 volts, the transistor and thus the block input is switched off.

When a diode "and" gate is turned on by the storage register, the output voltage from the inverting amplifier switches to 0 volts. This saturates the transistor in the transformer-symmetrical transistor
Figure 5.5
Block Switch Circuit for Block 0000
Figure 5.6
Head Switch - Block Switch - Read-Write Interconnections
gate, causing the block to be turned on.

When a block is switched on, -1.5 volts must be applied to the primary winding centre tap of the block switch transformer to supply the biasing level for the head switch gates (Figure 5.6). However, if -1.5 volts was applied to the centre tap of all fifteen block inputs, addressing a head between 1000 and 1111 would pass a 25 milliamp saturating current through the head addressed in each of the fifteen blocks. This would overload the head switch. To prevent overloading, +1.5 volts is applied to the primary winding centre tap of all unwanted blocks. This reverse biases all symmetrical transistors in the fourteen blocks by a minimum of 1.5 volts, sufficient to stop D.C. current flow, but insufficient to prevent passage of the 16 volt peak to peak write signal which must be stopped by the transformer-symmetrical transistor gates in the block switch.

The centre tap voltage level is generated by a 2N1306 inverting amplifier (Figure 5.5). When -12 volts is applied to the amplifier as is the case when a block is switched off, the 2N1306 is cut off, producing a +1.5 volt output. When a block is turned on, the 0 volts applied passes sufficient current through the 2.7K resistor to saturate the transistor, producing a -1.5 volt output.

5.5 The Write Circuit

Information is stored on the magnetic drum surface in the form of small magnetized elements. These elements are magnetized by passing a current pulse through a head for a length of time less than 1 bit period. The amplitude of this pulse must be sufficient to allow removal of old information from the drum by recording new information over it.

Information is recorded in the M.2 by current pulses which resemble the positive portion of a sine wave. The "1" is distinguished
from the "0" by passing the current pulse through the head in the opposite direction. This writing technique was tried on the M.3, but recording an unbalance of "1"s or "0"s resulted in an operating point shift of the transformer network between the write circuit and the head. The operating point returns to the normal level, but the return requires a length of time greater than the recovery time between two word locations. This prevented reading information immediately after recording. The use of this system would have made programming more difficult and reduced operating speed.

The use of double pulse writing was adopted to overcome the D.C. shift problem. The current pulse used in this system resembles a complete cycle of a sine wave and has a peak value of 1 amp in each direction. Again "1" is distinguished from "0" by passing the current pulse through the head in the opposite direction. Adjustment of the current pulse shape allows D.C. level shift in this system to be practically eliminated.

The write circuit is composed of three main parts, the write gate, the pulse shaper and the power amplifier. The write gate (Fig. 5.7) translates information from the accumulator or the shift register into a set of positive pulses. A pulse on one output from the write gate indicates a "1" is to be recorded; a pulse on the other line indicates a "0" is to be recorded.

The write gate is activated by an order to record the information stored in the accumulator (A(n)) or the information stored in the shift register (R(n)) in memory location "X". To record an n bit word, where n is 32 or less, C6 must initially be set to 32-n.

The 32 IMM pulses emitted at the "X" word location test g6. This gate, controlled by C6, allows the first n pulses to pass. The A(n)
(a) Write Gate Logic

(b) Write Gate Circuit \(g_6, g_7, g_8, g_9, g_{10}, g_{11}, g_{12}\)

Figure 5.7.
Write Gate
instruction opens \( g_7 \), allowing the 32 IMM pulses to test \( g_9 \) and \( g_{10} \).

A "1" stored in the thirty-third stage of the accumulator at the arrival time of an IMM pulse causes \( g_9 \) to emit a positive pulse. A "0" in this stage causes \( g_{10} \) to emit a positive pulse. The \( A(n) \) instruction also opens \( g_{14} \) to allow strobe pulses to pass. These cause \( C6 \) to count, shift the accumulator contents to the right and shift \( A31 \) to both \( A32 \) and \( A33 \).

To record information from the shift register, the \( R(n) \) instruction opens \( g_8 \) and \( g_{13} \). Immediate pulses through \( g_8 \) test \( g_{11} \) and \( g_{12} \), causing positive pulses to be generated on the appropriate output lines. Strobe pulses passing through \( g_{13} \) shift the shift register to the right and cause \( C6 \) to count.

The outputs from \( g_9 \) and \( g_{12} \) are merged by an "or" gate to form the write "1" output. Similarly, the outputs from \( g_{10} \) and \( g_{11} \) are merged to form the write "0" output.

The read amplifier has a low input impedance to the large signal generated by the write circuit. To prevent write circuit loading, the presence of a write order generates a -12 volt "read circuit inhibit" output. When a write order is not present, the 0 volt output allows normal read circuit operation.

The positive pulse generated by the write gate must be shaped to produce a sinusoidal current output from the power amplifier. When the write gate emits a write "1" pulse, this pulse passes directly through \( Q_1 \) of the pulse shaper (Figure 5.3) to cause current flow from the write "1" power amplifier to the primary centre tap. The trailing edge of the pulse from the write gate is differentiated by \( a_2 \) to trigger \( S_2 \). The output from \( S_2 \) causes current flow from the write "0" power amplifier to the centre tap.
Figure 5.8
Pulse Shaper and Power Amplifier Logic

Figure 5.9
Write Circuit Power Amplifier
When the write gate emits a write "0" pulse, the "0" power amplifier generates the first portion of the current pulse and the "1" power amplifier generates the second portion.

As both "1" and "0" inputs to the power amplifier cause current flow toward the primary centre tap of the output transformer, the secondary current generated by the "1" power amplifier flows in the opposite direction to the current generated by the "0" power amplifier. As the head is an inductive load, the output current is approximately sinusoidal.

Operating point shift is removed by first adjusting the pulse width of $S_2$ so that no D.C. shift occurs after writing 32 "1"'s. Then the pulse width of $S_1$ is adjusted so that no D.C. shift occurs after writing 32 0's.

The power amplifier circuit is shown in Figure 5.9. The 2N1999 transistors which supply the write current are normally cut off by the +1.5 volt output from the complementary pair emitter follower. The input to the emitter follower is produced by a normally saturated 2N1307 transistor. A positive-going input pulse switches the 2N1307 off, causing its output voltage to switch to the clamped -6 volt level. This saturates the 2N1999 transistor causing current flow through the output transformer winding to the centre tap.

A -1.5 volt level is applied to the secondary winding centre tap of the output transformer. This supplies the biasing level for block switching and for the read amplifier inhibit circuit (Figure 5.6).
5.6 The Read Circuit

To transfer information from the store, the small voltage induced in the recording head must be converted to a form acceptable to the logical circuits. This conversion is performed by the "read circuit"; a high gain amplifier whose output, when sampled by strobe pulses, sets the incident digit flip-flop (I.F.F.) to the appropriate state (Figure 5.10).

The signal induced in a recording head contains two basic frequencies, 75 Kc/s for alternate 1's and 0's and 150 Kc/s for continuous 1's or 0's. The signal level from the 1 microhenry head is approximately 350 microvolts peak to peak, however a 1:3.25 transformation at the head switch and a 1:10 transformation at the amplifier input transformer causes the amplifier input to appear as 9 millivolts from a 1 millihenry source.

The transformer-symmetrical transistor gate input to the amplifier is switched off during writing to prevent write circuit loading and extreme amplifier saturation.

The amplifier must not produce a large change in phase shift between 75 Kc/s and 150 Kc/s or the sampling circuit will not operate. Phase lag due to the inductive source impedance (1 KΩ at 150 Kc/s) is less than 2 degrees as the input impedance to the amplifier is greater than 50 KΩ. Phase change due to the amplifier in the 75 to 150 Kc/s range is reduced by non-linear negative feedback. The effect of power supply noise is reduced by an R.C. filtered supply used with the pre-amplifier. The amplifiers low 60 cycle/s gain eliminates problems due to 60 cycle pickup.

The sampling circuit requires two inputs; one input the inverted image of the other. This is obtained by placing equal resistors in series with the collector and emitter of the output transistor and connecting to
Figure 5.10
Read Circuit
both collector and emitter.

Points A and B of the sampling circuit, which are connected to the amplifier outputs by 1000 pf capacitors, are normally clamped to a slightly positive potential by 1N273 diodes and the 2N1306 base to collector junctions. Negative-going strobe pulses from $g_{15}$ reverse bias the 1N273 diodes allowing A or B to follow the input signal to a negative voltage. The negative level on A or B allows the attached 2N1306 transistor to operate as an emitter follower and set the I.F.F. by applying a negative voltage to the direct coupled trigger transistor.

In cases where the cycle register sets the I.F.F., the instr.
emit signal from the arithmetic unit prevents strobe pulses from passing through $g_{15}$ and shift pulses from the cycle register (a portion of the arithmetic unit) shift the contents of the thirty-second cycle register stage into the I.F.F.
6. OVERALL SYSTEM DESIGN OF THE M.3

The M.3 consists of two sections, namely control and arithmetic. Much of the logic is identical with that of the M.2. However, an additional shift register (the cycle register) has been added to the arithmetic unit. In the M.2, division is an operation which requires an entry and an exit subroutine; in the M.3 this division has been replaced by a unit which is completely automatic and does not involve manipulation of the signs of the interacting numbers.

6.1 The Control

The control consists of two units, the control network and the control register. Control is based upon the state of a single flip-flop, the "control flip-flop" (C.F.F.). When in the "0" state, the C.F.F. causes a new instruction to be shifted into the control register; when in the "1" state, it causes the instruction to be executed.

The control register (Figure 6.1) is a thirty-two stage shift register which holds an instruction until it is executed. The composition of the instruction is as follows:

- C.R. 1-4, "X" track location
- C.R. 5-10, "X" word location
- C.R. 11-14, "Y" track location
- C.R. 15-20, "Y" word location
- C.R. 21-25, order
- C.R. 26-31, C6 input
- C.R. 32, not used.

The "X" address is normally the memory location of a number required in the execution of an order. The "Y" address is normally the memory location of the next instruction. Following execution of an order, the "Y" word location must be shifted to C.R. 5-10 to locate the next in-
Control Register (M.3 Unit 5)

Figure 6.1

Function Table

C6 Count

Inhibit Counting

C6 Gating

Count Direction

From C.R. 20

FUNCTION TABLE EMIT

C6 Output
struction. This shift is possible as two input shift register stages are used in C.R. 5-10. A pulse applied to one set of trigger capacitors causes a normal right shift of data; a pulse applied to the other set causes a parallel shift of data from C.R. 15-20 to C.R. 5-10.

By decoding the order stored in C.R. 21-25, the "function table" (Figure 6.2) must activate one or more lines to the arithmetic unit. To prevent generation of incorrect orders when shifting data into the control register, an additional function table input from the C.F.F. prevents output while the C.F.F. is in the zero state. The diode "and" gates used in the function table generate a -6 volt output only when all inputs are -6 volts. A left shift order produces an output on both 00100 and 00110 lines; a right shift order produces an output on the 00110 line. Clear and add is produced by a 10000 input, clear and subtract by a 10010 input. A 10100 input causes addition and a 10110 input causes subtraction.

The "control counter" (C6) which controls the number of basic operations performed in some orders occupies C.R. 26-31 (Figure 6.1). This portion of the control register operates both as a shift register and as a counter. Each flip-flop has two shift inputs as described in Chapter 4.2. One input is connected as a standard shift register stage. The other input shifts the reverse contents of the stage back into itself when triggered, thus acting as a counter.

The interstage amplifiers S1 to S6 (Figure 6.3) emit a positive pulse to cause counting when a negative change in voltage is applied to the input. The amplifiers are connected to cause counting in the C.R. 31 to C.R. 26 direction. To prevent counting action during shifting, all interstage amplifiers are switched off by S7 when the C.F.F. is in the "0" state.

The operation of the control network (Figure 6.4) is as follows:
Figure 6.2

Function Table
Fig. 6.3

C6 Shift Register-Counter

When in the "0" state, the C.F.F. opens g₁ and activates the M emit line to the memory. ³ 32 pulses from the memory pass through g₁ to shift a new instruction into the control register. The op. comp. pulse which follows sets the C.F.F. to unity and tests g₄. This gate is cut off when the C.F.F. is in the zero state and the delay (Ⅳ) between the C.F.F. output and g₄ ensures that no breakthrough results from the C.F.F. changing states before the op. comp. pulse dies away.

When the C.F.F. is in the "1" state, the function table is primed and the "X" track address is shifted to the head switch. The course of action now followed is determined by the order:
(1) Add, subtract, clear and add, clear and subtract, record accumulator contents in memory location "X", record register contents in memory location "X", transfer contents of memory location "X" to register, transfer contents of memory location "X" to cycle register.

In this case a transfer of data to or from the store is required. The order code is designed so a "1" appears in the most significant digit of each of these orders. The output from C.R. 21 opens $g_5$ and produces an M. emit signal from $g_3$, causing emission of 32 pulses upon coincidence between the "X" word location and the word location available. The op. comp. pulse which follows tests $g_4$. As the C.F.F. is in the "1" state, the pulse passes to the arithmetic unit. Here it passes through an "or" gate after which it returns to test $g_5$. As $g_5$ is open, the pulse resets the C.F.F. to "0", and passes as a "Y" diode pulse to shift the "Y" track location to the head switch and cause transfer of the "Y" word location to C.R. 5-10 (the inverted outputs from $g_5, g_6, g_7, g_8$ and $a_3$ are merged by the use of a common collector resistor). The transfer of the next instruction to the control register will now proceed as before.

(2) Left shift and right shift.

In this case no M. emit is generated. Shifting is performed by continuous clock pulses and the op. comp. pulse is derived from the output of C6 which generates a pulse in the A.C. coupled $g_6$. This pulse resets the C.F.F. to "0" and passes as a Y diode pulse. The operation is then as described in (1).

(3) Multiply and divide.

In this case the operation complete pulse from the arithmetic unit after each basic operation tests $g_5$ and causes C6 to count. C.R. 21
is not unity in this case, and \( g_5 \) remains switched off until opened by C6. To ensure that breakthrough does not take place before the operation complete pulse has died away, a delay is placed on the C6 input. The following op. comp. pulse passes through \( g_5 \), generating a positive pulse which resets the C.F.F. and passes as a Y diode pulse. The operation is then as described in (1).

(4) Block switch and operations involving peripheral equipment.

In each of the above cases, the op. comp. pulse is generated within the unit a short time after receiving the instruction. The op. comp. pulse is merged by \( g_9 \) and inverted by \( a_3 \) to reset the C.F.F. and pass as a Y diode pulse. Operation is then as described in (1).

(5) Branch on accumulator contents and branch on shift register contents.

For an accumulator branch, when the C.F.F. switches to the "1" state, the branch instruction applies a -6 volt level to \( \nabla_1 \). \( \nabla_1 \) generates a delayed voltage change which tests \( g_8 \) and is differentiated to reset the C.F.F. to "0". If \( A_1 \) is unity, \( g_8 \) emits a Y diode pulse and attempts to reset the C.F.F. to "0". This reset pulse has no effect as the C.F.F. is already "0".

Following the reset of the C.F.F., the memory shifts the next instruction into the control register. If the Y diode pulse has not been generated, this instruction is shifted from the "X" memory location. However, if the Y diode pulse has been generated, the "Y" to "X" word location shift is performed and the "Y" track location is shifted into the headswitch. This causes the instruction to be shifted from the Y memory location.

The same procedure is carried out for the register branch instruction except that \( \nabla_{2} \), \( a_2 \) and \( g_7 \) are involved.
When testing computer operation or a portion of a program, it is useful to instruct the computer to perform one operation and then stop. This mode of operation is gained by the addition of \( g_2 \). In normal operation, \(-6\) volts is applied to the control input of \( g_2 \). However, for "one shot" operations, \(0\) volts is applied by operating a switch on the control panel. This prevents issue of the \( M \) emit order to the store when the C.F.F. is in the zero state and, as a result, causes operation to stop. An instruction can now be set manually from the control panel into the control register and can be executed by operation of a manual trigger switch which sets the C.F.F. to "1".

6.2 The Arithmetic Section

The arithmetic section of the logic is composed of four units; the arithmetic unit, the accumulator, the shift register and the cycle register. Its operation for the various orders is as follows:

6.2.1 Transfer of a Number from Memory Location "X" to the Shift Register

In transfer operations from the memory, each bit emitted from the incident-digit flip-flop (I.F.F.) arrives approximately 2 microseconds before the arrival of a \( \nabla \) 32 pulse. The transfer order opens \( g_{10} \) (Figure 6.5) allowing the \( \nabla \) 32 pulses to shift information from the I.F.F. into the first stage of the shift register and shift the register contents to the right. To prevent unnecessary circuits from operating, the register shift pulses pass through the "or" gate \( Q_1 \).

6.2.2 Transfer of a Number from Memory Location "X" to the Cycle Register

Here, the transfer is performed in a manner similar to that described in 6.2.1. The transfer to cycle register order opens \( g_{12} \) on Figure 6.6 to allow the \( \vee \) 32 pulses to pass. From \( g_{12} \), the I.F.F. contents into Cl and pass through \( O_2 \) to cause cycle register shift
Figure 6.5
Shift Register (M.3 Unit 3)
Figure 6.6
Cycle Register (M.3 Unit 4)
6.2.3 Right Shift and Left Shift

Right shift consists of shifting the accumulator and shift register contents to the right with the least significant stage of the accumulator shifting into the most significant stage of the shift register. The sign bit of the number in the accumulator is propagated across the accumulator and the shift register contents are lost out the least significant stage. Left shift is similar to right shift but data in the thirty-second stage of the shift register are shifted back to the first stage of the accumulator.

The right shift order from the function table opens the inverting gate g₁₄ on Figure 6.7. This allows clock pulses to shift A₃₃ to R₁, A₃₁ to A₃₃ via Q₄ and to shift the accumulator to the right via O₅. Pulses pass through O₃ to be counted by the C₆, and pass through O₁ on Figure 6.5 to cause right shift of the shift register.

To avoid duplication of equipment, the left shift order opens both g₁₃ and g₁₄. This causes a right shift to be performed but with pulses from g₁₃ shifting the contents of R₃₂ to A₁. The number of shifts are again counted by C₆ via O₃.

To perform a right shift of n bits, C₆ is initially set to (6₄-n). To perform a left shift of n bits, C₆ is set to n.

6.2.4 Addition and Subtraction

Addition is performed by the following rules:

If: Incident digit = carry digit (coincidence)

Send A₃₃ to A₁

Carry digit is unchanged.
Figure 6.7
Accumulator (M.3 Unit 2)
If: Incident digit ≠ carry digit (anti-coincidence)
    Send the inverse of A33 to AI
    Send A33 to the carry digit store.

The carry digit is initially set to zero.

The adder-subtractor circuit is complicated somewhat by the fact that a dummy stage, A33, is provided in the accumulator to facilitate left shift in division. In addition and subtraction, both A32 and A33 are fed from A31, causing A32 to equal A33. In division, A33 is fed from A32.

When addition is signalled, -6 volts is applied to the add line of Figure 6.8. The negative voltage change triggers the inverting amplifier a₁ causing the carry flip-flop "C" to be set to zero. The add order also opens g₁₇, g₁₈ and one input to g₂₅. As no divide order is present, the inverted divide input opens g₂₅. One side of g₂₃ is also open, but as the multiply order is not present, there is no output from this gate.

When the digits of the addend arrive from the memory, the coincidence senser (shown in Figure 6.9) compares each incoming digit with the corresponding carry digit and emits a -6 volt coincidence or anti-coincidence level. Approximately 2 microseconds after the arrival of each digit a V32 pulse tests the coincidence senser output via g₁₅ and g₁₆, causing the appropriate shift pulse to be passed through g₁₇ and g₁₈. A33 is shifted to AI if coincidence is sensed and the inverse of A33 to AI if anti-coincidence is sensed.

When anti-coincidence is sensed, the shift pulse also shifts the A33 contents into C. To prevent the change in the carry digit contents from distorting the output pulse from the circuit, the delay shown in Figure 6.9 is placed between C and the coincidence senser.
Figure 6.8

Arithmetic Unit (M.3 Unit 7)
Fig. 6.9
Arithmetic Unit Coincidence Senser

The \( \nabla \) 32 pulses pass through the inverting \( g_{25} \) to shift the the accumulator contents to the right and shift \( A_{31} \) to \( A_{33} \). This clears \( A_1 \) for the incoming digit of the sum, and advances the next digit to be added into \( A_{33} \).

Subtraction is performed by the following rules:

If: Incident digit = carry digit (coincidence)
Send the inverse of \( A_{33} \) to \( A_1 \)
Send \( A_{33} \) to the carry digit store.

If: Incident digit \( \neq \) carry digit (anti-coincidence)
Send \( A_{33} \) to \( A_1 \)
The carry digit is unchanged.
A subtract order from the decoder switches the subtract line voltage from 0 to -6 volts. This triggers $a_2$ to set $C$ to unity. Subtraction of incoming digits from the number stored in the accumulator is performed in a manner similar to addition. However, to produce the effect of inverting the incoming digits, $g_{17}$ and $g_{18}$ are switched off while $g_{19}$ and $g_{20}$ are opened by the subtract order. Coincidence now shifts A33 to the carry store and the inverse of A33 to Al; anti-coincidence shifts A33 to Al.

In both addition and subtraction, the operation complete pulse is generated by the memory following the thirty-second shift pulse.

6.2.5 Clear Operations

In clear and add, clear and subtract or multiply orders, the accumulator must be zeroed before the arithmetic operation can be performed. In the first two cases, the clear order is generated by a separate output from the function table. In multiplication, the clear order is generated by the arithmetic unit immediately following receipt of the multiply order.

The clear instruction passes through $O_7$ on Figure 6.5 to trigger a D.C. coupled one shot. The 5 microsecond pulse generated by this circuit triggers the zero accumulator circuit shown in Figure 6.10. The operation of this zeroing circuit is as follows: Normally, sufficient base current is drawn from $S_1$ to cause saturation. In this state, the output voltage of +1.3 to +1.4 volts allows normal accumulator operation. However, a positive pulse applied to the 3000 pf input capacitor switches $S_1$ off, causing a negative output voltage. The negative voltage draws current from the 8.2K biasing resistor of each accumulator flip-flop, causing the right hand transistor in each to be turned on. By this method, all flip-flops in the accumulator are zeroed in 2 to 3 microseconds.
The manual zero switch shown in Figure 6.10 zeros the accumulator by removing the saturating current from $S_1$.

### 6.2.6 Multiplication

The rules of multiplication are:

For basic operations 1 to 31:

- **If:** $R33 = R32$, shift accumulator and register one place right.
- **If:** $R33 = 1$, $R32 = 0$, add $C$ to the accumulator, then shift the accumulator and register one place right.
- **If:** $R33 = 0$, $R32 = 1$, subtract $C$ from the accumulator, then shift the accumulator and register one place right.
For basic operation 32:

This operation is identical to previous 31, but delete right shift.

The accumulator and R33 must be zeroed prior to the calculation. The multiplier 0 is stored in the cycle register and the multiplicand in the shift register.

The multiply order from the function table opens $g_{21}$ and $g_{22}$ (Fig. 6.8) so that according to the contents of R32 and R33, an add or subtract instruction can be issued by $g_{33}$ or $g_{34}$. If addition or subtraction is required, an inst. emit signal is sent to the memory by $g_{23}$ which is primed by the multiply order. This causes emission of the next available set of 32 pulses from the memory and permits emission of data from the cycle register by opening $g_{11}$ of Figure 6.6 and inhibing the strobe pulses to the read circuit. The 32 pulses cause cycling of cycle register contents and shift the contents of C32 to the I.F.F.

Following addition or subtraction, which is performed in the normal manner, the op. comp. pulse incident on $O_{0}$ passes to the control and also tests $g_{29}$.

If $g_{33}$ and $g_{34}$ signal neither addition nor subtraction, $g_{24}$ opens to allow clock pulses to pass to $O_{0}$. From here, the incident pulses pass to the control and also test $g_{29}$.

For the first 31 basic operations, $g_{29}$ is held open by C6. Incident pulses from $O_{0}$ pass via $g_{29}$ and $g_{27}$ (held open by the multiply order) as "X shift" pulses which cause a right shift of accumulator and shift register contents and cause C6 to count. Following the thirty-first basic operation, C6 switches $g_{29}$ off, preventing a thirty-second right shift, and opens a gate in the control to allow the thirty-second op. comp. pulse to signal the end of the multiplication. When programming a multiplication, C6 must be set to 33.
6.2.7 Division

Division in the M.3 is performed by the non-restoring process as follows:

For basic operations 1 to 31:

If: $C_1 = A_1$  add $2^{-31}$ to the register, shift accumulator and register one place left, subtract $C$ from the accumulator.

If: $C_1 \neq A_1$  add 0 to the register, shift accumulator and register one place left, add $C$ to the accumulator.

For basic operation 32:

Add $2^0$ to the register.

In division the divisor $C$ is initially stored in the cycle register and the dividend in the accumulator. The left shift required is obtained by interposing the additional stages A33 and R33 in the accumulator and register, and causing register shift with end round connection of R33 to R1 during the addition and subtraction cycles. Since there are only 32 shift pulses, the net result after each addition or subtraction is one left shift in the accumulator and register.

The divide order from the decoder activates the inst. emit line, switches off g_{25} and opens g_{26} to produce left shift, opens g_{28}, primes g_{30} and g_{31} and is differentiated by $a_6$ to generate a pulse which passes through O_{3} (Figure 6.8). In division, g_{29} is held open by C6 until the first thirty-one pulses pass. The pulse from O_{3} tests the control and passes through g_{28} and g_{29} to cause C6 to count, zero A33, shift the coincidence sensor #2 output into R32 and the "$P$" flip-flop and to switch off g_{31} and g_{32} for 2 microseconds. The latter operation is necessary to set the carry flip-flop prior to each addition or subtraction.
If coincidence is sensed, R32 and F are set to unity and the F output issues a subtract instruction via g31. If anti-coincidence is sensed, R32 and F are set to zero and an add instruction is issued via g30. The inst. emit signal to the memory causes emission of 32 pulses and the number stored in the cycle register is added to or subtracted from the accumulator. The op. comp. pulse which follows is incident on O8 causing the operation to be repeated. The op. comp. pulse following the thirtieth addition or subtraction causes C6 to switch g29 off and prime a gate in the control. The pulse following the next addition or subtraction sets the C.F.F. to zero, ending the division. The function table output change to 0 volts is differentiated by a5 to produce a pulse which changes R1 to a "0" if initially a "1" or to a "1" if initially a "0".
REFERENCES


### M.3 ORDER CODE

<table>
<thead>
<tr>
<th>Number</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>S</td>
<td>Block head switch. This enables the block of heads specified in &quot;X&quot; track location to be shifted into the working store.</td>
</tr>
<tr>
<td>1</td>
<td>H</td>
<td>Input. The 6 digits currently under the tape reader fingers are transferred into the 6 most significant digits of R. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>2</td>
<td>I</td>
<td>Punch. The digits contained in the 6 most significant places of R are punched onto the output tape. The digits are not lost from R in so doing. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>4</td>
<td>P</td>
<td>Type. The symbol represented by the digits in the 6 most significant places of R is typed. The digits are not lost from R in so doing. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>6</td>
<td>B&lt;sub&gt;A&lt;/sub&gt;</td>
<td>Branch (accumulator). If the contents of A are (&lt; 0) take next order from location &quot;Y&quot;, but if (\geq 0) from location &quot;X&quot;.</td>
</tr>
<tr>
<td>7</td>
<td>B&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Branch (shift register). If the contents of R are (&lt; 0) take next order from location &quot;Y&quot;, but if (\geq 0) from location &quot;X&quot;.</td>
</tr>
<tr>
<td>8</td>
<td>l&lt;sub&gt;n&lt;/sub&gt;</td>
<td>Left shift. Shift the contents of A and R left n places. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>10</td>
<td>r&lt;sub&gt;n&lt;/sub&gt;</td>
<td>Right shift. Shift the contents of A and R right n places. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>14</td>
<td>x</td>
<td>Multiply the number in the cycle register by the last n digits of the number in R, sending the 32 most significant digits of the product to A and the 31 least significant to R. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>15</td>
<td>—</td>
<td>Divide the number stored in A by the number stored in the cycle register. The quotient is set into the shift register. Next order in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>16</td>
<td>+c</td>
<td>Send the contents of location &quot;X&quot; to the cleared accumulator. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>Number</td>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>----------</td>
<td>-------------</td>
</tr>
<tr>
<td>18</td>
<td>(-c)</td>
<td>Subtract the contents of location &quot;X&quot; from the cleared accumulator. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>20</td>
<td>(+)</td>
<td>Add the contents of location &quot;X&quot; to the accumulator. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>22</td>
<td>(-)</td>
<td>Subtract the contents of location &quot;X&quot; from the accumulator. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>24</td>
<td>(T)</td>
<td>Transfer contents of location &quot;X&quot; to R. R is automatically cleared by the transfer. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>25</td>
<td>(C)</td>
<td>Transfer contents of location &quot;Y&quot; to the cycle register. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>26</td>
<td>((R_n) 32-n (R_{n-32})</td>
<td>Record either the first or the last of the digits in R in location &quot;X&quot;. The remaining digits of &quot;X&quot; are unaffected, but the contents of R are replaced by 0's or 1's according as the original contents were positive or negative. The next order is in location &quot;Y&quot;.</td>
</tr>
<tr>
<td>28</td>
<td>((A_n) 32-n (A_{n-32})</td>
<td>As for 26 except that the recording takes place from A and the contents of A are unchanged after recording.</td>
</tr>
</tbody>
</table>
APPENDIX A

The drawings used to construct the M.3 computer are shown on the following pages. Unless otherwise stated, resistors are one-half watt, ± 5%. Capacitors smaller than 2000 pf are ± 5% type CM-15 miniature silver mica. Larger capacitors are electrolytic. A crossed circle (⊗) indicates the location of required breaks in the copper busses of the vero cards.

Wiring conventions used are as follows:

-100 v Blue wire
-12 v Red wire
-6 v Orange wire
+1.5 v Yellow wire
± Black wire
Pulse Carrying White/Green wire
Flip-Flop level White/Red wire

Units are numbered as follows:
1. Counter and Coincidence Senser
2. Accumulator
3. Shift Register
4. Cycle Register
5. Control Register
6. Control
7. Arithmetic Unit
8. Read, Write Circuit
9. Track Selector
10. Block Selector
11. Head Switch.
$s_1, s_2 : 2N1307$
$D_1, D_2 : 1N678$
$D_3, D_4 : 1N678$ unless marked different.

GROUND BUS

$-12V$
$-6V$

12345678910111213141516

16 HOLES

+1.5
+1.5 (ZEROING LINE)
Figure 5.1
Counter and Coincidence Sensor (M.3 Unit 1)
WIRING IDENTICAL TO UNIT 1 CARD 1

COUNTER #4  COUNTER #5  COUNTER #6
Input from digit marker track

Continuous clock 14
From "I" emitter

32 nH

Strobe delay 20

-12 V bus
-6 V bus

Input from digit marker track (com)

Ground bus
1-8-18 1/8
1-7-20 1/8

+1.5 V bus
1-8-4 1/8
1-7-16 1/8
1-6-9 1/8
1-8-21 1/8
32 nH 1-1-3 8-2-15 1/8
-12 V

Output from counter and frequency doubler

S3, S4, S5, S6, S7, S8, S10, S16: 2N1307
S1, S2, S4, S7, S8, S10, S16: 2N1306

D3, D4: 1N67A
W1, W2: W8
D1, D2: 1N273
18 CONTINUOUS CLOCK

S1 + S6 : 2N1336
S7 + S9 : 2N1307
D1 + D4 : 1N41A
W1
W2 : ORANGE

-12V
-6V

1-5-19 W6
1-7-14 W6

+1.5V

0-2-7, 9-13, 1-9 8-1-12 3-15 1-5-19 W6

0-16-3 7-3-15 1-5-19 W6

1-5-20 2-22

-12V 22
Figure 6.7
Accumulator (M.3 Unit 2)
S1, S2: 2N1307
S3, S4: 2N1306
D1, D2, D3, D4, D5, D6: 1N625
W1, W2, W3, W4: W//

NOTE: D100E CHANGE IN BASIC F.F. A1
ALSO THE 300mF CAPACITORS OF A1 GO TO THE 22ND INSTEAD
OF THE 21ST BUS.
- 12V BUS
- 6V BUS
2-D2-9 2-U-19 2-W-3 2-W-4 2-W-5
2-D2-8 2-D2-7 2-W-5
2-D2-6

- 2-6-20 WIR 10
GROUND BUS

+1.5V BUS
ACCUMULATOR ZERO BUS
2-D-4-3 WIR
2-D-4-10 WIR 20

SAME AS UNIT 2 CARD 2
JOB NO. 1.3

Accumulator Assembly Drawings

SHEET NO. 8 OF 15

SHEET OF 79

DATE/REV: 3/6

UNIT 2 CARD 1

SAME AS UNIT 2 CARD Z

12V BUS
6V BUS

2-D3-7 2-B-19 W/R
2-D3-6 W/R
2-D3-5 W/R 5
2-D3-4 W/R

2-B-20 10

GROUND BUS

4.15V BUS

Accumulator Zero Bus
2-6-3 W/R
2-6-10 W/R 20
Accumulator Shift Bus
12V 22
NEON DRIVERS

SAME AS UNIT 2 CARD D1

2-3-5
2-6-4
2-6-3
2-7-6
2-7-5
2-7-4
2-8-6
2-8-5
2-8-4

#21 Acc. Neon Blue
#22 Acc. Neon Blue
#23 Acc. Neon Blue
#24 Acc. Neon Blue 15
#25 Acc. Neon Blue
#1.5 V BUS
#26 Acc. Neon Blue
#27 Acc. Neon Blue
#28 Acc. Neon Blue 20
#29 Acc. Neon Blue
#30 Acc. Neon Blue 22

DATE

PROJECT
UNIT 2
ACCUMULATOR
CARD D3

SHEET NO.
JOB NO.
ASSEMBLY DRAWINGS
M 3
OF 15
NEON DRIVERS

This is all that is required for Unit 2.
The remaining drivers will be used with Unit 4.

Used on Unit 3:
- $S_1, S_2, S_3, S_4, S_5, S_6$: 2N398
- $D_1, D_2, D_3, D_4, D_5$: 1N67A
- $W_1, W_2, W_3, W_4$: Yellow

Remarks:
- C.P. R1 "O": Black
- C.P. R2 "O": Black
- C.P. R3 "1": Yellow

Notes:
- Reg. Neon Blue 15
- Acc. Neon Blue 10
- Acc. Neon Blue 15
- Acc. Neon Blue 10
- Acc. Neon Blue 15
- Acc. Neon Blue 10

Diagram:
- Neons and transistors connected in series and parallel configurations.
- Resistors and diodes indicated for specific components.
- Wiring connections shown for integrated circuit assembly.
S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8; 2N1307
S_9, S_10, S_11, S_12, S_13, S_14, S_15; 2N1306
D_1, D_2, D_3; 1N67A
V_1, V_2
$S_1, S_2, S_3, S_4 : 2N1307$
$D_1, D_2, D_3, D_5, D_6, D_7, D_8 : 1N625$
$D_9, D_{10} : 1N67A$
$W_1, W_2, W_5, W_6 : W/R$
$W_3, W_4 : YELLOW$

基本翻转触发器
19
20

3
10

11
12
13

-12V BUS
-6V BUS
3-DG-1
3-DG-4
3-DS-4
3-DS-5
3-DS-6

SIMILAR TO UNIT 3 CARD 2

C.P. R7 "O" BLACK
C.P. R9 "O" BLACK
GROUND BUS

C.P. R9 "O" BLACK 15
C.P. R10 "O" BLACK
+1.5 V BUS
CLEAR REGISTER BUS
3-2-3 W/R
3-2-10 W/K 20
SHIFT REGISTER BUS
-12V 22

JOE NO. 4 OF 16
PART NO. 1615
SUBJECT UNIT 3
C.R. REGISTER
ASSY NO. 4-3
DRAWINGS
5-27-51
DATE
SERIAL NUMBER 1-3
-12V BUS
-6V BUS

3-D6-2 3-S-19 W/L
3-D6-4 W/L
3-D6-3 W/L 3
3-D6-2 W/L

3-S-20 W/L 10
C.P. R11 "0" BLACK
C.P. R12 "0" BLACK
GROUNDBUS

C.P. R13 "0" BLACK 53
C.P. R14 "0" BLACK
+1.5V BUS
CLEAR REGISTER BUS
3-3-3 W/L
3-3-10 W/L 20
SHIFT REGISTER BUS -12V 22

SIMILAR TO UNIT 3, CARD 2
-12V BUS
-6V BUS
3-D7-3
3-D7-2
3-D7-1
3-DG-6
3-L-2
C.P. R15 "0" BLACK
C.P. R16 "0" BLACK
GROUND BUS
C.P. R17 "0" BLACK
C.P. R18 "0" BLACK
+1.5V BUS
CLEAR REGISTER BUS
3-4-3 W/R
3-4-10 W/K 20
SHIFT REGISTER BUS
-12V 22

SIMILAR TO UNIT 3, CARD 2
-12 V Bus
-6 V Bus
3-D8-5  3-8-19  W/R
3-D8-4  W/R
3-D8-3  W/R B
3-D8-2  W/R

3-8-20  V/R
C.P. R23 "O"  BLACK
C.P. R24 "O"  BLACK
GROUND BUS

C.P. R25 "O"  BLACK
C.P. R26 "O"  BLACK
+15 V Bus
CLEAR REGISTER BUS
3-6-3  W/R
3-6-10  W/R 20
SHIFT REGISTER BUS

SIMILAR TO UNIT 3 CARD 2
SAME AS UNIT 3 CARD 2

C.P. R.27 "O" BLACK
C.P. R.28 "O" BLACK
GROUND BUS
C.P. R.29 "O" BLACK 15
C.P. R.30 "O" BLACK
+1.5 V BUS
CLEAR REGISTER BUS
3-7-3 W/R
3-7-16 W/R 20
SHIFT REGISTER BUS
-12 V 22
**NEON DRIVERS & ISOLATING DIODES**

1. 1
2. 7
3. 15
4. 19
5. 11
6. 20
7. 16
8. 12
9. 3
10. 4

SIMILAR TO UNIT 3 CARD D5

- 3-7-5 w/r 1
- 3-5-9 w/r
- 3-6-9 w/r
- 3-6-6 w/r
- 3-6-5 w/r 5
- 3-6-4 w/r 7
- C.P. R16 "1" w/r
- C.P. R17 "1" w/r
- C.P. R18 "1" w/r
- C.P. R19 "1" w/r 10
- C.P. R20 "1" w/r
- C.P. R21 "1" w/r

GROUND BUS
- #16 REG. NEON BLUE
- #17 REG. NEON BLUE 15
- #18 REG. NEON BLUE
- +15V BUS
- #19 REG. NEON BLUE
- #20 REG. NEON BLUE
- #21 REG. NEON BLUE 20

10 - 20 - 30 - 40 - 50 - 60 - 70 72
Neon Drivers & Isolating Diodes

1 14
2 15
3 16
4 10
5 19
6 20
7 11
8 12
9

Similar to Unit 3 Card D5
Figure 6.6
Cycle Register (M.3 Unit 4)
$S_1, S_2, S_3, S_4, S_5, S_6, S_7 = 2N1307$
$S_8, S_9, S_{10}, S_{11}, S_{12} = 2N1306$
$D_1, D_2, D_3, D_4 = 1N625$
$D_5, D_6, D_7, D_8 = 1N67A$
$W_1, W_2 = V_R$
$W_3, W_4 = W/R$

-12 V Bus
-6 V Bus
1-8-15 V_R
7-5-6 W/R INST E/F
1-6-18 W/R
5-11-10 W/K MEN THE
4-9-3 W/R
4-9-10 W/R
GROUNO BUS
8-1-14 W/K IFF 1
8-1-15 W/K IFF 2
8-1-21 W/K
+15 V BUS

W/6 CYCLE REG SHIF BUS
7-2-18 4-2-19
7-2-194-2-20
-12 V 11

10 24 30 40 50

K.P. 1 70.72
S, = 2N1306
W1, W2, W3, W4, W5, W6 : W/
<table>
<thead>
<tr>
<th></th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>C4</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
</tbody>
</table>

**Diagram**

- 12 V BUS
- 6 V BUS

**Notes**

- Similar to Unit 4
- Card 2

**Ground Bus**

- 4-4-19 WK
- 4-4-20 WK

**Additional Notes**

- 4-2-3
- 4-2-10
- CYCLE REG SHIF BUS
- -12 V 22
-12V BUS
-6V BUS
4-6-17 WKS
4-6-20 WKS
Ground BUS
+1.5V BUS
+1.5V BUS
4-4-3 WKS
4-4-10 WKS
4/6 CYCLE REG. SHIFTS BUSH
-12V BUS
-12 V BUS
-6 V BUS
4-9-19 W/I

4-9-20 W/I 10
GROUND BUS

+15 V BUS
+15 V BUS
4-7-3 W/I
4-7-18 W/I 24
W/CYCLE REG SHIFT BUS

-12 V

SIMILAR TO UNIT 4
CARD 2
DIODES D₁3 : IN67A
DIODES D₁₁ + D₁₂ INCLUSIVE : IN625
W₁, W₂, W₃, W₄, W₅ : W/R
W₆ : YELLOW

-12V BUS
-6V BUS
1-2-85-D11-1
1-2-75-D11-21
1-2-6 5-D10-6 W/6
1-2-9 5-D10-5 W/4
1-2-3 5-D10-21 W/R
1-2-5
5-5-4 W/R
5-5-9 W/R
5-5-6 W/R
5-5-7 W/R
GROUND BUS
5-5-5 W/R
5-5-8 W/R
GROUND BUS
5-1-3 W/R
5-1-10 W/R
GROUND BUS
5-3-22 W/R
1) NEW ROUTING OF W3, W6
2) #22 BUS CUT, AND
   1 & 22 BOARDS ARE
   JUMPERED TOGETHER.
Similar to Unit 3
Card D 5

With exception that an extra diode is added.
SIMILAR TO UNIT 5
CARD D10

GROUND BUS
# 7 CONTROL REG NEON RED
# 8 C.R. NEON BLUE 15
# 9 C.R. NEON BLUE
+1.5V BUS
#10 C.R. NEON BLUE
#11 C.R. NEON BLUE
#12 C.R. NEON BLUE 20
S-2-6 5W
C.P. C.R. 7 B BLACK
SIMILAR TO UNIT 5
CARD D10

S-7 - 4 W/C
S-8 - 4 W/C
S-8 - 5 W/C
S-9 - 5 W/C
S-9 - 6 W/C
S-9 - 6 W/C

C.P. CR 25 1/2" 3/8
C.P. CR 26 1/2" 3/8
C.P. CR 27 1/2" 3/8
C.P. CR 28 1/2" 3/8
C.P. CR 29 1/2" 3/8
C.P. CR 30 1/2" 3/8
GROUND BUS

#25 C.F. NEON BLUE
#26 C.F. NEON BLUE 11
#27 C.F. NEON BLUE
+15V BUS

#28 C.F. NEON BLUE
#29 C.F. NEON BLUE
#30 C.F. NEON BLUE 2A
S-8 - B W/C
C.P. CR 27 6" BLACK 22
FUNCTION TABLE PART I

INPUT TAPE

00010
00100
00110
01000
01100
10000
10010
10100
11000
11010
11100
11110

BRANCH ACCUM

RIGHT SHIFT ON LEFT SHIFT

S1, 2N1306
ALL OTHER TRANSISTORS 2N1307

LEFT SHIFT

Xn,

CLEAR, X -> R

ALL DIODES INGTA.

X -> CYCLE REG.

+12V BUS

GROUND BUS

\[ \begin{align*}
6-1-3 &: 5-12-15 \text{ V} & 5-10-15 &: 5-12-21 \text{ V} \\
6-2-9 &: 2-10-8 \text{ V} & 5-10-16 &: 5-10-18 \\
2-10-4 &: \text{ V} & 5-10-17 &: 5-10-20 \\
7-2-7 &: \text{ V} & 5-10-19 &: 5-10-21 \\
7-2-9 &: \text{ V} & 5-10-22 &: 5-12-21 \text{ V} \\
3-10-4 &: \text{ V} & 5-10-22 &: 5-12-22 \text{ V} \\
4-10-6 &: \text{ V} & 5-10-22 &: 5-12-22 \text{ V} \\
5-10-12 &: \text{ V} & 5-10-22 &: 5-12-22 \text{ V} \\
5-10-14 &: 5-12-16 \text{ V} & 5-10-22 &: 5-12-22 \text{ V} \\
5-10-15 &: 5-12-15 \text{ V} & 5-10-22 &: 5-12-22 \text{ V} \\
5-10-16 &: 5-12-16 \text{ V} & \end{align*} \]

* NOTE: RESISTOR THERE.
### Function Table Part 2

<table>
<thead>
<tr>
<th>Function</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add x to a</td>
<td>10010</td>
</tr>
<tr>
<td>Subtract x from a</td>
<td>10100</td>
</tr>
<tr>
<td>Clear accumulator before adding into or subtract from it</td>
<td>10000</td>
</tr>
<tr>
<td>Record A in X</td>
<td>1110</td>
</tr>
<tr>
<td>Record R in X</td>
<td>1111</td>
</tr>
<tr>
<td>Block of LEDs switch</td>
<td>00001</td>
</tr>
<tr>
<td>Type</td>
<td>00011</td>
</tr>
<tr>
<td>Branch shift register</td>
<td>00111</td>
</tr>
</tbody>
</table>

### Diagram

- **12 V BUS:**
  - 6-1-4 Wk
  - 5-11-11 5-13-11 5/4
  - 5-11-12 5-13-12 5/4
  - Ground bus
  - 5-11-14 5-13-14 5/4
  - 5-11-16 5-13-16 5/4
  - 5-11-18 5-13-18 5/4
  - 5-11-19 5-13-19 5/4
  - 5-11-20 5-13-20 5/4
  - 5-11-21 5-13-21 5/4
  - 5-11-22 5-13-22 5/4

- **4.7 K**
- **22K**
S1 \rightarrow S14 incl: 2N1307
S15, S17: 2N1306
D1, D16, D17, D18, D19, D20: 1N57A
D1 \rightarrow D14: 1N273
W1: yellow
W2, W3: w/g
W4: orange

-12v bus 1
-6v bus
7-2-11 W/8
7-2-12 W/6
8-1-15 W/6
8-1-19 W/6
9-1-15 W/6

Ground bus:
1-6-18 W/6
2-1-8 W/6

+12v bus:
2-1-22 W/7
2-9-5 W/6
2-9-8 W/6

-12v 22

all capacitors 200pF

By DATE

Unit 7 Assembly Diagram
SEE SHEET B-1 FOR LOGIC AND PIN NUMBERS

$S_1 \rightarrow S_6 : 2N1307$
$S_7 \rightarrow S_{12} : 2N1306$
$D_1 : 1N67A$
$D_2, D_3, D_4 : 1N273$
$D_6 : 1N625$
$W_1 : BLACK.$
$S_1, S_2, S_3, S_4, S_5 : 2N1307$
$S_6, S_7, S_8, S_9, S_{10} : 2N1306$
$D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8 : 1N914$
$D_9 : 1N917A$
$W_1, W_2, W_3, W_4, W_5, W_6 : W/R$
$W_7 : W/G$

Diagram:

- 12V Bus
- 6V Bus

To UNIT II CARD

5-1-5 W/R
5-1-8 W/R
5-1-4 W/R
S-1-7 W/R
6-1-6 W/R
GROUND BUS
5-9-5 W/R
5-9-8 W/R

1.5V Bus

5-7-6 W/R
5-9-7 W/R
9-2-26 W/G
Figure 5.6
Head Switch - Block Switch - Read-Write Interconnections
Track Switch Bus
Track # 18

Track Switch Bus
Track # 9

Track Switch Bus
Track # 10

Track Switch Bus
Track # 11

Track Switch Bus
Track # 12

Track Switch Bus
Track # 13

Track Switch Bus
Track # 14

Track Switch Bus
Track # 15

To Heads
On
Magnetic
Drum
Memory
Element.

To Block
Switch

To Read, Write ECTs.
$1 - S_8$ : 2N1307
All diodes! in 273

Drill & Tap similar to opposite end.

Turn on head screw

-12V Input
Ground Input
+1.5V Input

9-2-4
9-2-3
9-2-6
9-2-5
9-1-4
9-1-3
9-1-6

9" Long piece of .016 x 1" 22 AWG copper wire.
S1 → S8 incl.: 241307
ALL DIODES: ING7A
CARD SIMILAR TO
UNIT II CARD 3
BLOCK SELECTOR MATRIX #2

-12V INPUT
GROUND INPUT
+1.5V INPUT

1.0-2-9 wire 7
1.0-1-3 wire 2
1.0-2-8 wire 5
1.0-1-4 wire 4
1.0-2-7 wire 3
1.0-1-5 wire 8
1.0-1-6 wire 1

* THERE IS NO BLOCK #111, BUT THE BLOCK # IS AVAILABLE IF REQUIRED IN FUTURE.

UNIT II CARD 4
BLOCK SELECTOR MATRIX #2
OF HEAD SWITCH
SL - SB incl. 2N574
T2: PRIMARY 8T
  SECONDARY 26T, CT.
15 CARDS REQUIRED FOR
BLOCKS 0000 TO 1110

S1 → S8: EN594
T2: PRIMARY BT
SECONDARY BT 0T

TAP CENTRE OF ROD TO
ACCEPT 1/8" LONG
#4-40 SCREW

1/4 × 1/2" ALUMINUM BAR,
5" LONG

.15" PITCH VEEBOARD,
24 STRIPS,
5" LONG
$S_1 \rightarrow S_5$ Incl : 2N1304
$S_6 \rightarrow S_{10}$ Incl : 2N554

$T_3$ : Primary 24 T C.T.
Secondary 26 T C.T.
CONSTRUCTION
SIMILAR
TO
BLOCK SELECTOR #2

RETURN ON BLOCK 9101
RETURN ON BLOCK 0110
RETURN ON BLOCK 0111
RETURN ON BLOCK 1000
RETURN ON BLOCK 1001
+1.5V

-1.7 to -1.5V

TO READ
SITE C.C.T.
CONSTRUCTION SIMILAR TO BLOCK SELECTOR #1

TO OUTPUT FROM BLOCK 1010 TO OUTPUT FROM BLOCK 1011 TO OUTPUT FROM BLOCK 1100 TO OUTPUT FROM BLOCK 1101 TO OUTPUT FROM BLOCK 1110