DIGITAL PICTURE STORAGE FOR TELETEXT DECODING

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BY
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SASKATOON, SASKATCHEWAN.
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DIGITAL PICTURE STORAGE FOR TELETEXT DECODING

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ABSTRACT

The recent advance in digital memory technology makes it possible to introduce Field Memories in television receivers. This type of memory can store a complete picture which allows a number of new features to be added to a television receiver. Teletext and still video reception are such features and are the focus of this thesis.

This thesis describes a low cost digital field memory to be used in conjunction with the T.V receiver to facilitate Teletext reception. Considerations involved and the design of an experimental system are described. Tests to evaluate the performance of the experimental system are discussed and results presented. To familiarize the reader with the topic, some background information on Teletext and Television is also provided.
Table of Contents

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ABSTRACT

Table of Contents

List of Figures

1. Introduction

2. Background Information

2.1 Introduction
2.2 General Concepts
2.3 Graphic Display Systems
  2.3.1 Vector Graphic Systems
  2.3.2 Raster Graphic Systems
2.4 Decoding Schemes
  2.4.1 Alpha-Mosaic Systems
  2.4.2 Alpha Geometric systems
  2.4.3 Alpha-Photographic System and the Proposed System
2.5 Comparison of the Telidon System and the Proposed System

3. CONVERSION

3.1 Composite Video Signal
3.2 Coding
  3.2.1 Nyquist and Sub-Nyquist Encoding
  3.2.2 Coding Schemes
  3.2.3 Signal To Noise Ratios of LPCM, DPCM and DM
  3.2.4 Comparison of DM and DPCM with LPCM
  3.2.5 Video Encoding Methods and Encoding Rate
3.3 Digitization Techniques
3.4 Choice of the Converter
3.5 Digital To Analog Conversion

4. Video Codec Implementation

4.1 Video Codec as a Part of a TV Receiver
4.2 Implementation of the Encoder
  4.2.1 Input Video Amplifier
  4.2.2 A/D Converter
4.3 Implementation of the Decoder
  4.3.1 D/A Converter
  4.3.2 Output Stage
4.4 Implementation of the Memory Interface
  4.4.1 Driver Latch
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4.2 Deglitcher Latch</td>
<td>90</td>
</tr>
<tr>
<td>4.5 Clocking</td>
<td>91</td>
</tr>
<tr>
<td>4.6 Construction Technique</td>
<td>93</td>
</tr>
<tr>
<td>4.7 Power Supplies</td>
<td>96</td>
</tr>
<tr>
<td>5. Implementation of The Digital Field Memory</td>
<td>99</td>
</tr>
<tr>
<td>5.1 Memory Requirements</td>
<td>99</td>
</tr>
<tr>
<td>5.2 Overview of Memory Design</td>
<td>101</td>
</tr>
<tr>
<td>5.3 Storage Memory</td>
<td>107</td>
</tr>
<tr>
<td>5.4 Input Buffers</td>
<td>110</td>
</tr>
<tr>
<td>5.5 Output Buffers</td>
<td>112</td>
</tr>
<tr>
<td>5.6 Logic Controller</td>
<td>112</td>
</tr>
<tr>
<td>5.6.1 Control Sequencer</td>
<td>112</td>
</tr>
<tr>
<td>5.6.2 Output Data Sequencer</td>
<td>115</td>
</tr>
<tr>
<td>5.6.3 Address Generator</td>
<td>116</td>
</tr>
<tr>
<td>5.6.4 Read/Write Control Logic</td>
<td>119</td>
</tr>
<tr>
<td>5.6.5 Sync Detector</td>
<td>122</td>
</tr>
<tr>
<td>5.7 Interface Buffers</td>
<td>126</td>
</tr>
<tr>
<td>5.8 Bypass Circuit</td>
<td>127</td>
</tr>
<tr>
<td>5.9 Phasing Circuit</td>
<td>128</td>
</tr>
<tr>
<td>5.10 Construction Technique</td>
<td>130</td>
</tr>
<tr>
<td>6. PERFORMANCE TESTING</td>
<td>132</td>
</tr>
<tr>
<td>6.1 Amplifier Tests</td>
<td>133</td>
</tr>
<tr>
<td>6.2 D/A Converter Tests</td>
<td>136</td>
</tr>
<tr>
<td>6.3 Video Codec Tests</td>
<td>137</td>
</tr>
<tr>
<td>6.4 Digital Field Memory Tests</td>
<td>149</td>
</tr>
<tr>
<td>6.5 Discussion of Results</td>
<td>150</td>
</tr>
<tr>
<td>7. Conclusions</td>
<td>165</td>
</tr>
<tr>
<td>REFERENCES</td>
<td>169</td>
</tr>
<tr>
<td>I. APPENDIX 1</td>
<td>171</td>
</tr>
<tr>
<td>I.1 Data Sheets</td>
<td>171</td>
</tr>
<tr>
<td>II. APPENDIX 2</td>
<td>202</td>
</tr>
<tr>
<td>II.1 Circuit Schematic of the Video Codec</td>
<td>202</td>
</tr>
<tr>
<td>II.2 Circuit Schematic of the Logic Controller</td>
<td>202</td>
</tr>
<tr>
<td>II.3 Photograph of the Circuit Built</td>
<td>202</td>
</tr>
<tr>
<td>III. APPENDIX 3</td>
<td>206</td>
</tr>
<tr>
<td>III.1 Timing Diagram for the Digital Field Memory</td>
<td>206</td>
</tr>
</tbody>
</table>
vi

List of Figures

Figure 2-1: Teletext System 9
Figure 2-2: Videotex System 9
Figure 2-3: Existing Teletext System 11
Figure 2-4: Proposed System 12
Figure 2-5: Bit-Mapped Display 15
Figure 2-6: Character Oriented Display 16
Figure 2-7: General Telefield decoder 18
Figure 2-8: Picture Construction in an Alpha-Mosaic System 20
Figure 2-9: Character Oriented Telidon Decoder 23
Figure 2-10: Bit-Mapped Telidon Decoder 24
Figure 2-11: Proposed System Decoder 25
Figure 3-1: Electron Beam Scanning 31
Figure 3-2: One Line of a Video Signal 33
Figure 3-3: Vertical Synchronising Pulse 33
Figure 3-4: Frequency Allocation in a NTSC TV Channel 36
Figure 3-5: Composite Color Video Signal 39
Figure 3-6: Sub-carrier Phase in a Field 40
Figure 3-7: Spectrum of a PAM Signal 44
Figure 3-8: Foldover Distortion 44
Figure 3-9: Spectral Distribution of a NTSC Video Signal 46
Figure 3-10: Spectrum of a Sub-Nyquist Sampled NTSC 46
Figure 3-11: Comb Filter Response 48
Figure 3-12: LPCM Quantization noise 51
Figure 3-13: Slope Overload Distortion 52
Figure 3-14: Video Frequency Energy Distribution 57
Figure 4-1: Video Codec Block Diagram 66
Figure 4-2: Video Codec Implementation in TV Receiver 68
Figure 4-3: Input Video Amplifier 71
Figure 4-4: Schematic of CA3300 73
Figure 4-5: Timing Diagram of CA3300 73
Figure 4-6: A/D Converter Circuit 75
Figure 4-7: Errors Due To Improper References 78
Figure 4-8: Tracking Amplifier 80
Figure 4-9: Decoder of the Video Codec 82
Figure 4-10: Output Stages 85
Figure 4-11: Driver Latch 90
Figure 4-12: 14.32MHz PLL Oscillator 93
Figure 4-13: 3 - Phase Clocks 93
Figure 4-14: 5-15V Regulated Supply 97
Figure 5-1: Schematic of Digital Field Memory 101
Figure 5-2: Memory Write 103
Figure 5-3: Memory Read 103
Figure 5-4: A Single Memory Bank 107
Figure 5-5: Input Buffer Arrangement 110
Figure 5-6: Input Buffer Clocks 110
Figure 5-7: Output Buffers 112
Figure 5-8: Output Buffer Clocks 112
Figure 5-9: Control Sequencer Logic 112
Figure 5-10: Control Sequencer Timing 112
Figure 5-11: Output Data Sequencer
Figure 5-12: Address Generator
Figure 5-13: Read/Write Control Logic
Figure 5-14: Memory Read/Write Timing
Figure 5-15: Generation of Read/Write Signal
Figure 5-16: Sync Detector
Figure 5-17: Separation of Vertical Sync
Figure 6-1: Video Amplifier Troubles
Figure 6-2: D/A Conversion Errors <3 Bits>
Figure 6-3: D/A Converter Test Circuit
Figure 6-4: D/A Converter's Response to Test Input
Figure 6-5: Linearity Test
Figure 6-6: Polar Display of Vector Monitor
Figure 6-7: Line Display of Vector Monitor
Figure 6-8: Modulated Staircase Signals
Figure 6-9: FullField Color Bar Signal
Figure 6-10: Errors in Color Picture
Figure 6-11: Display of Stored Color Bars
Figure 6-12: Display of Color Bars <Direct>
Figure 6-13: Display of Color Bars Thru Video Codec
Figure 6-14: Display of Stored Monochrome Bars
Figure 6-15: Display of Monochrome Bars <Direct>
Figure 6-16: Display of Monochrome Bars Thru Video Codec
Figure 6-17: Vectorscope Display for FullField Color Bar Test
Figure 6-18: Vectorscope Display for Differential Phase Test
Figure 6-19: Display of Stored Color Picture
Figure 6-20: Display of Color Picture <Direct>
Figure 6-21: Display of Color Picture Thru Video Codec
CHAPTER 1

INTRODUCTION

This thesis proposes a new information system which utilizes the ubiquitous television receiver. Much of the technical work described relates to the standardized properties of the television receiver.

Over the past three decades television has had a profound cultural impact on society. Television seems to have a virtual monopoly in home entertainment. On an average the home TV set, in the U.S, is switched on for 45 hours a week, while the telephone is used for less than 3 hours a week, [4]. Similar statistics on the usage of TV in other nations can be perceived without exaggeration. Today, television seems to have gained precedence over residential necessities such as refrigerators and telephones, amongst the economically poorer sections of the population.

Black and white receivers were introduced in 1946. A decade later the first color TV system (NTSC\(^1\)) and color receivers were developed. Twenty seven years later there has been little change in the underlying concept of color television; but there has been vast technological improvement in the design of the TV receiver. The

\(^{1}\)NTSC-National Television System Committee
advancement of the semiconductor industry is responsible for this technological improvement. The first black and white TV receivers had as many as 30 vacuum tubes [12]. Color TV receivers were more complex and had a few more vacuum tubes. Today, a single integrated circuit has been developed to provide all the video processing circuit functions for a black and white TV set and for the more complex color receivers two integrated circuits provide all the video processing circuit functions. This improved technology provides low cost TV sets making it affordable to almost everyone.

The TV receiver has several applications other than merely providing a medium for watching broadcast entertainment, although this is its main use. Two important applications of the receiver include its use as a display medium for home computers and video games. Since most homes have a TV receiver, no additional cost is incurred for a display medium for both home computers and video games. Another useful application of the TV receiver is in its use as a home information system. The service called Teletext allows subscribers to receive news, stock quotations, weather reports, sports information, entertainment information, travel information etc., through the home TV receiver. Of course, a separate unit which interfaces to the existing TV receiver is necessary to facilitate reception and display of this Teletext information. The TV receiver
merely serves as a display medium. The purpose of this project is to design and build such a unit, that facilitates reception of Teletext using a home TV receiver.

With the advancement of semiconductor integrated circuits, digital technology is replacing analog techniques in many areas. In television transmission and reception analog methods have predominated until recently. Digital television was motivated by the need to improve picture quality, to reduce costs and to add new features and services.

Picture quality in analog transmission is degraded by noise, non-linearity, variable gain and delay in the transmission medium. Noise and non-linearity have a cumulative effect when the signal passes through two or more transmission links. Degradation in digital television can be essentially limited to the encoding process and therefore impairments are not cumulative. Digital signal processing of encoded signals allows reconstruction of better quality pictures on the TV screen. This signal processing is assisted by digital storage techniques. Some examples of using digital storage in TV applications are mentioned below.

A comb filter can be used for picture enhancement. These filters employ filter algorithms that require the use
of two TV raster scan lines (the current and a previous line). The previous line is made available by storing it in memory.

Adaptive filtering is used to remove noise on TV lines. This requires storage of TV lines for which digital memory is used.

Full TV picture fields can be stored and displayed at twice the rate of normal display used for broadcast TV. This helps eliminate large area flicker normally perceived on the TV screen.

There are many more TV applications in which digital memories and other digital elements are used. It is perceived that the next major technological advance in commercial TV receivers will be the introduction of low cost memories in the receiver to store a complete field or frame of a TV signal. This memory would be used to FREEZE a TV picture (field or frame). An application of such a storage memory would be in Teletext reception.

The topic of this thesis is the design of a Telefield decoder which can display text, graphics and picture information on a T.V receiver. In a Teletext system the information to be sent to the user is encoded as standard TV signals. A page of information is carried by each TV field,
A TV broadcast station will broadcast several hundred pages of Teletext information (TV fields), in a cyclic manner. At the users' premises the broadcast pages are captured and displayed on a normal TV receiver. The pages transmitted are numbered and hence with the use of a simple keypad a particular page of information may be singled out for selection and display. The Telefield decoder captures a single page of Teletext information and displays it on a TV receiver screen.

The manner in which Teletext reception is performed by the proposed Telefield decoder is as follows: The selected page of information is digitized and stored in memory. Once stored the page can be displayed by repeatedly reading it out of the memory and reconverting it to an analog TV signal, to be displayed on the television receiver. By repeatedly reading and displaying the memory contents every sixtieth of a second an illusion of a still picture is seen on the TV screen. This rate is a standard in the NTSC system and is based on the persistence of vision.

The Telefield decoder comprises two functional units. A unit called a Video Codec, that digitizes and codes the incoming Teletext information and also decodes the stored Teletext information, for display on a TV receiver. Codec is an acronym for CODer-DECoder. The second unit is a Digital Field Memory that stores the encoded Teletext
information. The Telefield decoder is to be incorporated in a commercial TV receiver. Thus, the clientele is the general public. A unit designed for the general public must be low priced and simple to operate. Most existing equipment available for Teletext and Videotex reception is rather expensive for the average person. Designing an affordable (low cost) alternative was one of the principal factors that motivated the attempt of this project.

In summary, the object of the work done in this dissertation comprises the design and implementation of a low cost Telefield decoder, to be used in conjunction with a conventional TV receiver to facilitate reception of Teletext information. This information may comprise text, graphics and pictures in color or black and white. The premise made is that pages of information are broadcast, from a database, for capture and display.

The thesis is organized as seven chapters. Chapter-2 provides background information related to Teletext and Videotex and elicits some advantages of the proposed system over existing methods. Chapter-3 describes the salient features of a TV signal, the type and methods of conversion involved, and coding schemes. Chapter-4 describes the implementation of the Video Codec. Chapter-5 deals with the requirements and implementation of the Digital Field Memory. Chapter-6 describes tests used to check the performance of
the system implemented and presents the results of tests pictorially. Chapter-7 concludes the work done and makes suggestions on the scope for future work.
CHAPTER 2
BACKGROUND INFORMATION

2.1 Introduction

Teletext and Videotex systems primarily designed to serve as information banks to be accessed by the general public are gaining increasing attention as they have introduced a new dimension to communication technology. These systems offer facilities such as news, weather reports, advertising, electronic telephone directories, performing business transactions such as buying and selling, electronic banking etc., through the medium of the home TV receiver. Information from the data base may be transmitted to the user via different communication media and different communication technologies. Examples are analog telephone networks, circuit switched and packet switched networks, like DATAPAC, the coaxial cable system and standard TV broadcast system. The method and mode of sending information from the information source to the users is the underlying difference between Teletext and Videotex systems. Before proceeding to discuss various Teletext and Videotex systems it is prudent to explain these terms, [3]:

Teletext is a computer system that allows users to select and display pages of information, which are broadcast or transmitted by cable, on their TV screens. In a Teletext system users are not individually connected to the central computer system. Pages of information are not sent on request. Instead, a number of pages containing information, called frames, are broadcast in a cyclic manner. The user can select any
frame as it comes by in the broadcast cycle; display it and then select another frame. In this system the information is transmitted as in Television, hence the name Teletext. As users are not connected to the information source the system is unidirectional. Further, a system affording Teletext facilities need not be computerized as will be evident from the description of the system proposed in this thesis.

Figure 2-1: Teletext System

Videotex is a computer system that allows selection and display of information on T.V screens as with Teletext. However, in a Videotex system each user is individually connected to the information source (host computer) via a telephone pair or cable. It also affords interactive capabilities whereby the user can communicate with the host computer system and other computer systems in the network and perform activities such as playing games, performing business transactions etc. Videotex is therefore a bidirectional system.

Currently there are three popular Videotex systems vying for acceptance, by CCITT\textsuperscript{2}, as an international

\textsuperscript{2}International Telegraph and Telephone Consultative Committee
standard. These three systems are PRESTEL(U.K), ANTOIPE(France) and TELIDON(Canada), [2]. Antiope and Telidon support both Videotex and Teletext and are referred to as videotex systems. Prestel supports only Videotex. Britain has in operation two popular Teletext systems called CEEFAX and ORACLE [4]. CEEFAX and ORACLE are considered to be technologically outdated as they were introduced in 1973 and 1976 respectively and are not discussed in this thesis.

Videotex and Teletext are public information systems. The principal difference between these systems is the way information is delivered to the user. Videotex systems use telephone lines or cable, while Teletext systems may broadcast information through the atmosphere, like Television transmission. Videotex systems require interactive (bidirectional) facilities, while Teletext is a unidirectional system. Except for this difference the two systems are similar, in that the components making up the information systems are the same. Both systems require an
information base to store and send information to the user. At the users premises a device is required to receive the transmitted information and display it for the user. Videotex, however, offers additional facilities over Teletext by virtue of its interactive capability.

In the following section we shall describe the system concepts of Prestel, Antiope, Telidon Videotex systems and the proposed Teletext system.

2.2 General Concepts

The Prestel, Antiope and Telidon systems comprise three essential components as indicated in Figure 2-3. The host computer serves as a data base which stores, maintains and communicates encoded information to the users. The TV screen or a special purpose terminal is the display medium for the user. The decoder serves to interpret the encoded information communicated from the host computer and produces suitable signals for display on the TV screen. The information that is displayed can be broadly categorized as text and graphics or pictures. The Prestel, Antiope and Telidon systems differ primarily in the way in which they encode this text and graphic information, which is stored and transmitted upon request, and the way in which they decode and display, this information, at the user premises.

Figure 2-4 illustrates the proposed Teletext system. Once again, there are three essential components; an
information source, a decoder and a display medium. The decoder is essentially a TV field selector and store and has been called as a Telefield decoder. The field referred to is a NTSC TV signal field. The display medium is a TV receiver. The information source is a TV broadcast station which scans, sequences and broadcasts pages of information to be selected, decoded and displayed. The messages can also be sent via cable, to the user premises.

The Telefield decoder receives and decodes the received Teletext information, which is then displayed on a TV receiver screen. With Teletext decoding in focus, the components of interest are the display system and the decoding scheme.
2.3 Graphic Display Systems

Graphic display systems are broadly classified as Vector and Raster graphic systems. Each of these systems and their characteristics are described hereunder.

2.3.1 Vector Graphic Systems

The display medium is a cathode ray tube (C.R.T). Pictures or graphics are displayed as being made up of a number of straight lines. The lines are drawn in a continuous fashion by directly controlling the position of the electron beam from the electron gun. Further, the lines can be drawn in any direction, not only horizontally as in raster systems. Thus, in these systems picture and text information are reproduced by directly controlling the position of the electron beam in the C.R.T, in response to the received picture or text information. Therefore vector
graphic systems require a complex display generator that will translate received picture or text information into beam positions on the C.R.T. As a result, these systems are rather expensive for domestic use.

Further, as the home TV receiver cannot be used for such display, the vector graphic system is unattractive for commercial Teletext and Videotex. However, an advantage of vector graphic systems is that they provide very high resolution.

2.3.2 Raster Graphic Systems

This is the system employed, for display, in Videotex and Teletext systems. Raster graphics is based on the principle of picture reproduction in TV receivers. TV receivers employ a C.R.T tube for display. The electron beam scans the screen from left to right and top to bottom just as we read a page. The scanned area is termed a raster or a frame. A picture is created by varying the intensity of the scanning beam in accordance with the amplitude of the received picture signal, producing on the screen spots of light and shade in a pattern that resembles the original image. Pictures are refreshed every thirtieth of a second. The raster can be thought of as a matrix of picture elements referred to as pixels or raster units. There are typically about 210,588 (483 horizontal lines with 436 pixels per line) pixels that make up a single frame or picture in the NTSC system, [1].
Raster graphic systems can be further categorized as bit-mapped and character-oriented systems. In a bit-mapped system, each pixel on the TV screen is associated with an addressable location of a display memory. Each memory location will contain the information to be displayed at the corresponding pixel position on the TV screen. A hardware unit, called the display generator, scans the memory locations at the same rate at which the TV screen raster is scanned. During this scan the contents of the memory are read out and displayed at the corresponding pixel positions. In the bit-mapped systems as the picture to be displayed changes so will the memory contents. This is, thus, called a dynamic system and the display memory used is a random access memory (RAM). This system requires a considerable amount of display memory but provides fairly high resolution. Figure 2-5 is a schematic representation of a bit-mapped display system.

In character oriented systems a character generating read only memory (ROM) and a display RAM are used as the display memory. The character generating ROM contains fixed characters or graphic symbols. Each memory location of the ROM contains a fixed pattern of a character or symbol. Unlike the bit mapped system, these memory locations are not associated with any particular pixel position on the screen. The ROM contents can be displayed at any position on the screen. The display RAM is used to store codes that
represent the characters or symbols stored in the ROM. These codes are nothing but the addresses of the ROM locations containing the patterns of the characters and symbols that are finally displayed. For example, to display the word "TART", the ROM locations containing the characters T, A, and R are addressed sequentially by placing appropriate codes in the display RAM. These characters are then read out of the memory and converted into a suitable form for display on the screen at the appropriate pixel positions, by a hardware unit (display generator). Figure 2-6 is a schematic representation of a character oriented display system.

The display RAM in the character oriented system stores only codes representing the characters, whereas the display
Figure 2-6: Character Oriented Display

RAM in the bit-mapped system stores the actual pixel values. Thus a much smaller display RAM is required by the character oriented system. For example, if the code length is 6 bits, then the code contained in a single RAM location of the character oriented system can represent 64 element locations in the character generating ROM. In a bit-mapped system, however, we would require 64 individual RAM locations for a similar display.

Graphics are displayed on the screen as a combination of elementary symbols. Thus character oriented systems produce poor resolution graphics as they have only a limited set of codes of graphic symbols, that can be put together to form a picture. This limited set of symbol codes arises from the impracticality of having millions of codes to
represent every possible symbol configuration. This impracticality has led to the use of a limited set of codes and hence coarse graphics.

2.4 Decoding Schemes

The decoder in all the systems under consideration comprises three essential parts as shown in Figure 2-7 and are listed below:

1. The Interpreter
2. The Display memory and
3. The Video generator

The interpreter, interprets incoming data from the information source and generates raster point information which is stored in the display memory. This raster point information is simply the information to be displayed at each pixel position on the TV screen. The video generator converts the stored raster point information into appropriate scan line information for display on the TV screen. The Prestel, Antiope and Telidon systems employ different schemes for coding graphic information. The display schemes are basically variations of the raster display scheme and are categorized as alpha-mosaic, alpha-geometric and alpha-photographic schemes. The decoders of the three systems are implemented in divers manners.
2.4.1 Alpha-Mosaic Systems

The Prestel system employs an alpha-mosaic scheme to define and display text and graphics. Alpha refers to text, which is transmitted in ASCII\(^3\). Mosaic refers to the way in which pictures are constructed. Each picture is treated as a mosaic of elementary graphic symbols. Each character position of the screen is divided into a 3 by 2 matrix. A TV screen contains 960 (24 by 40)\(^4\) such character positions.

\(^3\)American National Standard Code for Information Interchange

\(^4\)For the European TV systems
positions, as there are 24 horizontal lines each containing 40 characters per line, in each TV frame. This provides a resolution of 72 by 80 elements per frame. To create pictures, graphic symbols are transmitted in place of characters to fill portions of each defined 3 by 2 dot matrix on the screen. A combination of these elementary symbols generates a picture as illustrated pictorially below in Figure 2-8. This display scheme is essentially a character oriented scheme.

![Figure 2-8: Picture Construction in an Alpha-Mosaic System](image)

The Antiope system uses a modified version of the technique employed by its forerunner, the Prestel system. Text as before is transmitted in ASCII and displayed as in the Prestel system. For graphics an additional feature is provided to enhance the alpha-mosaic scheme. A fixed number of user defined picture elements or graphic symbols can be downloaded and stored in the system. These symbols can then
be recalled and displayed when required. The symbols stored in the memory can be of good resolution and hence the Antiope system produces smoother pictures than the Prestel system. This is referred to as dynamic redefinition of characters and the additional symbols are called as a dynamic reconfigurable set [4].

The following inherent disadvantages make the Prestel and Antiope systems somewhat unattractive for Teletext:

1. Resolution of graphics on a TV screen is poor and coarse. Each raster or frame consists of 24 lines with 40 characters per line. Since each character is subdivided into a 3 by 2 matrix we have an effective 72 by 80 matrix of pixels covering the entire screen. These 960 pixels are rather small in number resulting in coarse graphics. This is especially evident when we compare this system with the resolution capability of a NTSC TV set which comprises 210,588 pixels per picture frame. Higher resolution terminals can be used employing a larger number of character positions per screen (40 by 80) with each character defined as a 4 by 2 dot matrix, resulting in a resolution of 25,600 pixels per frame. These terminals require faster, more complex circuitry and processing requirements and would be expensive.

2. The information encoded in the data bank is done in a terminal dependent manner. For example, a page of information may be defined as containing 960 (24 by 40) characters with each character made up of a 3 by 2 mosaic. This allows a resolution of 72 by 80 elements. Hence if a higher resolution terminal is used as the display medium a higher resolution page must be stored in the data bank. Thus, the data bank must support multiple versions of the same page which would be

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[5] for the European TV systems; PAL and SECAM
very expensive.

2.4.2 Alpha Geometric systems

The Telidon system employs the alpha-geometric technique of defining text and graphics. As before alpha refers to text which is represented in ASCII format, while, graphics or pictures are described in terms of five basic geometric shapes. These five geometric shapes are a POINT, LINE, ARC, RECTANGLE and POLYGON. These basic geometric shapes together with picture attributes (color, shading) and environment attributes are encoded into terse 8-bit byte Picture Description Instructions (PDI). These PDIs are stored in the host computer. Upon request these PDIs are transmitted as a sequence of control words, command words and high resolution data words. The control words set up picture and environment attributes, while, the command words instruct the drawing of a geometric figure based on co-ordinates specified in the succeeding data bytes.

A microprocessor is used as the interpreter in the decoder. It interprets the PDIs and does simple tasks such as parity checking, masking extra bits to the desired terminal resolution and generating an output to the display memory. The display memory may be character oriented or bit-mapped; the former providing a lower resolution as it employs an alpha-mosaic display scheme. The two decoding schemes are illustrated, in Figure 2-9 and Figure 2-10.
When a character oriented memory is used the microprocessor interprets the PDIs and places an appropriate address in the character oriented memory. The contents of the character oriented memory addresses a location in either of the two ROMs containing alphanumerics or graphic symbols. The character oriented memory is scanned sequentially at the TV horizontal line scan rate and information is read out for display by the video generator circuitry.

![Diagram of Character Oriented Telidon Decoder](image)

**Figure 2-9: Character Oriented Telidon Decoder**

In the bit-mapped system a display generator receives instructions from the microprocessor and places raster point information in the display memory locations. Thus, the use of a display generator that addresses and stores the raster point information in the display memory, allows the microprocessor more time for processing PDIs. As before the display memory is scanned sequentially at the line rate to
generate a display. This is done by the video generator circuit.

Both the character oriented and bit-mapped systems have an input RAM buffer to equalize the rate at which the PDIs are received and the rate at which the microprocessor interprets and implements the PDI codes.

![Diagram of BIT Mapped Display System]

Figure 2-10: Bit-Mapped Telidon Decoder

2.4.3 Alpha-Photographic System and the Proposed System

The Telidon system has the feature of providing an alpha photographic mode when graphic images cannot be described by a practical number of geometric shapes. In the alpha-photographic mode, referred to as the BIT MODE in Telidon, an image is encoded and stored in a point by point or facsimile form. Each pixel in this image is transmitted to the decoder which is bit mapped as shown in Figure 2-10.
The alpha-photographic scheme is also employed in the decoder (Telefield decoder) of the proposed system, which is illustrated in Figure 2-11. In the proposed system the information is encoded as a TV signal. This signal when received at the decoder is digitized by a front end A/D converter serving as the interpreter. This digitized data is stored in a memory, point by point. The memory is similar to a bit-mapped memory. A D/A converter circuit serves as the video generator and converts the data read out of the memory into a TV signal for display on a TV screen. The A/D and D/A converters comprise the Video Codec while the memory is a Digital Field Memory.

Figure 2-11: Proposed System Decoder
2.5 Comparison of the Telidon System and the Proposed System

The two main advantages of the Telidon system over the proposed system are:

1. Pictures or graphics are encoded in a manner independent of the information access methods, the communication medium and display terminal resolutions. Thus, the introduction of new sophisticated high resolution terminals do not require any changes in the data base. However the decoder needs to be modified, in that a larger display memory is required for higher resolution terminals. This is because a higher resolution terminal has more pixel positions and hence the bit-mapped memory must have correspondingly increased memory locations. Such is also the case with the proposed system.

2. The PDIs are tersely encoded and are economical in storage and transmission. Bandwidth is also conserved and a wide bandwidth as required by TV signals is not required. In the proposed system since the messages are sent as a TV video signal the resolution is dependent on the bandwidth of the TV signal, which places it at a disadvantage when compared with the Telidon system.

The major disadvantage of the Telidon system is the cost entailed in its implementation. These costs include hardware and software costs. Hardware costs relate to the host computer, which must be a main-frame, and the terminal (decoder). When Telidon decoders are integrated in TV receivers the costs will perceivably drop but currently this is a major disadvantage. Software costs include the cost of the operating system, the data base system, information page creation and update costs, all of which are considerable.
The proposed system appears to have the following attractive features, for Teletext reception over the other systems discussed:

1. No change is required in the distribution network, since all information is transmitted as TV signals and the existing TV distribution network which is well established will suffice. Telidon, on the other hand employs distribution via cable (TV) or telephone pair and this requires additional interface units at the user end. Even in the TV broadcast mode, reception with a Telidon decoder requires additional interface equipment to extract the PDLs from the TV signal.

2. No major changes are required in the transmission mode or the stations as the information is sent as a TV signal.

3. Compatibility with present day sets and future digital sets. The introduction of the decoder does not require any change in the TV receiver design. The decoder is merely an auxiliary unit which can be attached to augment the TV receiver for Teletext reception. The TV receiver can display in color, text and graphics with medium resolution sufficient for commercial viewing. High resolution terminals are not required.

4. Telidon decoders have not been integrated in domestic TV receivers to receive Teletext. Instead separate terminals are used. These terminals and decoders containing a microprocessor, memory, a stored program and the display equipment entail a considerable cost. On the other hand the proposed decoder is designed to be connected in the TV receiver without any modifications whatsoever to the receiver. Further the circuitry is simple and is kept a minimum as the TV receiver in which it is to be incorporated affords many of the signal processing functions which would otherwise have been necessary to accomplish with the Telefield decoder, as in the Telidon decoder. This affords considerable cost saving.

The following points relate more to a comparison of Teletext and Videotex systems. It has been included to bring out two
important advantages of Teletext systems over Videotex systems rendering them very attractive for receiving messages from an information source.

1. The number of users do not impose restrictions on the proposed system. However as the number of pages broadcast cyclically increases the user has to wait longer for a page to reappear in the broadcast cycle. Telidon, as a Videotex system, is an on-line system and hence if there are a number of users accessing the data base the response will be slow. This may be alleviated by using large input buffers, to store several pages of information in the decoder terminals, each time the data base is accessed. This technique will result in added cost and complexity to the Telidon decoder.

2. In a Videotex system as telephone lines are used for interactive communication an additional cost of paying the telephone company for use of its facilities, is incurred by the user. Teletext on the other hand requires no such payment as messages are transmitted as with TV. This is an important point as observed in the British experience of Teletext versus Videotex, [4].

As a final note it may be added that the above comparison of the Telidon system and the proposed system is valid while considering the systems for reception of Teletext alone. The Telidon system is a highly sophisticated system and offers many more capabilities than mere Teletext and a consideration of all its present features and the future possibilities indicate a superior system. Each system in this chapter has its merits and de-merits and a particular application will warrant the use of the best suited system. From the point of view of Teletext decoding, the proposed system seems to afford a
cost advantage and simplicity in introduction over the other systems discussed.
CHAPTER 3
CONVERSION

In the proposed system, information is transmitted as a video signal. At the users premises this signal is digitized or encoded by Linear Pulse Code Modulation and stored in a Digital Field Memory. The memory is designed to store a complete field of the incoming composite video signal. The stored image is repeatedly read out of the memory and reconverted into an analog video signal for display on the TV screen. The reconversion is referred to as decoding.

This chapter discusses the encoding and decoding of the composite video signal. Prior to discussing the design and implementation of the Video Codec, performing the encoding and decoding, it is prudent that we consider the signal that is to be encoded, the coding scheme employed and the digitization technique adopted. These aspects lay the foundation of the proposed design.

3.1 Composite Video Signal

A signal to be encoded has to be digitized and coded. The signal in contention is the NTSC composite video signal, which is the carrier of the Teletext information in the proposed system. The nature of this signal and its salient characteristics such as bandwidth, amplitude variations, effects of frequency and phase distortion are described in this section. Important design aspects such as
preprocessing and signal conditioning requirements [amplification and filtering], sampling rate and speed criteria to be met by the codec circuitry can be deduced from the nature and characteristics of the NTSC composite video signal. The description of the composite video signal has been restricted to only those aspects pertinent to providing information for the design adopted.

The salient characteristics of the NTSC composite video signal are described hereunder, beginning with the manner in which pictures are recreated on the T.V screen. Figure 3-1 illustrates the scanning process used to recreate pictures on a T.V set screen.

Figure 3-1: Electron Beam Scanning
(adapted from [12])

Picture creation on the T.V screen is accomplished by electron-beam scanning. This is a raster graphic process in
which the beam of an electron gun is made to scan the screen from left to right and top to bottom producing a series of horizontal lines one below the other. On reaching the end of a line the electron beam rapidly returns to the left hand side to begin scanning the next line. This rapid return is referred to as the retrace period. During this short period the screen is not illuminated and hence no picture information is visible.

Television pictures are transmitted and displayed as frames. Each frame has 525 horizontal scan lines. These frames are displayed at a rate of 30 per second. At this rate, the human eye perceives a flicker of brightness and darkness as the screen goes blank between frames. To eliminate this flicker a technique known as odd line interlace is adopted in the NTSC system for TV picture transmission and display. In this scheme, each frame is split into two fields each comprising 262 1/2 horizontal lines. One field contains all the even numbered lines of the frame while the other field contains all the odd numbered lines of the frame. These fields are displayed, in an interlaced manner, at the rate of 60 per second. This process effectively appears as displaying each picture twice during a frame period and the flicker between frames is too rapid for the eye to perceive.

In the scanning process for picture creation no picture
information is displayed on the screen during the retrace time. When the electron beam returns to the left hand side of the screen to begin a new scan line, the electron gun is cut-off. This is accomplished by incorporating a blanking signal at the end of each line. At the end of each field a vertical retrace brings the scanning beam back to the top of the screen to start scanning the horizontal lines of the next field. Thus a blanking signal is also incorporated at the end of each field. These blanking signals are voltage levels which cut off the electron beam to the screen and hence the screen is not illuminated during the retrace period.

Each horizontal line is demarcated by a horizontal synchronising pulse at its end as illustrated in Figure 3-2.

Thus each horizontal scan line is contained between two horizontal synchronising pulses. Similarly each field is defined by two vertical synchronising pulses; one at the start and another terminating it. Figure 3-3 illustrates the two vertical synchronising pulses that terminate the odd and even fields in a frame. The synchronising pulses serve as timing signals to ensure that the picture recreated on the TV screen is in step with the original scene. The vertical synchronizing pulse starts the vertical scanning of each field and the horizontal synchronising pulse starts the scanning of each horizontal line in a field. Without these
pulses there would be spatial distortion in the reproduced picture.

Each horizontal scan line can be considered to have a number of elementary picture elements called pixels. Each pixel in a color picture has an average brightness level and a hue. As each horizontal line is scanned the pixels
Figure 3-3: Vertical Synchronising Pulse

(adapted from: A Core Refresh Color Display System for Minicomputers by J.A. Goldie, MSc thesis, Oct. 1974, Dept. of Electrical Engg., Univ. of Saskatchewan, Saskatoon, Canada)
contained in that line are illuminated with the brightness and the hue of the corresponding element in the actual scene. The eye then spatially integrates the screen of pixels to perceive a picture. The brightness and hue variation transmitted in each horizontal line of the NTSC video signal is referred to as the video information or picture information signal.

In the NTSC system, each channel is allocated a 6MHz band. In this band the picture and accompanying sound signals are transmitted. Figure 3-4 illustrates the frequency allocations in a typical NTSC TV channel. The picture signal is transmitted as the amplitude modulation of a picture carrier and sound is transmitted as the frequency modulation of a sound carrier, within the allocated 6MHz channel bandwidth. Sound is not of concern in this project. The picture signal contains the information to be captured, stored and displayed by the decoder.

Color in the NTSC TV system is created as a combination of three colors (Red, Green and Blue). These three colors are called primary colors. All other colors are formed as a combination of the primary colors. For example, yellow is a combination of red and green in equal proportion. A color camera produces red, green and blue signals corresponding to the colors in the scene. It is possible to use these three primary colors to carry all the color information to
Figure 3-4: Frequency Allocation in a NTSC TV Channel

the TV receiver, where the scene will be recreated. A different scheme, however, is adopted in the NTSC system.

NTSC color TV signals are described in terms of a luminance or brightness component and a chrominance or color component. The luminance component, designated as the Y component, contains information on the average brightness variations, of the scene and its individual elements. These amplitude variations occupy a 0-4MHz bandwidth. The lower frequencies in the luminance signal define the large areas in the scenes and the brightness of the background. The higher frequencies define fine detail such as edges, lines etc. A vestigial sideband system is used to send the luminance signal. The 6MHz bandwidth allocation for each channel does not allow double side band transmission.
The chrominance component carries color information in terms of two color attributes (hue and saturation). Hue refers to the attribute that determines whether a color is red, green or blue and the like. Saturation is the degree to which a color is not diluted by white light. For example, vivid red is highly saturated while pastel red has little saturation. The chrominance signal is formed by quadrature modulation of a 3.58MHz color sub-carrier by two color sub-components designated as I and Q (Inphase and Quadrature). The I and Q signals are formed by combining red, green and blue primary color signals in specific proportions. Due to modulation, the color information (hue and saturation) is contained in the sub-carrier and its sidebands. The hue information is carried by the sub-carrier phase and the saturation information is carried by the amplitude of the sidebands. The chrominance signal bandwidth extends from 2.1MHz to 4.1MHz centered about the subcarrier frequency of 3.58MHz as shown in Figure 3-4. A more detailed description of the luminance and chrominance signal can be found in [12].

An undesirable 920KHz beat interference occurs between the color sub-carrier (3.58MHz) and the sound carrier (4.5MHz). To minimize this interfering frequency the 3.58MHz color sub-carrier is suppressed in transmission. The TV receiver however requires the color sub-carrier for demodulating the chrominance signal information. To
facilitate this, a burst of 8 or more cycles of 3.58MHz is transmitted as part of the composite video signal, shown in Figure 3-5. This burst, referred to as the color burst, phase references a crystal oscillator in the TV receiver which generates a phase locked 3.58MHz sub-carrier required for demodulation. This color burst is critical for reproducing a stable color picture. If the color burst is absent on a horizontal scan line or if it is distorted, the oscillator falls out of synchronism and a continuous phase locked 3.58MHz sub-carrier is not provided for demodulation. This causes incorrect demodulation of the hue information and incorrect colors are seen in the reproduced pictures. However, the saturation of colors is not affected. A complete color video signal obtained by scanning a single line of a color bar pattern is shown in Figure 3-5.

![Figure 3-5: Composite Color Video Signal](image)

It is important to understand the characteristics of the color sub-carrier phase in the NTSC color signal as the
phase of this sub-carrier determines the hue or color information in the reproduced scene. The characteristics of the sub-carrier phase are described below.

Ordinarily, a spurious pattern of white and black dots will be seen on a monochrome TV screen, when a color transmission is being received. This is because the color sub-carrier causes the brightness of a raster line to rise and fall sinusoidally and the resulting positive and negative peaks produce white and black dots or speckles. This effect is minimized by making the sub-carrier frequency (Fsc) an odd multiple of one half the horizontal line frequency (Fsc=455xFh/2). As a result there are an odd number of sub-carrier half cycles on each horizontal line. Hence the sub-carrier phase is found to be inverted on successively scanned lines in a field. This causes vertical or spatial cancellation of the spurious dot pattern, as now white and black dots fall beneath each other in each field as shown in Figure 3-6. Each frame or picture has an odd number of scan lines(525) and since each line has an odd number of sub-carrier half cycles, each frame will end with half a sub-carrier cycle. Thus the sub-carrier phase on corresponding lines of successive frames will be inverted. This also provides a cancellation, in time, of

\[ \frac{Fsc}{Ph} = \frac{nPh}{2Ph} = \frac{n}{2}; \text{ where } n=\text{odd} \]
the spurious pattern of dots mentioned above. Thus we observe that it is only after two frames or four fields that the sub-carrier phase on a line returns to its normal phase. This is a very important aspect to be noted in designing the Digital Field Memory.

The NTSC composite video signal comprising the picture information, the synchronising pulses, the 3.58MHz color burst and the blanking signals is received with positive luminance and negative synchronising pulses. This indicates that the white portions of the picture are represented by the highest amplitudes in the picture signal, while the synchronising signals determine the most negative amplitudes.
From the above information on the video signal the following important deductions can be surmised:

1. The frequency content of the video signal indicates that all the processing circuits in the codec should be able to handle a 4MHz bandwidth. Frequency distortion will result in poor picture reproduction. Attenuation of higher frequency components will result in poor resolution of detail and attenuation of the lower frequencies results in improper rendition of background brightness. As a general requirement all circuits processing and conditioning the composite video signal must pass frequencies in the range of 30Hz to 4MHz.

2. The maximum frequency video signal tells us of the minimum required sampling rate required for encoding. It also places limitations on the slew rate and settling time of circuits handling the composite video signal.

3. Phase distortion, which is quite natural when a signal containing several frequencies passes through an electronic network, results in improper color reproduction. This is because colors in the reproduced scene are determined by the phase of a signal with respect to the 3.58MHz color sub-carrier. In passing through a circuit containing resistance and capacitance low frequencies are delayed more than high frequencies. This alteration in phase with respect to the color sub-carrier causes improper rendition of the hues in the reproduced picture. This criterion indicates that all the codec circuits are to have a constant delay or linear phase response.

4. Since the sub-carrier phase on corresponding lines of successive frames is antiphase (inverted), it takes two complete frames or four fields for the sub-carrier phase on a line to return to its original phase. In other words, the sub-carrier phase rotates through 90 degrees for each successive field. The phase relationship between the color sub-carrier and the 3.58MHz sub-carrier generated by the TV crystal oscillator determines the hues of colors in the reproduced picture. To maintain a continuous phase relationship between the color sub-carrier and the TV oscillator frequency four fields will have to be stored. A single field can be stored,
but this scheme requires a phasing circuit that advances the color sub-carrier phase of the stored field by 90 degrees each time the field is read out of the memory for display. Without such a circuit the phase relationship between the color sub-carrier and the 3.58MHz sub-carrier generated by the TV oscillator will be incorrect and the reproduced picture will have continuously changing hues, when a still picture is displayed.

5. The vertical synchronising pulses define fields. Hence these pulses can be used to start and terminate the digital storage of a complete field.

3.2 Coding

3.2.1 Nyquist and Sub-Nyquist Encoding

Digitizing an analog signal requires the proper choice of a sampling rate or frequency. The sampling rate defines discrete times at which the analog waveform is sampled and digitized. The rate of sampling differentiates Nyquist and Sub-Nyquist encoding.

The sampling theorem expresses the minimum sampling rate required to reconstruct an analog signal from its samples. The sampling theorem is stated as follows, [6]: A band limited signal of finite energy, which has no frequency components higher than W hertz, may be completely recovered from its samples taken at a rate of 2W per second. The sampling frequency of 2W hertz is called the Nyquist rate. For example, the video signal with a 4MHz bandwidth, described earlier, must be sampled at least at 8MHz to be reconstructed from its samples. Analog signals sampled at a rate exceeding two times the signal bandwidth satisfies the
Nyquist rate criterion and the encoding is termed Nyquist encoding.

Sampling an analog signal at discrete times yields a Pulse Amplitude Modulated (PAM) signal. The spectrum of a PAM signal indicates the original spectrum centered about integral multiples of the sampling frequency as shown in Figure 3-7. The separation of the lower sideband of the spectrum centered about the sampling frequency and the baseband spectrum allows the original signal to be reconstructed by removing all frequency components except for the baseband spectrum by filtering. Sampling at less than the Nyquist rate produces a spectrum as shown in Figure 3-8.

This undersampling results in overlapping of the lower sideband of the spectrum centered about the sampling frequency and the baseband spectrum. Therefore the baseband spectrum can no longer be separated completely to produce the original waveform without distortion. This distortion produces new frequency components in the original spectrum of the signal and is termed foldover distortion or aliasing.

If there were some means of recovering the original waveform even though the signal is undersampled, then there exists the advantage of a reduced number of samples and hence a reduction in the number of codewords for a signal of
Figure 3-7: Spectrum of a PAM Signal

Figure 3-8: Foldover Distortion
given duration. This reduction is of considerable significance in this project as it allows the use of a smaller storage memory, which would be simpler in design and cheaper. The technique of being able to encode at a rate less than the Nyquist rate and yet be able to recover the original signal upon reconstruction is termed Sub-Nyquist encoding.

The peculiar nature of the NTSC signal lends itself to Sub-Nyquist encoding. Figure 3-9 illustrates the spectral energy distribution of the luminance and chrominance components of a NTSC signal. The luminance information energy is clustered about the horizontal line frequency (15.75KHz) and integral multiples thereof; while the chrominance information energy is clustered at odd multiples of one half the horizontal line frequency. Thus we observe that the luminance and chrominance information energy are interleaved as illustrated in Figure 3-9. Therefore if the aliasing components, produced by Sub-Nyquist sampling, are shifted to those regions of the spectrum between the luminance and chrominance information clusters, no distortion through interference will occur. This is achieved by sampling the video signal at \(2F_{sc} + F_h/4\) or \(2F_{sc} - F_h/4\); where \(F_{sc}\) is the color sub-carrier frequency and \(F_h\) is the horizontal line frequency, [10].

Figure 3-10 shows the resulting spectral distribution
Figure 3-9: Spectral Distribution of a NTSC Video Signal

Figure 3-10: Spectrum of a Sub-Nyquist Sampled NTSC Signal
of a NTSC video signal sampled at the above Sub-Nyquist frequency. The undesirable aliasing components can now be removed by means of comb filters, several designs of which are possible. The response of a comb filter is illustrated in Figure 3-11. A description of comb filtering used in Sub-Nyquist encoding of video signals, is contained in [10].

**LEGEND:**
- Y: LUMINANCE ENERGY
- C: CHROMINANCE ENERGY
- A: ALIASING COMPONENTS
- H: HORIZONTAL LINE

**COMB FILTER ALGORITHM:** \( H \pm (H \pm 2) \)

![Diagram of Comb Filter Response](image)

The obvious advantage of Sub-Nyquist encoding is bit reduction and hence less storage required for each TV picture field. This simplifies the design of the Digital Field Memory and reduces the cost of the Field Memory. However, the Sub-Nyquist encoding technique requires the use of expensive comb filters which offset any cost advantage attained with reduced storage requirements. Further, the choice of a proper comb filter is very important as filtering causes a loss of vertical resolution, due to attenuation of some video signal frequencies in the filter cut-off region; another unattractive proposition. Thus, in
the Telefield decoder described in this dissertation the above Nyquist (2 X Nyquist) encoding technique was adopted.

3.2.2 Coding Schemes

Linear Pulse Code Modulation (LPCM) and Differential Pulse Code Modulation (DPCM) are the two coding schemes considered in this section and are the more commonly employed schemes for video signal encoding.

An analog signal is sampled, at a rate satisfying the Nyquist criterion rate, to produce a PAM signal. This PAM signal comprises a sequence of amplitude modulated pulses. Either, the pulse amplitudes are digitally encoded or the differences in successive pulse amplitudes are encoded into digital codewords. The former is termed Pulse Code Modulation and the latter Differential Pulse Code Modulation. This subsection discusses briefly the relative merits and demerits of these schemes based on a survey of available literature on coding schemes that have been implemented for video signals.

Linear Pulse Code Modulation

The conversion of an analog signal into a digital LPCM signal involves three steps. The first is to sample the signal at a rate greater than or equal to the Nyquist rate. The second step involves assigning each sample amplitude to one of Q discrete equidistant levels; where Q is the number 2 raised to the power of the number of bits(B) in the binary
This second step which is called quantization involves an approximation and introduces quantization error or noise. The larger the number of bits in the codeword the greater the resolution and the better will the approximation be. The third step involves coding. Each quantized level is associated with an unique binary codeword which corresponds to the middle of the respective quantization interval. Thus the quantized samples falling in a particular quantum range will be assigned the code associated with that quantization level. The entire conversion process involving sampling, quantizing and coding is implemented in a single integrated circuit A/D converter. Video speed A/D converters are commercially manufactured by RCA, Motorola and TRW corporations.

**Differential Pulse Code Modulation**

Since the range of sample amplitude differences is smaller than the range of individual sample amplitudes, a smaller number of bits may be used, in each codeword, to encode a sample difference. This is the principle of Differential Pulse Code Modulation. The technique involves comparing each sample amplitude with an approximation of the previous sample amplitude and encoding the difference. A better approximation of the previous sample value will result in more accurate encoding. Prediction can be employed in generating more accurate approximate sample values. A simpler DPCM technique called Delta Modulation
(DM) is quite popular. In DM the difference information is encoded using a single bit which indicates whether the current sample is greater than or less than the previous sample.

3.2.3 Signal To Noise Ratios of LPCM, DPCM and DM

Quantization in the encoding process is an approximation process and results in errors in coding of the absolute amplitudes (LPCM) or sample difference amplitudes (DPCM). These errors are called quantization errors or quantization noise as shown in Figure 3-12.

![Figure 3-12: LPCM Quantization noise (adapted from [6])](image)

If LPCM is used to encode a video signal then the quantization errors cause contouring in the reproduced image. A similar effect is observed with DPCM. In Delta Modulation and DPCM in addition to the quantization error which is called granular noise there is another error which arises when the input signal changes too rapidly for the
Delta Modulation encoder to follow and generate correct codes. This is referred to as slope overload distortion or noise as shown in Figure 3-13.

![Figure 3-13: Slope Overload Distortion](image)

Slope overload noise appears as a loss of bandwidth of the video signal, since its effect is to increase the rise time of the encoded signal. This results in a degradation of resolution in the reproduced image. As with LPCM and DPCM, the granular noise generated in a Delta Modulation system will cause a snowy picture and edges will be blurred in addition to the contouring effect.

As a result of the quantization errors or noise, modulation systems are characterized by a figure of merit called the signal to noise ratio. This ratio expresses the RMS signal to RMS noise power. The RMS signal to RMS noise ratios for the afore mentioned systems are listed below:

\[
\text{LPCM } S/N = 6N + 1.8 \, \text{dB} \quad ; \quad N = \text{No. of bits in codeword}
\]
DPCM-employing linear prediction, [9]

\[
\text{S/N} = 13.5 + 6N + 20 \log_{10} \left[ \frac{\text{rms value of signal}}{\text{rms value of prediction error}} \right]
\]

3.2.4 Comparison of DM and DPCM with LPCM for Video Encoding

Delta Modulation offers the simplest and probably the cheapest of the circuits. The one bit encoding however requires higher sampling frequencies than the other two schemes. Thus, DM provides fine resolution in time but coarse resolution in amplitude. Further, granular noise which produces snow and slope overload noise and slope overload distortion which causes blurred edges and a loss of resolution impair the reproduced image. However, since the viewed picture is perceived by its worst degradation, the quantizing step size, sampling rate and bandwidth can be chosen to spread the above degradation in manner to improve the reproduced image [8]. DPCM using prediction is probably the best scheme for monochrome TV picture encoding and storage; especially for high resolution systems. For monochrome TV systems DPCM provides a 15 dB improvement over LPCM using 8 bit encoding of the composite video signal and a 12 dB improvement if the sync signals are also encoded. By not encoding the sync signals a larger quantizing range is available for encoding the video.
information, resulting in less quantization noise. The improvement afforded by the DPCM system when translated into bits results in a saving of 300kbits or 25% per video field, assuming a constant S/N ratio and a 9MHz sampling rate [9].

The above mentioned saving in bits is very attractive in video storage applications such as this project. The reduced number of bits per video field affords saving in memory size and complexity. However the encoding circuitry for DPCM employing linear prediction is considerably more complex and expensive over the simpler LPCM and DM schemes. Further the advantages for DPCM are contingent on the statistics of the video signal. The advantages cited are for monochrome signals. Color signals have different statistics, notably more high frequency energy, and hence the validity of the above advantages is questionable in the case of color video signal encoding.

LPCM offers a simple and convenient method for encoding the composite video signal. The circuitry is not involved and complete A/D converters are available in a single integrated package or as modules. LPCM employing 7 or 8 bits provides good quality color pictures for entertainment TV of studio broadcast quality. The undesirable contouring, due to quantization errors, is not perceptible for 5 or more bits of encoding for monochrome pictures, [23]; while 6 or more bits are recommended for color pictures, [16]. These
word sizes are the results of subjective testing. LPCM provides a tradeoff between the more complex DPCM schemes employing linear prediction and the simpler but poorer DM scheme. In this project LPCM was chosen to digitally encode the composite video signal.

3.2.5 Video Encoding Methods and Encoding Rate

There are basically two methods of encoding a video signal. The first is to digitally code the composite video signal using LPCM. In the second method, the luminance and color component signals are encoded separately. The former is the predominant method in North America while the latter is extensively used in Europe. In the color encoding and decoding scheme the color signal is split into its Y (luminance), I and Q (color) components. This can be done by the TV receiver circuitry. These components are encoded, stored and decoded separately. Therefore this scheme requires the use of three separate channels, each comprising an A/D converter, a digital store and a D/A converter. Since the luminance and chrominance occupy a common portion of the spectrum allocated to each channel the I and Q components are contaminated with luminance information [11]. Separation can be achieved with comb filtering, which adds to the cost and complexity of the scheme. A description of comb filtering schemes used to separate chrominance and luminance components are described in [14]. Additional problems include I, Q channel crosstalk [11], regeneration of horizontal and vertical synchronization, color burst
synchronization and phasing with the sampling clock. The increased complexity of the second scheme is not attractive to this project but is worthwhile for applications such as standards conversion and in complete digital sets. This led us to accept the simpler "brute force" composite video signal encoding. Composite video encoding may be inefficient for conserving bandwidth and storage but affords considerable simplicity in design and implementation. The additional storage required is not a major limitation as extra memory is inexpensive. Further large integrated circuit memory is becoming increasingly inexpensive which makes the simple brute force encoding technique very attractive. Also, the associated problems of regeneration of synchronization signals and color burst are not experienced. However the sampling clock will have to be phased with the reference color burst for reasons to be explained in Section 5.9. This is done fairly easily. Having chosen to encode the composite video signal using LPCM it remains to choose a suitable encoding rate and the number of bits per codeword.

The encoding rate was chosen to be four times the color sub-carrier frequency (i.e. 4 x 3.58MHz = 14.32MHz). The choice of this rate is based on the fact that the pictures are less prone to visible beats when the sampling rate is three or four times the color sub-carrier frequency. The reason for the choice of this sampling rate is explained
The chrominance information energy is clustered about the sub-carrier frequency, with the more saturated colors closer to the sub-carrier. This is because saturation is most visible in the larger areas of the picture and large areas correspond to the slower variations (frequency) in the picture signal. Thus when this signal is modulated the saturated areas occupy a smaller bandwidth centered on the sub-carrier frequency.

When the sampling frequency and the sub-carrier frequency are not coherent, interfering beat patterns are observed in the picture. The quantization process produces modulation products. The lower in-band modulation products are concentrated near the sub-carrier frequency. Now, if the sampling frequency and the sub-carrier frequency are not coherent, beat products are formed and they produce
patterning in the highly saturated areas of the colors. However, if the sampling frequency is an integral multiple of the sub-carrier frequency, the modulation products produced by quantization coincide with existing TV signal components and will "zero beat", which eliminates the patterning in the reproduced picture [1]. With the above discussion in view the sampling frequency was chosen as 14.32MHz.

The phase of the color sub-carrier on successive fields of a NTSC TV signal is shifted by 90 degrees. When only one field is stored, a phasing circuit is required to perform the required sub-carrier phase shift in order to display the stored field. The use of 14.32MHz as the sampling frequency allows a simple phasing scheme which is explained in Section 5.9.

The size of the LPCM codeword is a tradeoff between resolution which improves picture quality and the size of the memory required. The larger the number of bits, the higher the resolution and the better will the picture quality be; but each extra bit in the codeword adds to the memory size and complexity. Further, each extra bit in the codeword causes an increase in the complexity of the encoder and its cost. As mentioned earlier, 7 or 8 bits per codeword provides studio quality pictures, while 6 bits produces good pictures of lower resolution. Although the
Signal to noise ratio is not an absolute indicator in measuring picture quality, it is recommended that this ratio be at least 36 dB. This is achieved using a minimum of 6 bits per codeword. The choice to use 6 bits per LPCM codeword is then based on achieving acceptable quality entertainment TV pictures and observing that cost increases exponentially for increasing resolution.

3.3 Digitization Techniques

Having chosen to digitize the composite video signal by LPCM, it remains to select an appropriate digitization technique. This involves the choice of an appropriate A/D converter. Several A/D converters are available as modules and as single integrated circuits. The varieties in A/D converters stem from the diverse digitization techniques employed. Each technique is suited for a particular class of applications. The choice of a particular technique and A/D converter is based on characteristics such as speed, resolution, accuracy, size, cost and output word format. The principles of four popular techniques employed in A/D conversion are briefly mentioned below, together with their salient characteristics. A more detailed description of the digitization techniques and circuitry employed in commercial A/D converters is contained in [18] and [19].
Counter and Servo Type

In this technique the count from a counter is compared with the analog input using a comparator and D/A converter. The counter is incremented by a clock until the count corresponds to the input signal. The counter output is the digitized codeword of the input signal. This technique is modified to provide tracking of the input using an UP-DOWN counter.

This technique is straightforward involving simple circuitry. The major disadvantage is that for a given resolution the conversion speed is slow. In other words increasing the resolution increases the conversion time for a given clock rate.

Dual and Quad Slope Type

This technique involves the conversion of the unknown signal into a proportional time interval which is recorded digitally. The unknown signal is initially integrated for a fixed duration, T. Then a reference signal is 'switched in' and it is integrated from the level determined by the unknown signal at the end of the fixed duration T, until zero level. The time for this second integration is recorded by a counter and is proportional to the average of the unknown signal over the fixed duration. The counter contents provide the digital codeword.
Conversion accuracy is high. Resolution is not restricted and can be increased by adding more bits to the counter. High frequency noise is integrated and therefore this conversion technique provides good noise immunity. For example, since the measurement is of the averaging type, changes in the input signal due to the noise are smoothed out. There are two significant disadvantages. The first is that the conversion speed is very slow and limited to a little less than 1/2T. A second disadvantage is that zero errors in the circuit components, such as the integrator and comparator, cause erroneous measurement. This is corrected by the quad slope technique, in which there are two dual slope measurement cycles. The first involves measuring the zero errors in an auto-balance cycle and then this error is subtracted from the final output count obtained in a sample cycle.

**Successive Approximation Type**

This technique is similar in nature to a binary search algorithm. The technique involves comparing a sample of the input signal with the output of a D/A converter, whose input is the output of the A/D converter. Starting with the most significant bit of the D/A converter, a logic 1 is placed in each successive bit and a comparison is effected until a match is realized. The conversion time is fixed for any amplitude of the input sample.
Successive Approximation conversion offers high speed and resolution. Conversion speed decreases as resolution increases. Successive Approximation converters require an accurate sample and hold circuit. At high speeds the cost of good sample and hold circuits are considerable. The conversion technique is affected easily by noise.

Parallel or Flash Types

This conversion technique is the fastest of the available types. The circuitry employed comprises $2^n - 1$ comparators, for an n bit output word, each biased 1 LSB apart. An increasing input signal causes more comparators to produce an output. The outputs of the comparators are decoded to form a digital codeword corresponding to the input signal. The main advantage of this technique is the very high speed, which is limited only by the switching times of the comparators and decoder. However as resolution increases arithmetically the number of comparators increases geometrically and hence complexity and cost increase enormously. Medium resolution flash converters are now available in integrated circuit form.

3.4 Choice of the Converter

The proposed application calls for a converter with very high speed, medium resolution, an accuracy of 1 LSB, circuit simplicity and low cost. It was decided to employ LPCM with 6 bits per codeword for the encoder. Since the resolution is only 6 bits, fairly low cost flash converters
are available making it suitable for such a converter to be used in the project. The speed of digitization of 14.32MHz required in the encoder far exceeds that available with the fastest Successive Approximation converter and is only available with flash conversion. Flash converters are available in a single integrated circuit package, which require a minimum of signal conditioning and processing circuits, such as costly Sample and Hold circuits. Further most available flash converters provide a 1/2 LSB accuracy.

Considering these features it was decided to use a flash converter as the encoder in the Video Codec.

3.5 Digital To Analog Conversion

The encoded video signal, when read out of the memory for display, has to be converted to an analog signal. This is accomplished by a digital to analog(D/A) converter. D/A converters are of two types, viz., current output and voltage output D/A converters. The former is faster but requires an output circuit for current to voltage conversion. A more detailed description of each of these types is contained in [19]. In this section, we briefly elicit the two mentioned D/A designs.

A D/A converter comprises four basic elements; a resistor network, current or voltage switches, a summing operational amplifier and a reference supply. The resistor network can be either a set of binary weighted resistors, a
R-2R ladder or any other suitable configuration. The resistor network and the switches, together, produce binary weighted currents or voltages corresponding to the weight of the input digital word. The currents or voltages produced are derived from a reference supply. These binary weighted currents or voltages are summed to produce an analog output (current or voltage).

The switches used may be of the current or voltage type. Current switches steer the reference current between the amplifier summing point and ground. The current is not interrupted and the voltage change across the switch is small, making the switching time short for a current switch [19]. A voltage switch switches between reference supply and ground. This larger change in voltage across the switch causes slower operating speed as compared to the current switch.

In a voltage output D/A converter the binary weighted currents or voltages produced by the resistor network and the switches is summed by a summing amplifier (op-amp). The speed of the voltage output D/A converters is, generally, restricted by the speed of this op-amp. The current output D/A converters do not have an internal op-amp and their speed is limited by the speed of the switches. Thus, fast D/A converters invariably employ current switches and have current outputs.
The D/A converter chosen in this design is a high speed current output D/A converter.
CHAPTER 4

VIDEO CODEC IMPLEMENTATION

A block diagram of the Video Codec design is shown in Figure 4-1. The Video Codec comprises three blocks: an encoder, a decoder and a memory interface. The encoder serves to convert an incoming composite video signal into 6 bit LPCM codewords. The decoder serves to convert the LPCM codewords into corresponding analog levels, so as to reconstruct an approximation of the original composite video signal. The memory interface serves to send codewords to and receive codewords from the Digital Field Memory used for storage.

Figure 4-1: Video Codec Block Diagram

4.1 Video Codec as a Part of a TV Receiver

The Video Codec and Digital Field Memory are collectively known as the Telefield decoder and it is proposed to incorporate this Telefield decoder in a commercial TV receiver. A detailed functional description
of the various circuit blocks of a color TV receiver is contained in [12]. A brief description of the TV receiver circuit functions is provided in this section to provide an insight into where the Video Codec and Field Store can be incorporated.

Broadcast TV signals are received via an antenna. A tuner serves to select a single channel. The tuner is a superheterodyne type comprising a RF amplifier, a local oscillator and a mixer. The selected RF channel is converted into an intermediate frequency (IF) by the tuner. This intermediate frequency is amplified by a set of IF amplifiers and then fed to two detectors. An FM detector is used for the sound signal and an AM detector is used to demodulate (detect) the AM picture signal. The AM detector is referred to as the second detector. The output of the second detector is the composite video signal (2Vp-p). From the output of the second detector the composite video signal is fed to the video amplifier, the sync detector and color circuits. These circuits strip the composite video signal into its component parts. The sync detector removes the horizontal and vertical sync signals, which are then used to synchronize the deflection oscillators that control the electron beam scanning. A chrominance or color section filters the color component of the composite video signal and demodulates it to produce the three primary color signals (red, green and blue). These three signals are fed
to the control grids of the respective electron guns of the color picture tube. The luminance signal is filtered out of the composite video signal, amplified by the video amplifier section and fed to the cathodes of the three electron guns of the picture tube. From this description it is evident that the Video Codec and Field Store is best incorporated after the second detector as shown in Figure 4-2.

![Figure 4-2: Video Codec Implementation in TV Receiver](image)

The input to the Video Codec is a 2Vp-p composite video signal from the second detector output. The output of the codec is fed to the video amplifier, sync detector and color demodulator circuits. The advantage of this location is that, since the path of the signal through the TV receiver is not disrupted, as the Video Codec is incorporated as a series element, we can use all of the existing TV receiver circuitry for pre-processing the video signal before
encoding. Also the existing TV receiver circuitry can be used for post-processing the reconstructed video signal before display. This allows the Video Codec to be designed with a minimum of external circuitry, which would otherwise be required to perform tasks such as channel selection, demodulation, sync detection and picture reproduction.

Further, any codec requires the use of an aliasing pre-filter and a post-detection filter. The former prevents foldover distortion or aliasing, while the latter smoothes the decoded output. These filters are required to have a linear phase, bandwidth of 0-4MHz with sharp skirt selectivity. These requirements make the filters complex to design and are fairly expensive. By incorporating the Video Codec as indicated in the TV receiver, this filtering is accomplished by the video processing circuitry of the receiver.

Therefore by using the existing TV receiver circuitry the design of the Telefield decoder is simplified and considerable cost saving is achieved.

4.2 Implementation of the Encoder

In this section the implementation of the encoder circuitry will be discussed. The video encoder comprises an input video amplifier and an A/D converter. Each of the component blocks is considered separately and the implementation described. The description includes the
requirements to be met followed by the selection of suitable components and devices. A description of the circuit operation and significant design features follow. A similar organization is followed in the description of the implementation of the decoder.

4.2.1 Input Video Amplifier

The input video amplifier is a wide band amplifier that amplifies the incoming composite video signal, to use a greater dynamic range of the A/D converter. This improves the S/N ratio of the encoding process. Some of the important requirements of the video amplifier are:

1. The video amplifier must be capable of providing sufficient gain to amplify the composite video signal to the required level before encoding. The amplification should however be within the dynamic range of the A/D converter to avoid overload clipping.

2. Proper video signal polarity should be maintained.

3. The bandwidth of the amplifier must extend from 10Hz to 4MHz. The low frequency response should be flat down to at least 30Hz and extend to 10Hz. Poor low frequency response results in smearing of objects from left to right and loss of background illumination. Poor high frequency response will result in loss of resolution and detail.

4. The amplifier should introduce no phase distortion. A linear phase characteristic is desired. Phase distortion results in displacement of picture elements in the reproduced picture causing smearing in monochrome receivers. In color receivers the effect is to distort the hues of the reproduced colors.

5. If an active device such as an operational amplifier (op-amp) is used to build the video amplifier then its slew rate is important. Slew
rate is the maximum rate of change of the output under large signal conditions. A reduced slew rate results in an increased rise time and hence reduced resolution in the reproduced picture. To handle video bandwidth signals (0-4MHz) the op-amp slew rate requirement is around 25 V/µs.

A variety of video operational amplifiers satisfying the bandwidth, phase and slew rate requirements were surveyed and the ECG915\(^7\) was chosen. Availability also influenced the choice.

\[
\text{INPUT COMPOSITE VIDEO} \quad \text{ECG915} \quad 100\mu\text{F} \quad \text{TO A/D CONVERTER}
\]

Figure 4-3: Input Video Amplifier

The circuit schematic of the designed input video amplifier is shown in Figure 4-3. The active device, the ECG915, is a high speed and high gain operational amplifier intended for use in wide bandwidth applications such as

\(^7\)From Sylvania Semiconductors
video amplification. The circuit configuration is in the non-inverting mode, with a closed loop gain of 100. A closed loop gain of 100 was chosen as typical performance curves indicate that slew rate (which is a function of the supply voltage and the closed loop gain) is 70 V/μs for a gain of 100 and supply voltages being +15V and -15V. A high slew rate is required to handle large bandwidth signals without distortion. The closed loop gain (Avf) is given by \( Avf = \frac{(Rf+Rl)}{Rl} \). Rl was chosen to be 51 ohms. Rf was then chosen to provide the required gain (100). A small 1pF capacitor is included across the feedback resistor to improve the high frequency transient response. An input voltage of 40mV is required to produce a 4Vp-p output. This can be produced by attenuating the 2Vp-p output from the second detector using a 1K ohm potentiometer as an attenuator at the input of the op-amp. Alternately, a lower gain can be used but this reduces the slew rate of the operational amplifier. Further, changing the gain may require a change in the compensation capacitors, which are recommended by the manufacturer to improve stability. Since the ECG915 is a high gain high bandwidth amplifier it is susceptible to oscillate. Manufacturer suggested compensation capacitors C1, C2 are used to improve the gain and phase margins of the operational amplifier for increased stability. Bias current errors can be minimized by making the DC resistances seen by the two input terminals equal. However, as the bias currents are very small (0.4nA) the
error introduced is negligible for small values of R1. It is therefore not required to balance the bias current by matching DC resistances at both terminals.

The designed input video amplifier gives good performance. It provides a bandwidth upto 4MHz with no phase distortion.

4.2.2 A/D Converter

The A/D converter digitizes the composite video signal and encodes it into 6 bit LPCM codewords. A Flash converter is used due to the high sampling speed (70ns) and parallel conversion requirement. Several flash converters available provide the above requirements. The CA3300 is used in this design, as it was the least expensive of the surveyed flash converters meeting the above requirements. The CA3300 is especially suited for high speed, low power digitizing applications such as TV video digitization. Detailed specifications of this A/D converter are provided in Appendix 1. Figure 4-5 is the timing diagram for the CA3300 and Figure 4-5 illustrates the schematic of the CA3300.

Device Operation: From Figure 4-5 we can trace through a single conversion cycle as follows: During the high state of the clock the comparators track the input voltage and the

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8 From RCA
Figure 4-4: Schematic of CA3300
latches track the comparator outputs (this allows us to eliminate the need for a sample and hold circuit). On the trailing edge of the clock the comparator outputs are latched. The auto balance phase follows. During the low state of the clock the latched data is decoded. On the next rising clock edge data is clocked into an output buffer and appears at the output after 20ns of time delay. Thus, the output is valid approximately one cycle + 20ns after the sampling instant.

Supply Voltages: A single supply of 8V is used to power the A/D converter and to provide a reference voltage. A 5V supply can also be used, but the speed of operation of the A/D converter is then restricted to 11MHz. The 8V supply allows a sampling frequency up to 15MHz.

Outputs: The outputs of the A/D converter will make transitions between binary levels of 0V and 8V. Since all other circuits in the codec and memory operate at TTL
Figure 4-6: A/D Converter Circuit
levels, the output is scaled down to 0V-4V using a potential divider network as shown in Figure 4-6, as recommended by the manufacturer.

Clock Phase and Output Enable: The CA3300 provides a phase pin(#8) which allows the clock to be inverted. To do this the pin is pulled up to 8V through a 1K resistor. Data is now shifted out on the rising edge of the clock as desired by the sequencing scheme adopted. The enable pins CE1(#5) and CE2(#6) serve to enable or disable the outputs and are connected as shown in Figure 4-6. The 0.1μF capacitors on the pins bypass high frequency noise to ground.

Reference Voltages: In order to produce a correct digital representation of an analog signal all flash converters require precise voltage references, as the digital output codewords are a result of a comparison between the input analog voltages and the reference voltage. These references must be accurate to 1 LSB. The reference voltage also fixes the dynamic range of the A/D converter. A reference voltage which is too small will produce errors as indicated in Figure 4-7.
Figure 4-7: Errors Due To Improper References

The CA3300 has three reference pins; a positive, a negative and a mid-point reference pin. A dynamic range of 4V is chosen. Therefore the positive reference $R^+$ is fixed at 4V by means of a 6.8V zener diode and a 1k potentiometer. The 220 ohm resistor serves to limit the zener current. The negative reference is kept at ground potential. The mid-point reference is hence fixed at 2V. All references are bypassed to ground using 0.1µF ceramic
capacitors. This capacitor serves to bypass high frequency noise that can cause reference voltage variations. With a 4V dynamic range, the size of a quantizing bin is 63.5mv.

Potentiometers P1 and P2 are included, as suggested by the manufacturer, to increase the accuracy of conversion. P1 produces a GAIN TRIM to adjust for full dynamic range utilization. P2 provides an OFFSET TRIM to adjust for the first transition from 0 to 1 to occur at 1/2 LSB or Vref/128.

It was observed that the stability and symmetry of the references determine the linearity and accuracy of conversion. Poor linearity results in straight lines having wobbles and element spacing discontinuity in the reproduced image.

Input: The input is supplied from the input amplifier with a 4Vp-p composite video signal. A somewhat elaborate system is used in supplying the input as shown in Figure 4-8. This comprises a tracking amplifier and an emitter follower. The tracking amplifier serves to hold the input DC level at 2V, while the emitter follower serves as a buffer and drives the input. The DC level of the input is centered on the reference center level, which references the tracking amplifier. If the DC level of the input were to be displaced, say, upward from the reference center level, then
the sensitivity of the counts above and below the reference center will be different (see Figure 4-7). Further clipping may occur on the upper or lower half of the dynamic range reducing the resolution. All these problems will reduce the resolution and impair picture quality. With the tracking amplifier the DC input level tracks the reference center voltage. Potentiometer P3 adjusts the tracking amplifier offset voltage to achieve a 2V DC input level when the reference center is at 2V. The 3K ohm resistor and the 0.1uF capacitor serve to block the video input from being fed back to the input of the tracking amplifier.

![Tracking Amplifier Circuit](Image)

**Figure 4-8: Tracking Amplifier**

Clocking: The sampling clock is provided through an open collector inverter (SN7406) with a 1K ohm pull-up resistor to 8V. A twisted pair with one wire grounded is used to feed the clock to the A/D converter as shown in Figure 4-6. The twisted pair minimizes lead inductance and reduces the ground current due to the clock line. At low
frequencies the inductance is low and ground currents flow in the ground loop formed. To minimize these currents a 20 ohm resistance is used in series with the ground wire of the pair. At high frequency the inductance of the ground lead limits the ground currents.

4.3 Implementation of the Decoder

The Decoder comprises a high speed D/A converter and an output stage.

4.3.1 D/A Converter

The important characteristics considered in choosing a suitable D/A converter are listed below:

1. Settling time of less than 69ns in order to handle signals sampled at 14.32 MHz.
2. Conversion with low glitch.
3. 6 bit D/A conversion.
4. Direct interface to TTL.
5. Low power consumption.
6. Large output voltage compliance.
7. Preferable to have differential outputs.
8. Low cost.

A survey of high speed D/A converters led to the selection of the DAC-08\(^9\). This is a fairly common D/A converter and is the least expensive of the D/A converters meeting the

\(^9\)From Precision Monolithics Incorporated[PMI]
above requirements. A circuit diagram of the designed D/A converter is shown in Figure 4-9.

![Circuit Diagram of DAC-08](image)

Figure 4-9: Decoder of the Video Codec

The DAC-08 is a high speed multiplying DAC providing a settling time of 85ns with low glitch, and allows differential operation. Typically it is not suited for conversion of video bandwidth signals, but an implementation has been designed which provides acceptable performance.

Reference Voltages: The DAC-08 provides an output current that is the product of the input digital number and the reference current. Hence a stable reference current is required as the output is a linear function of the reference
current. A reference scheme suggested by the manufacturer is used. In the reference scheme adopted a reference current of 2mA is fed to the two inputs of an internal reference amplifier (pin#14 and pin#15). The internal reference amplifier has a high gain and the voltage at the two inputs (pins #14 and #15) track each other. The reference voltage sourcing the 2mA reference current is derived from the +15V supply using a μA78L05 monolithic regulator. The 10K ohm potentiometer in series with pin#15 can be adjusted to vary the input reference current for full scale adjustment. The impedance seen by the two reference inputs is equal and approximately 5k ohm at 2mA. This serves to cancel bias current errors. The internal reference amplifier is compensated by using a recommended 0.01μF ceramic capacitor between pin#16 and the negative supply. A reference current of 2mA was chosen for fast settling time. Smaller values of reference current are not recommended in the manufacturers specifications as settling time is increased.

Logic Levels: The DAC-08 provides compatibility with TTL, ECL, HTL, CMOS and PMOS families. A logic threshold pin(#1) is provided to facilitate this compatibility. As the logic inputs are TTL pin#1 is grounded; the required connection for TTL logic compatibility.

Settling Time: The DAC-08 settles in 85ns with a
reference current of 2mA. A settling time less than 69ns is required for video signal reconstruction, at sampling frequencies of 14.32MHz. The speed of conversion depends on the following:

1. The output RC time constant of the converter.

2. The settling time of each switch in the converter. This in turn depends upon the characteristic of the switches and the time skew amongst the bits of the input word.

The output capacitance of the DAC-08 is given to be 15pF and the settling time is dominated by the output RC time constant if the load presented to the DAC-08 output exceeds 500 ohms. In the designed circuit a 24 ohm load is presented to the outputs. The settling time (7RC) was calculated to be 3.36ns. This indicated that the settling time was not restricted by the output RC time constant. The settling time is determined by the settling time of the internal current switches. The settling time of the LSB switch is 35ns and each higher order bit-switch takes a longer time to settle. For 8 bits the settling time is 85ns. This settling time was improved to 65-70ns by grounding the two most significant bits.

To obtain fastest settling times ground plane construction, short lead lengths, minimizing the output load resistance and bypassing supplies and references with 0.1uF capacitors are recommended by the manufacturer and were adopted. The resulting performance of the D/A converter was
observed to be very satisfactory.

Outputs: The output currents produced by the DAC-08 are complimentary and are jointly equal to the reference current. These complimentary output currents are fed to an operational amplifier current to voltage converter, which produces a signal of 2VP-p.

There are two significant advantages in using a differential output:

1. Since the output currents are small, noise even at low levels will have pronounced effects. If differential outputs are used noise will affect both the outputs. Differential amplification using an operational amplifier will reduce the noise as the noise is a common signal and the operational amplifier has a high common mode rejection.

2. Differential outputs provide twice the peak produced by a single output. This allows the use of a smaller output load resistor to obtain the same output level.

4.3.2 Output Stage

Figure 4-10 illustrates the designed output stage. The current to voltage converter converts the current outputs of the D/A converter to a 2VP-p composite video signal. The operational amplifier in the current to voltage converter has to handle signals of video bandwidth and hence the requirements mentioned for the input video amplifier hold for the current to voltage converter.

The ECG915 is used as the operational amplifier in the
current to voltage converter. The ECG915 being a high gain, high bandwidth amplifier oscillates easily. Manufacturer suggested compensation capacitors C3 and C4 are used to improve the stability. Rd1 and Ro determine the closed loop gain of the current to voltage converter. The selection of the closed loop gain is directly related to the stability of the circuit. The choice is made with respect to the open loop phase and open loop gain characteristics of the operational amplifier employed. A closed loop gain of 100 is chosen. Rd1 is then selected bearing in view that the load resistance seen by the D/A converter outputs must be small, so that it does not increase the settling time of the
D/A converter. Rd1 is chosen to be 24 ohms. Ro is chosen to provide the desired gain. To keep the voltages at the inverting and non-inverting terminals the same, the DC resistances seen by the two terminals must be equal. Thus Rd2 is made equal to the parallel combination of Rd1 and Ro, which is approximately Rd1. This also serves to reduce bias current errors. Ro, the feedback resistor is split into a fixed and a variable resistor to vary the amplitude of the output voltage. The output voltage is a function of the current through the feedback resistor, Ro and the current through the feedback resistor is proportional to the input current from the D/A converter. Using both the D/A converter outputs provides twice the output produced by using only one.

The output voltage of 1Vp-p is fed to a 75 ohm load. The resulting 13ma (1V/75ohms) current drive cannot be provided by the ECG915. Thus a complimentary emitter follower is used as a current boosting stage. This stage comprises complimentary transistors connected as a class-B push-pull amplifier. With class-B operation crossover distortion results. This distortion occurs at the zero crossing of the output signal, where one transistor of the push-pull circuit must be turned ON and the other must be turned Off. Since the transistors take a finite time to be turned ON and Off, there occurs a short duration of the output signal where both the transistors are Off. Thus, no
current is provided to the load and the output remains at ZERO level till one of the transistors turns ON. This is eliminated by providing a 75 ohm resistor, Rb, as shown and including the push-pull stage in the feedback loop of the current to voltage converter. The 75 ohm resistor serves to supply current to the load from the operational amplifier when the transistors are Off. However, now there is no current boosting but the current supplied should be sufficient for grounded loads and small output voltages. As the output increases from zero crossing the current drawn through the 75 ohm resistor biases one of the transistors ON, which then supplies the load with current.

Rb, should be chosen to be comparable with the load resistance to prevent crossover distortion which will occur due to the slew rate limitations of the operational amplifier. If the load resistor is much smaller than Rb, the output of the operational amplifier is much larger than that at the output of the push-pull amplifier during zero crossing of the output signal. If the push-pull amplifier output is large enough to slew rate limit the output of the operational amplifier, then there will be a delay in the rise of the push-pull output giving rise to crossover distortion, [5]. In the design Rb is chosen to be equal to the load resistance.

The 510 ohm resistors in the collectors of the
transistors T1 and T2 limit the maximum current through the transistors to a safe value. An additional stage is interposed between the push-pull output stage and the load. This is a buffer stage provided by an emitter follower. The buffer also transforms the 75 ohm load to a high impedance for the push-pull stage. The inclusion of the buffer stage eliminates the distortion, which was otherwise experienced.

The designed circuit provides satisfactory performance over the range of video frequencies.

4.4 Implementation of the Memory Interface

The memory interface comprises two clocked data latches serving as a driver and a deglitcher. The reason for their use is explained hereunder.

4.4.1 Driver Latch

Data from the encoder is to be stored in the memory. The memory receives data from the encoder (A/D converter) via a ribbon cable. Unless this cable is very short its capacitance loads the output of the A/D converter. This increases the rise time of the data put out by the A/D converter. This causes a problem in latching data in the input buffers of the memory, where a 20ns set-up time is required after the data has reached a steady state. Hence a Hex D-type flip flop (SN74174) is used at the output of the A/D converter to latch its output data. The latch is clocked at a time when the data from the A/D converter has
settled and a 20ns set-up is met. The SN74174 being a TTL device provides sufficient current to drive the cable. A schematic of the circuit is shown in Figure 4-11.

![Schematic of the circuit](image)

**Figure 4-11: Driver Latch**

4.4.2 Deglitcher Latch

With any high speed current switching DAC there exists the problem of glitches. Glitches are spikes or transients to unwanted states. For example, if the D/A converter switches from 011111 to 100000, all its bits are being switched. If its internal current switches do not switch simultaneously then a glitch occurs. For saturated logic the turn-off time (0 to 1) is faster than the turn-on time (1 to 0). Thus such switches cause the DAC to produce a 'zero output' before returning to the output corresponding to 100000. This in effect produces a glitch.
Glitches occur due to differences in the settling times of the internal switches of a D/A converter. This is attributed to:

1. Characteristic of the logic used in the implementation of the D/A converter switches.
2. Time skew in the arrival of the input bits.

The former cannot be rectified but the latter can be minimized using a deglitcher. Glitches manifest themselves as dark or white lines in the reproduced picture. They are especially cumbersome when TEXT messages are displayed as letters in the text have frayed edges and are ragged.

A deglitcher circuit is one that holds the input bits until the D/A converter switches have reached a steady state. In the circuit designed an octal D-flip flop is used (SN74374). Data from the memory is clocked into the deglitch latch. This clocking allows all bits to be latched simultaneously reducing the time skew between bits. The use of a deglitch latch and proper clocking resulted in a reduction of glitch energy from 8000pv-s to approximately 40pv-s which is comparable with some of the costlier D/A converters available. Glitch energy of 100pv-s is considered to be low and found acceptable for good video codec response.

4.5 Clocking

The system clock serves to time and sequence all
operations in the video-codec and memory. The sampling clock of the A/D converter must be stable at 14.32MHz to minimize the undesirable beating between the modulation products, produced by sampling, and the sub-carrier frequency as explained in Section 3.2.5. A stable phase locked loop (PLL) oscillator is used which holds the sampling frequency at 14.32MHz, thereby eliminating much of the patterning in the reproduced picture due to modulation beats. In addition it was observed that unless the clock is stable at 14.32MHz it is not possible to display a stable color picture (constant hues) after storing it in memory.

The circuit of the PLL oscillator used is shown in Figure 4-12. The oscillator comprises an integrated circuit PLL (NE564) referenced by the 3.58MHz crystal oscillator in the TV receiver. This is done to synchronize the system clock and sub-carrier frequencies. It was observed that an asynchronous clock does not allow a stable picture to be displayed after storage, for the designed system. To obtain 14.32MHz frequency multiplication is done by using a divide by four circuit in the feedback loop of the PLL circuit.

A three phase clock is used. The clock to the video-codec is buffered through an open collector inverter (SN7416) on the video-codec board. The three phases of the clock are obtained by delaying the clock through three inverters of the SN7416. The phase relation of the three
Figure 4-12: 14.32MHz PLL Oscillator

Figure 4-13: 3 - Phase Clocks
clocks is shown in Figure 4-13. The three phase clocking scheme is required for proper sequencing of a number of buffers and data latches which have to be clocked at different instants dictated by the data set-up requirements.

4.6 Construction Technique

Noise is unwanted or spurious voltages induced in a circuit. Noise affects signals to produce undesirable outputs. Even in the higher immunity digital circuits if noise exceeds the threshold limits spurious level changes occur. For example, if the noise were to affect the codewords produced by the encoder, the decoded output will be an incorrect replica of the input signal. The ground plane construction technique adopted helps minimize noise.

In any high speed electronic circuit, analog and digital, in addition to the usual sources of noise; thermal, contact and electromagnetic pick up, there are three other sources of interference:

1. Noise due to switching. Switching at high speeds from one level to another produces current spikes on power supply and ground lines. Ground wires have appreciable inductance resulting in appreciable impedance for high frequency current spikes. Ground currents flowing through these wires produce undesirable voltage drops or noise.

2. At high frequencies the electrostatic coupling between leads increases. This can be reduced by maintaining low impedance terminations.

3. At high frequencies magnetic coupling increases. This can be reduced by separating signal lines and providing a nearby ground return for each signal line. This can be done with a coaxial or
twisted line pair.

4. Transmission line effects. At high frequencies long interconnecting wires act as transmission lines. If these lines are not terminated reflections occur. Reflections cause pulses to be received with negative going excursions, which could cause damage to chips which do not have clamping diodes at their inputs. Reflections are minimized by terminating the lines in their characteristic impedance.

A good grounding system is essential to minimize noise pick up and interference. Hence for the Video Codec design a "ground plane" construction is used. The use of AC power ground is poor practice as there may exist several hundred millivolts of potential difference between points on such grounds. The following construction techniques are used in the Video Codec design:

1. Each individual circuit is mounted on an island etched on the ground plane. The islands provide better isolation between circuits. The use of the ground plane provides two advantages:

   a. At high frequencies its low inductance provides a low impedance path for supply ground currents.

   b. It offers a constant characteristic impedance for signal interconnections.

2. The circuit layout employs a multipoint ground used in combination with parallel grounding. In this scheme each individual circuit is grounded to its own ground plane island by very short connections. All islands are connected to a star point which is connected to the supply ground. The advantage of this scheme is that at high frequencies the ground plane provides a low impedance path and at low frequencies the ground potential is determined only by the ground current and impedance of that circuit. This helps in minimizing differences in ground
potentials and hence ground noise.

3. Leads from one circuit to another (signal interconnections) are glued onto the ground plane. This helps split and therefore minimize coupling capacitance, reducing electrostatically coupled crosstalk and noise.

4. Radiation is a small problem at 14.32MHz of operation; yet lead lengths are kept as short as possible.

5. Noise due to high frequency switching is minimized by using 0.1uF ceramic capacitors to ground on all supply pins. In addition power supplies are decoupled using a simple R-C filter to reject frequencies higher than 30Hz coupled into the supply.

These construction techniques helped reduce noise considerably, improving circuit performance. Noise levels measured on the supply and ground leads of the Video Codec did not exceed 200mV, which is within the noise margin of the circuits employed.

4.7 Power Supplies

The Video Codec operates on five supplies: +15V, -15V, +10V, +8V and +5V. Laboratory power supplies were used to provide +15V and -15V. The laboratory power supplies must be capable of sourcing at least 250ma of current. The 10V, 8V and 5V are derived from the +15V supply using a monolithic voltage regulator (μA7805). Two versions of the μA7805 are used. One version, the μA78L05 has a current sourcing capability of 140mA while the other, the μA7805, can source up to 1.5A. These voltage regulators supply a 5V output but can be used as shown in Figure 4-14 to supply outputs from 5-15V. To prevent noise from being coupled
into the circuits via the power supply, each individual circuit's power supply is provided with a R-C decoupling filter at its input. This R-C filter is designed to reject frequencies above 30Hz. The R-C filtering is restricted by the drop across the resistor for higher resistor values. Thus in designing the filter the resistor is chosen based on the current drawn by the circuit. The capacitor is then chosen to achieve the desired cut-off frequency given by:

\[ F_c = \frac{1}{2\pi RC} \quad \text{where } F_c = \text{cut-off freq.} \]

\[ R = \frac{V_{\text{supply}} - V_{\text{input}}}{I_{\text{supply}}} \quad \text{where } V_{\text{supply}} = 15V \]
\[ V_{\text{input}} = \text{min. input voltage reqd. for the regulator.} \]
\[ I_{\text{supply}} = \text{current drawn by the regulator.} \]

![Figure 4-14: 5-15V Regulated Supply](image)

An L-C filter will provide more decoupling but does not remove noise as effectively as an R-C filter, since a R-C filter dissipates noise energy as heat but in an L-C filter
noise is not removed, rather it is shifted between the inductor and the capacitor, [15]. A 0.1µF ceramic capacitor is used across the 100µF decoupling capacitor to provide a low impedance path to ground for high frequencies; as the leads of the larger capacitor have fairly high inductance at these frequencies.

Each individual integrated circuit in the Video Codec is provided with an individual power supply. This scheme provides good isolation and minimal interference between circuits.
CHAPTER 5

IMPLEMENTATION OF THE DIGITAL FIELD MEMORY

5.1 Memory Requirements

The Digital Field Memory stores a page of Teletext information. The page corresponds to one field of a NTSC TV picture. Although TV pictures are normally displayed as frames (2 interlaced fields), it was decided to store only a single field to minimize memory requirements (capacity and complexity). It was observed that pictures of acceptable quality are obtained by storing and displaying a single field.

The size of the memory required to store a single NTSC TV picture field can be determined from the sampling frequency and the number of bits used to encode each sample. With a sampling frequency of 14.32MHz there are 14.32 million samples produced per second. Each sample is encoded as a 6 bit LPCM codeword. Therefore there are 85.92 (14.32x6) million bits produced per second. Since in the NTSC system a TV picture field occurs every sixtieth of a second there are 1.432 (85.92/60) million bits per field. Thus, a memory of 1.432 megabits is required to store a complete NTSC TV picture field.

A second requirement for the memories, used to store the field, is a fast read and write cycle time. Cycle times comparable with the encoding rate are desirable. This
reduces the need for buffers to equalize the encoding rate and the cycle times.

The field store was implemented using 24 (64Kx1) Dynamic Random Access Memories (DRAMs). The 24 DRAMs cost about $180(CDN) and accounts for the major cost of the proposed field store. With the introduction of the faster and larger 256K DRAMs and CCD memories the cost of a field store will drop considerably. Forecasters Figure that by 1988 256K DRAMs will sell for about 1 millicent per bit, [13] and hence a store with a capacity of 1.5 to 2.0 megabits would cost $15 to $20(us). The Philips Research Laboratories at Eindhoven, Netherlands, have produced a 308K bit CCD memory for video storage applications. This device has a simple serial structure(FIFO\textsuperscript{10}) that does not require address circuitry. Thus, the chip occupies a small area(34.8sq mm), [17] and the size is well suited for incorporating in a TV receiver. This chip will cost about $23(us), the same as the 256K DRAM, when introduced in 1985, [13].

Currently DRAMs offer the lowest storage cost per bit. In the designed memory 24 (64K) DRAMs, HYB4164-1, are used to implement the field store. The HYB4164-1 has the fastest

\textsuperscript{10}FIFO: First In First Out
read and write cycle time (250ns) available for DRAMs of this capacity (64K). Availability of this chip also influenced the choice.

5.2 Overview of Memory Design

The Digital Field Memory comprises four functional blocks as shown in Figure 5-1. These are a storage memory, a set of input buffers, a set of output buffers and a logic controller.

The storage memory serves to store the digitized TV field. The storage memory WRITE cycle time is four times as long as the required encoding rate. Therefore input buffers are used to assemble four samples for simultaneous writing into the memory. Similarly the memory READ cycle time is four times slower than the rate at which samples are to be read out, to create a NTSC TV picture. Output buffers are used to store four samples which are then given sequentially to the D/A converter for decoding. Thus, samples are multiplexed before storage and demultiplexed after reading from the store.

The logic controller controls and sequences operations of reading from and writing into the storage memory. The logic controller essentially comprises a control sequencer, an address generator, a read/write control logic and a sync detector. The control sequencer produces four clocks which are used to sequence data through the input and output
Figure 5-1: Schematic of Digital Field Memory
buffers. The address generator produces the addresses of the memory locations to be accessed during a read or write cycle. The Read/Write control logic produces the signals to write into or read from the storage memory. The Sync detector is used to detect the occurrence of vertical sync pulses, which are used to start and terminate the storage of a complete field.

In a multiplexed TV signal several fields occur successively, which are displayed as they arrive. The TV receiver does not have a facility whereby a user can view a particular field for a while. This can be achieved by storing the desired field in memory and displaying it at the standard NTSC field rate (60 fields per second). A STORE switch is provided which when depressed activates circuitry to store a field. When the switch is released the stored field is displayed until a new field is to be stored. This provision is analogous to the PAUSE feature in Video Cassette Recorders (VCRs). The designed circuit allows the storage of a single field, but there is no provision to select an individual field.

The scheme used for storing a field and reading it out for display is as follows:
Figure 5-2: Memory Write

Figure 5-3: Memory Read
Writing Into Memory<Storage>

When data is being written into the memory, a memory bypass path is used, as shown in Figure 5-2, to allow a display on the TV screen. To store a single field a STORE switch is depressed. This switch disables the memory output buffers and enables the data to pass through the bypass path. Simultaneously, data is written into the memory. The first vertical sync pulse that occurs, after the STORE switch is depressed, is detected by the sync detector and it is used to reset the address generator to the first memory location. The address generator is incremented, once during each write cycle, to access successive memory locations into which data is written. The next vertical sync pulse is detected and used to reset the address generator again to the first memory location. Thus, during the time between the two vertical sync pulses a complete TV field would have been written into the memory.

The vertical sync pulses occur every sixtieth of a second and hence during the time the STORE switch is depressed several vertical sync pulses will occur. Each successive vertical sync pulse begins writing a new field into the memory. The memory can store only one field and hence the new field is written over the previous one. When the STORE switch is released the storage of the current field continues until it has been completely stored in the memory. This is necessary, for if the storage of the field
stopped at the instant the switch was released, then the memory could contain data from two fields. Thus, when the memory contents are displayed the reproduced picture will not be as desired. When the STORE switch is released the field being written at that time will be completely stored.

Reading From Memory<Display>

When data is being read out of the memory for display the output buffers are enabled and the memory bypass path is disabled, as illustrated in Figure 5-3. Once again a vertical sync pulse is detected by the sync detector and is used to begin reading data out of the memory, by resetting the address generator to the first memory location. The address generator is incremented once every read cycle, to access successive memory locations containing the data to be read out. The next vertical sync pulse is detected and used to reset the address generator. This terminates the reading out of one complete field. The reading process is continuous and is terminated only by depressing the STORE switch, which then causes a memory write operation to begin. Since successive vertical sync pulses, occurring a sixtieth of a second apart, start the reading of the stored field, the stored field is displayed at a rate of 60 times per second. This rate is a standard in the NTSC system and allows a still picture to be seen on a TV screen.

Details of the Digital Field Memory design are
presented in the following sections. Each block of the digital memory is considered separately and its function and design features are outlined.

5.3 Storage Memory

The storage memory stores a digitized TV field. The HYB4164-1\textsuperscript{11} was selected in this design to implement the storage memory.

The HYB4164-1 is a high speed dynamic random access memory (DRAM), organized as 65,536 one bit words. The 65,536 bit locations are addressed by 256 row addresses and 256 column addresses. It has fast read and write cycle times of 250ns each and a long refresh period of 4ms. Appendix 1 contains a detailed description of its specifications.

Twenty four memory chips are used to provide 1.536 megabits of storage, which is adequate to store a complete field. The store is organized as four parallel memory banks, with each bank comprising 6 memory chips in parallel. Figure 5-4 illustrates the schematic of one memory bank. The parallel memory organization was chosen due to read and write cycle time limitations. The minimum write cycle time is 250ns, while the sampling time is 70ns. Thus,

\textsuperscript{11}from Siemens
Figure 5-4: A Single Memory Bank

multiplexing at the memory input is required if all the encoded words, of one field, are to be stored. This is done by storing four successive codewords from the A/D converter in four input buffers. These four words are simultaneously written into the four memory banks, each associated with one of the input buffers. This scheme results in four codewords being written into the memory every 280ns (70x4), which satisfies the minimum required write cycle time. Each codeword contains 6 bits and hence each bank is implemented with 6 memory chips in parallel.

The minimum read cycle time is 250ns. If the codewords
stored in the memory are read out at this rate and converted, by the D/A converter, to an analog signal, the frequency of this analog signal will be approximately one fourth that of the original signal, which was encoded at a rate of 70ns and stored. Therefore if the original signal is to be reproduced the memory contents must be read out at a rate of 70ns. The scheme adopted to achieve this as follows: Four codewords, one from each bank, are read out simultaneously into four output buffers during each read cycle. The buffers are then sequentially read at a rate of 70ns, which is the desired data output rate.

Hence, the parallel memory organization adopted eliminates the read and write cycle speed limitation. In this arrangement all memory chips have their corresponding address and read/write control lines tied together. Therefore any memory operation involves all the memory chips. This is convenient in memory refreshing.

The DRAMs are to be refreshed periodically, at least every 4ms, if their contents are to remain valid. Every time a location is addressed all locations in the same row are refreshed. Hence during each memory read or write cycle a complete row of locations will be refreshed. Each read or write cycle takes 280ns and since there are 256 rows the entire memory is refreshed in 71.68μs (280x256ns), easily satisfying the refresh period requirement (4ms). Hence in
the scheme of operation adopted, as the memory is being continuously read from or being written into the contents will be refreshed automatically and no separate refresh cycle is required.

5.4 Input Buffers

The input buffers serve to equalize the input data rate and the memory write cycle time. The double buffering arrangement of input buffers used is shown in Figure 5-5.

Each buffer is a Hex D-flip flop (DM74LS174). Data from a common input data bus to the four input buffers is sequenced using four clocks Q0, Q1, Q2 and Q3, shown in Figure 5-6 generated by the control sequencer. Clocks Q3, Q0 and Q1 enter three consecutive coded words, from the A/D converter into buffers F1, F2 and F3 respectively. The next clock Q2 enters the next coded word into the buffer I4 and simultaneously transfers the contents of buffers F1, F2 and F3 to buffers I1, I2 and I3 respectively. Thus, four codewords are simultaneously presented to the four memory banks, associated with the buffers I1, I2, I3 and I4, during each read cycle. During the memory write cycle time three new codewords are produced by the A/D converter, for storage. These three codewords are stored in buffers F1, F2 and F3 by Q3, Q0 and Q1 respectively. Thereby, this double buffering scheme prevents the contents of the buffers I1, I2 and I3 from being altered, by the new codewords produced, during a write cycle.
Figure 5-5: Input Buffer Arrangement

All times in nanoseconds.

Figure 5-6: Input Buffer Clocks
5.5 Output Buffers

The output buffers serve to equalize the memory read cycle time and the desired output data rate. Four output buffers, each associated with a memory bank, are used. The schematic of the arrangement is shown in Figure 5-7.

Each output buffer is an octal D-flip flop (SN74LS374) with tri-state outputs. An open collector or tri-state buffer is used as all the output buffers are connected to a common output data bus. This feature eliminates the need for separate multiplexers. Figure 5-8 illustrates the timing for sequencing the data out of the four output buffers 01, 02, 03 and 04. Four stored words are simultaneously clocked from the memory banks to the associated output buffers on the rising edge of clock Q1 (Co). The buffers are then sequentially enabled by applying their output enable pins low for a duration of 70ns. These enabling waveforms, shown in Figure 5-8 are generated by the logic controller.

5.6 Logic Controller

The logic controller controls and sequences the memory read and write operations. It comprises a control sequencer, an address generator, a read/write logic circuit, an output data sequencer and a sync detector.

5.6.1 Control Sequencer

The sequencer comprises two D-flip flops (SN7474)
**Figure 5-7: Output Buffers**

**Figure 5-8: Output Buffer Clocks**

**ALL TIMES ARE IN NANOSECONDS**
Figure 5-9: Control Sequencer Logic

Figure 5-10: Control Sequencer Timing

ALL TIMES ARE IN NANOSECONDS
interconnected as a Johnson counter is shown in Figure 5-9.

The two flip flops are synchronously clocked at 14.32 MHz by the system clock. The sequencer produces four clocks Q0, Q1, Q2 and Q3 (see Figure 5-10), each of frequency 3.58MHz and 70ns apart. These clocks are used for the following purposes:

1. Sequence the clocking of data into the input buffers.
2. Generating signals to sequentially enable the data out of the output buffers.
3. Increment the memory address generator.
4. Generate the memory read/write control signals.

5.6.2 Output Data Sequencer

This circuit sequentially clocks the data out of the output buffers. The enabling waveforms, shown in Figure 5-8, are generated by decoding the four clocks Q0, Q1, Q2 and Q3 produced by the control sequencer. The decoder is implemented using two four input NAND gates (SN7420) as shown in Figure 5-11. A strobe (disable) input is provided for the NAND gates of the decoder. When the STORE switch is depressed and data is being written into the memory, the output buffers are to be disabled as mentioned earlier. This is done as follows: The strobe input is taken LOW causing the outputs of all the NAND gates of the decoder to go HIGH. These NAND gate outputs are connected to the output enable pins of the output buffers. These are active
low pins and hence the output buffers are disabled (outputs are tri-stated).

5.6.3 Address Generator

Figure 5-12 is a schematic of the address generator. Sixteen address bits are required to decode 1 of 65,536 memory locations, each located with a 8-bit row and a 8-bit column address. These sixteen address bits are provided by means of a 16-bit counter, implemented using four binary counters (SN74161). The SN74161 is a four bit counter with a carry look ahead facility that allows cascading of several of these counters to obtain a fast n-bit synchronous counter. The lower 8 bits of the address counter are used to address the memory rows while the upper 8 bits are used to address the memory columns. The counter is incremented
Figure 5-12: Address Generator

once every read or write cycle (280ns) by clock Q0. In this addressing scheme the column address remains constant while the row address is incremented 0 to 255 and then the column address is incremented and so on. The lower 8 bits of the counter were chosen to represent the memory row addresses to satisfy the memory refresh requirement. All memory locations in the memory should be refreshed at least once every 4ms. Refreshing is done by accessing rows. When a row is accessed all locations of that row are refreshed. Since there are 256 rows and a row address is presented every 280ns, in our addressing scheme, a complete memory refresh takes 71.68μs (256x280ns).
The memory chips (HYB-4164-1) have only eight address pins (A0-A7). Hence a data selector or multiplexer (2:1) is used to present the row and column addresses to the memory chips. The row address is first selected and set up on the address pins (A0-A7) and then latched onto the chip by a row address strobe (\( \overline{\text{RAS}} \)). Next, the column address is selected and latched onto the memory chips by a column address strobe (\( \overline{\text{CAS}} \)). The selection of rows and columns is implemented using two SN74157 2:1 line multiplexers whose select input is driven by an address select signal. This address select signal and the \( \overline{\text{CAS}}, \overline{\text{RAS}} \) signals are generated by the read/write logic circuitry.

When a video pattern, from a NTSC pattern generator, was stored and displayed errors appeared as spurious black and white dots on the displayed pattern. These errors were traced to the following condition: whenever the row address 00000000 occurred the memory would produce bit errors. It appeared as if the memory was storing random data in the locations corresponding to the row address 00000000. The experiment used to trace the problem was as follows: a sinusoidal signal of 5KHz was stored in the memory and displayed on an oscilloscope. The errors were observed as glitches on the displayed sinusoidal signal. All the row address bits were fed to a 8 input NOR gate and the output of the gate was used to trigger the oscilloscope. It was observed that the glitches occurred whenever the row address
was all zero and the gate output was 1.

The timing of the memory read and write operations was checked. Further the circuit was checked to identify if switching noise was the problem. These checks gave no indication of why the errors were occurring. No reason was found for the problem experienced.

The errors were eliminated by not allowing the row address to go to 00000000. This is done as follows: the row address following 11111111 is 00000000. When the row address reaches 11111111 the ripple carry output of binary counter#2 goes LOW for a duration of one clock period. This signal is used to load the number 0001 in binary counter#1. Thus the row address following 11111111 is 00000001, which obviates the all zero row address and the resulting bit errors produced by the memory.

The address counters are reset by the vertical sync pulses detected and regenerated by the sync detector.

5.6.4 Read/Write Control Logic

The read/write control logic provides four signals that control memory read and write operations. The signals produced are:

1. Row Address Strobe(\text{RAS}): To latch the row address onto the memory chips.

2. Column Address Strobe(\text{CAS}): To latch the column
address onto the memory chips.

3. Read/Write signal(R/W): To read from and write to the memory.

4. Row/Column select: To select row and column addresses, from the address counters, using a 2:1 multiplexer.

The RAS, CAS, Row/Column select signals are generated from the clocks Qo and Q1 of the control sequencer using a D-flip flop (DM7474), two AND gates (SN7408) and two EX-OR gates (SN7486) as shown in Figure 5-13. The timing diagram of the signals produced by the read/write control logic is illustrated in Figure 5-14. These signals satisfy the read/write cycle timing specified by the manufacturer for the memory chips. Appendix 1 contains a list of these specifications.

The read/write signal is produced using a D-flip flop (DM7474) as shown in Figure 5-15. The input to the D-flip flop is the output of a contact debounce circuit for the STORE switch. The flip flop is clocked by the vertical sync from the sync detector. To begin writing into the memory the STORE switch is depressed (LOW). The D-flip flop output goes LOW after the first vertical sync pulse and remains LOW on subsequent vertical sync pulses until the STORE switch is released (HIGH). As long as Qd is LOW data can be written into the memory. On the next vertical sync pulse Qd goes high and data can be read from the memory. Since the D-flip flop is clocked by the vertical sync pulse, its output
Figure 5-13: Read/Write Control Logic

Figure 5-14: Memory Read/Write Timing
cannot change state from HIGH to LOW (start write) and then LOW to HIGH (stop write) before the occurrence of two vertical sync pulses. Thus, Qd will be LOW (MEMORY WRITE) for the duration between two successive vertical sync pulses and hence a full field can be written into the memory. In the normal state Qd is HIGH (MEMORY READ) allowing continuous reading from the memory.

5.6.5 Sync Detector

The sync detector serves to detect the occurrence of the vertical sync pulses in the composite video signal that is to be stored. These detected vertical sync pulses are
used to START and STOP the storage of one complete field. The circuit used is shown in Figure 5-16.

The sync detector comprises of a clipper, an integrator, a threshold detector and a monostable multivibrator.

Clipper

The clipper removes the horizontal and vertical sync pulses from the composite video signal. A comparator (LM311) is used to implement the clipper as shown in Figure 5-16. The capacitor C1 blocks the DC level of the composite video signal. Resistors R1 and R2 serve to bias the input at 500mv to prevent noise from triggering the comparator. The negative going horizontal and vertical sync pulses (-0.5V) will trigger the comparator to produce an output.

Integrator

The integrator serves to separate the vertical sync from horizontal sync pulses obtained at the output of the clipper. The vertical sync pulses are of the wide width (830us) while the horizontal sync pulses are of the width (5.08us). To separate these pulses an integrator with a long time constant (26.4ms) is used. Due to a long time constant, the capacitor of the integrator charges and discharges slowly and will not produce an appreciable output.
Figure 5-16: Sync Detector

Figure 5-17: Separation of Vertical Sync
for the shorter horizontal sync pulses. The output of the integrator is illustrated in Figure 5-17.

**Threshold Detector**

This is a Schmitt trigger implemented using a LM311 comparator as shown in Figure 5-16. The threshold level is adjusted by a potentiometer P4 so that only the integrated vertical sync pulses can trigger the comparator to produce an output. Resistor R5 is used to provide hysteresis (positive feedback) for greater noise immunity. The output of this stage is a negative going vertical sync pulse of approximate duration 160µs.

**Monostable**

The address counters have an active LOW asynchronous reset. Therefore, if the wide vertical sync pulse from the output of the threshold detector were used to reset the address counters, the counters will be disabled for the entire duration of the vertical sync pulse (160µs). During this time 2286 (160µs/70ns) digitized codewords, from the A/D converter will be produced and will not be stored, as the address counters are disabled. The codewords that will be lost are the ones that represent the vertical sync pulse of the TV field to be stored. Hence the stored picture will have no vertical sync pulse. When such a picture is displayed on the TV screen it rolls up or down. To avoid this the address counters should be reset by a narrow
vertical sync pulse, which disables them only for a very short duration. A monostable (SN74121) is used to produce a narrow vertical sync pulse. The monostable is triggered by the wide vertical sync pulse from the output of the threshold detector and it generates a narrow vertical sync pulse (width=104ns). This narrow vertical sync pulse is used to reset the address counters.

5.7 Interface Buffers

Two additional buffers are used in the designed memory to serve as an interface between the Video Codec and the Digital Field Memory. These buffers are clocked D-flip flops (SN74174). Buffer B1 receives data from the A/D converter via a ribbon cable. The data received at the memory input buffers was observed to be noisy. Buffer B1 is used to latch the incoming data and regenerate a "clean" output to the input buffers.

During a memory read operation it is observed that, with the sequencing scheme adopted for enabling the output buffers, for a short duration in each enabling interval the outputs from two buffers are present on the common output data bus. This is because the enabling signals from the output data sequencer overlap for a short interval, as shown in Figure 5-8. To ensure that the proper data is decoded by the D/A converter, buffer B2 is clocked at an instant when the data from only one output buffer is valid. Buffer B2 latches the data from the memory output buffers during
memory read and data from the bypass path during memory write and transmits the data to the deglitch latch of the Video Codec at a fixed instant.

5.8 Bypass Circuit

During a memory write operation data from the A/D converter is sent to the memory output buffers. This data is also transmitted via a memory bypass path to the D/A converter, where it is reconverted to an analog signal for display. This allows a picture to be displayed while writing into the memory. When the data from the memory is being read out, data through the bypass path must be disabled. This is done by using a bypass circuit, implemented using an Octal D-type latch (SN74373). The latch is enabled during a memory write operation and disabled during a memory read operation.

It was observed that the data arrives at buffer B2, during a memory read, at a different time from that during a memory write cycle. Since the deglitch latch is to be clocked only after the data at its inputs has met the set-up requirements, this difference in the arrival of data during a memory read and memory write cycle causes a problem in the instant of clocking. The bypass latch introduces a delay in the bypass path that minimizes the time difference in the data received at the buffer B2, during a memory read and memory write operation. This helps in clocking buffer B2, at a fixed instant, with the required data set-up time.
5.9 Phasing Circuit

The relation between the color sub-carrier frequency and the horizontal line frequency is such that there is an odd multiple of half cycles (227 1/2) on each horizontal line. Successive fields are separated by a difference of half a horizontal line. This half line difference results in a quarter cycle difference of the sub-carrier phase on successive fields. This is equivalent to saying that the sub-carrier phase is shifted by 90 degrees on successive fields. Therefore, to define a complete NTSC TV picture four fields are to be stored; since after four fields the sub-carrier phase has rotated through 360 degrees. Storing four fields is uneconomical as the memory chips (HYB 4164-1), alone, will cost $720(CDN). As an alternative, a single field can be stored and the effect of shifting the sub-carrier phase on successive fields can be simulated using a phasing scheme.

A 90 degree phase shift corresponds to quarter cycle delay of the sub-carrier. Since the sub-carrier frequency is 3.58MHz, this delay is approximately 70ns which incidentally is the sampling rate. Therefore, if a single field is stored and read out each time with a 70ns delay (one sample duration) the required 90 degree phase shift of the sub-carrier in successive fields is achieved.

In the color TV receiver hue information is demodulated
from the chrominance signal, for which a 3.58MHz sub-carrier is locally generated by a crystal oscillator. Proper phase relation between this generated sub-carrier and the chrominance signal sub-carrier determines whether the hues will be demodulated correctly. If a single field is stored and read out repeatedly for display without the required 90 degree phase shift, on successive fields, the phase relation between the chrominance sub-carrier and that generated by the TV crystal oscillator will be correct for only one out of four fields. Thus, the hues in the displayed picture will not be stable. This was observed and a sub-carrier phasing scheme was considered necessary.

The phasing scheme adopted is as follows: the control sequencer is clocked by the system clock at 14.32MHz and it generates four clocks Q0, Q1, Q2 and Q3 of frequency 3.58MHz and 70ns apart. This 70ns delay is equal to one quarter the sub-carrier cycle. These clocks (Q0 through Q3) are used to enable the memory output buffers and therefore control the reading from the Digital Field Memory. Hence, if these clocks are sequenced appropriately in each successive field the required 90 degree phasing can be achieved. This sequencing occurs automatically in each successive field if the system clock that clocks the control sequencer is phase locked to the sub-carrier frequency of the signal to be digitized. This is achieved by using the 3.58MHz sub-carrier derived from the input signal to phase reference
a PLL frequency multiplying circuit which generates the 14.32MHz system clock [Section 4.5]. Using this scheme, storage of a single field was seen to be adequate for display of a still picture.

The scheme used has two limitations. The first limitation is that a picture with stable hues is seen only if the sequencer is clocked at exactly four times the sub-carrier frequency (14.31818MHz±100Hz). The second limitation is that a circuit is required to demodulate the sub-carrier in the incoming TV signal. This sub-carrier is then used to phase reference the system clock. This means that a portion of the TV receiver (sub-carrier demodulation) must be built into the proposed design.

5.10 Construction Technique

The construction technique used to implement the Digital Field Memory is similar to that adopted for the Video Codec. Ground plane construction is used. The ground plane helps to provide a constant characteristic impedance for interconnecting wires and also provides a low inductance ground. At high frequencies of operation, such as in the designed circuit, the low inductance ground helps to reduce the difference in ground potentials at different points in the circuit.

Current spikes due to high frequency switching is minimized by using 0.1μF capacitors on the supply pins of
the integrated circuits used. In addition the power supply to the Digital Field Memory board is decoupled using a simple R-C filter that rejects frequencies higher than 30Hz from being coupled into the supply.

It was observed that there was excessive ringing on the address lines and memory read/write control lines. This ringing is due to reflections that occur on an unterminated line, [7]. If the ringing (oscillations) in the negative direction exceeds -0.7V the memory could be damaged. The ringing was minimized considerably by terminating each line with an effective resistance of 180 ohms.
CHAPTER 6

PERFORMANCE TESTING

The performance of the designed Video Codec and the Digital Field Memory is characterized by a set of parameters. This chapter describes tests adopted to measure performance in terms of these parameters. Each performance characterizing parameter is explained to define what it implies. These definitions are considered necessary as the parameters in focus could have a different implication in a different test environment. The definitions are followed by a description of the test adopted to obtain a performance measure.

The tests are grouped into four categories, based on the component blocks of the system. This grouping serves to identify critical characteristics of the component blocks, which would seriously impair overall system performance if not satisfied. The choice of the tests was largely dictated by the availability of testing equipment. However, the tests conducted afford a good measure of the important parameters characterizing the designed Video Codec's performance. A function generator, an oscilloscope, a vector monitor, a video monitor and a distortion analyser were used to conduct all the tests in this thesis.
The following tests were conducted:

1. Amplifier Tests
   
   a. Frequency Response
   b. Square Wave Response

2. D/A Converter Tests
   
   a. Differential Non-Linearity and Monotonicity

3. Video Codec Tests
   
   a. Linearity and Accuracy
   b. Bandwidth
   c. S/N Ratio
   d. Differential Gain and Differential Phase
   e. Color Bar Response

4. Digital Field Memory Tests.

6.1 Amplifier Tests

   The frequency response of the input and output video amplifiers of the Video Codec can limit the overall system bandwidth. Any frequency and phase distortion introduced by the amplifiers will impair the reproduced picture as explained in Section 3.1. Thus, amplifier tests are aimed at determining the frequency and phase distortion, if any, of the input video amplifier and the output video amplifier. The amplifiers in the system must have linear phase and a bandwidth of 4MHz. The low frequency response must be flat
down to 30Hz and extend to 10Hz.

**Frequency Response**

A range of frequencies from 10Hz to 5MHz were fed to the amplifier and the output response was measured. A sinusoidal signal generated by a function generator was used as the input. An oscilloscope or RMS voltmeter can be used to measure the output and input levels. A dual trace oscilloscope was used to observe the input and output simultaneously; a method useful in observing phase shifts. The output amplitude versus the frequency of the input signal was measured and the the bandwidth determined. The amplifiers were observed to have a wide bandwidth extending from 10Hz to 4MHz, satisfying the video frequency requirements.

**Square Wave Response**

An approximate and practical method of detecting video amplifier troubles, is to observe the response of the amplifier to a square wave. Frequency and phase distortion alter the shape of the output response which should ideally be a square wave. A low frequency square wave (60Hz) was used to test the low frequency response of the amplifier. A high frequency square wave (25KHz) was used to test the high frequency response of the amplifier. A function generator was used as the source to the amplifier and the input and output are observed on a dual trace oscilloscope. Care was
taken not to drive the amplifier into saturation by the
input as this causes clipping of the tops of the output
makes the observation of distortion difficult. Figure 6-1
adapted from [12], provides a summary of symptoms observed
for common video amplifier troubles, using the square wave
test. The test was conducted and observations indicated
that the amplifiers have little waveform distortion.

<table>
<thead>
<tr>
<th>INPUT TO VIDEO AMP</th>
<th>SHAPE OF OUTPUT</th>
<th>INTERPRETATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 Hz</td>
<td></td>
<td>Good low freq. response.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>constant delay or linear phase</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low freq. phase lead.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low freq. attenuation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low freq. phase lag.</td>
</tr>
<tr>
<td>25KHz</td>
<td></td>
<td>Good high freq. response.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High freq. attenuation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Oscillation due to excessive high freq. response and phase shift.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Poor mid freq. response and phase distortion.</td>
</tr>
</tbody>
</table>

Figure 6-1: Video Amplifier Troubles
6.2 D/A Converter Tests

Differential Non-Linearity and Monotonicity

Differential Non-Linearity

Ideally if the digital value of the input word to a D/A converter changes by one bit (1 LSB) there should be a corresponding constant increment in the analog output. If the analog output changes by varying amounts there is differential non-linearity in the D/A conversion. Differential non-linearity is thus a measure of the actual increment in analog output compared to the ideal increment expected for a one bit change in the digital input to the D/A converter.

Monotonicity

A D/A converter is monotonic if its analog output increases uniformly with a corresponding increase in the weight of the input digital word. Non-monotonicity occurs when the differential non-linearity error is greater than the weight of 1 LSB.

Figure 6–2 illustrates these two D/A conversion errors.

![Figure 6-2: D/A Conversion Errors <3 Bits](adapted from [19])

Non-monotonicity causes the reproduced video picture to be distorted with discontinuities and gaps and straight lines in the pictures will have wobbles, [19]. Line and dot
patterns show up with irregular spacing. Monochrome pictures are observed to have improper shades.

Monotonicity and differential non-linearity were tested with the circuit shown in Figure 6-3. The digital sequence generator produces a binary sequence that increases from 0 to 63 and then decreases from 63 to 0, in a cyclic manner. This sequence was fed to the six least significant bits of the D/A converter. The output of the D/A converter was observed on an oscilloscope. The output obtained is illustrated in the Figure 6-4. The following information can be obtained from the output (staircase) waveform:

1. The step heights (size) and spacing is a measure of non-linearity. The step size is 1 LSB.

2. If the steps do not increase monotonically as the input increases from 0 to 63 and decrease monotonically as the input decreases from 63 to 0 then the D/A converter is non-monotonic.

3. Glitch energy at major bit transitions can be observed by expanding a step on the oscilloscope.

The D/A converter output illustrated in Figure 6-4 was observed to be monotonic.

6.3 Video Codec Tests

The tests described hereunder are adapted from [20], [21] and [22].

Linearity and Accuracy

Accuracy of a D/A converter is the
Figure 6-2: D/A Converter Test Circuit

Figure 6-3: D/A Converter's Response to Test Input
difference between the theoretical and measured analog output for a given input digital code. For an A/D converter it is the difference between the theoretical and actual input analog value required to produce a specific digital code. Since the Video Codec contains an A/D converter and a D/A converter the above definition can be generalized: Accuracy of a Video Codec is the difference between the actual and theoretical analog output values for a given analog input.

**Linearity**

Theoretically the conversion relationship between input and output of a codec can be expressed as a straight line. Linearity, then is a measure of the maximum deviation, from this straight line, when a plot of input versus output is made from measured values.

Linearity errors cause distortion in pictures or graphics. Text is not affected as much.

**Figure 6-5: Linearity Test**

Linearity error of a Video Codec should not exceed $\pm 1/2\text{LSB}$. Quantization results in an inherent error of $\pm 1/2\text{LSB}$. Thus the overall accuracy of the Video Codec is required to have an error less than $\pm 1\text{LSB}$ or 2LSBs peak to peak [20].
Figure 6-5 shows the test set-up to measure linearity. The test comprises of feeding a 25KHz ramp input from a function generator to the Video Codec and to one channel of a dual trace oscilloscope. The output of the Codec was fed to the second channel of the oscilloscope. The oscilloscope was set in the differential (subtract) mode. Thus, the waveform observed on the scope was the error waveform. This error waveform should not exceed 2LSBs peak to peak.

In the test performed the peak to peak linearity error was observed to be slightly less than 2LSBs (125mv).

**Bandwidth**

Bandwidth is the range of frequencies that the Video Codec can pass without attenuation.

Since the sampling rate is 14.32MHz the A/D converter can handle signals up to 7.16MHz in frequency which is more than the required video signal bandwidth of 4MHz. Essentially, in the Video Codec designed the bandwidth is determined by the input and output amplifiers, whose frequency response is measured as described under the amplifier tests.

**Signal to Noise (<S/N>) Ratio**

S/N Ratio This is the ratio of the RMS signal to RMS noise level, measured at the Video Codec output.
A HP\textsuperscript{12} distortion analyser (334A) was used in the measurement. A full load sine wave with a fundamental frequency of 50KHz was fed to the Video Codec. The output of the Video Codec was fed to the distortion analyser. With the analyser set to the "distortion" measuring mode, the output was measured in dB. This is essentially a measure of the RMS signal to noise ratio. The theoretical RMS signal to noise ratio for a sinewave signal is $6N + 1.8$ dB, [16]; where $N =$ the number of bits in the digital word. Thus for a full load sinusoidal signal, the minimum signal to noise ratio for 6 bit encoding is 37.8dB. However, for a LPCM NTSC TV signal the S/N ratio will be slightly different from the theoretical value, [1]. This is because the luminance component is only 57 percent of the composite signal and secondly, the quantizing noise will be band-limited to 4.2MHz (Video bandwidth). The net effect is to reduce the peak signal to RMS noise ratio. The RMS S/N ratio remains approximately same.

A S/N ratio of 36dB allows fairly good color picture reproduction. The RMS S/N ratio of the Video Codec, measured using the distortion analyser was 32.5dB. This indicates a reduction of 5.3dB from the ideal value of 37.8dB. This reduction is due to noise from the digital

\textsuperscript{12}Hewlett Packard
circuits of the designed system.

**Vector Monitor**

The remaining Video Codec tests make use of a Vector Monitor. The Vector Monitor provides a visual display of the amplitudes (saturation) and relative phase angles (hues) of the chrominance component of the NTSC color signal. This allows us to check, with a standard test signal, whether the encoding has been carried out properly. Two types of display options are provided by the Vector Monitor. A Polar display, in which each individual color is represented as a vector whose length is equal to the signal amplitude and phase is relative to the reference color burst phase. The display for each color on the Vector Monitor is a vector which resembles two dots with faint lines joining them. Figure 6-6 illustrates the display graticule that is used for interpreting Vector displays of the chrominance component of a color signal.

A second display option, the Line display, allows a presentation of luminance signal amplitudes. This mode is also used for measurement of differential gain and differential phase, which are two important measures of a Video Codec's performance. Figure 6-7 illustrates the Vector Monitor display graticule for this measuring mode.

The instrument used in the remainder of the tests described in this section was a fairly sophisticated Vector
Figure 6-6: Polar Display of Vector Monitor
(adapted from Instruction Manual for the Tektronix NTSC Vectorscope 520A)
Figure 6-7: Line Display of Vector Monitor

(adapted from Instruction Manual for the Tektronix NTSC Vectorscope 520A)
Monitor, the Tektronix NTSC Vectorscope (520A). A measurement is made by applying a specific input signal to the device under test and selecting one of the display measurement functions. An appropriate display is then provided from which measurement of errors can be directly recorded or observed.

Details on the Vector Monitor used in the following tests can be obtained from the instruction manual for the Tektronix NTSC Vectorscope (520A).

**Differential Gain and Differential Phase**

A color signal has two components; a luminance and a chrominance component. If the gain or phase of the chrominance signal varies as a function of the luminance signal, distortion in the color signal results. Differential gain and differential phase are measures of this distortion.

**Differential Gain**

A small sub-carrier signal is superimposed on a black level luminance signal. The percentage change in the sub-carrier amplitude is measured, as the luminance signal is varied from the black level to the white level. This measure is referred to as differential gain.

**Differential Phase**

This is the largest phase change of a small sub-carrier component superimposed on a luminance signal that varies from black level to white level. This phase change is measured with reference to the phase of the sub-carrier at black level. Usually this
measurement is carried out at, only, two levels of the luminance signal. The larger phase reading is taken as the differential phase.

In terms of the reproduced picture, differential gain errors cause the saturation of colors to be distorted in areas between light and dark portions of the screen. Differential phase errors cause the hue to vary with the brightness of the scene.

![Modulated Staircase Signals](adapted from [20])

Figure 6-8: Modulated Staircase Signals

The test comprises of feeding a 40IRE\(^{13}\) (1V=140IRE units) unit modulated staircase signal, as shown in Figure 6-8, to the Video Codec input. The modulated staircase signal has a luminance component, that increases in steps from the black level to the white level, and a 3.58MHz sub-carrier component (chrominance) superimposed on

\(^{13}\)IRE=Institute of Radio Engineers, now called Institute of Electrical and Electronic Engineers (IEEE)
each luminance step. Therefore, this signal is useful in measuring the variation of sub-carrier phase (differential phase) and amplitude (differential gain) at different luminance levels.

The codec output was observed on the 520A Vectorscope. Differential gain and differential phase are measured from the displays provided by the Vectorscope. During the measurement, the video codec sampling frequency was unlocked from 14.32MHz by about 100Hz. This is suggested in [20] to obtain a clearer display.

Differential gain upto 8 percent and differential phase upto 3 degrees are considered acceptable values for well designed Video Codecs [20].

Color Bar Response

The color bar response was used to observe color purity in the reproduced video picture after passing through the codec. The test may be done in two ways. The first is subjective and the second uses the 520A Vectorscope.

In the first method a 75 percent fullfield color bar signal from a NTSC pattern generator was fed to the Video Codec. The output of the codec was displayed on a Video Monitor. The displayed picture observed was compared with that obtained by directly displaying the input, to the
Figure 6-9: FullField Color Bar Signal

codec, on the Video Monitor. A subjective comparison was then made.

In the second method instead of a Video Monitor the codec output was fed to the 520A Vectorscope, set in the fullfield mode. The 75 percent fullfield color bar signal, shown in Figure 6-9, was used as the test signal.

The Vectorscope display graticule (Polar Mode) has a number of tolerance squares that lie along specific axes and at a fixed distance from its center as shown in Figure 6-6. The axes represent the phase angles corresponding to the different hues of a fullfield color bar test signal. The distance of the tolerance squares from the center of the graticule corresponds to the saturation of the colors in the test signal. Hence for a pure picture (no amplitude and
phase distortion) distinct vectors in the form of faint lines are seen to lie along the specific color axes and terminate in the tolerance squares. If the vectors fall short of the tolerance squares, amplitude distortion and poor saturation or purity of colors are present. Phase distortion and incorrect hue reproduction will result if the vectors do not lie on their respective axes (usually seen as blurred lines).

Figure 6-10: Errors in Color Picture
(adapted from [20])

6.4 Digital Field Memory Tests

All the tests conducted for the Video Codec can also be conducted with the Field memory connected. This will indicate if any distortion is introduced by storing and reading out of the memory.

The fullfield color bar response and the differential phase and gain tests are the most significant tests for evaluating the performance of the Video Codec and the Field Memory (Store). The results of these tests are presented in the following section.
6.5 Discussion of Results

A fullfield color bar test pattern from a NTSC pattern generator was digitized and stored in the designed system. The stored pattern was displayed on a Video Monitor and a photograph of the display was taken. A photograph of a direct display of the test pattern on the Video Monitor and a photograph of the display obtained by passing the test pattern through the Video Codec were also taken. These photographs are presented in Figure 6-11, Figure 6-12 and Figure 6-13 respectively.

Observations of the three displays obtained on the Video Monitor indicate that there is a reduction in saturation of the displayed color bars when the color bar pattern is passed through the Video Codec. A slightly greater reduction in saturation is observed when the color bar pattern is stored and displayed. No change in hue or tint in the colors were perceptible from the three displays. Further, it was observed that the reduction in saturation of the colors for the three displays is less visible on a Video Monitor than it is in the photographs presented. The loss of saturation is due to a reduced high frequency response (greater than 3.6MHz) of the input and output amplifiers of the designed system. However, this loss of response was not observed over the video band of frequencies, when the amplifiers were tested with a sinusoidal signal.

The color bar test was repeated using a monochrome bar
Figure 6-11: Display of Stored Color Bars
Figure 6-12: Display of Color Bars (Direct)
Figure 6-13: Display of Color Bars Thru Video Codec
pattern, from a NTSC pattern generator. The results obtained are illustrated in Figure 6-14, Figure 6-15 and Figure 6-16. It is seen that the three displays are very similar and indistinguishable indicating that the Video Codec and Field Store work very well for monochrome TV signals.

The Vectorscope display obtained by passing a 75 percent fullfield color bar test signal through the Video Codec indicated no distortion of hue, that may have occurred by digitizing the picture. There was a reduction in the saturation level (about 20 percent) in the colors, as was observed in the display of the test color bars on a Video Monitor. Photographs of the Vectorscope display for this test were taken and are presented in Figure 6-17.

The reduction in saturation is not seen on the photograph because the sensitivity (gain) of the Vectorscope was raised during this observation. This was done to aid the reading of the shift in phase of the color vectors, from the graduated markings on the circumference of the Vectorscope graticule. Photographs of the Vectorscope display showing the 20 percent reduction in saturation were unfortunately not taken during the photographic session.

When the Field Store was used to store the 75 percent fullfield color bar test pattern and display it on the Vectorscope, the display comprised of concentric circles
Figure 6-14: Display of Stored Monochrome Bars
Figure 6-15: Display of Monochrome Bars (Direct)
Figure 6-16: Display of Monochrome Bars Thru Video Codec
**Figure 6-17:** Vectorscope Display for FullField Color Bar Test
indicating rotating color vectors and a useful observation of color saturation and hue could not be made. However, the display of the fullfield color bar test pattern on a Video Monitor, with and without the use of the Field Store was fairly similar indicating that the corresponding Vectorscope displays should be similar. This was not so and an explanation for this is not immediately evident.

Differential phase measurements indicated a measure of 2 degrees, which is an acceptable amount of phase distortion of the color sub-carrier as a function of the luminance signal variation. Physically, this means that the tint of the colors in the reproduced picture will not change, noticeably, with brightness variations. Photographs of the Vectorscope display for this test were taken and are presented in Figure 6-18.

As with the fullfield color bar test, a differential phase measurement could not be made on the Vectorscope, when the Field Memory was used to store the test pattern and display it on the Vectorscope. The display observed for this test on the Vectorscope was very noisy and unstable, precluding a proper measurement to be made.

The Vectorscope used for the tests had a faulty circuit that precluded a proper measurement of differential gain. As a result the differential gain test was not made for the
Figure 6-18: Vectorscope Display for Differential Phase Test
Video Codec and the Field Store.

Additional tests conducted on the Video Codec and the Field Store involved testing the quality of a displayed picture, color and monochrome, by reducing the number of bits in each LPCM sample. It was observed that for respectable color pictures 6 bit encoding was essential. Acceptable monochrome pictures were obtained for 4 bits, with some contouring in the displayed picture. In conclusion it may be stated that with 6 bit encoding, pictures obtained for color and monochrome were of good quality. A display of a digitized and stored image on a Video Monitor of a color slide is shown in Figure 6-19. Photographs of the same slide displayed directly on the Video Monitor and through the Video Codec, respectively, are also presented in Figure 6-20 and Figure 6-21 for comparison.
Figure 6-19: Display of Stored Color Picture
Figure 6-20: Display of Color Picture (Direct)
Figure 6-21: Display of Color Picture Thru Video Codec
CHAPTER 7
CONCLUSIONS

The major objective of this project was to design and build a low cost Field Store, capable of storing a single field of a NTSC TV picture. The perceived application of this Field Store is in TV receivers for Teletext and still Video reception.

The project was conducted in three steps. First, a Video Codec was constructed as described in Chapter-4. A Digital Field Store was then constructed and interfaced with the Video Codec, as described in Chapter-5. Finally, the designed system comprising the Video Codec and the Field Store was tested to evaluate its performance.

Test results indicated that monochrome patterns can be stored and displayed without any visible distortion. Color patterns can also be stored, but display of the stored pattern indicated a reduction in saturation. However, there is no perceptible reduction in the tint or hue of the colors that are displayed after storage. Further, a color picture was digitized and stored. The display of the stored image subjectively indicated a picture of good quality.

In order to evaluate the performance of the Video Codec and the Digital Field Store, more thoroughly, a number of tests such as: chrominance-luminance distortion,
chrominance phase, 2T-pulse, and 12.5T-pulse tests, [20] were to be performed. These tests would have provided valuable performance measures that would have helped to diagnose problems with the designed system. These tests were not performed, as equipment to provide the required test signals was not available.

The cost of the components in the Video Codec and Digital Field Store is estimated at $300(CDN). The major component of this cost is contributed by the memory chips that store the digitized TV field. These chips cost $180(CDN) and make Digital Field Stores rather expensive to be included as a standard feature in TV receivers. Larger and faster memories such as the 256K DRAM and the Philips 308K CCD memory will be available in 1985, at an estimated cost of $23(US). It is anticipated that by 1988 these memories will cost around $3(US) apiece and a Digital Field Store with memory capacity of 2 to 3 megabits can be economically installed as a standard feature in TV receivers. At that stage the concept of Teletext decoding using the scheme mentioned in this project would be simple and very cost effective.

Possible future work on this project includes performance enhancement and applications. The work would include modifications and extensions. In terms of performance enhancement the phasing scheme adopted to
maintain the phase relationship between the regenerated sub-carrier and chrominance signal on successive fields, could be changed. The current scheme has two disadvantages as mentioned in Section 5.9. The current phasing scheme appears to interfere with the Digital Field Store measurements on the Vectorscope. Further, the phasing scheme can be eliminated if four successive fields were stored. This is economically feasible only after the cost of memory drops considerably.

A single page of Teletext information, corresponding to one TV picture field, can be stored and displayed by the designed system. In a Teletext system several pages are broadcast in a cyclic manner. Selection is possible as individual pages are numbered. Pages may be selected with a Keypad, similar to that of a pocket calculator, and associated circuitry. The design and fabrication of such a circuit to select individual pages is an useful extension of this project.

Teletext pages can also be sent as coded information on the horizontal lines that occur during the vertical blanking interval of a TV signal. A unit to detect the vertical blanking interval and then store the next sixteen or so horizontal lines can be designed. The Digital Field Store augmented with this unit would be very useful even in the existing Telidon system, as it can be used to provide a
store of several pages of Teletext information. The pages of information thus stored can be decoded by a microprocessor decoder and displayed. Such a store for several pages is sometimes referred to as a Background Memory.

In concluding this thesis, it is to be mentioned that a Video Codec and Digital Field Memory can be applied to diverse applications in the Television industry. A few of these applications are listed below:

1. Standards conversion or Transcoding.
2. Time base synchronization.
3. Elimination of large area flicker.
4. Reduction of Noise in TV pictures.
5. Picture processing and image enhancement.
6. High definition TV.

Most of the above applications involve digital processing of video signals and hence arises the requirement for a Video-Codec and a Digital Field Store.
REFERENCES


23. Goodall, W.M. Television By PCM. BSTJ 30 (JAN 1951), 47.
I. APPENDIX 1

I.1 Data Sheets
The ECG915 is a high speed, high gain, monolithic operational amplifier constructed on a single silicon chip. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The ECG915 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The ECG915 is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analog gates, precision comparators, sample and holds, and general feedback applications requiring DC wide bandwidth operation.

Absolute Maximum Ratings

Supply Voltage ..................... ±18 V
Internal Power Dissipation (Note 1) ..................... 500 mW

Differential Input Voltage ..................... ±15 V
Input Voltage (Note 2) ..................... ±15 V
Storage Temperature Range ..................... -65°C to +150°C
Operating Temperature Range ..................... 0°C to 70°C
Lead Temperature (Solder, 60 Seconds) ..................... 300°C

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15$ V, $T_A = 25^\circ$C unless otherwise specified)

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<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
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<td>7.5</td>
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<td>1.0</td>
<td></td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>$R_i \leq 10$ kΩ</td>
<td>±10</td>
<td>±12</td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td>Supply Voltage Rejection Ratio</td>
<td>$R_i \leq 10$ kΩ</td>
<td>74</td>
<td>92</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>$R_i \geq 2$ kΩ, $V_{in} = \pm 10$ V</td>
<td>45</td>
<td>400</td>
<td></td>
<td>µV/V</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>$R_i \leq 10$ kΩ</td>
<td>75</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Supply Current</td>
<td></td>
<td>5.5</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Power Consumption</td>
<td></td>
<td>168</td>
<td>300</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>Acquisition Time (Unity Gain)</td>
<td>$V_{in} = +5$ V</td>
<td>800</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Settling Time (Unity Gain)</td>
<td></td>
<td>300</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Transient Response (Unity Gain)</td>
<td>$V_{in} = 400$ mV</td>
<td>30</td>
<td>75</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>slew rate</td>
<td></td>
<td>25</td>
<td>50</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Overshoot</td>
<td></td>
<td>10</td>
<td>18</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>slew rate (non-inverting)</td>
<td></td>
<td>100</td>
<td></td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>slew rate (inverting)</td>
<td></td>
<td></td>
<td></td>
<td>V/µs</td>
<td></td>
</tr>
</tbody>
</table>

The following apply for $0^\circ$C $\leq T_A \leq +70^\circ$C:

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>$R_i \leq 10$ kΩ</td>
<td>10</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$T_A = +70^\circ$C</td>
<td>750</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$T_A = 0^\circ$C</td>
<td>1.5</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>$R_i \geq 2$ kΩ, $V_{in} = \pm 10$ V</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$R_i \geq 2$ kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
(1) Rating applies for ambient temperatures as $+70^\circ$C.
(2) For supply voltages less than $\pm 15$ V, the absolute maximum input voltage is equal to the supply voltage.

**FREQUENCY COMPENSATION CIRCUIT**

**COMPENSATION COMPONENTS VALUES**

<table>
<thead>
<tr>
<th>CLOSED LOOP GAIN</th>
<th>$C_1$</th>
<th>$C_2$</th>
<th>$C_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>10</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>100</td>
<td>50</td>
<td>250</td>
<td>—</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
<td>500</td>
<td>1000</td>
</tr>
<tr>
<td>1</td>
<td>500</td>
<td>2000</td>
<td>1000</td>
</tr>
</tbody>
</table>

*For Gain $10^\circ$: Compensation may be improved by replacing $C_2$, $C_3$ and adding a 200 pf capacitor ($C_4$) between Pins 7 and 10.

**SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP GAIN**

**LARGE SIGNAL PULSE RESPONSE**

**HIGH SLEW RATE CIRCUIT**

**SMALL SIGNAL PULSE RESPONSE**

**INVERTING UNITY GAIN**

**INVERTING UNITY GAIN**
TYPICAL PERFORMANCE CURVES

VOLTAGE FOLLOWER

VOLTAGE FOLLOWER
TRANSIENT RESPONSE

COMMON MODE REJECTION RATIO
AS A FUNCTION OF FREQUENCY

SUPPLY VOLTAGE REJECTION RATIO
AS A FUNCTION OF FREQUENCY

SUPPLY VOLTAGE REJECTION RATIO
AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE REJECTION RATIO
AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL APPLICATIONS
HIGH SPEED SAMPLE AND HOLD
**TYPICAL APPLICATIONS**

**WIDE BAND VIDEO AMPLIFIER WITH 75Ω COAX CABLE DRIVE CAPABILITY**

![Amplifier Diagram]

**HIGH SPEED 10 BIT DIGITAL TO ANALOG CONVERTER**

**ANALOG OUTPUT 0 TO ±5.0 V**

![Converter Diagram]

**VOLTAGE OFFSET NULL CIRCUIT**

![Offset Null Circuit Diagram]

**HIGH SPEED INTEGRATOR**

![Integrator Diagram]

**DEFINITION OF TERMS**

**INPUT OFFSET VOLTAGE** — The voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

**INPUT OFFSET CURRENT** — The difference in the currents into the two input terminals with the output at zero volts.

**INPUT RESISTANCE** — The resistance looking into either input terminal with the other grounded.

**INPUT BIAS CURRENT** — The average of the two input currents.

ECG915
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to function improperly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

ACQUISITION TIME — The time from change of input until last time output exceeds specified percent of final value.

SLEW RATE — The maximum rate of change of output under large signal conditions.

SETTLING TIME — The time from output first reaching final value until last time output remains specified percent of final value.

HELPFUL HINTS

LAYOUT — The layout should be such that stray capacitance is minimized.

SUPPLIES — The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RMSING — Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by adding the capacitive load with a resistance of 1000Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 Ohms for unity gain configuration and around 3.0 Ohms for gain 10 should be adequate.

LATCH UP — This may occur when the amplifier is used as a voltage integrator. The inclusion of a divider between pin 6 and 2 with the capacitance towards pin 2 is the recommended precaution.

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CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:
- CMOS low power with speed
- Parallel conversion technique
- 15-MHz sampling rate (66-nS conversion time)
- 6-bit latched 3-state output with overflow bit
- ±1/2 LSB accuracy
- Single supply voltage (3 to 10 V)
- 2 units in series allow 7-bit output
- 2 units in parallel allow 30-MHz sampling rate
- Internal \text{V}_{\text{REF}}\text{ with ext \text{V}_{\text{REF}}\text{ option}}

Applications
- The CA3300 is especially suited for high-speed conversion applications where low power is also important
- TV video digitizing (industrial/security)
- High-speed A/D conversion
- Ultrasound signature analysis
- Transient signal analysis
- High-energy physics research
- High-speed oscilloscope storage/display
- General-purpose hybrid A/D converters
- Optical character recognition
- Radar pulse analysis
- Motion signature analysis

The RCA CA3300 is a CMOS 50-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3300 operates over a wide dynamic input-voltage range of 2.5 volts up to the dc supply voltage with maximum power consumptions as low as 50 to 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 11 MHz, the power consumption of the CA3300 is less than 50 mW. When operated from an 8-volt supply at a frequency of 15 MHz, the power consumption is less than 150 mW.

The intrinsic high conversion rate makes the CA3300 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3300s in series to increase the resolution of the conversion system. A series connection of two CA3300s may be used to produce a 7-bit high-speed converter. Operation of two CA3300s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3300s in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed A/D converter.

Sixty-four parallelised auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3300. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3300 type is available in an 18-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).
<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td></td>
<td>MIN.</td>
<td>TYP.</td>
</tr>
<tr>
<td>Linearity Error</td>
<td>VDD=8 V, VREF=7.58 V, CLK=15 MHz, gain adjusted</td>
<td>-</td>
<td>±0.5</td>
</tr>
<tr>
<td>Differential Linearity Error</td>
<td>VDD=8 V, VREF=7.58 V, CLK=15 MHz</td>
<td>-</td>
<td>±0.5</td>
</tr>
<tr>
<td>Quantizing Error</td>
<td></td>
<td>-1/2</td>
<td>-</td>
</tr>
<tr>
<td>Analog Input:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full Scale Range</td>
<td>VDD=8 V, CLK=15 MHz</td>
<td>2.4</td>
<td>-</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td></td>
<td>-</td>
<td>50</td>
</tr>
<tr>
<td>Input Current</td>
<td></td>
<td>-</td>
<td>500</td>
</tr>
<tr>
<td>Gain Temperature Coefficient</td>
<td>VDD=8 V, CLK=15 MHz</td>
<td>-</td>
<td>0.016</td>
</tr>
<tr>
<td>Maximum Conversion Speed</td>
<td>VDD=8 V</td>
<td>-</td>
<td>12M</td>
</tr>
<tr>
<td>VDD=5 V</td>
<td></td>
<td>15M</td>
<td>19M</td>
</tr>
<tr>
<td>Device Current:</td>
<td></td>
<td>-</td>
<td>7</td>
</tr>
<tr>
<td>(Excludes IREF, IZ)</td>
<td>VDD=8 V, CLK=15 MHz</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td>VDD=5 V (Auto Balance State)</td>
<td></td>
<td>-</td>
<td>6.4</td>
</tr>
<tr>
<td>VDD=8 V (Auto Balance State)</td>
<td></td>
<td>-</td>
<td>24</td>
</tr>
<tr>
<td>Ladder Impedance</td>
<td></td>
<td>1000</td>
<td>1400</td>
</tr>
<tr>
<td>Digital Inputs:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Voltage</td>
<td>VDD=5 V</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>VDD=8 V</td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>High Voltage</td>
<td>VDD=5 V</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>VDD=6 V</td>
<td></td>
<td>5.5</td>
<td>-</td>
</tr>
<tr>
<td>Input Current</td>
<td>VDD=8 V</td>
<td>-</td>
<td>±1</td>
</tr>
<tr>
<td>Digital Outputs:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low</td>
<td>VDD=5 V, VO=0.4 V</td>
<td>1.8</td>
<td>10</td>
</tr>
<tr>
<td>(Sink) Current</td>
<td>VDD=8 V, VREF=0.5</td>
<td>3.2</td>
<td>15</td>
</tr>
<tr>
<td>Output High</td>
<td>VDD=5 V, VO=4.6 V</td>
<td>-0.8</td>
<td>6</td>
</tr>
<tr>
<td>(Source) Current</td>
<td>VDD=8 V, VREF=7.5 V</td>
<td>-1.8</td>
<td>9</td>
</tr>
<tr>
<td>Zener Voltage</td>
<td>IZ=10 mA</td>
<td>5.8</td>
<td>6.4</td>
</tr>
<tr>
<td>Zener Dynamic Impedance</td>
<td>IZ=10 mA</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Zener Temperature Coefficient</td>
<td></td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Digital Output Delay, tD</td>
<td>VDD=8 V</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Aperture Time</td>
<td>VDD=8 V</td>
<td>-</td>
<td>25</td>
</tr>
</tbody>
</table>
MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY VOLTAGE RANGE (VDD) .......................... -0.5 to 10 V
(VOLTAGE REFERENCED TO VSS TERMINAL)

INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) .......................... -0.5 to VDD +0.5 V

DC INPUT CURRENT
CLK, PH, CE1, CE2, VIN .......................... ±10 mA

POWER DISSIPATION PER PACKAGE (PD)
FOR TA = -40 to 55°C ........................................... 315 mW
FOR TA = 55°C to 85°C ........................................... Derate linearly at 3.3 mW/°C

TEMPERATURE RANGE
OPERATING ........................................... -40 to +85°C
STORAGE ........................................... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX ........................................... +265°C

Fig. 1 - Block diagram for the CA330D.
Fig. 2 - Timing diagram for the CA3300D.

Fig. 3 - Typical current drain versus sampling rate as a function of supply voltage.

Fig. 4 - Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

Fig. 5 - Typical maximum sample rate versus supply voltage.

Fig. 6 - Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)
During the "Auto Balance" phase, a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. These tap voltages will be as follows:

\[
V_{tap}(n) = \frac{V_{REF}/64 \times N - [V_{REF}/(2 \times 64)]}{V_{REF}[2N - 1]/128}
\]

Where: 
- \(V_{tap}(n)\) = reference ladder tap voltage at point \(n\).
- \(V_{REF}\) = voltage across \(R^+ \) to \(R^-\)
- \(N\) = tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately \((V_{DD} - V_{SS})/2\). The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Single Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and \(V_{IN}\) is switch to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than \(V_{IN}\) will drive the comparator outputs to a "low" state, all comparators with tap voltage lower than \(V_{IN}\) will drive the comparator outputs to a "high" state.
The status of all these comparator amplifiers are stored at the end of this phase (92), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators are encoded by a 64 to 7 bit decode array and the results are locked into a storage register at the rising edge of the next 2.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. CE1 will independently disable 81 through 82 when it is in a high state. CE2 will independently disable 81 through 86 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it inter the chip. Also, an onboard zener is provided for use as a reference voltage.

Continuous Clock Operation

The complete conversion cycle can be traced through the CA3300 via the following steps. (Refer to timing diagram No. 1.) With the phase control in a 'High' state, the rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 64 comparators will accept the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock output the output of the latches propagates through the decode array and a 7-bit code appears at the 0 inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with no delay by as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, whereby repeating the conversion process for the next state.

Idle Mode Operation

For sampling high-speed non-recurrent or transient data, the converter may be operated in a pulse mode in one of two ways. The fastest method is to keep the converter in the analogue Unknown phase, 82, during the standby state. The device can now be pulsed through the Auto Balance phase as little as 33 ns. The analog value is captured on the leading edge of 82 and is transferred into the output registers on the trailing edge of 82. We are now back in the standby state, 82, and another conversion can be started 33 ns, but not later than 10 µs due to the eventual flop of the commutating capacitors. Another advantage this method is that it has the potential of having the lowest power drain. The larger the time ratio between 82 and 81, the lower the power consumption. (See timing diagram No. 3.)

The second method uses the Auto Balance phase, 81, as the standby state. In this state the converter can remain indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two 82 pulses. The first pulse starts a Sample Unknown phase and stores the analog value in the comparator latches on the leading edge. A second 82 pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place 37 ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of 82 to 81. (See timing diagram No. 3.)

Preserved Accuracy

In most cases the accuracy of the CA3300 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V\text{IN} or by the offset trim of the op-amp. When this is not possible the R\text{+} (pin 10) input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is 4 LSB. The equation is as follows:

\[ V\text{IN} \text{ (0 to 1 transition) = } \frac{1}{2} \text{ LSB = } \frac{1}{2}(V\text{REF}/64) = V\text{REF}/128 \]

If V\text{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between R\text{+} and ground will accomplish the adjustment. Set V\text{IN} to 1/2 LSB and trim the pot until the 0 to 1 transition occurs.

If V\text{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between R\text{+} and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op-amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V\text{IN} should be set to the 63 to overflow transition. That voltage is 4 LSB less than V\text{REF} and is calculated as follows:

\[ V\text{IN} \text{ (63 to 64 transition) = V\text{REF} - V\text{REF}/128 = V\text{REF} (127/128) } \]

To perform the gain trim, first do the offset trim and then apply the required V\text{IN} for the 63 to overflow transition. Now adjust V\text{REF} until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC), pin 16, is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 32\% LSB's. That voltage is as follows:

\[ V\text{IN} \text{ (32 to 33 transition) = } 32.5 \text{ (VREF/64) } \]

An adjustable voltage follower can be connected to the RC pin or a 2K pot can be connected between R\text{+} and R\text{+} with the wiper connected to RC. Set V\text{IN} to the 32 to 33 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create some unique transfer functions. For example, if R\text{+} is grounded, RC is connected to 3.25 volts, and R\text{+} is connected to 4.8 volts then the lower order counts, 1 through 32, will have an LSB value of 100 mV while the upper order counts. 34 through Overflow, will have an LSB value of 50 mV. This effectively doubles the sensitivity in the upper counts as compared to the lower counts.
7-Bit Resolution
To obtain 7-bit resolution, two CA3300s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls—all of which are available on the CA3300.

The first step for connecting a 7-bit circuit is to take the ladder networks, as illustrated in Fig. 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the CE1 control of the lower a-d converter and the CE2 control of the upper a-d converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit a-d converter is shown in Fig. 14.

![Fig. 12 - Typical CA3300 8-bit configuration 15-MHz sampling rate.](image)

![Fig. 13 - Typical CA3300 7-bit resolution configuration 15-MHz sampling rate.](image)
6-bit to 12-Bit Conversion Techniques

obtain 6 to 12-bit resolution and accuracy, use a feed-
ward conversion technique. Two a-d converters will be
added to convert up to 11 bits; three a-d converters to
vert 12 bits. The high speed of the CA3300 allows 12-bit
versions in the 500 to 900-ns range.

A circuit diagram of a high-speed 12-bit a-d converter is
own in Fig. 15. In the feed-forward conversion method
sequential conversions are made. Converter A first
is a coarse conversion to 6 bits. The output is applied to a
bit d-a converter whose accuracy level is good to 12 bits.
A d-a converter output is then subtracted from the input
age, multiplied by 32, and then converted by a second
A-d-a converter, which is connected in a 7-bit

configuration. The answers from the first and second
conversions are added together with bit 1 of the first
conversion overlapping bit 7 of the second conversion.

When using this method, take care that:
- The linearity of the first converter is better than ¼ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first
  conversion since the second converter is unipolar.
- The d-a converter and its reference are accurate to the
total number of bits desired for the final conversion (the
d-a converter need only be accurate to 6 bits).

The first converter can be offset-biased by adding a
20Ω resistor at the bottom of the ladder and increasing
the reference voltage by 1 LSB. If a 5.40-voltage
reference is used in the system, for example, then the
first CA3300 will require a 6.5-V reference.

Fig. 14 - Typical CA3300 6-bit resolution configuration
30-MHz sampling rate.
Fig. 15 – Typical CA3300 800-nanosecond 12-bit A/D system.

Fig. 16 – TTL interface circuit for VDD > 5.5 volts.
OPERATING AND HANDLING CONSIDERATIONS

Handling
All inputs and outputs of RCA CCS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for CCS/MOS devices are described in ICAN-6525, “Guide to Better Handling and Operation of CMOS Integrated Circuits.”

Input Signals
To prevent damage to the input protection circuit, input signals should never be greater than VDD nor less than VSS. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs
A connection must be provided at every input terminal. All unused input terminals must be connected to either VDD or VSS, whichever is appropriate.

Output Short Circuits
Shorting of outputs to VDD or VSS may damage CCS/MOS devices by exceeding the maximum device dissipation.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

The photographs and dimensions of each CCS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CA3500H.
DAC-08
8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER
UNIVERSAL DIGITAL LOGIC INTERFACE

FEATURES
- Fast Settling Output Current: 55ns
- Full Scale Current Preset Matched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% Maximum Over Temperature Range
- High Output Impedance and Compliance
- Differential Current Outputs
- Wide Range Multiplying Capability: 1MHz Bandwidth
- Low FS Current Drift: ±10ppm/°C
- Wide Power Supply Range: ±4.5V to ±15V
- Low Power Consumption: 33mW @ ±5V
- Low Cost

GENERAL DESCRIPTION
The DAC-08 series of 8-bit monolithic Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 55ns settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within ±1 LSB between references and full scale currents eliminate the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High-voltage compliance dual-complementary current outputs are provided, increasing versatility and enabling different operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ±4.5 to ±15V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1047 A/D converters, servomotor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT

ORDERING INFORMATION & PIN CONNECTION

<table>
<thead>
<tr>
<th>MODEL</th>
<th>TEMP RANGE</th>
<th>NONLINEARITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC-08A</td>
<td>-55°C to 125°C</td>
<td>±0.1%</td>
</tr>
<tr>
<td>DAC-08B</td>
<td>-55°C to 125°C</td>
<td>±0.15%</td>
</tr>
<tr>
<td>DAC-08C</td>
<td>±0°C to ±70°C</td>
<td>±0.15%</td>
</tr>
<tr>
<td>DAC-08D</td>
<td>±0°C to ±70°C</td>
<td>±0.3%</td>
</tr>
<tr>
<td>DAC-08E</td>
<td>±0°C to ±70°C</td>
<td>±0.10%</td>
</tr>
<tr>
<td>DAC-08F</td>
<td>±0°C to ±70°C</td>
<td>±0.25%</td>
</tr>
<tr>
<td>DAC-08G</td>
<td>±0°C to ±70°C</td>
<td>±0.3%</td>
</tr>
</tbody>
</table>

For MIL-STD-883 Class B Processors: DAC-08A/B/C
For MIL-STD-883 Class B Processors: DAC-08D/E/F

Military Temperature Range Devices: DAC-08A/B/C/D/E/F/G

PAGE 11-35
**DAC-08 8-BIT HIGH-SPEED MULTIPLYING DAC CONVERTER**

### ABSOLUTE MAXIMUM RATINGS

- **Operating Temperature**: DAC-08AQ, Q: -55°C to +125°C, DAC-08HQ, EQ, CQ: 0°C to +70°C
- **Storage Temperature**: -45°C to 150°C
- **Power Dissipation**: 500mW
- **Derate above 100°C**: 10mW/°C
- **Lead Soldering Temperature (60 sec.)**: 300°C

*Over load operating range*

- **V+ Supply to V- Supply**: 36V
- **Logic inputs**: V+ to V- plus 36V
- **V+ to V-**: 36V
- **Analog Current Outputs**: See Figure 12
- **Reference Inputs (V1h to V1l)**: V+ to V- 18V
- **Reference Input Differential Voltage**: (V1h to V1l) ±18V
- **Reference Input Current (I1k)**: ±2.5mA

### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>DAC-08AQ</th>
<th>DAC-08HQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance</td>
<td>Rth</td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Capacitance</td>
<td>Cth</td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Temperature</td>
<td>Top</td>
<td>±5°C to +125°C</td>
<td>±0.1</td>
<td>±0.15</td>
</tr>
<tr>
<td>Sensitivity Time</td>
<td>t0</td>
<td>0 or 0.05 (T0 = 25°C)</td>
<td>85</td>
<td>150</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>Each bit</td>
<td>1.5ns</td>
<td>±50</td>
<td>±50</td>
</tr>
<tr>
<td>All bits simultaneous</td>
<td>1.5ns</td>
<td>±50</td>
<td>±50</td>
<td></td>
</tr>
<tr>
<td>Full Scale Temperature</td>
<td>TFS</td>
<td></td>
<td>±10</td>
<td>±50</td>
</tr>
<tr>
<td>Output Voltage Range (Linear Components)</td>
<td></td>
<td>10%</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>Full Scale Current</td>
<td>10%</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Full Range Current</td>
<td>10%</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Full Range Symmetry</td>
<td>10%</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Zero Scale Current</td>
<td>10%</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Output Current Range</td>
<td>5%</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Logic Input Levels</td>
<td>Vih</td>
<td>±15V, Vio = 0V</td>
<td>±0.5</td>
<td>±0.5</td>
</tr>
<tr>
<td>Logic Input VIH</td>
<td>Iih</td>
<td>±15mA</td>
<td>±15mA</td>
<td></td>
</tr>
<tr>
<td>Logic Input VOH</td>
<td></td>
<td>±15mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Input IOL</td>
<td></td>
<td>±15mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Input ISH</td>
<td></td>
<td>±15mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Input ISL</td>
<td></td>
<td>±15mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Input VIL</td>
<td></td>
<td>±15mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Threshold Range</td>
<td>Vih</td>
<td>±15V, Vio = 0V</td>
<td>±15V, Vio = 0V</td>
<td></td>
</tr>
<tr>
<td>Reference Input Range</td>
<td>Vih</td>
<td>±15V, Vio = 0V</td>
<td>±15V, Vio = 0V</td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td></td>
<td>±15V, Vio = 0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Input Noise</td>
<td>0.6mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Input Bandwidth</td>
<td>5kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>PSS</td>
<td>±0.00025</td>
<td>±0.00025</td>
<td></td>
</tr>
<tr>
<td>Power Supply Current</td>
<td></td>
<td>±0.00025</td>
<td>±0.00025</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td></td>
<td>±0.1W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE**: Parameter met 100% without any voltage 100% guaranteed by design.
**ELECTRICAL CHARACTERISTICS** at $V_{cc} = \pm 15V$, $I_{PP} = 2.0mA$, $T_{a} = 0^\circ C$ to $+70^\circ C$ unless otherwise noted. Output characteristics are to both Low and High.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>DAC-08H</th>
<th>DAC-08E</th>
<th>DAC-08C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>$R$</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$ohm$</td>
</tr>
<tr>
<td>Temperature</td>
<td>$T_{a}$</td>
<td>$0^\circ C$ to $+70^\circ C$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$oC$</td>
</tr>
<tr>
<td>Water vapor</td>
<td>$W_{v}$</td>
<td></td>
<td>$-26.0$</td>
<td>$-20.0$</td>
<td>$-15.0$</td>
<td>$%$</td>
</tr>
<tr>
<td>Sinking Time</td>
<td>$t_{s}$</td>
<td>$t_{s} = 0$ to $2000$ must be met</td>
<td>55</td>
<td>100</td>
<td>55</td>
<td>$us$</td>
</tr>
<tr>
<td>Power Supply Range</td>
<td>$V_{cc}$</td>
<td>$+5V$ to $+15V$, $V_{pp} = 0$</td>
<td>$1.15$</td>
<td>$1.55$</td>
<td>$1.15$</td>
<td>$V$</td>
</tr>
<tr>
<td>Output Reference</td>
<td>$V_{OR}$</td>
<td>$V_{OR} = +0.5V$</td>
<td>$0.25$</td>
<td>$0.25$</td>
<td>$0.25$</td>
<td>$V$</td>
</tr>
<tr>
<td>Power Supply Current</td>
<td>$I_{cc}$</td>
<td>$I_{cc} = 0$ to $2.0mA$</td>
<td>$-0.00$</td>
<td>$0.00$</td>
<td>$-0.00$</td>
<td>$mA$</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>$V_{cc}$</td>
<td>$V_{cc} = 5V$</td>
<td>$0.0005$</td>
<td>$0.0005$</td>
<td>$0.0005$</td>
<td>$V$</td>
</tr>
</tbody>
</table>

**PULSED REFERENCE OPERATION**

**FAST PULSED REFERENCE OPERATION**

---

PAGE 11-25
TYPICAL PERFORMANCE CURVES

OUTPUT CURRENT vs OUTPUT VOLTAGE
(OUTPUT VOLTAGE COMPLIANCE)

OUTPUT VOLTAGE
COMPLIANCE vs TEMPERATURE

BIT TRANSFER
CHARACTERISTICS

POWER SUPPLY CURRENT vs V+

POWER SUPPLY CURRENT vs V−

POWER SUPPLY CURRENT vs TEMPERATURE

BASIC CONNECTIONS

BASIC POSITIVE REFERENCE OPERATION

ACCOMODATING BIPOLAR REFERENCES
OFFSET BINARY OPERATION

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

INTERFACING WITH VARIOUS LOGIC FAMILIES
APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to ±4.0mA. The full scale output current is a linear function of the reference current and is given by:

\[ I_{OL} = \frac{1}{256} \times I_{REF} \quad \text{where} \quad I_{REF} = I_{IN} \]

In positive reference applications, an external positive reference voltage forces current through \( R_{12} \) into the \( V_{REF(+)\ldots} \) terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to \( V_{REF(-\ldots)} \) at pin 15; reference current flows from ground through \( R_{14} \) into \( V_{REF(-\ldots)} \) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. \( R_{13} \) (nominally equal to \( R_{14} \)) is used to cancel bias current errors; \( R_{13} \) may be eliminated with only a minor increase in error.

Stabilized references may be accommodated by offsetting \( V_{REF} \) or pin 15. The negative common mode range of the reference amplifier is given by: \( V_{CM(-)} = V_{+} - \frac{1}{128} \times I_{REF} \times 1\,\text{k} \Omega \) plus 2.5V. The positive common mode range is \( V_{+} \) less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, \( R_{14} \) should be split into two resistors with the junction bypassed to ground with a 0.1\,\mu F capacitor.

For most applications, the tight relationship between \( I_{REF} \) and \( I_{OL} \) will eliminate the need for trimming \( I_{REF} \). If required, full scale trimming may be accomplished by adjusting the value of \( R_{14} \) or by using a potentiometer for \( R_{14} \). An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier - negative common mode range. The recommended range for operation with a DC reference current is ±0.2mA to ±4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 15 to \( V_{+} \). For fixed reference operation, a 0.01\,\mu F capacitor is recommended. For variable reference applications, see section entitled “Reference Amplifier Compensation for Multiplying Applications”.

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between \( I_{OL} \) and \( I_{IN} \) over a range of 4mA to 4.0A. Monotonic operation is maintained over a typical range of \( I_{OL} \) from 100\,\mu A to 4.0mA.
REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to Y- . The value of this capacitor depends on the the impedance presented at pin 14: for RS values of 1.0, 2.5 and 10k, minimum values of C2 are 15, 37, and 75pF. Larger values of R14 require proportionately increased values of C2 for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C2 values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C2 = 150pF, the reference amplifier slew rate at 4mA/µs enabling a transition from I低 = 0 to I高 = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accomplished by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff flag flag = 0 condition. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 2000Ω and C2 = 0. This yields a reference slew rate of 16mA/µs which is relatively independent of R14 and C2 values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2mA logic input current and completely adjustable logic threshold voltage. For V- = -15V, the logic inputs may swing between +10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given as +10V and +15V, respectively. Logic threshold voltage of 2.5V logic level, may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V1C). The appropriate graph shows the relationship between V1C and VTH over the temperature range, 40°C to 85°C. For TTL and OTL interfaces, simply ground pin 1. When interconnecting ECL, an I低 = 1mA is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will source 2mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01µF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are powered where I低 + I高 = I低. Current appears at the "true" output when a "1" is applied to that logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases I低 as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously, if one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I低; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage sources. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by V+ plus (I低 x 1kΩ) plus 2.5V. The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 5V to 25V. When operating at supplies of ±5V or less, I低=1mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, logic negative input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at ±4.5V with I低=2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required, however, an artificial ground may be used to ensure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

P电源 = (±V + ±1) (V + ±1) (V + ±2 I低 (±V) . A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptologic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to ±1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at -35°C; at -125°C an increase of about 15% is typical.
SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85ns at I\textsubscript{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70ns. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if R\textsubscript{L} > 5000.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I\textsubscript{REF} values down to 1.0mA, with gradual increases for lower I\textsubscript{REF} values. The principal advantage of higher I\textsubscript{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4µA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 29 uses a cascode design to permit driving a 1kΩ load with less than 50pF of parasitic capacitance at the measurement node. At higher values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of \textit{I}_{\text{REF}}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and \textit{V}_{\text{out}} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1µF capacitors at the supply pins provide full transient protection.
except for the cycle times and the access times.

**HYB 4164-2, HYB 4164-3**

**65,536-Bit Dynamic Random-Access Memory (RAM)**

- 65,536 x 1 organization
- Industry standard 16-pin JEDEC configuration
- Single ±5 V ± 10% power supply
- Low power dissipation
  - 150 mW active (max.)
  - 20 mW standby (max.)
- 150 ns access time,
  - 280 ns cycle (HYB 4164-2)
  - 280 ns cycle (HYB 4164-3)
- All inputs and outputs compatible
- Page Mode Read and Write
- 256 refresh cycles with 6 ms long refresh period
- High over- and undershooting capability on all inputs
- Low supply current transients
- CAS controlled output providing latched or unlatched data
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, hidden refresh

### Pin Configuration

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>A1-4</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>DI</td>
<td>A5-12</td>
<td>CAS Column Address Strobe</td>
</tr>
<tr>
<td>WE</td>
<td>A13</td>
<td>Data In</td>
</tr>
<tr>
<td>RAS</td>
<td>A14</td>
<td>No Connection</td>
</tr>
<tr>
<td>A2</td>
<td>A15</td>
<td>Data Out</td>
</tr>
<tr>
<td>A3</td>
<td>A16</td>
<td>RAS Row Address Strobe</td>
</tr>
<tr>
<td>A4</td>
<td>A17</td>
<td>WE Write Enable</td>
</tr>
<tr>
<td>VCC</td>
<td>GND</td>
<td>Power Supply (±5V)</td>
</tr>
</tbody>
</table>

### Pin Names

- A1-4: Address Inputs
- CAS: Column Address Strobe
- DI: Data In
- NC: No Connection
- A15: Data Out
- RAS: Row Address Strobe
- WE: Write Enable
- VCC: Power Supply (±5V)
- GND: Ground (0V)

### Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limit Value</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vih</td>
<td>High level input voltage (all inputs)</td>
<td>2.4</td>
<td>V</td>
<td>0.8</td>
</tr>
<tr>
<td>Vil</td>
<td>Low level input voltage</td>
<td>-1.0</td>
<td>V</td>
<td>0.8</td>
</tr>
<tr>
<td>V0H</td>
<td>Output high voltage</td>
<td>2.4</td>
<td>V</td>
<td>VCC</td>
</tr>
<tr>
<td>V0L</td>
<td>Output low voltage</td>
<td>-0.4</td>
<td>V</td>
<td>0.8</td>
</tr>
<tr>
<td>ICC</td>
<td>Average VCC power supply current</td>
<td>3.6</td>
<td>mA</td>
<td>RAS at VCC</td>
</tr>
<tr>
<td>ICC</td>
<td>Standby VCC power supply current</td>
<td>24</td>
<td>mA</td>
<td>RAS at VCC</td>
</tr>
<tr>
<td>ICS</td>
<td>Average VCC current during refresh</td>
<td>20</td>
<td>mA</td>
<td>RAS at VCC</td>
</tr>
<tr>
<td>IS</td>
<td>Input leakage current (any input)</td>
<td>10</td>
<td>pA</td>
<td>-</td>
</tr>
<tr>
<td>IOH</td>
<td>Output leakage current</td>
<td>10</td>
<td>pA</td>
<td>-</td>
</tr>
</tbody>
</table>

### Capacitances

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limit Value</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cm</td>
<td>Input capacitance (A1-A4, DI)</td>
<td>6</td>
<td>pF</td>
<td>-</td>
</tr>
<tr>
<td>Cg</td>
<td>Input capacitance (VCC, CAS, WE)</td>
<td>10</td>
<td>pF</td>
<td>-</td>
</tr>
<tr>
<td>CO</td>
<td>Output capacitance</td>
<td>7</td>
<td>pF</td>
<td>DO disabled</td>
</tr>
</tbody>
</table>

### Notes

1. Internal power dissipation is 200 µW at a maximum of eight initialization cycles prior to normal operation.
2. Capacitances measured with a Function Meter 7250 AD or effective capacitance calculated from the equation $C = \frac{1}{2\pi f} - \frac{1}{2\pi f} V = 3 V$.
3. Output leakage current is measured at the fastest cycle rate.
4. All leakage pins of 0 V and pin under test at ± 5 V.

March 1982
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>HYB 4164-1</th>
<th>HYB 4164-2</th>
<th>HYB 4164-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>l_t</td>
<td>Data in set-up time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_p</td>
<td>Data in hold time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_c</td>
<td>Write command hold time referenced to RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_r</td>
<td>Write command set-up time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_w</td>
<td>Write command pulse width</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_cw</td>
<td>Write command to CAS lead time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_m</td>
<td>Write command to CAS lead time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_s</td>
<td>Data in hold time referenced to RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_u</td>
<td>CAS to WE delay</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uo</td>
<td>CAS to WE delay referenced to RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_tw</td>
<td>CAS precharge time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_tw0</td>
<td>Refresh period</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_wi</td>
<td>Access time from RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_cwi</td>
<td>Access time from CAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_gf</td>
<td>RAS hold time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_cwi</td>
<td>CAS hold time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>CAS pulse width</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_cwi</td>
<td>RAS precharge time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>RAS pulse width</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>RAS to CAS delay time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>RAS to CAS delay time referenced to RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uw0</td>
<td>CAS to WE delay referenced to RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>Column address set-up time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>Column address hold time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uw0</td>
<td>Column address hold time referenced to RAS</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>Head command set-up time (RAM)</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>Head command hold time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>l_uwi</td>
<td>Write command hold time</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
</tbody>
</table>

Notes:

1. V_i and V_c are reference levels for measuring timing of input signals. All transition times are measured between V_i and V_c.
2. The specifications for l_u and l_u0 are not used in actual circuitry. They are included in the data sheet as electric characteristics only. If l_u < l_u0, the cycle is an early write cycle and the data buffer remains open circuit (high impedance) throughout the cycle. If l_u = l_u0, the cycle is a normal cycle and the data buffer will remain open circuit (high impedance) throughout the cycle.
3. The specifications for l_u and l_u0 are not used in actual circuitry. They are included in the data sheet as electric characteristics only. If l_u < l_u0, the cycle is an early write cycle and the data buffer remains open circuit (high impedance) throughout the cycle. If l_u = l_u0, the cycle is a normal cycle and the data buffer will remain open circuit (high impedance) throughout the cycle.
4. Operation within the l_u limit ensures that l_u < l_u0 and l_u < l_u0, the cycle is an early write cycle and the data buffer will remain open circuit (high impedance) throughout the cycle.
5. l_u and l_u0 are not used in actual circuitry. They are included in the data sheet as electric characteristics only. If l_u < l_u0, the cycle is an early write cycle and the data buffer remains open circuit (high impedance) throughout the cycle. If l_u = l_u0, the cycle is a normal cycle and the data buffer will remain open circuit (high impedance) throughout the cycle.
The Read and Write cycle timing diagrams for the HYB 4164-1 were not available. However, these timing diagrams are similar to those of the Motorola MCM 6665. Hence, the READ and WRITE cycle timings of the MCM 6665 are presented here.
II. APPENDIX 2
1.1 Circuit Schematic of the Video Codec
II.2 Circuit Schematic of the Logic Controller
II.3 Photograph of the Circuit Built
III. APPENDIX 3
III.1 Timing Diagram for the Digital Field Memory