PHASE-LOCKED LOOP CLOCK EXTRACTION FOR FDDI SYSTEMS

A Thesis

Submitted to the Faculty of Graduate Studies and Research
in Partial Fulfilment of the Requirements
for the Degree of

Master of Science

by

G. Kate Harris
Saskatoon, Saskatchewan
May 1988

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UNIVERSITY OF SASKATCHEWAN

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PHASE-LOCKED LOOP CLOCK EXTRACTION FOR FDDI SYSTEMS

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ABSTRACT

The American National Standards Institute (ANSI) is in the process of standardizing a Fiber Distributed Data Interface (FDDI). This local area network optically transmits data at 125 Mb/s using a point to point clocking scheme. Data is transmitted at each station using the station clock and recovered at the next station by a clock extracted from the data. Clock recovery in the existing FDDI framework is investigated in this paper.

The conditions necessary for clock recovery are reviewed, and the FDDI code analyzed for transmission and clock recovery qualities. The remainder of the thesis is devoted to the design and performance testing of a phase-locked loop clock extraction circuit. The design meets the performance criteria specified in the current FDDI draft standard.
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RB  Run bound  (bits)
RDS  Running digital sum  (bits)
\( R_{\text{tol}} \)  Tolerance of VCO center frequency  (ppm)
\( R_L \)  Lock-in range of PLL  (rad/s)
\( R_H \)  Hold-in range of PLL  (rad/s)
\( R_f \)  Frequency range of incoming signal  (ppm)
\( R_p \)  Pull-in range of PLL  (rad/s)
\( R_{\text{VCO}} \)  Frequency range of VCO  (rad/s)
\( RZ \)  Return to zero
\\( s = \sigma + j \omega \)  Laplace transform complex variable
\( S(\omega) \)  Power Spectral Density  (\( \text{V}^2/\text{Hz} \))
SNR  Signal to Noise ratio
\( S_n(\omega) \)  Power Spectral Density of \( x(t) \)  (\( \text{V}^2/\text{Hz} \))
t  Time  (s)
\( t_{\text{sec}} \)  Negative zero crossing time  (s)
\( T \)  Bit period  (s)
\( T_p \)  Pulse width  (s)
\( T(s) \)  Closed loop transfer function of PLL
\( t_{\text{acq}} \)  Time needed to acquire lock  (s)
\( t_{\text{p}} \)  Pull-in time  (s)
\( t_{\phi} \)  Phase slip time  (s)
\( t_{\phi} \)  Phase acquisition time  (s)
\( v_c, v_o \)  Control voltage  (V)
\( v_d, v_o \)  Phase detector output voltage  (V)
VCO  Voltage control oscillator
\( v_x \)  Velocity of propagation  (m/ns)

XOR  Exclusive OR
\( x(t) \)  Data waveform
\( \delta(t) \)  Dirac delta function
\( \epsilon_\phi \)  Mistuning phase angle  (rad)
\( \epsilon_\phi \)  Offset phase error angle  (rad)
\( \epsilon_\phi \)  Relative tuning angle  (rad)
\( \epsilon_{\text{rms}} \)  RMS jitter  (rms rad)
\( \theta \)  Phase angle  (rad)
\( \theta_0 \)  Phase offset (phase difference when \( f_s = f_0 \))  (rad)
\( \theta_\phi = \Theta_\phi - \theta_0 \)  Phase difference between input and VCO  (rad)
\( \theta_\phi = \Theta_\phi - \theta_0 \)  Phase error between input and VCO  (rad)
\( \Theta_\phi \)  Phase angle of input  (rad)
\( \Theta_\phi \)  VCO phase angle  (rad)
\( \tau_{\text{sec}} \)  Shift in zero crossing time  (sec)
\( \omega_0 \)  VCO center frequency or self resonant frequency of tuned circuit  (rad/s)
\( \omega_s \)  Input signal frequency  (rad/s)
\( \omega_c \)  VCO frequency  (rad/s)
\( \omega_n \)  Natural frequency of second order system  (rad/s)
\( \zeta \)  Damping factor of second order system
\( \delta \)  Amplitude difference
Operations

exp(x) \quad e^x
E\{\}\quad \text{Expectation operation}
R(\quad \text{Autocorrelation function}
* \quad \text{Convolution}
< > \quad \text{Time average}
sinc(x) \quad \frac{\sin(\pi x)}{\pi x}
X^* \quad \text{Complex conjugate of } X
1. INTRODUCTION

The recent surge in the use of multiple processors, graphic workstations and fast storage devices has created a demand for higher speed communication. To address this need, the American National Standards Institute (ANSI) began developing a new set of standards for a Fiber Distributed Data Interface (FDDI). This 100 Mb/s optical communications network uses a packet switching mode of operation with a token protocol. Work on FDDI started in 1982 and is nearing completion. Work has also begun on a companion standard known as FDDI-II. This is a hybrid network designed to support both isochronous circuit switching and packet switching modes of operation [1].

A FDDI network is composed of stations which are serially connected by dual fiber optic transmission links to form a closed loop, as shown in Fig. 1.1. The dual fibers produce two rings, a primary data ring and a redundant ring operating in the reverse direction. If a fault occurs in the transmission of the primary ring, the loop can reconfigure. By looping back on the redundant path a larger ring can be formed that avoids the fault.

Fiber loss and bandwidth considerations limit the length of each dual fiber link to 2 km. Although there is no limit to the length of the ring and the number of stations, default timer values have been chosen for a maximum ring length of 100 km and 500 stations.

Transmission at 100 Mb/s is implemented using a 4b/5b code. Four bit data symbols are coded into 5 bit line symbols for transmission between stations. The 5 bit symbols are read using a clock recovered
Fig. 1.1 FDDI Loop.
from the transmitted data. They are retransmitted using the independent 125 MHz station clock. This point to point clocking avoids the synchronization delay and jitter accumulation which can cause problems when data symbols are regenerated multiple times.

Data encoding schemes are numerous and each has its own benefits. As the FDDI encoding scheme is new, it is analyzed for its features and compared to existing codes. Of particular interest is the transmission bandwidth necessary and the clock content available.

Clock recovery has remained a topic of interest for decades. The basic concerns of recovering a clock from digital baseband data were investigated by Bennet [2] in his 1958 paper, "Statistics of Regenerative Digital Transmission". This paper focused on clock recovery using a tuned circuit. Later investigators applied phase-locked loops to the same problem. One of the major concerns discussed in the literature, the accumulation of jitter after multiple regenerations, has been removed by the point-to-point clocking used in FDDI. Other basic concerns remain.

This thesis will investigate the advantages of phase-locked loop clock recovery, and the concerns when it is applied to FDDI. Most of the literature on PLL design is on frequency demodulation, frequency synthesis, or oscillator stabilization. Clock recovery from baseband data has a number of unique aspects. By presenting and testing a PLL design for FDDI, these aspects are investigated.

Clock recovery from FDDI has several unique aspects. The data rates are faster than most existing commercial systems, the data encoding is a new format, and complete retiming is performed at each
regenerator. This thesis investigates the concerns of clock recovery in FDDI. Based on the preliminary specification, a clock recovery circuit was designed, built, and tested.
2. CLOCK RECOVERY

2.1 Introduction

The transmission of data by pulse coded modulation (PCM) is achieved by encoding the data into a series of pulses. Typically the data is encoded into a binary sequence, with a "one" representing a pulse and a "zero" the absence of a pulse. This pattern of 1's and 0's comprises the message sequence:

\[(a_n)_{n=-\infty}^\infty = \ldots , a_{-1} , a_0 , a_1 , \ldots \]  (2.1)

where: \(a_n\) = a message value.

The spacing of the pulses is controlled by the data clock. Thus the binary waveform is given by:

\[x(t) = \sum_{n=-\infty}^{\infty} a_n d(t-nT),\]  (2.2)

where: \(d(t)\) = pulse shape, and \(T\) = clock period.

The message sequence can be recovered from the binary waveform by sampling in each bit period. This sampling process requires knowledge of the data clock. The clock can be sent along with the data or, as in this application, it can be recovered from the binary waveform. Clock recovery can be aided by choosing a form of encoding that insures sufficient clock content. The clock content of the message waveform is affected by the message statistics and the pulse shape. Relevant statistical calculations and assumptions are briefly reviewed in Appendix A.
2.2 Power Spectral Density (PSD)

If the data or processed data spectrum has a spectral component at the clock frequency, it can be extracted by filtering. The calculation of the power spectral density is outlined in Appendix B. A general PSD equation is given in equation (B.5):

\[ S_m(\omega) = f_1 |D(\omega)|^2 \left\{ R(0) + \sum_{k=1}^{\infty} R(k) \cos(\omega k T) \right\} \]  \hspace{1cm} (2.3)

where, \( f_1 = 1/T \) = Incoming data clock frequency
\( D(\omega) \) = Fourier transform of the pulse shape \( d(t) \), and
\( R(k) = k^{th} \) autocorrelation of the pulse sequence.

The autocorrelation of independent data pulses, with probability \( p \) of being "one", is given by:

\[ R(k) = \begin{cases} p, & k=0 \\ p^2, & k \neq 0 \end{cases} \]  \hspace{1cm} (2.4)

For the case of independent pulses, Lathi [3] has rewritten the power spectral density to clarify the continuous and discrete components. For this case:

\[ R(0) + \sum_{k=1}^{\infty} R(k) \cos(\omega k T) = p + 2p^2 \sum_{k=1}^{\infty} \cos(\omega k T) \]

\[ = (p-p^2) + p^2 \sum_{k=-\infty}^{\infty} \delta(\omega - \frac{2nk}{T}) \]

\[ = (p-p^2) + p^2 \sum_{k=-\infty}^{\infty} \frac{2\pi}{T} \delta(\omega - \frac{2nk}{T}) \]  \hspace{1cm} (2.5)

This produces the following spectrum:

\[ S_m(\omega) = f_1 |D(\omega)|^2 \left\{ (p-p^2) + p^2 \sum_{k=-\infty}^{\infty} \frac{2\pi}{T} \delta(\omega - \frac{2nk}{T}) \right\} \]  \hspace{1cm} (2.6)

From inspecting (2.6) it can be seen that the power spectrum of \( \{x(t)\} \) is continuous and proportional to the square of the magnitude of the Fourier transform of the unit pulse. The spectrum also has
discrete components at the clock frequency, and its harmonics (providing the pulse spectrum has a non-zero value at these frequencies). These components are proportional to the value of the continuous unit pulse spectrum evaluated at that frequency. The amplitudes of the discrete components relative to the adjacent continuous spectrum will not be affected by the pulse shape but only by the autocorrelation of the message signal \( R(k) \).

If the pulses are rectangular \( D(\omega) \) is:

\[
D(\omega) = T_p \text{sinc}(\frac{\omega T_p}{2\pi}) \quad \text{where, } T_p \text{ is the pulse width [3].} \quad (2.7)
\]

If the pulses are full width (NRZ) then \( T_p = T \), and the clock frequency and its harmonics become zero. These frequencies also vanish from the data spectrum. Return to zero (RZ) pulses will have clock content in their spectrum but they require more bandwidth to transmit. A common solution is to transmit NRZ pulses, and at the receiver, produce an RZ pulse at each data transition. The rule for constructing the transition message is:

<table>
<thead>
<tr>
<th>Original Message</th>
<th>Transition Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 followed by 0</td>
<td>0</td>
</tr>
<tr>
<td>0 followed by 1</td>
<td>1</td>
</tr>
<tr>
<td>1 followed by 0</td>
<td>1</td>
</tr>
<tr>
<td>1 followed by 1</td>
<td>0</td>
</tr>
</tbody>
</table>

The similarity to the truth table for the XOR should be noted. The use of an XOR to produce a transition wave is discussed in chapter 7.

As the ratio of the power at the clock frequency to the continuous spectral power density is independent of the pulse shape, the length of the transition pulse is not critical. The magnitude of the power at the clock frequency will be reduced with very short pulses and with pulses
approaching a full bit period. In both extremes added noise may cause significant problems. The maximum power at the clock frequency for an approximately rectangular unit pulse shape occurs when the width of the pulse is $T/2$.

The pulses in this transition pulse stream are sequentially dependent, even if the original data pulses are independent. The PSD can be derived from the autocorrelation function. The amplitude of the clock relative to the continuous spectrum will be increased by more data transitions. If the original NRZ signal had independent pulses then $p_t = p(p-1)$, where $p_t$ is the probability of a transition. The maximum value $p_t = 0.5$ occurs when $p = 0.5$. It is possible by using a restricted code set (thus, the values of $a_n$ are no longer independent) to send a data stream that has a probability of transition that is greater than 0.5. FDDI uses a restricted code to increase the number of transitions in the transmitted data stream.

2.3 FDDI Encoding Scheme

FDDI uses 485B block encoding followed by transition encoding. The incoming data is handled as 4 bit words or symbols. The symbols are denoted by hexadecimal digits (0-F). The message symbols can occur in any order.

The block encoding turns each 4 bit symbol into a unique 5 bit NRZ blocks. There are 32 unique 5 bit blocks possible, of these only 22 meet the coding requirements. These are discussed in chapter 3. The 6 codes not used for data symbols are system control symbols. Fig. 2.1 shows the assignment of the five bit codes [4].
<table>
<thead>
<tr>
<th>DECIMAL GROUP</th>
<th>CODE</th>
<th>SYMBOL</th>
<th>ASSIGNMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LINE STATE SYMBOLS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>00000</td>
<td>Q</td>
<td>QUIET</td>
</tr>
<tr>
<td>31</td>
<td>11111</td>
<td>I</td>
<td>IDLE</td>
</tr>
<tr>
<td>04</td>
<td>00100</td>
<td>H</td>
<td>HALT</td>
</tr>
<tr>
<td>STARTING DELIMITER</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>11000</td>
<td>J</td>
<td>1st of Sequential SD Pair</td>
</tr>
<tr>
<td>17</td>
<td>10001</td>
<td>K</td>
<td>2nd of Sequential SD Pair</td>
</tr>
<tr>
<td>DATA SYMBOLS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>11110</td>
<td>0</td>
<td>Hex: 0, Binary: 0000</td>
</tr>
<tr>
<td>09</td>
<td>01001</td>
<td>1</td>
<td>1, 0001</td>
</tr>
<tr>
<td>20</td>
<td>10100</td>
<td>2</td>
<td>2, 0010</td>
</tr>
<tr>
<td>21</td>
<td>10101</td>
<td>3</td>
<td>3, 0011</td>
</tr>
<tr>
<td>10</td>
<td>01010</td>
<td>4</td>
<td>4, 0100</td>
</tr>
<tr>
<td>11</td>
<td>01011</td>
<td>5</td>
<td>5, 0101</td>
</tr>
<tr>
<td>14</td>
<td>01110</td>
<td>6</td>
<td>6, 0110</td>
</tr>
<tr>
<td>15</td>
<td>01111</td>
<td>7</td>
<td>7, 0111</td>
</tr>
<tr>
<td>18</td>
<td>10010</td>
<td>8</td>
<td>8, 1000</td>
</tr>
<tr>
<td>19</td>
<td>10011</td>
<td>9</td>
<td>9, 1001</td>
</tr>
<tr>
<td>22</td>
<td>10110</td>
<td>A</td>
<td>A, 1010</td>
</tr>
<tr>
<td>23</td>
<td>10111</td>
<td>B</td>
<td>B, 1011</td>
</tr>
<tr>
<td>28</td>
<td>11010</td>
<td>C</td>
<td>C, 1100</td>
</tr>
<tr>
<td>27</td>
<td>11011</td>
<td>D</td>
<td>D, 1101</td>
</tr>
<tr>
<td>28</td>
<td>11100</td>
<td>E</td>
<td>E, 1100</td>
</tr>
<tr>
<td>29</td>
<td>11101</td>
<td>F</td>
<td>F, 1111</td>
</tr>
<tr>
<td>ENDING DELIMITER</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>01101</td>
<td>T</td>
<td>Used to Terminate the Data Stream</td>
</tr>
<tr>
<td>CONTROL INDICATORS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>00111</td>
<td>R</td>
<td>Denoting Logical ZERO (Reset)</td>
</tr>
<tr>
<td>25</td>
<td>11001</td>
<td>S</td>
<td>Denoting Logical ONE (Set)</td>
</tr>
<tr>
<td>INVALID CODE ASSIGNMENTS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>00001</td>
<td>V or H</td>
<td>These code patterns shall not be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>transmitted because they violate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>consecutive code-bit zero or duty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>cycle requirements. Codes 01, 02, 08</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>and 16 shall however be interpreted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>as Halt when received.</td>
</tr>
<tr>
<td>02</td>
<td>00010</td>
<td>V or H</td>
<td></td>
</tr>
<tr>
<td>03</td>
<td>00011</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>05</td>
<td>00101</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>06</td>
<td>00110</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>08</td>
<td>01000</td>
<td>V or H</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>01100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>10000</td>
<td>V or H</td>
<td></td>
</tr>
</tbody>
</table>

(12345) = sequential order of code-bit transmission.

Fig. 2.1 FDDI Symbol Codes [4].
Transition encoding converts this NRZ stream into an NRZI (non-return-to-zero-invert-on-ones) transmission stream. In this format a transition indicates a '1' and no transition a '0'. The encoded NRZ blocks were chosen so that each NRZI transmission block would have at least two transitions.

At the receiver, the clock is recovered from the NRZI stream. The NRZI sequence is converted back into NRZ and put into a FIFO (first-in-first-out) "elasticity" buffer using the recovered clock [4]. The 5 bit blocks are removed from the "elasticity" buffer at the local clock rate and decoded into their hexadecimal symbols or recognized as control codes. Code violations are indicated at this time.

As FDDI uses NRZI to transmit, the net result after transition detection is the original data reproduced in RZ format. The autocorrelation for independent random data is not applicable because the restricted code makes the pulses dependent.

2.4 Summary

For a binary waveform, the relative power of the clock to the adjacent continuous power is dependent only on the message signal (not on the pulse shape). The total power in the clock signal is determined by the pulse shape and magnitude.

FDDI transmits full width pulses as they require less bandwidth. As full width pulses have no power at the clock frequency, clock power is obtained by using transition detection to produce an RZ stream. FDDI restricts the codes sent to produce more power at the clock frequency than would be obtained from random data.
3. FDDI DATA ENCODING

3.1 Introduction

The purpose of data encoding is to convey the message, system control codes, and clocking information. The signal must be transmitted in the bandwidth available and should be unaffected by the noise of the transmission channel. This discussion will cover baseband signalling techniques and will not cover carrier modulation.

The most suitable data encoding for a particular system is largely determined by the transmission channel. FDDI uses a multi-mode fiber with a minimum bandwidth of 400 MHz-Km. The maximum link length is 2 km, thus the bandwidth will be at least 200 MHz. At the transmitter a light emitting diode (LED) turns the electrical pulses into light pulses with a wavelength of approximately 1300 nm. A PIN diode receiver converts the received optical signal back into an electrical signal. The combination of light emitting diode, multi-mode fiber and PIN diode receiver can be cheaply implemented. FDDI transmits at 125 Mbps data. This is near the upper limit of data rates currently commercially implemented but it is expected that, with advances in this combination of components, operation will be feasible up to about 300 Mbps [5].

In all transmission channels, there are both high and low frequency limitations on the transmitted signal. In systems with electrical transmission, transformers are used to couple the signal to the channel. This allows dc power for repeaters to be sent along the same wires as the signal. Unfortunately, it also blocks low frequency components of the signal. For a specific high frequency cut-off
frequency in a transformer, it is costly to decrease its low frequency cut-off.

In a fiber based communication system, the receiver circuitry causes a dc offset. This can be removed with blocking capacitors. Their size determines the low frequency cut-off. The fiber itself does not restrict low frequencies. Thus, it is inexpensive to reduce the low frequency cut-off. The high frequency cut-off is determined in a fiber system by, the optical source modulation bandwidth, fiber dispersion, and the speed of the optical detector and the receiver electronics [5].

The clock information is included by adding redundancy to the original signal. In systems with electrical transmission channels, two methods are used. In the first, the signal rate is kept constant and signalling levels added. Usually a three level code such as bipolar or duobinary coding is chosen. The third level can also improve the dc balance and low frequency content. In the second method only two levels are used but the signalling rate is increased. Manchester (Bi-phase) coding is an example.

In systems using fiber transmission, multilevel coding is not common as it requires more complex and costly circuitry to produce and receive the multilevel optical pulses. Fiber based systems usually add the redundancy required for clocking and dc balance by increasing the transmission signalling rate.

The usual method of adding this type of redundancy in fiber systems is to use block codes, which are called mBnB codes. This coding changes a group of m bits from the message signal to n bits in the transmission signal, where n>m. Only a subset of the possible
transmission codes are needed to uniquely transmit the message codes. Some of the remaining codes can be used as control codes. The remaining transmission codes do not meet clocking criteria and are not used.

Scrambling is another technique used to help insure clocking content. This produces no increase in bit rate and is simple to implement. It improves clocking by breaking up long strings of ones and zeros and short repetitive data streams. Scrambling makes the message sequence look more like a random data sequence. This tends to even the distribution of transitions and reduce pattern dependent jitter, but does not guarantee a minimum transition density [6].

Scrambling can be combined with overhead bits. In this type of encoding, k overhead bits are inserted after every m scrambled message bits. Often one of the overhead bits is a parity bit thereby allowing some error monitoring. If odd parity is used, a transition is insured every m+k-1 bits. The remainder of the overhead bits are usually used for system control and framing. The length m is generally large, as this encoding is used when bandwidth is at a premium.

FDDI has a dual-embedded coding scheme. First, the data are coded from 4 bit blocks into 5 bit blocks. Then it is transmitted in NRZI format. NRZI coding can be considered transition encoding or '2-bit' scrambling.

3.2 FDDI Coding Performance

Listed below are six areas of concern when evaluating a coding scheme. The performance of the FDDI code is discussed in each area.

1) Increase in bit rate
Scrambling and transition encoding do not increase the bit rate. In block and overhead encoding the ratio of the transmitted bit rate to the message bit rate is given by \( n/m \) and \( m+k/m \) respectively. This increase in bit rate is also a measure of redundancy and increased bandwidth. If the receiver noise is flat across the entire bandwidth and dispersion effects in the fiber are negligible an \( n/m \) (or \( m+k/m \)) increase in source power is required to maintain the same signal to noise ratio (SNR). If dispersion or receiver noise increases with frequency, then the penalty is greater. With greater redundancy, tighter clocking criteria can be set. However, this is limited by the system bandwidth and the signal power available.

The small block size of FDDI results in a 25% increase in bit rate, \( (n/m=1.25) \). Available multi-mode fibers can easily meet this bandwidth requirement. Larger data blocks (ie 5B6B, 6B7B etc) may achieve similar performance to 4B5B at lower transmission rates but the convenient half byte relationship is lost.

2) Clock Content
a) Transition Density

The average density of transitions determines the necessary 'Q' (quality) in the clock recovery circuit. There is a worst case group of codes that have only two transitions per code. If only these codes are sent the probability of transition is \( 2/5 \) or 0.4. The best case data codes have 4 transitions. With only these codes transmitted the probability of transition is \( 4/5 \) or 0.8. The greater the difference between the maximum and minimum probability of transition, the greater the data dependent jitter. If all data codes are equi-probable, the
average transition density of the FDDI code is 60.9% \( (p_t=0.609) \). This is an improvement over the 50% obtained with uncoded equi-probable random data.

The best code for clock content is the idle pattern as it has all transitions \( (p_t=1) \). Whenever data is not present, this code is sent to maintain the clock synchronization.

b) Run Bound (RB)

This is the maximum number of sequential bits that can occur without a transition. The longer the period without transitions the higher \( Q \) must be.

The run bound in FDDI is 3 bits. The data codes and most of the control codes, in Fig. 2.2, can be transmitted in any order and will still satisfy the run bound. The J and K symbols are always transmitted sequentially. In this order the run bound requirement is met.

3) DC Balance

a) Maximum cumulative dc value \( (\pm x\%) \)

This is a measure of the amount the dc balance varies. When block coding is employed, the block code with the minimum "dc value" sets the lower limit of the cumulative dc value. The block code with the maximum "dc value" sets the upper limit. These limits can be expressed as percentage distortion from the nominal average value of the code. The nominal average value is the dc value that occurs if all block codes are equally likely.

In FDDI there are 5 bits to a transmission code and at least two transitions. A given data code when transmitted in NRZI form will have a dc balance of 40% or 60%, depending on whether previous transmitted
NRZI symbol ended in a 1 or a 0. The nominal average value is 50%, therefore, the maximum cumulative dc balance is ±10% from the nominal average value. When the idle signal is repeated the balance is exactly 50%.

Large transmitted power, decreases the transmitter lifetime and increases the cooling it requires. For a random binary sequence the average power transmitted is the same as the dc balance. The FDDI 4B5B code limits the duty cycle of the transmitter and prevents overload.

b) Running Digital Sum (RDS)

It is sometimes more convenient to measure the dc balance as the Running Digital Sum (RDS). This measurement treats the transmitted sequence as bits and not as blocks. If the transmission sequence is:

\[ (a_n)_{n=0}^k \]

where: \( a_n \) = transmitted value (1 or 0)

Then the running digital sum at instant \( k \) is:

\[ \text{RDS} = \sum_{n=0}^{k} a'_n, \]

where: \( a'_n = 1 \) if \( a_n = 1 \), and \( -1 \) if \( a_n = 0 \).

The maximum absolute value of the RDS indicates the amount the instantaneous average voltage changes. In some systems the RDS is monitored at the receiver and an error is indicated if the maximum RDS is exceeded. The RDS is not bounded in the FDDI code and therefore cannot be used.

4) Frequency content

The frequency content of the code is important as low and high
frequency components can be lost due to the characteristics of the channel. The loss of low frequency components will cause the optimum threshold or decision level at the receiver to wander. The loss of high frequency components cause the received eye pattern to narrow due to reduced slew rate [8]. Thus the FDDI fiber transmission system must have a bandwidth which encompasses nearly all of the energy of the NRZI code power spectrum. In the transition RZ code produced in the clock recovery circuitry, the relative power at the clock frequency will determine the amount of jitter in the extracted clock.

The PSD for the NRZI and the corresponding transition RZ code appear in Fig. 3.1. The plots are calibrated in terms of clock frequency. They were produced at a much lower frequency than 125 MHz, by using a VIC-20 microcomputer to encode random 4 bit symbols to the FDDI transmission codes. The transition RZ pulses are half bit period long.

Fig. 3.1a shows the spectrum of the transmitted code. There are no discrete components and there are nulls at the clock frequency and its harmonics. This is expected from full width rectangular pulses. The minimum fiber bandwidth of 200 MHz will encompass the entire first lobe (up to 125 MHz) and most of the second lobe. This should produce reasonably sharp pulses at the receiver.

The highest concentration of power is around $P_s/3$. The power drops off towards dc but is not zero. This is as expected from the dc balance calculations. There is also a noticeable dip in power at $P_s/2$. Although it will not affect the transmission characteristics, it is noticeably different from the spectrum of random full width pulses (NRZ).
Fig. 3.1 Power Spectral Density of FDDI Data:
(a) During Transmission; (b) After Transition Detection.
In Fig. 3.1b the received data has been transition decoded. A half bit pulse was produced at each transition. The half bit length has moved the first null to 2F_s. Discrete spectral components have appeared at the clock frequency and its odd harmonics. This produces a strong signal from which to recover clock. Again, the flat top of the lobes distinguishes this spectrum from random half bit wide RZ data.

5) Error Performance

a) Bit Error Multiplication

This is a measure of the number of bits that will be decoded incorrectly if one bit is corrupted in the channel. In transition encoding each transmission error causes two bit errors after decoding. Systems using scrambling also have bit error multiplication. The amount of multiplication will depend on the scrambling algorithm used [6].

b) Symbol Error

Symbol error is usually a better measure of the system error performance than bit error. In block encoding one incorrect bit will cause the entire block to be incorrectly decoded. However, several incorrect bits in one block still only cause one symbol error.

c) Error Detection and Correction

This is the ability to detect and in some cases correct bits that have been incorrectly received. In block encoded data, symbol errors can be detected when unused codes are received, but the majority of single bit errors are not detectable. Reliable detection or correction requires higher redundancy. Cyclic redundancy check bits can be appended to a message to allow error detection but do not usually allow correction.
The FDDI combination of block and transition encoding produces a symbol error rate only slightly worse than block encoding alone. Transition decoding causes two adjacent bits to be decoded incorrectly for every one received in error. This will cause one hexadecimal symbol to be incorrect, unless the errors span the block boundary. This happens one fifth of the time. Thus the FDDI symbol error rate due to error multiplication is $6/5$, times that of 4B5B encoding alone. FDDI encoding has some error detection ability but will not catch all errors in which one bit was corrupted in transmission. It can not correct errors.

6) Encoder/Decoder Complexity

The complexity of encoding, decoding and symbol synchronizing circuitry increases with increased block length. The choice of 4B5B block encoding interfaces well with computer storage which often has a hexadecimal base. The block size is relatively small and the encoding and decoding function can be achieved with small ROM (Read Only Memory) chips. Scrambling and transition encoding do not require symbol synchronization, and can be encoded and decoded with simple circuitry.

3.3 Analysis of Alternatives to the FDDI code

The FDDI performance can be put in perspective by comparing it to other two level codes. In 4B5B block encoding without NRZI coding, the best 22 codes have a run bound of 4 bits. It has average transitions of 57.2% and minimum and maximum of 40% and 100% respectively. This is similar to the FDDI clock content. The maximum cumulative dc average is
much worse as it varies 10% to 90%. Thus the block encoding alone is inferior to the FDDI combination of block and transition encoding.

Using a 4B6B block format with NRZI coding will produce a code in which all blocks are exactly dc balanced, have at least two transitions and are run bounded by three. The 21 usable codes that result have a 59.1% average transitions, 33% minimum and 100% maximum. The biggest drawback of this code is a further 25% increase in bit rate, which is a large price for better dc balance.

The dc balance can also be improved by monitoring the Running Digital Sum (RDS). Each code has a dc value of either +10% or -10%. The RDS indicates the balance of the sequence already transmitted. Each code is then sent in the polarity that will correct the dc balance. The receiver can correctly decode if it also monitors the RDS. The encoder/decoder circuitry is more complex in this coding system. If an error occurs in transmission, the error multiplication will be greater than in the scheme chosen for FDDI.

Manchester (Bi-phase) code has three variations. They are similar, as all provide a transition every bit period and have the same PSD. Manchester I (Bi-phase mark or digital FM) is a common form. It has a transition at the beginning of each bit, with an additional midbit transition in the '0' pulse. Although there is 100% clock content and very little low frequency this is achieved by a factor of two increase in bandwidth [7].

In Miller code (delay modulation) a '1' is sent by a midbit transition. A '0' preceded by a zero has a transition at the beginning of the bit period, otherwise a '0' has no transition. This code insures
a transition every 1.5 bits, requires no increase in bandwidth, and has very little low frequency content. Unfortunately, determining the correct phase of the clock requires a 'one'-'zero'-'one' sequence [7].

An advantage of block codes over Miller and Manchester codes are the unique control codes. This protects control codes from being mistaken as data and generally means less complex coder/decoder circuitry is required.

3.4 Summary

The FDDI encoding scheme combines block encoding with transition encoding. The 22 codes which include 6 unique control codes provide reasonable dc balance and reasonable clock content. The penalty paid is slightly higher symbol error multiplication, and slightly more receiver and transmitter circuitry. Overall the FDDI code compares very well to other two level codes.
4. **JITTER IN THE RECOVERED CLOCK**

4.1 **Jitter**

The clock recovery filter can either be a tuned circuit or a phase-locked loop. To evaluate these options, the quality of the extracted clock must be measured. Jitter is the standard measurement of clock quality.

Jitter is a measure of the phase variation of the clock or data period. It is given in units of radians, degrees or bit periods and as a peak-to-peak or rms value. The phase error can be measured from the expected axis crossing of the waveform, or a desired axis crossing. Usually the average component of the phase error is not included in the jitter calculation. The rms phase error or jitter is:

\[ \epsilon_{\text{rms}} = \sqrt{\langle \epsilon^2 \rangle} \]  

where: \( \epsilon = \) phase error from mean zero crossing time.

4.2 **Jitter Tolerance**

Jitter produced by a communication system can be analyzed in three stages. The first stage is the data jitter that is produced in the transmission circuitry and channel. The second stage is the jitter on the recovered clock from a single retiming circuit. The third stage is the jitter accumulation that occurs when the data is regenerated multiple times using recovered clocking.

Most of the published work on jitter is concerned with the third stage. The jitter accumulation in a chain of regenerators is due to noise at each regenerator and pattern effects. As the same pattern is
present at each repeater, the accumulation of pattern jitter increases more rapidly than with random noise effects.

This third stage of jitter is avoided in FDDI by using an independent clock at each repeater to transmit the data. Thus, only the clock jitter produced in a single retiming circuit and the data jitter is of concern.

Jitter tolerance is a measure of how much jitter can be present without a significant increase in the probability of error. The peak phase error influences the probability of error. Given a rms value of Gaussian distributed jitter, an effective peak value can be found using a peaking factor. The probability of exceeding the effective peak value is used to set the peaking factor.

The optimum sampling point is in the center of the eye opening for each data bit [8]. Jitter on the incoming data closes the eye pattern. Average phase errors due to mistuning offset the average sampling point from center, and clock jitter distributes the sampling about the average. Thus to correctly recover the data:

\[ \frac{T}{2} > \epsilon_m + J_o + J_d \]

where: 
- \(J_d\) = peak jitter on the information pulse,
- \(J_o\) = peak jitter on the clock,
- \(T\) = bit period (width of information pulse), and
- \(\epsilon_m\) = static mistuning phase error of the clock.

This is illustrated in Fig. 4.1.

4.3 Jitter from Tuned Circuit and PLL Clock Extraction

The factors causing jitter in the recovered clock can be evaluated by developing statistical equations. This has done by Bennet [2] for tuned circuit recovery and by Roza [9] for PLL recovery. As
there is a number of printing errors in Bennet's paper "Statistics of
Regenerative Digital Transmission" the development of the equations is
included in Appendix C. The final results agree with Bennet's but some
of the intermediate steps differ from the published work. Appendix D
outlines the development of the equations for the PLL as found in
Roza's paper "Analysis of Phase-Locked Timing Extraction Circuits for
Pulse Code Transmission". An intuitive route is followed in this
section quoting the final results found by Bennet and Roza. The results
for the PLL, all assume the loop is second order. Loop order is
discussed in chapter 5.

The ideal resonant circuit for clock extraction would have
infinite Q and would be correctly tuned to the bit frequency. Thus, it
could separate the clock from the surrounding spectrum and would
continue to output the clock even with widely spaced data transitions.
In a practical system the tuned circuit resonant frequency will deviate from the clock frequency. The bandwidth must be enlarged to accommodate this deviation. Thus, power near the clock frequency also passes through. The output amplitude will also vary if transitions are widely spaced due to decay in the resonant circuit.

The ideal phase-locked loop would have a VCO correctly centered on the bit frequency, and a very narrow low pass filter to sustain the flywheel effect over missing pulses. The VCO in a practical phase-locked loop will also be slightly mistuned, and the narrowness of the lowpass filter will be restricted by the required acquisition time, as discussed in chapter 5. The clock produced by either method will therefore have some jitter as a result of mistuning and filter bandwidth.

General equations for jitter are very difficult to solve but can be simplified. The following calculations of this jitter are valid only when the bandwidth is much less than the bit rate, there is sufficient clock content, disturbances to the system are linear and the noise effects are independent of pattern [9].

4.3.1 Mistuning Phase Error ($\epsilon_m$)

The signal arriving at the clock recovery circuit can be separated into a periodic waveform, a random data waveform and noise. Viewed in the frequency domain the periodic waveform produces discrete components at the incoming clock frequency and its harmonics. For the periodic component a bandpass filter or resonant circuit at the fundamental frequency will recover the clock perfectly. If the circuit is mistuned
the output amplitude will be reduced and a static mistuning phase shift \((\epsilon_m)\) added. The output clock, \(c(t)\), will be:

\[
c(t) = \cos(\epsilon_m)\cos(\omega_2 t - \epsilon_m),
\]

where:
\[
\tan(\epsilon_m) = Q(\omega_2/\omega_a - \omega_a/\omega_2),
\]

\(Q\) = quality of the tuned circuit, and
\(\omega_a\) = center frequency of tuned frequency.

Therefore, if \(\epsilon_m \ll 1\):

\[
\epsilon_m = \frac{2Q(\omega_2-\omega_a)}{\omega_2}.
\]

In a PLL with a center frequency of the oscillator different from the incoming frequency, a phase offset is produced that adjusts the loop frequency. This static angle due to mistuning is given by (D.13):

\[
\epsilon_m = \frac{\omega_2-\omega_a}{\omega_2 K_v}
\]

where: \(K_v\) is the DC loop gain, and \(\omega_a\) = center frequency of the tuned circuit.

4.3.2 Pattern Dependent Jitter

The random data waveform produces a continuous spectrum. Depending on the pulse shape there will also be discrete spectra at the harmonics of the data rate. If the pulses are short enough to be considered impulses, the continuous spectrum will be flat around the clock frequency and the continuous power will be constant over the bandwidth of the tuned filter. The approximation holds for rectangular pulses not exceeding half the clock period. The response of a narrow bandpass filter centered at incoming clock frequency is an amplitude modulated sinusoid at the frequency of the resonant circuit. A lower quality tuned circuit allows more interfering spectral components and hence has larger amplitude modulation.
In the case where there is sufficient clock content and high Q, the clock amplitude varies only slightly and the clock waveform can be predicted. With no mistuning the recovered clock will be amplitude and phase modulated but will have the correct average frequency. In this case the expected output clock is given by (C.11) and is reproduced below:

\[ E(c(t)) = \frac{\pi \omega_s (4Q^2+1)^{1/2} \exp(-\omega_s t/N/20) \cos(\omega_s (t-T/2)+\theta)}{4RQ^2 \sinh(N/20)}. \]  

(4.6)

Thus the initial amplitude depends on the mean of the message signal \( m_1 \) and the rate of amplitude decay depends on the value of Q.

If the circuit is mistuned the recovered clock power will be reduced while the interference power remains unchanged. The interference power will now be maximum at the resonant frequency. This pulls the average output clock frequency away from the data frequency toward the resonant frequency. The relationship between pattern jitter, mistuning, and quality, where \( (\omega_o - \omega_s)/\omega_s << 1 \) and \( Q > 1 \), is given by (C.37):

\[ E(\epsilon^2) = \frac{(\omega_o - \omega_s)^2 (1 - m_1)Q}{\omega_o^2 m_1}. \]  

(4.7)

This result is important as it shows that with any mistuning the rms jitter will increase by the square root of the Q factor. Therefore, an infinite Q is not desirable in the practical case.

The filtering in a PLL is achieved with a lowpass filter near dc, not at the data rate. A comparison to tuned circuits can be made if an effective quality is assigned to the PLL. Roza [9] defines this \( Q_{eff} \) as:

\[ Q_{eff} = \frac{\pi}{4TB_s}. \]  

(4.8)
where, $B_n$ = noise bandwidth of PLL (Hz), and $T$ = bit period.

For the PLL the pattern jitter is then given by (D.20):

$$E(\varepsilon_n^2) = \frac{\pi}{m_140\text{eff}} \left[ \frac{(\omega_n - \omega_o)^2(1 - m_1)\pi}{(\omega_n - \omega_o)^2(1 - m_1)\pi} \right]$$

Thus, an increase in $Q$ or dc gain $K_o$ will decrease the pattern jitter. In practice a large dc gain will not eliminate pattern jitter unless the free running frequency of the PLL is identical to the input frequency. This is discussed in more detail in chapter 7.

The above formulas for pattern jitter hold only for messages with independent pulses.

### 4.2.3 Jitter due to Noise

Noise causes phase variations even when the filter is correctly tuned. If the shifts due to noise are independent of each other and of the message values the jitter can be calculated. There is no requirement for the message pulses to be independent. The relationship of jitter to noise for the tuned circuit is given by equation (C.49),

$$E(\varepsilon_n^2) = \frac{\pi \omega_n^2 r_n^2 \pi}{T^2 m_1^2 2Q}$$

where, $r_n^2$ = variance of the shift in zero crossing time due to noise.

Thus the larger the value of $Q$ the less phase noise will be caused by the noise on the input waveform.

For the PLL, the jitter contribution due to noise is given in (D.25):

$$E(\varepsilon_n^2) = \frac{\pi \omega_n^2 r_n^2 \pi}{T^2 m_1^2 2Q_{\text{eff}}}$$

This again shows the noise jitter will decrease with an increase in
4.3.4 Overview

Increasing the quality of a clock recovery tuned circuit will reduce the effect of noise and help keep the output amplitude constant. However it will increase the effects of mistuning. If the noise and mistuning are known, \( Q \) can be optimized.

The output clock from a PLL clock recovery circuit has constant amplitude and the mistuning phase error can be reduced to an sufficiently low value by a large dc gain (\( K_\omega \)). Thus, \( Q_{\text{eff}} \) can be made large (noise bandwidth small) to reduce the effect of noise. Equation (4.10) indicates pattern jitter can also be reduced to zero by a large dc loop gain. In a loop whose free running frequency is not the same as the incoming frequency this will not be the case. The independence of the mistuning phase error from noise jitter is the main benefit of a PLL recovery circuit. The increase in acquisition time that accompanies an increase in \( Q_{\text{eff}} \) will be discussed in chapter 5.

4.4 Jitter Allocation

4.3.1 Data Jitter Allocations and Measurement

The FDDI data jitter specifications [10] are broken into three categories, Duty Cycle Distortion (DCD), Data Dependent Jitter (DDJ), and Random Jitter (Ran). They are measured from the nominal average or 50% point. For measurement purposes this is the zero crossing of the AC coupled signal.

Duty cycle distortion is the shrinkage in the eye pattern caused
by differences in delay from low-to-high and high-to-low transitions. It is measured when the idle pattern is sent continuously. The idle pattern is a 62.5 MHz square wave. DCD is specified as a zero-to-peak value, and its values are added linearly through the system.

**Data dependent jitter** is due to the data pattern combined with bandlimiting, non-zero DC balancing, and imperfections in the system. It is measured with a specified "worst case" data sequence. The contribution from DCD as measured above is subtracted. The DDJ measurements are also given in zero-to-peak values but are added as the square root of the sum of squares.

**Random jitter** is mainly due to thermal noise. It is considered a Gaussian process and is measured in rms values using an "idle" data pattern, to eliminate contribution from DDJ. The DCD component is again subtracted. Random jitter is added as the square root of the sum of the squares. The total is multiplied by a peaking factor to give the peak value. A peak to rms value of 6.3 is specified for this application. The probability of exceeding this value is \(2.5 \times 10^{-10}\) (6.3 standard deviations).

The FDDI specifications of maximum data jitter at the input to the clock recovery circuit are:

- D\_DCD 1.0 ns peak
- D\_DDJ 0.90 ns peak, and
- D\_RAN 0.180 ns rms.

### 4.3.2 Clock Jitter Allocation

FDDI specifications do not give precise recovered clock jitter allocations. However, the total peak data and clock jitter and
mistuning phase error must not exceed the peak eye opening of 4.0 ns:

\[ \frac{T}{2} \geq \text{data jitter + clock jitter + } \epsilon_m \]

\[ \geq D_{DCD} + D_{DDJ} + C_{DCD} + C_{DDJ} + 6.3(D_{RAN^2} + C_{RAN^2})^{1/2} + \epsilon_m \]  \hspace{1cm} (4.12)

In a high dc gain PLL the mistuning phase error \( \epsilon_m \), will be reduced to almost zero. The exact allowable peak jitter will depend on the distribution between duty cycle distortion, data dependent jitter and random jitter. A conservative estimate can be made by assuming the peak random clock jitter and the peak random data jitter add linearly. Thus:

\[ 4.0 \text{ ns} \geq J_e + J_a + \epsilon_m \]

\[ \geq D_{DCD} + D_{DDJ} + 6.3D_{RAN} + J_a + \epsilon_m \]

\[ \geq 1.0 \text{ ns} + 0.9 \text{ ns} + 6.3(0.18) + J_a + 0 \text{ ns.} \]  \hspace{1cm} (4.13)

Therefore:

\[ J_a \leq 1.9 \text{ ns peak} \]  \hspace{1cm} (4.14)

This estimate also neglects the benefits gained by the PLL tracking the data jitter.

4.5 Summary

Phase-locked loop clock extraction has several advantages over tuned circuit extraction. The chief of these is that the mistuning phase error can be reduced to zero without increasing the noise jitter. The allowable jitter in the clock depends on the data jitter present, the width of the data pulse, and the relative importance of the jitter causing mechanisms. When using a high dc gain PLL, a conservative estimate of allowable clock jitter is 1.9 ns peak.
5. PHASE-LOCKED LOOP OVERVIEW

The three basic components in a phase-locked loop (PLL) are a phase detector, a loop filter and a voltage controlled oscillator (VCO). The phase detector compares the phase of the incoming signal to that of the VCO signal. Its output is low pass filtered, and applied to the VCO to control the output frequency. A basic PLL is shown in Fig. 5.1.

![PLL Diagram](image)

Fig. 5.1 Basic PLL Configuration

5.1 Basic Loop Equations

Mathematical descriptions of the three loop components can be combined in an equation to predict the loop's performance. The following equations assume the loop is locked. Linear mathematical descriptions make the equation easier to solve and are used wherever reasonable.

If the phase detector is linear, its output \((V_d)\) is proportional to the difference in phase between its inputs:
\[ V_e(s) = K_d(\theta_1(s) - \theta_o(s)) + \text{high frequency terms} \]
\[ = K_d\theta_m(s) + \text{high frequency terms} \quad (V), \quad (5.1) \]

where: \( \theta_1(s) = \text{phase of input signal (rad)} \),
\( \theta_o(s) = \text{VCO phase angle (rad)} \),
\( K_d = \text{phase detector gain (V/\text{rad})} \),
\( V_e(s) = \text{phase difference voltage (V), and} \)
\( \theta_m(s) = \theta_1(s) - \theta_o(s) = \text{phase error (rad)}. \)

The phase difference voltage is passed through a low pass filter with transfer function \( P(s) \). This filter removes high frequency components and noise. The output of the filter is the control voltage, \( V_o(s) \):
\[ V_o(s) = P(s)V_e(s) \quad \text{(Volts).} \quad (5.2) \]

The VCO has an output frequency proportional to the input control voltage. The output phase \( \theta_o(s) \) is obtained by integrating:
\[ \theta_o(s) = \frac{K_oV_o(s)}{s} \quad \text{(rad),} \quad (5.3) \]
where: \( K_o = \text{VCO gain (rad/V-s).} \)

The locked PLL can be analyzed as a feedback control system. The open loop transfer function \( G(s) \) is the forward path and contains the phase detector, filter and oscillator. It is given by:
\[ G(s) = \frac{K_oK_dP(s)}{s} \quad (5.4) \]

In a basic PLL the feedback path is unity \((B(s)=1)\). The closed loop transfer function \( T(s) \) relates the output phase to the input phase, and is given by:
\[ T(s) = \frac{\theta_o(s)}{\theta_1(s)} = \frac{G(s)}{1 + G(s)H(s)} \]
\[ = \frac{K_oK_dP(s)}{s + K_oK_dP(s)} \quad (5.5) \]

The loop noise bandwidth \( B_L \), can be found by integrating the closed loop transfer function:
Specific loop bandwidths will be discussed with filters in section 6.3.

The error response of the loop, relates the phase error to the input phase. It is given by:

$$\frac{\theta_m(s)}{\theta_i(s)} = \frac{1}{1 + G(s)H(s)} = \frac{1}{1 + K_v K_d F(s)}$$  \hspace{1cm} (5.7)

The gain of the loop will be frequency dependent if a loop filter is included. The DC gain of the loop is denoted $K_v$ to correspond to the velocity error constant found in control theory. It is given by:

$$K_v = K_v K_d F(0).$$  \hspace{1cm} (5.8)

The high frequency gain, $K_m$, is given by:

$$K_m = K_v K_d F(\infty).$$  \hspace{1cm} (5.9)

### 5.2 Loop Order

The order of a PLL is given by the number of poles in the closed-loop transfer function, $T(s)$. A first order loop is obtained by omitting the filter altogether, thus $F(s)=1$. Second order loops have low pass filters with one pole, and third order loops have two pole low pass filters. Loops of higher order are not generally used as stability becomes a problem.

Narrow noise bandwidth and good tracking of the input signal are desired in a PLL. First order loops and second order loops using a simple lag filter ($F(s)=1/(sT+1)$), are seldom used as bandwidth must be sacrificed to obtain good tracking response.

Second order loops using lead-lag filters are the most commonly implemented. They are unconditionally stable and have independent
control of the loop noise bandwidth and tracking. Lead-lag filters can be passive or active as discussed in Chapter 6.

5.3 Loop Type

The phase-locked loop type is determined by the number of perfect integrators. The VCO is a perfect integrator, so all loops are Type I or higher.

The PLL design is largely determined by the desired time domain error response. Type I systems give zero steady state error for an input unit step in phase, a constant error to an input phase ramp, and an unbounded error to an accelerating phase input.

Type II systems produce a zero steady state error to both step and ramp phase inputs, and a constant error to an accelerating phase input. Thus the type II loop is the more desirable configuration.

A type III loop will have zero steady state error in response to step, ramp and acceleration inputs. These filters are more complex and the loop can be made stable only at certain gains.

5.4 Hold-in, Pull-in and Lock-in Ranges

A PLL has three input signal frequency ranges that describe its operation. Unfortunately, several different names for these ranges are in use. The relative size of these ranges and their more common names are shown in Fig. 5.2. This report will use the terms hold-in, pull-in and lock-in as defined by Gardner [11]. The hold-in range $R_h$ is the range of frequencies over which the loop can track if it is already successfully locked. The pull-in range is the frequencies over which
the loop can acquire lock, and the lock-in range is the frequencies over which lock is acquired without cycle slipping.

\[
\begin{align*}
R_H & \quad R_P \quad R_L \\
\text{Hold-in} & \quad \text{Pull-in} \quad \text{Lock-in} & \quad \text{Gardner [11], Krause [12], Klapper[13]} \\
\text{Lock} & \quad \text{Capture} \quad ----- & \quad \text{Kaufman [14], RCA [15]} \\
\text{Synchronization} & \quad \text{Acquisition} \quad ----- & \quad \text{Blancard [16]}
\end{align*}
\]

Fig. 5.2 Frequency Range Terms in Common Use.

The hold-in range is determined by the first loop component that saturates. In a loop where the phase detector can reach its maximum without saturating the other loop components, the hold-in range is given by:

\[
R_H = \pm v_{\text{max}}K_v, \quad (5.10)
\]

In a high gain loop, the active filter or the VCO usually saturates before the phase detector. For the case of the amplifier saturating first:
\[ R_m = \pm \frac{(V_{\text{max}} - V_{\text{min}})}{2} K_v, \quad (5.11) \]

and for the case of the VCO limiting the range, the hold-in range is equal to the VCO tuning range.

5.5 Acquisition

Acquisition is the process of adjusting the frequency and phase of the loop oscillator to that of the incoming signal.

5.5.1 Frequency Acquisition

Frequency acquisition is the process of adjusting the loop oscillator to the incoming frequency. If the initial frequency difference is very large, the input signal cycles will slip in and out of phase with the loop clock before the frequency can be acquired. This is called cycle slipping.

During cycle slipping, the output of the phase detector has a beat note. Its frequency is given by the difference frequency of the VCO and the input signal. On one half of the beat note the control voltage forces the loop toward the input frequency, thereby reducing the beat note frequency. On the other half, the voltage opposes acquisition by pushing the loop frequency away from the input frequency and increasing the frequency of the beat note. The aiding half of the beat note will become longer and the opposing half shorter, producing an average dc component. The loop filter attenuates high frequencies and amplifies the dc and low frequency components of the control signal. This pulls to the correct frequency and locks the loop.

If the loop filter contains a perfect integrator all frequencies
within the hold-in range will eventually lock, although cycle slipping may occur for long periods. If the loop filter integration is not perfect, there are some input frequencies where the VCO will continuously cycle slip and never acquire lock. The range of frequencies over which the VCO can acquire lock with cycle slipping is the pull-in range. When the initial frequency difference is small enough, the frequency is acquired without cycle slipping. This range of input frequency is called the lock-in range.

In a loop employing an active filter with very high DC gain and low voltage offsets, the pull-in range nearly equals the hold-in range. In loops using passive filters the pull-in range is much smaller. First order loops having no filter have a lock-in range equal to their hold-in range. The term pull-in range is not generally applied to these loops, as they cannot acquire lock if cycle slipping occurs.

The frequency acquisition of a phase-locked loop is a very nonlinear process. During cycle slipping, the feedback is sometimes positive and sometimes negative. To further compound the problem, each integrator in the loop adds a state variable to the analysis. The initial value for each state variable must be known for a complete analysis. For a second order loop, both the initial phase and frequency are needed to predict the exact response. The equations that result cannot be solved analytically. Viterbi [16] has produced phase-plane plots that graphically display a family of solutions for second order loops with specific phase detectors and damping ratios.

Defining the lock-in range in terms of frequency only is not completely accurate but is a useful (and solvable) engineering
approximation. For a first order loop the lock range is given by its gain. In higher order loops the high frequency gain, $K_m$ (as illustrated in Fig. 6.6), approximates the lock-in range:

$$ R_L = \pm K_m \quad \text{(rad).} \quad (5.12) $$

This approximation tends to be more conservative than the average lock-in frequency determined from the Viterbi phase-plane plots [16].

5.5.2 Phase Acquisition

During phase acquisition the loop is acting correctly as a negative feedback control loop. The phase acquisition is described by the error response. To describe the transient and steady state response control terminology is followed. For a second order loop the damping ratio ($\zeta$), and natural frequency ($\omega_n$), are used. If $\zeta < 1$ the system is underdamped and overshoots the target. If $\zeta > 1$ the system is overdamped.

A damping ratio of $0.5$ minimizes the noise bandwidth for a given $v_n$ (constraint on the acceleration error). If the noise bandwidth is fixed, choosing $\zeta = 0.707$ will minimize the pull-in time, and a ratio of $0.81$ will maximize the frequency step the loop can handle without being pulled out of lock. Optimum damping ratios for these and other criteria are given by Gardner [11]. Moderate departure from these points does not radically affect loop performance. Most criteria are adequately met if $0.5 \leq \zeta \leq 1.14$.

If the loop is higher than second order, the root locus technique discussed later in this chapter can be used to predict the dominant second order response.
5.5.3 Acquisition Time

The total acquisition time can be broken into times for frequency and phase acquisition:

\[ t_{\text{acq}} = t_p + t_s + t_a, \]

where: 
- \( t_p \) - pull-in or cycle slipping time,
- \( t_s \) - phase slip time (s) and,
- \( t_a \) - phase acquisition time (s).

For initial frequencies well outside the lock-in range but inside the pull-in range, the acquisition time is dominated by cycle slipping. This is the time it takes to change from the initial frequency to the lock limit (within \( \pm K_m \) rad/s of the input frequency). It can be very long in narrowband loops.

An approximate pull-in time for a second order loop with a sinusoidal phase detector if \( |\omega_s - \omega_0| > > K_m \), is given by Gardner [11]:

\[ t_p = \frac{(\omega_s - \omega_0)^2 T_a}{K^2} = \frac{(\omega_s - \omega_0)^2}{2\omega_0^2} \]  

(5.14)

Equation (5.14) is a good conservative estimate for most phase detectors. If the initial frequency is not significantly outside the lock range the estimated pull-in time will be widely effected by the initial phase.

When the initial frequency is in the lock-in range, the frequency acquisition time can be dominated by the phase slip time. Phase slip occurs if the initial phases of the input and loop clock are such that the feedback is positive and the loop frequency is pushed away from lock. The phases must slip enough for the feedback to become negative. A slip of up to half the beat note period could be required. The time to slip into negative feedback will be bounded by:
\[ t_p = \frac{1}{2(f_s - f_i)} \]  \hspace{1cm} (5.15)

If the input and loop frequencies are close, this can take a very long time.

The phase acquisition time is determined by the settling time of the loop. In five time constants the loop will settle to within ± 0.7% of the final value. Using this definition:

\[ t_s = \frac{5}{5\omega_n} \]  \hspace{1cm} (5.16)

The fastest acquisition time occurs when the signal frequency is just inside the lock-in range. The wider this range the smaller that maximum phase slip time will be. Equation (5.14) shows the high frequency gain must be increased to increase the lock-in range. As will be seen in the filter discussion in section 6.3 a larger high frequency gain produces a larger natural frequency, \( \omega_n \). This will also reduce \( t_s \). The minimum bandwidth needed to achieve a specific maximum acquisition time can be calculated.

5.6 Root Locus Analysis

The root locus method is a graphical method of analyzing the stability and transient response of feedback control systems. It is applicable to a locked PLL and can give insight into the effects of the loop parameters on the loop performance. Most systems are basically second order systems. When the loop is of higher order the root locus plot can be very useful in determining the dominant second order response.

The root locus plot shows graphically how the roots of the
characteristic equation, 
\[ 1 + G(s)B(s) = 0, \quad (5.17) \]
are changed as parameters in the system changes. In the case of the PLL this can be rewritten:
\[ \frac{1 - K_w K_d P(s)}{s} = 0 \quad (5.18) \]

The closed loop roots for a specific value of loop gain \((K_w K_d)\) are found by solving equation \((5.18)\). A root locus is obtained by plotting the closed loop roots on the \(s\) plane as the loop gain is varied from zero to infinity. When the gain is zero, the closed loop roots will fall on the open loop poles. When the gain is infinite, the closed loop roots will fall on the open loop zeros. Thus all lines of increasing gain originate on an open loop pole and terminate on a zero.

Fig. 5.3 shows one closed loop pole of a complex-conjugate pole pair plotted on the \(s\) plane. The distance from the origin to the root indicates the natural frequency \((\omega_n)\) of the second order response. The vertical axis indicates the damped frequency \((\omega_d)\), and the cosine of the angle from the horizontal axis is the damping ratio \((\zeta)\). For gains that produce only roots in the left hand plane the system is stable. Gains that produce roots on the right hand side make the system unstable. Sensitivity to changes in gain is measured by the amount of movement in the closed loop poles as the gain is varied. Rules for sketching root locus are available in Dorf [17].

For repeated use or for a complex system a computer program is worthwhile. The program \((RLOCI)\) which is used in this thesis is presented in Van de Vegte [18] and was modified, by George Knopf, for use at the University of Saskatchewan.
Fig. 5.3 Second Order Root Location in the S Plane.

5.7 Summary

Although exact equations describing PLL operation are cumbersome (or not available), many suitable engineering approximations exist. These approximations along with control theory and root locus analysis provide a framework for PLL design.
6. LOOP COMPONENTS

A phase locked loop is comprised of three components, a phase detector, a loop filter and a VCO. These components are selected to achieve the loop design parameters. In other PLL applications such as FM modulation/demodulation and carrier recovery, all clock transitions are present, and it is not essential to have high gain loops. Unlike a carrier waveform, binary data does not have all transitions present. This restricts the choice of phase detector in a clock recovery PLL. Furthermore, a high dc loop gain is required to keep the mistuning phase error small. The gain of the loop is usually set by the choice of filter. The VCO criteria is essentially the same in a clock recovery circuit as for other PLL applications.

6.1 Phase Detectors

In a PLL, the phase detector produces an error signal proportional to the phase difference between the incoming signal and the loop clock. This is lowpass filtered to produce an average voltage that controls the VCO frequency.

The purpose of producing a clock at the receiver is to sample the incoming data bits. The preferred sampling time is at the center of each bit. If the loop has locked to a stable incoming frequency, the phase angle between the input data and the loop clock will be constant and the average output of the phase detector will also be constant. A phase difference of π radians (T/2) will place the clock in the middle of the data bit periods.
6.1.1 Properties of Phase Detectors

A random NRZI data stream has missing transitions, and does not have a spectral component at the clock frequency. If the phase detector requires a clock frequency component, the data stream must be processed to produce it. Missing transitions in the input are not easily replaced and the inability to handle them makes many phase detectors unsuitable for clock recovery from binary data. Other qualities to be examined when choosing a phase detector are, the phase detector characteristic, noise immunity, and ripple frequency of the output.

The phase detector characteristic is a plot of the average output voltage versus the phase difference of the input signals. From the characteristic, the center of the phase range (phase offset), the center of the voltage range (voltage offset), the linear range, and the gain can be determined. The three most common characteristics are sinusoidal, triangular, and sawtooth are pictured in Fig. 6.1.

The sinusoidal and triangular phase comparators have a phase offset of $\pi/2$ radians, and sawtooth phase comparators of $\pi$ radians. If a transition detector is included in the phase detector its delay will also affect the value of the total phase offset ($\theta_0$), and system stability. Usually the phase offset ($\theta_0$) is removed in analysis. Thus the phase error is given by:

$$\theta_\text{m} = \theta_1 - \theta_0 - \theta_\text{m}$$

$$= \theta_\text{m} - \theta_0$$

(6.1)

The linear region is $-\pi/2 \leq \theta_m \leq \pi/2$ for a triangular phase detector, and $-\pi \leq \theta_m \leq \pi$ for a sawtooth phase detector. The sinusoidal phase detector is considered linear for angles $\theta_m$ such that $\sin(\theta_m)=\theta_m$. If
loop components are not approximately linear over their active regions, analysis becomes difficult if not impossible. In high gain loops the active region is small so a constant phase detector gain is reasonable for calculations on the locked loop. Therefore, linearity and large phase ranges are not as important qualities in high gain clock recovery loops as they are in other applications.

The phase detector gain, $K_a$, is the slope of the characteristic and has units of volts/radians. If the characteristic is non-linear the gain is measured at the operating point.

The ability to handle additional transitions implies the phase detector has noise immunity. It does not indicate the phase detector can handle missing transitions. Transitions due to noise differ from
transitions in the received data, as they occur at unpredictable times and usually cause only a short level change.

The frequency of the ripple in the phase detector output can become important when the loop filter is active. The operational amplifier used in the filter may not handle high frequency inputs, and bandpass or lowpass ripple filters may be needed before the operational amplifier. The ripple filter must be included in the loop analysis if the cut-off frequency is not well removed from that of the loop filter. Therefore, if filtering is required, the higher the ripple frequency the easier it is to filter without affecting the loop response.

The offset voltage error \( (V_o) \) is the difference of the actual voltage offset from the expected voltage offset. It is measured with the input frequency set to the VCO center frequency. This voltage offset error causes a phase error because it is misinterpreted as phase information.

The offset phase error \( (\epsilon_o) \) is related to the offset voltage by the phase detector gain:

\[
\epsilon_o = K_o V_o
\]

(6.2)

If the dc offset voltage is significant, a null adjustment is needed.

6.1.2 Types of Phase Detectors

Phase detectors fall into three general categories. Multiplier circuits and sequential circuits have outputs whose averages produce analogue control signals. Digital circuits produce an output which is used as a discrete control signal.
Discrete or "true" digital phase detectors are used only in digital phase locked loops. The output from these phase detectors is a discrete number. The locally generated oscillator is restricted to discrete phase increments. For the loop to operate correctly the incoming signal must be sampled at greater than twice its bandwidth. In the case of 125 Mbps data the sampling rate would approach the limits of ECL and, therefore, the digital phase locked loop was not considered further.

6.1.2.1 Multiplier Phase Detectors

Multiplier phase detector circuits produce an average output proportional to the product of the two incoming signals. They are level activated circuits and do not respond to extra noise transitions. This gives them high noise immunity. These circuits have no memory.

All multiplier phase detectors require both the input and the reference signals to have a spectral component at the clock frequency. Received NRZI data can be processed to give a component at the clock frequency using non linear methods.

For each missing transition pulse, a multiplier detector outputs the VCO clock or the inverted VCO clock. Due to the symmetry of the clock the average output from the phase detector for one bit will be the voltage offset. This voltage corresponds to the center frequency of the VCO. The VCO continues to oscillate at the same frequency due to the low frequency response of the loop filter, but it will drift toward its free running frequency. Thus the multiplier phase detector has a flywheel effect.
Multiplier phase detectors utilize all the transitions in the received data. Therefore, the fraction of the time which they rely on the flywheel effect \( (F_{\text{mul}}) \) is given by:

\[
F_{\text{mul}} = 1 - p_e.
\]  

(6.3)

This result holds for correlated and uncorrelated transitions. The effect can be incorporated into the phase detector characteristic by multiplying \( K_e \) by \( p_e \), yielding a new phase detector gain, \( K_{ae} \).

If both inputs are square waves the phase characteristic will be triangular and the phase offset is \( N/2 \). The effect of one asymmetric input is to cause a shift in the phase offset and to limit the peaks resulting in a trapezoidal characteristic. If both inputs are asymmetric, these limiting zones become unequal and the phase offset is again shifted. The phase detector gain is unaffected by the duty cycle of the input signals. Fig. 6.2 shows the phase characteristic for each of these cases. For symmetric inputs both signals have pulse widths of \( T/2 \), for one asymmetric input the clock width is \( T/2 \) and the input signal pulse width \( T/4 \), and for two asymmetric inputs the clock width is \( 3T/8 \) and the input signal pulse width \( T/4 \).

Several problems arise with asymmetric inputs. The shift in phase offset can be compensated, if the duty cycle of each input is known. However, the output of the phase detector (without an input signal) will have the duty cycle of the clock. If the VCO clock is asymmetric, the average output voltage will not maintain the VCO's center frequency. Thus, the flywheel effect will not work properly. The unequal limiting zones caused by two asymmetric inputs will cause a dc offset voltage during cycle slipping. This can either aid or hinder
Fig. 6.2 XOR Phase Detector Characteristic With Asymmetric Inputs.
frequency acquisition. Halgren, Harvey and Peterson [15] suggest acquisition will not be unduly effected if each input is within 8% of the desired half bit width. The limiting zones will not affect the operation of the loop if the loop is already locked or does not cycle slip during acquisition.

Multiplier phase comparators are usually implemented using switching circuits. These give a close approximation to a true multiplier. Most commonly used are double balanced diode mixers and XOR gates.

The exclusive-or gate is a digital integrated circuit, and is easily included in larger digital designs. A 'sample' of the phase difference is taken at the zero crossings of the waveforms. Although not included in this thesis, a precise analysis of loop dynamics should include the one half bit delay of this process plus the propagation delay through the device.

The best results are produced when both the input and the clock signals are rectangular. When the loop is locked the output is a pulse train. It has the period of the half the incoming data stream period and a duty cycle proportional to the phase difference ($\Theta_d$). Thus, when the input frequency is close to $f_0$, there is a ripple component at approximately twice the data frequency.

The XOR phase detector characteristic is a function of the probability of data transitions ($p_e$), the rise and fall times of the gate, and the duty cycle of each input. The range of input frequencies is limited by the logic speed. For infinitely fast rise and fall times and a 50% duty cycle for both inputs, the familiar triangular
characteristic is obtained.

A double balanced mixer uses four diodes to produce the switching action. The advantages of a double balanced mixer are: isolation between the reference signal, the input signal and the output signal, and low dc offset. As the inputs are transformer coupled, the output will be affected if the input is not dc balanced.

Double balanced mixers are available for use with inputs up to the microwave frequencies. They accept either rectangular or sinusoidal inputs and have phase characteristics which are triangular and sinusoidal respectively.

6.1.2.2 Sequential Phase Detectors

A sequential phase detector produces an output proportional to the average time interval between the zero crossings of the two input signals. A precise analysis of the loop dynamics should include the one bit delay of this sampling process. These circuits have memory of past transitions, and most implementations are intolerant of missing or extra transitions. They are usually implemented using digital integrated circuits and operate best on signals with rapid rise and fall times. They produce an analogue output and are not "true digital" phase detectors.

The characteristic of most sequential phase detectors is sawtooth. Sequential phase detectors are transition activated and they are not affected by other characteristics of the waveforms such as pulse duration. Thus, asymmetric input signals do not change the phase characteristic. Sequential phase detectors do not require the input
signal spectrum to have power at the clock frequency. However, transition encoding will produce positive transitions at both the positive and negative transitions in the data signal. The output is a rectangular wave at the signal frequency with a duty cycle dependent on the phase error. When the input frequency is near $f_o$, the ripple frequency is at approximately the data rate.

A single R-S flip-flop is the simplest form of sequential phase detector. Incoming signal transitions set the output high, and the VCO clock resets it low. This implementation is not suitable for data streams since missing transitions produce a high or low voltage that is one bit long. For the flywheel effect to work properly the average output for missing transitions must be close to the offset voltage.

A toggled sequential phase detector can be obtained by the circuits in Fig. 6.3. In both of these circuits the output is set high by a data transition and toggled by a clock transition. The set function in Fig. 6.3a is level active. Thus, if a clock transition occurs during a data transition pulse it will be ignored. In the circuit in Fig. 6.3b both the data and the clock inputs edge active.

If a data transition is missing the next clock transition will toggle the output high. Regardless of whether a data transition occurs, the output will stay high until the next clock transition. After it is reset low, the circuit will once again respond normally to data transitions. Thus, for every missing data transition, the output is high for one bit and low for one bit period giving an average of the offset voltage.

The flywheel action works correctly since the transition that
Fig. 6.3 Toggled Sequential Phase Detectors;
a) Level Active Circuit; b) Edge Active Circuit.
immediately follows the missing transition is not utilized. Thus, the
time spent on flywheel is greater than for the multiplier phase
detector. For random transition data, with uncorrelated transitions,
the fraction of time that the loop operates on flywheel $F_{\text{sto}}$ is:

$$F_{\text{sto}} = 2p_e^2q_e + 2p_e^2q_e^2 + 4p_e^2q_e^3 + 4p_e^2q_e^4 \ldots$$

$$= 2p_e^2\left( \sum_{n=0}^{\infty} \frac{n(q_e^n)}{q_e} + \sum_{n=0}^{\infty} n(q_e^n)q_e \right)$$

where $q_e = 1-p_e$ \hspace{1cm} (6.4)

Using the series solution:

$$\sum_{n=0}^{\infty} nx^n = \frac{x}{(1-x)^2}$$ \hspace{1cm} (6.5)

Substituting (6.5) into (6.4), and simplifying:

$$F_{\text{sto}} = \frac{1-2p_e}{1-p_e}$$ \hspace{1cm} (6.6)

The toggled sequential phase detector has a frequency
discriminator characteristic. If the data rate is higher than the clock
frequency the probability that no transitions occur between clock
pulses is reduced, and $V_o$ increases. This tends to push the clock
frequency higher and thus closer to lock. Similarly $V_o$ decreases when
the data rate is decreased.

The different delays in the two signal paths can cause a negative
slope region on the phase detector characteristic. This causes an
offset voltage that hinders acquisition. The effect is similar to flat
spots in the XOR phase detector characteristic. The sections of
variable delay line allow the two path delays to be equalized. To
again insure the acquisition time is not unduly affected, the path
delay difference should be less than 0.16XT [15].
The phase-frequency detector is another sequential phase detector implementation. It is unique, as when the loop is out of lock, the control signal indicates the direction of the error and provides automatic sweep frequency acquisition. It is unfortunately unsuitable for data applications since the frequency is not maintained when transitions are missing.

6.1.3 Comparison of XOR Multiplier and Toggled Sequential Phase Detectors

In clock recovery, the phase detector should use all incoming clock information. The sequential detector ignores much of this information as indicated by its flywheel fraction. The flywheel fraction versus the probability of transition is plotted for both phase detectors in Fig. 6.4. The transitions were assumed uncorrelated. These results were experimentally confirmed using pseudo-random data of length 255. For random transition pulses with \( p_e = 0.5 \) (\( F_{\text{mul}} = 1/2 \), \( F_{\text{seq}} = 2/3 \)), the multiplier phase detector relies on the flywheel effect half the time but the sequential circuit relies on it two thirds of the time.

For FDDI encoded data if all codes are random and equiprobable, \( F_{\text{mul}} = 1-p_e = 0.39 \), and \( F_{\text{seq}} = 0.61 \) . This means the sequential phase detector will use the flywheel effect 61% of the time. It will ignore 1/3 of the available transitions, and thus 1/3 the clock information provided by the data encoding. In this calculation the correlation of the transitions was included.

In the sequential phase detector, the effect of unequal path
Fig. 6.4 Flywheel Fraction Versus Probability of a Pulse.
delays can either aid or oppose acquisition during cycle slipping. To have negligible effect at 125 MHz, the paths may differ by up to 12.8 ps. This is virtually impossible to achieve as the propagation delay of the gates vary as much as 1.7 ns. The amount of aid from the frequency discriminator characteristic of a sequential phase detector is relatively small, and in this case is easily swamped by the effect of different delay paths. Acquisition during cycle slipping with multiplier phase detectors is affected if both inputs are asymmetric. The adjustment need only be within 8%. This effect is unimportant if cycle slipping is avoided.

The sequential phase detector is less affected by the logic rise and fall times as it switches at half the frequency of the XOR phase detector. If the ripple must be filtered, the higher ripple frequency from the XOR detector is preferable.

In overview, the major disadvantage of the sequential phase detector is poor utilization of clock information. The XOR phase detector was chosen for use in this study. Details of the design are discussed in Section 7.3.1.

6.2 Voltage Controlled Oscillators

The voltage controlled oscillator adjusts its output frequency according to the control voltage. It is considered to be a perfect integrator as discussed in Chapter 5.

6.2.1 Properties of VCO Circuits

The important features of a VCO are: electrical tuning range
(frequency deviation), modulation bandwidth, phase and frequency stability, gain \(K_o\), and linearity of frequency versus control voltage.

The electric tuning range is the range of output frequencies that can be obtained from the VCO by adjusting the control voltage. Usually, the tuning range is centered around the "center frequency". The range is often given as a percentage or fraction of the center frequency. The tuning range must be larger than the range of incoming frequency to allow for a mistuned center frequency. There should also be enough range to allow for overshoot in response to a step phase change or during acquisition. The amount required depends on the loop damping factor. For a damping ratio of 0.707 a buffer of 30% of the incoming signal is recommended [16].

As will be discussed in chapter 7, a much larger tuning range may be used to obtain a fast acquisition time.

The Gain or sensitivity is the slope of the frequency versus control voltage plot. The gain must be large enough to produce the desired frequency range with the range of control voltages available from the filter or gain block.

Linearity is a constant gain or slope over the VCO's frequency range. In some PLL applications linearity is essential. In clock recovery the loop will operate correctly with a non-linear VCO, but the loop equation will be much more difficult to solve.

The modulation bandwidth indicates how quickly the frequency can be changed. Frequency control is obtained by using voltage or current to change the value of a component in the oscillation circuit. The time
delay in varying the tuning element stops the circuit from reacting to high frequency signals. The modulation bandwidth (or 3 dB point) is the frequency at which the effect of the control signal is attenuated by 0.707.

**Phase and frequency stability** are measures of short and long term deviations in the VCO output. Phase noise or jitter can be caused by white noise and non-linear oscillator circuit elements. Causes for frequency drift are thermal effects and aging.

6.2.2 Types of VCO Circuits

Common types of VCO's include crystal oscillators (VCXO), LC oscillators, RC multivibrators and, YIG tuned oscillators.

Quartz crystal oscillators are the most common crystal oscillators. They tend to have a very high Q, but narrow tuning range. Extreme limits of the tuning range are in the order of 0.25 to 0.5% of the center frequency. The cut and dimensions of the crystal determine its oscillating frequency. Fundamental frequencies from 1 kHz to 25 MHz are common. Crystals with higher fundamental frequencies become fragile, but by using 3rd, 5th, 7th and 9th harmonics, oscillation frequencies up to 500 MHz can be obtained.

Crystal oscillators are usually tuned with a voltage controlled capacitor or varactor. The modulation bandwidth is determined by the rate the tuning capacitance can be changed. The quality of the entire circuit is determined by both the quality of the crystal and the tuning circuit. If a wide modulation bandwidth is required the tuning circuitry will dominate the circuit Q. In this case, similar circuit
qualities may be obtainable more cheaply without using a crystal.

**LC Oscillators** are built around resonant LC circuits. They have a wider tuning range than crystal oscillators and can be built for a wide range of center frequencies at low cost. Frequency control is usually by varactor and the modulation bandwidth is again determined by the rate its capacitance can be changed. Integrated oscillator circuits are available which can be customized to the correct frequency by the addition of an external LC circuit. These chips are available with ECL power supplies and output levels.

The frequency of a **RC multivibrator** is determined by a RC time constant. Frequency control is obtained by varying the effective resistance of a FET transistor. The output waveform is a square wave. RC multivibrators are available cheaply in IC form. They generally are used under 100 MHz. The Motorola MC1658 operates up to about 130 MHz.

**YIG (Yttrium Iron Garnet) oscillators** are used at microwave frequencies. They can be slowly tuned by changing the surrounding magnetic field. Their tuning range is large and linear but they have considerable phase noise [17].

6.2.3 Oscillator Implementation

To obtain fast acquisition time, the oscillator needs a wide modulation bandwidth and tuning range. The MC1648 voltage-controlled oscillator chip was chosen. An external LC circuit determines the center oscillating frequency. One component in the tuned circuit is a varactor, which allows the electrical tuning of the VCO. Details of the design are discussed in chapter 7.
6.3 Loop Filter

Once the type of phase detector and VCO have been fixed their parameters are not widely adjustable. The design of the filter is more flexible. Most PLL are second order and use lead-lag filters. They can be simply implemented in either a passive or active configuration and, allow the bandwidth, damping and dc gain to be independently set. Fig. 6.5 shows two common configurations. Fig. 6.6 shows a Bode plot for the lead-lag filter.

6.3.1 Passive Filters

A passive second order lead-lag filter is shown in Fig. 6.5a. Its transfer function is given by,

\[ P_p(s) = \frac{SCR_2+1}{SC(R_1+R_2)+1} = \frac{sT_2+1}{sT_1+1} \]  

(6.7)

where: \( T_1 = (R_1+R_2)C \) and, \( T_2 = R_2C \).

The closed loop transfer function for a basic loop containing this filter is:

\[ T_p(s) = \frac{K_0K_a(sT_2+1)/T_1}{s^2 + s(1+K_aK_qT_2)/T_1 + K_aK_q/T_1} \]  

(6.8)

This gives a natural frequency, damping factor and, high frequency gain of:

\[ \omega_n = (K_aK_0A/T_1)^{1/2} \]  

(6.9)

\[ \zeta = 0.5\left(\frac{AK_aK_q}{T_1}\right)^{1/2} \left(\frac{1}{AK_aK_q}\right) \]  

(6.10)

\[ K_m = \frac{K_aK_qT_2}{T_1} \]  

(6.11)

The noise bandwidth \( B_L \) for the passive lead-lag filter is given by:
Fig 6.5 Lead-Lag Filters: (a) Passive Filter; (b) Active Filter.

Fig. 6.6 Bode Plot for a Lead-Lag Filter.
The gain of a loop using a passive filter can be increased by adding a gain block, \( G \). The passive filter loop equations must now be modified by replacing \( K_a K_d \) by \( K_a K_d G \). To obtain the same \( \omega_n, T_1 \) must be much larger, and it may be difficult to obtain suitable component values. The amplifier gain in the passive filter will effect damping and the natural frequency and must be kept within tolerance.

### 6.3.2 Active Filters

An active second order lead-lag filter is shown in Fig. 6.5b. Its transfer function is:

\[
F_a(s) = \frac{-A(sCR_2+1)}{sCR_2+1+(1+A)sCR_1} \tag{6.13}
\]

where: \( A = \) amplifier dc open loop gain

For a large amplifier gain \( A \), this transfer function becomes:

\[
F_a(s) = -\left(\frac{sCR_2+1}{sCR_1}\right) = -\left(\frac{sT_2+1}{sT_1}\right) \tag{6.14}
\]

where, \( T_1 = R_1 C \) and, \( T_2 = R_2 C \).

The closed loop transfer function of the entire loop will then be:

\[
T_a(s) = \frac{K_a K_d (sT_2+1)/T_1}{s^2 + s(K_a K_d T_2/T_1) + K_a K_d/T_1} \tag{6.15}
\]

The natural frequency, damping factor and, high frequency gain are:

\[
\omega_n = (K_a K_d/T_1)^{0.5}, \tag{6.16}
\]

\[
\zeta = \frac{T_2 (K_a K_d/T_1)^{1/2}}{2} = \frac{T_2 \omega_n}{2} \quad \text{and,} \tag{6.17}
\]

\[
K_m = \frac{K_a K_d T_2}{T_1} \tag{6.18}
\]

In an active filter the gain \( A \) only needs to be above a minimum
level to insure design parameters are met.

The noise bandwidth for the active lead-lag filter is [12]:

$$B_L = \frac{K_m (1+s \tau)}{4 K_m} = \frac{\omega_m (\frac{\tau}{2} + \frac{1}{2\tau})}{(\text{Hz})} \quad (6.19)$$

The use of the operational amplifier requires some precautions. An operational amplifier may not handle high frequency signals. Ripple filters placed before the op-amp can reduce the high frequency component. The positive and negative slew rates are not necessarily matched and this causes a dc error which may aid or oppose acquisition during cycle slipping. The operational amplifier must be chosen to avoid slew limiting for beat notes that may be encountered. Ripple filters placed before the op-amp can reduce these effects.

The gain-frequency bandwidth of the op-amp should be much greater than the loop bandwidth. If this is not the case, loop analysis must include all significant op-amp poles. A passive filter will be necessary if the loop bandwidth is greater than the unity gain bandwidth of the op-amp.

The magnitude of the mistuning phase error depends on the dc loop gain and the difference between the incoming frequency and the VCO center frequency. The mistuning phase error adjusts the average output voltage. This changes the VCO from its center frequency to the incoming frequency. If the dc gain of the loop is high, very little phase shift is needed to adjust the frequency. The phase relationship of the clock to the data remains almost constant. Thus, high gain clock recovery loops keep the sampling point close to the center of the bit. This is a result of the loop being approximately type II. Other advantages in tracking of a type II loop are discussed in chapter 5.
In a high gain loop without an input signal, the loop clock will eventually reach one of the limits of the VCO frequency range. This is because the reference voltage can not be set to the accuracy required by the gain. This is not a problem in FDDI as a recovered clock signal is not required when the input is unavailable.

An active, second order lead-lag filter was chosen for implementation. It is based on the TL082 operational amplifier. It is followed by a video amplifier gain block which provides additional high frequency gain. Design details and the determination of time constants is discussed in section 7.3.3.

6.4 Summary

The PLL application determines which qualities are important in its components. For each of the components there are a number of options available. In the FDDI clock recovery circuit, a XOR based phase detector, an LC voltage controlled oscillator, and an active lead-lag filter were chosen.
7. Design of a PLL Clock Recovery Circuit For FDDI

7.1 Requirements

FDDI specifies the clock is to be acquired in less than 10 μs. The clock recovery circuit must lock and hold for all frequencies in the range 125MHz ±0.005% (50ppm) as this is the accuracy of the transmitting clock. During acquisition the IDLE symbol will be sent. When transmitted, this is an on-off pattern with all transitions present. Synchronization is not required during HALT symbols, QUIET symbols, or alternating HALT and QUIET symbols. These symbols indicate the physical link between the adjacent stations is disabled [4].

The jitter in the recovered clock should not cause bits to be sampled in error. No specific measurements of clock jitter are given in the specifications but upper boundaries have been inferred in chapter 4.

7.2 Design Steps

From the performance specifications, the loop parameters of gain and bandwidth can be determined. Achieving these parameters requires the design of the VCO, phase detector, and filter to be interrelated. General designs for these components were chosen in chapter 6. The predicted performance and limitations of these general designs and the loop performance specifications are used to determine the specific component designs. The steps in finalizing the designs follow.

Step 1) All excess poles were assumed to have negligible affect on the loop operation. Initial calculations were therefore based on second
order loop equations.

Step 2) A type II second order loop was chosen. This gives high dc gain, and independent control of the bandwidth and damping ratio.

Step 3) The loop was designed so no cycle slipping would occur. This helps meet the fast specified acquisition time. The acquisition time is composed of the phase slip time \( t_a \) and the phase acquisition time \( t_a \). Substituting equations (5.15) and (5.16) yields:

\[
t_{acq} = t_a + t_a = \frac{1}{2|f_1-f_o|} + \frac{5}{\zeta \omega_n} \tag{7.1}
\]

The phase slip time is reduced by making \( |f_1-f_o| \) large. For equation (7.1) to apply, the input frequency must be in the lock range. Thus, by equation (5.12), the high frequency gain must be:

\[
K_m \geq 2\pi|f_1-f_o| \tag{7.2}
\]

Using equation (6.18) for the high frequency gain \( K_m \) of an active lead-lag filter:

\[
2\pi \omega_n \geq 2\pi|f_1-f_o| \tag{7.3}
\]

Step 4) The active filter has an almost infinite dc gain. This insures the VCO free running frequency will be either the high or low extremity of its frequency range.

To minimize phase slip time the initial frequency difference must be the maximum possible in the pull-in range. If the two sides of equation (7.3) are assumed equal, equation (7.1) for acquisition time can be rewritten in terms of \( |f_1-f_o| \):

\[
t_{acq} \leq \frac{1}{2|f_1-f_o|} + \frac{5}{\pi|f_1-f_o|} \tag{7.4}
\]

Setting \( t_{acq}=10\mu s \), a reasonable minimum frequency difference can be found:
\[ |f_1 - f_0| > 209.2 \text{ kHz}. \] (7.5)

The frequency of transmitting clock \( f_1 \) is 125 MHz ±0.005%. Thus it can vary by ±6.3 kHz. The VCO range must be enlarged by this amount to insure the minimum initial frequency difference:

\[ R_L > R_{\text{VCO}} > (209.2 + 6.3) \text{ KHz} > 215.5 \text{ KHz}. \] (7.6)

To allow for inaccuracy in mechanically tuning the center of the VCO range to exactly 125 MHz and any drift due to temperature or aging the VCO range should be larger than this minimum value. In the VCO design of section 7.3.2 the frequency range obtained is 460 kHz. If correctly centered this will produce \( R_{\text{VCO}} = 230 \text{ kHz}. \)

Step 5) Substituting the value of \( |f_1 - f_0| = 230 \text{ kHz} \) back into equation (7.3) the bandwidth required for pull-in can be calculated. A damping ratio of 0.707 was used, as this produces the fastest acquisition time for a fixed noise bandwidth [11]. Thus:

\[ \omega_n > 1.022 \text{ (Mrad/s)}. \] (7.7)

To cause negligible phase shift, the poles of the operational amplifier in the active filter should be at least a decade away from \( \omega_n \) (in this case greater than 10.2 Mrad/s or 1.6 MHz). The TL082 operational amplifier has typical unity gain bandwidth of 3 MHz. If the high frequency gain of the filter is unity, the pole due to the finite open loop gain of the operational amplifier will appear at 3 MHz. This operational amplifier can not both produce substantially larger high frequency gain and have this pole remain at a frequency higher than 1.6 MHz.

The time constants \((T_1, T_2)\) for unity high frequency gain are equal. Thus, \( R_1 \) and \( R_2 \) are also equal. The values of \( R_1, R_2 \) and \( C \) were
chosen using (6.14). The value of capacitance was chosen as 1.0 nF and 
\( R_1 = R_2 = 1.0 \text{k} \Omega \). Using equation (6.16) these values give:

\[
\omega_n = 1.414 \text{ (Mrad/s)}
\]  
(7.8)

This larger natural frequency will reduce the phase acquisition
time, resulting in a total acquisition time of less than 10 \( \mu \text{s} \). The 3
MHz unity gain bandwidth of the TL082 should still be sufficient, as
poles above 2.25 MHz (14.14 Mrad/s) should have little effect.

Additional high frequency gain was obtained with the Motorola
MC1733 Video Amplifier. The output of the video amplifier has a swing
of 4 \( V_{p-p} \). Its gain is adjustable from 10 to 400 (V/V), and its
bandwidth is typically 120 MHz. The pole due to the video amplifier
bandwidth has negligible effect.

Step 6) The electrical tuning range available to the VCO is the 4
V swing obtained at the output of the video amplifier (gain block). For
the VCO frequency range of approximately \( \pm 230 \text{ KHz} \), the VCO gain should
be:

\[
K_o = \frac{R_{\text{VCO}}}{V_{\text{max}} - V_{\text{min}}} = \frac{460(2\pi)}{4} = 723 \text{ (krad/V)}.
\]  
(7.9)

It is desired to achieve this gain with a high VCO quality and a
large modulation bandwidth. A modulation bandwidth of greater than 2.25
MHz should have negligible effect on the loop performance. Quality and
modulation bandwidth are discussed further in the VCO design section
7.3.2.

The value of VCO gain was measured in section 7.3.2 to be:

\[
K_o = 707 \text{ (krad/V)}.
\]  
(7.10)

Step 7) The phase detector has been chosen as an ECL XOR gate.
Using ECL logic levels of \( V_H = -0.8 \text{V} \) and \( V_L = -1.8 \text{V} \). The gain of the phase
detector is calculated as:

\[ K_d = \frac{V_m - V_L}{n} = \frac{-0.8 - (-1.8)}{n} = 0.318 \text{ (V/rad)}. \]  

(7.11)

The actual gain of the phase detector will depend on the number of transitions present. A modified gain factor can be obtained by multiplying the gain with all transitions present by the probability of transition. The measured gain with all transitions present was:

\[ K_d = 0.32 \text{ (V/rad)}. \]  

(7.12)

Step 8) The required gain (G) from the video amplifier was calculated by replacing \( K_d \) in equation (6.17) by \( G K_d \), and solving for G.

\[ G = \frac{\omega_2 T_1}{K_d K_o} = \frac{\omega_2 R_c C}{K_o K_d} \]

\[ = \frac{(1.414 M)^2(1.0 k)(1.0 n)}{707k(0.32)} = 8.84 \text{ (V/V)}. \]

(7.13)

This is the gain required during acquisition. At this time \( p_e = 1 \) and is not included in the calculation. Changing the value of the gain, until a damping ratio of \( \xi = 0.707 \) was obtained, resulted in:

\[ G = 8.75 \text{ (V/V)}. \]

(7.14)

Step 9) The gains and poles were measured or calculated from the component designs. They were entered into a root locus program to ensure the assumption made in step 1 was reasonable.

Step 10) Adjustments for incorrect assumptions and new limitations due to finalized component design were made.

7.3 Component Implementation and Testing

Each of the PLL components was designed to meet or exceed the criteria found in steps 1 through 8. The components were built and the
important parameters measured. The circuit diagram of the final PLL design appears in Fig. 7.1. The component designs, the tests performed, and their results, are presented below. The root locus based on the final loop values and the loop performance tests are discussed in chapter 8.

7.3.1 Phase Detector

The phase detector must operate at 125 MHz and handle missing transitions. The circuit, shown in Fig. 7.1, includes a buffer gate to square the incoming waveforms.

The conversion of incoming full width NRZI data stream into transition pulses is achieved by an XOR gate with the data and the delayed data as inputs. The clock power is proportional to the surrounding continuous power for any delay length. A delay of half a bit period produces the maximum absolute output power at the clock frequency in the transition detector.

Keeping close to the half bit delay does allow the XOR phase detector more time to respond. This is important as the rise and fall times of the IC are significant. Using Fairchild F100L ECL, the 20-80% rise and fall times were approximately 0.7 ns.

The half bit delay was implemented with a length of coaxial cable. The length was determined by the velocity of propagation in the coaxial line. For RG-580 the propagation velocity is 66% of the speed of light: 

\[ V_p = 66\% (3\times10^8) = 0.198 \text{ m/ns.} \]  

(7.15)

The length is given by multiplying the velocity of propagation by the desired delay:
Fig. 7.1 Circuit Diagram of the Clock Recovery PLL.
\[ L = V_p T_d = (0.198 \text{ m/ns})(4.0 \text{ ns}) = 0.792 \text{ m}. \] (7.16)

Fig. 7.2 is a plot produced by the HP 54110D digitizing oscilloscope. The upper traces show the inputs to the transition encoder with 79 cm delay line. The lower trace shows the resulting output transition pulse. The delay measured at -1.3 V was 4.3 ns and the transition pulse width was 4.0 ns.

The phase characteristic was measured with the phase detector in loop. The loop filter reference voltage was varied from -1.8 V to -0.8 V. The data input was viewed before transition detection and the clock at the input of the phase comparator. Thus, the phase relationship includes all the delays in the phase detector not just those of the comparator. The results for an input square wave \((p_t=1)\) and pseudo-random data of length 255 \((p_t=0.5)\) are shown in Fig. 7.3. The plot is inverted to display the information in the standard phase detector characteristic form.

The slope of this graph is the phase detector gain. It was 0.32 V/rad with all transitions present. This is close to 0.318 V/rad, predicted in equation (7.11). With \(p_t=0.5\) the gain is 0.15 V/rad, which is, as expected, approximately half of the previous measurement.

When pseudo-random data is sent, the optimum reference voltage can be determined by observing the control voltage. When the control voltage ripple is minimum it indicates little frequency drift occurs when using the flywheel effect. This reference voltage was found to be -1.27 V. This is approximately where the characteristic with all transition present crosses that with \(p_t=0.5\).
Fig. 7.2 Transition Detector Output.

Ch. 1 = 320.0 mV/Div
Ch. 2 = 320.0 mV/Div
Timebase = 5.00 nsec/Div
Offset = -1.300 volts
Offset = -1.500 volts
Delay = 0.00000 sec

Trigger mode: Edge
On Pos. Edge on Chan 1
Trigger Levels
Chan 1 = -1.300 volts
Holdoff = 70.000 nsecs
Fig. 7.3 Measured Phase Detector Characteristic.
7.3.2 VCO

The VCO circuit is shown in Fig. 7.1. It is based on the MC1648 VCO chip. An XNOR ECL gate is used to square the output clock waveform. The oscillation frequency is determined by an external LC tank circuit. The tank circuit consists of an external inductance, electrically adjustable external capacitance, and internal chip capacitance. The inductor is one turn of #30 magnet wire on a Cambion 534-3603-02-00-00 coil form. It has a moveable core that mechanically adjusts its inductance. Its value was in the 30 nH range, but was not precisely measured. The internal capacitance of the VCO chip is 6 pF. A parallel 48 pF chip capacitor was added to produce the approximate desired frequency.

A Siemens BB505B varactor was used to produce an electrically variable capacitance. Its capacitance is determined by the reverse voltage across it. The 1648 VCO chip produces a -3.2 V at pin 12, and the control voltage from the video amplifier ranges from 0.6 to 4.7 V. Thus, the reverse bias will range from 3.8 V to 7.9 V. With this range of reverse bias voltages the capacitance will vary from approximately 9 pF to 6 pF. A chip capacitance was placed in series with the varactor to limit the frequency range of the VCO. The VCO frequency is determined by:

\[
 f_0 = \frac{1}{2\pi \sqrt{L \left( C_o C_v + C_p + C_a \right)}}^{1/2}.
\]  

(7.17)

The value \( C_a = 3.3 \) pF gave a tuning range of \( R_{\text{VCO}} = \pm 230 \) kHz.

The resistor \( R_a \) is necessary to avoid loading the video amplifier and to keep the quality of the VCO circuit high. Without this
resistance the low output impedance of the video amplifier would virtually produce a short across \( C_m \). The quality of the tank circuit can be calculated by:

\[
Q = \frac{\omega_0 CR}{\omega_0(C + C_m + C_v + C_C + C_A)(R_A Q_a^2)}
\]

(7.18)

where, \( C_A = \frac{C_m(Q_a^2 + 1)}{Q_a^2} \), \( R_A = \frac{R_p}{Q_a^2 + 1} \), \( Q_A = \frac{C_v + C_A}{\omega_0 C_v C_AR_A} \), and \( Q_b = \frac{C_v + C_A}{\omega_0 C_v C_AR_A} \).

To change the reverse bias across the tuning varactor, \( C_v \) and \( C_m \) must discharge through \( R_p \). Thus, the modulation bandwidth becomes:

\[
\text{Modulation bandwidth} = \frac{1}{(C_v + C_m)R_p}
\]

(7.19)

Therefore, choosing the size of \( R_p \) is a tradeoff between large modulation bandwidth and VCO quality. For the values used in the final design \( (C_m = 3.3 \text{ pF}, 6 \text{ pF} \leq C_v \leq 9 \text{ pF}, C_{\text{CHP}} = 6 \text{ pF}, C_p = 48 \text{ pF}, L = 30 \text{ nH}, R_p = 2.4k\Omega) \), the quality and modulation bandwidth are:

\[
Q = 220, \quad \text{and} \quad \text{Modulation bandwidth} = 33.8 \text{ Mrad/s} = 5.4 \text{ MHz}.
\]

(7.20) (7.21)

For simplicity, the effective resistance of the varactor was not included in this calculation. Including the varactor resistance would reduce \( Q_A \) by approximately 5%.

The VCO frequency range was measured in loop by adjusting \( V_{ref} \) to push the video amplifier to its maximum and minimum output voltages. The upper frequency was 125.220 MHz and the lower frequency 124.760 MHz. The voltage versus frequency plot was measured by cutting the loop between the video amplifier and the VCO input. An external dc voltage was applied and the output frequency was measured. The plot is given in Fig. 7.4. The gain of the VCO is 707 krad/s. This is close to the
Fig. 7.4 Measured VCO Characteristic.
value calculated in step 6.

The modulation bandwidth can be measured by determining the output deviation ratio for input sinusoids of various frequencies. The deviation ratio $\rho$, is given by:

$$\rho = \frac{A_mK_o}{\omega_m}$$  \hspace{1cm} (7.22)

where: $A_m$ = peak amplitude of input sinusoid (V),
$K_o$ = gain of VCO, and
$\omega_m$ = frequency of input sinusoid (rad/s).

When the control signal is modulated by a sinusoid, the output of the VCO will have an FM spectrum described by $J_n(\rho)$ (an nth order Bessel function of the first kind). By comparing the ratio of spectral amplitudes to values in Bessel function tables, the measured value of $\rho$ can be found. The modulation bandwidth is the frequency at which the measured $\rho$ is 3 dB less than the calculated value.

When attempting to measure the modulation bandwidth the amplitude of the input sinusoid was kept within the VCO operating range ($A_m<2$ V). Before the modulation bandwidth was reached the value of $\rho$ became too small for accurate measurements. It was confirmed that the bandwidth was greater than 2.8 MHz.

7.3.3 Loop Filter

The loop filter is shown in Fig. 7.1. A TL082 operational amplifier was used in the active filter. It has a unity gain-bandwidth product of 3 MHz. The operational amplifier bandwidth should be much greater than the loop or the loop will be higher than second order and potentially unstable. The filter is designed to have unity high frequency gain. Thus, the operational amplifier contributes an extra
pole at 3 MHz.

The values for R1, R2, and C were chosen to produce a bandwidth slightly greater than the value needed for pull-in as discussed in step 5. The final values were:

\[ R_1 = R_2 = 1.0 \, \text{(kA)} \quad \text{and} \quad C = 1.0 \, \text{(nF)} \] (7.23)

The high frequency gain was achieved by using the MC1733 differential video wide-band amplifier. This amplifier has a typical bandwidth of 125 MHz and can be adjusted to yield gains from 10 to 400. Adjusting \( R_p = 1.3 \, \text{kA} \), resulted in \( G = 8.75 \). The input voltage range is only \( \pm 1 \text{V} \). In the op-amp feedback path IN914 signal diodes limit the filter output voltage to \( \pm 0.5 \text{V} \).

The voltage divider potentiometer provides a reference voltage for both the op-amp filter and video amplifier gain block. Its nominal setting is \( -1.3 \text{Vdc} \) which is the average output value of ECL. In section 7.3.2, it was discovered that \( -1.27 \text{Vdc} \) was optimum.

The video amplifier output has an offset of about \( 1.5 \text{Vdc} \). It comprises some of the dc offset needed to properly reverse bias the varactor in the VCO circuit. The video amplifier load impedance (VCO input impedance) was made greater than \( 1 \text{kA} \) for all frequencies up to 2 MHz. This was achieved by making \( R_p \) of the VCO circuit greater than \( 1 \text{kA} \).

In response to concern about inadequate filtering of the 250 MHz ripple, a passive ripple filter was inserted before the active filter. It did not cause a noticeable improvement and was removed.

The frequency response of the filter and gain block is shown in Fig. 7.5. It was measured with the filter removed from the loop. The dc
Fig. 7.5 Measured Filter Frequency Response.
gain of the filter was spoiled by adding a 100 kΩ resistor in parallel to the feedback path. Thus, the dc offset of the variable frequency input sinusoid could be set to avoid unequal clipping by the feedback diodes. The output of the video amplifier was fed into the ac coupled channel 2 of a Tektronix the 754A oscilloscope. This provides a high impedance load for the video amplifier and removed any dc component before the spectrum analyzer. The vertical channel 2 signal, available at the back of the oscilloscope, was fed into the 50 Ω input of HP8557A Spectrum Analyzer. The low frequency distortion in Fig.7.5 is due to the dc characteristic of the spectrum analyzer.

Achieving the high frequency gain with an amplifier separate from the filter, was necessary because of the 3 MHz gain bandwidth product of the TL082 op-amp. This gain bandwidth product is typical of readily available wide bandwidth operational amplifiers. However, recently op-amps with gain bandwidth products of up to 20 MHz have become available. Including the filtering and gain would require a gain bandwidth product of at least 19.7 MHz. Thus, the wider bandwidth operational amplifier would just suffice.

7.4 Summary

All loop components were successfully designed and built to calculated specifications. All parts were off the shelf components that are generally and cheaply available.
8. LOOP PERFORMANCE

The loop performance measures of most interest are loop stability, the transient behavior of the loop during acquisition and the recovered clock jitter. The root locus is a powerful technique for analyzing stability and transient behavior.

8.1 Root Locus

The open loop roots of the system consist of desired roots, and unwanted roots that appear because of the characteristics of the real devices. The clock recovery loop has two desired poles, one due to the integration of the VCO and one due to the active lead-lag filter. Both appear at the origin \( s = 0 \). There is also one zero due to the lead-lag filter which appears at:

\[
s = -1/T_1 = 1/(RC) = -1 \times 10^{-6}.
\]  

With only these open loop roots, the open loop transfer function will be:

\[
G(s) = \frac{p_\ast G K D P(s)}{s} = \frac{p_\ast G K D (T_1/T_2)(s+1/T_2)}{s^2} = \frac{K(s+1 \times 10^6)}{s^2},
\]  

(8.2)

where: \( K = p_\ast G K D (T_1/T_2) \) = loop gain.

The root locus plot of this function is shown in Fig. 8.1a. Fig. 8.1b shows the desired operating region enlarged. The equations used to design this clock recovery loop assume this ideal case which neglects the effect of extra roots.

In this implementation, there are two additional roots that should be included. The first is due to the gain-bandwidth product of the
Fig. 8.1 Root Locus Plot of Ideal Clock Recovery PLL;
(a) Closed loop poles plotted at gain increments of 200k;
(b) Enlarged view, Closed loop poles plotted at gain increments of 50k.
operational amplifier. The second is due to the modulation bandwidth of
the VCO. As discussed in chapter 7, the operational amplifier pole
appears at 18.8 Mrad/s and the VCO pole at 33.8 Mrad/s. Thus the open
loop transfer function becomes:

\[
G(s) = \frac{P_1 P_2 G K K_d (T_2 / T_1) (s+1/T_2)}{s^2 (s+P_1)(s+P_2) K(1+1M)}
\]

\[
= \frac{s^2 (s+18.8M)(s+33.8M)}{s^2 (s+18.8M)(s+33.8M)}
\]

where:
- \( P_1 \) = pole due gain bandwidth product of op-amp
- \( P_2 \) = pole due to modulation bandwidth of the VCO
- \( K = p_1 P_2 G K K_d (T_2 / T_1) \) = loop gain

Fig. 8.2a shows the overall root locus plot. Fig. 8.2b shows the
desired operating region enlarged. The response near the origin is
slightly elongated from the perfect circle observed in Fig. 8.1. This
indicates that equations (6.10) and (6.11) will be slightly in error,
as they predict \( \zeta \) and \( \omega_n \) assuming no excess poles. Also, in the ideal
case increasing the gain past critical damping (\( \zeta = 1 \)) will make the loop
increasingly overdamped, as both closed loop poles stay on the real
axis. In the actual case, the loop will become more overdamped until
the break away point at \( s = -6.86M \) is reached. At this point an
underdamped component appears. Increasing the gain far enough will make
the loop unstable.

8.2 Acquisition Time

During clock acquisition the gain \( K \) is \( 1.26 \times 10^{13} \). In this case,
equation (8.2) places the dominant closed loop poles at point \( p_{c}=1 \)
shown in Fig. 8.2. From this plot the damping and natural bandwidth at
this point are:

\[
\zeta = 0.70 \text{ and, } \omega_n = 1.54 \text{ Mrad/s,}
\]

(8.4)
Fig. 8.2 Root Locus Plot of Actual Clock Recovery PLL;
(a) Closed loop poles plotted at gain increments of $100 \times 10^{18}$;
which are close to the designed values.

The IDLE symbol sent during acquisition is a 62.5 MHz square wave. A low frequency rectangular signal gated the square wave signal to the input of the PLL. By triggering the HP54110D scope on this gating signal the loop behavior during acquisition could be observed.

Fig. 8.3 shows the control voltage during acquisition. Fig. 8.3a is a typical plot. The flat section at the start is the phase slip region. The remaining section is phase acquisition. It displays a damping near the designed value of 0.707. The settling time was 4.6 μs, this is close to the calculated value of 5 μs.

Fig. 8.3b shows two traces one adjusted for minimum phase slip time and one for maximum. The minimum time is 0.4μs. The maximum time is 3.3 μs. This is less than the estimate of 4.6 μs. The total acquisition time is approximately 7.9 μs.

It was observed that by careful phase adjustment of the input signal, a single cycle slip could be caused. The acquisition time, when this occurred, was not easily measured but was predominantly less than 10 μs. It does not seem to be possible to remove this cycle slip by increasing the bandwidth. It occurs when the initial phase difference is very close to the unstable null point of the phase detector.

8.3 Transient Performance During Data Transmission

During data transmission some of the transitions are missing. This reduces the gain of the loop and thus changes the transient response. In FDDI the probability of transition when data is sent can vary from 0.4≤p≤0.8 as discussed in chapter 3. The range of closed loop poles
Fig. 8.3 Control Voltage During Acquisition
(a) Typical Acquisition Plot; (b) Minimum and Maximum Phase Slip.
corresponding to these gains is plotted on Fig. 8.2b. The damping range is $0.42 \leq \xi \leq 0.612$ and the natural frequency is $0.92 \text{ Mrad/s} \leq \omega_n \leq 1.35 \text{ Mrad/s}$.

The noise bandwidth will be smaller when the loop is locked to data than during acquisition. Using the range of damping ratio and natural frequency corresponding to data transmission, the noise bandwidth calculated using (6.19) will range from:

$$4.67\text{kHz} \leq B_L \leq 1.38 \text{ MHz}$$

The settling time of a phase transient will be longer than with all transitions present, however, frequency steps are not expected to occur at this time.

8.4 Recovered Clock Quality

In Fig. 8.4 square wave data, as illustrated in the lower trace, was sent. The HP54110 oscilloscope is triggered off the rising data edge. The upper trace shows the recovered clock which has some line width due to jitter. The 200 ps peak-to-peak jitter is mainly due to noise.

In Fig. 8.5 the oscilloscope is triggered on the rising edge of length 255 pseudo-random data. In Fig. 8.5a the reference voltage level has been set to the optimum $-1.27 \text{ V}$. The upper trace shows the recovered clock which has a peak-to-peak jitter of 480 ps. This is a combination of noise and pattern effects. In Fig. 8.5b the reference voltage has been set to $-1.36 \text{ V}$. The jitter in the recovered clock increased to 670 ps, as the flywheel effect no longer maintained the correct frequency. In all these measurements the oscilloscope was set
Ch. 1 = 320.0 mV/div
Ch. 2 = 320.0 mV/div
Timebase = 2.00 nsec/div

Trigger mode: Edge
On Pos. Edge on Chan2

Trigger Levels
Chan2 = -1.299 volts
Holdoff = 70.000 nsecs

Fig. 8.4 Clock Recovered from Square Wave Input.
Fig. 8.5 Clock Recovered from Random Data:
(a) $V_e = -1.27$ V; (b) $V_e = -1.36$ V.
to infinite persistence to obtain a reasonable peak-to-peak jitter measurement.

8.5 Summary

The root locus technique was particularly useful in determining the effect of unwanted poles. It closely described the transient performance of the loop.

The clock was acquired in less than 7.5 µs, unless a cycle slip occurred. The single cycle slip resulted from a small range of initial relative phase between the data and the loop clock. Even with a cycle slip, the acquisition time was almost always less than 10 µs.

The FDDI specifications do not indicate specific clock jitter performances or measurements. The recovered clock was clean both for square wave and pseudo-random data. Peak-to-peak jitter with pseudo-random data was 480 ps. This is considerably less than the maximum allowable clock jitter of 1.9 ns peak calculated in chapter 4.
9. CONCLUSIONS

Several aspects of clock recovery in FDDI have been investigated. These included analysis of the FDDI code, comparison of tuned circuit and PLL clock extraction, and the design and testing of a PLL clock extraction circuit operating at 125 MHz.

The FDDI code was analyzed and compared to other two level coding schemes. Its most unique aspect is the combining of 4B5B block encoding with NRZI transmission. FDDI code provides a reasonable dc balance, guaranteed clock content, 6 unique control codes, and simple encoder/decoder circuitry and the bit rate increased by 25% over uncoded data due to the 4B5B block encoding. The symbol error rate with both block and transition encoding is 6/5 that of 4B5B block encoding alone.

In the transmitted code the largest power contribution occurs at 1/3 the transmitted bit rate. The power dips toward dc and has nulls at the harmonics of the transmitted bit rate. By transition decoding, a clock component greater than 15 dB above the surrounding spectrum can be obtained. Considering all aspects, the FDDI code compared favorably to existing coding formats.

Jitter produced in tuned circuit and PLL clock recovery circuits was compared using results derived by Bennet [2] and Roza [9]. The main benefit of a PLL circuit is that the mistuning phase error can be reduced to an arbitrarily low value without increasing the jitter due to noise. Roza's results also indicated that pattern jitter could be made insignificant. This result required that the free running
frequency of the loop was the center frequency of the VCO range. If the dc loop gain is very large, this is unlikely. The jitter produced by pattern effects was observed when testing the PLL clock recovery circuit.

A PLL clock recovery circuit was successfully designed, built, and tested. The most difficult criterion was the 10 \( \mu \text{s} \) acquisition time. To keep the acquisition time to a minimum, cycle slipping was avoided. The phase slip time was bounded by ensuring that, at the beginning of acquisition, the VCO was at one extreme of its frequency range. This effect was produced by the very large dc gain of the active filter. Decreasing the acquisition time requires increasing the loop bandwidth (and noise jitter).

A phase detector that would produce a flywheel effect was chosen. The flywheel effect stops the loop frequency from changing widely when input transition pulses are missing. Under 'flywheel' conditions, the clock phase error increases. Thus, it is essential that the code be run bounded. FDDI has a run bound of 3 bits and at least 40% of the transitions present.

Tests on the PLL clock recovery circuit confirmed the predictions of transient performance made using the root locus analysis. The damping ratio was measured to be 0.7, which was close to the 0.707 calculated. The measured total acquisition time of 7.9 \( \mu \text{s} \) was under the designed 10 \( \mu \text{s} \). The problem of a single cycle slip was very rare. It occurred when the initial phase difference was close to the unstable null of the phase detector characteristic. Under these conditions the acquisition time was sometimes exceeded.
Measurements of jitter made with pseudo-random data were considerably less than the maximum allowed. Due to the complexity of the required test circuitry measurements with FDDI codes were not made. However, the dc balance and run length constraints should ensure the jitter produced by FDDI code is less than that of pseudo-random data. This work has developed a clock extraction circuit that meets the FDDI requirements.
REFERENCES


Appendix A: Message and Waveform Statistics

The message sequence is a discrete series of values, while the corresponding binary waveform is continuous with a periodic component due to the bit period. Both the message signal and the binary waveform are random or stochastic processes. In determining their statistical properties the ensemble of all possible functions will be considered. For the message signal a function or member is one sequence of values.

The development of the following statistics will assume that the message sequences are ergodic. From this it follows that the process is strictly stationary and that the averages of the ensemble, at a fixed time or sample, are identical to the averages of any individual member. In a strict sense stationary process, all statistical properties are unaffected by a shift in the time origin.

In the calculation of ensemble averages or expectations, the sample number in the discrete case (and time in the continuous case) is fixed. The average is found over the ensemble. Ensemble averages are indicated by \( E\{ \} \), where the \( E \) stands for expectation. For the message sequence, the values of \( a_n \) are discrete. The expected value is:

\[
E\{a_n\} = \sum_{i=1}^{b} p_i a_{n_i}
\] (A.1)

where: \( p_i \) = probability of the discrete level \( i \), and
\( b \) = number of discrete levels (for binary PCM \( b=2 \)).

It should be noted that \( n \) is fixed for this calculation. However, as the process is strict sense stationary the result will be the same for any value of \( n \).

In the member averages only one function is taken but it is averaged over all its samples (or time). The member average for the message signal is given by:

\[
\langle a_n \rangle = \lim_{N \to \infty} \frac{1}{2N+1} \sum_{n=-N}^{N} a_n.
\] (A.2)

The averages of interest are the 1st and 2nd moments and the autocorrelation. Since the message signal is assumed ergodic, these averages will refer interchangeably to the ensemble and member values. Thus the first moment (\( m_1 \)) or mean is:

\[
m_1 = E\{a_n\} = \langle a_n \rangle.
\] (A.3)

The 2nd moment (\( m_2 \)) or mean square value is:

\[
m_2 = E\{a_n^2\} = \langle a_n^2 \rangle,
\] (A.4)
and the autocorrelation $R(k)$ is:

$$R(k) = E(a_n a_{n+k}) = \langle a_n a_{n+k} \rangle. \quad (A.5)$$

The following development of the ensemble mean, mean square and autocorrelation for the binary waveform shows the close relationship to the message sequence statistics:

$$E[x(t)] = E\left( \sum_{n=-\infty}^{\infty} a_n d(t-nT) \right)$$

$$= \sum_{n=-\infty}^{\infty} E(a_n) d(t-nT)$$

$$= m_1 \sum_{n=-\infty}^{\infty} d(t-nT), \quad (A.6)$$

$$E[x^2(t)] = E\left( \sum_{n=-\infty}^{\infty} a_n^2 d^2(t-nT) \right)$$

$$= \sum_{n=-\infty}^{\infty} E(a_n^2) d^2(t-nT), \quad (A.7)$$

$$R_x(r,t) = E[x(t)x(t+r)]$$

$$= E\left( \sum_{m=-\infty}^{\infty} a_m d(t-mT) \sum_{n=-\infty}^{\infty} a_n d(t-nT+r) \right)$$

$$= \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} E(a_ma_n) d(t-mT)d(t-nT+r)$$

$$\quad = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} R(m-n)d(t-mT)d(t-nT+r). \quad (A.8)$$

These averages do vary with time and the waveform is not stationary. However, the statistics are periodic. Thus:

$$E[x(t+T)] = E[x(t)], \quad (A.9)$$

$$E[x^2(t+T)] = E[x^2(t)], \quad (A.10)$$

$$R_x(r+T,t+T) = R_x(r,t). \quad (A.11)$$

This property is described as "periodically stationary" or "cyclostationary". The term cycloergodic can be used where the statistics over the ensemble at a fixed time are the same as the member statistics over the instants of time differing from that fixed instant by multiples of the period. If the message sequence is stationary the corresponding PAM (pulse amplitude modulation) signal is cyclostationary [22].
Appendix B: The Power Spectral Density

The power spectral density (PSD) can be found by phase randomization, or by ensemble averaging the power spectral densities of the member functions. These two approaches give the same answer.

Phase randomization makes the assumption that the phase of the sample functions are unknown. The phase becomes a random variable uniformly distributed over one cycle:

\[ x(t) = x(t+\theta) \text{ phase randomized function} \]  \hspace{1cm} (B.1)

where:

\[ p_{\theta}(\theta) = \begin{cases} 
1/T & |\theta| \leq T/2 \\
0 & |\theta| > T/2 
\end{cases} \]  \hspace{1cm} (B.2)

= probability density function of \( \theta \)

A cyclostationary function that is phase randomized becomes stationary. The power spectral density can now be found by taking the Fourier transform of the autocorrelation function. This method is the most commonly used in the literature [8,23]. However, the phase of the signal in a synchronous system is an important parameter containing vital information. It is, therefore, more satisfying to obtain the result without the assumption of random phase.

Bennet [21] has approached the derivation of the power spectrum by ensemble averaging the members' power spectrum. This approach requires the waveform be stationary or cyclostationary. In his derivation he removes the mean from each function. This is not necessary for the general result and will not be done here.

The Fourier transform is used to transform the binary waveform into the frequency domain. The Fourier transform of a power signal only exists in the limit. By truncating the signal in time, the energy is limited and the transform can be found. Thus letting \( x_n(t) \) include only pulses from \( n = -N \) to \( N \):

\[ x_n(t) = \sum_{n=-N}^{N} a_n d(t-nT). \]  \hspace{1cm} (B.3)

The Fourier transform is given by:

\[ X_n(\omega) = \sum_{n=-N}^{N} a_n D(\omega) e^{-j\omega nT}, \]  \hspace{1cm} (B.4)

where: \( D(\omega) = \text{Fourier transform of } d(t) \).

To calculate the expected spectrum an ensemble average is taken. By dividing the waveform by its duration, the signal can be handled in terms of power rather than energy. The limit can now be extended to
infinity. Thus, the equation for PSD is given by [23]:

\[ S_x(\omega) \xrightarrow{N \to \infty} \text{lim}_{N \to \infty} \frac{E[|X_n(\omega)|^2]}{(2N+1)T} \quad \left(\frac{V^2}{\text{Hz}}\right) \]  

(B.5)

It is important to note that the operations of taking the ensemble average and taking the limit may not be interchanged [24].

From equation (B.4) the ensemble average of the Fourier transform of truncated waveform is:

\[ E\{|X_n(\omega)|^2\} = E\{X_n(\omega)X^*_n(\omega)\} \]
\[ = \sum_{m=-N}^{N} \sum_{n=-N}^{N} E\{a_m a_n\} D(\omega) D^*(\omega) e^{-j\omega T (m-n)} \]
\[ = \sum_{m=-N}^{N} \sum_{n=-N}^{N} R(m-n) |D(\omega)|^2 e^{-j\omega T (m-n)}. \]  

(B.6)

Letting \( m-n=k \):

\[ E\{|X_n(\ell)|^2\} = \sum_{m=-N}^{N} \sum_{k=-N}^{m+N} R(k) |D(\omega)|^2 e^{-j\omega T}. \]  

(B.7)

Changing the order of summation:

\[ \sum_{m=-N}^{N} \sum_{n=-N}^{m-N} = \sum_{m=-N}^{N} \sum_{k=-N}^{2N} \sum_{k=1}^{2N} \sum_{m-k-N}^{m-N} \]  

(B.8)

As the summand does not depend on \( m \) the terms can be counted to perform the summation:

\[ E\{|X_n(\omega)|^2\} = 2(N+1)|G(\omega)|^2 \left\{ R(0) + 2\sum_{k=1}^{2N} R(k) \cos(2\pi k f T) \right\}. \]  

(B.9)

Substituting into equation (B.5), yields the PSD:

\[ S_x(\omega) = \int \frac{|G(\omega)|^2 \left\{ R(0) + 2\sum_{k=1}^{\infty} R(k) \cos(2\pi k f T) \right\}}{2N+1} \quad \left(\frac{V^2}{\text{Hz}}\right). \]  

(B.10)
APPENDIX C: Jitter From Tuned Circuit Clock Recovery

The following derivations follow the general pattern of Bennet's paper "Statistics of Regenerative Transmission"[2].

C.1 Jitter

The clock signal (c(t)) recovered by a resonant circuit will be approximately sinusoidal. It is assumed cycloergodic, therefore the ensemble averages at a fixed period of time as the same as the time averages for a member at instants varying from that fixed time by multiples of the period.

The ensemble negative zero crossings will be clustered around a time \( t=t_{zc} \). The time \( t_{zc} \) is defined as:

\[
E[c(t_{zc})] = 0. \tag{C.1}
\]

The actual axis crossing for a member occurs at \( t_{zc}+\epsilon/\omega_1 \), where \( \epsilon \) is the phase difference in radians from the expected axis crossing. The rms jitter is defined as:

\[
\epsilon_{rms} = E[\epsilon^2]^{1/2} \text{ (rad)}. \tag{C.2}
\]

To calculate the effect of input noise and resonant circuit mistuning, it is useful to calculate jitter in terms of the amplitude rather than the phase of the recovered clock. The maximum amplitude of the sine wave occurs \( T/4 \) after the axis crossing. The difference from expected height is \( \delta \). For these calculations it will be assumed \( \epsilon \) and \( \delta \) are small and their second order effects can be ignored. The peak amplitude of the clock is given by:

\[
c(t_{zc}+T/4) = (1+\delta)E[c(t_{zc}+T/4+\epsilon/\omega_1)]. \tag{C.3}
\]

Thus, the clock waveform can be expressed:

\[
c(t) = -(1+\delta)E[c(t_{zc}+\epsilon/\omega_1+T/4)]\sin[\omega_1(t-t_{zc})-\epsilon]. \tag{C.4}
\]

For small \( \epsilon \), the value of the clock waveform at the expected axis crossing time is:

\[
c(t_{zc}) = -\sin(-\epsilon)(1+\delta)E[c(t_{zc}+\epsilon/\omega_1+T/4)]
= \epsilon(1+\delta)E[c(t_{zc}+T/4)]. \tag{C.5}
\]

The mean square value of clock waveform at the expected axis crossing is:

\[
E[c^2(t_{zc})] = E[\epsilon^2(1+2\delta+\delta^2)E^2[c(t_{zc}+T/4)]
= E[(\epsilon^2)]E^2[c(t_{zc}+T/4)]. \tag{C.6}
\]

Solving for the rms jitter:
C.2 Expected Clock Waveform Recovered by a Tuned Circuit

The following derivations depend on the assumptions that the amplitude variation of the clock signal is small and that the tuned circuit is shock excited. The first assumption is valid if there is no long periods without an impulse and the quality of the circuit is high. The second requires the pulse shape is short enough to be considered an impulse. The error will be slight as long as the continuous component of the spectrum is nearly flat over the bandwidth of the recovery filter. Rectangular pulses not exceeding half the clock period are considered to approximate impulses.

The impulse response \( h(t) \) of a series-tuned RLC circuit is:

\[
h(t) = A e^{-\alpha t} \cos(\omega_c t + \theta) \quad \text{(C.8)}
\]

where,

\[
\begin{align*}
\alpha &= \frac{(4Q+1)^{1/2}}{2L}, \\
\omega_c &= \frac{1}{LC} - \frac{R^2}{4L^2}^{1/2} \\
\tan(\theta) &= \frac{1}{2Q}, \\
Q &= \frac{\omega_c L}{R} = \text{quality factor}
\end{align*}
\]

Note: \( \omega_c \) is the resonant frequency of the damped system as distinguished from \( \omega_n = 1/(LC)^2 \) which is the natural frequency of an undamped system.

The ensemble average of the clock signal is found by replacing \( d(t) \) in equation (A.6) with \( h(t) \):

\[
E\{c(t)\} = m_1 \sum_{n=0}^{\infty} h(t-nT) = m_1 \sum_{n=0}^{\infty} A \exp(-\omega_c(t-nT)/2Q)\cos(\omega_c(t-nT)+\theta)
\]

After numerous trigonometric manipulations:

\[
E\{c(t)\} = \frac{m_1 A e^{-\tau (t-T/2)}}{2 \cosh^2 \omega_c T/4Q - \cos^2 \omega_c T/2} \left[ \sinh \omega_c T \cos \omega_c T/2 \cosh^2 [\omega_c (t-T/2) + \theta] - \cosh \omega_c T \sin \omega_c T \sin [\omega_c (t-T/2) + \theta] \right] \quad \text{(C.10)}
\]

The expected value of the clock waveform depends only on the first moment, \( m_1 \), of the message sequence. Therefore, this result holds for
both independent and transition messages.

With perfect tuning $\omega_0 = \omega = 2\pi/T$. The output becomes:

$$E[c(t)] = \frac{m_1 \omega (4Q^2 + 1)^{1/2} \exp(-\omega t \pi)/20) \cos(\omega t T/2 + \theta)}{4RQ^2 \sinh(\pi/2Q)}$$  \hspace{1cm} (C.11)

This shows the initial amplitude depends on the mean of the message signal, and the rate of decay in amplitude depends on the value of $Q$.

C.3 Effects of Mistuning on Jitter

Equation (C.7) can be used to calculate the jitter due to mistuning. First $E[x^2(t)]$ must be calculated:

$$E[x^2(t)] = \mathbb{E}[E[c(t)]^2 + \{c(t) - E[c(t)]\}^2]$$

where:

$\mathbb{E}[y(t)] = c(t) - E[c(t)]$

$$= \sum_{n=-\infty}^{\infty} (A_n - m_1) h(t - nT).$$  \hspace{1cm} (C.13)

As $y(t)$ is the clock waveform with the mean removed:

$$R_y(0,t) = \mathbb{E}[y^2(t)],$$  \hspace{1cm} (C.14)

and equation (C.12) becomes,

$$E[x^2(t)] = \mathbb{E}^2[c(t)] + R_y(0,t).$$  \hspace{1cm} (C.15)

The autocorrelation $R_y(0,t)$ is:

$$R_y(0,t) = \mathbb{E}[y(t)y(t)]$$

$$= \mathbb{E}\left[ \sum_{m=-\infty}^{\infty} (a_m - m_1) h(t - mT) \sum_{n=-\infty}^{\infty} (a_n - m_1) h(t - nT) \right]$$

$$= \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \mathbb{E}((a_m - m_1)(a_n - m_1)) h(t - mT) h(t - nT)$$

$$= \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \{R(n-m) - m_1^2\} h(t - mT) h(t - nT).$$  \hspace{1cm} (C.16)

The value of $R_y(0,t)$ is affected by the dependence of the message values. The value calculated for an independent message sequence will not hold for dependent message sequence.

In the case of a binary independent message:
\[ R(n) = \begin{cases} m_1 & \text{if } n=0 \\ m_1^2 & \text{if } n>0 \end{cases} \] (C.17)

Therefore equation (C.16) is zero unless \( n=m \):

\[ R_{v}(0, t) = m_1 (1-m_1) \sum_{n=0}^{\infty} h^2 (t-nT) \] (C.18)

Using the geometric expansion similar to that used in (C.10), equation (C.18) becomes:

\[
R_{v}(0, t) = m_1 (1-m_1) A^2 \exp\left(-\frac{\omega_c t}{Q}\right) \sum_{n=0}^{\infty} \left\{ 1 + \cos(\omega_c t + \theta - \omega_c nT) \right\} \exp\left(\frac{\omega_c t}{Q}\right) \left[ 1 + \cos(\omega_c t + \theta - \omega_c nT) \right] \]

where,

\[ \omega_c = \omega_c T/(4Q), \] (C.20)

\[ \rho = \omega_c T/2, \quad \text{and} \]

\[ \sigma = \omega_c (t_{sc} - T/2 + \theta). \] (C.21)

The value of \( R_{v}(0, t_{sc}) \) becomes:

\[
R_{v}(0, t_{sc}) = m_1 (1-m_1) \omega_c^2 (4Q^2+1) \exp\left(-\frac{\omega_c (t_{sc} - T/2)}{Q}\right) \left\{ \sinh^2(2\alpha) + \sin^2(2\beta) + \frac{\sinh^2(2\alpha) \cos(2\sigma) \cos(2\varphi) - \sin(2\alpha) \cosh(2\alpha) \sin(2\beta) \sin(2\varphi)}{1+\tanh^2(\alpha) \cot^2(\beta)} \right\}. \] (C.23)

As \( E(t_{sc}) = 0 \), for \( t=t_{sc} \) the expression in the square brackets of (C.10) is zero. Substituting in \( \sigma \), and solving yields the following expression for \( \sigma \):

\[ \sigma = \arctan\left[ \tanh(\omega_c T/4Q) \cot(\omega_c T/2) \right]. \] (C.24)

Therefore,

\[ \sin(\sigma) = \tan(\alpha) \cot(\beta) (1+\tanh^2(\alpha) \cot^2(\beta))^{-1/2}, \] (C.25)

\[ \cot(\sigma) = (1+\tanh^2(\alpha) \cot^2(\beta))^{-1/2}, \] (C.26)

\[ \sin(2\sigma) = \frac{2\tanh(\alpha) \cot(\beta)}{1+\tanh^2(\alpha) \cot^2(\beta)}, \quad \text{and} \] (C.27)

\[ \cos(2\sigma) = \frac{1-\tanh^2(\alpha) \cot(\beta)}{1+\tanh^2(\alpha) \cot^2(\beta)}. \] (C.28)
Substituting (C.27) and (C.28) into equation (C.23) and reducing:

\[ R_\nu(0, t_{\infty}) = \frac{m_1(1-m_1)\omega_c^2(4Q^2+1)\sin^2(2\beta)\exp(-\omega_c(t_{\infty}-T/2)/Q)}{16R^2Q^4 \sinh2\alpha(\cosh^2(2\alpha)-\cos^2(2\beta))}. \]  

(C.29)

If \( Q \) is high then the \( E(t_{\infty}+T/4) \) is very close to the maximum value of \( E(c(t)) \). This can be found by substituting \( t=t_{\infty}+T/4 \) into equation (C.10), and squaring:

\[ E^2\{c(t_{\infty}+T/4)\} = \frac{m_1^2\omega_c^2(4Q^2+1)\sin^2(\beta/2)\exp(-\omega_c(t_{\infty}-T/2+T/4)/Q)}{(4)16R^2Q^4(\cosh^2(\alpha)-\cos^2(\beta))}. \]  

(C.30)

By definition \( E\{c(t_{\infty})\}=0 \), therefore by (C.7) and (C.15):

\[ E(\varepsilon^2) = \frac{R_\nu(0, t_{\infty})}{E^2\{c(t_{\infty}+T/4)\}} = \frac{(1-m_1)\sin^2(2\beta)\exp(-\omega_c(t_{\infty}-T/2)/Q)}{4m_1\sin^2(\beta/2)\sinh2\alpha(\cosh^2(\alpha)-\cos^2(\beta))}. \]  

(C.31)

By defining a fractional tuning coefficient \( k \),

\[ k = \frac{\omega_c-\omega_1}{\omega_1}, \]  

(C.32)

the terms \( \alpha \) and \( \beta \) can be written as,

\[ \alpha = (1+k)\Pi/Q \quad \text{and} \]  

(C.33)

\[ \beta = (1+k)\Pi. \]  

(C.34)

Equation (C.31) can now be written in terms of \( k \) and \( Q \),

\[ E(\varepsilon^2) = \frac{(1-m_1)\sin^2(2k\Pi)\exp\left(\frac{(1-k)\Pi}{20}\right)}{4m_1\sinh\left(\frac{(1+k)\Pi}{Q}\right)\sin^2\left(\frac{(k+1)\Pi}{2}\right)\cosh\left(\frac{(1+k)\Pi}{20}\right)-\sin^2(k\Pi)}. \]  

(C.35)

For the region of interest, \( k<1 \) and \( Q>>1 \), the equation simplifies:

\[ E(\varepsilon^2) = \frac{(1-m_1)nk^2Q}{m_1} = \frac{(1-m_1)\Pi(\omega_c-\omega_1)^2Q}{m_1 \omega_1^2} \]  

(C.36)

This result shows that if there is any mistuning the rms jitter will increase with the square root of the \( Q \) factor. Therefore in the practical case an infinite \( Q \) is not desirable.

C.3 The Effect of Noise on Jitter

Noise can shift the pulses at the input of the tuned circuit causing jitter on output clock. The following development assumes the noise is ergodic.
The response of the tuned circuit to the noisy impulses is:

\[ z(t) = \sum_{n=-\infty}^{\infty} a_n h(t-nT+r_n) \]  

(C.37)

where, \( r_n \) = shift in reference time due to noise.

If \( r_n \) is small a first order power series can represent the output:

\[ z(t) = \sum_{n=-\infty}^{\infty} a_n [h(t-nT)+r_n h'(t-nT)] \]

\[ = c(t) + \sum_{n=-\infty}^{\infty} a_n r_n h'(t-nT). \]  

(C.38)

Correctly adjusting the output phase makes:

\[ E(r_n) = 0. \]  

(C.39)

Therefore:

\[ E[z(t)] = E[c(t)], \]  

(C.40)

and the mean square phase error can be written from (C.7):

\[ E[\epsilon_n^2] = \frac{E[z^2(t_{sc})]}{E^2[c(t_{sc}+T/4)]}. \]  

(C.41)

Using (C.38):

\[ E[z^2(t_{sc})] = E[(c(t_{sc}) + \sum_{n=-\infty}^{\infty} a_n r_n h'(t_{sc}-nT))^2] \]

\[ = E[x^2(t_{sc})] + 2E[c(t_{sc}) \sum_{n=-\infty}^{\infty} a_n r_n h'(t_{sc}-nT)] + E[\sum_{n=-\infty}^{\infty} a_n r_n h'(t_{sc}-nT)]^2 \]  

(C.42)

With independent noise values \( E[r_n^2] \) is a constant, and with no tuning error,

\[ E[c(t_{sc})] = 0. \]  

(C.43)

Therefore,

\[ E[z^2(t_{sc})] = \sum_{n=-\infty}^{\infty} \frac{E[a_n^2]E[r_n^2] h''^2(t-nT)}{n} \]

\[ = m^2 \sigma^2 \sum_{n=-\infty}^{\infty} [h'(t-nT)]^2. \]  

(C.44)
Taking the derivative of the impulse response in (C.8) gives:

\[ h'(t) = [A \exp(-\omega_c t/2Q) \cos(\omega_c t + \theta - \tau)] \frac{\omega_c (1-4Q^2)^{1/2}}{2Q} \]  
(C.45)

where, \( \tan(\tau) = 2Q \).

Setting \( \omega_c = \omega_s = 2\pi/T \), and solving the summation in the same manner as (C.19) gives:

\[ E[z^2(t_m)] = \frac{m^2 \omega_s^2 r_n^2 (4Q^2 + 1) \exp(-\omega_c t/2Q) \exp[\frac{n\omega_c T}{Q}] [1 + \cos(\omega_c t + \theta - \omega_c nT - \tau)]}{4Q^2 + 1} \]

\[ = \frac{m^2 \omega_s^2 r_n^2 (4Q^2 + 1)^2 \exp(-\omega_s (t_m - T/2)/Q) (2\cos^2(\omega_s t + \theta - \tau) + 1)}{64R^2 Q \sinh(\pi/Q)} \]  
(C.46)

The limit as \( Q \) approaches infinity is,

\[ E[z^2(t_m)] = \frac{m^2 \omega_s^4}{2\pi R^2 Q} r_n^2 \]  
(C.47)

Therefore, substituting (C.46) and (C.30) into (C.41) and letting \( Q \) approach infinity yields:

\[ E[\epsilon_n^2] = \frac{m^2 \omega_s^2 \pi \omega r_n^2}{2Q(m_1)^2} \]

\[ \lim_{Q \to \infty} E[\epsilon_n^2] = \frac{m^2 \omega_s^2 \pi \omega r_n^2}{2Q(m_1)^2} \]  
(C.48)

Thus, the larger the value of \( Q \) the less phase noise will be caused by the noise. It should be noted that for independent message values \( m_2 = m_1 \).
APPENDIX D: JITTER FROM PLL CLOCK RECOVERY

D.1 Jitter in PLL

The following analysis is based on Roza's paper "Analysis of Phase locked Timing Extraction Circuits for Pulse Coded Transmission" [8].

The signal into the loop will be a binary waveform as given by equation (2.2). The pulses will be less than a bit period wide. Due to the VCO integration, the power in each pulse is more important than the exact pulse shape. Thus, to simplify calculations the input waveform is written as a sum of weighted Dirac delta functions:

\[ N x_1(t) = \sum_{n=0}^{N} a_n \delta(t-nT-r_n) \]  \hspace{1cm} (D.1)

where, \( \theta_1 \) = input phase
\( \theta_0 \) = VCO phase
\( \phi_e \) = phase error
\( a_n \) = pulse weighting
\( r_n \) = shift from nominal or reference phase
\( \omega_c \) = center frequency of VCO
\( \omega_d = 2\pi/T \) = input data clock frequency

Fig. D.1 illustrates this digital interpretation of a PLL. The input to the loop is the phase angle \( \theta_1(NT) \), followed by a weighting factor \( a_n \).

![Digital Model of a PLL](image)

All phase angles in the loop can be written with respect to the output clock. The input phase has two components. One is the average input phase which is related to the output signal by the mistuning of the loop. The other is due to random noise effects:
Roza defines the phase error as the difference between the average input phase and the output phase:

$$\Theta_a(NT) = (\omega_1 - \omega_0) NT - 2\pi T n/T$$  \hfill (D.2)

It should be noted that in Bennet's analysis of tuned circuit clock recovery the phase error is between the actual input phase and the output phase.

In the digital model, the integration of the VCO sums effects from all of the past pulses. Thus, the output is obtained by convolving the output of the phase detector with the impulse response of the loop filter followed by an ideal VCO:

$$\Theta_o(NT) = \sum_{n=0}^{N} a_n(\Theta_a(nT) - \Theta_o(nT)) g(NT-nt) T$$  \hfill (D.4)

Substituting (D.2) and (D.3):

$$\Theta_o(NT) = \sum_{n=0}^{N} a_n [(\omega_1 - \omega_0) NT - 2\pi T n/T - \Theta_o nT] g(NT-nt) T$$

$$= \sum_{n=0}^{N} a_n \Theta_o(nT) g(NT-nt) T - 2\pi \sum_{n=0}^{N} a_n r_n g(NT-nt) T$$ \hfill (D.5)

Solving for the phase error $$\Theta_a(NT)$$:

$$\Theta_a(NT) = (\omega_1 - \omega_0) NT - \sum_{n=0}^{N} a_n \Theta_a(nT) g(NT-nt) T + 2\pi \sum_{n=0}^{N} a_n r_n g(NT-nt) T$$ \hfill (D.6)

The phase error can be written in terms of an expected value, and a zero mean random value:

$$\Theta_a(nT) = \mathbb{E}[\Theta_a(nT)] + \Delta \Theta_a(nT)$$  \hfill (D.7)

In the case where:

$$\lim_{N \to \infty} \sum_{n=0}^{N} a_n T g(NT-nt) >> 1$$ \hfill (D.8)

Roza separated the average or static phase error $$\mathbb{E}[\Theta_a(nT)]$$ into two significant components.

$$\mathbb{E}[\Theta_a(nT)] = \epsilon_m + \epsilon_r + \text{negligible effects}$$ \hfill (D.9)

where:
\[ \epsilon_m = \frac{(\omega_1 - \omega_c)NT}{\lim_{n \to N} \sum g(NT-nT)} \quad (D.10) \]

\[ \epsilon_r = \frac{2\pi \epsilon_{\omega}}{\pi E\{a_n\}} \quad (D.11) \]

\( \epsilon_m \) is the phase error caused by the VCO having a center frequency different from the bit frequency. This corresponds to a mistuned filter. For a second order phased locked loop the open loop transfer function is given by \( G(s) \) (the Laplace transform of \( g(t) \)):

\[ G(s) = \frac{s \omega n(2\xi - \omega n/K_v) + \omega n^2}{s(s + \ln^2/K_v)} \quad (D.12) \]

By using the final limit theorem, for this transfer function (D.10) simplifies to,

\[ \epsilon_m = \frac{\omega_1 - \omega_c}{m_1 K_v} \quad (D.13) \]

\( \epsilon_r \) term is caused by referencing the phase error to the average not the actual incoming phase. Bennet referenced to the actual incoming phase and thus a similar term does not occur.

Roza also determines an equation for the fluctuating phase shift or jitter:

\[ \epsilon(NT) = \sum_{n=0}^{N} [-T(a_n - m_1)\epsilon_m - 2\pi E\{a_n, r_n\}/m_1]g(NT-nT) \quad (D.14) \]

If \( a_n \) and \( r_n \) are mutually independent then their contributions can be considered separately:

\[ E[\epsilon^2] = E[\epsilon_p^2] + E[\epsilon_n^2] \quad (D.15) \]

From equation (D.14) the pattern jitter is then,

\[ E[\epsilon_n^2] = T^2 \epsilon_m^2 \lim_{N \to N+1} \sum_{n=0}^{N} \sum_{n=0}^{N} (a_n - m_1)(a_m - m_1)g(NT-nT)g(NT-mT) \]

\[ = T^2 \epsilon_m^2 \lim_{N \to N+1} \sum_{n=0}^{N} \sum_{n=0}^{N} (R(0) - m_1^2)g(NT-nT)g(NT-mT) \quad (D.16) \]

If the values of \( a_n \) are statistically independent then the term in the summation becomes zero when \( n \neq m \). Therefore:

\[ E[\epsilon_p^2] = T^2 \epsilon_m^2 (R(0) - m_1^2) \lim_{N \to N+1} \sum_{n=0}^{N} g(NT-nT)^2 \quad (D.17) \]
Defining \( B \) the closed loop noise bandwidth as:

\[
B_L = m_1^2 T \lim_{N \to \infty} \frac{1}{N+1} \sum_{n=0}^{N} g^2(NT-nT),
\]

and defining the effective \( Q \) as:

\[
Q_{\text{eff}} = \frac{\pi}{4TB_L},
\]

and substituting the value of \( R(0) \) given in (A.18) equation (D.18) can be written as:

\[
E(\epsilon_\rho^2) = \frac{\epsilon_m^2 \pi}{4Q_{\text{eff}} m_1} (\frac{1-m_1}{m_1})^2 (\omega_0 - \omega_c)^2 \pi (1-m_1),
\]

\[
= \frac{(m_1 K_c)^2}{4Q_{\text{eff}} m_1}.
\]

The jitter term due to pattern vanishes as \( m_1 \) approaches 1. This corresponds to all pulses present.

The jitter due to noise on the input signal from equation (D.14) is:

\[
E(\epsilon_n^2) = \frac{2\pi}{m_1} \lim_{N \to \infty} \frac{1}{N+1} \sum_{n=0}^{N} \left( \frac{E(a_n r_n) - E(r_n)}{m_1} \right)^2,
\]

but if \( a_n \) and \( r_n \) are independent,

\[
E(a_n r_n) = E(a_n) E(r_n).
\]

Therefore,

\[
E(\epsilon_n^2) = \frac{4\pi^2}{m_1} \lim_{N \to \infty} \frac{1}{N+1} \sum_{n=0}^{N} \sum_{n=0}^{N} a_n a_m E(r_n-E(r_n))(r_m-E(r_m))g(NT-nT)g(NT-mT)
\]

\[
= \frac{4\pi^2}{m_1} \lim_{N \to \infty} \frac{1}{N+1} \sum_{n=0}^{N} \sum_{n=0}^{N} a_n a_m E[Rr_n (n-m)-E^2(r_n)]g(NT-nT)g(NT-mT)
\]

If \( r_n \) are zero mean and independent then, using (A.4),

\[
E(\epsilon_n^2) = \frac{4\pi^2 m_2 r^2}{m_1} \lim_{N \to \infty} \frac{1}{N+1} \sum_{n=0}^{N} g^2(NT-nT)
\]

Substituting in \( Q_{\text{eff}} \),

\[
E(\epsilon_n^2) = \frac{4\pi^2 m_2 r^2}{T^2 m_1^2 2Q_{\text{eff}}},
\]

It should be remembered \( r_n \) and \( a_n \) are rarely truly independent.
APPENDIX E: DATA SHEETS
SILICON EPICAP DIODES

... designed in the new low-inductance mini-L package for high volume requirements of UHF and VHF TV tuning and AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- Guaranteed Minimum Q Values at VHF and UHF Frequencies
- Controlled and Uniform Tuning Ratio

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Reverse Voltage</td>
<td>VR</td>
<td>30</td>
<td>Volts</td>
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<tr>
<td>Forward Current</td>
<td>IF</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Device Dissipation @ T8 = 26°C</td>
<td>PD</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>Derate above 26°C</td>
<td></td>
<td>4.0</td>
<td>mW/°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>Tj</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tstg</td>
<td>-65 to +150</td>
<td>°C</td>
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FIGURE 1 - DIODE CAPACITANCE

<table>
<thead>
<tr>
<th>Capacitance (pF)</th>
<th>VR Revers Voltage (Volts)</th>
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<td>0.5</td>
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BB105A — White on ridge, Blue on flat
BB105B — White on ridge, Yellow on flat
BB105G — White on ridge, Green on flat

CASE 22G01
BB105A • BB105B • BB105G

ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Characteristic All Types</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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<td>Reverse Breakdown Voltage</td>
<td>BVR</td>
<td>30</td>
<td>-</td>
<td>Vdc</td>
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<tr>
<td>(IR = 10 μAdc)</td>
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<tr>
<td>Reverse Voltage Leakage Current</td>
<td>IR</td>
<td>-</td>
<td>50.0</td>
<td>nAdc</td>
</tr>
<tr>
<td>(VIR = 28 V)</td>
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<tr>
<td>(VIR = 28 V; TA = 80°C)</td>
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<td>Series Inductance</td>
<td>Ls</td>
<td>-</td>
<td>3.0</td>
<td>nH</td>
</tr>
<tr>
<td>(f = 250 MHz)</td>
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<td></td>
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</tr>
<tr>
<td>Diode Capacitance Temperature Coefficient</td>
<td>TCC</td>
<td>-</td>
<td>400</td>
<td>ppm/°C</td>
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<table>
<thead>
<tr>
<th>Device Type</th>
<th>CV</th>
<th>Gy</th>
<th>RS</th>
<th>Cy/C25</th>
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<tr>
<td></td>
<td>Min</td>
<td>Min</td>
<td></td>
<td>Max</td>
</tr>
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<td>2.9</td>
<td>225</td>
<td>0.9</td>
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<td>BB105B</td>
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<td>BB105G</td>
<td>1.8</td>
<td>2.9</td>
<td>150</td>
<td>1.2</td>
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</table>

**Figure 2 – Figure of Merit**

**Figure 3 – Diode Capacitance**

![Figure 2](image1.png)

![Figure 3](image2.png)


**MC1733**

**DIFFERENTIAL VIDEO WIDE-BAND AMPLIFIER**

SILICON MONOLITHIC INTEGRATED CIRCUIT

---

**DIFFERENTIAL VIDEO AMPLIFIER**

...a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth - 120 MHz typical @ A_{in} = 10
- Rise Time - 2.5 ns typical @ A_{in} = 10
- Propagation Delay Time - 3.6 ns typical @ A_{in} = 10

---

**MC1733C**
### MAXIMUM RATINGS

<table>
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<th>Property</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>(V_{CC})</td>
<td>+6.0</td>
<td>(\text{Vrms})</td>
</tr>
<tr>
<td>(V_{EE})</td>
<td>-2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(V_{IN})</td>
<td>15.0</td>
<td>(\text{Vrms})</td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>(V_{CM})</td>
<td>15.0</td>
<td>(\text{Vrms})</td>
</tr>
<tr>
<td>Output Current</td>
<td>(I_O)</td>
<td>10</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>Internal Power Dissipation (Max)</td>
<td>(P_{D})</td>
<td>800</td>
<td>(\text{mW})</td>
</tr>
<tr>
<td>Metal Can Package</td>
<td>800</td>
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</tr>
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<td>Operating Temperature Range</td>
<td>MC1733C</td>
<td>(T_A)</td>
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<td>MC1733</td>
<td>(T_{min}) to (T_{max})</td>
<td>(125)°C</td>
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<td>MC1733C</td>
<td>(T_{min})</td>
<td>-65°C to 150°C</td>
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### ELECTRICAL CHARACTERISTICS

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<th>Characteristics</th>
<th>Symbol</th>
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<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<td>(A_{in})</td>
<td>200</td>
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<td>900</td>
<td>250</td>
<td>600</td>
<td>800</td>
<td>(\text{MHz})</td>
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<td>Gain 2 (Note 3)</td>
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<td>(B_W)</td>
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<tr>
<td>Rise Time ((I_{in} = 50 \Omega, V_{in} = 1 \text{Vp-p}))</td>
<td>(T_{RL})</td>
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<td>Input Noise Voltage ((I_{in} = 50 \Omega), (8 \leq f \leq 10 \text{MHz}))</td>
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<td></td>
</tr>
<tr>
<td>Gain 2 and Gain 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Common-Mode Voltage (Gain 3)</td>
<td>(V_{CMO})</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>(\text{V})</td>
<td></td>
</tr>
<tr>
<td>Gain 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Gain (Gain 3)</td>
<td>(V_{O})</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
<td>(\text{V})</td>
</tr>
<tr>
<td>Gain 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Saturation Current (Gain 3)</td>
<td>(I_{SAT})</td>
<td>10</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>Gain 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Resistance ((R_{out}))</td>
<td>(R_{OUT})</td>
<td>20</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td>Gain 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Current (Gain 3)</td>
<td>(I_{PS})</td>
<td>10</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td>(\text{mA})</td>
</tr>
</tbody>
</table>
MC1733, MC1733C

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5$ V, $V_{EE} = -5$ V, $T_A = +70\degree C$ unless otherwise noted)\(^\ddagger\)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>MC1733</th>
<th>MC1733C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Voltage Gain</td>
<td>$A_{DD}$</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Gain 1 (Note 2)</td>
<td>90</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>Gain 2 (Note 2)</td>
<td>80</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Gain 3 (Note 3)</td>
<td>60</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>Input Resistance Gain 2</td>
<td>$R_{IN}$</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Input Offset Current (Gain 2)</td>
<td>$I_{OS}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Bias Current (Gain 2)</td>
<td>$I_{B}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Voltage Range (Gain 2)</td>
<td>$V_{IN}$</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio Gain 2</td>
<td>$CMRR$</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Supply Voltage Loading (Gain 2)</td>
<td>$PSR/H$</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Output Offset Voltage Gain 1</td>
<td>$V_{OS}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Gain 2 and Gain 3</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing (Gain 2)</td>
<td>$V_{OS}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output Sink Current (Gain 2)</td>
<td>$I_{S}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power Supply Current (Gain 2)</td>
<td>$I_{P}$</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

\(^\ddagger\)Note: $+60\degree C$ for MC1733C, $-50\degree C$ for MC1733

NOTES

1. Operate metal package at $6.5$ mV/$\degree C$ for operation at ambient temperatures above $75\degree C$ and dual-in-line pack- age at $5$ mV/$\degree C$ for operation at ambient temperatures above $100\degree C$ (see Figure 4). All parts are rated for high-ambient temperatures in a standard MC1733B 8-lead package, but if operated at high ambient temperatures, a heat sink may be necessary to limit maximum junction tempera- ture to $150\degree C$. Thermal capacitances (measured for the metal package at $60\degree C$ per foot).

2. Gain 2, 3, and 4 gain stages are connected together.

3. Gain 2, 3, and 4 gain stages are connected together.

4. All four gain stages are connected.

TYPICAL CHARACTERISTICS ($V_{CC} = +5$ V, $V_{EE} = -5$ V, $T_A = +70\degree C$ unless otherwise noted)

- **Figure 4** - Maximum allowable power dissipation
- **Figure 5** - Supply current vs. ambient temperature
- **Figure 6** - Supply current vs. supply voltage
TYPICAL CHARACTERISTICS (continued)

(WCC = +6.0 Vol, VGE = -6.0 Vol, T_A = +25°C unless otherwise noted.)

FIGURE 7 - GAIN versus TEMPERATURE

FIGURE 8 - GAIN versus FREQUENCY

FIGURE 9 - GAIN versus SUPPLY VOLTAGE

FIGURE 10 - GAIN versus BUSS

FIGURE 11 - GAIN versus FREQUENCY and SUPPLY VOLTAGE

FIGURE 12 - GAIN versus FREQUENCY and TEMPERATURE

6-103
TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the read circuit. The first block, referred to as "amplification", increases the level of the signal available from the read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system uses a direct or tape, and the type of head and the density used. For a representative tape system, levels of 7 to 25 mV for the signal from the read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 20 to 40 dB.

The overall gain requirement is implemented with several stages of amplifiers. For instance, a tape cartridge system with variable tape speed may require a few stages for gain and a second stage primarily for gain equalization. The input stage amplified signals 25 mV in the first stage and 10 to 15 dB in the second stage.

Decomposes suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with lower transfer rates approximately uses low cost operational amplifiers. Examples of these are the MC174I, MC1492, MC1749, and MLAS01. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual crossover point where wideband amplifiers are cost-effective varies with equipment design. For purposes of comparison, the MLAS01 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 28 dB open-loop gain at 100 kHz; the MC1733 has approximately 29 dB of gain out to 108 MHz (depending on gain option and loading).

There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive diode circuit that generates "zero-crossings" at each of the data peaks in the read signal.

The actual circuitry used to determine the read signal varies from a differential LC type in disc systems to a single RC type in reel and cartridge systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossing is performed with the threshold. These transistors serve to generate a TTL compatible pulse waveform with "zero" corresponding to zero-crossing. For low transfer rates, the circuit often used consists of an operational amplifier with a few or two diodes. For higher transfer rates (greater than 100 MHz), comparators are used. The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, sense-detector" has the output NAND gate when either the negative or positive data peaks of the read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first requires the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gate.
APPLICATIONS INFORMATION (continued)

FIGURE 25 - READ CIRCUIT METHOD II

Another common technique is shown in Figure 25. The branch labeled 'm will fire, push, etc., provides a match condition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuits prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 26 - READ CIRCUIT METHOD II

The technique shown in Figure 26 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuit. For instance, if cost is the predominant overall factor, then approach one may be the only feasible alternative.

Method four was included in a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

6-107
MC1648/MC1648M
VOLTAGE-CONTROLLED
OSCILLATOR

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a variable frequency input for the oscillator (VCO). The MC1648 was designed for use in the Master/Phase-Locked Loop shown in Figure 9. The device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>Gnd Pin</th>
<th>Supply Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5.0 Vdc</td>
<td>7.9</td>
<td>1.14</td>
</tr>
<tr>
<td>-5.2 Vdc</td>
<td>1.14</td>
<td>7.8</td>
</tr>
</tbody>
</table>

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 648

F SUFFIX
CERAMIC PACKAGE
CASE 607

FIGURE 1 - CIRCUIT SCHEMATIC
**ELECTRICAL CHARACTERISTICS**

Supply Voltage = ±5.0 Volts

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>-55°C</th>
<th>-25°C</th>
<th>+25°C</th>
<th>+55°C</th>
<th>+125°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Drain Current</td>
<td>Ig</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>41</td>
<td>mA</td>
</tr>
<tr>
<td>Logic &quot;1&quot; Output Voltage</td>
<td>VOD1</td>
<td>3.87</td>
<td>3.85</td>
<td>3.90</td>
<td>3.95</td>
<td>4.00</td>
<td>VDC</td>
</tr>
<tr>
<td>Logic &quot;0&quot; Output Voltage</td>
<td>VOD0</td>
<td>3.73</td>
<td>3.60</td>
<td>3.63</td>
<td>3.64</td>
<td>3.67</td>
<td>VDC</td>
</tr>
<tr>
<td>B思 Voltage</td>
<td>VBD</td>
<td>1.87</td>
<td>1.87</td>
<td>1.87</td>
<td>1.87</td>
<td>1.87</td>
<td>VDC</td>
</tr>
<tr>
<td>Peak-to-Peak Output Voltage</td>
<td>Vpp</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td>Output Duty Cycle</td>
<td>VDC</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>%</td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>fmax</td>
<td>226</td>
<td>226</td>
<td>226</td>
<td>226</td>
<td>226</td>
<td>MHz</td>
</tr>
</tbody>
</table>

*This measurement guarantees the ac potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

*Frequency variation over temperature is a direct function of the DC/8 Temperature and AL/I8 Temperature.*

**TEST VOLTAGE/CURRENT VALUES**

<table>
<thead>
<tr>
<th>Test Temperature</th>
<th>VDD</th>
<th>VILmin</th>
<th>VOH</th>
<th>Ic</th>
</tr>
</thead>
<tbody>
<tr>
<td>-25°C</td>
<td>+2.00</td>
<td>+1.50</td>
<td>5.0</td>
<td>-5.0</td>
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<tr>
<td>+25°C</td>
<td>+1.80</td>
<td>+1.25</td>
<td>5.0</td>
<td>-5.0</td>
</tr>
<tr>
<td>+55°C</td>
<td>+1.70</td>
<td>+1.20</td>
<td>5.0</td>
<td>-5.0</td>
</tr>
<tr>
<td>-55°C</td>
<td>+2.67</td>
<td>+1.57</td>
<td>6.0</td>
<td>-5.0</td>
</tr>
<tr>
<td>+125°C</td>
<td>+1.60</td>
<td>+1.10</td>
<td>6.0</td>
<td>-5.0</td>
</tr>
</tbody>
</table>

**FIGURE 2 - SPECTRAL PURITY OF SIGNAL AT OUTPUT**

- The 1300 ohm resistor and the 1000 ohm resistor in parallel produce a 20 nF attenuation probe. Each shall be C0105 50 of equipment.
<table>
<thead>
<tr>
<th>Test Voltage/Current Values</th>
<th>MC1648A</th>
<th>MC1648M</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-30°C</td>
<td>2.70</td>
<td>2.70</td>
</tr>
<tr>
<td>+26°C</td>
<td>3.36</td>
<td>3.86</td>
</tr>
<tr>
<td>+65°C</td>
<td>4.60</td>
<td>4.60</td>
</tr>
<tr>
<td>-65°C</td>
<td>3.13</td>
<td>3.63</td>
</tr>
<tr>
<td>+26°C</td>
<td>3.26</td>
<td>3.86</td>
</tr>
<tr>
<td>+65°C</td>
<td>4.60</td>
<td>4.60</td>
</tr>
</tbody>
</table>

**ELECTRICAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>-50°C</th>
<th>-30°C</th>
<th>0°C</th>
<th>+25°C</th>
<th>+60°C</th>
<th>+125°C</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Drain Current</td>
<td>IC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
<td>Input and output sums.</td>
</tr>
<tr>
<td>Logic &quot;A&quot; Output Voltage</td>
<td>VOUT</td>
<td>-1.080</td>
<td>-0.870</td>
<td>-1.046</td>
<td>-0.815</td>
<td>-0.860</td>
<td>-0.756</td>
<td>-0.860</td>
<td>-0.860</td>
</tr>
<tr>
<td>Logic &quot;G&quot; Output Voltage</td>
<td>VODL</td>
<td>-1.620</td>
<td>-1.620</td>
<td>-1.600</td>
<td>-1.850</td>
<td>-1.820</td>
<td>-1.875</td>
<td>-1.820</td>
<td>-1.820</td>
</tr>
<tr>
<td>Peak to Peak Pack Voltage</td>
<td>VPP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
<td>See Figure 3.</td>
</tr>
<tr>
<td>Output Duty Cycle</td>
<td>VDC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>fout</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Hz</td>
<td></td>
</tr>
</tbody>
</table>

*This measurement guarantees the AC potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

**Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔI/Δ Temperature.
Figure 3 illustrates the circuit schematic for the MC1648B. The oscillator incorporates active feedback by causing the base of transistor Q2 to follow the emitter of Q3. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain a high Q of the oscillator, and provide high overall stability at the output, transistor Q6 is used to transfer the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in combination with output transistor Q1, provide a high bandwidth output which produces a square wave. Transistors Q9 and Q11 provide the base drive for the oscillator and output buffer. Figure 3 indicates the high frequency stability of the oscillator output (see 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diodes (D1) should be biased at least 2 V above Vgg (41.4 V for positive supply operation).

When the MC1648B is used with a constant dc voltage to the varactor diodes, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

### Figure 4 - The Voltage Operating in the Voltage Controlled Mode

![Diagram of voltage operating in the voltage controlled mode]

### Table 4.9

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>200</td>
<td>400</td>
</tr>
</tbody>
</table>

### Figures 5 - Noise Deviation Test Circuit and Waveform

![Diagram of noise deviation test circuit and waveform]

### Text:

**NOTE:** Any frequency deviation caused by the signal generator and MC1648B supply should be determined and maintained prior to testing.
TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE
USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^\circ$C

**FIGURE 6**

![Graph and Circuit Diagram]

**FIGURE 7**

![Graph and Circuit Diagram]

**FIGURE 8**

![Graph and Circuit Diagram]
Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figure 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, B). Typical Figure 7 illustrates the oscillator operating in a voltage controlled mode when the output frequency range limit is 10. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to prevent the varactor diode from becoming forward biased. The larger-value resistor (10 kΩ) in Figure 8 is required to provide operation for the high-impedance functions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

\[ f_{\text{max}} = \sqrt{\frac{C_B f_{\text{max}}}{C_D}} \]
\[ f_{\text{min}} = \sqrt{\frac{C_B f_{\text{min}}}{C_D}} \]

where \( f_{\text{max}} \) is the maximum frequency, \( f_{\text{min}} \) is the minimum frequency, \( C_B \) is the capacitance as a function of bias voltage, and \( C_D \) is the short circuit capacitance (input plus external capacitance).

Good RF and low-frequency switching is necessary on the power supply pins. (See Figure 2.)

Capacitors C1 and C2 of Figure 4 should be used to bypass the AGC point and the VCO input transistor dielectric, guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. As high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is used from the AGC point to the most negative power supply potential (ground). If a 5.0 volt supply is used, -5.2 volts is used if a negative voltage is used as shown in Figure 10. At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to drive the sine wave at the output of the MC1648. This is accomplished by using a series resistor (1 kΩ minimum) from the AGC to the most positive power supply potential (ground) if a 5.0 volt supply is used). Figure 11 illustrates this principle.

Applications Information

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer uselful in tuners for FM broadcast, general aviation, marine and hammobile communications, amateur and CB receivers. The system operates from a single +5.0 volt supply, and requires no internal transistors, since all components are monolithic.

Frequency generation of this type offers the advantages of single crystal operation, simple circuitry, and employment of special circuitry to prevent harmonic buildup. Additional features include digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter, \( f_{\text{out}} = f_{\text{ref}} \). The channel spacing is equal to frequency (100 kHz).

For additional information on applications and designs for phase locked loops and digital frequency synthesizers, see Moteurs Applications Notes AN522A, AN523, AN553, AN 564, and AN586.
Figure 9 shows the MC1548 operating from a ±5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added to the AGC output from 5 to VCC.

Figure 10 shows the MC1548 in the variable frequency mode operating from a ±5.0 Vdc supply. To extend the useful range of the device (minimum square wave output above 175 kHz), a resistor is added to the AGC output at pin 5 (13 kΩ minimum).

Figure 11 shows the MC1548 operating from ±5.0 Vdc and ±9 Vsupply pair power supplies. This permits a higher output power and higher output power than is possible from the MECL output (pin 23). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The ideal collector load includes R in parallel with Rp at L1 and C1 at resonant. The optimum value for R at 100 MHz is approximately 250 ohms.

Figure 12 shows the MC1548 square wave output (pin 1).
FIGURE 12 - CIRCUIT USED FOR COLLECTOR OUTPUT OPERATION

FIGURE 13 - POWER OUTPUT vs COLLECTOR LOAD
See the circuit, Figure 12. T = 100 kHz
C3 = 30 - 250 nF
Collector Tank
L1 = 0.22 mH
C1 = 10 - 100 nF
R = 5025 ± 10%
Rg of C1 and C5 = 116 Ω @ 100 kHz Resonance
Output Tank
L2 = 4 turns 470 mH G 2/16 - 10
C5 = 10 - 70 nF

FIGURE 14 - POWER OUTPUT vs COLLECTOR LOAD
See the circuit, Figure 12. T = 10 MHz
C3 = 470 nF
Collector Tank
L1 = 0.2 mH
C1 = 26 - 200 nF
R = 5025 ± 10%
Rg of C1 and C5 = 116 Ω @ 10 MHz Resonance
Output Tank
L2 = 7.2 mH
C5 = 10 - 150 nF
TYPES TL080 THRU TL085, TL086A THRU TL084A
TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- Low-Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonics Distortion...<0.003% TYP

TL080, TL084
JE OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

TL081, TL081A, TL081B
JE OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

TL082, TL082A, TL082B
JE OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

OPERATIONAL AMPLIFIERS

DEVICE TYPES, SUPPLY VOLTAGES, AND PACKAGES

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Supply Voltage</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL080</td>
<td>±5 V</td>
<td>JE</td>
</tr>
<tr>
<td>TL081</td>
<td>±5 V</td>
<td>JE</td>
</tr>
<tr>
<td>TL082</td>
<td>±5 V</td>
<td>JE</td>
</tr>
<tr>
<td>TL083</td>
<td>±5 V</td>
<td>JE</td>
</tr>
<tr>
<td>TL084</td>
<td>±5 V</td>
<td>JE</td>
</tr>
<tr>
<td>TL085</td>
<td>±5 V</td>
<td>JE</td>
</tr>
</tbody>
</table>

*These corrections are not derived to the order sheet.

Copyright © 1983 by Texas Instruments Incorporated
TYPES TL080 THRU TL088, TL089A THRU TL094A
TL0810, TL0820, TL0840
JFET-INPUT OPERATIONAL AMPLIFIERS

TL083A, TL083B
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

TL084A, TL084B
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

Rows 8 and 12 are internally interconnected

TL083A, TL083B
CHP CARRIER PACKAGE
(TOP VIEW)

TL084A, TL084B
CHP CARRIER PACKAGE
(TOP VIEW)

Operational Amplifiers

Symbols

Texas Instruments
FOR OFFICE USE ONLY • DALLAS, TEXAS 75201
**TYPES TLO80 THRU TLO85, TLO80A THRU TLO84A**  
TLO81B, TLO82B, TLO84B  
**JFET-INPUT OPERATIONAL AMPLIFIERS**

**Description**

The TLO8_ JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TLO8_ family.

Device types with an "M" suffix are characterized for operation over the full military temperature range of -55°C to 125°C, those with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

**Schematic (each amplifier)**

![Schematic Diagram](image)

**Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

<table>
<thead>
<tr>
<th></th>
<th>TLO80-M</th>
<th>TLO80-I</th>
<th>TLO80-AC</th>
<th>TLO80-BC</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, VCC</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
</tr>
<tr>
<td>Supply voltage, VEE</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
</tr>
<tr>
<td>Differential input voltage (see Note 1)</td>
<td>±30 V</td>
<td>±30 V</td>
<td>±30 V</td>
<td>±30 V</td>
<td>±30 V</td>
</tr>
<tr>
<td>Input voltage (see Notes 1 and 3)</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±18 V</td>
</tr>
<tr>
<td>Continuous power dissipation at 25°C free-air temperature (see Note 5)</td>
<td>680 mW</td>
<td>680 mW</td>
<td>680 mW</td>
<td>680 mW</td>
<td>680 mW</td>
</tr>
<tr>
<td>Operating free-air temperature range</td>
<td>-25°C to 125°C</td>
<td>-25°C to 85°C</td>
<td>0°C to 70°C</td>
<td>0°C to 70°C</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>Voltage temperature range</td>
<td>-66°C to 150°C</td>
<td>-65°C to 150°C</td>
<td>-65°C to 150°C</td>
<td>-65°C to 150°C</td>
<td>-65°C to 150°C</td>
</tr>
<tr>
<td>Load temperature 1.0 mm 1/16 inch from case for 60 seconds</td>
<td>±90°C</td>
<td>±90°C</td>
<td>±90°C</td>
<td>±90°C</td>
<td>±90°C</td>
</tr>
<tr>
<td>Load temperature 1.0 mm 1/16 inch from case for 10 seconds</td>
<td>±80°C</td>
<td>±80°C</td>
<td>±80°C</td>
<td>±80°C</td>
<td>±80°C</td>
</tr>
</tbody>
</table>

**Notes:**
1. All voltage values, except differential voltages, are with respect to the negative terminal VCC-, and VEE-.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitudes of the input voltage must never exceed the magnitudes of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltage must be limited so that the junction temperature is not exceeded.
5. An overvoltage test at 25°C free-air temperature, other than Overvoltage Ratings C in Section 2 in the JFET-INPUT amplifier, TLO80_M types are also measured. TLO80-I, TLO80-C, TLO80-AC, and TLO80-BC types are gross measured.

---

**Texas Instruments**  
POST OFFICE BOX 202824, DALLAS, TEXAS 75220
## Types TL080M, TL081M, TL082M, TL083M, TL084M

### Low-Noise JFET-Input Operational Amplifiers

Electrical Characteristics. \( V_{CC} = \pm 15 \) V (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>TL080M</th>
<th>TL081M</th>
<th>TL082M</th>
<th>TL083M</th>
<th>TL084M</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DD} ) input offset voltage</td>
<td>( V_{DD} = 0 )</td>
<td>( T_A = 25^\circ C )</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DD} ) output voltage</td>
<td>( V_{DD} = 0 )</td>
<td>( T_A = 25^\circ C )</td>
<td>( T_A = -55^\circ C ) to ( 125^\circ C )</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input current ( I_{IN} )</td>
<td>( V_{DD} = 0 )</td>
<td>( T_A = 25^\circ C )</td>
<td>( T_A = 50^\circ C ) to ( 125^\circ C )</td>
<td>( I_{IN} )</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input bias current ( I_{B} )</td>
<td>( V_{DD} = 0 )</td>
<td>( T_A = 25^\circ C )</td>
<td>( T_A = -55^\circ C ) to ( 125^\circ C )</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-mode input voltage range</td>
<td>( T_A = 25^\circ C )</td>
<td>( V_{CM} )</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-mode rejection ratio</td>
<td>( V_{CM} = V_{DD} ), ( V_{IN} = 0 )</td>
<td>( T_A = 25^\circ C )</td>
<td>80</td>
<td>80</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew rate</td>
<td>( V_{DD} = \pm 15 ) V</td>
<td>( T_A = 25^\circ C )</td>
<td>80</td>
<td>80</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply current</td>
<td>( V_{DD} = \pm 15 ) V</td>
<td>( T_A = 25^\circ C )</td>
<td>1.4</td>
<td>2.5</td>
<td>1.4</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply current ( I_{PS} )</td>
<td>( V_{DD} = 0 )</td>
<td>( T_A = 25^\circ C )</td>
<td>120</td>
<td>120</td>
<td>120</td>
<td>120</td>
</tr>
</tbody>
</table>

1 All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

- Input bias currents of a JFET-input operational amplifier are normal operating reverse currents, which are temperature dependent as shown in Figure 16. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.
<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
<th>Voltage</th>
<th>Current</th>
<th>Power</th>
<th>Gain Factor</th>
<th>Stability</th>
<th>Output</th>
<th>Linearity</th>
<th>Frequency</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLO60</td>
<td>Low Power, High Gain</td>
<td>-4 to 5 V</td>
<td>10 mA</td>
<td>1 W</td>
<td>1000</td>
<td>+/-2%</td>
<td>+/-1%</td>
<td>+/-0.1%</td>
<td>10 kHz</td>
<td>80°C to 125°C</td>
</tr>
<tr>
<td>TLO61</td>
<td>High Power, Low Gain</td>
<td>-12 to 15 V</td>
<td>50 mA</td>
<td>5 W</td>
<td>10</td>
<td>+/-1%</td>
<td>+/-2%</td>
<td>+/-0.5%</td>
<td>20 kHz</td>
<td>70°C to 125°C</td>
</tr>
<tr>
<td>TLO62</td>
<td>Ultra-High Power</td>
<td>-24 to 30 V</td>
<td>100 mA</td>
<td>10 W</td>
<td>1</td>
<td>+/-3%</td>
<td>+/-3%</td>
<td>+/-1%</td>
<td>30 kHz</td>
<td>55°C to 125°C</td>
</tr>
</tbody>
</table>

Note: All specifications are for room temperature unless otherwise stated.
TYPES TLO98 THRU TLO05, TLO00A THRU TLO04A 
TLO01B, TLO02B, TLO04B 
JFET-INPUT OPERATIONAL AMPLIFIERS

Operating characteristics, VCC = ±15 V, TA = 25°C

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>GB</td>
<td>V1 = 10 V, A1 = 2 KΩ</td>
<td>0</td>
<td>10</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>R1</td>
<td>C1 = 100 µF</td>
<td>0.1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Feedback factor</td>
<td>C1 = 100 µF</td>
<td>15%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VS</td>
<td>Rg = 100 KΩ</td>
<td>1</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>0.5s</td>
<td>Rg = 100 KΩ</td>
<td>1</td>
<td></td>
<td>4</td>
<td>µA</td>
</tr>
<tr>
<td>ThD</td>
<td>Vg, Vm = 10 V, Rg = 1 KΩ</td>
<td>0.01</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

PARAMETER MEASUREMENT INFORMATION

![Operational Amplifiers](image)

FIGURE 1-UNITY GAIN AMPLIFIER  FIGURE 3-GAIN OF 10 INVERTING AMPLIFIER  FIGURE 4-FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

![Input Offset Voltage Null Circuits](image)
TYPICAL CHARACTERISTICS

FIGURE 6
FIGURE 7
FIGURE 8
FIGURE 9
FIGURE 10
FIGURE 11
FIGURE 12
FIGURE 13
FIGURE 14

1 Values at high carrier temperatures are applicable only within the recommended output temperature ranges of the various devices. A '3' of compensation extension is used with TLO60 and TLO604A.

TEXAS INSTRUMENTS

POST OFFICE BOX 655040, DALLAS, TEXAS 75265
TYPES TL080 THRU TL085, TL080A THRU TL084A
TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

FIGURE 16
INPUT BIAS CURRENT
FREE AIR TEMPERATURE

FIGURE 17
OUTPUT VOLTAGE
CLAMPED TEMPERATURE

FIGURE 18
COMMON-MODE REJECTION RATIO
FREE AIR TEMPERATURE

FIGURE 19
SLOPE IN NONLINEAR VOLTAGE
FREE AIR TEMPERATURE

FIGURE 20
TOTAL HARMONIC DISTORTION
FREE AIR TEMPERATURE

1Data at high and low temperature are applicable only within the rated operating temperature range of the various devices. A 12°F temperature span is used with TL082 and TL083A.

TEXAS INSTRUMENTS
POST OFFICE BOX 2896 - DALLAS, TEXAS 75260
## F100107
Quint Exclusive OR/NOR Gate

### Description
The F100107 is a monolithic quint exclusive-OR/NOR gate. The function output is the wire-OR of all five exclusive-OR outputs: \( F = (D_{1}\oplus D_{2}) + (D_{10}\oplus D_{20}) + (D_{11}\oplus D_{21}) + (D_{12}\oplus D_{22}) + (D_{13}\oplus D_{23}) \)

### Pin Names
- **Dna - Dne**: Data Inputs
- **F**: Function Input
- **Qa - Qe**: Data Outputs
- **Qa\,\,Qe**: Complementary Data Outputs

### Logic Symbol
![Logic Symbol](image)

### Connection Diagrams
#### 24-Pin DIP (Top View)
![24-Pin DIP Diagram](image)

#### 24-Pin Flatpak (Top View)
![24-Pin Flatpak Diagram](image)

### Ordering Information
See Section 5:

<table>
<thead>
<tr>
<th>Package</th>
<th>Outline</th>
<th>Order Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic DIP</td>
<td>6Y</td>
<td>DC</td>
</tr>
<tr>
<td>Flatpak</td>
<td>4V</td>
<td>FC</td>
</tr>
</tbody>
</table>

---

142
### DC Characteristics: \( V_{EE} = -4.2 \text{ V to } -4.8 \text{ V} \) unless otherwise specified. \( V_{CC} = V_{CCCA} = \text{GND}, \; T_C = 0^\circ\text{C to } -85^\circ\text{C} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{IH} )</td>
<td>Input High Current ( D_{2a} - D_{2e} )</td>
<td>-250</td>
<td></td>
<td></td>
<td>( \mu A )</td>
<td>( V_{IH} = V_{IH(\text{max})} )</td>
</tr>
<tr>
<td>( I_{IEE} )</td>
<td>Power Supply Current</td>
<td>-96</td>
<td>-66</td>
<td>-48</td>
<td>mA</td>
<td>inputs Open</td>
</tr>
</tbody>
</table>

#### Ceramic Dual In-line Package AC Characteristics: \( V_{EE} = -4.2 \text{ V to } -4.8 \text{ V}, \; V_{CC} = V_{CCCA} = \text{GND} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>( T_C = 0^\circ\text{C} )</th>
<th>( T_C = +25^\circ\text{C} )</th>
<th>( T_C = -85^\circ\text{C} )</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay ( D_{2a} - D_{2e} ) to 0, ( \overline{0} )</td>
<td>0.55</td>
<td>0.55</td>
<td>1.80</td>
<td></td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay ( D_{1a} - D_{1e} ) to 0, ( \overline{0} )</td>
<td>0.55</td>
<td>0.55</td>
<td>1.60</td>
<td></td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay Data to ( F )</td>
<td>1.15</td>
<td>2.75</td>
<td>1.15</td>
<td></td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Transition Time 20% to 80%, 80% to 20%</td>
<td>0.45</td>
<td>1.80</td>
<td>0.45</td>
<td></td>
</tr>
</tbody>
</table>

#### Flatpak AC Characteristics: \( V_{EE} = -4.2 \text{ V to } -4.8 \text{ V}, \; V_{CC} = V_{CCCA} = \text{GND} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>( T_C = 0^\circ\text{C} )</th>
<th>( T_C = -25^\circ\text{C} )</th>
<th>( T_C = -85^\circ\text{C} )</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay ( D_{2a} - D_{2e} ) to 0, ( \overline{0} )</td>
<td>0.55</td>
<td>0.55</td>
<td>1.60</td>
<td></td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay ( D_{1a} - D_{1e} ) to 0, ( \overline{0} )</td>
<td>0.55</td>
<td>0.55</td>
<td>1.40</td>
<td></td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay Data to ( F )</td>
<td>1.15</td>
<td>2.55</td>
<td>1.15</td>
<td></td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Transition Time 20% to 80%, 80% to 20%</td>
<td>0.45</td>
<td>1.70</td>
<td>0.45</td>
<td></td>
</tr>
</tbody>
</table>

*See family characteristics for timing dc specifications*
Fig. 1  AC Test Circuit

Notes
Vcc: VCCA = +2 V, VEE = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
Ry = 50 Ω terminator external to scope
Decoupling 0.1 μF from GND to Vcc and VEE
All unused outputs are loaded with 50 Ω to GND
Cf = Fixture and stray capacitance ≤ 3 pF

Fig. 2  Propagation Delay and Transition Times