A COMPARISON OF $\pi/4$-DQPSK MODEMS FOR USE IN A RURAL WIRELESS INTERNET ACCESS SYSTEM

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Abstract

Currently, rural residents are not well served by existing Internet access options. Their primary option is the standard telephone modem, which does not allow for high speed access.

A wireless Internet access solution has advantages over its wired counterpart, since it is cost-effective to deploy the system in sparsely populated areas. Telecommunications Research Laboratories has proposed a multipoint communication system (MCS) as a solution for rural network access. This thesis discusses radio modem solutions that are suitable for such a system.

The $\pi/4$-differential quadrature phase shift keying ($\pi/4$-DQPSK) modulation scheme is used in the radio link of the system. This type of modulation allows three different types of detection: the baseband differential detector, the IF differential detector, and the frequency discriminator detector. These types of detectors have been assumed to have identical theoretical performance under ideal conditions in the existing literature. Little comparison has been performed that considers the effects of practical implementation issues on modem performance and implementation complexity.

Practical impairments present in systems of this type are presented. These impairments include frequency offset, symbol timing offset, DC offset, phase imbalance, sub-optimal receiver filtering, hard-limiting effects, and frequency converter phase noise. Various detector implementations are simulated and the effect of the impairments on bit error rate (BER) performance for the different types of detectors is compared. Most impairments produce similar results in the detectors, but some discrepancies are noted.

The detectors lend themselves to digital hardware implementation. Digital hardware realizations and their simulated BER performance are discussed for each detector type. The relative implementation complexity and the trade-offs between performance and complexity are discussed in terms of implementation in Altera Flex10K Complex Programmable Logic Devices (CPLD). The sensitivity of the BER

performance to impairments is also discussed.

For the proposed system, the baseband differential detector is the best solution since it results in the smallest hardware realization, while also achieving the best BER performance. The IF differential detector is similar in implementation size to the baseband differential detector, but has poorer BER performance. The frequency discriminator detector is not well suited to a digital realization, which results in poor BER performance and a greater implementation complexity.

The most hardware intensive component of the detectors is the root raised cosine (RRC) filter. Replacing the RRC filters with analog Butterworth filters simplifies the detector realizations, but introduces BER performance degradation. A transmitter phase compensation technique is presented that improves the BER performance of a modem that uses sub-optimal detector filtering, while significantly reducing the detector complexity.

Acknowledgements

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Thanks is extended to SED Systems for financial assistance, as well as for providing the opportunity to take a sabbatical to complete this thesis work.

I would also like to thank my parents and immediate family for their support throughout this project.

Last, but certainly not least, I would like to thank my wife, Tracey, for her support, encouragement, love, and patience that has allowed me to complete my graduate program.

Dedication

To my lovely wife, Tracey, who has sacrificed so much so that I could complete this thesis!

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List of Abbreviations

ADS	Advanced Design System
ADSL	Asymmetric Digital Subscriber Line
AFC	Automatic frequency control
AGC	Automatic gain control
AM	Amplitude modulation
AMPS	American Mobile Phone Service
AWGN	Additive white Gaussian noise
BER	Bit error ratio
BPSK	Binary phase shift keying
CDMA	Code Division Multiple Access
CPLD	Complex Programmable Logic Device
CRBB	Constant rate baseband differential detector
CW	Continuous wave
DARPA	Defense Advanced Research Projects Agency
DC	Direct current
DQPSK	Differential quadrature phase shift keying
DRBB	Decimated rate baseband differential detector
FIR	Finite impulse response
FM	Frequency modulation
FPGA	Field Programmable Gate Array
FRC	Full raised cosine
FWA	Fixed wireless access
GMSK	Gaussian minimum shift keying
HP	Hewlett-Packard

HPA	High power amplifier
HTTP	Hypertext Transport Protocol
I	Inphase
IF	Intermediate frequency
IIR	Infinite impulse response
IP	Internet Protocol
ISDN	Integrated Services Digital Network
JDC	Japanese Digital Cellular
LAN	Local area network
LC	Logic cell
LDI	Limit-discriminate-integrate
LNA	Low noise amplifier
LO	Local oscillator
LOS	Line of sight
MCS	Multipoint communications system
NRZ	Non-return to zero
PA	Power amplifier
PLL	Phase locked loop
PM	Phase modulation
ppm	Parts per million
Q	Quadrature
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
RRC	Square root raised cosine
SAW	Surface acoustic wave
SNR	Signal to noise ratio
TDMA	Time division multiple access
WWW	World Wide Web

Chapter 1

INTRODUCTION

1.1 Background

1.1.1 Wireless Communications

Wireless communications is now over 100 years old [1]. From the early discoveries of Hertz and Marconi, wireless communications has now managed to fulfill its promise to connect distant people with commonplace communication devices [2, 3].

Wireless communications was not immediately embraced by the mainstream population. Throughout the early part of the century, the main user of wireless communications was the military for ship to shore communication. Additional wireless applications were found with the arrival of the space age, as satellite communications began to play a larger role in telephony [1].

The public began to embrace wireless communications with the advent of the modern cellular telephone. Wireless phone systems have been available since the early part of the 20th century, but did not immediately become popular due to their high subscriber cost and low reliability. The first national cellular public radio telephone system, known as the American Mobile Phone Service (AMPS), was introduced in the United States in 1979 [4]. This system uses analog FM technology. Second generation cellular phone systems use digital communication techniques to further improve the quality of cellular telephone communications.

Due to the popularity of the cellular telephone and pagers, wireless communications is ubiquitous in the developed world as the 20th century concludes.

1.1.2 Development of the Internet

The Internet started out as a United States Defense Advanced Research Projects Agency (DARPA) research project in 1967 and was originally called the ARPANET [5]. Originally, this network linked only a handful of educational and military institutions in the United States for the purpose of sharing information.

The ARPANET slowly evolved into what we know now as the Internet. As more and more universities and private enterprises joined the network, the ARPANET was removed from military control and became administered by civilian agencies.

The widespread development of personal computers and workstations propelled the development of local area networks (LAN), as well as the Internet. The Hypertext Transport Protocol (HTTP) was developed in 1992 and has become the common protocol used in the world wide web (WWW). This development allowed common people to use the Internet to easily exchange information, causing explosive growth in the use of the Internet [5].

1.2 High-Speed Wireless Rural Internet Access System

Currently, most Internet access from consumer homes is through wired technologies, such as telephone lines and cable television lines. This section describes an application in which a wireless Internet access method has advantages over its wired counterparts. This thesis work is based on the assumptions of the system application described in this section.

City dwellers have many high speed Internet access options available to them. These options include cable modems, asymmetric digital subscriber lines (ADSL), and integrated services digital network (ISDN) lines. All these technologies are based on cables and wires connected to the subscribers' homes. Due to the high cost of implementing wired systems, it is not economically feasible to provide these services in sparsely populated areas. To fill this void, TRLabs in Saskatoon, SK,

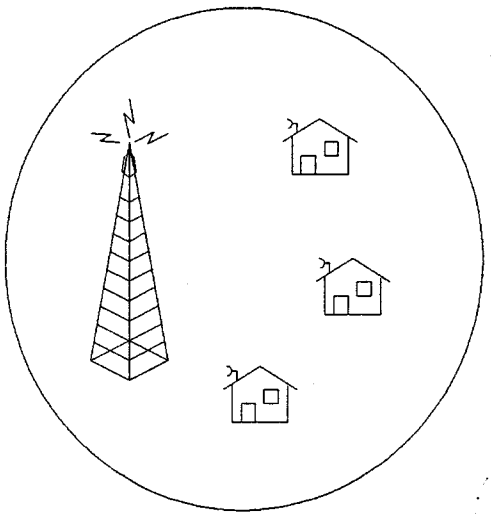


Figure 1.1: Architecture of a system cell

Canada has begun development on a wireless Internet access system to provide high speed data services to rural customers. The objective of the system is to provide a data access service that is applicable for current and future multimedia applications. The system must be cost-effective, with a low capital investment required for the radio hardware at the remote rural sites.

The system is a two-way multipoint communication system (MCS), configured in a point to multipoint arrangement. The system is arranged in a cellular architecture, with a maximum cell diameter of 30 km. Figure 1.1 shows a single cell of the system. Each cell contains a hub radio that is likely installed at an existing cellular tower. This hub coordinates access to all the remote subscriber sites located within the cell and is connected to a high bandwidth link that completes the connection to the Internet. At the remote sites, the radio provides a standard Ethernet interface for connection to a computer or IP phone equipment.

A common frequency channel is used between the hub and the remote sites. The forward channel (from the remote sites to the hub) is a time division shared channel. The hub also shares this common channel for the communication on the reverse channel to the remote sites. The hub coordinates access to the channel using a token passing protocol that prevents more than one user from simultaneously accessing the radio channel.

The system is designed to operate in the 3400-3700 MHz frequency band. This frequency spectrum has recently been designated by Industry Canada for fixed wireless access (FWA) systems in rural areas [6]. The system has been designed to use low transmit power levels (1 W or less) and small directional antennas to provide data rates on the order of 2 Mbps for each radio channel.

The $\pi/4$-DQPSK modulation scheme was chosen for this application since it meets the system objective for a simple receiver with adequate performance. The modulation scheme provides reasonable spectral efficiency (1.6 bps/Hz typical) and power efficiency (bit energy to noise level, $E_b/N_o = 12$ dB, at a bit error ratio of 10^{-5}). In addition, this modulation scheme can be detected noncoherently, which allows simple, low cost receivers to be used at the remote rural sites. Noncoherent detection also allows rapid demodulator synchronization in the burst mode shared channel since long preambles are not required, which increases system data throughput.

The system can provide reasonable data rates for up to 200 users per channel. In addition, the system is designed to be scalable. If additional capacity is needed in a particular cell, additional channels can be added to supply the extra capacity. However, in sparsely populated areas, a single channel may be sufficient to provide service. This scalable architecture allows the system to be deployed incrementally as subscriber demand for the service grows.

1.3 Research Motivation

The initial motivation for this research was to investigate a radio modem suitable for use in the wireless rural Internet access system described in Section 1.2. The main criteria in this selection process was to find a modem with suitable performance that was both low-cost and simple to build.

Preliminary investigation showed that a radio modem using $\pi/4$-DQPSK modulation met the requirements for the system. This modulation scheme is popular in wireless communications since its performance is good in terms of spectral and power

efficiency. This modulation scheme also offers three different methods of detection which provides a designer with options in the receiver implementation.

The three standard types of $\pi/4$-DQPSK detectors are the IF differential detector, frequency discriminator detector, and baseband differential detector. Previous research has proven that these three different types of detectors are mathematically equivalent [7]. However, these articles assume ideal detector characteristics that neglect the real-world impairments and the hardware complexity associated with the implementation.

The focus of this thesis is to investigate the performance of the three $\pi/4$-DQPSK detector types, taking into account real-world implementation details. The initial hypothesis was that practical considerations would cause the detectors to exhibit differences in performance and complexity. Each of the three standard detector types was included to determine which modem type was the most suitable for this wireless application.

1.4 Research Objectives

There were four main objectives in this research work. The first objective was to research the different detection methods for the $\pi/4$-DQPSK modulation scheme and to review the previous literature associated with these detectors.

The second objective was to compare the performance of the IF differential detector, baseband differential detector, and frequency discriminator detector through simulation. A number of common impairments were selected for investigation. Each impairment was isolated to investigate the effect on the detector performance. Also, the sensitivity of the detector performance to the degree of these impairments was determined. This allows a system designer to specify modem components based on the impairment sensitivity, while insuring that the overall impairment degradation meets the system requirements.

The third objective was to propose compensation techniques (where applicable) for the effects of the impairments present in the modem. Investigation was required

to determine appropriate compensation techniques to increase the modem performance, while under the effect of the impairment.

The fourth and final objective was to design the three detector types in digital hardware with the synthesized design suitable for implementation in a digital hardware device. The designed modems were to be compared on the basis of their implementation complexity, as well as their BER performance and sensitivity to impairments. The trade-offs between complexity and performance were to be investigated.

1.5 Literature Review

The $\pi/4$-DQPSK modulation scheme was first proposed by Baker in 1962 for data transmission over telephone lines [8]. Ten years later it was recognized that this modulation scheme was also suitable for mobile wireless digital communications [9]. As modulation schemes were considered for second generation digital cellular communications, $\pi/4$-DQPSK became a subject of active research in the late 1980s and early 1990s.

An overview of the modulation scheme is presented by Feher [7]. Due to the common usage of the modulation type, descriptions of the modulation type, in the context of cellular systems, can now also be found in a number of textbooks [10, 11, 12].

A thorough summary of the existing literature on $\pi/4$-DQPSK, up to the time of the article, is presented by Feher [7]. This article, as well as others, discuss the ideal transmitter model for $\pi/4$-DQPSK and introduce the three standard detection methods for the modulation scheme [13]. The frequency discriminator detection method was introduced by Akaiwa and Nagata [14]. The other detector models were derived from standard differential detection techniques. The equivalence of the three detectors is proven mathematically and demonstrated through simulation results [13, 15, 16].

Noncoherent detection has been studied in the context of a number of channel

impairments, including cochannel interference and various fading conditions [13, 15, 16, 17, 18, 19, 20, 21, 22]. Channel impairments are not considered in this thesis.

The effects of transmitter and receiver impairments were studied in a number of articles. Compensation for frequency offset effects in the frequency discriminator detector were presented by Liu [13]. Modulator nonlinearities and mixer imbalance, in the context of the baseband differential detector, were studied by Wang and Cole [23, 24]. Symbol timing error for baseband differential detectors was investigated by Kiaseleh [25]. The effects of nonlinear transmit amplifiers were demonstrated by Liu and Boccuzzi [26, 27].

The $\pi/4$-DQPSK modulation scheme was eventually chosen by both the North American IS-54 and Japanese digital cellular (JDC) time division multiple access (TDMA) standards. After adoption as a standard, research has diminished in this area. However, the utility of the modulation scheme is well known, so it is often used in industry.

The existing research is deficient in comparing the effects of impairments on the three common detector types. It is important to characterize these effects, so that a communication system designer is able to specify the required tolerances on subsystems and to decide which detector is appropriate for a particular application. It is also valuable to understand the sensitivity of the detector to various impairments that may be tolerated as a trade-off for achieving a simplified hardware solution.

1.6 Thesis Organization

This thesis is organized as follows:

Chapter 1 provides an introduction to this thesis. The research motivation and objectives are discussed. A brief literature review on the topic is presented. The system application which provides the context for the thesis work is introduced.

Chapter 2 discusses basic modulation theory and introduces the details of the $\pi/4$-DQPSK modulation scheme, which is crucial to the understanding of the remainder of this thesis.

Chapter 3 discusses the theory and mathematical derivation of the simulation models used throughout the thesis. The transmitter model and the three detector types used in the receiver are presented. The simulation methodology is also discussed.

Chapter 4 discusses a number of practical impairments encountered in a system of this type. The basis of these impairments is developed and discussed in detail. The BER performance of the detectors, in the presence of the impairments, is characterized.

Chapter 5 presents the design of the demodulators in digital hardware. The demodulator design is presented in detail for each detector type and the simulated BER performance is characterized. In addition, the relative implementation complexity is discussed, as well as the trade-off between performance and complexity.

Chapter 6 summarizes the results of the research and provides future work directives.

Chapter 2

MODULATION THEORY

2.1 Overview

Modulation is the process of encoding the source information onto a bandpass signal with a prescribed carrier frequency [28]. The modulated portion of a signal contains the desired information of the bandpass signal. A modulated signal, $s(t)$, can be expressed mathematically as

$$s(t) = a_m(t)\cos\{2\pi[f_c + f_m(t)]t + \theta_m(t)\} \tag{2.1}$$

where $a_m(t)$ denotes the amplitude modulation, $f_m(t)$ denotes the frequency modulation, and $\theta_m(t)$ denotes the phase modulation of the signal. The bandpass carrier frequency is represented by f_c.

As shown in Equation 2.1, source information can be transmitted by varying the amplitude, frequency, or phase of the signal. Modulation schemes vary one or more of these parameters to encode the desired signal information.

In analog communications, the signal is varied continuously to encode information that is not discrete in nature. The receiver decodes the received signal to retrieve the transmitted information. Common analog modulation schemes include amplitude modulation (AM), frequency modulation (FM), and phase modulation (PM).

Digital communications maps a binary sequence of information signals, $\{a_n\}$, into a set of L discrete waveforms, $\{s_l, l = 1, 2, ..., L\}$. The mapping is generally

performed by taking $k = \log_2 L$ binary digits at a time from the information sequence, where n indicates the information symbol index [29]. This block of k binary digits is mapped deterministically to one of $L = 2^k$ discrete states for transmission. These L states are referred to as symbols in the modulation scheme. Each symbol represents a sequence of k bits.

The binary information sequence arrives at the modulator at a rate R_b bits per second (bps) and is mapped into symbols. The symbols are output at a symbol rate of $R_s = R_b/k$.

2.2 Modulation Scheme Selection Trade-Offs

In order to make efficient use of a communication system, the modulation scheme must be chosen carefully. The main considerations in choosing an effective modulation scheme for an application include spectral efficiency, power efficiency, and fading immunity [10].

2.2.1 Spectral Efficiency

Spectral efficiency describes the ability of a modulation scheme to transmit data within a particular bandwidth [12]. As the data rate increases, the bandwidth of the signal generally increases. However, some modulation schemes perform this relationship better than others. The spectral efficiency, η_s, can be expressed as

$$\eta_s = \frac{R}{B} \quad \text{(bps/Hz)} \tag{2.2}$$

where R denotes the bit rate and B denotes the information signal bandwidth.

The spectral efficiency defines the system capacity for an application, since the available bandwidth is usually limited. This wireless application requires a reasonable spectral efficiency to provide a high data rate to the end users.

2.2.2 Power Efficiency

Power efficiency refers to the ability of a modulation scheme to maintain the fidelity of a digital signal at low power levels. In a digital system, it is necessary to increase the signal power to increase noise immunity. Each modulation scheme requires a different increase in signal power to obtain a certain level of fidelity. Power efficiency, η_p, is often expressed as

$$\eta_p = E_b/N_o, \quad BER = 10^{-5} \tag{2.3}$$

where E_b/N_o denotes the signal energy per bit (E_b) to noise power spectral density (N_o) required at the receiver input for a particular bit error ratio (BER).

In some modulation schemes, like filtered $\pi/4$-DQPSK, the transmit signal amplitude envelope varies. Other modulation schemes, such as FM, have a constant transmit signal envelope. Due to this envelope variation, $\pi/4$-DQPSK transmit amplifiers must operate at a level below the maximum operating point, so that the signal can be linearly amplified.

This application does not require an extremely high power efficiency, compared to mobile communication systems, since the hub and remote transmitters are fixed. The maximum desired system transmit power is limited to 1 W for this application. With this transmit level, a preliminary link budget indicates a sufficient margin to achieve the required signal strength at the receiver while maintaining the desired BER performance.

2.2.3 Fading Immunity

Fading immunity refers to the ability of a modulation scheme to withstand both flat fading conditions and frequency selective fading conditions. In flat fading, the received signal strength changes over time, but the spectral characteristics of the transmitted signal are preserved [12]. The signal strength varies in amplitude due to the fluctuations of the channel gain caused by environmental events. In frequency

selective fading, the received signal amplitude changes over time. In addition, the spectral characteristics of the transmitted signal are not maintained, resulting in time domain dispersion of the information signal. This dispersion causes intersymbol interference in the received signal and leads to higher bit error ratios.

This application should encounter predominantly Rician fading, since the application deals with primarily line of sight (LOS) communication [11]. A 24 dB fade margin has been been predicted for this application to handle the fading. The fade margin should be sufficient, since particularly fast, deep frequency-selective fades as often observed in mobile communication systems should not be encountered, since the receiver and transmitter are both fixed. Field trials will determine whether this fade margin is sufficient.

2.2.4 Comparison of Modulation Schemes

Figure 2.1 displays a summary of the different modulation schemes highlighting their strengths and weaknesses with regard to the particular modulation scheme's characteristics [10]. It can be observed that modulation schemes with high power efficiency (FM, GMSK) are not particularly spectrally efficient. Linear modulation schemes (QAM, QPSK) are increasingly spectrally efficient, but require power amplifiers with nonlinear compensation to achieve power efficiency [12]. In addition, it can be seen that as linear modulation schemes increase in spectral efficiency, the power efficiency decreases.

2.3 Phase Modulation

Digital phase modulation manipulates the phase of a signal in order to encode the desired information sequence. The binary digits are mapped into discrete phases of the carrier. A baseband equivalent representation, $u_l(t)$, of the phase modulated signal can be expressed as

$$u_l(t) = p(t)\exp(j\theta_l), \quad l = 1, 2, \ldots, L \tag{2.4}$$

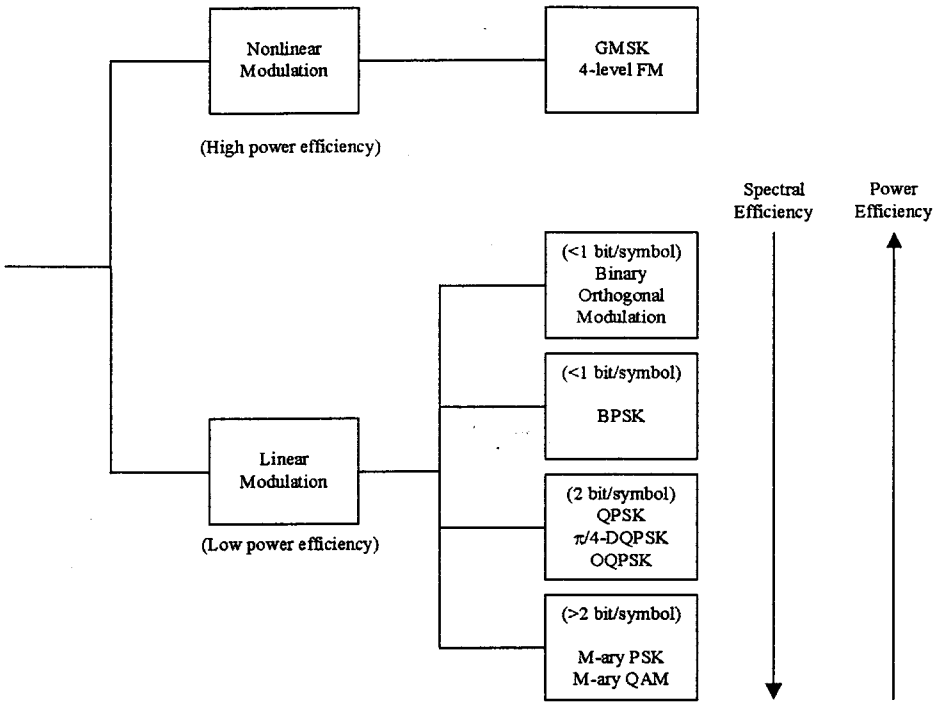


Figure 2.1: Comparison of common digital modulation schemes

where $p(t)$ denotes the pulse shape of the signal, θ_l denotes the discrete phase angle of the signal, and L denotes the number of discrete phases in the symbol set [29]. The amplitude of the signal is defined by the pulse shaping waveform, $p(t)$.

The baseband signal described by Equation 2.4 can be expressed as a bandpass signal, $s_l(t)$, as

$$s_l(t) = Re[u_l(t)\exp(j2\pi f_c t)], \quad l = 1, 2, \ldots, L \tag{2.5}$$

or

$$s_l(t) = p(t)\cos(2\pi f_c t + \theta_l), \quad l = 1, 2, \ldots, L \tag{2.6}$$

where f_c denotes the carrier frequency. The set of discrete phase angles is typically chosen to be equally spaced around a circle and can be expressed as

$$\theta_l = \frac{2\pi}{L}(l-1), \quad l = 1, 2, \ldots, L. \tag{2.7}$$

The bandpass signal, $s_l(t)$, of Equations 2.5 and 2.6 can be expressed equivalently in terms of its quadrature components as

$$s_l(t) = u_I(t)\cos(2\pi f_c t) - u_Q(t)\sin(2\pi f_c t) \tag{2.8}$$

where $u_I(t)$ describes the inphase (I) component of the signal and $u_Q(t)$ denotes the quadrature (Q) component of the signal. The quadrature components, $u_I(t)$ and $u_Q(t)$, are assumed to contain the pulse shaping signal, $p(t)$. These two components are related to the instantaneous phase, $\theta(t)$, as

$$\theta(t) = \tan^{-1}(\frac{u_Q(t)}{u_I(t)}). \tag{2.9}$$

Ideally, the instantaneous phase, $\theta(t)$, maps directly to one of the set of discrete signal phases, θ_l, when sampled at the symbol interval.

The relationship between inphase and quadrature components is often illustrated geometrically in signal state diagrams, sometimes referred to as I-Q constellation diagrams. An example constellation diagram for QPSK is shown in Figure 2.2. As shown in this diagram, the x-axis corresponds to the inphase component and the y-axis displays the quadrature component.

Popular digital phase modulation techniques include binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), and $\pi/4$-QPSK.

The focus of remainder of this chapter will be the quadrature phase shift keying (QPSK) modulation scheme and its variation $\pi/4$-DQPSK, since this is the modulation scheme chosen as the focus for this thesis.

2.4 QPSK Modulation

QPSK is a modulation scheme that transmits two bits of information per symbol, using four discrete phase states. Both absolute phase encoding and differential phase encoding are applicable to QPSK.

Table 2.1 shows the relationship between the information sequence, $\{a_n\}$, and

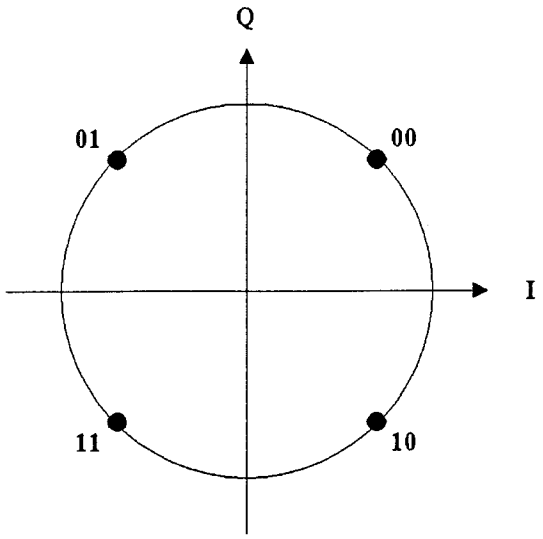


Figure 2.2: Signal state diagram of QPSK

Table 2.1: Relationship of input dibit to phase state for QPSK

Dibit (a_{2n-1}, a_{2n})	*Phase* (θ_n)
00	$\pi/4$
01	$3\pi/4$
10	$-\pi/4$
11	$-3\pi/4$

the assigned phase, θ_n, for absolute phase encoded QPSK. The phase, θ_n, is chosen from the set of discrete phases described in Equation 2.7 for each symbol denoted by the subscript n. Figure 2.2 shows the corresponding signal state diagram. Gray coding is used in the state assignments to limit an adjacent symbol error to a one bit error. If the signal were not Gray coded, an adjacent symbol error could cause a two bit error.

Differentially encoded QPSK is referred to as DQPSK. When differentially encoded, symbols are represented as changes in carrier phase, rather than by the absolute carrier phase. The absolute phase state for the n-th symbol, θ_n, is given by

$$\theta_n = \theta_{n-1} + d\theta_n \tag{2.10}$$

Table 2.2: Relationship of input dibit to phase transition for DQPSK

Dibit (a_{2n-1}, a_{2n})	*Phase Transition* $(d\theta_n)$
00	0
01	$\pi/2$
10	$-\pi/2$
11	π

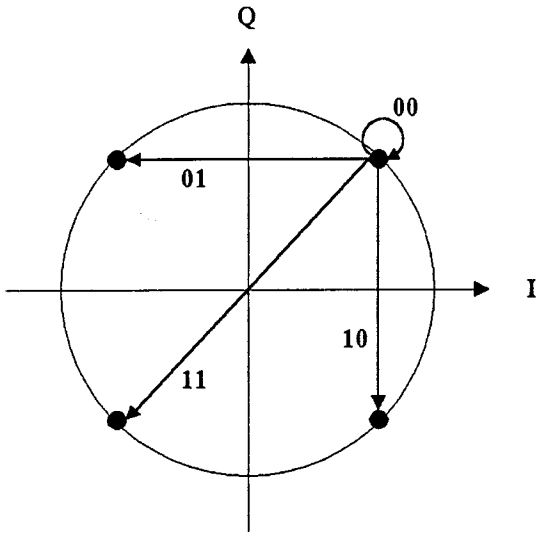


Figure 2.3: Signal state diagram of DQPSK

where $d\theta_n$ denotes the phase transition of the signal and represents the symbol.

Table 2.2 shows the relationship between the information sequence and the assigned differential phase, $d\theta_n$. Figure 2.3 shows the corresponding signal state diagram for an initial phase state, $\theta_{n-1} = \pi/4$. This modulation method has memory, as encoding of the n-th symbol phase requires knowledge of the previous symbol phase.

2.5 $\pi/4$-QPSK Modulation Scheme

The $\pi/4$-QPSK modulation scheme was first described in an article for use in telephone transmission lines [8]. Since then, this modulation scheme has become popular in wireless communication systems. The $\pi/4$-QPSK scheme is a modifica-

Table 2.3: Relationship of input dibit to phase for $\pi/4$-QPSK

	Phase (θ_n)	
Dibit (a_{2n-1}, a_{2n})	$t = nT_s, n$ *even*	$t = nT_s, n$ *odd*
00	$\pi/4$	0
01	$3\pi/4$	$\pi/2$
10	$-\pi/4$	$-\pi/2$
11	$-3\pi/4$	π

tion to the QPSK modulation scheme previously described. Like QPSK, this scheme can be either absolute phase encoded or differentially encoded.

In this modulation scheme, the inphase (I) and quadrature-phase (Q) axes alternate between (0, $\pi/2$) and ($-\pi/4$, $\pi/4$) every symbol period (T_s). Table 2.3 shows the relationship between the information sequence, $\{a_n\}$, and the assigned absolute phase, $\theta_n(t)$. Figure 2.4 shows the corresponding signal state diagram. When time, $t = nT_s$ (n even), the black circles are used to encode the symbol information. At alternate symbol periods, $t = nT_s$ (n odd), the white circles are used.

The main advantage of this modulation scheme is reduced amplitude variation in the modulated signal envelope, since the signal amplitude ideally never goes through the origin (zero amplitude). Therefore, transmit power amplifiers can be operated at higher efficiencies, since the modulated signal is less sensitive to power amplifier nonlinearities. For this reason, this modulation scheme is more popular than regular QPSK in radio systems [11].

2.6 $\pi/4$-DQPSK Modulation Scheme

Like regular QPSK, $\pi/4$-QPSK signals can be differentially encoded. This differential modulation scheme is referred to as $\pi/4$-DQPSK.

When differentially encoded, the absolute phase state for the n-th data symbol, θ_n, of a $\pi/4$-DQPSK modulated signal is given by

$$\theta_n = \theta_{n-1} + d\theta_n \tag{2.11}$$

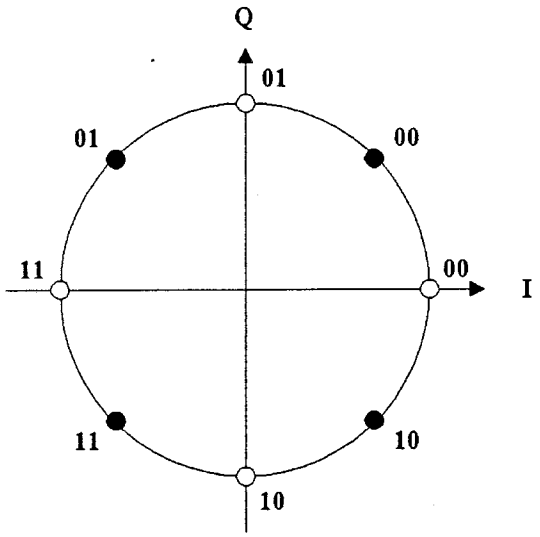


Figure 2.4: Signal state diagram of $\pi/4$-QPSK

Table 2.4: Relationship of input dibit to phase transition for $\pi/4$-DQPSK

Dibit (a_{2n-1}, a_{2n})	*Phase Transition* $(d\theta_n)$
00	$\pi/4$
01	$3\pi/4$
10	$-\pi/4$
11	$-3\pi/4$

where $d\theta_n$ denotes the phase transition of the signal and represents the symbol.

Table 2.4 shows the relationship between the information sequence and the assigned phase transition, $d\theta_n$, defined in Equation 2.11. Figure 2.5 shows the corresponding signal state diagram for an initial phase state, $\theta_{n-1} = \pi/4$.

Unlike the DQPSK modulation scheme, phase shifts are guaranteed between each symbol in $\pi/4$-DQPSK. The phase state always changes by $k\pi/4$ between symbols, where $k = \pm 1, \pm 3$. This is advantageous for symbol timing circuits that require transitions to provide synchronization. In addition, the signal amplitude never goes through zero amplitude, ensuring a relatively small envelope variation.

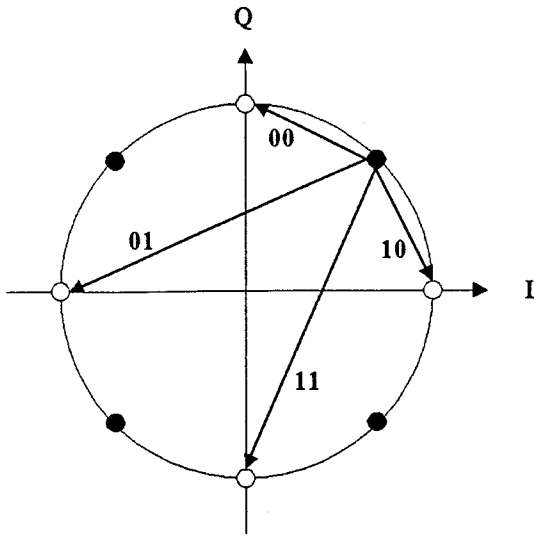


Figure 2.5: Signal state diagram of $\pi/4$-DQPSK

2.6.1 Power Spectral Density and Capacity

The power spectral density of a signal relates the distribution of signal power as a function of frequency. A $\pi/4$-DQPSK signal, with a carrier frequency of 3500 MHz and a data rate of 2 Mbps, is shown in Figure 2.6. The unfiltered digital signal has a $\frac{\sin(x)}{x}$ spectral characteristic that contains significant power well beyond the channel bandwidth. To reduce the adjacent channel interference, the signal must be pre-filtered to limit the transmission bandwidth.

The pre-filtered $\pi/4$-DQPSK signal is also shown in Figure 2.6. The unfiltered signal is filtered by an ideal square root raised cosine filter with a roll-off factor of 0.35. It can be seen that pre-filtering removes the signal sidelobes, which limits the adjacent channel interference.

The filtered power spectral density depends on the roll-off factor and filter characteristic chosen for the pre-filtering. With ideal brick wall filtering, the maximum spectral efficiency that can be achieved with this modulation scheme is 2 bps/Hz. With a typical roll-off factor of 0.35, the spectral efficiency is reduced to 1.62 bps/Hz. More details on the specification and implementation of the pre-filtering for this application is presented in subsequent chapters.

The power spectral density of $\pi/4$-DQPSK is the same as that for QPSK when

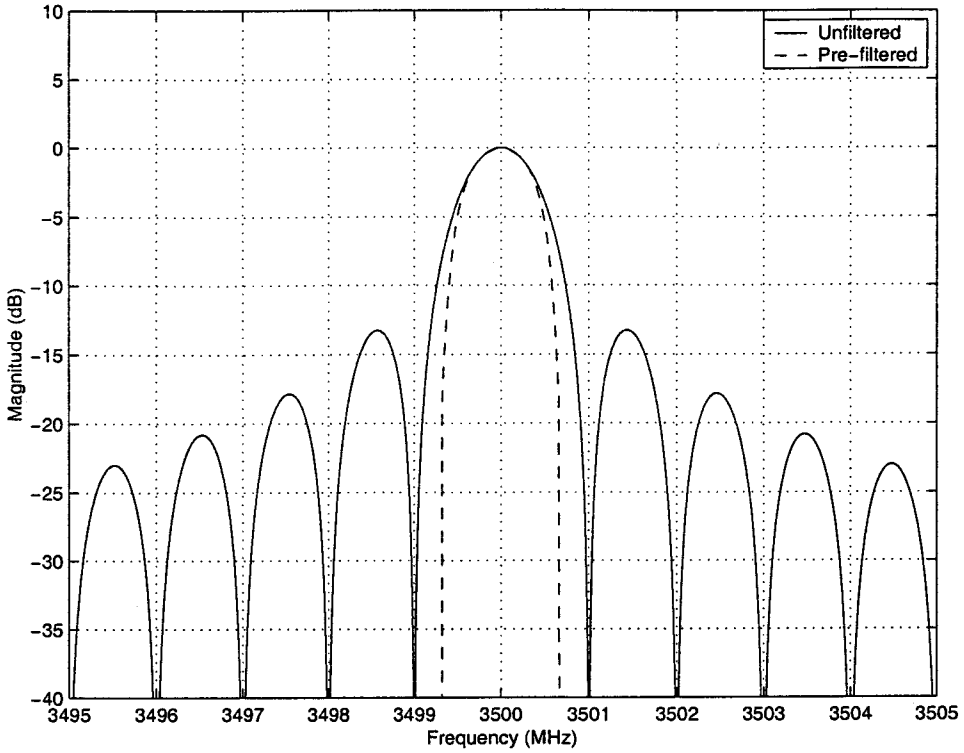


Figure 2.6: Power spectral density of unfiltered and pre-filtered $\pi/4$-DQPSK

the same roll-off factor is used. The spectral efficiency is double that of binary phase shift keying (BPSK) for the same data rate, but is less than the higher order quadrature amplitude modulation (QAM) schemes with eight or more constellation points, since the spectral efficiency is related to the order of the modulation scheme.

The capacity of a system relates directly to the spectral efficiency of the chosen modulation scheme, since it defines the maximum data rate that is possible given the frequency allocations for the application.

2.7 Summary

Modulation encodes source information onto a bandpass signal. Digital phase modulation maps discrete symbols to the phase of a carrier signal. Common digital phase modulation schemes include BPSK, QPSK, and $\pi/4$-QPSK.

Digital phase modulation schemes, like QPSK and $\pi/4$-QPSK, use absolute phase detection to determine the received symbols. $\pi/4$-QPSK reduces the signal envelope

variation, which allows high efficiency power amplifiers to be used in the transmitter.

Differential modulation schemes, such as DQPSK and $\pi/4$-DQPSK, map the phase difference to discrete symbols. Differential modulation schemes suffer a performance penalty relative to absolute detection, but allow a less complicated receiver to be used, as will be shown in later chapters.

The $\pi/4$-DQPSK modulation scheme has an ideal power spectral efficiency of 2 bps/Hz that is reduced to 1.62 bps/Hz when using a RRC filter with a roll-off factor of 0.35. $\pi/4$-DQPSK has a smaller signal envelope variation than DQPSK which allows simpler power amplifiers to be used. Unlike DQPSK, $\pi/4$-DQPSK guarantees signal transitions between symbols, which is advantageous for symbol timing circuitry.

Chapter 3

SIMULATION MODELS

This chapter presents the simulation models used throughout this thesis. The ideal $\pi/4$-DQPSK transmitter and detector models are introduced. In addition, the simulation methodology is presented.

3.1 Transmitter

A radio transmitter is composed primarily of the modulator, which transforms the incoming bit stream for transmission. In addition, the transmitter often contains an upconversion stage and a power amplification stage to prepare the signal for the radio transmission channel. The block diagram of an ideal transmitter is shown in Figure 3.1.

3.1.1 Modulator

The block diagram of an ideal $\pi/4$-DQPSK modulator is shown in Figure 3.2 [13]. The binary serial input data (bits) is divided into two parallel data sequences for the

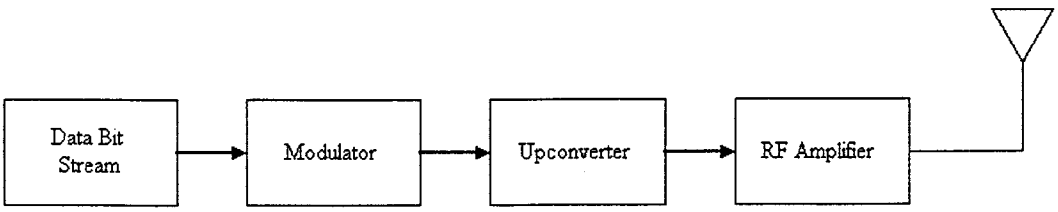


Figure 3.1: Block diagram of an ideal transmitter

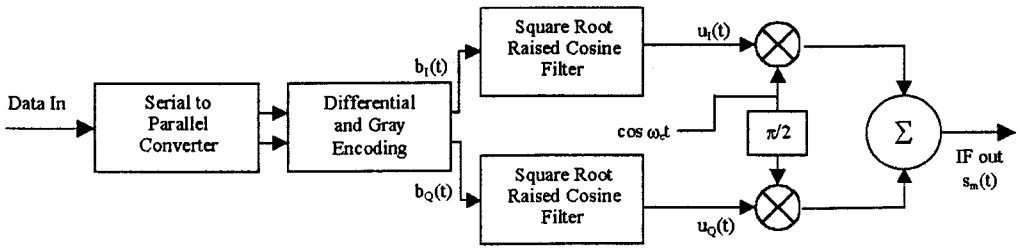


Figure 3.2: Block diagram of an ideal modulator

inphase (I) and quadrature (Q) components of the modulation. After the conversion to a parallel data sequence, the serial to parallel data converter output symbol time, T_s, is twice as long as the original bit time, T_b. These parallel bit streams are Gray coded and differentially encoded, according to the $\pi/4$-DQPSK signal mapping rules described in Table 2.4, to produce the desired transmit symbol. The baseband waveform, $b(t)$, can be expressed as

$$b(t) = b_I(t) + jb_Q(t) \tag{3.1}$$

$$= \sum_{n=-\infty}^{\infty} \cos(\theta_n)\delta(t - nT_s) + j \sum_{n=-\infty}^{\infty} \sin(\theta_n)\delta(t - nT_s) \tag{3.2}$$

where $b_I(t)$ represents the inphase component of the baseband signal, $b_Q(t)$ represents the quadrature component, θ_n describes the phase angle for the n-th symbol based on the coding for the information sequence, and $\delta(t)$ represents Dirac's delta function.

The encoded data streams are filtered to band-limit the signal prior to transmission over the radio frequency (RF) channel. The transmit filtering is optimally performed using a square root raised cosine (RRC) filter with sinc compensation for sampling, when a matched RRC filter is used in the receiver [29].

The frequency response of the RRC filter, which meets Nyquist's criterion for zero intersymbol interference, is shown in Figure 3.3 [30]. Its frequency response,

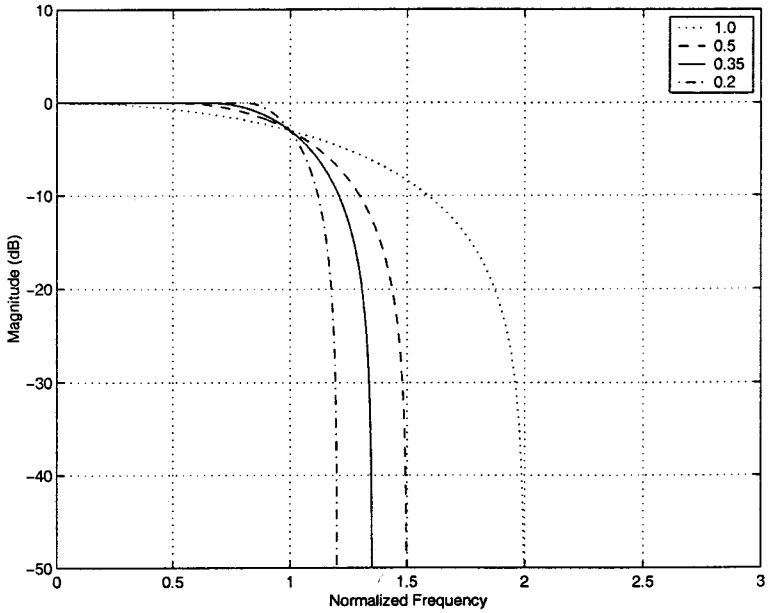


Figure 3.3: Frequency response of the square root raised cosine filter for various roll-off factors

$H_{\mathrm{RRC}}(\omega)$, can be expressed mathematically as

$$H_{\mathrm{RRC}}(\omega) = \begin{cases} 1 & 0 \leq \omega \leq \pi\frac{(1-\alpha)}{2F} \\ \cos(\frac{1}{2F\alpha}(\omega - \pi\frac{(1-\alpha)}{2F})) & \pi\frac{(1-\alpha)}{2F} \leq \omega \leq \pi\frac{(1+\alpha)}{2F} \\ 0 & \omega \geq \pi\frac{(1+\alpha)}{2F} \end{cases} \tag{3.3}$$

where α denotes the roll-off factor of the filter and F is the filter bandwidth. The parameter, α, is often referred to as the excess bandwidth of the filter. It represents a trade-off between the sharpness of the transition band of the filter and the magnitude of the ringing of the impulse response of the filter. Figure 3.3 illustrates the magnitude frequency response for a number of common roll-off factors. The 3-dB bandwidth of the filter, $F = \frac{1}{2T_s}$, is inversely proportional to the symbol period, T_s. The figure frequency is normalized to the symbol rate, $R_s = \frac{1}{T_s}$.

The impulse response of the root raised cosine filter is shown in Figure 3.4 for various values of α. The filter's infinite impulse response has been truncated in the figure. In practical systems, the impulse response is also truncated to realize a synthesizable finite impulse response (FIR) digital filter.

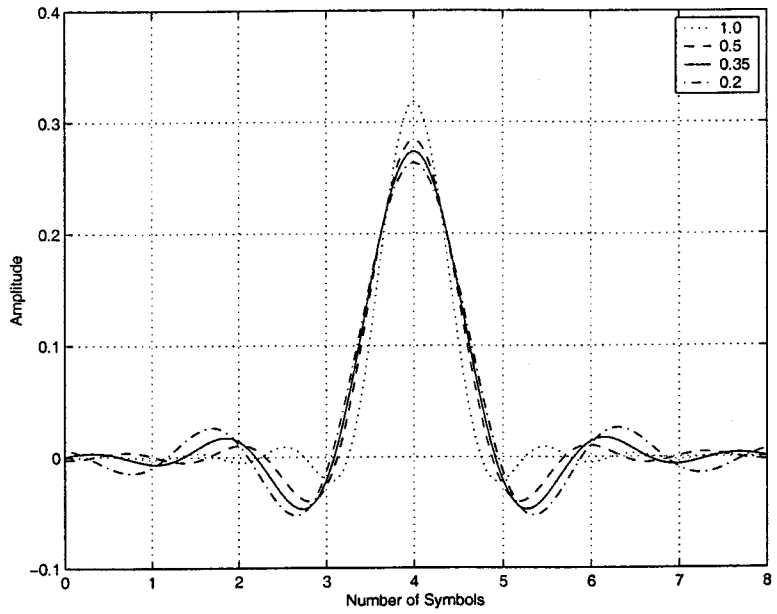


Figure 3.4: Impulse response of the square root raised cosine filter for various roll-off factors

The filter's time response, $h_{\mathrm{RRC}}(t)$, can be expressed mathematically as

$$h_{\mathrm{RRC}}(t) = \frac{1}{\pi t}\frac{1}{1-(\frac{4\alpha t}{T_s})^2}\sin\{2\pi(1-\alpha)\frac{t}{T_s}\} + \frac{1}{\pi}\frac{\frac{4\alpha}{T_s}}{1-(\frac{4\alpha t}{T_s})^2}\cos\{2\pi(1+\alpha)\frac{t}{T_s}\} \tag{3.4}$$

where α denotes the roll-off factor of the filter and T_s is the symbol period [30].

Inverse sinc compensation is added to the root raised cosine filter for simulation purposes. This compensation offsets the effects of the sample and hold operation of the D/A converter. The sinc compensation frequency response, $H_{is}(\omega)$, can be expressed as

$$H_{is}(\omega) = \frac{\frac{\omega}{2F_s}}{\sin(\frac{\omega}{2F_s})} \tag{3.5}$$

and is related to the sampling rate, F_s. The associated time domain signal, $h_{is}(t)$, is the inverse Fourier transform of the frequency response.

After pre-filtering, the baseband signal, $u(t)$, can be expressed in terms of in-

phase, $u_I(t)$, and quadrature, $u_Q(t)$, components as

$$u(t) = u_I(t) + j \cdot u_Q(t) \tag{3.6}$$

$$= b(t) \otimes h_{\mathrm{RRC}}(t) \otimes h_{is}(t) \tag{3.7}$$

using the time domain responses developed in Equations 3.1, 3.4, and 3.5.

Finally, the signal is modulated by the I-Q modulator. The resulting modulated signal, $s_m(t)$, can be expressed as

$$s_m(t) = Re[u(t)\exp(j2\pi f_m t)] \tag{3.8}$$

$$= u_I(t)\cos(2\pi f_m t) - u_Q(t)\sin(2\pi f_m t) \tag{3.9}$$

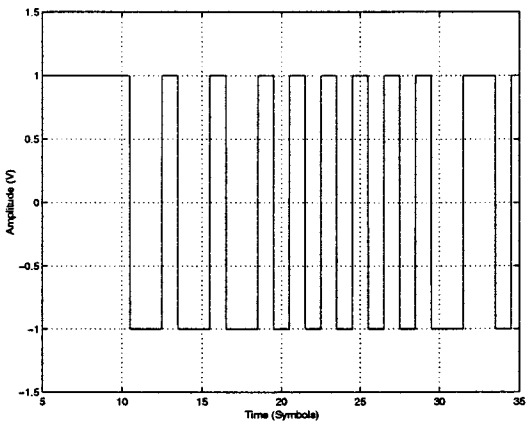
where f_m is the modulated carrier frequency and $u(t)$ is the baseband signal of Equation 3.6.

Figure 3.5 displays the relationship between the original inphase bit stream data and the filtered output of the inphase signal component. The original inphase bit stream is shown in Figure 3.5(a). The encoded data is shown in Figure 3.5(b). The filtered encoded data is displayed in Figure 3.5(c) for filtering of $\alpha = 0.35$. As can be seen in Figures 3.5(b) and 3.5(c), encoding and filtering delay the signal relative to the original waveform. The time axis on these figures is shifted, so that the encoded and filtered waveforms line up with the original inphase bit stream.

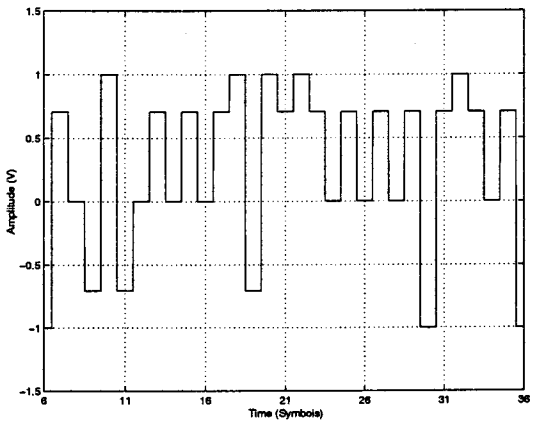
3.1.2 Upconverter

The modulator output frequency is often lower than the desired transmit frequency, since many modulator components are more cost-effective at lower frequencies. The modulator frequency must then be converted to the channel frequency dictated for the system.

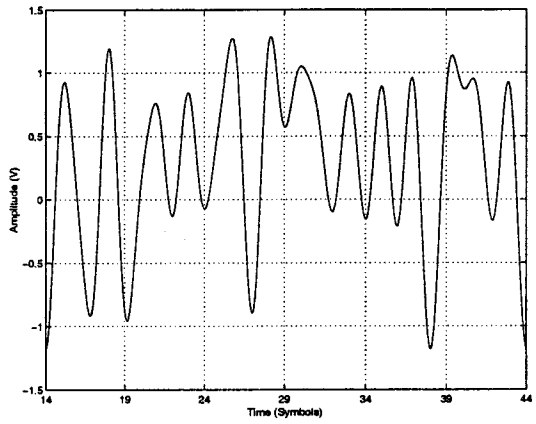
The resulting bandpass signal at the output of the upconverter, $s_{uc}(t)$, and its



(a) Original inphase bit stream



(b) Encoded waveform, $b_I(t)$



(c) Filtered waveform, $u_I(t)$

Figure 3.5: Time domain waveforms for the transmitter inphase component

bandpass frequency, f_c, can be expressed as

$$s_{uc}(t) = Re[u(t)\exp(j2\pi f_c t)] \tag{3.10}$$

$$f_c = f_m + f_{uc} \tag{3.11}$$

where f_m is the modulator output frequency, f_{uc} represents the frequency shift introduced by the upconverter, and $u(t)$ is the baseband signal.

The upconverter normally consists of an oscillator, feeding a double balanced mixer that translates the incoming frequency to a higher frequency. The image frequencies, which are created by the mixing process, are filtered and removed from the transmitted signal.

3.1.3 Power Amplifier

The signal is amplified to the appropriate level for the system channel by a power amplification stage. The amplified signal, $s(t)$, is a scaled version of Equation 3.10 and ideally expressed as

$$s(t) = Re[A \cdot u(t)\exp(j2\pi f_c t)] \tag{3.12}$$

where A represents the linear gain of the amplifier.

Since a linear modulation method is used, it is necessary for the power amplifier to be linear. Nonlinearities cause intermodulation distortion and spectral regrowth of the sidelobes in the amplified signal that results in reduced performance and adjacent channel interference.

For the purposes of this thesis, the upconverter and amplification stages of the transmitter will normally be assumed to be ideal. When investigating impairments associated with upconversion and amplification, the corresponding section will describe the cause and effect of the impairment in detail.

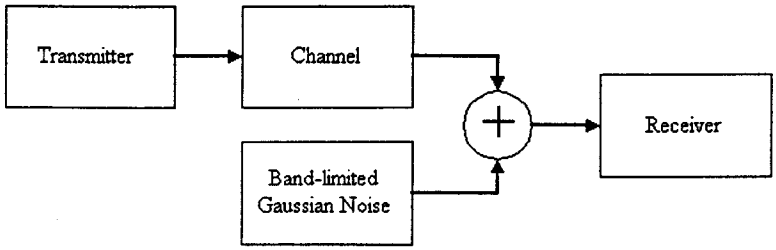


Figure 3.6: Block diagram showing additive noise

3.2 Channel

The characteristics of the channel are usually beyond the control of the communication system designer. These characteristics are defined by the geography and atmospheric effects to which the signal is subjected. For simplicity, a good approximation to the characteristics of an actual channel is an additive white Gaussian noise (AWGN) channel [31].

For the simulation models, it is assumed that the received signal is corrupted with AWGN. This band-limited Gaussian noise is added to the transmitted signal prior to reception at the receiver as shown in Figure 3.6. The Gaussian noise consists of independent baseband inphase and quadrature components that are modulated to the radio channel frequency for addition to the transmitted signal. The quadrature modulation ensures that there is no correlation between the inphase and quadrature noise components.

Channel fading effects on $\pi/4$-DQPSK have been discussed extensively in the existing literature [13, 15, 17, 16, 21, 24], so this topic will not be discussed in this thesis. The reader is referred to these articles for additional information.

3.3 Receiver

A block diagram of an ideal receiver is shown in Figure 3.7. A typical receiver consists of a low noise amplifier (LNA) and downconverter followed by a demodulator that performs the majority of its work at an intermediate or baseband frequency.

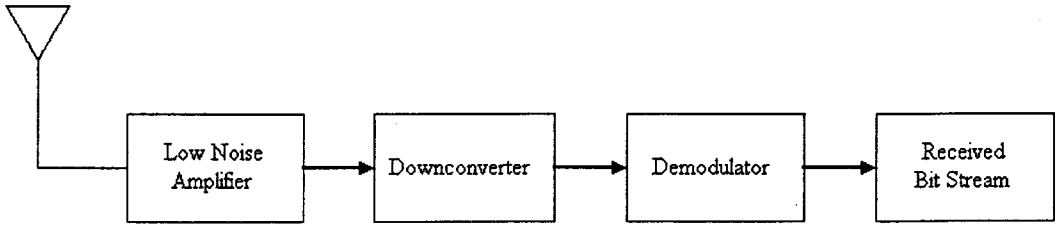


Figure 3.7: Block diagram of an ideal receiver

The downconversion stage is neglected in receivers that directly demodulate at the transmit frequency.

The receiver amplifier boosts the received signal level, just as the power amplifier did for the transmitted signal as described in Section 3.1.3. Typically, this amplifier has a low noise figure, since it is desirable to amplify the received signal without introducing considerable additional noise.

The downconverter stage converts the received frequency to a lower intermediate frequency. It performs the inverse function of the upconverter described in Section 3.1.2. The rationale for this is the same as the upconverter in the transmitter. Typically, the demodulation is done at a lower frequency, where components are more cost-effective and are readily available from suppliers.

3.4 Detector Models

The $\pi/4$-DQPSK modulated signal can be detected both coherently and noncoherently. Coherent demodulators require the local oscillator to be locked to the received carrier signal in both frequency and phase. Noncoherent receivers do not require the phase locking mechanism, which makes them simpler to implement. Common $\pi/4$-DQPSK noncoherent detectors include the baseband differential detector, the IF differential detector, and the frequency discriminator detector [7].

For the following models, it is assumed that the received signal is corrupted with AWGN as described in Section 3.2. The received signal, $r(t)$, can be expressed as

$$r(t) = s(t) + n(t) \tag{3.13}$$

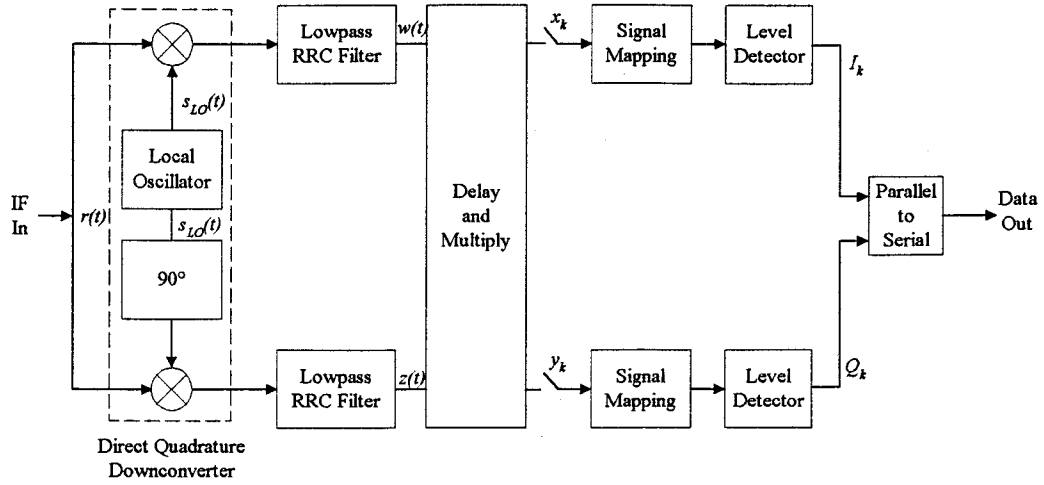


Figure 3.8: Block diagram of the baseband differential detector

where $s(t)$ denotes the transmitted signal and $n(t)$ refers to the additive noise. The AWGN, $n(t)$, can also be expressed as quadrature noise

$$n(t) = n_I(t)\cos(2\pi f_c t) - n_Q(t)\sin(2\pi f_c t) \tag{3.14}$$

where $n_I(t)$ represents the inphase component of the noise and $n_Q(t)$ denotes the quadrature component of the noise. It is assumed that these noise components are independent and uncorrelated.

3.4.1 Baseband Differential Detector

The baseband differential detector performs the majority of the detection process at baseband. Figure 3.8 displays a block diagram of an ideal baseband differential detector [13]. This detector is sometimes referred to as the optimal differential detector [32].

In this detector, it is assumed that the local oscillator (LO) frequency is the same as the incoming frequency and that the phase offset between the oscillator and the carrier signal varies slowly relative to the symbol period. In this way, a fixed phase offset between the LO and the IF carrier signal can be assumed between symbols, which is accounted for in the differential detection process as explained below.

At the input of the detector, the IF or RF signal is directly converted to baseband by the quadrature downconverter. After the ideal mixing, the I and Q signal components are lowpass filtered by a square root raised cosine filter. This filter provides optimal performance in the presence of AWGN, which reduces intersymbol interference and removes the higher order mixing products. After filtering, the signal is differentially decoded using a delay and multiply operation.

The baseband differential detection process is derived mathematically as follows. The effects of noise as well as intersymbol interference are neglected in this derivation. The received bandpass signal, $r(t)$, is specified as

$$r(t) = A(t)\cos(2\pi f_c t + \theta(t)) \tag{3.15}$$

where f_c is the bandpass carrier frequency, $A(t)$ is the signal amplitude, and $\theta(t)$ is the phase angle of the signal. This bandpass signal is quadrature downconverted to baseband by a local oscillator signal, $s_{\mathrm{LO}}(t)$, which is defined as

$$s_{\mathrm{LO}}(t) = \cos(2\pi f_c t + \phi) \tag{3.16}$$

and has the same frequency as the input signal with a fixed phase offset to the input signal, ϕ.

The inphase component, $w(t)$, of the signal can be found by multiplying Equations 3.15 and 3.16. Using trigonometric identities and neglecting higher order terms that are assumed to be removed by the lowpass filtering, this produces a baseband signal that can be expressed as

$$w(t) = \frac{A(t)}{2}\cos(\theta(t) - \phi) \tag{3.17}$$

which is dependent on the input carrier phase and the phase offset between the LO and the input signal, as well as the signal amplitude.

The quadrature component, $z(t)$, can be found in a similar manner to the inphase component. In this case the LO waveform is phase shifted by 90° to produce a sine

wave, rather than a cosine wave. Again using trigonometric identities and neglecting higher order terms, produces a baseband signal, similar to Equation 3.17, that can be expressed as

$$z(t) = \frac{A(t)}{2}\sin(\theta(t) - \phi). \tag{3.18}$$

For mathematical simplicity, the remainder of the derivation is done at discrete sample points, k, which are separated by a symbol interval. The ideal sampling point is the point at which the signal eye diagram is most open and thus, most likely to produce a mapping to the correct symbol. The ideal sampling points are separated by a symbol period in time.

The detection operation is performed by multiplying the current sampled value by the sample value from the previous symbol period. After the detection operation, the inphase signal output, x_k, is given by the differential decoding logic, through the use of trigonometric identities, as

$$\begin{aligned} x_k &= w_k w_{k-1} + z_k z_{k-1} && (3.19)\\ &= \frac{A_k A_{k-1}}{4}\cos(\theta_k - \phi)\cos(\theta_{k-1} - \phi) + && (3.20)\\ &\quad \frac{A_k A_{k-1}}{4}\sin(\theta_k - \phi)\sin(\theta_{k-1} - \phi) \\ &= \frac{A_k A_{k-1}}{4}\cos(\theta_k - \theta_{k-1}). && (3.21) \end{aligned}$$

Assuming that the amplitude at the ideal sampling points is slowly changing (slow fading compensated by automatic gain control), it can be assumed that $A_k \approx A_{k-1}$ and the inphase detector output can be simplified to

$$x_k = \cos(\theta_k - \theta_{k-1}) \tag{3.22}$$

which is simply the cosine of the phase difference between symbols. This detected signal level can be mapped to the detector output as indicated in Table 3.1.

The quadrature signal output, y_k, is given by the differential decoding logic and

Table 3.1: Relationship of detected signal levels to output bits

x_k	I	y_k	Q
+	0	+	0
−	1	−	1

is derived in a similar manner as the inphase component as

$$y_k = z_k w_{k-1} - w_k z_{k-1} \tag{3.23}$$

$$= \frac{A_k A_{k-1}}{4} \sin(\theta_k - \phi)\cos(\theta_{k-1} - \phi) - \frac{A_k A_{k-1}}{4} \cos(\theta_k - \phi)\sin(\theta_{k-1} - \phi) \tag{3.24}$$

$$= \frac{A_k A_{k-1}}{4} \sin(\theta_k - \theta_{k-1}). \tag{3.25}$$

Neglecting amplitude variation at the ideal sampling point between symbols ($A_k \approx A_{k-1}$), the quadrature phase detector output simplifies to

$$y_k = \sin(\theta_k - \theta_{k-1}) \tag{3.26}$$

which is the sine of the phase difference between symbols. These detected signal levels can be mapped to the detector output as illustrated in Table 3.1.

3.4.2 IF Differential Detector

The IF differential detector performs most of its detection process at an intermediate frequency. A block diagram of the detector is shown in Figure 3.9. This demodulator is sometimes referred to as the conventional delay and mix detector [17].

An optimal RRC bandpass filter is used to filter the signal at the front-end of the receiver. The signal is then multiplied by a delayed version of itself. The length of the delay is one symbol period, T_s. After the multiplication, the second order frequency components are removed by a filter with a lowpass bandwidth, $BW = \frac{2(1+\alpha)}{T_s}$, leaving only the baseband signal.

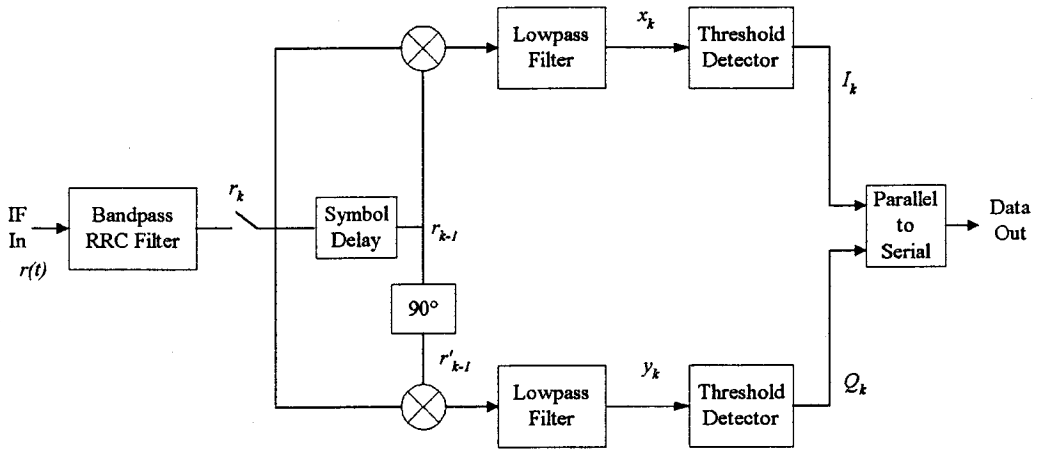


Figure 3.9: Block diagram of the IF differential detector

The IF differential detection process is derived mathematically as follows. The effects of noise as well as intersymbol interference are neglected in this derivation. The received bandpass signal, $r(t)$, is specified as

$$r(t) = A(t)\cos(2\pi f_c t + \theta(t)) \tag{3.27}$$

where f_c is the bandpass frequency, $A(t)$ is the signal amplitude, and $\theta(t)$ is the phase angle of the signal. Typically, the incoming RF signal is downconverted to an intermediate demodulation frequency. This signal can be expressed in a similar manner as Equation 3.27 as

$$r(t) = A(t)\cos(2\pi f_m t + \theta(t)) \tag{3.28}$$

where f_m is the intermediate frequency.

The inphase component of the signal can be found by multiplying Equation 3.27 with a time delayed version of the same signal. For simplicity, the remainder of the derivation takes place at discrete points, k, which are integer multiples of the sampling point that are separated by a symbol period in time. Using trigonometric identities and neglecting higher order terms that are assumed to be removed by the

detector filtering, the detected inphase baseband signal, x_k, can be expressed by

$$\begin{aligned} x_k &= r_k \cdot r_{k-1} && (3.29)\\ &= A_k \cos(2\pi f_m k + \theta_k) \cdot A_{k-1} \cos(2\pi f_m (k-1) + \theta_{k-1}) && (3.30)\\ &= \frac{1}{2} A_k A_{k-1} [\cos(\theta_k - \theta_{k-1}) + \cos(4\pi f_m k + \theta_k + \theta_{k-1})] && (3.31)\\ &= \frac{1}{2} A_k A_{k-1} \cos(\theta_k - \theta_{k-1}). && (3.32) \end{aligned}$$

Assuming that the amplitude is slowly changing at the ideal sampling instants (slow fading) between symbols, the inphase detector output can be simplified to

$$x_k = \cos(\theta_k - \theta_{k-1}) \tag{3.33}$$

which is simply the cosine of the phase difference between symbols. It should be noted that this is the same output as the baseband differential detector that was developed in Equation 3.22. This detected signal level can be mapped to the detector output as indicated in Table 3.1.

The corresponding quadrature component signal output is derived in a similar manner using trigonometric identities and neglecting higher order terms that are removed by the lowpass filter. The quadrature component output, y_k, can be expressed as

$$\begin{aligned} y_k &= r_k \cdot r'_{k-1} && (3.34)\\ &= A_k \cos(2\pi f_m k + \theta_k) \cdot A_{k-1} \sin(2\pi f_m (k-1) + \theta_{k-1}) && (3.35)\\ &= \frac{1}{2} A_k A_{k-1} [\sin(\theta_k - \theta_{k-1}) + \sin(4\pi f_m k + \theta_k + \theta_{k-1})] && (3.36)\\ &= \frac{1}{2} A_k A_{k-1} \sin(\theta_k - \theta_{k-1}) && (3.37) \end{aligned}$$

where r'_{k-1} is phase shifted 90° relative to r_{k-1}.

Neglecting amplitude variation at the ideal sampling point between symbols, the

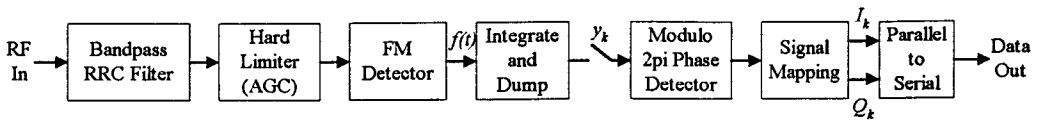


Figure 3.10: Block diagram of the frequency discriminator detector

quadrature phase detector output simplifies to

$$y_k = \sin(\theta_k - \theta_{k-1}) \tag{3.38}$$

which is the sine of the phase difference between symbols and the same as Equation 3.26 for the baseband differential detector. These detected signal levels can be mapped to the detector output as illustrated in Table 3.1.

3.4.3 Frequency Discriminator Detector

The frequency discriminator detector uses FM detection to accomplish the demodulation process. The block diagram of an ideal frequency discriminator detector is shown in Figure 3.10. This detector is sometimes referred to as the limit-discriminate-integrate (LDI) detector.

Like the IF differential detector, the received signal is filtered at the front end of the receiver by an optimal square root raised cosine filter. This filtering produces phase trajectories corresponding to four different frequency deviations. The resulting FM detected voltages map to the $\pi/4$-DQPSK symbols, allowing this detection method to be used.

Following the filter, a hard limiter is used to remove the signal envelope variation so that it does not affect the FM detection process, which is often sensitive to amplitude variation. The ideal hard limiter is assumed to not affect the phase of the received signal.

After hard limiting, the signal is differentiated using a frequency modulation (FM) discriminator. The differentiator extracts the instantaneous frequency deviation of the signal. The response of the discriminator, $f(t)$, is ideally represented

Table 3.2: Relationship of detected discriminator signal levels to output bits

y_k	IQ
$3\pi/4$	01
$\pi/4$	00
$-\pi/4$	10
$-3\pi/4$	11

as

$$f(t) = \frac{d\theta(t)}{dt}. \tag{3.39}$$

which differentiates the phase, $\theta(t)$, of the signal. This process is not sensitive to amplitude variation, since the signal has already been hard limited.

After differentiation, the signal is integrated over an entire symbol period. At the ideal sampling instant, the accumulated signal is sampled and the integrator is reset to zero. This integrate and dump operation has an output, y_k, that can be expressed mathematically as

$$y_k = \int_{(k-1)T_s}^{kTs} f(t)dt \tag{3.40}$$

$$= \theta_k - \theta_{k-1} + 2\pi k. \tag{3.41}$$

This output is proportional to the phase difference between the k-th symbol and the previous symbol.

It can be seen that the phase difference between the two symbols is detected as a four level signal, which corresponds to the four $\pi/4$-DQPSK symbols. In addition, a phase ambiguity of $2\pi k$ is also introduced, which is indicated by Equation 3.40. The phase ambiguity is due to FM click noise and can be eliminated by using a modulo-2π phase detector after the integrate and dump operation. The modulo-2π detector ensures the detected phase difference falls between $\pm\pi$. The modulo-2π phase detector outputs a four level signal corresponding to the four possible phase differences. The detected phase angles are mapped to the desired symbols as shown in Table 3.2.

The phase ambiguity in this detector results from FM click noise [14]. This click noise causes the phase trajectory of the signal to go the other way around the phase circle, since the noise causes the signal to wrap around the origin. This results in a signal with a frequency deviation other than that expected from the four standard symbols. The most likely occurrence of this phenomenon is with the $\pm 3\pi/4$ phase shifts, since these transitions go nearest the origin of the phase circle. The modulo-2π phase detector maps the signals affected by click noise into the appropriate quantization bin and reduces errors caused by this phenomenon.

3.4.4 Demodulator Equivalence

In a number of articles, it has been proven that the baseband differential detector, intermediate frequency (IF) differential detector, and the frequency discriminator detector with modulo-2π phase detection are mathematically equivalent [13, 15, 16]. Each demodulator has identical bit error ratio (BER) performance.

The BER performance of the ideal demodulators is equivalent and is illustrated in Figure 3.11. The derivation of the BER is very complicated due to the correlation between the inphase and quadrature components of the detected signal [29]. The result of the derivation is the error probability, P_e, as a function of bit energy to noise density, E_b/N_o, and is given as

$$P_e(E_b/N_o) = Q(a,b) - 0.5I_0(ab)\exp(-0.5(a^2+b^2)) \tag{3.42}$$

$$a = \sqrt{2E_b/N_o(1-\frac{1}{\sqrt{2}})} \tag{3.43}$$

$$b = \sqrt{2E_b/N_o(1+\frac{1}{\sqrt{2}})} \tag{3.44}$$

where $Q(a,b)$ is Marcum's Q-function defined as

$$Q(a,b) = \int_b^\infty tI_0(at)\exp(-0.5(a^2+t^2))dt \tag{3.45}$$

and I_0 is the modified Bessel function [29].

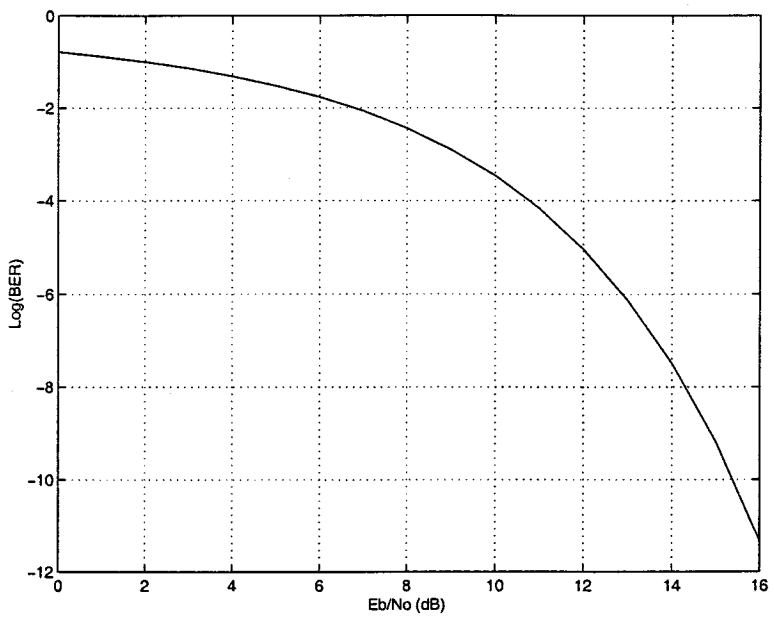


Figure 3.11: Bit error ratio characteristic of the ideal $\pi/4$-DQPSK demodulators

When E_b/N_o is high, the BER under AWGN conditions can be approximated by

$$P_e(E_b/N_o) = 0.5\text{erfc}(2\sin\frac{\pi}{8}\sqrt{E_b/N_o}) \tag{3.46}$$

where erfc is the complementary error function.

The remainder of the sections will investigate detectors based on the models shown in this section. Transmitter and receiver impairments will be simulated to determine the performance of each modem.

3.5 Simulation Notes

Simulation has become the dominant method of investigating design alternatives in communication systems [31]. The simulation of communication systems imitates the behavior of the actual hardware found in communication systems. In order to get accurate results, it is important to model the parameters of the physical communication system accurately.

The majority of the results in this thesis are generated through simulation. This

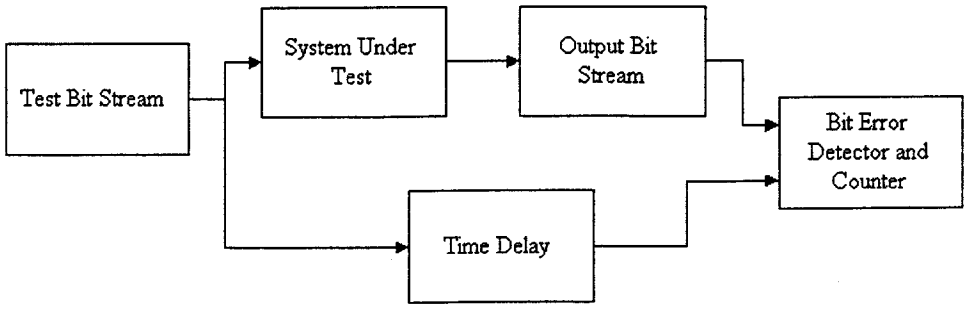


Figure 3.12: Block diagram of the simulation test setup

chapter has presented the basic models used in the simulations throughout the thesis. The primary performance measure used to compare the results is the bit error ratio (BER) performance of the system, which is the most common measure used to compare digital communication systems.

The simulation results were generated using the Hewlett Packard (HP) Advanced Design System (ADS) v1.1 computer program, as well as its precursor HP Series IV Omnisys. This computer program is a powerful simulation tool for communication design. Simulations can be performed using high-level functional blocks (eg. an ideal quadrature amplitude modulation (QAM) demodulator) or low-level circuit diagrams (eg. a mixer schematic within the demodulator) or a combination of both. The program has an extensive built-in collection of the common building blocks of communication systems.

Figure 3.12 shows the general test set up for determining the BER performance of a communication system [31]. An input bit stream is fed to the system under test. The output bit stream, which contains the combined effects of the transmitter, receiver, and channel, is compared to the input to determine if any bit errors have occurred. To compare the input and output bit streams, it is necessary to delay the input bit stream by the amount of delay present within the system under test.

This simulation methodology is known as the Monte Carlo simulation type. In a Monte Carlo simulation, a sequence of Bernoulli trials is set up [31]. The system is stimulated with an input. The number of successes is counted and divided by the number of trials to determine the statistics of the system. For a communication

system, this is interpreted as the bit error ratio. This BER is calculated as

$$\text{BER} = \frac{N_e}{N_b} \tag{3.47}$$

where N_e is the number of errors and N_b is the number of bits in the simulation run.

The Monte Carlo simulation method requires no assumptions about the input processes or the system itself, since the system under test is bypassed. Only the input and output bit streams are used to determine the success or failure of each trial (bit) in the simulation. Since no assumption is made about the system under test, it is possible to accurately determine the performance degradation caused by both linear and nonlinear events in the communication system.

A disadvantage of the Monte Carlo simulation method is that it requires long simulation times. Other simulations methods such as importance sampling and the quasi-analytical method have shorter simulation times, but make assumptions about the nature of the system being tested which can bias the result accuracy [31].

Monte Carlo simulations derive the performance of the system in a statistical manner. Figure 3.13 demonstrates the relationship between the number of bits simulated, the associated bit error ratio and the confidence level of the simulated result [31]. This figure demonstrates that by simulating a greater number of bits, a more accurate result (one with less statistical variance) will be produced.

However, the variance decreases nonlinearly with the number of bits simulated. For the purposes of this thesis, all simulations generate at least 50 errors. In this manner, the variance on the results is limited to 2%. This number of simulation trials is a reasonable compromise between simulation run time and simulation result accuracy. The statistical accuracy of a simulation performed in this manner compares favorably to a well calibrated physical measurement of a communication system's performance [31].

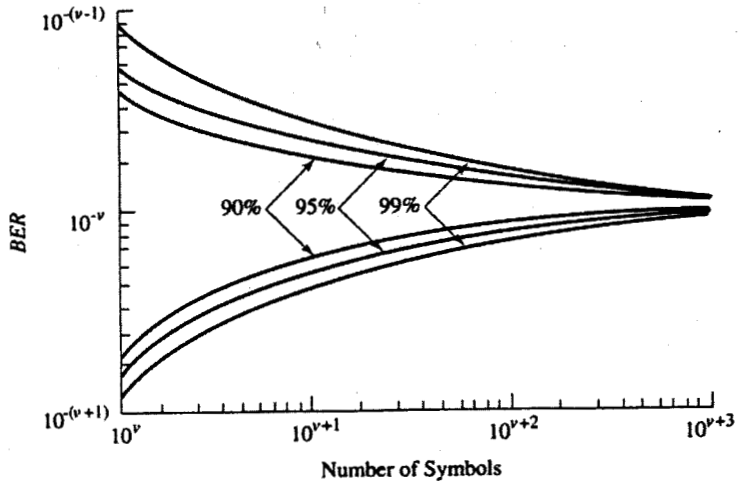


Figure 3.13: Monte Carlo simulation result confidence level

3.6 Summary

An ideal $\pi/4$-DQPSK transmitter consists of a modulator, upconverter, and a power amplification stage. The modulator encodes the incoming bit stream and performs the quadrature modulation. The upconverter translates the modulator frequency to the bandpass carrier frequency where the signal level is increased to the desired transmit power by the power amplifier.

An ideal $\pi/4$-DQPSK receiver consists of an amplification stage, downconverter, and demodulator. The amplification stage amplifies the received signal, without significantly increasing the noise in the signal. The downconverter translates the bandpass frequency to an intermediate frequency, suitable for the demodulation process. Finally, the demodulator converts the information in the received signal into the decoded bit stream.

The three standard detector types for a $\pi/4$-DQPSK demodulator are the IF differential detector, baseband differential detector, and the frequency discriminator detector. The baseband differential detector performs most of its processing at baseband, while the IF differential detector performs its processing at an intermediate frequency. The frequency discriminator detector uses an FM detector to determine the detected phase trajectory. These detectors accomplish the detection in different ways, but are proven to have mathematically equivalent bit error ratio performance

in the literature.

To compare the detector performance, the Monte Carlo simulation method is used. It provides an unbiased estimate of the BER performance. The output bit stream is compared to the input bit stream to determine the bit error statistics in the simulation run.

Chapter 4

PERFORMANCE IMPAIRMENTS

Many performance impairments in communication systems are caused by deviations from the ideal transmitter and receiver. Common transmitter impairments include DC offset of input signals and modulator phase imbalance between the in-phase and quadrature signal components. Common receiver impairments include imperfect symbol timing recovery and degradation caused by signal limiting. Other system impairments include frequency offset, sub-optimal filtering, and phase noise effects.

The causes and effects of these impairments are analyzed in this chapter. The BER performance of the $\pi/4$-DQPSK detector types in the presence of these impairments is characterized and compared. Compensation techniques are proposed to reduce the performance degradation caused by the particular impairment.

4.1 Frequency Offset Impairment

4.1.1 Cause

Frequency offsets between the receiver and the transmitter can occur in a number of ways. In coherent systems, the frequency offset can be caused by imperfect carrier recovery mechanisms. Noncoherent detectors do not usually suffer from this problem since they do not have to incorporate carrier recovery circuits, but offsets can be caused by frequency instability in either the transmitter or receiver oscillators. In

a mobile environment, frequency offsets are created by Doppler shifts due to the relative motion between the transmitter and receiver.

The main source of frequency error for this application is the oscillators used in the transmitter upconverter and the receiver downconverter. The oscillators are used to convert the signal frequency up to RF or down to IF, respectively.

Cost effective crystals used in oscillators typically have a drift on the order of 50 parts per million (ppm). This translates into an error of ± 87.5 kHz, at a nominal frequency of 3500 MHz, which is transferred to IF or baseband in the frequency translation. This frequency drift changes slowly with respect to the symbol period. However, the amount of frequency offset between the receiver and the transmitter is significant relative to the symbol rate and causes system performance degradation.

4.1.2 Simulation Notes

The frequency offset error is modeled by offsetting the transmitter frequency, f_t, relative to the receive frequency, f_r, such that $f_t \neq f_r$. The frequency offset, Δf, is defined as

$$\Delta f = f_t - f_r. \tag{4.1}$$

The frequency offset, f_{offset}, can be normalized in terms of the symbol rate, such that

$$f_{\text{offset}} = \Delta f \cdot T_s \tag{4.2}$$

where $T_s = 1/R_s$ is the symbol period and R_s is the symbol rate.

In the simulations for the detector types, the transmit frequency is offset by fixed amounts relative to the receive frequency. Frequency drift is more accurately defined as a statistical process which varies around the nominal frequency. However, for ease of simulation, the frequency drift is instead modeled as discrete fixed offsets.

4.1.3 Effect

A frequency offset has the same effect in all the detector types. The impairment causes a proportional phase shift in the detected constellation. This phase shift, $\Delta\theta$, is defined as

$$\Delta\theta = 2\pi\Delta f T_s \tag{4.3}$$

where Δf is the frequency offset defined in Equation 4.1. Table 4.1 shows the phase offset associated with a number of frequency offsets. The frequency offset, f_{offset}, is given as a percentage of the symbol rate, R_s.

This phase shift causes a significant reduction in the BER performance of the communication system. Besides the phase shift, additional degradation is observed since the detector filter is not centered at the received signal frequency. However, the majority of the degradation observed for the impairment is due to the detected phase offset caused by the frequency offset.

The BER performance degradation caused by frequency offset is derived by Liu for the frequency discriminator detector [26]. A summary of the derivation is presented here. The frequency offset impairment causes the detected signal constellation to be rotated by $\Delta\theta$ from the nominal points. The average probability of error, P_e, can then be calculated as

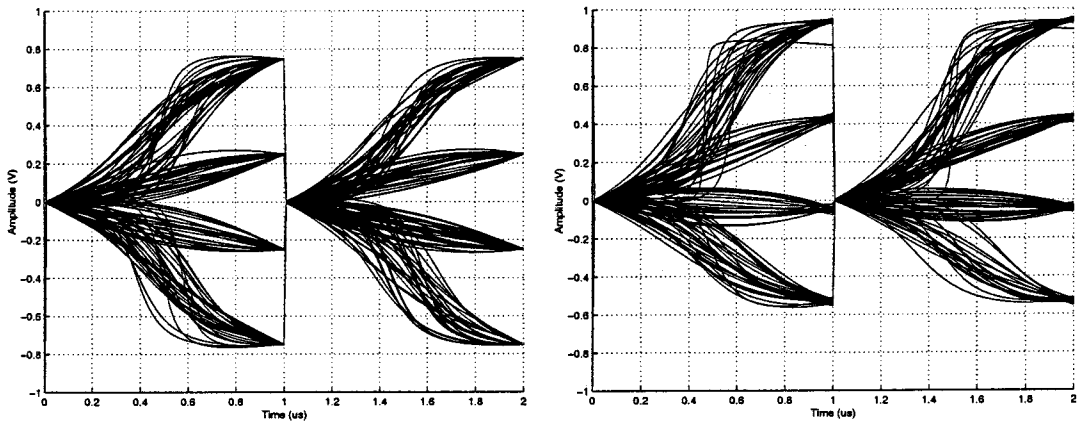
$$P_e(E_b/N_o|\Delta\theta) = 0.5(P_1 + P_2) \tag{4.4}$$

where

$$\begin{aligned} P_1 &= P_e(2\cos^2(\pi/4 - \Delta\theta)E_b/N_o) \\ P_2 &= P_e(2\cos^2(\pi/4 + \Delta\theta)E_b/N_o). \end{aligned}$$

Table 4.1: Phase shifts for a number of frequency offsets

Frequency Offset (%)	*Phase Offset (°)*
1	3.6
2.5	9
5	18
10	36
12.5	45



(a) No frequency offset

(b) $f_{\text{offset}} = 10\%$

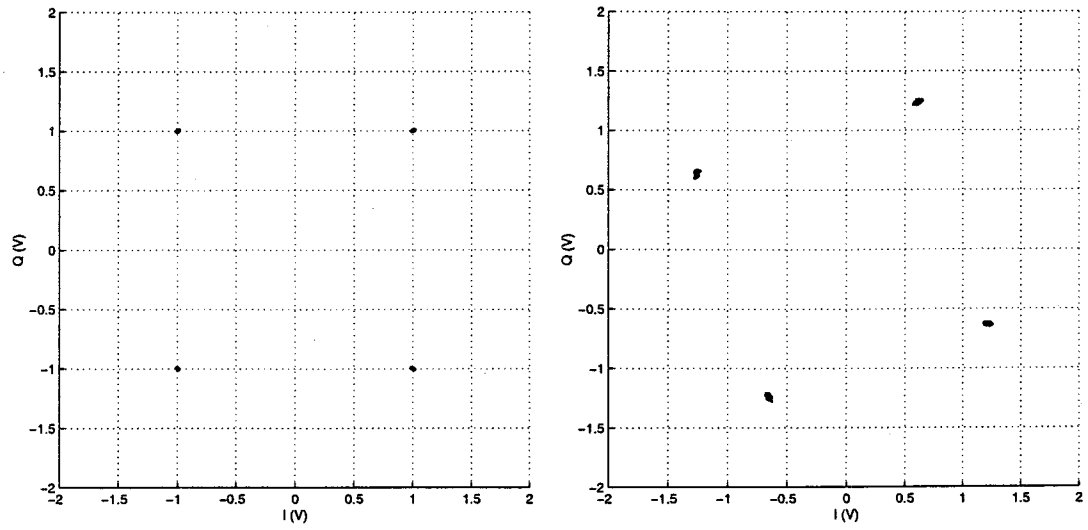
Figure 4.1: Frequency offset eye diagrams for the frequency discriminator detector

4.1.3.1 Frequency Discriminator Detector

In the frequency discriminator, the phase shift caused by the frequency offset results in a DC shift in the detected signal. Figure 4.1(a) shows the eye diagram of a detected $\pi/4$-DQPSK signal that does not have any frequency offset. Figure 4.1(b) shows the eye diagram of the same signal, but with a frequency offset of $f_{\text{offset}} = 10\%$. It can be observed that the detected eye diagram in Figure 4.1(b) has a DC offset which is proportional to the frequency offset applied to the transmitter.

4.1.3.2 IF Differential and Baseband Differential Detector

In the IF differential and baseband differential detector, the phase shift caused by the frequency offset results in a corresponding phase shift in the I-Q constellation



(a) No frequency offset

(b) $f_{\text{offset}} = 5\%$

Figure 4.2: Constellation diagrams for the differential detectors impaired by frequency offset

diagram. The entire constellation is rotated by the phase shift associated with the frequency offset. Figure 4.2 shows the ideal and shifted constellation points for a frequency offset of 5%.

4.1.4 BER Performance

Figure 4.3 shows the simulation results of the BER performance for the IF differential detector for a number of frequency offsets. The performance of the baseband differential detector was observed to be similar to the IF differential detector within the simulation accuracy.

As the frequency offset increases, the BER performance decreases since the detected signal levels have reduced noise margins. A frequency offset of 10% causes severe BER performance degradation, resulting in BER performance that does not increase significantly with increased E_b/N_o.

Simulated BER performance agrees closely for the differential detectors and is very similar to the calculated values derived by Liu [26]. At a BER of 10^{-4}, the performance degradation is 0.2 dB and 1.2 dB for frequency offsets of 1% and 2.5%

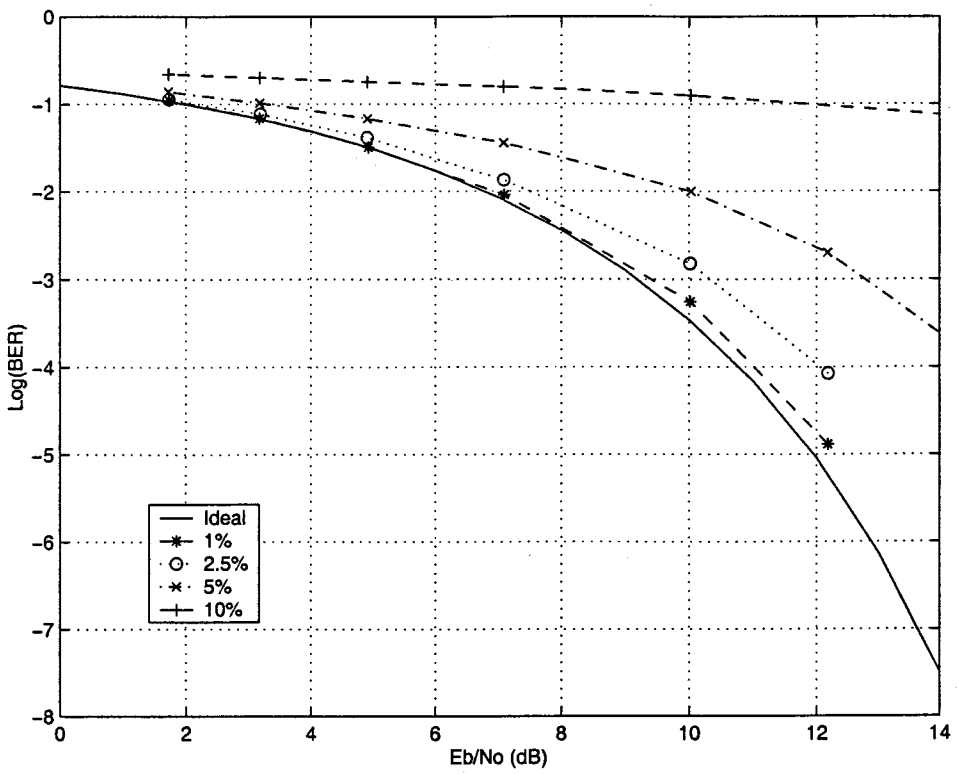


Figure 4.3: BER performance for the differential detectors impaired by frequency offset

respectively.

4.1.5 Compensation Techniques

A number of compensation techniques are possible for this impairment. Liu proposed a simple offset compensation for the frequency discriminator detector [13]. In this scheme, a known preamble sequence of symbols is transmitted. The detector receives the preamble symbols and compares them to the expected symbol voltages of the preamble. In this manner, the DC offset is determined that corresponds to the frequency offset. The inverse offset is applied to the rest of the received data symbols, which effectively removes the frequency offset from the subsequent symbols. This type of a technique is also applicable to the differential detectors, but must be applied to the I-Q phase rotation to remove the frequency offset rotation [10].

A similar technique to the one just described can be performed in the digital

domain. In this method, derotation of the phase constellation can be performed numerically. The phase offsets are detected through a preamble sequence, similar to the technique just described. Subsequent sampled values are adjusted to compensate this effect and remove any fixed numerical phase offsets caused by the frequency offset.

Automatic frequency control (AFC) loops that are based on phase locked loops or other methods can be used to synchronize the receiver frequency to the received signal [29]. In packet based communications, the traffic is of a bursty nature. Therefore, it is important that the AFC loop has a short acquisition time so it does not decrease the system data throughput efficiency with a long preamble.

Another possible technique is the use of a pilot channel, like that used in CDMA systems [10]. The receiver can lock to the pilot tone to synchronize frequencies. This technique is simple to implement, but requires frequency locking circuitry in the receiver. It also requires additional frequency spectra for the transmission of the pilot tone.

Another possible method is the use of a high level protocol check, when the frequency offset has been determined to be the major source of error in the system. The transmitted packet contains an error detection code so the receiver can detect packet errors. When the packet error rate is high, the receiver adjusts the frequency in discrete steps until the error rate decreases.

4.2 DC Offset Impairment

4.2.1 Cause

DC offset is the difference between the desired voltage levels and the actual voltage level. The encoded inphase and quadrature signal levels for $\pi/4$-DQPSK are ideally 0, $\pm\sqrt{2}/2$, or ± 1, and are symmetrical about zero. However, due to inaccuracies in the signal sources, the modulating signal may have an inherent DC offset voltage. Ideally, the random symbols do not have a DC offset component,

since this offset results in carrier feedthrough and leads to a shift in the detected signal constellation that causes degraded BER performance.

4.2.2 Simulation Notes

The DC offset error is modeled by shifting the ideal modulating signal voltages by a fixed offset, v_{dc}, relative to the original symbol levels. The transmitted symbol voltage, v_t, is defined as

$$v_t = v_i + v_{\mathrm{dc}} \tag{4.5}$$

where v_i is the ideal transmit voltage. DC offset is modeled for both the inphase and quadrature signal components.

The DC offset can be normalized to the symbol amplitude by multiplying the additive DC offset by the maximum voltage deviation. This offset percentage, DC, is expressed as

$$\mathrm{DC} = \frac{v_{\mathrm{dc}}}{v_+ - v_-} \times 100\% \tag{4.6}$$

where v_+ is the maximum positive signal level and v_- is the maximum negative signal voltage level. For this application, DC offset is specified as a percentage of the 2V range of the input signals (-1V to +1V).

4.2.3 Effect

DC offsets cause a shift in the phase constellation. Figure 4.4 demonstrates how the detected phase constellation in the detectors is affected by a DC offset of 10% in both the I and Q signals.

The DC offset creates different phase trajectories between the constellation points, when compared to the ideal case. These differences in phase trajectory result in phase shifts between constellation points that are not the $\pm\pi/4$ or $\pm 3\pi/4$ phase shifts expected for $\pi/4$-DQPSK. The phase shifts are still discrete, but are now dependent on the preceding symbols. The number of possible phase shifts remains finite (16 possible phase shifts) and is illustrated in the figure by the cluster

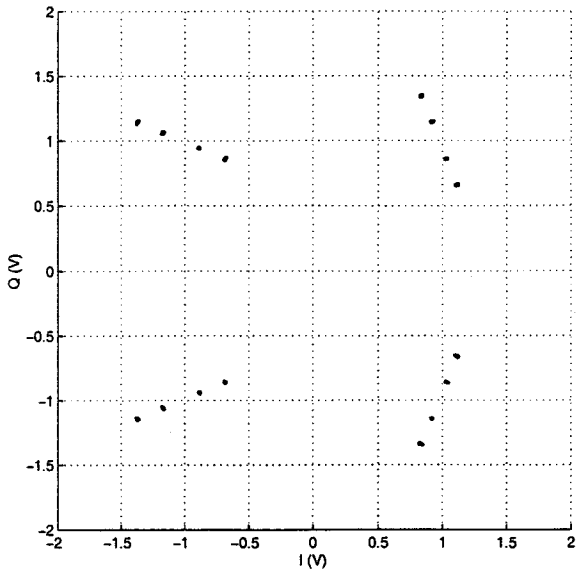


Figure 4.4: Constellation diagram of the differential detectors impaired by DC offset

of four points, which are around the expected constellation point.

This offset from the ideal causes degradation in the BER performance, since noise effects are more likely to cause symbol detection errors.

4.2.3.1 Frequency Discriminator Detector

In the frequency detector, the new set of phase trajectories leads to sixteen distinct detection points. Figure 4.5 shows the eye diagram for a signal with inphase and quadrature component DC offsets of 10% in the transmitted symbols. Ideally, the symbol integration should yield one of four possible phase differences, that map to the $\pi/4$-DQPSK symbols. However, this effect causes each of the four decision levels to have four distinct points. The additional points are caused because the phase shifts between points are not exactly $\pm k\pi/4, k = 1, 3$. Since the phase shifts depends on the starting and ending symbol and each have different phase shifts, increased variance is present around the ideal detection levels. As the signal to noise ratio (SNR) of the signal decreases, the noise is more likely to shift these points with greater variation into the adjacent sampling bin, leading to an increased probability of bit error.

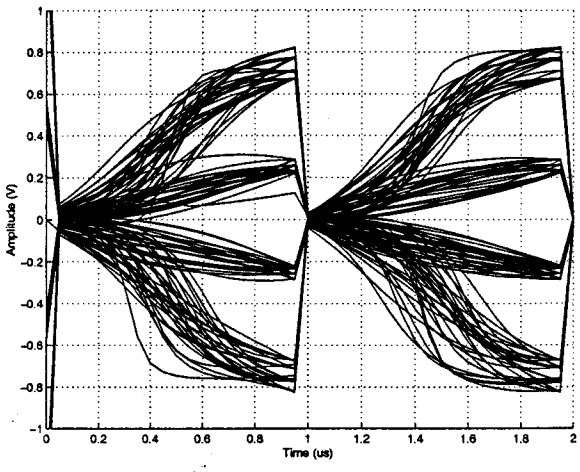


Figure 4.5: Eye diagram of the frequency discriminator detector impaired by DC offset

4.2.3.2 IF Differential and Baseband Differential Detectors

The effect in the IF differential and baseband differential detectors is similar to the effect in the frequency discriminator detector. Figure 4.6 displays the eye diagram for the differential detectors when confronted with a 5% inphase and quadrature DC offset. For the inphase signal shown, eight distinct voltage levels can be seen at the ideal sampling point. The quadrature signal (not shown) also has eight distinct voltage levels.

Figure 4.4 displays the phase constellation diagram for the differential detectors. With a DC offset of 5%, the detected phase differences are grouped around the ideal constellation point in four separate clusters. These clusters are caused by the unequal phase distances between symbols and represent the phase transitions caused by the DC offset. The number of transitions is finite and manifest the clusters on the phase constellation diagram. Additive noise makes these clusters less distinct, but does not remove the clustering effect.

4.2.4 BER Performance

Figure 4.7 shows the BER performance of the IF differential detector for a number of transmitter DC offsets. The performance of the baseband differential detector

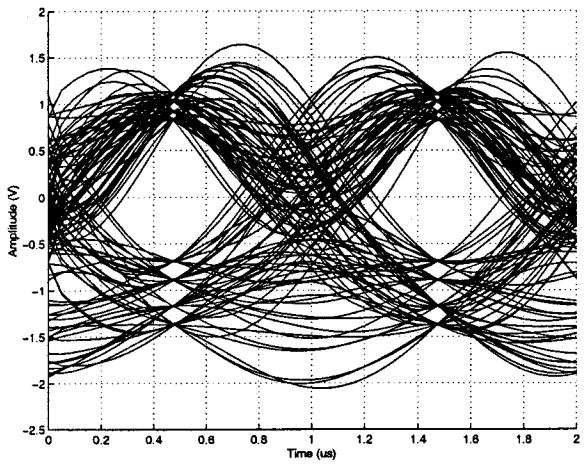


Figure 4.6: Eye diagram of the differential detectors impaired by DC offset

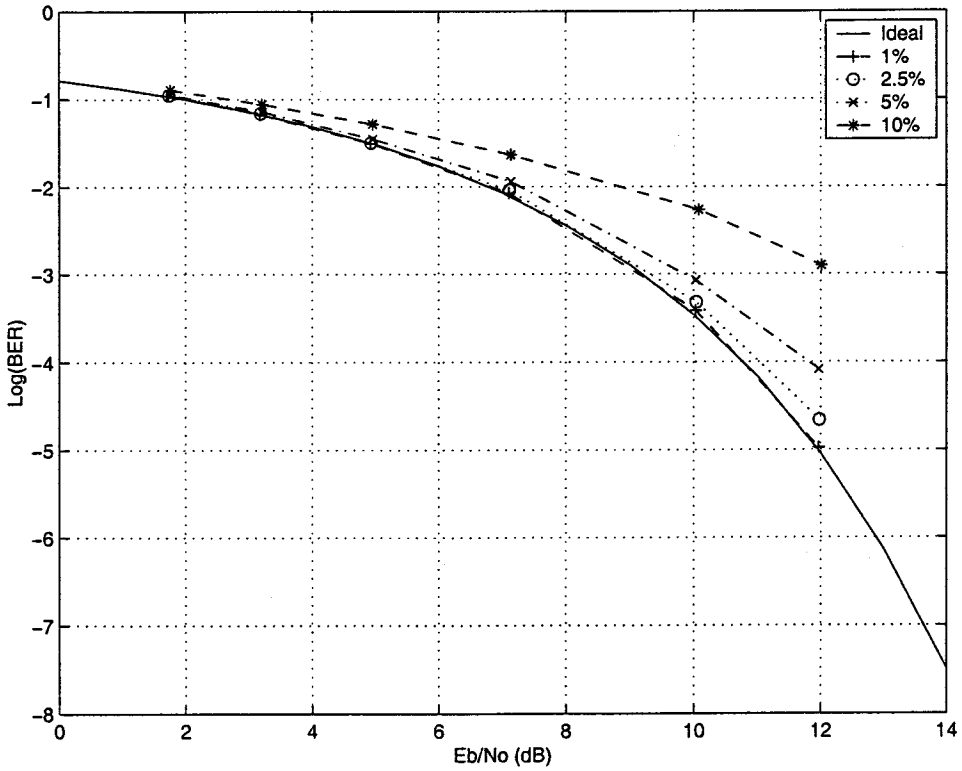


Figure 4.7: BER performance of the detectors impaired by DC offset

was also determined to be identical within statistical uncertainty. At a BER of 10^{-4}, performance degradations of 0.05 dB, 0.2 dB, and 1.0 dB are observed for inphase and quadrature component DC offsets of 1%, 2.5%, and 5% respectively.

4.2.5 Compensation Techniques

This impairment is best compensated in the transmitter of the system. The transmitted signal levels should be carefully controlled, so that the signal levels are symmetrical about 0 V. This symmetry will ensure that the transmitted signal is relatively free of DC offset, which will alleviate the performance degradation caused by this effect. Precompensation can be used to ensure that any fixed DC offsets are removed from the transmitted signal levels.

4.3 Phase Imbalance

4.3.1 Cause

Phase imbalance in quadrature modulators and demodulators results from the difficulties in producing a precise 90° phase shift between the inphase and quadrature phase components. These differences cause phase error in the modulated signal, since the phase angles no longer represent the ideal phases associated with $\pi/4$-DQPSK. These phase shifts, similar to the frequency offset impairment, shift the phase constellation and increase the probability of detection error.

Typical modulator phase imbalances are between 0.5° and 1.5°, with most devices having a maximum phase imbalance of 5 degrees [33].

4.3.2 Simulation Notes

The phase imbalance is modeled in the quadrature modulator of the system, which translates the baseband information signal to the desired carrier frequency. A baseband information signal, $v_{bb}(t)$, that contains both inphase and quadrature components is modulated with a quadrature continuous wave (CW) carrier frequency signal to produce the modulated output signal, $v_{mod}(t)$. The output of the modulator is expressed as

$$v_{mod}(t) = v_{I_{bb}}(t)\cos(2\pi f_c t) - v_{Q_{bb}}(t)\sin(2\pi f_c t + \frac{\phi\pi}{180}) \quad (4.7)$$

$$v_{mod}(t) = \Re\{(v_{I_{mod}}(t) + jv_{Q_{mod}}(t))\exp(j2\pi f_c t)\} \quad (4.8)$$

$$v_{I_{mod}}(t) = v_{I_{bb}}(t) - v_{Q_{bb}}(t)\sin(\frac{\phi\pi}{180}) \quad (4.9)$$

$$v_{Q_{mod}}(t) = v_{Q_{bb}}(t)\cos(\frac{\phi\pi}{180}) \quad (4.10)$$

where ϕ is the phase imbalance between the I and Q ports of the modulator and f_c is the modulating carrier frequency. The I and Q subscripts denote the inphase and quadrature components of the signals.

4.3.3 Effect

The phase imbalance results in a rotation in the received phase constellation that causes a BER performance degradation as seen in other impairments.

4.3.3.1 Frequency Discriminator Detector

Figure 4.8 shows the eye diagram for a signal with phase imbalance of 5° between the modulator ports. This impairment creates two clusters around the expected detector voltage, similar to the four clusters caused by the DC offset effect. The clusters are caused by different phase trajectories between signal points than the ideal case. As the SNR of the signal decreases, the noise is more likely to shift the sampled point into the adjacent phase quadrant, which leads to a bit error.

4.3.3.2 IF Differential and Baseband Differential Detectors

The effect in the IF and baseband differential detectors is similar to the effect in the frequency discriminator detector. Figure 4.9 displays the eye diagram for the differential detectors when faced with a 5° imbalance between the modulator I and Q ports. The eye diagram for the inphase component shows four distinct points at the ideal sampling point. The quadrature component (not shown) does not exhibit the same characteristic and has only two levels at the ideal sampling point. The inphase and quadrature voltage levels lead to the eight distinct points shown in the

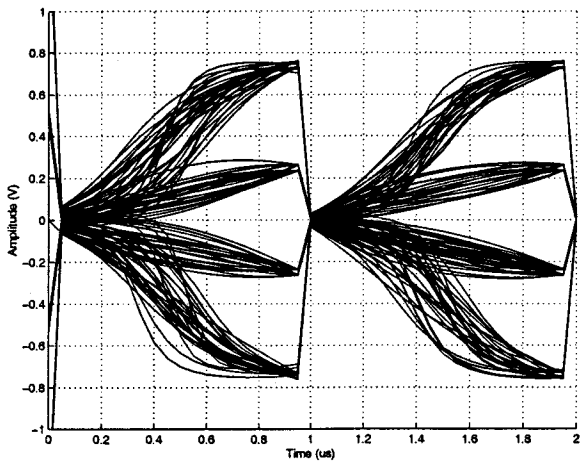


Figure 4.8: Eye diagram of the frequency discriminator detector impaired by phase imbalance

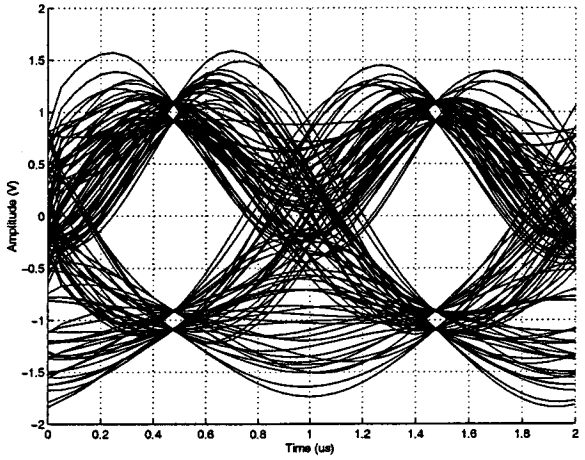


Figure 4.9: Eye diagram of the differential detectors impaired by phase imbalance

phase constellation diagram of Figure 4.10. This illustration clearly displays the cluster of two points distributed around the ideal constellation point. Like the DC offset, the clusters become less distinct when additional noise is present, but the clustering effect remains.

4.3.4 BER Performance

Figure 4.11 shows the BER performance of the IF differential detector for three modulator phase imbalances. The performance of the baseband differential detector is similar for this impairment. As expected, the larger the phase imbalance, the

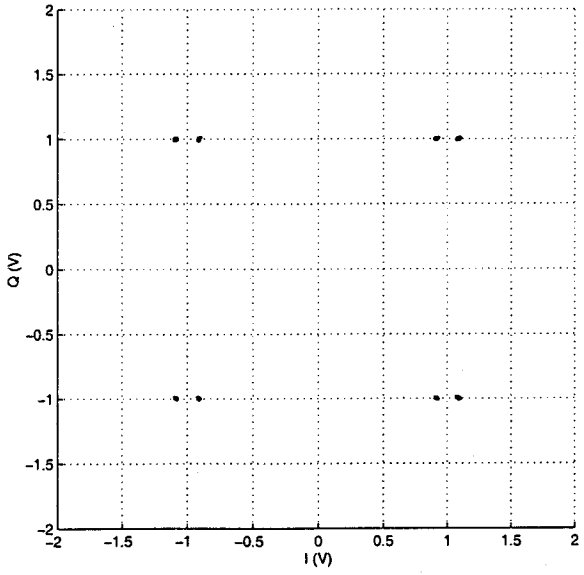


Figure 4.10: Constellation diagram of the differential detectors impaired by phase imbalance

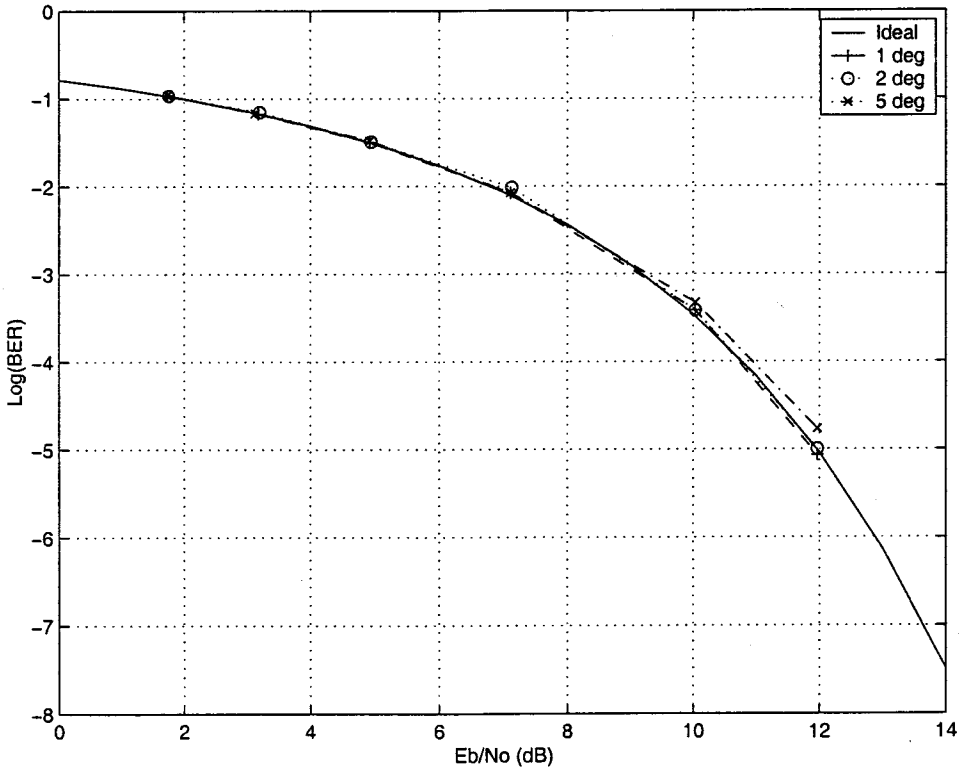


Figure 4.11: BER performance of the detectors impaired by phase imbalance

larger the BER performance degradation. At a BER of 10^{-4}, implementation losses of 0.02 dB, 0.05 dB, and 0.2 dB occur for phase offsets of 1°, 2°, and 5° respectively.

4.3.5 Compensation Techniques

This impairment is most easily compensated in the transmitter of the system. If prior knowledge of the magnitude of the phase imbalance is known, the levels of the inphase and quadrature voltages can be pre-adjusted in the transmitted signal to perform an inverse phase adjustment. This calculation can be made in a processor or in a lookup table, when the phase imbalance is assumed to be stationary.

If the phase imbalance is not static, a complicated control structure is required in the receiver or transmitter. The phase imbalance must be distinguished from the other impairments. In order to isolate this impairment, the other impairments causing rotation effects must be first compensated prior to compensating the phase imbalance. It may be possible to jointly compensate this impairment with the other impairments like DC offset and frequency offset that also cause phase constellation rotation.

4.4 Limiter

In many applications, the received signal strength varies over a wide range (up to 100 dB) [10]. To stay within the linear region of amplifiers and mixers, as well as the input range of analog to digital converters, it is necessary to keep the input signal level approximately constant. This function is often called automatic gain control (AGC).

Limiters can be used as a form of AGC to keep the input level constant. This is a simple technique to keep the signal level in the proper range, when compared to other methods of automatic gain control. The other techniques typically require feedback loops or other complicated methods to maintain a constant signal level. Since limiting is a nonlinear function, matched filtering must be done prior to limiting to maintain optimal receiver performance.

4.4.1 Hard Limiter

A baseband hard limiter generates a bipolar output signal based on the sign of the input signal. The output signal of an ideal baseband hard limiter, $y(t)$, is defined as

$$y(t) = \text{sgn}[z(t)] = \begin{cases} +A & z(t) \geq 0 \\ -A & z(t) < 0 \end{cases} \tag{4.11}$$

where $z(t)$ is the input to the hard limiter, sgn denotes the signum function, and A is the limiter output level.

A bandpass hard limiter maintains a constant RF signal envelope. The output of an ideal bandpass hard limiter, $y(t)$, is defined as

$$y(t) = \frac{A}{\sqrt{z_I^2(t) + z_Q^2(t)}} z(t) \tag{4.12}$$

where z_I and z_Q are the quadrature components of the input signal, $z(t)$. The bandpass hard limiter is applicable to this application since the input signal is received at IF or RF frequencies.

4.4.2 Soft Limiter

Hard limiters are often replaced with amplifiers which are operated in the saturation region. This type of a limiter is termed a soft limiter, since a portion of the output signal is linear where the input signal is not driven to saturation. Soft limiting is often an undesirable effect introduced by the transmitter HPA.

The baseband soft limiter is defined similarly to Equation 4.11 with an additional linear region as

$$y(t) = \begin{cases} +A & z(t) > +A/K \\ Kz(t) & -A/K \leq z(t) \leq +A/K \\ -A & z(t) < -A/K \end{cases} \tag{4.13}$$

where K is the linear gain of the soft limiter outside of the saturation region.

The bandpass soft limiter is defined similarly to Equation 4.12, but also contains

a linear region. This limiter is expressed mathematically as

$$y(t) = \begin{cases} Kz(t) & -A/K < \sqrt{z_I^2(t) + z_Q^2(t)} < +A/K \\ A & otherwise. \end{cases} \tag{4.14}$$

4.4.3 AM/AM and AM/PM Conversion Effects

Non-ideal limiters are subject to both an AM to AM conversion effect and an AM to PM conversion effect. AM to AM conversion refers to a nonlinear output level variation in response to an input signal level variation to the device. In AM to PM conversion, the input signal level variation leads to a phase shift at the output of the limiter. Since this application uses phase modulation, it is expected that the system performance would be sensitive to the AM to PM conversion effect.

The combined effects of AM/AM and AM/PM conversion on an output signal, $y(t)$, based on a quadrature bandpass signal can be expressed as

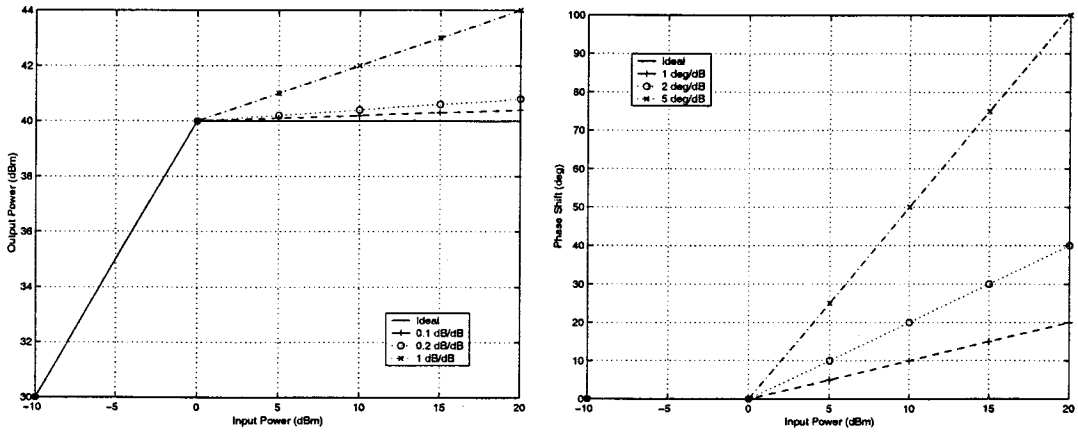
$$y(t) = f[A(t)] \exp(j2\pi f_c t + \phi(t) + g[A(t)]) \tag{4.15}$$

where $A(t)$ represents the instantaneous envelope of the input signal, f_c denotes the nominal bandpass frequency, and $\phi(t)$ is the instantaneous phase offset of the signal. The function, $f[\cdot]$, denotes the AM to AM conversion characteristic and $g[\cdot]$ represents the AM to PM conversion characteristic of the limiter.

Practical hard limiters have a dynamic range of 20 dB, with a typical AM to AM conversion effect of 0.1 to 0.3 dB/dB and an AM to PM conversion ratio of 1 to 2°/dB [33]. Soft limiters have a larger dynamic range than hard limiters, but still suffer from similar AM to AM and AM to PM characteristics.

4.4.4 Simulation Notes

The ideal limiter is modeled as a nonlinear amplifier in which all the signals are amplified to the saturation level. Thus, the simulated limiter is modeled as a soft limiter that amplifies all signals, except those of extremely low power, to the



(a) AM to AM conversion

(b) AM to PM conversion

Figure 4.12: Limiter characteristics

saturated level. For ease of simulation, the AM to AM and AM to PM characteristics are modeled in a piece-wise linear fashion, even though typical characteristics have smoother transitions between the the linear and saturation regions.

AM to AM effects are modeled in the amplifier by using a nonlinear output response based on the input power amplitude to the limiter. Figure 4.12(a) shows a number of different AM to AM conversion characteristics for the limiting amplifier and the associated amplifier magnitude output characteristic.

AM to PM conversion effects are modeled in the amplifier by using a nonlinear phase output response based on the input power level to the amplifier. Figure 4.12(b) shows a number of AM to PM conversion characteristics for the limiting amplifier and the associated amplifier phase characteristic.

4.4.5 BER Performance

Figure 4.13 shows the BER performance for the IF differential detector that incorporates a limiter impaired by a number of different AM to PM conversion characteristics. The simulated limiter characteristics were previously displayed in Figure 4.12. AM to PM conversions of 1°/dB, 2°/dB, and 5°/dB cause implementation losses of 0.1 dB, 0.4 dB, and 2.0 dB, respectively, at a BER of 10^{-4}.

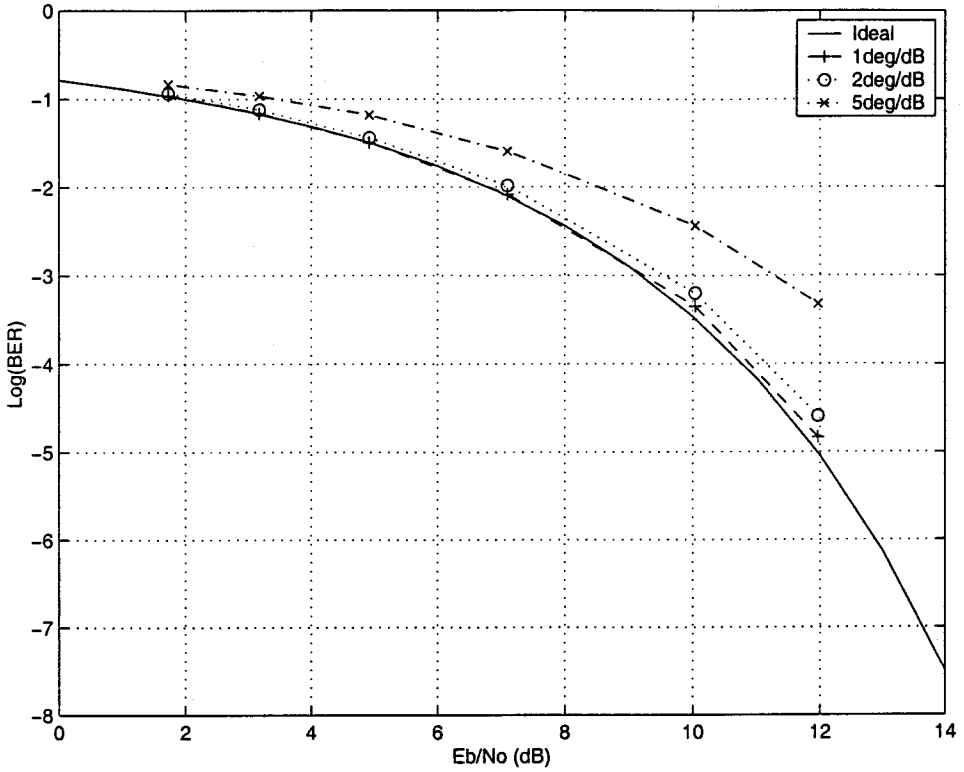


Figure 4.13: BER performance impaired by limiter AM to PM conversion

Simulations were also run for typical AM to AM conversion characteristics. For characteristics typically found in real limiters (< 0.5 dB/dB), there was no significant performance degradation so these results are not presented.

4.4.6 Detector Comparison

4.4.6.1 Frequency Discriminator Detector

The frequency discriminator detector normally contains a limiter in its receiver. This limiter is necessary so that the instantaneous frequency differences in the signal can be detected. This limiter is necessary in common FM detection methods such as the slope detector, quadrature detector, Foster-Seely detector, balanced discriminator, and zero-crossing detector that require the signal amplitude variation to be removed [12]. If a phase locked loop (PLL) FM detection method is used, the limiter is not required since the FM detection process is not amplitude sensitive.

4.4.6.2 IF Differential and Baseband Differential Detectors

Ideal versions of the IF differential and baseband differential detectors do not contain a limiter in the receiver and do not suffer the performance degradation associated with the limiter AM to PM characteristics. Practical differential receivers require a form of amplitude control to ensure the received signal falls within the dynamic range of the hardware used in the detection process. Amplitude control is also necessary to reduce fading effects in a wireless channel. A simple way to implement this amplitude control for detectors of this type is a limiter, so differential detectors may include this hardware and suffer from this impairment.

4.4.7 Compensation Techniques

Compensation techniques normally used in amplifier design to ensure low phase distortion can be used to improve the AM to PM in practical limiters. One compensation technique is predistortion, which adjusts the signal to provide an inverse AM to PM conversion so that the output of the predistortion and limiter combination does not suffer from AM to PM. Feedback circuitry can be used to adaptively adjust the AM to PM effect.

4.5 Up/DownConverter Phase Noise

Upconverters are used to translate the modulated signal to a higher bandpass frequency. Downconverters perform the inverse operation, translating a high frequency received signal to a lower intermediate frequency. These converters are often used in high frequency applications, since components used in the modulator and demodulator are more cost-effective at the lower intermediate frequencies.

A typical frequency downconverter is shown in Figure 4.14. The converter consists of an oscillator connected to a mixer to translate the incoming frequency. The mixer is followed by a filter to remove the unwanted image frequency. A highpass or bandpass filter is used to remove the lower image in an upconverter, while a lowpass

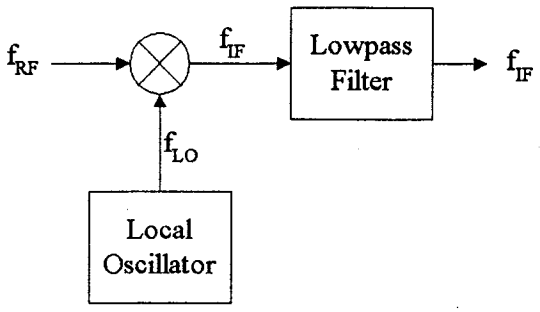


Figure 4.14: Typical downconverter

or bandpass filter is used in a downconverter.

Phase noise is caused by the oscillator used in the converter. The primary sources of the phase noise are oscillator instability and thermal noise.

4.5.1 Cause

Phase noise creates an instability in the oscillator phase used in the mixing or multiplication process with the incoming signal. This phase uncertainty causes additional phase modulation on the already modulated signal. The effective phase noise, $\mu(t)$, is given by

$$\mu(t) = \epsilon_n(t) + \delta(t) \tag{4.16}$$

where $\epsilon_n(t)$ is the thermal noise and $\delta(t)$ represents the oscillator instability due to flicker noise, shot noise, and other effects [31, 34, 35].

Phase noise is expressed on manufacturer data sheets relative to the main CW tone as a power density function (dBc/Hz). These points are measured at a number of logarithmic intervals. Figure 4.15 illustrates three typical phase noise power spectra for voltage controlled oscillators. The displayed curves are for oscillators with a translation frequency of around 3.5 GHz, which is similar to the upconverters and downconverters used in this application [33]. Table 4.2 summarizes the three characteristics that are shown in Figure 4.15. These three characteristics will be referred to as low, medium, and high throughout this section as noted in the illustration.

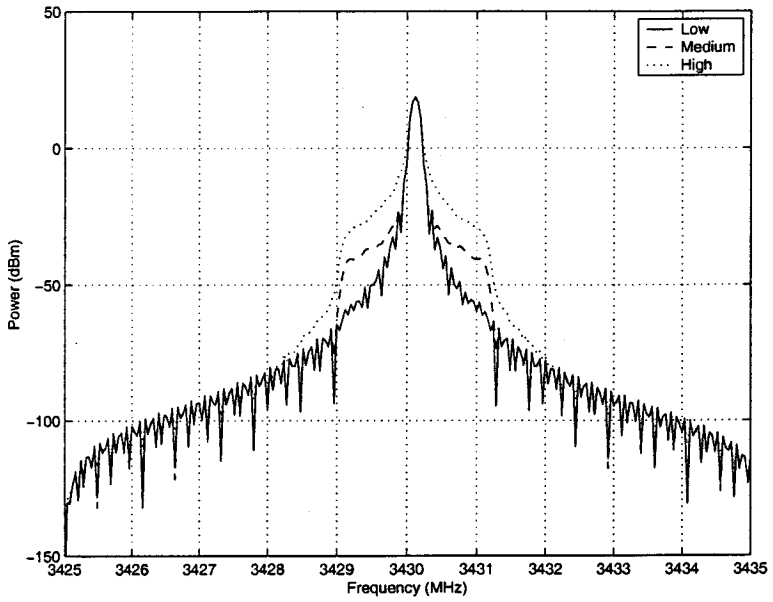


Figure 4.15: Typical oscillator phase noise characteristics

Table 4.2: Three typical oscillator phase noise characteristics

Frequency Offset (Hz)	*Low (dBc/Hz)*	*Medium (dBc/Hz)*	*High (dBc/Hz)*
1000	-60	-40	-30
10000	-90	-70	-50
100000	-110	-90	-70
1000000	-130	-110	-100

4.5.2 Simulation Notes

The effect of oscillator phase noise is modeled in the system through the use of the typical characteristic curves shown in Figure 4.15. The relative magnitude of the noise components are specified discretely for the simulations. Values that fall between between the specified values are logarithmically interpolated. The oscillator output takes into account the power of the main oscillator frequency component, as well as the frequency components derived from the phase noise characteristic.

4.5.3 Effect

4.5.3.1 IF and Baseband Differential Detectors

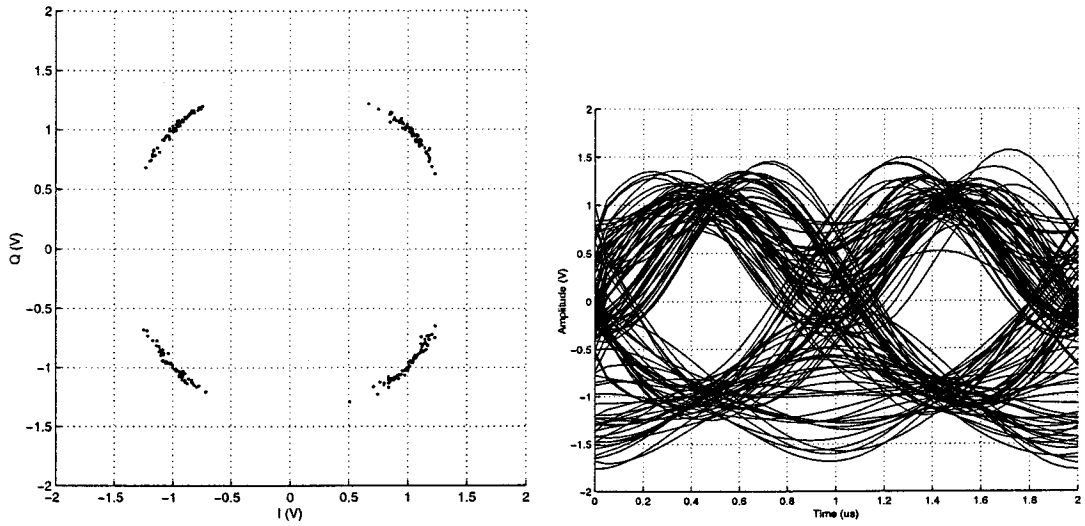
The detected constellation diagram is shown in Figure 4.16(a) for the medium phase noise characteristic. It can be seen that the phase noise increases the spread of the detected constellation points when compared to constellations not affected by phase noise. This variance is expected, since the phase noise modifies the phase differences detected at the receiver. The corresponding inphase signal component eye diagram is illustrated in Figure 4.16(b).

4.5.3.2 Frequency Discriminator Detector

The frequency discriminator eye diagram for the medium oscillator phase noise characteristic is shown in Figure 4.17. Like the differential detectors, the frequency discriminator eye diagram exhibits increased variance as compared to the detector with ideal frequency conversion. This variance is due to the modified phase trajectories caused by the random phase noise.

4.5.4 BER Performance

Figure 4.18 demonstrates BER performance of the IF differential detector when impaired by downconverter phase noise. This impairment is illustrated for the phase noise characteristics presented in Figure 4.15. Performance degradation at a BER



(a) Constellation diagram

(b) Eye Diagram

Figure 4.16: Differential detectors constellation and eye diagrams impaired by phase noise

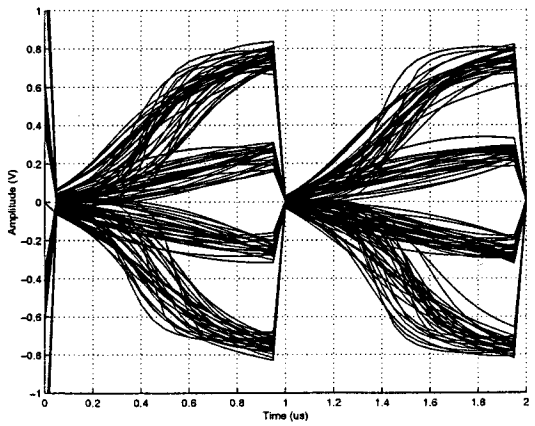


Figure 4.17: Eye diagram for the frequency discriminator detector impaired by phase noise

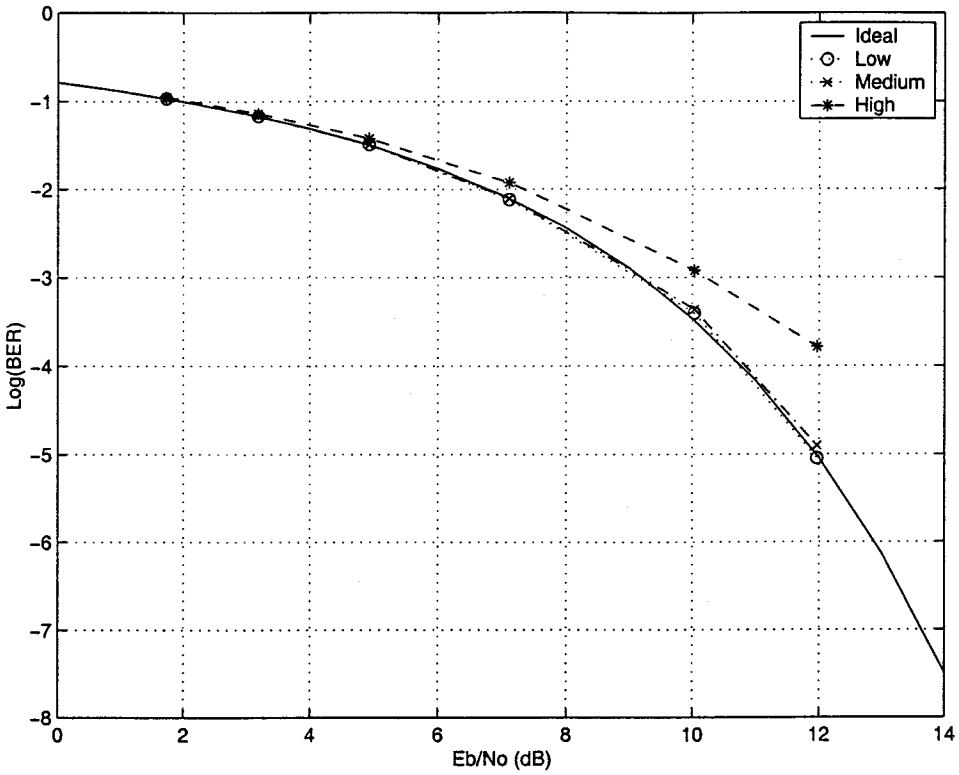


Figure 4.18: BER performance impaired by oscillator phase noise

of 10^{-4} is 0.05 dB for the low phase noise characteristic, while the medium and high characteristics have a degradation of 0.1 dB and 1.5 dB, respectively.

4.6 Symbol Timing Offset

4.6.1 Cause

Symbol synchronization is a necessity in digital communication systems in order to properly decode the transmitted waveform. It is necessary to correctly detect the beginning and end of the symbol period in order to sample the received waveform at the proper instant to minimize the bit error ratio.

Symbol timing synchronization is one of the most important aspects of the demodulator design because the optimal receive SNR is at the peak of the eye opening. In addition, recently developed receiver optimization techniques, such as fading compensation, are performed using the baseband signal sampled at the symbol tim-

ing [10]. Therefore, symbol timing recovery must be robust to frequency offset, DC offset, fading, and noise. In systems with bursty traffic, transmission efficiency increases when receiver circuitry is able to quickly acquire symbol timing information.

It is assumed that the receiver is not physically located in the same place as the transmitter. Thus, it is not possible for the receiver to directly lock to the transmitter reference clock. The transmitter must either multiplex a timing reference signal along with the transmitted signal or alternatively, the receiver must derive the symbol timing information from the received waveform. The second approach is more commonly used in practice, since it does not require additional channel power to be used for a reference signal [10]. Discussion will be limited to this approach in this section.

Symbol timing offsets between the receiver and the transmitter occur because they are not locked to the same reference source. Slight frequency differences between the sampling clocks of the transmitter and receiver result in phase shifts in the optimal receiver sampling point. These phase shifts are known as timing jitter and are a result of phase error which occurs as the recovery circuit attempts to track timing information in the receive signal.

The synchronization is normally performed in the receiver by a symbol timing recovery loop. The receiver symbol timing is preset when a received signal is detected. The recovery loop then adjusts the phase of the sampling clock in response to transitions in the receive signal in order to sample the received waveform as closely as possible to the optimum point.

4.6.2 Simulation Notes

The symbol timing offset error is modeled by shifting the experimental sampling point, t_k, relative to the ideal sampling point, t_0, such that $t_k \neq t_0$. The symbol timing offset, Δt, is defined as

$$\Delta t = t_k - t_0. \tag{4.17}$$

The symbol timing offset, t_{offset}, can be normalized in terms of the symbol rate,

such that

$$t_{\text{offset}} = \frac{\Delta t}{T_s} \tag{4.18}$$

where T_s is the symbol period and Δt is the timing offset of Equation 4.17.

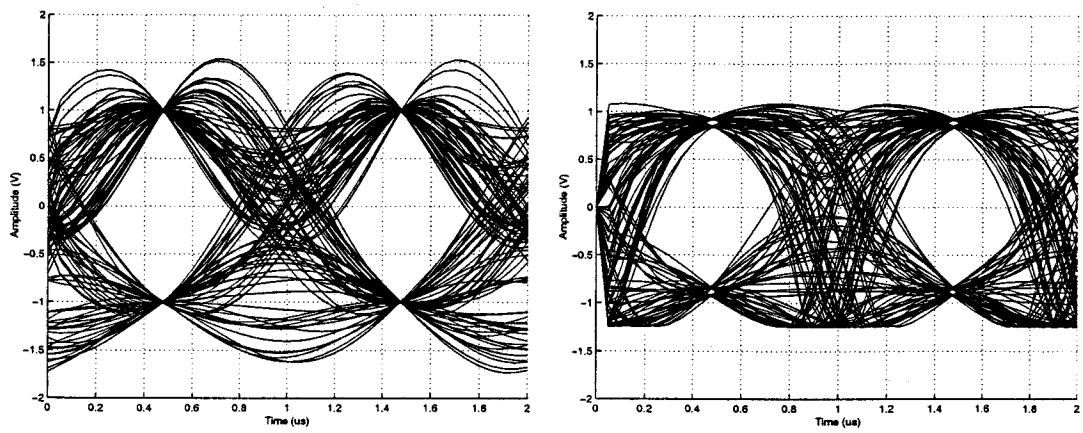
In the simulations for the detector types, the symbol sampling point is offset by fixed amounts relative to the ideal sampling instant. Timing offset is more realistically defined as a statistical process that varies around the nominal timing instant [36]. However, for ease of simulation, the timing jitter is instead modeled as discrete fixed offsets in order to demonstrate the symbol timing error tolerance required for a particular performance level.

4.6.3 Effect

4.6.3.1 IF and Baseband Differential Detectors

A symbol timing offset causes the detector to sample the received waveform at a distance away from the ideal sampling instant. Figure 4.19 shows eye diagrams for the differential detectors, both with and without a hard limiter present in the receiver. It can be seen in these figures that the eye diagram is less open as the distance away from the sampling point is increased. With a timing offset present, the detector is forced to make a decision at these sub-optimal points. Under noisy conditions, this offset increases the probability that the symbol will be detected incorrectly.

Figure 4.19(b) displays an eye diagram with a hard limiter present in the receiver. In this case, it can be seen that the eye closes more slowly than in Figure 4.19(a) as the distance from the ideal sampling point is increased. It is hypothesized that this is an advantage when confronted with a symbol timing impairment. However, at a low E_b/N_o, the detector with a hard limiter did not show any improvement in BER performance in simulation results. Nevertheless, it is believed that at high signal to noise ratios, the hard limiter does improve the BER performance, but this was not proven due to the lengthy amount of time required to simulate a sufficient number of bits through the detector.



(a) No hard limiter (b) With hard limiter

Figure 4.19: Eye diagrams for the differential detectors

With or without a hard limiter present in the detector, shifting the sample point 30% away from the optimal point of the detector places the eye diagram in the signal transition region. The detector is unable to make a reasonable decision regarding the transmitted signal in this area.

Figure 4.20 displays a constellation diagram for the differential detectors impaired with a timing offset of 10% ($t_{\text{offset}} = 10\%$). Sampling at the non-optimal point causes a spread in the detected constellation points. These points are spread around the ideal detected constellation points. This increased variance increases the probability of a symbol detection error.

4.6.3.2 Frequency Discriminator Detector

The frequency discriminator detector is also affected by symbol timing offset. This detector normally has a hard limiter in the front end of the receiver as shown in Figure 3.10. This limiter removes amplitude variation, since most FM detectors are sensitive to envelope variation and rely on being able to distinguish the frequency deviation independently of the amplitude variation.

A sample eye diagram for the frequency discriminator detector is shown in Figure 4.21. It has a similar characteristic as the differential detectors when a limiter

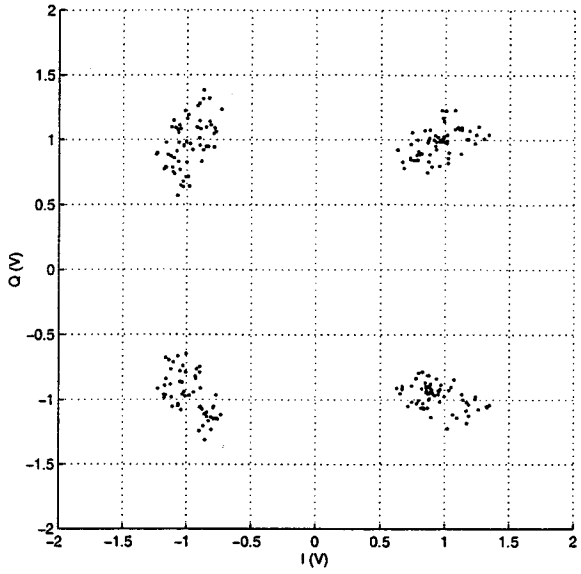
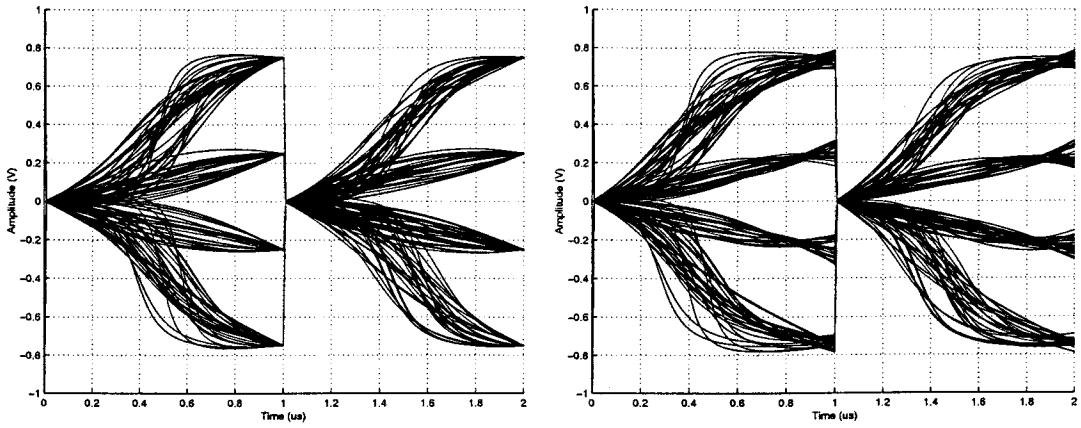


Figure 4.20: Constellation diagram for the differential detectors impaired by 10% symbol timing offset

is present in those detectors. The frequency discriminator detector relies on proper synchronization, since it integrates the frequency deviation over an entire symbol period. If symbol timing error is present, this integration includes part of the frequency deviation from the previous symbol and only a portion of the phase trajectory of the desired (current) symbol. This offset leads to an degraded BER performance, since the four-level eye diagram has increased variance at the detection point as shown in Figure 4.21(b). The ideal eye diagram, shown in Figure 4.21(a), does not exhibit this same variance.

4.6.4 BER Performance

Figure 4.22 shows the BER performance for the IF differential detector that is impaired by symbol timing offset. The BER performance was observed to be similar for the baseband differential detector. It can be seen that as the timing offset increases, the degradation in BER gets larger. For example, at a BER of 10^{-4}, there is negligible implementation loss for a 1% timing offset. However, offsets of 2.5%, 5%, and 10% have implementation losses of 0.1 dB, 0.3 dB, and 1.5 dB respectively.



(a) No timing offset

(b) Timing offset = 10%

Figure 4.21: Eye diagram for the frequency discriminator detector impaired by timing offset

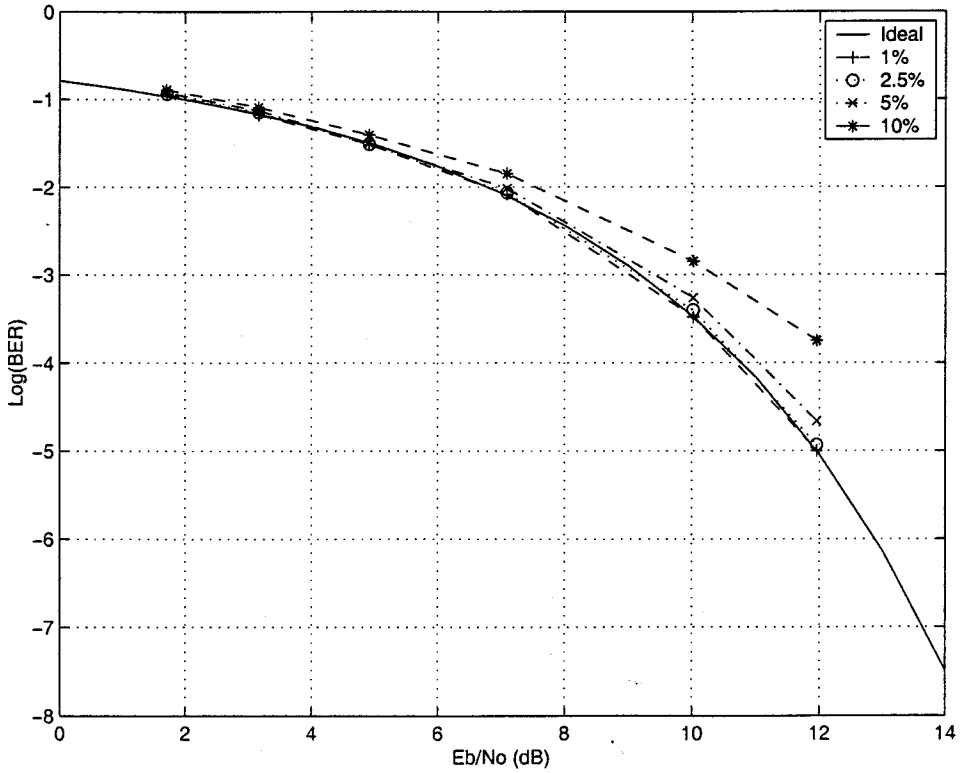


Figure 4.22: BER performance impaired by symbol timing offset

4.6.5 Timing Recovery Techniques

Timing recovery has been the subject of much research over the years. This research has focused on optimizing the symbol timing recovery methods for different modulation schemes and system characteristics. In addition, recent work has focused on joint estimation of carrier and symbol timing synchronization [37, 38].

One of the most common synchronization techniques is the early-late gate synchronizer [29]. This synchronizer assumes that the received pulse shape is symmetrical, which is true in $\pi/4$-DQPSK when a bit transition occurs. The early gate accumulator integrates the signal over the first half of the symbol period, while the late gate accumulator integrates the signal over the final half of the symbol period. When perfectly synchronized, the early gate and late gate integrations should be equal. If unequal, the timing clock phase can be advanced or retarded as appropriate, so that eventually the timing clock is properly synchronized.

Another common method of synchronization is the zero-crossing method [10]. This method can be implemented digitally using phase-locked loops. This scheme looks for a zero-crossing and assumes the optimum sampling point is half the timing clock period later. This method averages the zero-crossing jitter, which is extreme in filtered $\pi/4$-DQPSK where the jitter for zero-crossings is approximately 1/3 of the symbol period even under low noise conditions.

Two other methods are derived from the maximum likelihood estimation technique: the maximum amplitude method and the wave differential method [10]. Both these techniques entail block processing and require memory to implement.

The maximum amplitude method stores amplitude values for a number of samples. The periodic samples are averaged over a number of symbols to determine which sample within the symbol period has the highest average value. The sample clock is adjusted to this maximum average sample point.

The wave differential method is similar to the maximum amplitude method. It determines the sampling points at which the slope is closest to a zero value, determining the maximum/minimum value point within a symbol period. This

point is chosen as the best sampling instant and the symbol timing is adjusted accordingly.

4.7 Sub-Optimal Receiver Filtering

In an ideal digital communication system, a filter is used in the receiver that is matched to the characteristics of the received signal. This matched filter takes into account the attributes of both the transmitted signal and any channel effects. In a real system, it is not possible to have knowledge of all the factors that affect the received signal, since the channel is subject to time-varying phenomena.

In place of ideal matched filters, raised cosine filtering is often used in digital communication systems. The raised cosine filter response is typically split between the transmitter and receiver by using two identical root raised cosine filters as discussed in Section 3.1.1. This family of filters minimizes the effects of noise and intersymbol interference to provide optimum filtering for a transceiver in an AWGN environment [29].

4.7.1 Sub-Optimal Filter Realizations

4.7.1.1 Analog

It is not possible to realize a square root raised cosine filter using analog hardware components. Existing research discusses the approximation of the raised cosine filter response using common analog filter types. Approximating a full raised cosine filter with a roll-off factor of 1.0 using a second order Butterworth filter is discussed by Bank and Gavin [39]. Other articles mention using a fourth order Butterworth filter to approximate the root raised cosine filter with an excess bandwidth of 0.35 that is used in this application [13, 15].

The frequency response of a fourth-order Butterworth filter that approximates the response of a RRC filter is shown in Figure 4.23. The filter cut-off frequency is chosen to be $0.57/T_s$, which is slightly larger than the ideal RRC cutoff of 500

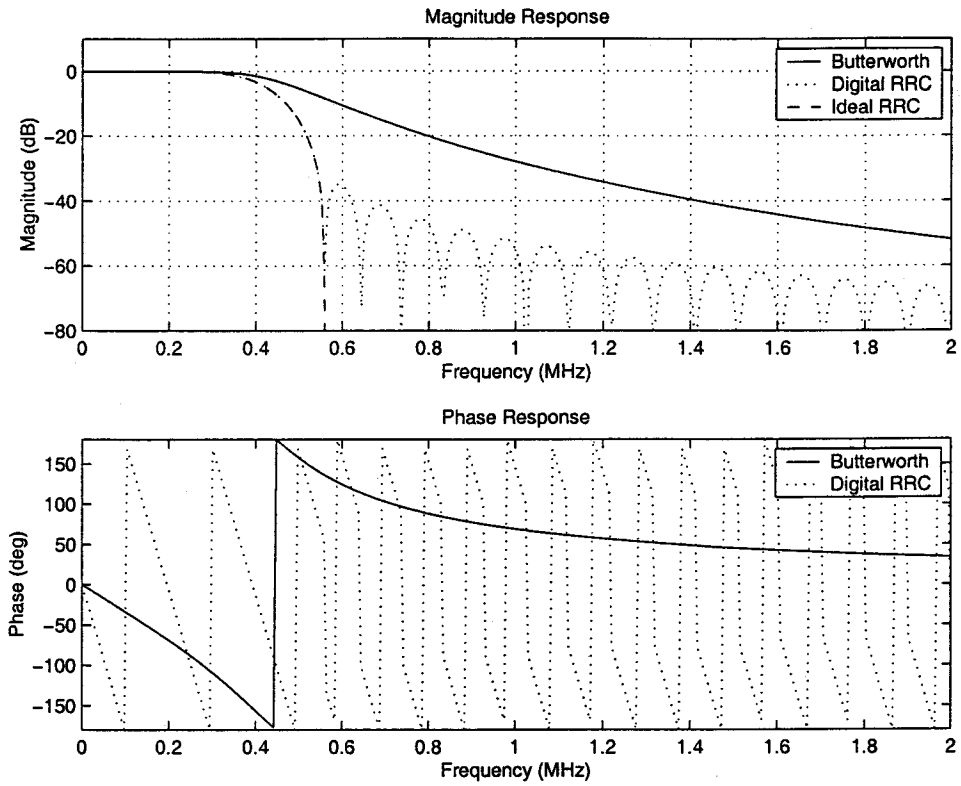


Figure 4.23: Frequency response of sub-optimal receive filters

kHz for this application. This larger bandwidth results in an increased noise level at the filter output. It can be seen that the magnitude response of the maximally-flat Butterworth filter is very similar to the RRC filter over the filter passband.

The phase response of a RRC filter is linear, while the Butterworth filter has a nonlinear phase response at the cutoff frequency. To more closely approximate the RRC filter and to reduce group delay distortion, it is necessary to move the effects of the nonlinear phase response outside of the passband. This group delay distortion causes performance degradation in systems that use phase modulation, since the detected phase is distorted.

The stopband rejection of the low order Butterworth filters is not as good as the RRC filter. Higher order filters would provide better stopband rejection, but at the expense of increased group delay distortion around the cutoff frequency.

The BER performance of a modem that incorporates a fourth order Butterworth receive filter in place of the optimal RRC filter is shown in Figure 4.24. The sub-

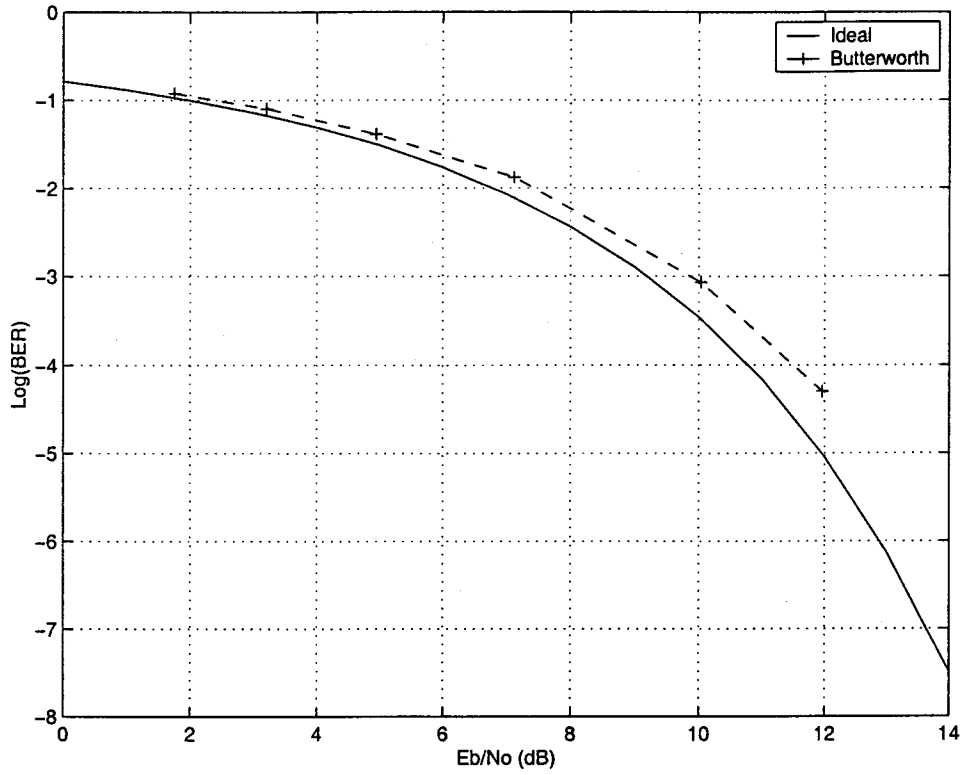


Figure 4.24: BER performance impaired by sub-optimal filtering

optimal analog filtering causes a performance degradation of 0.7 dB at a BER of 10^{-4}. A compensation technique to improve the BER performance of this degradation is described in Section 5.11.

4.7.1.2 Digital

It is possible to implement raised cosine filters using a digital filter and to achieve the desired magnitude characteristic with a linear phase response. However, it is not possible to get an ideal raised cosine response, since this requires an infinite filter impulse response. Practical realizations of the filter truncate the impulse response after a number of symbol periods.

As can be seen in Figure 4.23, the digital implementation of the RRC filter closely approximates the magnitude response of the ideal RRC filter throughout the passband. The phase response of the digital implementation is also linear over the filter passband, which eliminates the group delay distortion observed in the analog

version of this filter.

The truncation of the filter impulse response leads to sidelobes in the frequency response of the digital implementation of the RRC filter when compared to the ideal RRC filter. These sidelobes reduce the stopband rejection of the filter, and allow noise and other frequency components outside of the passband to have a greater effect on the signal.

Truncation of the filter impulse response presents a tradeoff between performance and implementation complexity when designing the digital filter. A longer filter requires more taps, which increases the hardware complexity of the filter. A longer filter also introduces additional delay into the system, which may impact the overall packet throughput. However, a shorter filter less closely approximates the ideal RRC filter and has poorer noise rejection due to the stopband isolation.

A digital filter also suffers from finite numeric effects. Common numeric data formats include 32-bit floating point precision, as well as 32, 16, 8, or other bit widths of fixed-point precision. Floating point realizations have better performance since they have a higher dynamic range and suffer from less numerical truncation than fixed point computations. However, they require increased complexity and higher power consumption devices.

Figure 4.25 shows the BER performance of a receiver that incorporates a digital RRC filter. The impulse response of each filter is truncated after different numbers of symbol periods. It can be seen that with eight and sixteen symbol length truncation, the BER performance very closely approximates the performance of an ideal RRC filter that has an infinite length impulse response. Six symbol length truncation causes a 0.1 dB implementation loss at a BER of 10^{-4}. The four symbol length filter causes a 1.0 dB implementation loss at the same BER.

The system designer must make a tradeoff between complexity of the implementation and the desired response of the filter. Fixed point implementations are suitable for programmable digital hardware and are discussed in more detail in Chapter 5.

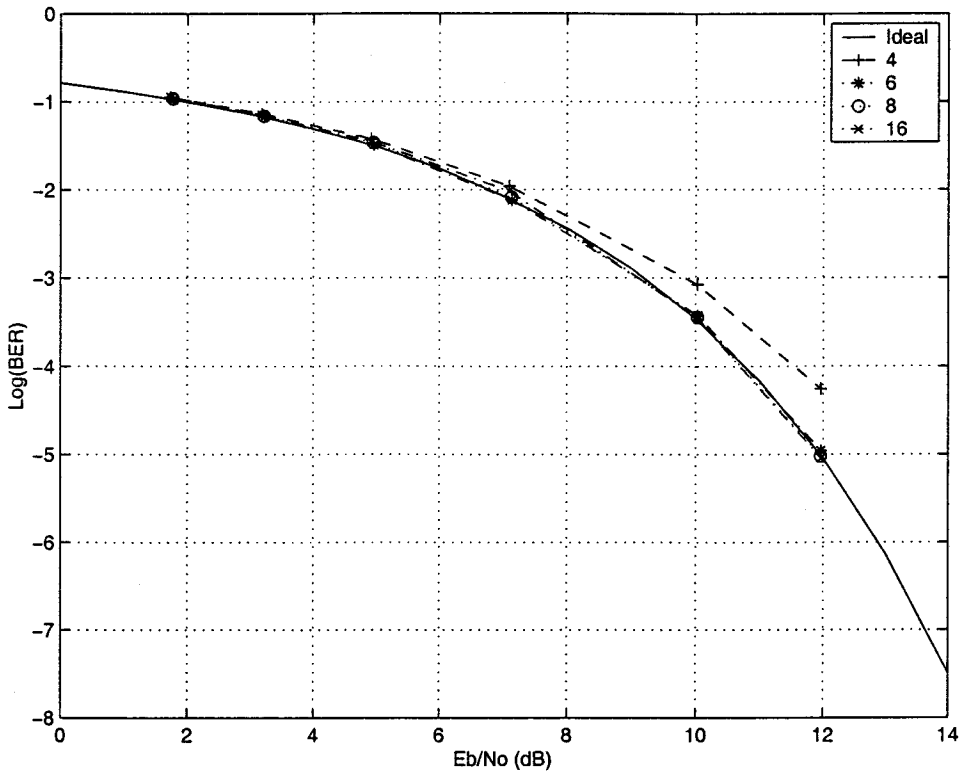


Figure 4.25: BER performance of receivers with truncated root raised cosine filtering

4.7.2 Filtering Considerations in the Demodulators

4.7.2.1 Frequency Discriminator Detector

The frequency discriminator detector lends itself well to analog hardware implementation, since analog FM demodulators have better performance than digital ones. Therefore, this detector is likely to use analog filtering in the receiver. Since the RRC filter is not realizable in analog hardware, the BER performance of a frequency discriminator detector will be degraded due to the sub-optimal characteristics of the receive filter.

However, the simplified hardware complexity of the analog receive filter makes it attractive in a detector realization. In addition, the delay through the analog filter is negligible compared to the several symbol delay present when using the digital filter. This reduces the overall modem delay and can result in better packet transmission efficiency, particularly in systems with bursty data communications.

4.7.2.2 Baseband Differential Detector

The baseband differential detector lends itself well to a digital hardware implementation. Thus, the baseband differential detector will normally use lowpass digital filters to perform the optimal RRC filtering. Since it is possible to perform square root raised cosine filtering digitally, this detector only suffers from the degradation caused by the finite numeric precision effects and impulse response truncation. The designer can trade required BER performance for computational efficiency and hardware complexity. This detector also has an advantage since the filtering can be performed at baseband. This is an advantage since the baseband filtering can be performed at a lower sampling rate than the bandpass equivalent.

4.7.2.3 IF Differential Detector

The IF differential detectors can be implemented either using analog or digital hardware components. When using analog components, the IF differential detector faces the same challenges as the frequency discriminator detector. When using digital components, it suffers the same effects as the baseband differential detector. However, the IF differential detector requires bandpass filtering, which typically increases the sampling rate required for the filter realization.

4.8 Combined Impairments

Up to this point in the chapter, impairments have been considered in isolation. Each impairment was added to the system while the remainder of the modem components were modeled as ideal.

Scenarios allow the effects of multiple concurrent impairments to be observed. These scenarios combine most of the impairments described in this chapter – DC offset, phase imbalance, symbol timing offset, AM to PM conversion, phase noise, and frequency offset. The magnitude of the impairments is varied in each scenario to observe the effect on the overall BER performance.

Table 4.3: Combined impairment magnitudes used in various scenarios

Impairment	*Scenario A*	*Scenario B*	*Scenario C*
DC offset	1%	2.5%	2.5%
Phase imbalance	1°	2°	2°
Timing offset	2.5%	2.5%	2.5%
Limiter AM to PM	1°/dB	2°/dB	2°/dB
Phase noise	low	medium	medium
Frequency offset	0%	0%	2.5%

Table 4.3 describes the magnitude of the impairments used in each scenario. The first scenario (Scenario A) resembles a modem with high quality components; very low levels of distortion are present for each impairment (typically 1%). The second scenario (Scenario B) describes a modem with poorer components than in the first scenario, but which still has reasonable performance. In Scenario B, the magnitude of the impairments is typically 2.5%. The third scenario (Scenario C) demonstrates the effect of one large impairment (frequency offset of 2.5%), while keeping the magnitude of the other impairments the same as in Scenario B. All the scenarios incorporate digital RRC filters that are eight symbols in length. Only Scenario C includes frequency offset, since it was expected that this dominant impairment would overshadow the effects of the other impairments.

The BER performance of the three scenarios is shown in Figure 4.26. As expected, Scenario A has better BER performance than Scenarios B and C, since the magnitudes of the impairments are smaller. For example at a BER of 10^{-4}, the degradation is 0.3 dB for Scenario A, while degradations of 1.0 dB and 2.5 dB are present for Scenarios B and C, respectively.

In Scenarios A and B, the dominant impairment is limiter AM to PM. It causes the majority of the performance degradation observed in the scenario, with the remainder of the impairments also contributing to the overall degradation. In Scenario C, the small amount of frequency offset (2.5%) causes considerable degradation. In Scenario C, the frequency offset is the only impairment with a different magnitude than in Scenario B which indicate that it is the major cause of the greatly increased

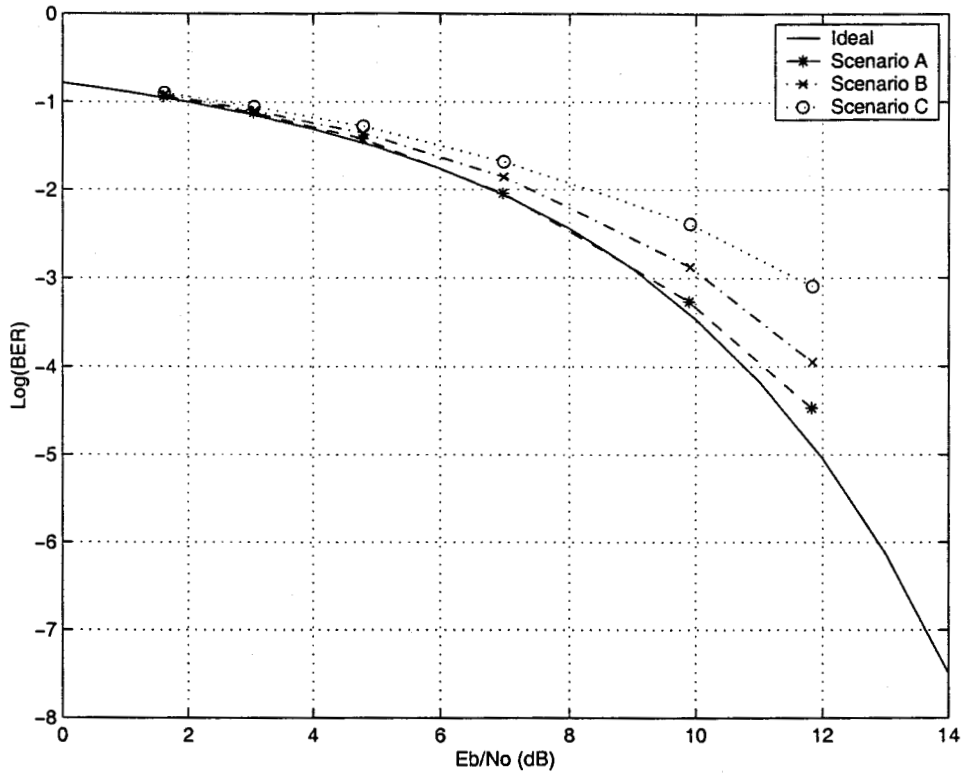


Figure 4.26: BER performance of combined impairments

degradation in this scenario. As expected, the remainder of the impairments contribute, but to a lesser extent, to the overall performance loss in Scenario C.

It is interesting to note that in all scenarios, the combined impairment loss is greater than the sum of the individual impairments. This demonstrates that the nonlinear effects of each impairment cause a cumulative effect that worsens as the impairments become greater.

4.9 Impairment Discussion

The impairments discussed in this chapter each caused BER degradation, but to varying degrees. The most severe impairment studied is the frequency offset impairment, which causes a performance degradation of 1.2 dB at a BER of 10^{-4} with an offset of 2.5%. Frequency translation errors are more severe at high frequencies (i.e. 3.6 GHz) than at lower frequencies (900 MHz), since the magnitude of frequency

error caused by the oscillator instability is proportional to the translation frequency. The frequency error caused by the LO is significant relative to the symbol time. For this application, the modems will be typically subjected to a time-variant frequency offset of at least 10% due to these difficulties in maintaining carrier frequency synchronization between the receiver and transmitter. Since degradation is extreme at this offset, the severity of this effect mandates the implementation of carrier frequency synchronization circuitry in the modem. The designer must choose an appropriate frequency synchronization method to ensure the modem has reasonable BER performance.

Another severe impairment is the DC offset effect. This impairment causes a BER degradation of 0.2 dB at a BER of 10^{-4} with an offset of 2.5%. It is common in a practical circuit to be faced with an offset of ± 50 mV, which corresponds to a DC offset of 2.5%. Fortunately, it is simple to compensate this impairment by fine-tuning the circuit to reduce any static DC offset. Time varying DC offset, which may be caused by temperature sensitivity, requires adaptive compensation.

Another potentially severe impairment is symbol timing offset. This impairment causes a performance degradation of 0.2 dB at a BER of 10^{-4} with a timing offset of 2.5%. The timing offset represents the average jitter observed in a practical circuit. Symbol timing circuits for bursty communications are faced with a trade-off between the speed of initial timing acquisition and the amount of jitter encountered thereafter. The tolerance of the symbol timing circuitry must be controlled so that this impairment does not cause severe BER degradation.

Practical modems will require automatic gain control to ensure that the incoming RF signal is within the receiver dynamic range. A limiter can be used to provide the AGC when faced with a fading environment. Limiter AM to PM conversion of $2°/\text{dB}$ causes a BER degradation of 0.4 dB at a BER of 10^{-4}. If the BER degradation caused by the limiter is too extreme, it may be necessary to compensate the AM to PM conversion of the limiter or to instead use a more complicated linear AGC that requires a rapid response time in burst mode.

Filter design is an important consideration in a modem realization. A designer

must recognize the degradation caused by the filter realization. If some degradation can be tolerated, the simple Butterworth filter may have sufficient performance, while reducing the modem implementation complexity. However, if better performance is required, a digital filter realization of an appropriate symbol length must be used.

Phase noise and phase imbalance cause smaller BER degradations than the other impairments. As such, it is unlikely compensation would be implemented for these impairments. For typical component impairments, the degradation of these impairments is insignificant relative to other impairments in this chapter. Compensation for these impairments should only be provided in cases where BER performance cannot be sacrificed at any cost.

4.10 Summary

Many impairments are present in a typical communication system. These impairments are caused by deviations from the ideal in the transmitter and receiver components. Some common impairments in a communication system are frequency offset, DC offset, phase imbalance, limiter AM to PM conversion, phase noise, symbol timing offset, and sub-optimal filtering. In general, one is faced with a trade-off between modem simplicity and performance degradation due to increased impairments.

Frequency offsets occur in a communication system due to the difficulties in maintaining frequency synchronization between the transmitter and receiver. The frequency offset causes a phase offset in the detectors.

DC offset effects cause increased variance in the detected levels at the sampling points. This variance is caused by phase shifts that do not correspond to the ideal $\pm\pi/4$ or $\pm 3\pi/4$ phase transitions. The variance results in clusters of four points around the ideal detection point.

Quadrature modulators create a phase imbalance when modulating a complex signal. This imbalance is inherent in the modulator, since it is difficult to produce a

precise 90° shift between the inphase and quadrature ports of the modulator. Phase imbalance manifests itself in the detector output as two clusters around the ideal detection point, due to the different phase trajectories traversed by the imbalanced signal.

Limiters are commonly used in communication receivers as a simple form of automatic gain control. The limiter is required in most forms of the frequency discriminator detector, and will be present in some implementations of the differential detectors. Practical limiters are impaired by AM to AM and AM to PM conversion effects. The BER performance of the detectors is not significantly affected by AM to AM characteristics of practical limiter implementations. However, the performance is affected by the AM to PM conversion effects. This effect is profoundly felt, since the $\pi/4$-DQPSK modulation scheme is dependent on the signal phase characteristics.

Phase noise occurs in downconverters and upconverters due to the instability of the oscillator used to provide the reference frequency signal. The phase noise causes increased variance at the detector sampling points, due to the random phase variations in the signal.

Symbol timing error is present in receivers because it is difficult to synchronize the phase of the receiver symbol timing clock to the received signal. The timing offset tolerance must be carefully controlled to limit the amount of degradation caused by the offset from the ideal sampling point.

One of the most difficult parts of the detectors to implement is the receive filtering. This is particularly true in the frequency discriminator detector and the IF differential detector where the required filter is bandpass in nature, although this requirement can be reduced if a low IF frequency is used. The baseband differential detector has an advantage over the other two detectors, since filtering can be performed at baseband. It is not possible to implement the optimal RRC filtering when using an analog filter as the receive filter. For this reason, sub-optimal Butterworth filters are often used instead. The Butterworth filters provide a reasonable approximation to an RRC filter and also cause less signal delay, but cause additional BER

performance degradation. Digital RRC filters also suffer from implementation loss, which is caused by the truncation of the filter impulse response.

The worst impairment demonstrated in this chapter was frequency offset. This impairment must be compensated for reasonable performance. Another severe impairment that is likely to be compensated is DC offset. Symbol timing recovery must be implemented so the modem is able to detect the received signal at the proper sampling point, with low jitter and a fast response time. The limiter AM to PM conversion impairment may be compensated, but performance is not degradaded to the point where compensation is mandatory. Phase noise and phase imbalance cause small degradations when using typical components and are unlikely to be compensated.

Scenarios illustrate the effect of concurrent impairments in the detectors. The combined degradation was greater than the sum of the individual impairments in each scenario.

Chapter 5

DETECTOR DESIGN CONSIDERATIONS

5.1 Overview

The previous chapter discussed impairments that affect the BER performance of the three $\pi/4$-DQPSK demodulator structures. In that analysis, the detectors were composed of ideal components except for the single component that caused the impairment.

This chapter discusses the design of the detector structures that were originally presented in Chapter 3. The receivers described in this chapter use digital signal processing to accomplish the detection process. The digital designs lend themselves to digital hardware realizations. The BER performance of the digital realizations is characterized, as well as their implementation complexity. The trade-offs between performance and complexity are discussed. The detector designs are compared when faced with a number of typical impairments as described in the previous chapter.

Finally, a combined digital transmitter and analog detector is presented. The BER performance of this modem is compared to the other detector implementations. This detector illustrates how the realization can be simplified by using analog filtering instead of digital filtering in the receiver.

5.2 Numerical Representation

In digital hardware, there are many ways to represent numerical data. These representations are called data formats and have significant effects on the accuracy of digital signal processing algorithms. The simpler formats (fixed point numbers) provide reduced implementation complexity, but lead to poorer arithmetic performance. More complicated formats, like floating point number representations, have much better mathematical performance, but have very high implementation complexity [40].

The two's complement format was chosen for the digital realizations presented in this chapter. This format was chosen for its simple hardware design, since addition and subtraction can be performed using the same hardware logic.

In the two's complement format, one bit is used to represent the sign of the number. The remainder of the bits represent the magnitude of the number. All positive numbers are represented with a zero for the sign bit. A negative number is formed by complementing the associated positive number and adding one. Using two's complement format, it is possible to represent numbers ranging between -2^{N-1} to $2^{N-1} - 1$ when using N bits to represent the numeric data [40].

In the designs presented in this chapter, three different bit widths are considered – 16, 12, and 8 bits. At the input of the detector, the sampled waveform is represented numerically in the two's complement format. In each case, one bit is used to represent the sign of the number, while the remainder of the bits represent the magnitude.

An undesirable effect that occurs when using fixed point numbers is data overflow. It is caused when arithmetic operations produce a result that is too large to represent with the bits available. When confronted with this problem, the designs in this chapter saturate at the largest positive or negative value that can be represented, rather than performing wrap-around [41].

Fixed point arithmetic is only able to represent a numerical precision that is based on the available number of bits. When performing arithmetic computations,

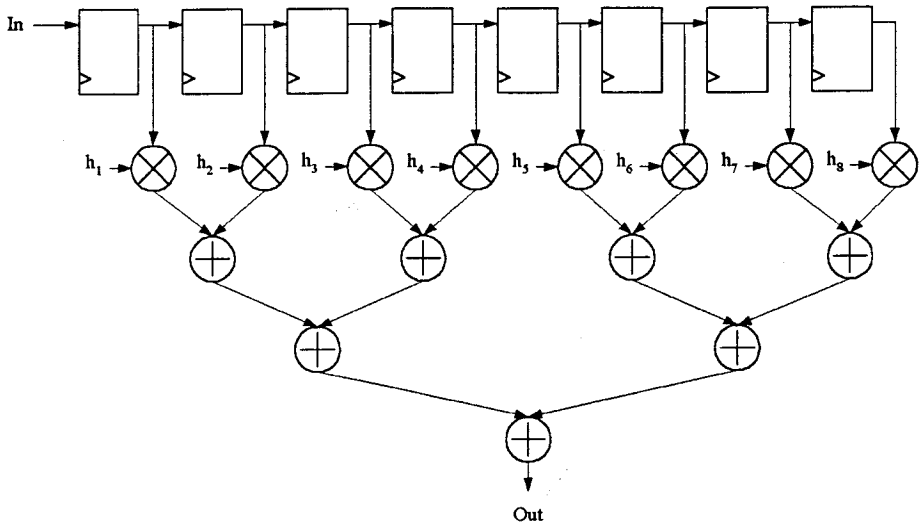


Figure 5.1: Conventional FIR filter architecture

the result of the computation must be either truncated or rounded. Truncation is simpler to implement than rounding, since it merely neglects (throws away) any bits of finer precision. Rounding requires more complicated hardware, but leads to lower arithmetic error, particularly in two's complement arithmetic [41]. For the designs in this chapter, rounding is used in intermediate arithmetic calculations.

5.3 Digital Filter Architecture

Filtering is required in all the detector realizations presented in this chapter. The filters are realized using finite impulse response (FIR) digital filters, that use a multiply and accumulate architecture. A hardware simplication can be used when the filter coefficients are symmetrical or antisymmetrical.

The conventional FIR filter architecture is shown in Figure 5.1 [40]. The architecture is illustrated for an 8 tap filter, but is scalable for a larger number of taps. The filter consists of a number of registers, multipliers and adders. Each register output is called a tap and is multiplied by the appropriate filter coefficient. After multiplication, the products are summed together to produce the filter output. An 8 tap filter using this conventional architecture consists of 8 registers, 8 multipliers, and 7 adders.

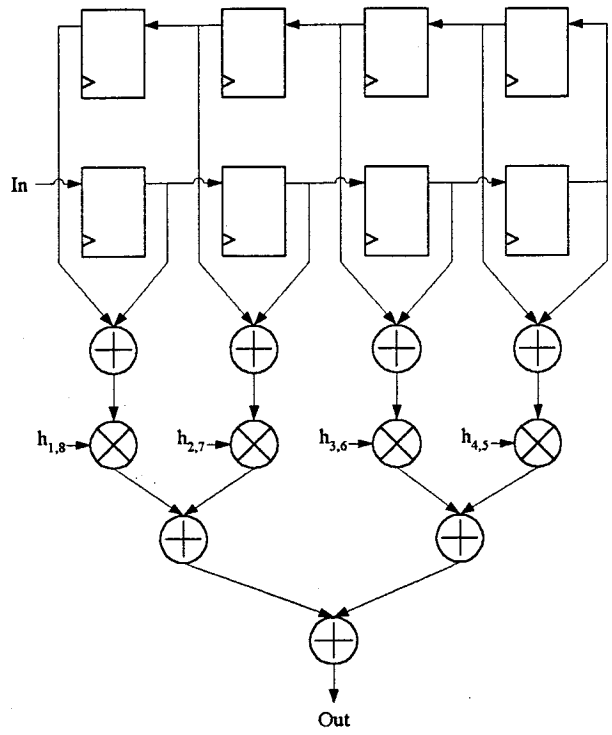


Figure 5.2: Symmetrical FIR filter architecture

Figure 5.2 shows an improved filter architecture, which can be used when the filter coefficients are symmetric or antisymmetric. The symmetry allows the symmetric (antisymmetric) coefficients to be added (subtracted) before the multiplication takes place. This lowers the number of required multipliers by a factor of 2, which is a significant savings since multipliers are normally much more complex to implement in digital hardware than adders. An 8 tap filter using this architecture uses 8 registers, 4 multipliers, and 7 adders. This is a savings of 4 multipliers compared to the conventional FIR filter architecture.

5.4 Detector Characteristics

The detector realizations in this chapter share a number of common traits that are based on the wireless application described in Chapter 1. The data rate is 2 Mbps, which corresponds to a symbol rate of 1 MHz. The RF channel frequency of the application is 3500 MHz.

The channel frequency is downconverted to an IF frequency of 4 MHz prior to detection. This IF frequency was chosen, so that a low sample rate could be used in the detectors without introducing aliasing.

The A/D converter at the input of the detector is operated at 16 MHz, which provides samples at the rate of 16 samples/symbol to the detector. This sample rate was chosen since it is the same rate that was used in the simulations in the previous chapter. It allows the simulation results of this chapter to be easily compared to those results.

This sample rate also provides other advantages. It satisfies the Nyquist criterion, so that no aliasing is introduced in the detectors. In addition, it provides enough timing resolution to determine accurate symbol timing. Finally, using this sample rate allows multiplierless mixing to baseband for the baseband differential detector as described later in Section 5.5.1.1.

The samples are provided by the A/D converter in three different numerical precisions – 16, 12, and 8 bit. These bit widths were chosen because they are common A/D output sample widths. The different widths are used to provide performance and implementation complexity comparisons. After conversion to a digital format, the two's complement data format is used within the detectors for arithmetic operations.

5.5 Baseband Differential Detector

This section discusses two design variations of the baseband differential detector that was originally presented in Section 3.4.1. The first type, the constant sample rate detector (CRBB), maintains the same sample rate throughout all the detector components. The second type, the decimated sample rate detector (DRBB), reduces the number of samples used in the latter stages of the detector to reduce hardware complexity.

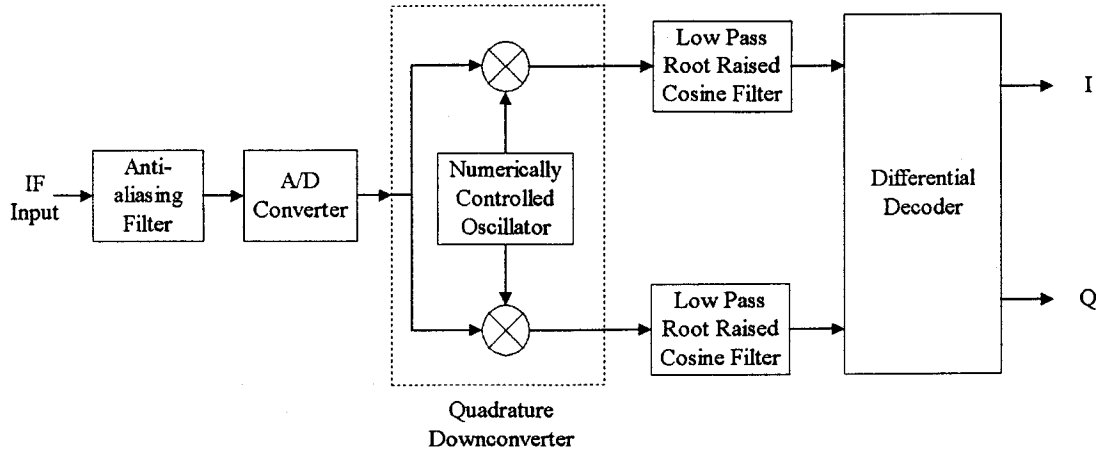


Figure 5.3: Block diagram of the constant sample rate baseband differential detector

5.5.1 Constant Sample Rate Detector

Figure 5.3 shows a block diagram of the constant sample rate baseband differential detector. In this detector, the sample rate is maintained at a constant rate throughout the entire detector.

The input RF signal is quantized by the A/D converter. The digitized signal is quadrature downconverted to baseband using a numerically controlled oscillator and multipliers. The resulting inphase and quadrature waveforms are lowpass filtered using the root raised cosine filters. The lowpass waveform is then delayed and multiplied to produce the output of the differential detector.

5.5.1.1 Quadrature Downconverter

The quadrature downconverter section converts the bandpass IF signal into two baseband signals that correspond to the inphase and quadrature components of the signal. This block consists of a numerically controlled oscillator and two multipliers.

The numerically controlled oscillator creates the sine and cosine waves to multiply with the incoming signal. The oscillator frequency must match the incoming IF signal frequency to convert the signals to baseband.

Sine and cosine functions are difficult to implement directly in digital hardware, since they require extensive calculations. To alleviate the computational complexity,

look-up tables are often used to implement these functions. Memory is used to store the trigonometric function values at a number of phase intervals. The stored values can be retrieved by fast, direct memory accesses that are addressed based on the current phase of the sine/cosine wave. Separate memories can be used for the sine and cosine functions, which allows the look-ups to be performed in parallel for look-up speed.

The symmetry of the trigonometric functions is exploited to reduce the memory required in the look-up tables. Since the sine and cosine functions exhibit odd and even symmetry through the four phase quadrants, it is only necessary to store one quarter (one quadrant) of the complete phase trajectory in memory. The remainder of the values can be derived, either through proper addressing or by negating the lookup value as appropriate.

The incoming signal is converted to baseband through multiplication with the oscillator sine/cosine wave using hardware multipliers. This mixing operation can be simplified so that hardware multipliers are not required. This optimization is applicable when the sampling rate is a factor of 4 greater than the incoming IF frequency that is to be mixed to baseband [40]. If the oscillator frequency has 4 samples per cycle (i.e. 1/4 of the sampling frequency), the cosine wave can be made up of the set of four samples, $\{1, -1, -1, 1\}$. The associated sine wave has a sample set of $\{1, 1, -1, -1\}$. Multiplying these sample sets with the incoming samples results in the incoming sample value passing directly through or being negated. Thus, the oscillator sine or cosine wave can be effectively multiplied with the incoming waveform without actually performing the multiplication.

5.5.1.2 Root Raised Cosine Filter

The baseband differential detector filters the baseband signal using a square root raised cosine filter, with a roll-off factor of 0.35. In this detector, a filter is necessary for each of the I and Q channels of the modulator.

For this realization, the filter impulse response is truncated after 8 symbol periods. The BER performance of a filter of this length was described in Section 4.7.1.2

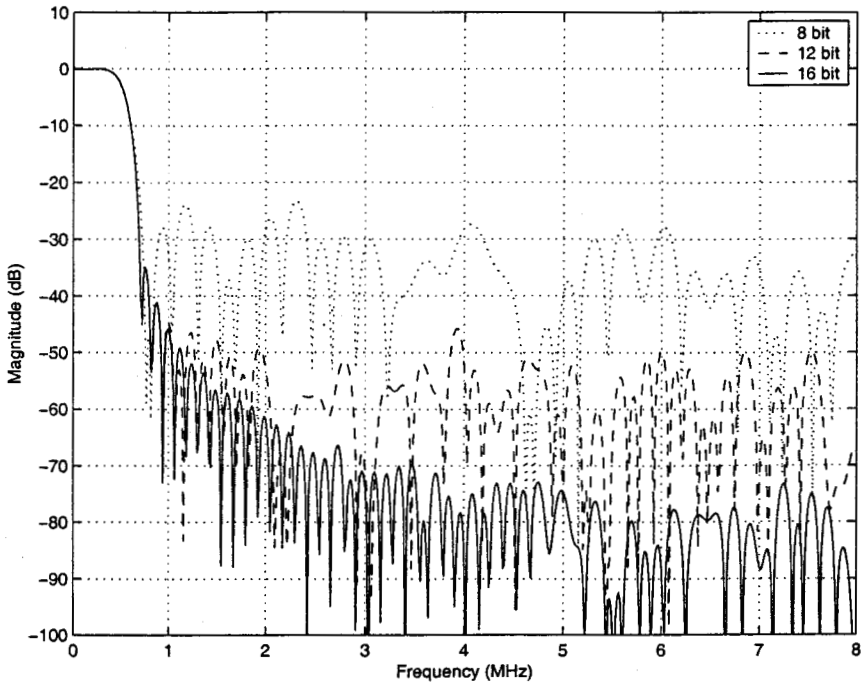


Figure 5.4: Frequency response of the lowpass root raised cosine filter

and was shown to not significantly reduce performance. The total length of the designed filter is 16 samples/T_s * $8T_s + 1 = 129$ taps. The filter introduces a signal delay that is half of the filter length, $4T_s = 4\mu s$.

Figure 5.4 shows the frequency response of the designed RRC filters for implementations of 8, 12, and 16 bit numeric formats. The lowpass cutoff frequency of the filters matches the signal bandwidth of 500 kHz. The 16 bit version of the filter provides 70 dB of rejection in the stopband, while the 8 and 12 bit versions provide 25 dB and 50 dB, respectively. All versions of the filter have very flat responses over the filter passband and have the same roll-off characteristic in the filter transition band.

The designed FIR filter has symmetric coefficients, so the filter architecture described in Section 5.3 was used to reduce implementation complexity. The I and Q filters each use 129 registers, 65 multipliers, and 129 adders.

5.5.1.3 Differential Decoder

After lowpass filtering, the differential decoding is performed according to the technique for $\pi/4$-DQPSK. The decoding consists of the delay and multiply operation as described in Section 3.4.1.

The delay is implemented using a number of registers arranged in a shift register configuration. Samples are clocked through the shift register to produce a one symbol delay. Multiplication is performed using hardware multipliers of the same bitwidth as the input signal. The signals are then added and subtracted using adders and subtractors of the same bitwidth as the input signal.

The differential decoding block requires 32 registers, 4 multipliers, 1 adder, and 1 subtractor.

5.5.2 Decimated Sample Rate Detector

Decimation is the process of removing samples from a stream of sample values. This process is used to reduce the required number of computations, which can be extreme when a high sampling rate is used. The end result is a reduced number of hardware components that have less stringent performance requirements.

The baseband differential detector lends itself well to using decimation in its implementation since the majority of its processing is performed at baseband. Once the signal is converted to baseband, the signal's frequency components are much lower than the sampling clock rate. Thus, it is possible to reduce the sample rate, without violating the Nyquist sampling criterion.

A block diagram of the decimated sample rate detector is shown in Figure 5.5. The quadrature downconverter is identical to the one discussed in Section 5.5.1.1. It translates the incoming IF signal into the inphase and quadrature component baseband signals. After conversion to baseband, the signal is filtered by a half-band filter to remove the double frequency components introduced by the multiplication process. The signal is then decimated to lower the sampling rate. The root raised cosine filtering is then performed at the lowered sampling rate. Differential decoding

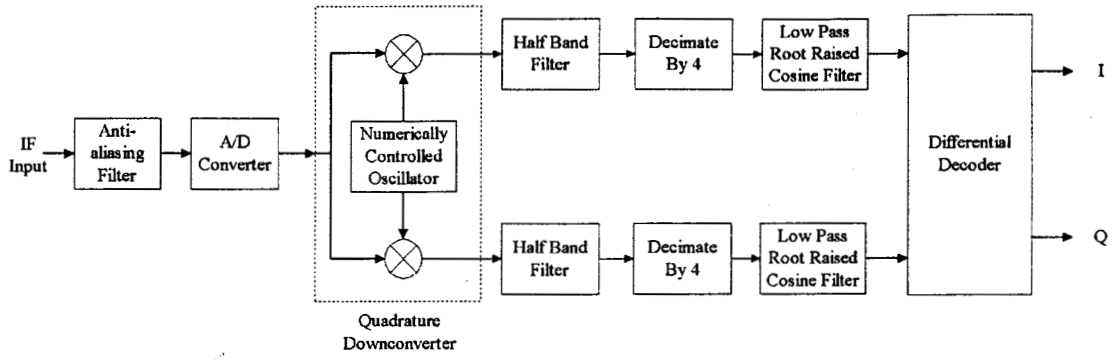


Figure 5.5: Block diagram of the decimated sample rate baseband differential detector

completes the demodulation process.

5.5.2.1 Half-Band Filter

A half-band filter is a specialized FIR filter that is often used in decimation applications [40]. This type of filter eliminates high frequency signals, with a cutoff frequency at $f_s/4$, where f_s is the sampling frequency. This filter also has an advantageous time domain response associated with it, wherein the filter coefficients are symmetrical with every second coefficient having a value of zero. This significantly reduces the complexity of the filter since multiplications and additions do not have to be performed for the zero-valued coefficients. Only half the number of multipliers are required for the regular symmetrical filter architecture, which also reduces the number of adders required.

Figure 5.6 shows the frequency responses for the half-band filters for data word lengths of 8, 12, and 16 bits. The filter realization exhibits good high frequency rejection. The 16 bit filter has a stopband rejection of 90 dB, while the 8 and 12 bit filters have rejections of 35 dB and 60 dB, respectively.

The half-band FIR filter uses the symmetrical filter architecture described in Section 5.3 to reduce complexity. The filter structure is further optimized, since multipliers are implemented only for non-zero (every second) coefficients. This filter requires 23 registers, 6 multipliers, and 11 adders. Two half-band filters are required for each of the I and Q channels.

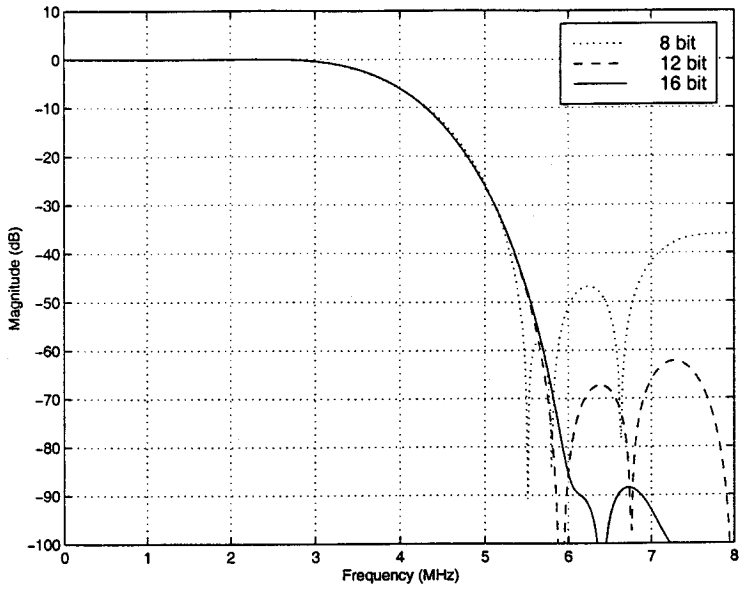


Figure 5.6: Frequency response of the half-band filter

5.5.2.2 Decimation Stage

Decimation is performed in the filter to reduce the sampling rate for subsequent components. These components then have less stringent performance requirements imposed on them, enabling simpler implementations of these components. In this detector, the decimation process reduces the sample rate from 16 samples/symbol to 4 samples/symbol.

The output of the quadrature downconversion is lowpass filtered by the half-band filter to remove the double frequency components centered at 8 MHz. The filtered output can then be decimated by a factor of 2, without suffering any aliasing. The same filtering process is performed again to further reduce the sampling rate to 1/4 of the original rate. This new sample rate is then propagated to the remainder of the baseband processing.

5.5.2.3 Root Raised Cosine Filter

An RRC filter is used to filter the decimated baseband signal. Its design is similar to the filter described in Section 5.5.1.2 for the constant sample rate baseband

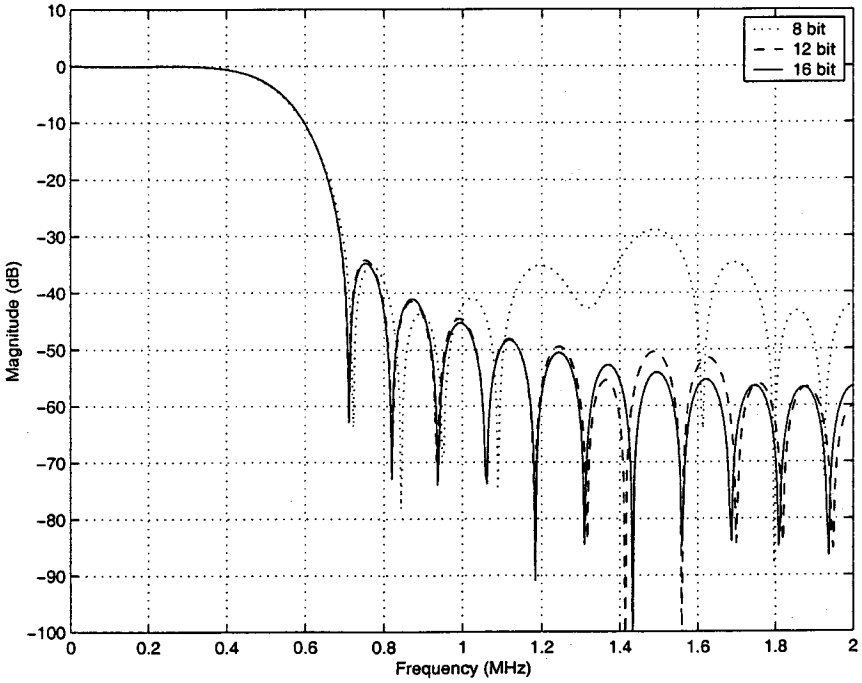


Figure 5.7: Frequency response of the decimated lowpass root raised cosine filter

differential detector. The filter is again implemented for a lowpass cutoff frequency of 500 kHz, with a roll-off factor of 0.35. The impulse response is truncated after eight symbol periods, resulting in a four symbol period delay. However, the decimation reduces the original 129 tap filter to 33 taps, due to the lower sample rate. This greatly reduces the complexity of the designed filter.

The frequency response of this filter is shown in Figure 5.7 for data word lengths of 8, 12, and 16 bits. The filter passband and transition responses are similar to those of the non-decimated filter shown in Figure 5.4. Stopband rejection is 55 dB, 50 dB, and 30 dB for the 16, 12, and 8 bit filters, respectively.

The symmetrical filter structure described in Section 5.3 is used for this filter realization. This filter requires 33 registers, 17 multipliers, and 33 adders which is a substantial reduction in the RRC filter hardware components required for the constant sample rate differential detector.

5.5.2.4 Differential Decoder

After filtering, the differential decoding is performed using the same structure as the CRBB detector described in Section 5.5.1.3. However, this shift register requires fewer registers to produce a one symbol length delay, since only four samples/symbol are used in the baseband processing of this detector, instead of 16 in the CRBB detector. The DRBB differential decoder requires 8 registers, 4 multipliers, 1 adder, and 1 subtractor.

5.6 IF Differential Detector

This section discusses a digital implementation of the IF differential detector that was originally presented in Section 3.4.2. In this detector, the sample rate is maintained constant through the detector.

Figure 5.8 shows a block diagram of the IF baseband differential detector. The input RF signal is quantized by the A/D converter. The digitized input signal is bandpass filtered using a square-root raised cosine filter. The filtered signal is phase shifted by 90° using a Hilbert Transformer to obtain the quadrature portion of the bandpass signal [41]. The inphase component is delayed to synchronize it with the output of the Hilbert Transformer. The transformed signal is then delayed and multiplied to differentially decode the inphase and quadrature components of the signal. After the multiplication, the signals are lowpass filtered to remove the double frequency components caused by the multiplication process.

5.6.1 Root Raised Cosine Bandpass Filter

The IF differential detector filters the input signal using a square-root raised cosine filter, with a roll-off factor of 0.35. This filter is similar to the one in the baseband differential detector that was described in Section 5.5.1.2. However, in this detector the filter is bandpass and is centered at the incoming IF frequency. To transform the lowpass filter into a bandpass filter equivalent, the lowpass filter was

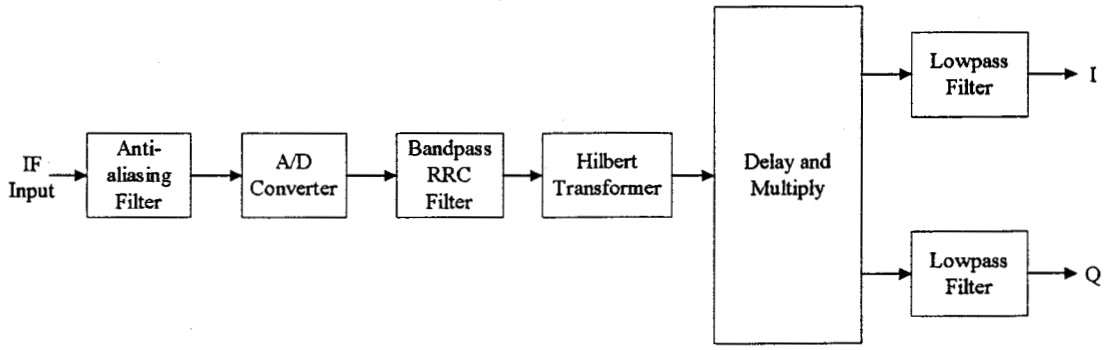


Figure 5.8: Block diagram of the IF differential detector

multiplied by a cosine wave of 4 MHz, which is the desired translation frequency [40]. Since half of the cosine wave values are zero, the resulting filter is simplified to contain only half the number of non-zero coefficients as the equivalent baseband filter.

Figure 5.9 shows the frequency response of the bandpass RRC filters for realizations with data widths of 8, 12, and 16 bits. The stopband rejection of the filter is 60 dB, 50 dB, and 30 dB for the 16, 12, and 8 bit versions of the filter. All the filter realizations exhibit similar responses over the passband and transition bands of the filter.

The symmetrical filter structure described in Section 5.3 is used for this filter. In addition, all odd filter coefficients are zero-valued which further reduces the number of multipliers required. The bandpass RRC filter requires 129 registers, 33 multipliers, and 65 adders.

5.6.2 Hilbert Transformer

After filtering, the inphase and quadrature components must be extracted from the signal. A Hilbert transformer can be used for this purpose. An ideal Hilbert transformer is an allpass filter that shifts the input signal by 90°. The ideal frequency response of this filter can be expressed mathematically as

$$H_{hb}(\omega) = \begin{cases} -j & 0 < \omega \leq \pi \\ +j & -\pi < \omega < 0 \end{cases} \tag{5.1}$$

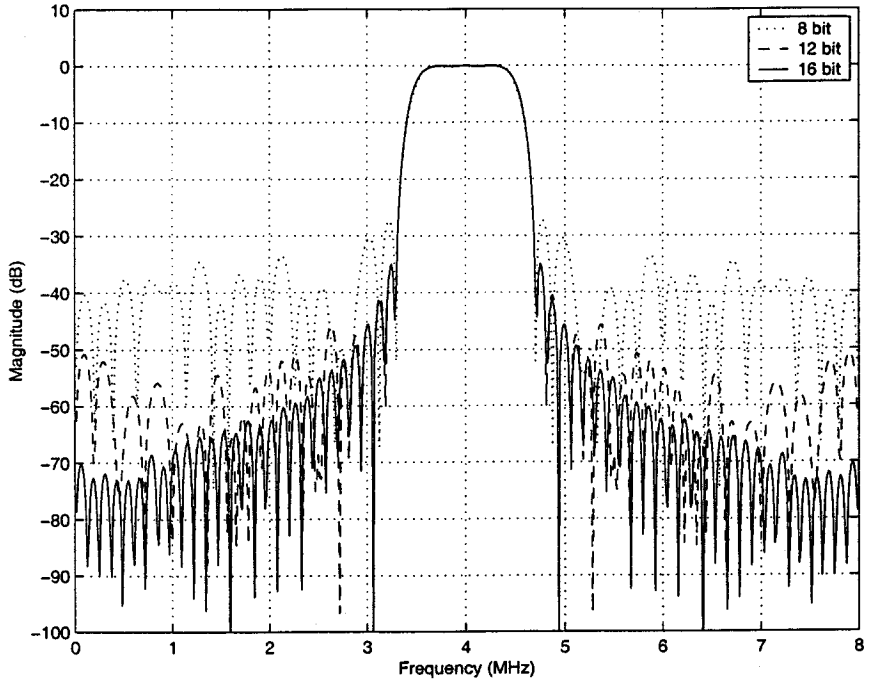


Figure 5.9: Frequency response of the bandpass root raised cosine filter

where ω is the normalized frequency.

The Hilbert transformer is used in this application to extract the quadrature phase of the input signal, so that operations can be performed on the complex signal. Hilbert transformers are often used for this purpose in bandpass digital signal processing algorithms [42].

The designed filter contains 15 antisymmetric taps and was designed using the Parks-McLellan algorithm [41]. Figure 5.10 shows the frequency response of the filter using 8, 12, and 16 bit word lengths. The filter was designed for a passband magnitude ripple of less than 1 dB.

The symmetric filter architecture described in Section 5.3 was used for this filter. Since the filter is antisymmetric, the filter is designed slightly differently than the symmetric filters described in the other sections of this chapter. For an antisymmetric filter, the coefficients are subtracted instead of added prior to the shared multiplier. This allows the filter antisymmetry to be exploited and results in a filter with fewer multipliers than the conventional architecture. This filter uses 15 registers, 8 multipliers, and 14 adders/subtractors.

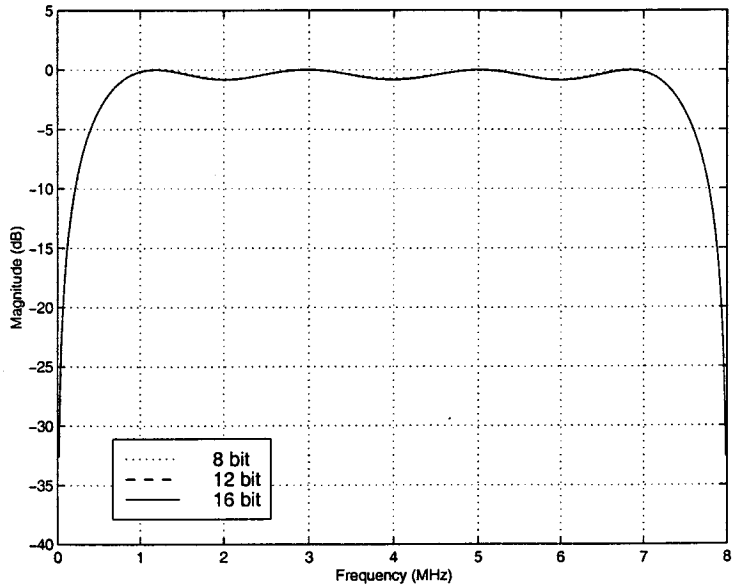


Figure 5.10: Frequency response of the Hilbert transformer

The Hilbert transformer introduces a delay through its filtering process. The original signal, although not phase shifted, must be delayed to ensure synchronization with the Hilbert transformer output. This delay is implemented by directly passing the samples through the same registers found in the Hilbert transformer. It is necessary to ensure the Hilbert transformer delay is an integral number of clock periods, so that the inphase component of the input signal can be properly synchronized.

5.6.3 Differential Decoder

Once the complex signal values have been extracted, the differential decoding is performed according to the technique for the IF differential detector. The decoding consists of multiplying the input signal by a delayed version of the signal and producing the demodulated output signal. In the bandpass case, this multiplication is a complex multiplication involving the inphase and quadrature phase components of the signal as described in Section 3.4.2.

The differential decoder block is composed of a delay block and a multiplication

block. The delay is implemented using registers arranged in a shift register configuration, with the samples advancing through the delay block to produce a one symbol delay. Multiplication is performed using multipliers of the same bitwidth as the input signal. The signals are then added and subtracted using adders of the same bitwidth as the input signal. This decoder block requires 32 registers, 4 multipliers, and 2 adders.

5.6.4 Baseband Lowpass Filter

A lowpass filter is necessary after the multiplication process of the decoder to remove the second order frequency components centered at 8 MHz. These frequency components have significant power levels (i.e. the same as the desired baseband signal). Thus, the lowpass filter must have sufficient stopband rejection to remove the high frequency components.

The filter was designed using the Remez exchange algorithm [41]. The resulting filter is a 16 tap filter, with a stopband rejection of 45 dB in the 16 bit version, 40 dB for the 12 bit filter, and 35 dB for the 8 bit filter. Figure 5.11 shows the frequency response of the designed filters for data word lengths of 8, 12, and 16 bits. The filters are designed to be symmetrical to ensure linear phase characteristics, as well as to allow implementation using the symmetric filter architecture. This filter requires 16 registers, 8 multipliers, and 15 adders.

5.7 Frequency Discriminator Detector

This section discusses a digital implementation of the frequency discriminator detector that was originally presented in Section 3.4.3. In this detector, the sample rate remains constant throughout the detector.

Figure 5.12 shows a block diagram of the digital frequency discriminator detector. The quadrature baseband downconversion is performed in exactly the same manner as in the baseband differential detector discussed in Section 5.5.1.1. The inphase and quadrature components are frequency demodulated using the cross-

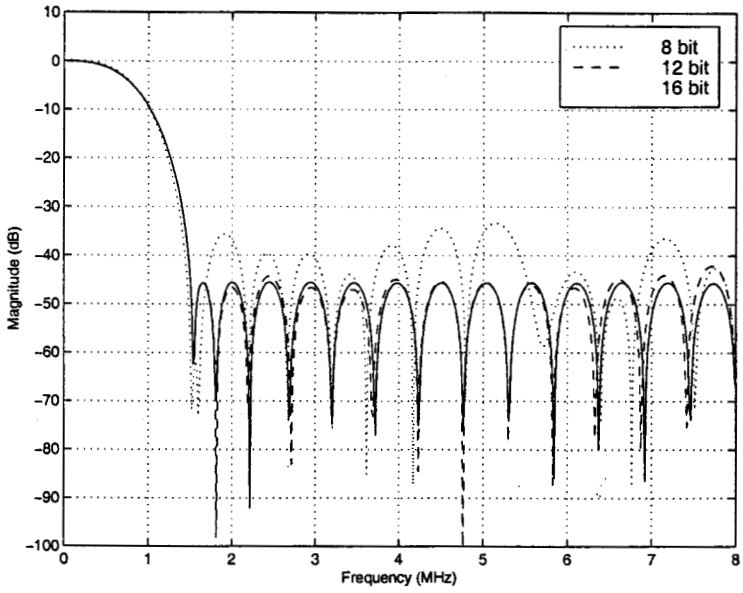


Figure 5.11: Frequency response of the lowpass filter

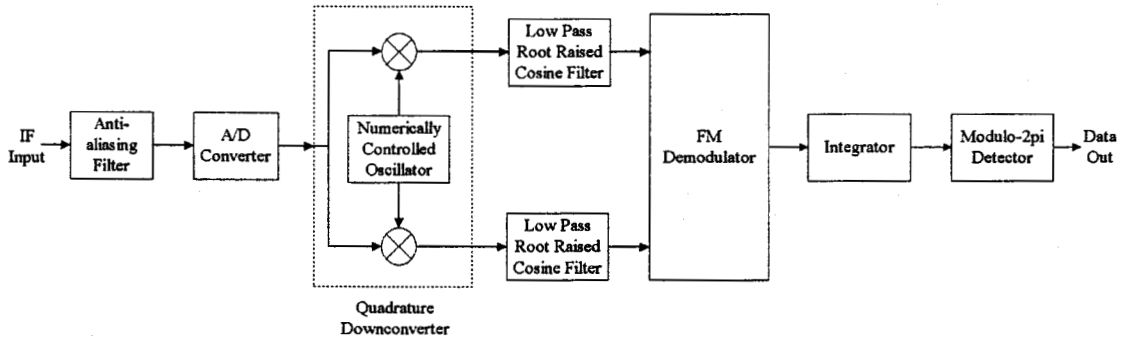


Figure 5.12: Block diagram of the frequency discriminator detector

differentiate and multiply method [43]. This method is mathematically equivalent to the differentiation of the arc-tangent function used in the limiter-discriminator-integrator detector that was described mathematically in Section 3.4.3. After the cross-differentiate and multiply block, the signal is normalized for the varying signal envelope. The signal is then integrated over the symbol period to obtain the four-level output that corresponds to the four possible $\pi/4$-DQPSK phase trajectories. These levels are then decoded by a modulo-2π detector to determine the appropriate output symbol.

5.7.1 Quadrature Downconversion and Filtering

The quadrature downconversion and RRC filtering are performed in the same manner as the baseband differential detector as presented in Sections 5.5.1.1 and 5.5.1.2. The hardware design is identical for this detector.

5.7.2 FM Demodulator

The digital FM demodulation is performed using the cross-differentiate and multiply method [43]. This demodulation can also be performed using an arc-tangent lookup table [44], a tracking phase lock loop method, or by using zero-crossing detectors [45, 46]. However, the cross-differentiate and multiply method was chosen, since it is similar to the method presented earlier in Section 3.4.3, without requiring the use of a large memory block for an arc-tangent lookup table.

The phase, $\theta(t)$, of the baseband signal is

$$\theta(t) = \tan^{-1}(\frac{Q(t)}{I(t)}) \tag{5.2}$$

where $Q(t)$ is the quadrature signal and $I(t)$ is the inphase component. The cross-differentiate and multiply block differentiates the phase to produce an output signal, $x(t)$, which is described as

$$x(t) = \frac{d\theta(t)}{dt}. \tag{5.3}$$

This signal is the same as that originally described in Equation 3.39. Substitution of Equation 5.2 into Equation 5.3 for $\theta(t)$ and performing the differentiation with respect to time produces the following output for the cross-differentiate and multiply block, $x(t)$, as

$$x(t) = \frac{Q'(t)I(t) - I'(t)Q(t)}{I^2(t) + Q^2(t)} \tag{5.4}$$

where $'$ indicates differentiation of the indicated signal component.

Figure 5.13 is a block diagram of the hardware implementation of this block. Multipliers perform the cross-multiplication of the differentiated signals. The differ-

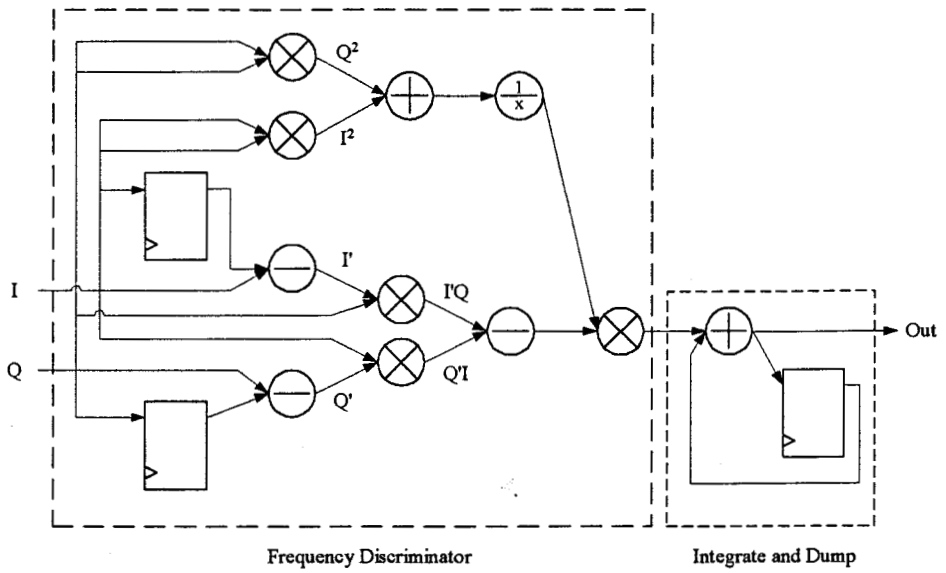


Figure 5.13: Block diagram of the digital FM demodulator

entiation is performed by a first-order differentiator. The outputs are summed and normalized by dividing by the sum of the squared inphase and quadrature components. The reciprocal ($\frac{1}{x}$) function requires a larger number of bits than the other components, since the reciprocal of a small number is a very large number. This large bit width is propagated to the output multiplier.

The digital hardware solution for this block requires 3 registers, 5 multipliers, 1 divider (reciprocal), and 3 adders/subtractors.

5.7.3 Integrator

The integrator section sums the FM demodulator output over one symbol period using a first-order approach. The output of the integrator uses a greater bitwidth to ensure the accumulator does not overflow when presented with typical sample values.

Control logic is necessary to ensure the integrator value is reset to zero at the start of a new symbol period. This control logic uses the symbol timing circuitry indication of the beginning of a new symbol period to reset the accumulated value to zero.

Digital hardware implementation of the integrator requires 1 register and 1 adder. In addition, a number of gates are required for the control logic of the integrator.

5.7.4 Modulo-2π Detector

The modulo-2π detector detects the four levels of the frequency discriminator detector and maps the output to the corresponding $\pi/4$-DQPSK symbol as described in Section 3.4.3. It is necessary to perform modulo-2π detection for the cases in which the phase trajectory goes the opposite way around the unit circle as described in Section 3.4.3.

The modulo function is implemented by allowing the detector numeric output to wrap around to the negative values. It is possible to do this since the integrator output divides the numerical output range into four sections. Each of these sections corresponds to one of the four level outputs that map to a $\pi/4$-DQPSK symbol. Thus, this function can be very simply implemented by wrapping, not saturating, the integrator output.

5.8 BER Performance

This section compares the BER performance of the detector implementations described earlier in this chapter.

Figure 5.14 illustrates the performance of the IF differential detector using data widths of 8, 12, and 16 bits. The 12 bit and 16 bit detectors have very similar performance characteristics, with the 16 bit detector holding a very slight advantage. The 8 bit detector has much poorer performance than the other two detectors. At a BER of 10^{-4}, the detectors have an implementation loss of 0.2 dB, 0.2 dB, and 1.3 dB for the 16, 12, and 8 bit detectors, respectively.

Figure 5.15 illustrates the performance of the constant rate baseband differential detector. The 16 bit realization has slightly superior performance to the 12 bit detector, while the 8 bit detector suffers from a much greater implementation loss.

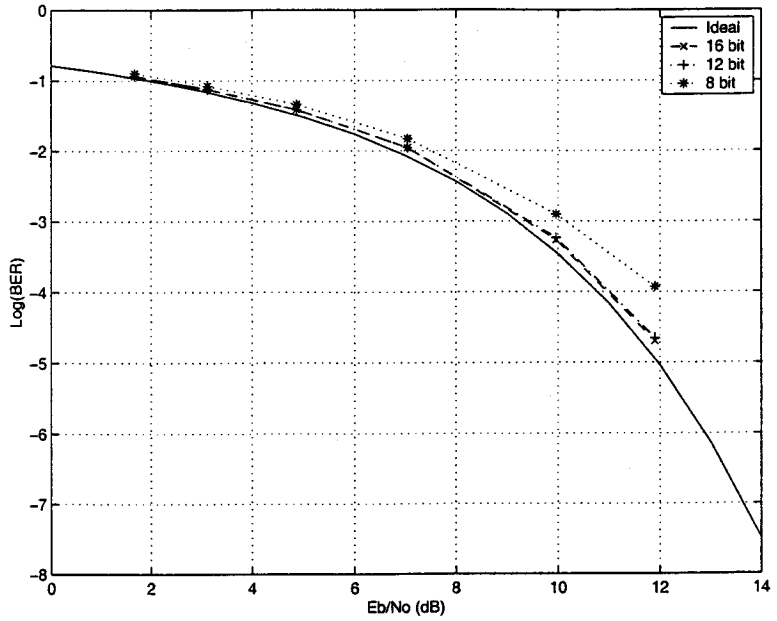


Figure 5.14: BER performance of the synthesized IF differential detector

At a BER of 10^{-4}, the detectors have an implementation loss of 0.05 dB, 0.1 dB, and 1.0 dB for the 16, 12, and 8 bit realizations, respectively.

Figure 5.16 displays the performance of the decimated rate baseband differential detector. The 16 and 12 bit detectors have virtually identical performance that closely tracks the ideal performance, while the 8 bit detector has slightly poorer performance. At a BER of 10^{-4}, the detectors have an implementation loss of 0.05 dB, 0.05 dB, and 0.4 dB for the 16, 12, and 8 bit realizations, respectively.

The performance of the frequency discriminator detector is shown in Figure 5.17. The performance of the 16 bit realization is very poor and does not approach the ideal performance characteristic. For this reason, the 8 and 12 bit realizations were not simulated, since it is expected that their performance would be even worse. The performance of the digital frequency discriminator can be improved by increasing the sample rate of the detector. The differentiation and integration processes need more samples to accurately detect the instantaneous frequency deviations that are used to determine the detector output.

Both forms of the baseband differential detector outperform the IF differential detector. The baseband differential detector has an inherent advantage over the IF

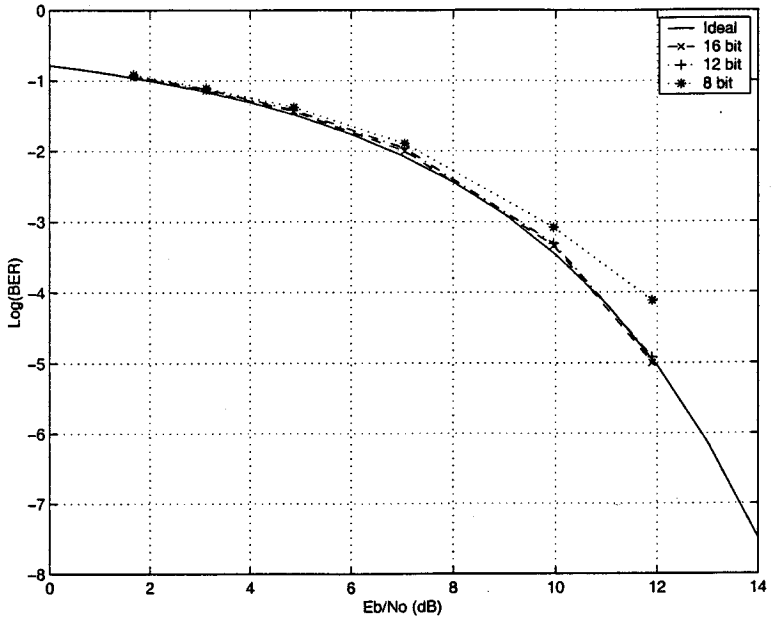


Figure 5.15: BER performance of the synthesized constant rate baseband differential detector

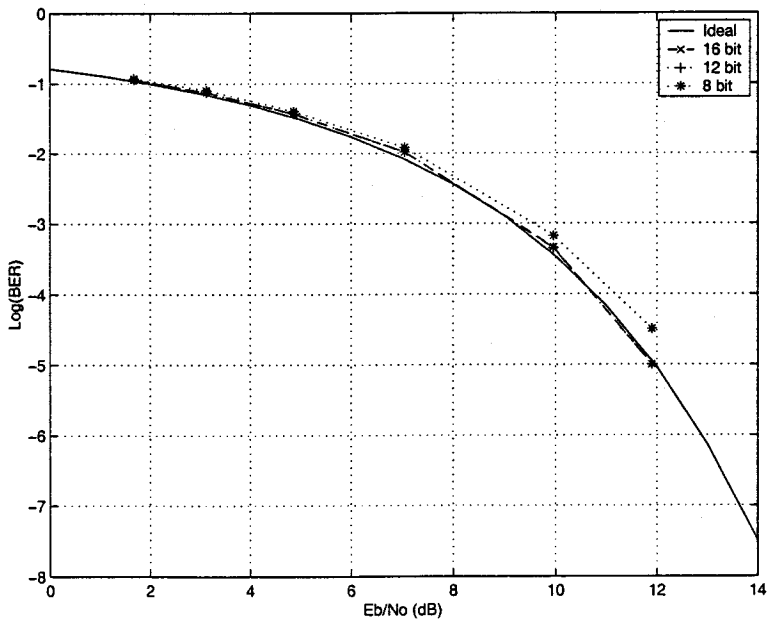


Figure 5.16: BER performance of the synthesized decimated rate baseband differential detector

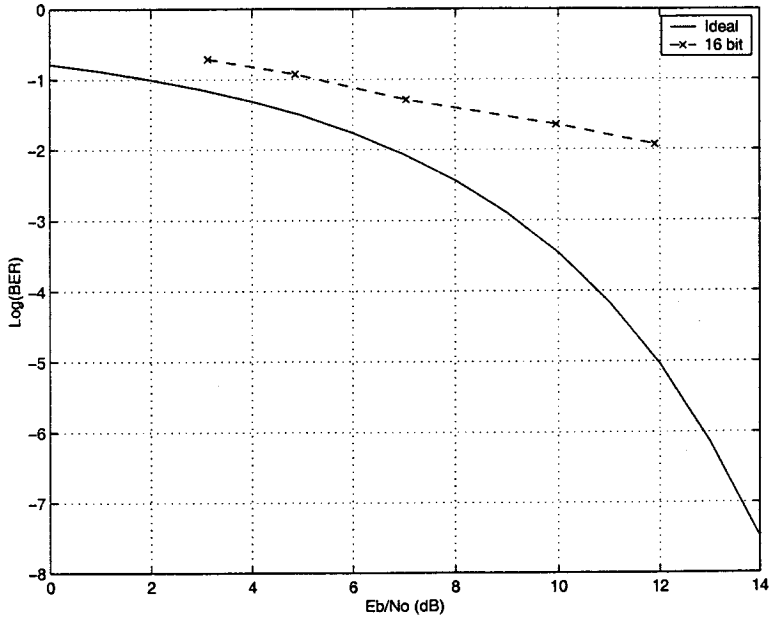


Figure 5.17: BER performance of the synthesized frequency discriminator detector

differential detector since its filtering can be performed at baseband. The IF differential detector realization is also complicated by the need to perform the differential decoding process at a bandpass frequency. This requires complex multiplication which makes the use of a Hilbert transformer necessary. The Hilbert transformer introduces additional performance loss into the IF differential detector, even when carefully designed. Finally, the IF differential detector is at a disadvantage since it requires additional baseband lowpass filtering to remove the second-order frequencies caused by the differential detector. Even when carefully designed, this filter introduces additional signal degradation.

The decimated rate baseband differential detector (DRBB) has better performance than the constant rate baseband differential detector (CRBB). The performance advantage is very slight in the 16 and 12 bit realizations, but is more pronounced in the 8 bit realization. The DRBB detectors have better performance, since they have fewer filter taps than the CRBB realizations. This is an advantage since the reduced length of the filter is subject to less rounding through the adders and multipliers and results in a more accurate output.

In the DRBB, the symbol timing was carefully controlled to ensure the detector

sampled the received waveform at the optimal point. However, in a practical modem the DRBB is at a disadvantage compared to the CRBB. The DRBB has only four samples/symbol to use to determine the optimal sampling point, while the CRBB has sixteen. The additional time resolution of the CRBB allows it to more accurately fine-tune the symbol timing point. To counteract this disadvantage, a practical DRBB must resample the detected waveform at a higher rate to more accurately detect the optimal sampling point. The resampling procedure requires additional circuitry that increases the complexity of the DRBB modem.

The BER performance of the modem realizations when faced with a number of concurrent impairments is displayed in Figure 5.18. The performance is displayed for common numeric precisions of the detector types. The modem realizations are subjected to a DC offset of 2.5%, modulator phase imbalance of 2°, timing offset of 2.5%, and the medium downconverter phase noise characteristic. This scenario is similar to Scenario B of Section 4.8. However, the limiter impairment of Scenario B was not included in this scenario, since the digital detector realizations described in this chapter do not include a limiter. In addition, frequency offset was not included in this scenario, since it was expected that this impairment would overshadow the other impairments as shown in Section 4.8.

As expected, the modem realizations suffer from additional loss when subjected to the concurrent impairments. All the detector types suffer from a similar amount of degradation when realized using 12 and 16 bit detectors. These detectors each suffer from an additional loss of 0.8 dB at a BER of 10^{-4}. This is a similar amount of degradation as observed for the ideal detectors in Scenario B of Section 4.8, despite the dominant impairment (limiter AM to PM) of that scenario not being included in this scenario. This degradation indicates that the digital realizations are more sensitive to impairments than the ideal detectors presented in Chapter 4.

Interestingly, the 8 bit CRBB and IF detectors perform better than the DRBB detector when faced with the concurrent impairments. The IF and CRBB detectors suffer from an additional loss of 0.6 dB at this BER, while the DRBB detector suffers an extra 0.8 dB loss. The CRBB and IF detectors have poorer BER performance

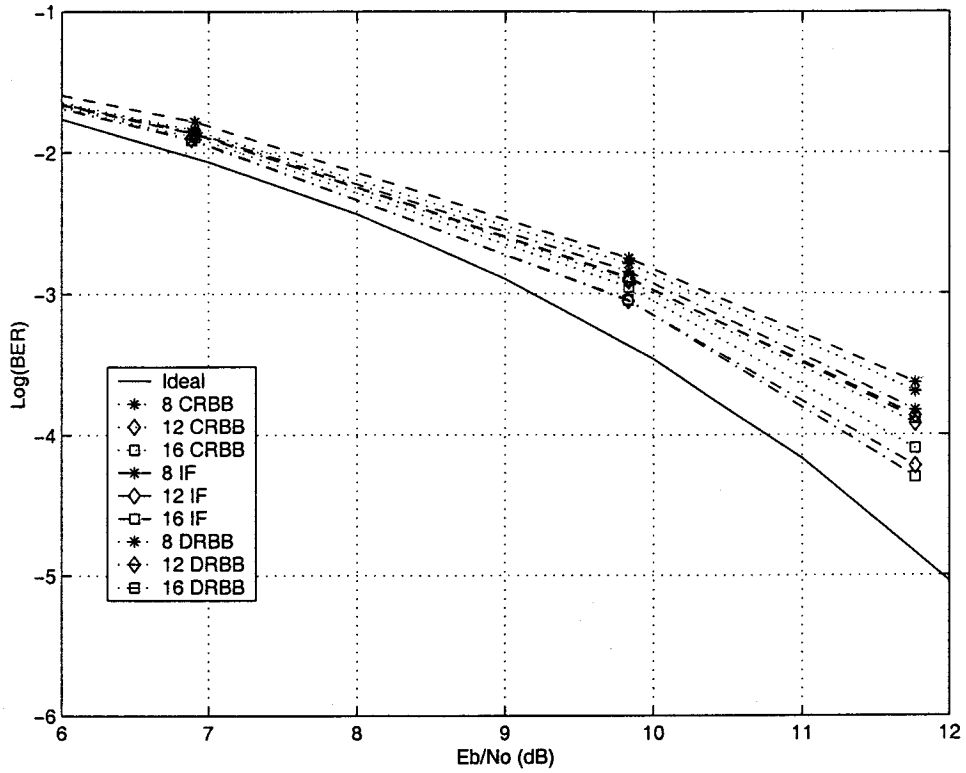


Figure 5.18: BER performance of the synthesized modems with multiple impairments

than the DRBB without impairments. It is suspected that part of the impairment degradation is masked by this initial implementation loss, so the impairments cause a smaller additional degradation in the CRBB and IF detectors, but this requires further investigation.

5.9 Digital Hardware Realization

The digital detector designs discussed in this chapter can be realized in any type of digital logic device, including application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and complex programmable logic devices (CPLDs). In this chapter, the realizations are compared on the basis of their implementation complexity in Altera Flex 10K CPLDs [47].

This technology was chosen even though the Flex 10K CPLDs offer gate densities and chip speeds that are lower than ASICs. However, unlike ASICs, CPLDs are

programmable. This minimizes development time since new designs can be quickly prototyped, tested, and re-designed within the same facility, unlike ASICs that must be fabricated at special-purpose facilities.

CPLDs are very similar to FPGAs, but do have some advantages [47]. The primary advantage is that CPLDs have continuous interconnect structures between logic cells, while FPGAs have a segmented interconnect structure. The continuous interconnect structure provides better logic cell connectivity that leads to slightly faster chip speeds and smaller implementation sizes. In addition, delays between logic cells are reduced which provide predictable timing performance for signals between logic cells.

5.10 Detector Size Estimate

The demodulators discussed in this chapter were not actually implemented in the Altera chips. This chapter discusses size and speed estimates for the designs that are based on the Altera Flex10K technology. Altera area estimates are based on the Altera unit of measure, which is called a logic cell (LC) [47].

Table 5.1 shows the area estimate for an adder and a multiplier with two's-complement numeric precisions of 8, 12 and 16 bits. The adder and multiplier implement rounding and saturation, so that the output bit precision is the same as the input precision. The size of the 16 bit adder is approximately twice as large as the 8 bit adder, with the 12 bit adder falling in between. This indicates that the size estimate of an adder increases linearly in area as the number of input bits increases. However, a multiplier increases in size quadratically as the number of input bits increases. The increase is caused by the additional partial products that have to be maintained within the multiplier. Doubling the input bit size from 8 to 16 bits quadruples the area of the multiplier. It can also be seen that multipliers are significantly larger than adders of the same numeric precision. All synthesized multipliers and adders are able to perform their processing at speeds greater than 16 MHz, which is the fastest clock rate encountered in the detectors for this application.

Table 5.1: Area estimates of multipliers and adders

Numeric Precision (bits)	*Multiplier Size (LC)*	*Adder Size (LC)*
8	84	9
12	163	13
16	312	17

The size estimates for the detector types are based on the synthesis of the individual multipliers and adders shown in Table 5.1. The size estimate for the entire detector is determined by summing the number of multipliers and adders used in the detector components. These sums are multiplied by the size of the individual multipliers and adders to obtain the total size estimate.

Space required for registers is neglected, since each logic cell in the Altera technology has a built-in register. Space for interconnection between adders and multipliers is also neglected, because investigation showed that interconnect added less than 5% to the area estimate. Actual realization sizes will be somewhat different from the estimate derived in this section, due to space required for interconnection and control logic. The multipliers have the dominant effect on the size of the realization. This simple method allows the relative sizes of the detectors to be compared in terms of implementation complexity.

Table 5.2 shows the total number of multipliers and adders in each component of the detector types. The numbers of multipliers and adders are separated for each component and each detector type. Table 5.3 shows the total area estimates for the Altera realization of the detectors described in this chapter. This estimate is derived from the number of the multipliers and adders in each modem multiplied by the number of logic cells found in Table 5.1.

The decimated rate baseband differential detector (DRBB) has a smaller footprint than the CRBB realization. The size savings come from the lower sampling rate of the decimated portion of the modem. This allows the inphase and quadrature RRC filters to have fewer taps while still maintaining a similar filter approximation as the constant rate baseband differential detector (CRBB). The decimation does

Table 5.2: Number of multipliers and adders in detector designs

Component	*Multipliers*	*Adders*
Constant Rate Baseband Differential Detector (CRBB)		
Quadrature Downconverter	0	1
RRC Filter (I)	65	129
RRC Filter (Q)	65	129
Differential Decoder	4	2
Total	134	261
Decimated Rate Baseband Differential Detector (DRBB)		
Quadrature Downconverter	0	1
Half-Band Filters (4)	24	44
RRC Filter (I)	17	33
RRC Filter (Q)	17	33
Differential Decoder	4	2
Total	62	113
IF Differential Detector (IF)		
RRC Filter	33	65
Hilbert Transformer	8	14
Differential Decoder	4	2
Lowpass Filters (2)	16	30
Total	61	111
Frequency Discriminator Detector (FM)		
Quadrature Downconverter	0	1
RRC Filter (I)	65	129
RRC Filter (Q)	65	129
FM Demodulator	6	3
Integrator	0	1
Total	136	262

require half-band filters that take up additional area. However, the net effect of the decimation is positive in terms of complexity, since the DRBB realizations are much smaller than the corresponding CRBB realizations.

The IF differential detector has a comparable, but slightly smaller area than the decimated rate baseband differential detector. It achieves this small area despite a much higher sampling rate throughout the detector than the decimated portion of the DRBB. The IF differential detector achieves area savings since it only requires one bandpass RRC filter, instead of the two RRC filters required in the other detectors. This saving is offset by the additional Hilbert transformer and lowpass filters used in the detection process. However, the sizes of the additional components are still significantly less than the size of the RRC filter realization, so the IF differential detector has a relatively low chip area estimate.

The constant rate baseband differential detector has a large size estimate, which is dominated by the size of the two RRC filters used in the realization. To reduce the area required, the decimation technique that is used in the DRBB is very effective. For this reason, decimation is a very attractive option to reduce the size requirements of the detector and is feasible for this detector type.

The frequency discriminator detector has a larger size estimate than the other detectors. It shares a similar realization to the baseband differential detectors, but requires additional components to perform the frequency demodulation and integration. This detector could also use decimation, so that the RRC filter sizes would be smaller and lead to an overall size reduction. However, this detector relies on detecting phase differences between samples in the differentiation process. Earlier discoveries showed that the BER performance decreases significantly when few samples/symbol are used in the detection process. Therefore, decimation is not recommended in this detector, even though it would produce a smaller realization.

All the designed modems are very large in size. Only the 8 bit and 12 bit versions of the decimated rate baseband differential detector and the IF differential detector will fit in currently available Altera devices that have a maximum of 12160 logic cells [47]. Other research has shown that by optimizing the modem multipliers and

Table 5.3: Total area estimates of the detector types

Numeric Precision (bits)	*CRBB*	*DRBB*	*IF*	*FM*
8	13605	6225	6123	13782
12	25235	11575	11386	25574
16	46245	21265	20919	46886

adders, the size of the baseband differential modem can be reduced [48].

5.11 Analog Filter Compensation Realization

An especially hardware intensive portion of the digital demodulators described in this chapter is the square root raised cosine receive filter (or filters). Simplification to this filter results in a significant reduction in the demodulator hardware complexity.

The optimal RRC receive filter can be approximated by a fourth order Butterworth filter, as presented in Section 4.7.1.1. The Butterworth filter is very simple to realize using analog components and is much less complex than the comparable RRC filter. However, the BER performance of the resultant detector is poorer, due to group delay distortion caused by the nonlinear phase response of the filter. Phase compensation can be used to reduce the group delay distortion in the receive Butterworth filter. This compensation was shown by Waskowic and Klymyshyn [49] to improve the BER performance of a modem containing the analog filter.

A Butterworth filter that matches the RRC lowpass signal bandwidth of 500 kHz can be used when phase compensation is added to the modem. This narrower bandwidth is possible since the group delay distortion that is normally present at the passband edge is reduced by the phase compensation. This also results in better noise rejection than the uncompensated wider bandwidth Butterworth filter that was originally described in Section 4.7.1.1.

The algorithm used to calculate the phase compensation is described in a paper by Lang and Laakso [50]. Their paper proposes a method to design allpass filters used for phase equalization. The algorithm determines the coefficients of an infinite

impulse response (IIR) phase equalization filter that approximates the desired phase response. This filter can then be used to correct another filter with a nonlinear phase response to produce a combined response with an almost linear phase characteristic.

Lang and Laakso's algorithm is based on a weighted iterative least-squares error estimation technique. The desired phase response is prescribed at a discrete set of frequency points as an input to the algorithm. A weighting function can also be specified to give higher priority to the desired phase response at certain frequencies, although this feature was not used in this implementation.

With all the inputs specified, an initial filter solution is calculated. The algorithm then iteratively adjusts the filter coefficients until the produced phase response is within the phase error tolerance specified. Optimization is based on minimizing the weighted phase error. For this particular filter, five iterations were used to generate a sixth order (N=6) IIR filter.

The calculated IIR allpass filter is truncated after six symbols to produce an FIR filter for implementation in the transmitter. The phase compensation could be improved by incorporating a longer filter response. The filter implementation can be simplified by using a shorter impulse response, at the expense of poorer filter performance. The phase compensator frequency response is shown in Figure 5.19. The allpass filter has a magnitude ripple of less than 0.1 dB over the signal passband. This small ripple has little effect on the filtered output spectrum. The filter impulse response is shown in Figure 5.20. The impulse response has very small sample values after 6 μs (symbols), which allows truncation of the impulse response after this point.

Figure 5.21 shows the Butterworth filter group delay characteristic and the corresponding compensated response. The group delay distortion in the uncompensated filter has been corrected to produce a flat response ($<$ 1 ns ripple) over the passband of the compensated response.

Often, the transmitter is implemented using memory lookup tables to produce the transmit symbols, rather than producing the output by multiply-and-accumulate computations. This type of transmitter can be modified to implement the phase

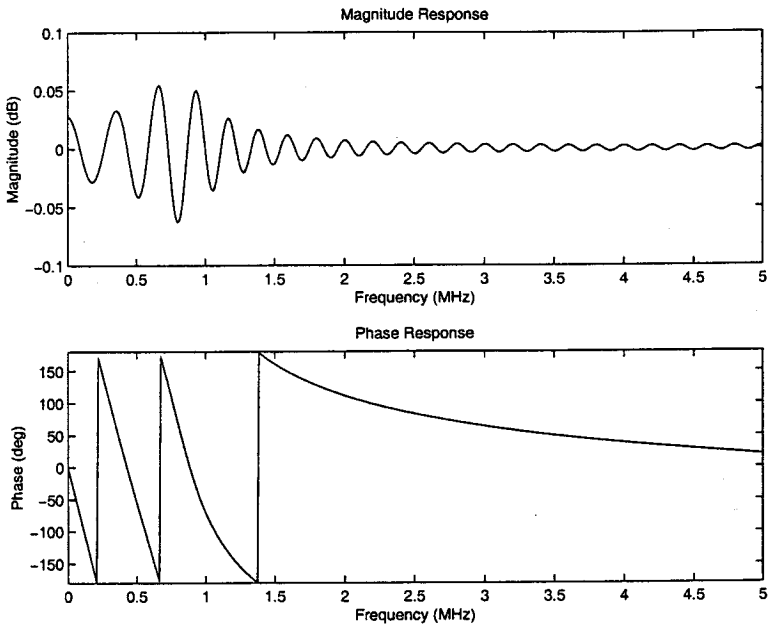


Figure 5.19: Frequency response of the allpass phase compensation filter

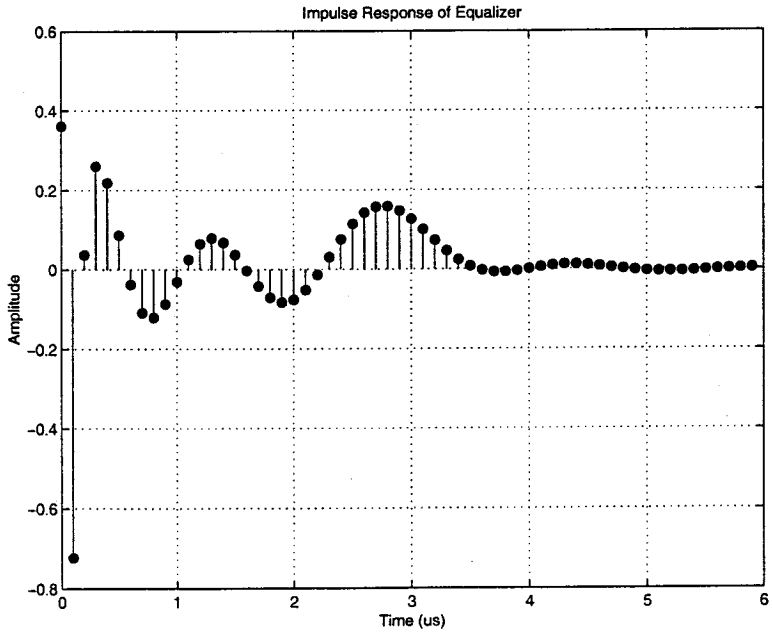


Figure 5.20: Impulse response of the allpass phase compensation filter

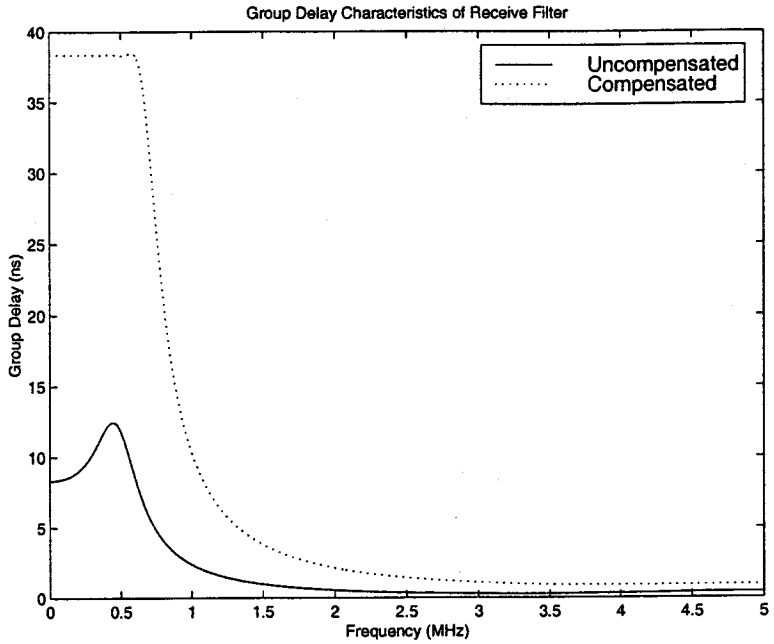


Figure 5.21: Group delay response of the compensated and uncompensated filter

compensation described in this section. The lookup table read only memory (ROM) is expanded to include the compensator filter response.

The impulse responses of the original transmitter RRC filter and the compensator filter are convolved to provide a new response that incorporates the phase compensation. This convolution causes time domain spreading that expands the lookup table size required to store the additional information. The number of symbols in the lookup table ROM grows by a factor of 2.5 due to the increased length of the combined impulse response. This increases the memory requirements of the ROM used for the lookup table. However, this memory is usually less expensive than the hardware required to implement the optimal RRC filter in the receiver.

Figure 5.22 shows the BER performance diagram for the ideal modem and the sub-optimal modem, with and without compensation. A significant improvement in BER performance is obtained with the compensated modem when compared to the uncompensated one. For example, it can be seen that for a BER of 10^{-5}, the required $E_b/N_o = 12.3$ dB for the compensated system, while the uncompensated system required an additional 0.7 dB to obtain the same BER performance. In addition, the implementation loss for the compensated receiver is only 0.3 dB at

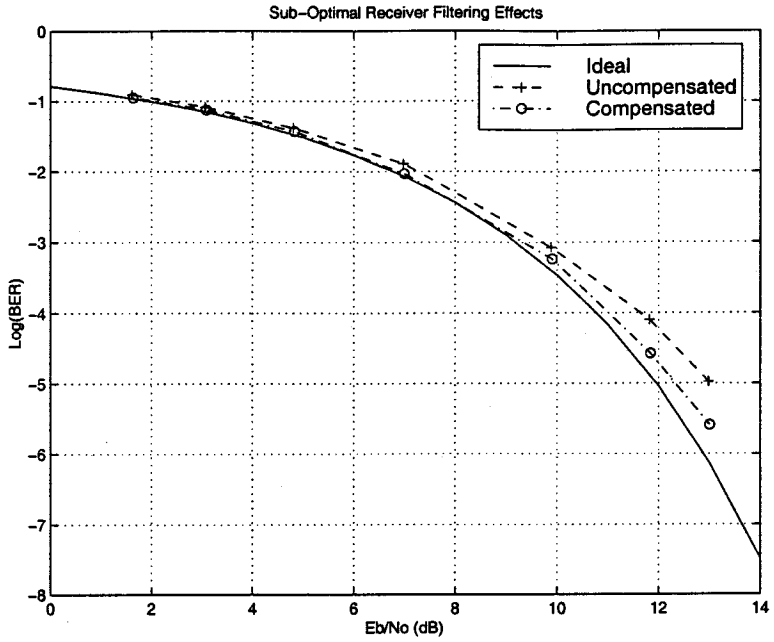


Figure 5.22: BER performance of the ideal, compensated, and uncompensated modems

this BER when compared to the ideal.

An IF differential detector using this compensation technique replaces the digital RRC filter with an analog Butterworth filter. The received signal is converted to digital by the A/D converter after the filter. The replacement of the RRC filter reduces the digital hardware requirements significantly. In the case of the 12 bit detector, the number of logic cells used to realize the modem is reduced over 50%, from 11386 LC to 5162 LC. Similar savings can be realized for the baseband differential and frequency discriminator detectors.

5.12 Summary

This chapter detailed digital realizations of the three detector types. Designs were presented for the IF differential detector, frequency discriminator detector, and the baseband differential detector (both with and without decimation). The designs use digital signal processing to accomplish the detection process, making it suitable for implementation in digital hardware such as CPLDs, FPGAs, and ASICs.

The BER performance of the detectors was characterized. The decimated rate baseband differential detector (DRBB) had the best performance and was closely followed by the constant rate baseband differential detector (CRBB). The IF differential detector performance was poorer than the baseband differential detectors, but was still reasonable. The frequency discriminator detector performance was atrocious when implemented with digital hardware.

The detector types were realized for three numeric precisions – 8, 12, and 16 bits. For the baseband differential detectors and the IF differential detectors, the BER performance of the 12 bit detectors was very similar to the performance of the 16 bit detectors. This indicates that there is no significant performance advantage to using 16 bit detectors over 12 bit detectors. The performance of the 8 bit detectors was much worse than the 12 and 16 bit realizations. However, depending on the application this performance may be acceptable. All detector realizations showed greater sensitivity to impairments than the ideal detectors presented in the previous chapter.

A digital hardware size estimate was derived for the designs, using the Altera Flex10K family of logic devices. The IF differential detector had the smallest size estimate, and was followed closely by the decimated rate baseband differential detector. The frequency discriminator detector and the constant rate baseband differential detector each had much larger size estimates than the other two detectors.

A majority of the detector size comes from the RRC filters used in the detector realizations. Removing the RRC filters and replacing them with analog Butterworth filters greatly simplifies the modem realizations. However, this introduces additional BER performance degradation. A phase compensation technique was presented that improves the performance of the modem with sub-optimal analog filtering. The performance of this compensated modem is comparable to the RRC filtering and is significantly superior to the uncompensated modem. This performance increase can be realized through compensation in the transmitter, without greatly increasing the complexity of the transmitter. The replacement of the digital RRC filter reduces the CPLD area estimate by at least 50%, making this technique very attractive.

Chapter 6

SUMMARY AND CONCLUSIONS

6.1 Summary of Objectives

There were four main objectives in this thesis work. The first objective was to research the detection methods for the $\pi/4$-DQPSK modulation scheme and to review the previous literature associated with these detectors. This information was presented in Chapters 1 through 3.

The second objective was to compare the performance of the IF differential detector, baseband differential detector, and frequency discriminator detector through simulation. A number of typical system impairments were selected for investigation. The BER performance was characterized for the baseband differential detector and IF differential detector. For the most part, Chapter 4 showed the impairments have identical effects on these two detectors.

Unfortunately, it was not possible to characterize the BER performance of the frequency discriminator detector, which was originally expected to have some performance differences compared to the other detectors. The frequency discriminator detector was unable to be characterized due to difficulties in simulation of the detector. The differentiation and integration process require a large number of samples to accurately model the processes. This leads to a very large number of simulation steps that cause excessively long simulation times.

The third objective was to propose compensation techniques (where applicable) for impairments found in the modem. Research was performed to determine appro-

priate compensation techniques to increase the modem performance while under the effect of the impairment. The research was presented along with the impairment discussions in Chapter 4.

The fourth and final objective was to design the three modem types using digital signal processing. The goal was to synthesize designs that were suitable for implementation in a digital hardware device. The detectors were compared based on their BER performance as well as their implementation complexity in Chapter 5.

6.2 Result Summary and Conclusions

Chapter 4 discussed the causes and effects of common impairments that are confronted in a modem design. The effect of the impairment on the BER performance was also characterized in the chapter. Table 6.1 provides an overview of the degradation at a BER of 10^{-4} for each impairment that was studied.

The most severe impairment, shown in Table 6.1, is the frequency offset impairment. A typical modem will encounter a frequency offset of approximately 10%. At this level of impairment, the modem has extremely poor performance and makes compensation of this impairment mandatory. The original intention of using non-coherent detection in this application was to simplify the detector, since it was assumed that carrier recovery wouldn't be required. However, this impairment indicates that even when using non-coherent detection, carrier frequency synchronization is still required.

The filter realization is also very important in the detector design. Digital filter realizations that use shortened impulse responses are attractive, since they have lower implementation complexity. However, this reduction in complexity is offset by the loss in BER performance. RRC filters greater than eight symbol periods in length do not benefit from a very large performance gain, so there is little motivation to use an RRC filter longer than this. The performance of six symbol period length filter is still adequate, but for filters with shorter lengths the performance is much worse. To reduce the filter complexity, an analog Butterworth filter can be used that

Table 6.1: Degradation of impairments at BER = 10^{-4}

Impairment	*Degradation (dB)*
Frequency offset (1%)	0.2
Frequency offset (2.5%)	1.2
Frequency offset (5%)	3.0
DC offset (1%)	0.05
DC offset (2.5%)	0.2
DC offset (5%)	1.0
Phase imbalance (1%)	0.02
Phase imbalance (2%)	0.05
Phase imbalance (5%)	0.2
Timing offset (1%)	0.01
Timing offset (2.5%)	0.1
Timing offset (5%)	0.3
Timing offset (10%)	1.5
RRC filter of length $8T_s$	0.05
RRC filter of length $6T_s$	0.1
RRC filter of length $4T_s$	1.0
Butterworth filter	0.7
Limiter AM to PM (1°/dB)	0.1
Limiter AM to PM (2°/dB)	0.4
Limiter AM to PM (5°/dB)	2.0
Phase noise (low)	0.05
Phase noise (medium)	0.1
Phase noise (high)	1.5

approximates the RRC response. Despite being very attractive from a complexity standpoint, the Butterworth filter has relatively poor BER performance compared to a digital RRC filter.

The detectors rely on symbol timing recovery to properly decode the received signals. It is necessary for the clock recovery circuit to accurately determine the symbol timing period, since timing offsets greater than 5% have large performance losses. This is a major consideration when using lower sampling rates. For example, when using 16 samples/symbol, the average symbol timing offset for an accurate circuit is 3.3%. When using a low sampling rate of 4 samples/symbol, time resolution is very poor, so the average offset is 12.5%. If a low sampling rate is used, the received waveform must be resampled at a higher rate, so that the timing recovery can be performed more accurately.

DC offset causes a small, but still significant BER performance degradation. Fortunately, this impairment is relatively easy to fine-tune in the transmitter, so that its effect can be minimized in the detectors. The limiter AM to PM conversion impairment is also worthy of consideration. When using low-cost limiters, the AM to PM conversion leads to significant degradation. Unfortunately, this impairment is complicated to compensate, so the designer must decide whether it is worth the extra complexity to compensate.

Degradation due to the phase noise and phase imbalance impairments is negligible compared to the other impairments studied in this chapter. It is fortunate that the oscillator phase noise degradation is low, since this impairment is difficult to compensate. The phase imbalance impairment is easier to compensate. However, the compensation is unnecessary, since the degradation observed in the detector is very slight.

The $\pi/4$-DQPSK detector types were designed in Chapter 5. Designs were presented for the IF differential detector, the frequency discriminator detector, and the baseband differential detector. Two variations of the baseband differential detector were designed. The constant rate baseband differential detector (CRBB) maintains a constant sample rate throughout the detector, while the decimated rate baseband

differential detector (DRBB) reduces the sample rate in the latter stages of the detection process.

The designed detector types were synthesized for Altera Flex10K CPLDs. Each detector type was designed for fixed-point numeric precisions of 8, 12, and 16 bits. The BER performance of each detector was characterized and the chip area for each detector was estimated.

The BER performance of the baseband differential detectors was virtually identical, although the DRBB had slightly better performance than the CRBB. This performance advantage is attributed to the shorter lengths of the filters in the DRBB. Since the samples go through fewer arithmetic operations, the DRBB filters suffer from diminished finite numeric effects. If the CRBB used extremely wide bit widths within the filter so that no rounding or truncation was performed in intermediate calculations, it is believed that the BER performance of the CRBB and DRBB would be identical.

The IF differential detector has poorer BER performance than the baseband differential detectors. This performance degradation is attributed to the difficulty in realizing the Hilbert transformer. The non-ideal characteristics of the transformer make the complex signal decoding process less accurate. The Hilbert transformer could be made more accurate by adding additional filter length, although this increases the implementation complexity. The optimum length of the transformer could be studied in more detail, so that the performance of the IF differential detector is similar to that of the baseband differential detectors.

The BER performance of the frequency discriminator detector is terrible. The performance degradation results from the differentiation and integration processes within the detector. These processes are continuous in nature and are not approximated well by the discrete operations in a digital implementation. The functions can be improved by using a greater sampling rate in the digital realization. However, the rates required for accurate representation are over 100 samples/symbol, which is prohibitively expensive in terms of implementation complexity. It is believed that the FM detector is still a simple and cost effective detector, but is more effectively

realized in the analog domain.

The BER performance for the detector types was compared using three numeric precisions. Interestingly, the performance of the 12 bit detector was comparable to the 16 bit detector, for all the detector types. With this knowledge, it is recommended that the 12 bit representation be used for a digital detector, since there is no significant advantage to using the 16 bit detector. The 8 bit detectors had significantly worse performance than the 12 and 16 bit detectors. This realization is only recommended if the designer wants to decrease implementation complexity at the expense of the detector performance. The BER performance of the detector realizations was compared when confronted with multiple concurrent impairments. All the detector realizations displayed a greater sensitivity to the impairments than the ideal detectors presented in Chapter 4.

The detector types were also compared on their CPLD area estimate. The IF differential detector had the smallest area estimate, but was followed closely by the DRBB. The CRBB and frequency discriminator detector had area estimates that are over twice as large as the other detectors.

The IF differential detector has a relatively small area estimate, since it only requires one RRC filter. The filter is bandpass, but is less expensive to realize than the comparable baseband filters. The remainder of the processing is slightly more complicated than the other detectors (Hilbert transformer and lowpass filters), but is more than offset by the area reduction required for the filtering.

The DRBB differential detector has a small area estimate due to the lowered sampling rate in the latter part of the detector. The decimated sampling rate allows the RRC filter to be approximated with many fewer taps than the comparable CRBB filter. Additional complexity is added by the half-band filters required for the decimation process, but the net effect is a reduction in the area estimate for the detector.

The CRBB and frequency discriminator detector each have very large area estimates. The majority of the area is taken up by the two RRC filters required for the detection process. The area required for the remainder of the detection blocks

is small when compared to the filters. The CRBB detection is straightforward after the filtering, so it has an advantage over the frequency discriminator detector which requires extra area to implement the FM demodulator, which consists of a cross-differentiate and multiply operation.

The area estimation showed that the major factor that influences complexity is the size of the RRC filters. A Butterworth analog filter can be used in place of the RRC filter, which reduces the area estimate by at least 50% in the detectors. However, a performance penalty is introduced when using the Butterworth filter in place of the RRC filters. Transmitter phase compensation reduces the degradation caused by the analog filter. This technique is recommended to reduce the modem complexity, while maintaining reasonable performance.

The modem realizations were subjected to a typical impairment scenario in Chapter 5. The DRBB modem realization has the best performance when confronted with the impairments. The CRBB and IF differential detector performance is slightly worse than that of the DRBB.

The digital frequency discriminator detector realization is not recommended for the wireless application described in Chapter 1. Not only is this detector's area estimate the largest of all the synthesized detectors, but its BER performance is also the worst. A designer should not consider this detector type when planning a digital realization of the modem. However, the designer may want to pursue this option when realizing this detector with analog hardware.

The CRBB detector realization has good BER performance. However, due to the large area required by its RRC filters, the modem is not recommended, since its complexity is high relative to the other detectors.

The IF differential detector realization is attractive because it had the lowest implementation complexity of the detectors. Unfortunately, its BER performance was worse than the baseband differential detectors. For this reason, this detector is not the best option for this application.

The DRBB realization is the recommended choice for this wireless application. It has the best BER performance of all the detectors, even when confronted by

common impairments. The size estimate of the DRBB is relatively low and is only slightly more complex than the IF differential detector. These factors make the DRBB detector realization the most attractive for this application. As discussed earlier, the 12 bit detector realization seems to be the best compromise between both implementation complexity and BER performance.

6.3 Recommendations for Future Study

The thesis has uncovered a number of possible areas for future study. These recommendations for future study are presented here.

A major limitation in completing this thesis was the length of time it took to perform the simulations. Unfortunately, simulating enough bits to obtain a statistically significant BER is very lengthy. For example, some points on the BER curves took one week to simulate. This limited the minimum simulated BER to between 10^{-4} and 10^{-5}. Some applications may require BER performance characterization for lower BERs. These simulations could be executed on faster computers than were available to the researcher, which would generate additional data. It would be interesting to determine if different effects would be observed when simulating higher E_b/N_o than those presented in this thesis.

A limited number of impairments were characterized. Additional impairments of interest could be simulated to observe their effects. These impairments could include multipath channel effects or other nonlinearities.

The BER performance of the frequency discriminator detector was unable to be characterized for comparison purposes, due to the digital sampling nature of the simulations. Additional investigation may deduce a method to simulate this detector so that its BER performance could be compared to the results for the baseband and IF differential detectors.

The frequency discriminator detector lends itself well to an analog hardware implementation. Designing this detector at microwave frequencies would allow the downconversion stage of the receiver to be removed, which would simplify the re-

sulting receiver. Additional investigation is required to determine the feasibility of such a detector at frequencies suitable for this wireless application.

Results presented in this thesis were generated through simulation. Implementing the various modem configurations in digital hardware would allow the measured BER performance to be compared to the results shown in this thesis.

The phase compensation technique described in Section 5.11 looks promising. However, the technique should be implemented in hardware to further study its effectiveness. In this thesis, the use of this compensation technique with $\pi/4$-DQPSK was presented, but it is anticipated that the technique could be applied to other linear modulation methods that employ matched filtering in the receiver.

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