A DIGITAL FREQUENCY-CUM-RATE OF CHANGE OF FREQUENCY RELAY

A Thesis

Submitted to the Faculty of Graduate Studies and Research
in Partial Fulfilment of the Requirements
for the Degree of

Master of Science

in the Department of Electrical Engineering
University of Saskatchewan

by

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Saskatoon, Saskatchewan
November 1978

ACKNOWLEDGEMENTS

The author expresses his gratitude and appreciation to Dr. M. S. Sachdev for his guidance and assistance in the preparation of this thesis.

The author is also grateful to Professor A. E. Krause for his help in the work conducted on PDP-8/E minicomputer.

Special thanks are extended to his wife for her encouragement during the study.

Financial assistance provided by University of Saskatchewan is thankfully acknowledged.

UNIVERSITY OF SASKATCHEWAN

Electrical Engineering Abstract 78A193

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ABSTRACT

Under-frequency relays are often used to detect deficiency of generation in a power system and to shed load to restore generation-load balance. These relays operate somewhat after the frequency falls to a prespecified level.The difference between the set frequency and the frequency at which load shedding is initiated depends on the rate at which the frequency continues to change. To eliminate this delay frequency-cum-rate of change of frequency relays have been proposed, developed and used. These relays are designed using analog electronic circuits.

The availability of digital processing devices has considerably increased during the last few years while the cost of these devices has been rapidly decreasing. The use of digital processors in system control and protection is at the verge of becoming economically competitive.

This thesis examines the presently used methods of measuring frequency and rate of change of frequency at a power system bus. A few new and novel approaches are then proposed. Also examined are the relative advantages and suitability of these approaches for use in relays based on digital processors. A relay design using the selected techniques of measuring frequency and rate of change of frequency is then outlined. Implementation of this design and relay tests performed in the laboratory are also described.

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1. INTRODUCTION

1.1 Background

The functioning of the society is presently dependent on the continuity of power supply. Partial or total blackouts usually have serious economic and social consequences. To ensure a continuous supply of electrical energy and to minimize damage to the equipment, a power system is protected against faults. Relays are used to detect intolerable and unwanted operating conditions and to then initiate actions to either correct the abnormality or to isolate the faulted section.

The first protective device developed and used to isolate faulted equipment in a power system is the fuse. They are quite effective in limiting the damage due to faults and are, therefore, widely used in distribution circuits. The major disadvantage of using fuses is that they have to be replaced before power supply can be restored. The early relay designs used the attracted armature structures Later designs used induction disc structures which are more flexible and reliable. Continuous development of networks dictated that relays have higher operating speeds and increased ability to select the faulted zone. In 1920's, induction disc inverse time and high speed differential relays were introduced[1]. Later, balanced beam and induction cup units were used in protective devices. These structures proved useful in designing devices and systems which can meet the protection requirements of the present day power systems of

large size and complexity.

Solid state (electronic) relays were introduced some years ago and have gradually become acceptable. Many forms of phase and amplitude comparators have already been developed and used. These devices generally use analog and digital integrated circuits in addition to discrete components. Advances in the technology of computing processors have made it possible to consider their use in the area of power system protection. Digital processor based relays attempt to perform the functions normally expected of electromechanical and static (solid state) relays. Because of their high operating speed, inherent flexibility and ability to perform conditional branches and storing data acquired over long periods of time,[2] computers can perform additional tasks which the previously designed relays can not. The use of digital computers for system protection was first suggested by Last and Stalewsky[3]. The feasibility of protecting a substation by a digital computer was then investigated and reported in 1968 by G. D. Rockefeller[4]. Mann and Morrison[5] demonstrated the feasibility of applying a digital computer for transmission line protection. Computerized transformer and generator protection have also been attempted[6,7]. Sachdev and Wind[8] demonstrated that ditigal computers can be used for differential protection of generators.

1.2 Underfrequency Protection and Frequency Relays

Frequency relays are generally used to automatically disconnect prespecified blocks of load in case of generation deficiency in a

system and, thus, restore the system frequency to normal levels.

Loads were shed manually by the operators before the frequency relays were used for this purpose. To detect sub-normal frequency conditions and take action in time is not easy for an operator especially when the frequency drops at a high rate. As the power systems increased in size and complexity, it became impractical to manually shed load without jeopardizing system operation. This difficulty was overcome by installing frequency relays at substations and having them trip breakers of selected feeders supplying loads.

Electromagnetic frequency relays were first developed and are widely used at present. These relays respond to a decrease in the frequency; a prespecified time delay is also incorporated. The delay in operation is not constant; it depends on the rate of change of frequency. Relays which respond to a combination of the frequency and rate of change of frequency have also been developed. A solid state relay developed by the Ontario Hydro[3] responds to the rate of change of frequency as the system frequency reduces to sub-normal levels. Prespecified blocks of load are shed at various levels of rate of change of frequency after the system frequency decreases to a prespecified level. Durkin, Eberle and Zarakas[10] developed a frequency relay which responds to a combination of the frequency and its rate of change. This relay uses analog circuits in its design and its frequency vs rate of change of frequency characteristic is continuous. Widrevitz and Armington[11] developed a frequency cum rate of change of frequency relay using digital electronics.

1.3 Objectives of the Project

The objectives of the project are to design a computer based frequency cum rate of change of frequency relay. A conceptual arrangement of this relay is shown in Figure 1.1. A set of potential transformers reduce the voltage signals from the E.H.V. level to 110 Volts. These signals are reduced to 25 Volts peak to peak and applied to a preprocessor which is basically a low pass filter. The output of the processor is applied to a hardware block which measures the time durations of the cycles of the input signals. These measurements are in the form of counts of high frequency pulses counted in the duration of interest. The counts are then transferred to a computing device which calculates the frequency and the rate of change of frequency and then decides if any action to shed load is warranted or not.

This thesis presents a design of the hardware processor, evaluation of the methods of measuring frequency and the rate of change of frequency, a design of the frequency relay and results of the tests performed on this relay in the lab.

The philosophy of frequency relaying and the necessity of their use are examined in Chapter 2. The reasons for using both frequency and its rate of change for a frequency protection scheme are discussed. A basic form of an underfrequency protection scheme is also briefly presented.

Methods of determining frequency are presented in Chapter 3. Accuracy and suitability of these methods for digital relaying are examined. Two of these methods are found to be adequate for use in a software based relay.

Techniques of measuring the rate of change of frequency are presented in Chapter 4. The suitability of these methods are examined and reported in this chapter. Two of the four methods discussed in Chapter 4 are found to be suitable for determining the rate of change of frequency for digital relaying.

The hardware and software of the proposed digital frequency cum rate of change of frequency relay are described in Chapter 5. The performance of the relay was tested in the laboratory; the results of these tests are also given in this chapter.

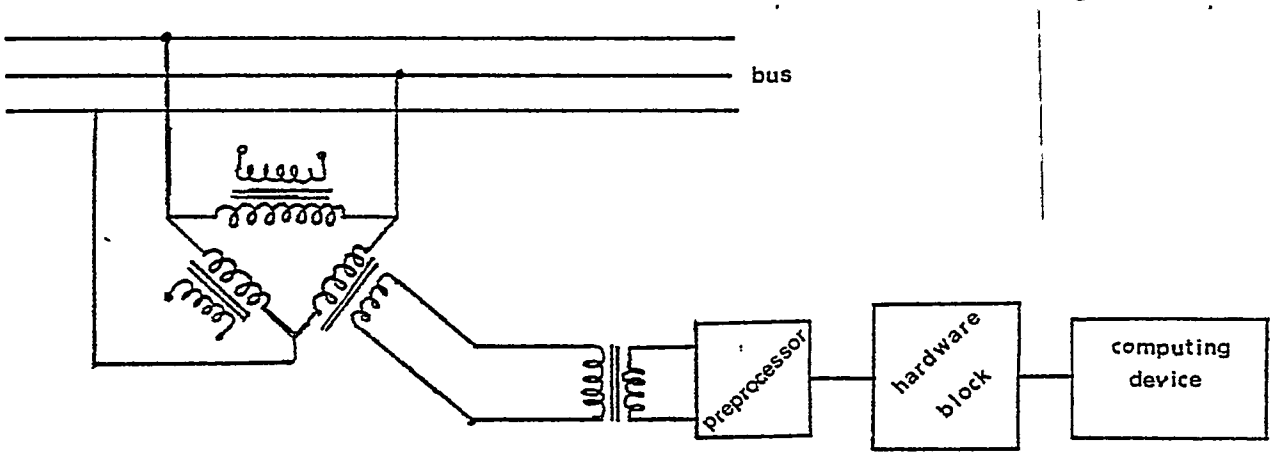

Fig. 1.1 A conceptual arrangement of a software based frequency relay.

2. PROTECTION PHILOSOPHY AND FREQUENCY RELAYING

This chapter briefly describes the general philosophy of protecting power systems. The hazards of operating a system at subnormal frequencies and the necessity of frequency relaying are discussed. The advantages of relays which respond to a combination of the system frequency and the rate of change of frequency are enumerated. The commercially available frequency relays are also briefly described.

2.1 General Protection Philosophies

Relays are used to limit equipment damage and to maintain continuity of service in modern power systems. Protective relays detect the presence of faults, such as, short circuits between phases and to ground, and isolate the faulted equipment by opening appropriate circuit breakers. Some other relays, such as, automatic reclosing relays attempt to restore power on lines which may have been removed from service to isolate temporary flash overs to ground. To minimize the effects of disturbances, a protective system should be reliable and selective and should be capable of operating at high speeds. It is also desirable that the cost of a protective equipment be commensurate with the benefits derived by its use. These objectives can not usually be met and, therefore, some compromises are made to arrive at acceptable designs.

2.1.1 Classification of relays

ANSI Standard C.37.90(IEEE 313)[12] classifies relays by:

i) the functions they perform.

ii) their operating principles and the operating principles of their structures.

iii) their operating characteristics.

iv) the inputs which excite the relay.

The relays classified by their functional categories include monitoring relays, protective relays, programming relays, regulating relays and auxiliary relays. Percentage, thermal, solid state and electromechanical relays are some of the examples of relays classified by their operating principles or the operating principles of their structures. The relays classified by their performance characteristics include, among others, distance, directional, overcurrent, under-voltage and ground and phase comparison relays. Current, voltage, pressure, frequency and temperature relays are the examples of relays classified by the types of inputs which excite the relays.

2.1.2 Applying protective relays

Before the relays classified in the last paragraph are applied, the following aspects of the system and its operating experiences need to be considered.[13]

i) System configuration.

ii) Existing protective equipment and experiences of its maloperation or failure to operate.

iii) Present operating procedures and practices; possible future expansion.

iv) Desired degree of protection.

v) Fault levels.

vi) Maximum load.

vii) The ratios of voltage and current transformers.

viii) Location of voltage transformers.

ix) Parameters of generators, lines, transformers and loads.

Many of these aspects need to be considered for applying relays which respond to system frequency and its rate of change.

2.2 Frequency Relaying

Protection philosophy and classification of relays have been briefly given in the last section. One of the relays classified by the type of input quantity used is the frequency relay. The reasons for applying the relays of this type are discussed in this section.

An unbalance between generation and load tends to change the system frequency which should be maintained very close to its rated value. Frequency relays are usually used to detect changes in frequency, and to then initiate action to restore the frequency to its nominal value.

Frequency changes which can be generally tolerated in a system, are determined by the characteristics of the rotating equipment. For example, the blades of a steam turbine have resonance frequencies in the neighborhood of three percent below the rated frequency of the system. This resonance usually damages the blades seriously; the damage suffered is cumulative in nature.[9] To minimize the possibility of fatigue failure due to vibrations, operation at low frequencies is limited to the levels given in Table 2.1.[14] A perusal of this table suggests that normal frequency levels should be restored as quickly as possible.

Table 2.1 Maximum Cumulative Operating Time at Subnormal Frequencies

Operating Frequency-Hz	59.4	58.8	58.2	57.6	56
Total Permissible Operating Time (minutes) over the Life of the Unit	No Limit	90	10	1	0

The speed of generating station auxilaries, such as, fans, pumps and mills which are driven by electrical motors decreases as the system frequency reduces. A 10% reduction of speed of the auxiliaries can lower the plant output by up to 30%[15]. A decrease in frequency also requires that the operating flux must increase if the operating voltage level is to be maintained. This increases the magnetizing current of transformers, motors and other electromagnetic devices and, in turn, causes excessive heating of these devices and increases the reactive load of the system. Another effect of a drop in system frequency is the reduction of the reactive power generated by the capacitors, overhead lines and underground cables. The reactive power balance is, therefore, adversely affected if the system is allowed to operate at sub-normal frequencies. Operating time of most induction relays increases with a decrease in system frequency.[9] Accuracy of measuring instruments is also affected by frequency deviations.

2.3 Load Shedding

The frequency of a power system remains constant if the generated power is equal to the sum of all loads plus system losses.

An upset of this balance tends to change the system frequency. A decrease in available generation causes a decline in the frequency of a system if it is isolated from the interconnected network and sufficient spinning reserve is not available. In such cases, under-frequency relays should automatically shed some load to raise the frequency back to normal. This action involves deliberate interruption of power to some customers but is essential to prevent excessive damage to major equipment and subsequent major dislocation of services.

2.4 Frequency Relays

As discussed in the last section, frequency relays are used to shed load. Two types of relays generally used are the induction disc/induction cylinder and solid state types. The induction disc and induction cylinder relays are of the electromagnetic type whereas the electronic relays use analog and digital circuits. These relays respond to a decrease in frequency and have characteristics similar to those shown in Figure 2.1[13]. The relay operation is delayed by a specifid time after the frequency is detected to have declined below a set value. It is obvious that the frequency at the time of relay contact closure will be different from the set value. The difference will depend on the rate at which frequency has been declining.

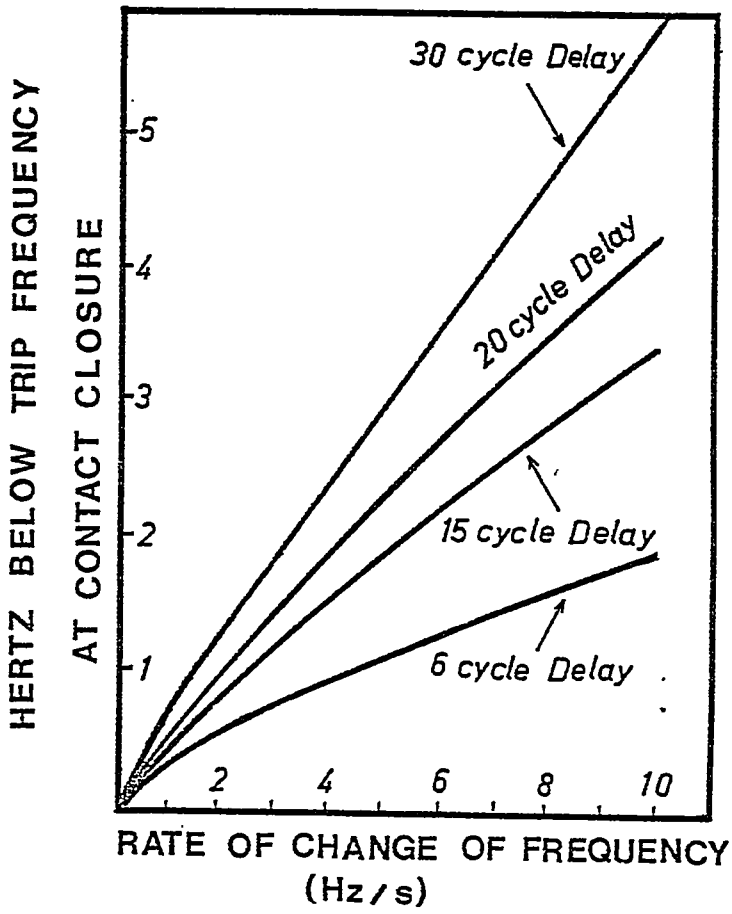

Figure 2.1 Characteristic of an induction cylinder frequency relay.

2.5 Rate of Change of Frequency

It has been pointed out in the last section that the system frequency at the time of relay contact closure depends on the rate at which the frequency has been declining. This problem can be alleviated by modifying the criterion of tripping to include a rate of change of frequency feature which is discussed in this section.

Frequency of a power system declines at a rate inversely

proportional to the system inertia and directly proportional to the difference between the generated power and system load. This can be mathematically expressed as:[14]

$$\frac{df}{dt} = -\frac{\Delta P}{M} \qquad (2.1)$$

where: f is the system frequency;

ΔP is the unbalance between generated power and load;

M is the inertia constant of the system.

It is obvious from this equation that, for a given system, the rate of change of frequency indicates the unbalance between generation and load. A frequency cum rate of change of frequency relay is, therefore, likely to be more effective than a frequency relay.

Another advantage of including the rate of change of frequency feature in a frequency relay is a reduction of the dynamic error between the frequency setting and the supply frequency at the instant of relay operation. This advantage increases with an increase of the rate of frequency change.

2.6 A Load Shedding Scheme

The necessity of load shedding when a generation-load unbalance occurs has been discussed in the last section. For effective results, a load shedding scheme should be carefully designed. Some aspects associated with the design of such schemes are given in this section.

A load shedding scheme should decide when some load should be curtailed. It should also decide how much load needs to be shed and which circuit breakers should be opened to reduce the system load. These requirements are somewhat different in each case and, therefore,

load shedding schemes should be specifically designed for each system.

One of the features of a load shedding scheme is its upper and lower frequency limits. No load shedding is necessary if the system frequency is above the upper limit. Also, the system frequency is not allowed to fall below the lower limit. A number of load blocks are shed as the system frequency falls below the upper limit and approaches the lower limit.

The frequency of an interconnected system doesn't change appreciably if enough spinning reserve is available and the interconnections remain in operation. Maximum generation loss which can be tolerated without impairing the integrity of the system is calculated as demonstrated in the following example.

Consider an interconnected network of three systems as shown in Figure 2.2 and consider that a disturbance causes a deficiency of D_1 MWs in system 1. If the deficiency made up by each system is proportional to its capacity, additional power transfers between the systems will be given by

$$T_{21} = \frac{D_1 C_2}{C_1 + C_2 + C_3} \tag{2.2}$$

$$T_{31} = \frac{D_1 C_3}{C_1 + C_2 + C_3} \tag{2.3}$$

where: C_i denotes the capacity of the ith system.

The remaining deficiency which is equal to $\frac{D_1 C_1}{C_1 + C_2 + C_3}$ will be made up by system 1. The decrease of frequency due to the loss

of generation is determined by the permanent droop of the governors and is given by:

$$\Delta f = \frac{\text{generation loss}}{\text{Capacity X Permanent droop}} \qquad (2.4)$$

A 1000 MWs load over generation unbalance in system 1 will cause the intertie flows, T_{21} and T_{31}, to increase by 37.5 and 929 MW. If the normalized permanent droop is 1.0, the decrease of frequency for correcting the unbalance will be 0.25 Hz. The upper frequency of a load shedder for this system should, therefore, be 59.75 Hz if the maximum unbalance which can be absorbed by the system is 1000 MWs. In this case the system integrity will be maintained for frequencies above 59.75 Hz and there will be no danger of the frequency falling to unacceptable values if the load over generation unbalance is less than 1000 MWs.

If the tie line connecting areas 1 and 3 is not capable of transmitting the required additional power, the line will be disconnected leaving only systems 1 and 2 as a network with generation deficiency of 1000 MW. The frequency deviation in these areas will be 3.53 Hz which is unacceptable. This example reveals that a generation load unbalance causes large frequency deviations when the integrity of the system is upset.

The low frequency limit of a load shedding program is selected such that the frequency will never fall below the critical value. This limit is dictated by considering the operating problems of steam turbines and power plant auxiliaries. In general, steam turbines should be operated at speeds corresponding to frequencies above 59.5 Hz. Operation below 58.5 Hz is permitted for a limited

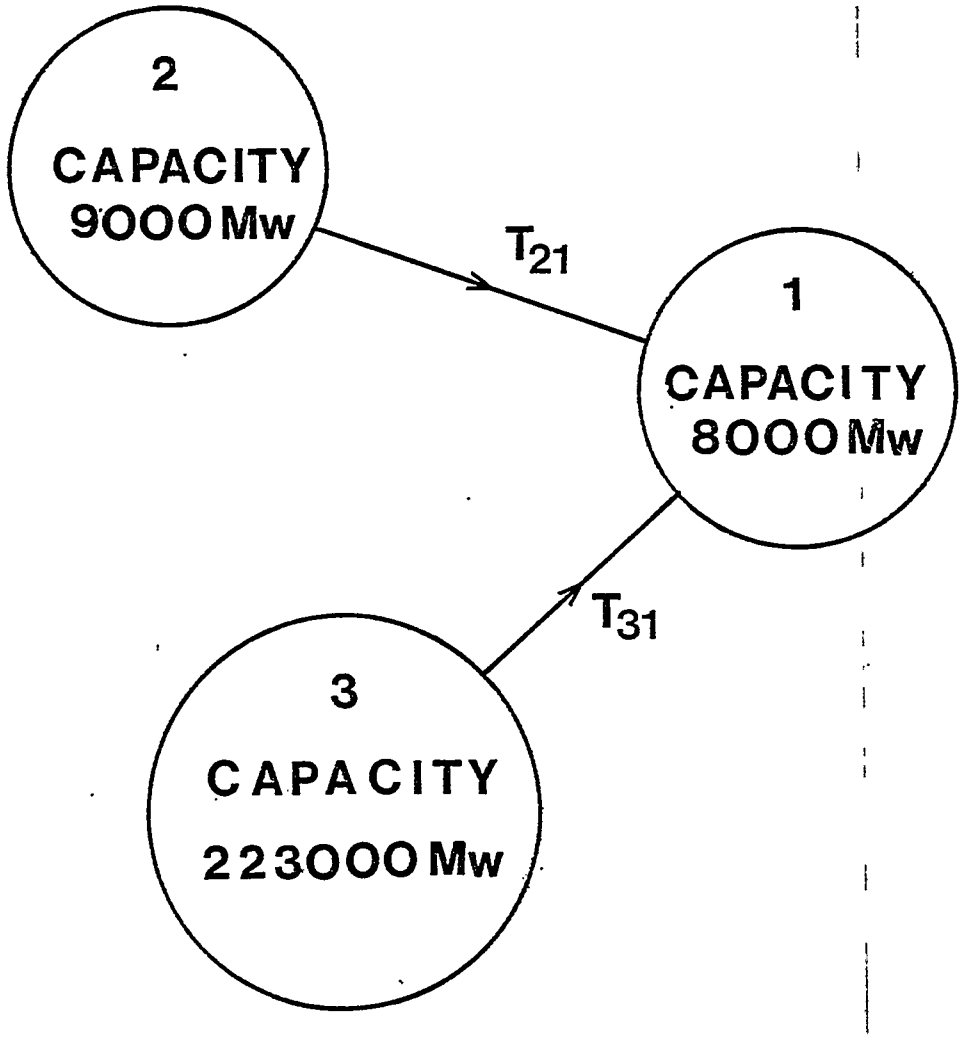

Figure 2.2 An interconnection of power systems.

time only. At this low frequency limit,the entire scheduled load relief process should be completed.

Between the high and low frequency limits a number of load shedding steps are usually introduced. Larger the number of steps selected, smaller is the load shed at each step. This makes the load shedding scheme more flexible but the coordination of the steps becomes more difficult. Experience has shown that, for most systems, three to five steps for load shedding are adequate.[13]

The total load which should be shed depends on the maximum anticipated overload. Theoretically, there is no limit to the extent of load to be shed. Service can be restored much more rapidly if 100% load is shed instead of allowing a system to collapse.

A four-step load shedding program is shown in Figure 2.3[16] which is designed to protect up to 100% overload and settles at 57 Hz Load shedding curves for settling at 58,59 and 60 Hz are also included in this figure. The frequency at which the system will settle after a predetermined load is shed for specified overloads can be determined from this figure. For example, when the overload is 20%, the load is shed in two steps and the frequency will settle at approximately 59.5 Hz. For some overloads the frequency will rise above 60 Hz after load shedding because the shed load is more than the extent of overload.

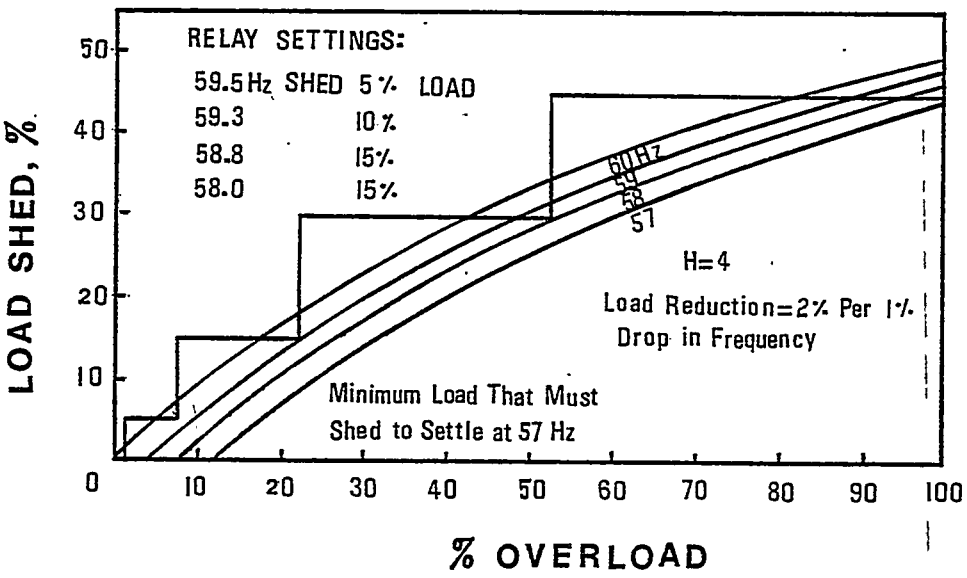

Figure 2.3 Four step load shedding program to protect up to 100% overload.

2.7 Other Frequency Relay Applications

Frequency relays are used for many functions other than detecting under frequency and shedding load. Some of these functions are as follows [13].

i) Frequency relays are also applied to protect generators from overspeed during start up and loss of load.

ii) Frequency relays can be applied to isolate generating units when load shedding is not able to restore frequency to acceptable levels.

iii) Frequency relays can also be used to disconnect interconnections between systems when load shedding is not able to restore frequency to acceptable levels.

A brief description of protection philosophy has been presented. The importance of frequency relaying and some applications of under frequency relays have been outlined. The basis of a load shedding program has also been discussed in this chapter.

3. TECHNIQUES OF MEASURING FREQUENCY

The importance of measuring frequency and the rate of change of frequency for protecting power systems has been discussed in Chapter 2. It has been demonstrated that, both the frequency and its rate of change need to be accurately measured for providing adequate protection. Methods of measuring frequency are examined in this chapter. The suitability of these methods is also investigated.

3.1 Classification of the Measurement Techniques

Until recently, electromechanical devices were used to measure frequency. These devices have, however, been gradually replaced by electronic equipment using digital counters. The approach is simple and is more accurate than the electromechanical devices. The methods for determining frequency by digital techniques may be classified into the following categories:

i) Direct method.

ii) Measuring time for a specified number of periods and calculating frequency.

iii) Measuring time for a specified number of periods and estimating frequency.

3.2 Direct Method

This approach consists of counting the number of cycles of the input signal during a specified time interval, Tg; called gating time. This interval is usually controlled by an internal reference

oscillator. The recorded count will be the frequency in Hz if the gating time is one second. By selecting intervals which are multiples or submultiples of one second, different resolutions of the measurement can be achieved. The basic approach is described by the block diagram of Figure 3.1. The input signal is applied to a pulse shaping circuit which converts the sinusoidal input to short duration pulses -one for each cycle. The output of the reference oscillator controls the gate and enables the counting of the pulse shaper output during a gating period. The accuracy of this approach depends on the maximum gating time available for measuring frequency. For example, the accuracy of the frequency measurements of a 100 Hz signal will be within ±1% if the gating time is one second. Longer gating times are needed to obtain better accuracies; but large gating times cannot be permitted in power system protection applications.

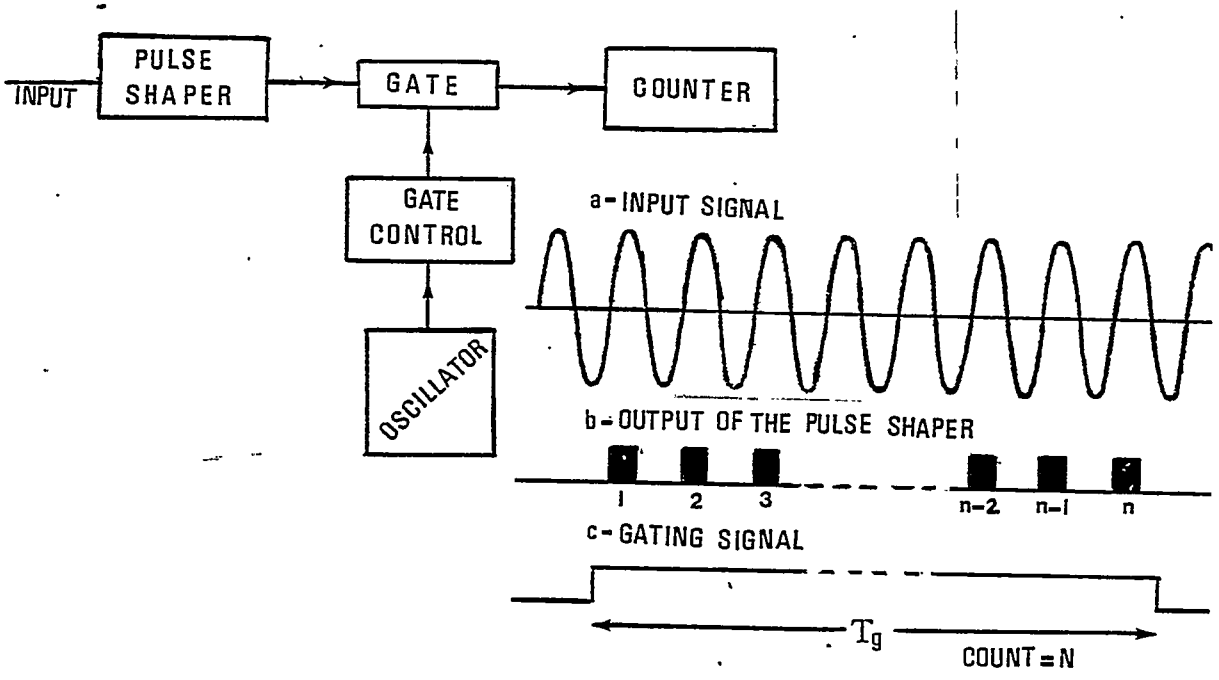

Figure 3.1. Simplified block diagram of a frequency counter.

The accuracy of this approach can be improved by counting half cycles instead of full cycles. This approach reduces the error of measurement by 50%. In other words, the accuracy of measuring frequency by counting half cycles in a specified time, Tg, is the same as the accuracy obtained by counting full cycles in an interval equal to twice the specified time (2 Tg).

When measuring the frequency of three phase power systems, the accuracy of the direct method can be further improved by utilizing the information of all three phases. If the frequency is obtained by averaging the number of cycles of the three phases observed in a specified interval, Tg; the result will be similar to that obtained by using one phase and gating intervals of 3 Tg. In this approach, the three signals can be applied to pulse shaping circuits which convert the waveforms to short pulses for counting during each gating interval. Figure 3.2 depicts waveforms encountered in this approach. Should the gating waveform start just after a zero crossing of the Phase A, the counter of this phase will indicate n-1 cycles whereas the Phases B and C counters will record n cycles. The frequency will, therefore, be given by $1/3 \cdot [(n-1) + n+n] = n-1/3$. This measurement is much closer to the actual frequency than n-1 which would be obtained if only the Phase A signal was used. The averaging process eliminates most of the error caused by the missed count in Phase A; but the accuracy of measurements obtained by this method is also not adequate for power system protection.

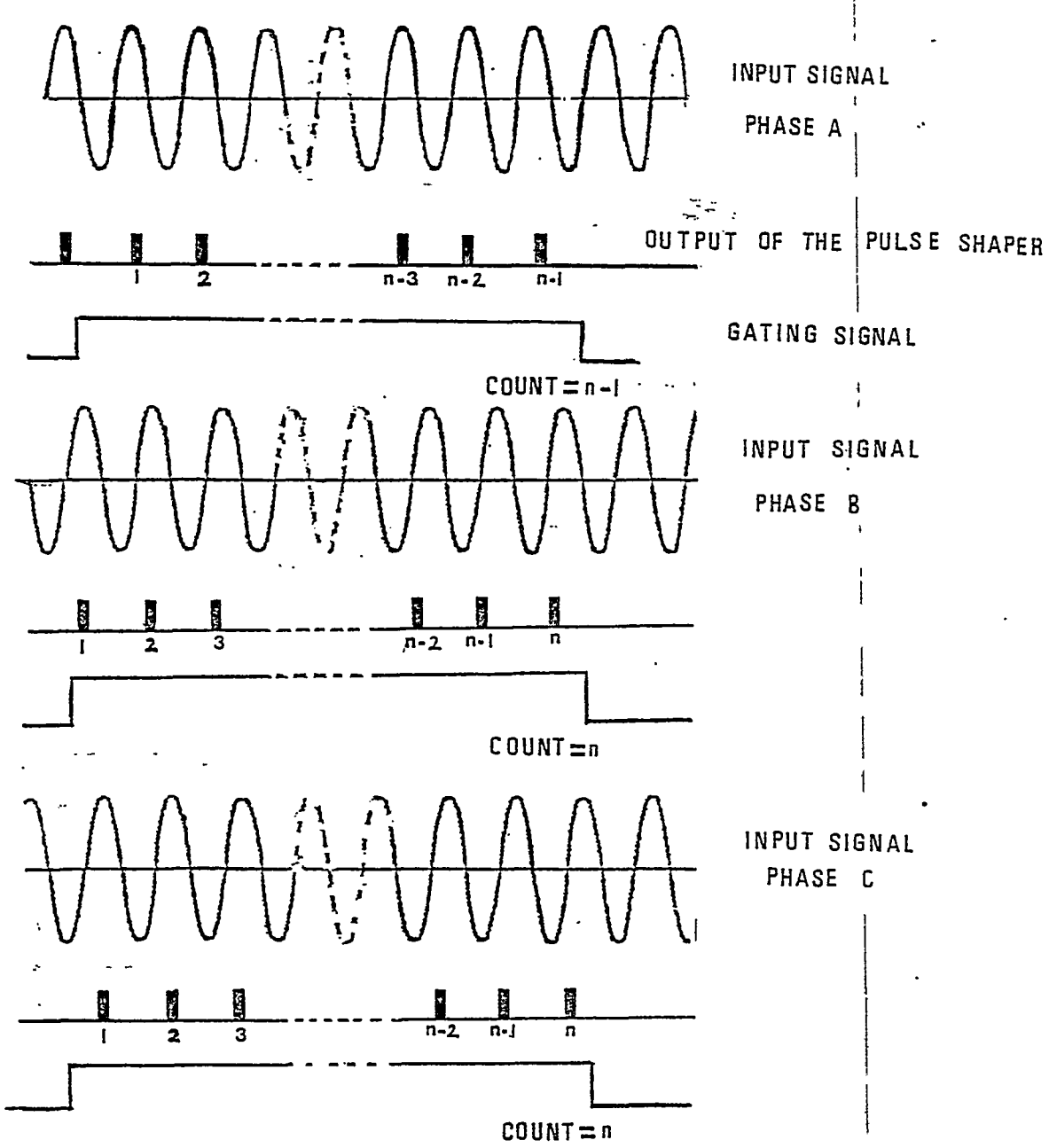

Figure 3.2. Voltages, pulsed information and gating signals for measuring the frequency of a three phase system

The accuracy of frequency measurements can be further improved by using the 3 phase approach and counting half cycles of each phase. The improvement is, however, not adequate to make the approach suitable for measuring the frequency of power systems for protection purposes.

3.3 Measuring Time for a Specified Number of Periods and Calculating Frequency

Power system applications require that the frequency be measured in a few cycles and the accuracy be better than that of the techniques described in Section 3.2. An approach which satisfies this requirement consists of measuring the time duration of an integral number of cycles of the signal and calculating the frequency from this measurement. High frequency pulses produced by an oscillator can be counted during specified cycles of the input signal to measure the time duration. A 1 MHz oscillator provides a count of 10000 in a period of 100 Hz signal. The accuracy of this approach is at least an order of magnitude better than that obtained by the direct method using gating periods of 10 seconds. Moreover, the measurement is completed in 10 msec. This method makes use of the basic relation between the period and frequency; frequency is the reciprocal of the time of a period. If the time of an integral number of cycles, say p, is measured using a high frequency clock, the frequency of the signal can be calculated by using Equation 3.1.

$$f = \frac{pfc}{N} \tag{3.1}$$

where, fc is the frequency of the clock,

N is the number of high frequency pulses counted in p cycles.

Random phasing of the clock pulses and pulses generated at the zero crossings of the input signal cause errors in measurements. These errors can be reduced by using longer gating periods (selecting p grater than one). This approach, however,slows the speed of completing

the measurement.

The present frequency measuring techniques use only one phase of the three phase power system. It has been demonstrated in Section 3.2 that information from all three phases can be used to improve the accuracy of frequency measurements by direct methods. A similar approach can be used in measuring time durations of all the three phases, and then calculating the system frequency. Advantages expected by utilizing information from all the three phases are explained in the following example. Consider that the frequency is determined by measuring the time duration of p cycles, p = 3, of a single phase signal as shown in Figure 3.3. The N pulses recorded during the measurement is the average information of three cycles. Now consider that the frequency is determined by measuring the time duration of one cycle of all the three phases of the system as shown in Figure 3.4.

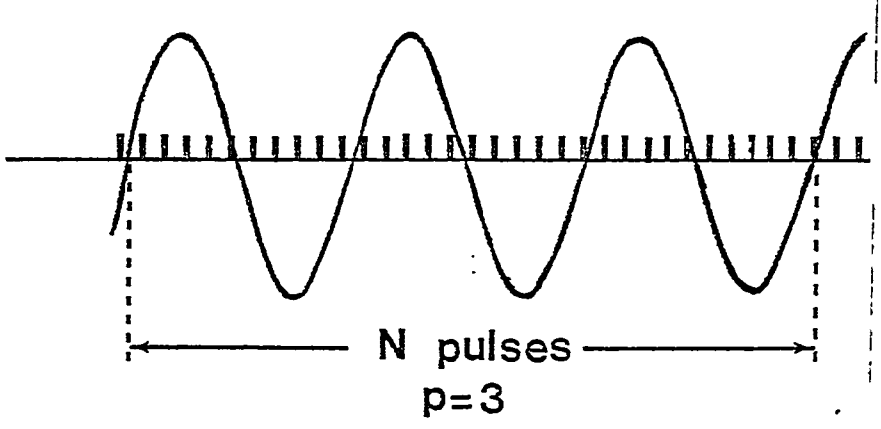

Figure 3.3. Measuring time duration of a single phase signal.

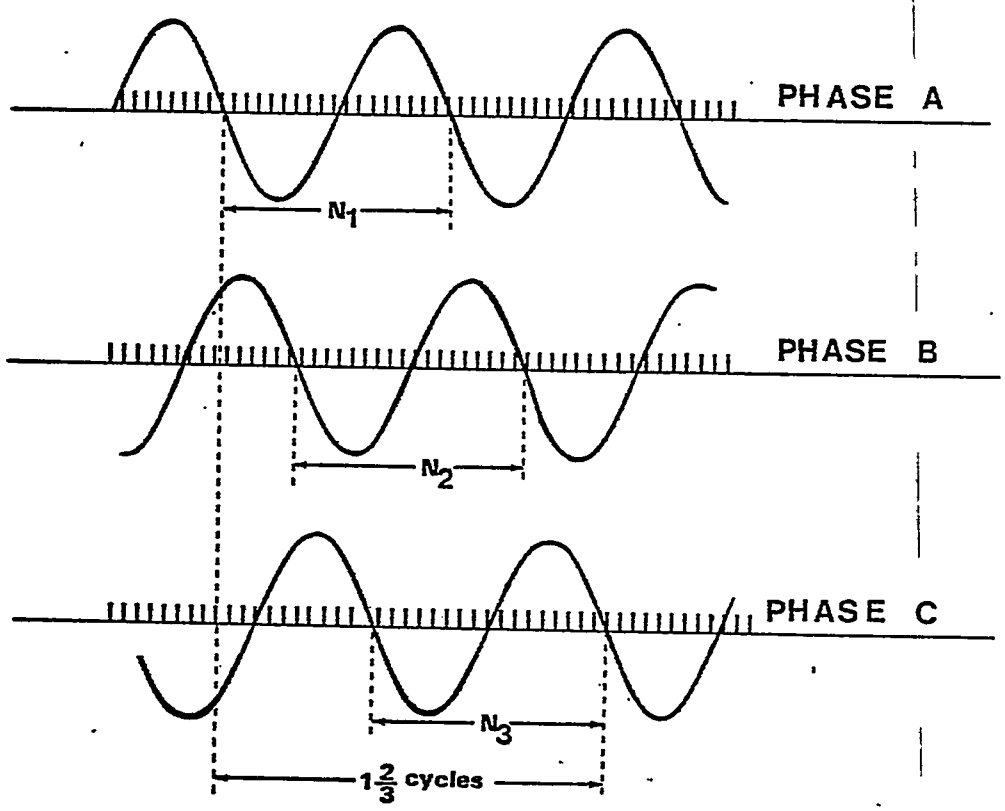

Figure 3.4. Measuring time durations of the three phase signals.

If the high frequency counts for a cycle of the three phases are N_1, N_2 and N_3, average count $\frac{1}{3} \cdot (N_1+N_2+N_3)$ can be used to calculate frequency. The frequencies calculated from the time period of three cycles of a single phase signal and from the time durations of one cycle of all the three phases will have similar levels of accuracies. The measurement is completed in $1\frac{2}{3}$ cycles in the three phase approach compared to three cycles of the single phase approach. This represents a 44 percent saving in the time required for measuring frequency.

The method of measuring period has basically three potential sources of error; gating error, high frequency clock errors and noise.[17]

3.3.1 Gating error

A random phase relationship exists between the gating and gated signals. This introduces an inherent error of ±1 count as is obvious in Figure 3.5.

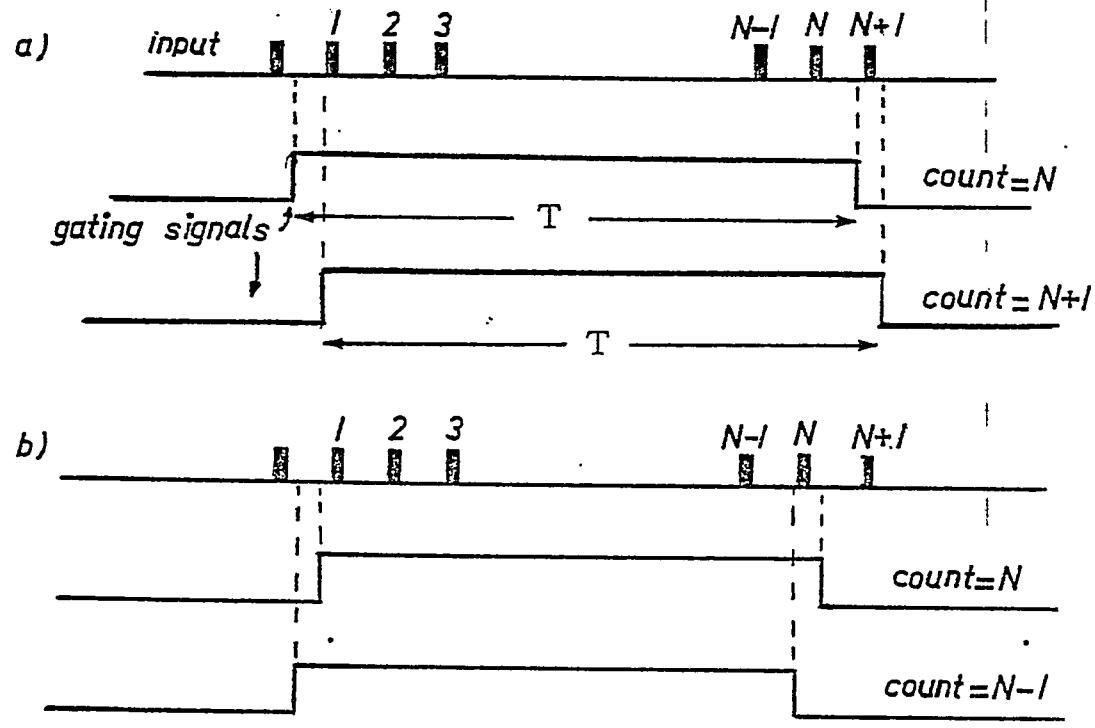

Figure 3.5 Gating error

If the gating waveform starts midway between the two input pulses, the recorded count will be correct, say n. Should the gate open just before or during an input signal pulse, the recorded count will be n+1. The recorded count will be n-1 if the gate opens just after an input pulse. The count error is, therefore, -1 or +1 and corresponds to a frequency error of approximately $\pm \frac{1}{n} f$.

3.3.2 High frequency clock errors

The accuracy of measurements also depends on the stability and accuracy of the high frequency clock which is usually a crystal

oscillator. The accuracy of most crystal oscillators is temperature dependent. If frequency measurements are recorded at room temperature, no special measures, such as, using temperature controlled ovens will be needed.

3.3.3 Noise

Noise distorts the input waveforms and causes the trigger point to vary from cycle to cycle as shown in Figure 3.6. The time duration measurements are affected by changing the count n to $n \pm \Delta n$ which changes the measured frequency from f to $f \pm \frac{\Delta n}{n} f$. The measurement errors can be reduced by increasing the interval over which the time is measured. The increase of the measurement interval also reduces the inaccuracies caused by the gating errors and noise. Using longer measurement intervals, however, slows the determination of frequency.

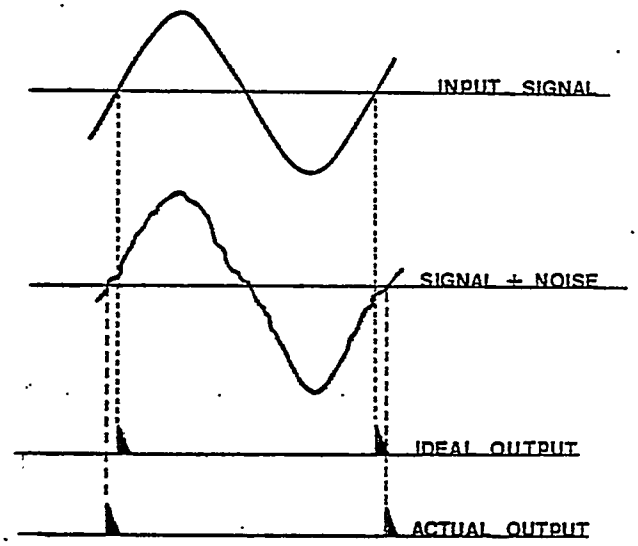

Fig. 3.6 Effect of noise on the zero crossings of the signal.

Effect of presence of D.C. offset on frequency measurements was also studied and it is given in Appendix I.

The method of measuring time for specified number of periods and calculating frequency using Equation 3.1 described in this section can not be conveniently used in digital relays which use computing devices, such as, microprocessors and minicomputer. This is because Equation 3.1 requires that a prespecified number, product of p and fc, be divided by a variable count, N. Approximate methods which avoid this division are discussed in the next section.

3.4 Measuring Time for a Specified Number of Periods and Estimating Frequency

As described in Section 3.2, the frequency of a signal can be measured by counting the number of cycles of the signal in a specified time interval. Another method which is described in Section 3.3 consists of counting high frequency pulses in the time of a specified number of cycles of the signal, then calculating frequency. This method involves a division of a pre-specified number by a variable count of the high frequency pulses. To avoid the division, modified approaches which estimate frequency without resorting to division can be used. These approaches are based on the first and second order approximations developed by using the Taylor series expansion of Equation 3.1. The essential features of these methods are discussed in this section.

3.4.1 First order approach

The Taylor series of a function y(x) in the neighborhood of x_0 is expressed as:

$$y(x) = y(x_0) + y'(x)\Big|_{x=x_0}\cdot(x-x_0) + \frac{y''(x)}{2!}\Big|_{x=x_0}\cdot(x-x_0)^2 + \ldots + \frac{y^n(x)}{n!}\Big|_{x=x_0}\cdot(x-x_0)^n + \cdots \quad (3.2)$$

Using this equation, $y = \frac{1}{f}$ can be expressed in the neighborhood of fo by the following equation.

$$\frac{1}{f} = \frac{1}{fo} - \frac{(f-fo)}{fo^2} + \frac{(f-fo)^2}{fo^3} - \cdots \qquad (3.3)$$

Considering the first two terms of this equation and substituting for f from Equation 3.1, the following equation is obtained.

$$f \simeq \frac{fo^2}{pfc} \cdot \left[\frac{2pfc}{fo} - N\right] \qquad (3.4)$$

In this equation, $\frac{pfc}{fo}$ is the number of high frequency pulses in p periods of nominal frequency, fo. Defining this high frequency count as No, Equation 3.4 can be rewritten as:

$$f \simeq \frac{fo^2}{pfc} \cdot [2No - N] \qquad (3.5)$$

The clock frequency, fc, and periods of measurement, p, can be selected in such a manner that $\frac{fo^2}{pfc}$ becomes a multiple of $2, 2^{-k}$. A division by using a variable count, N, is now transformed to a subtraction and multiplication by 2^{-k}. The subtraction is a simple operation and the multiplication by 2^{-k} can be achieved by a bit shift operation which takes very little computation time. In this manner, a division by N is replaced by operations which are convenient to perform in digital computing devices. The estimated frequency is, however, somewhat inaccurate due to neglecting the second and higher order terms of the Taylor series.

3.4.2 Second order approach

It is also possible to use the first three terms of the Taylor series expansion of $\frac{1}{f}$ (Equation 3.2) for expressing frequency

as a function of the high frequency count, N. Using this approach and a procedure similar to that used in the last section, the following expression is obtained.

$$f = \frac{3}{2} fo - \frac{fo}{2} \sqrt{\frac{4fo}{pfc} N - 3} \qquad (3.6)$$

The accuracy of this approach is better than that of Equation 3.4; but a division by N in Equation 3.1 has been replaced by a square root of a function of N which increases the complexity and computation time instead of reducing these factors.

Another possible approach is to expand the function, $f = \frac{pfc}{N}$ in the neighborhood of No using the Taylor series. This series for a function $\emptyset$ (N) in the neighborhood of No is as follows:

$$\emptyset(N) = \emptyset(No) + \emptyset'(N)\Big|_{N=No} (N-No) + \frac{\emptyset''(N)}{2!}\Big|_{N=No} (N-No)^2 + \cdots \qquad (3.7)$$

Considering only the first three terms of this expansion provides the following equation.

$$\emptyset(N) = f = \frac{pfc}{No} - \frac{pfc}{No^2} \cdot (N-No) + \frac{2pfc}{No^3} \cdot \frac{(N-No)^2}{2!} \qquad (3.8)$$

Substituting N-No = ΔN frequency is given by

$$f = \frac{pfc}{No} - \frac{pfc}{No^2} \Delta N + \frac{pfc}{No^3} (\Delta N)^2 \qquad (3.9)$$

Dividing both sides of the Equation 3.9 by $fo = \frac{pfc}{No}$, the following equation is obtained.

$$\frac{f}{fo} = fpu = 1 - \frac{fo}{pfc} \cdot \Delta N + \left(\frac{fo}{pfc}\right)^2 . \Delta N . \Delta N. \qquad (3.10)$$

This approach eliminates the square root operation. The terms $\frac{fo}{pfc}$ and $\frac{fo^2}{p^2 fc^2}$ are constants; p and fc can be selected such that these

terms are multiples of two, 2^{-k}. This approach replaces a division by a variable, N, by three additions/subtractions, two bit shifts and a multiplication($\Delta N. \Delta N$). Hardware multiplier can be used for this purpose. No hardware dividers are available at present. The accuracy of measurements is considerably improved as compared to the first order approach but the computation effort required by the second order approach is more than that for the first order approach.

3.5 Off-Line Testing of the Methods of Determining Frequency

The methods of measuring frequency have been presented in the previous sections of this chapter. These methods were tested to determine their effectiveness. The test results of the following methods are presented in this section.

i) Measuring time for a specified number of periods and calculating frequency.

ii) Measuring time for a specified number of periods and estimating frequency by using first order approach.

iii) Measuring time for a specified number of periods and estimating frequency by using second order approach.

3.5.1 Measuring time for a specified number of periods and calculating frequency

This method has been explained in Section 3.3. The time for an integral number of cycles is measured from which frequency of the input signal is calculated using Equation 3.1. For the tests described in this section, sinusoidal signals of frequencies ranging from 50 to 70 Hz were simulated in a software program. Clock pulses of frequencies ranging from 10kHz to 1MHz were also simulated in this program. The frequencies of the signals were calculated using Equation 3.1. Time duration of one cycle was used in these studies.

Maximum errors observed from amongst a large number of simulations are listed in Table 3.1. A perusal of this table reveals that, as expected, the observed errors depend on the clock frequency. Higher clock frequencies result in lower errors.

Table 3.1 Maximum Errors Observed in the Frequency Calculated by Equation 3.1 Using Different Clock Frequencies and One Cycle Measurement Duration (p = 1)

Clock Frequency	Maximum Error
10 kHz	± 0.49
50 kHz	± 0.098
100 kHz	± 0.049
200 kHz	± 0.025
360 kHz	± 0.0136
500 kHz	± 0.0098
1 MHz	± 0.0049

The time period of each measurement was then increased from one to four cycles in steps of one cycle. Table 3.2 lists the calculated frequency for the selected measuring intervals. A study of this table reveals that the accuracy improves with an increase of clock frequency and with an increase of the duration of measurement. The disadvantage of increasing the measuring duration is that it slows the speed of measurement. A suitable combination of the clock frequency and the duration of measurement can, however, provide the desired accuracy when Equation 3.1 is used.

Table 3.2 Maximum Errors Observed in the Frequency Calculated by Equation 3.1 Using Different Clock Frequencies and Measurement Durations.

Clock Frequencies	Maximum Error p = 2	Maximum Error p = 3	Maximum Error p = 4
10 kHz	0.248	0.165	0.122
50 kHz	0.049	0.033	0.024
100 kHz	0.0245	0.016	0.0122
200 kHz	0.012	0.008	0.006
360 kHz	0.0068	0.0045	0.0034
500 kHz	0.0049	0.0033	0.00245
1 MHz	0.00245	0.0016	0.0012

3.5.2 Measuring time for a specified number of periods and Estimating the frequency by first order approach

Equation 3.4 developed with the help of Taylor series expansion avoids the division by high frequency count N. This approach has, however, two sources of error. One of these sources is the terms of the Taylor series neglected while developing the equation. Random phasing of the high frequency and zero crossing pulses is the second source of the errors. The errors of first kind can be estimated from Equation 3.11 as follows:

$$fe = f - \frac{fo^2}{pfc} \cdot (2No-N) = \frac{(f-fo)^2}{f} \qquad (3.11)$$

where, f is the system frequency,

fo is the nominal frequency of the system and

fe is the error in the estimated frequency.

Figure 3.7 depicts the frequency error determined by Equation 3.11 as a function of the frequency. As expected, the errors are large for

frequencies substantially different from the nominal value. This is not a major concern because in power system applications frequency is usually not allowed to deviate by more than two or three percent and in this range the accuracy is quite good.

The errors of the second kind are caused by the fact that the observed high frequency count can differ from the true count by ±1. To examine the effect of this error on the measured time periods, sinusoidal signals of frequencies 50 to 70 Hz were simulated in a software program; clock pulses of frequencies ranging from 100 kHz to 1 MHz were also simulated in this program. The frequencies of the signals were determined by Equation 3.4. Time duration of one, two and four cycles were tested in these studies. Figure 3.8 depicts the errors in measuring frequencies ranging from 50 to 70 Hz due to the missed high frequency count.

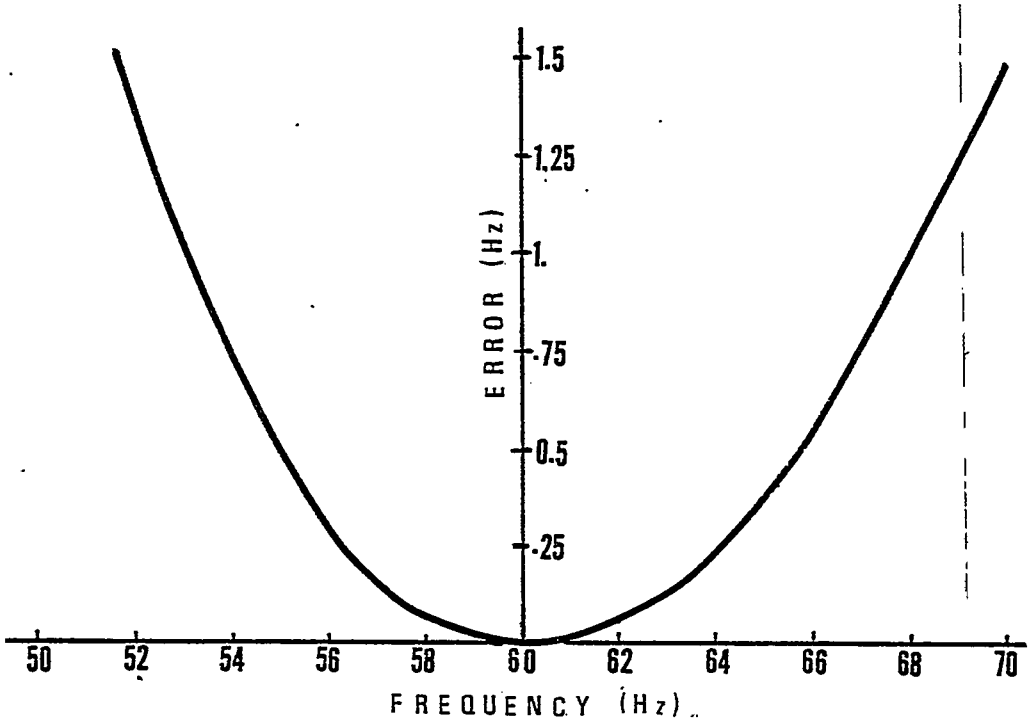

Figure 3.7 Curve represents the error due to the neglected terms of the Taylor series expansion.

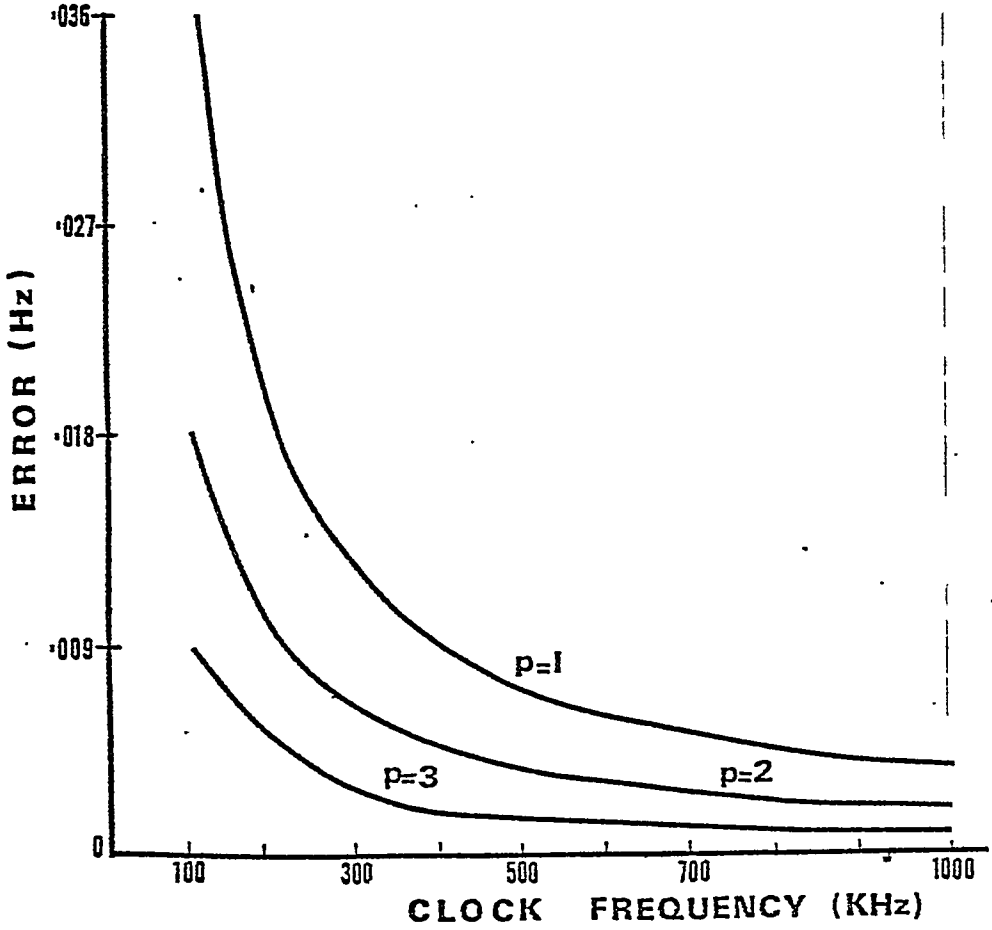

Figure 3.8 The curves represent the errors due to random phasing of pulses during the measurements, for different values of p in the 100 kHz to 1 MHz clock frequency range.

3.5.3 Measuring time for a specified number of periods and estimating the frequency by second order approach

Equations 3.6 and 3.10 use the first three terms of the Taylor series expansion of $\frac{1}{f}$ and f. The use of these equations do not provide true measurements of frequency. The errors are due to neglecting third and higher order terms of the Taylor series. These equations, however, provide measurements which are more accurate than those obtained by using the first order approach of Equation 3.4 . For comparison the errors in measurements obtained by the first

order and second order approaches are plotted in Figure 3.9. This figure indicates that the measurements by the second order approaches are substantially more accurate than those obtained by the first order approach. A ten percent deviation of frequency causes less than 0.1% error in the frequency estimated by the second order approach.

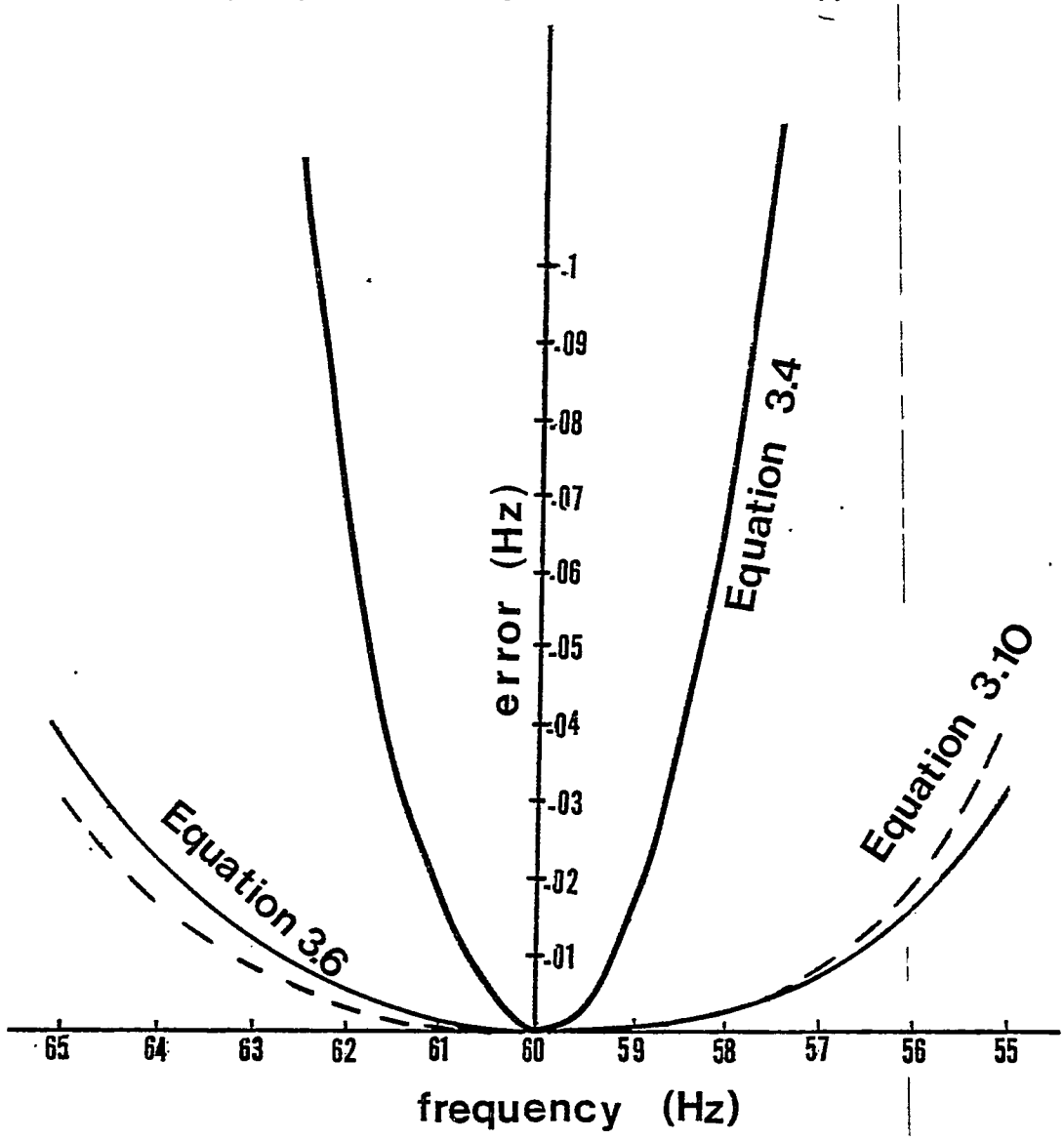

Figure 3.9 Error in the frequency calculated by the first and second order equations derived from Taylor series expansion.

In addition to the error due to the neglected terms of the Taylor series, some error is also caused by the random phasing of high frequency pulses and the commencement of a cycle of the signal. Figure 3.10 represents this additional error when Equation 3.6 is used to estimate frequency. This information was obtained by simulating the frequency measurements in a software program.

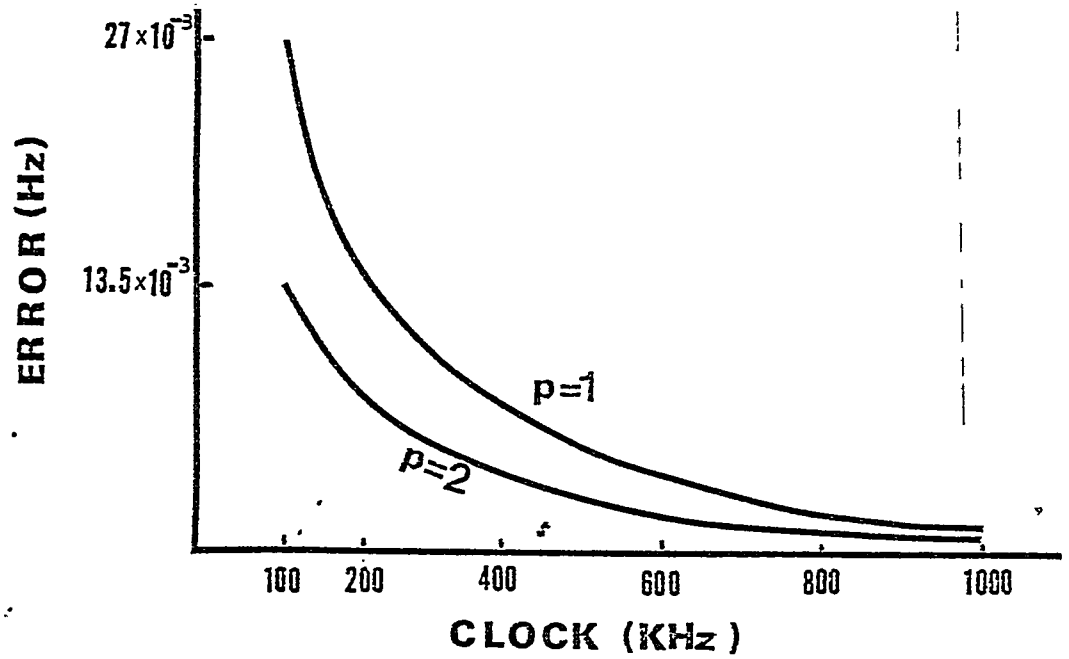

Figure 3.10 The curves represent the error due to random phasing of pulses during the measurements, for different values of p in the 100 kHz to 1 MHz clock frequency range.

These errors are insignificant as compared to the errors depicted in Figure 3.8. The error of ±1 count causes the measured frequency to be in error by $\pm \frac{fo^2}{pfc}$ when the first order estimation approach is used. A similar error in the high frequency count causes the term inside the square root to be in error by $\pm \frac{4fo}{pfc}$. It is obvious that the count error affects the second order approach to a lesser degree than it affects the first order approach.

Techniques of measuring frequency have been presented in this chapter. The suitability of these approaches for use in relays based on digital devices has been discussed. The accuracy of these methods has also been examined.

4. METHODS OF DETERMINING RATE OF CHANGE OF FREQUENCY

The importance of measuring frequency and rate of change of frequency and using them for saving a power system from collapse have been discussed earlier. Methods of measuring frequency have been presented in Chapter 3. Different methods of determining the rate of change of frequency are discussed in this chapter. The effectiveness of each method is also investigated.

4.1 Classification of Methods

The methods of determining the rate of change of frequency can be classified in two groups as follows:

i) Measuring the time periods of successive cycles of the signal and calculating the rate of change of frequency.

ii) Measuring the time periods of successive cycles of the signal and estimating the rate of change of frequency. These methods use the Taylor series expansion and curve fitting technique to estimate the rate of change of frequency.

4.2 Measuring the Periods of Successive Cycles and Calculating the Rate of Change of Frequency

If the frequency at a power system bus changes from f_1 to f_2 in a small interval of time, Δt, the approximate value of the rate of change of frequency, f^1, may be calculated using Equation 4.1.

$$f^1 = \frac{f_2 - f_1}{\Delta t} \quad \text{Hz/sec} \qquad (4.1)$$

If N_1 and N_2 are the high frequency clock pulses recorded in two consecutive periods of p cycles, Δt may be approximated as $(N_1 + N_2)/2f_c$. As discussed in Chapter 3, f_1 and f_2 are approximately given by $\frac{pf_c}{N_1}$ and $\frac{pf_c}{N_2}$ respectively. Making these substitutions in Equation 4.1, the following equation is obtained.

$$f' = \frac{2pf_c^2.(N_1 - N_2)}{N_1.N_2.(N_1 + N_2)} \quad \text{Hz/sec} \qquad (4.2)$$

This form is not convenient for use in digital relays because it involves multiplications and divisions by variable numbers. To simplify this equation, linearized approximations of f_1 and f_2 may be used from Equation 3.4. Substituting f_1 and f_2 by $f_o^2/pf_c.(2N_o-N_1)$ and $f_o^2/pf_c.(2N_o-N_2)$ in Equation 4.1, the following expression is obtained.

$$f' = \frac{f_o^2}{p} \cdot \frac{(N_1 - N_2)}{(N_1 + N_2)} \quad \text{Hz/sec} \qquad (4.3)$$

This expression is simpler than Equation 4.2 but it still requires that a variable count be divided by another variable count.

4.3 Measuring the Period of Successive Cycles of the Signal and Estimating the Rate of Change of Frequency

The approach discussed in Section 4.2 is not suitable for use in digital relays because divisions by variable numbers are time consuming operations. This problem can be avoided by using a linearized approximation. Three linearized approaches which estimate the rate of change of frequency are presented in this section. These approaches are:

1) First order approximation,

ii) Second order and

iii) Curve fitting approach.

4.3.1 First order approximation

A simple expression for the rate of change of frequency can be obtained by using the Taylor series expansion of Equation 3.3 which is as follows.

$$\frac{1}{f} = \frac{1}{f_o} - \frac{(f - f_o)}{f_o^2} + \frac{(f - f_o)^2}{f_o^3} - \cdots\cdots$$

The frequency f is given by $\frac{pf_c}{N}$. Making this substitution in Equation 3.3 and considering the first two terms of the series, Equation 4.4 is obtained.

$$\frac{N}{pf_c} = \frac{1}{f_o} - \frac{(f - f_o)}{f_o^2} \qquad (4.4)$$

Differentiating both sides of this equation, the following expression is obtained.

$$\frac{1}{pf_c}\frac{dN}{dt} = -\frac{1}{f_o^2}\cdot\frac{df}{dt} \qquad (4.5)$$

This equation provides the following expression for the rate of change of frequency.

$$\frac{df}{dt} = -\frac{f_o^2}{pf_c}\cdot\frac{dN}{dt} \qquad (4.6)$$

In this Equation $\frac{dN}{dt}$ is the rate at which the number of recorded pulses change during the measurements and is approximately given by

$$\frac{dN}{dt} = \frac{N_2 - N_1}{\Delta t} \qquad (4.7)$$

where: N_1 is the number of pulses recorded in the first p cycles,

N_2 is the number of pulses recorded in the next p cycles and

Δt is the time interval between the two successive measurements.

Substituting for $\frac{dN}{dt}$ in Equation 4.6, the following equation is obtained.

$$f' = \frac{df}{dt} = \frac{f_o^2}{pf_c \Delta t} \cdot (N_1 - N_2) \quad \text{Hz/sec} \qquad (4.8)$$

In Equation 4.8, Δt can be approximated as the measurement period at the base frequency $(\frac{1}{f_o})$. $\frac{f_o^2}{pf_c \Delta t}$ is, therefore, a constant; p and f_c can be selected in such a manner that this term is a multiple of two. In this manner, Equation 4.8 does not require any multiplications or divisions except by a factor of 2^n which can be achieved by bit shifts in a digital device.

So far it has been assumed that the rate of change of frequency is obtained from the data of only one phase of a three phase system. In Chapter 3, advantages of measuring frequency from the data of all three phases were discussed. It is also possible to use information from all three phases for measuring the rate of change of frequency. The rate of change of frequency can be measured from the data of each phase separately, then the average of these measurements

can be calculated. This process reduces the inaccuracies caused by noise and gating errors. If f^1 is measured from the time periods of two successive cycles, the three phase approach will take a total time of $2\frac{2}{3}$ cycles as is obvious from Figure 4.1. Achieving a similar averaging effect will require 6 cycles measurement time if data from only one phase is used. The calculation of the rate of change of frequency from three phase data can also be combined in a single equation as follows.

$$\left(\frac{df}{dt}\right)_{av} = \frac{1}{3} \cdot \left(\left(\frac{df}{dt}\right)_A + \left(\frac{df}{dt}\right)_B + \left(\frac{df}{dt}\right)_C\right) \qquad (4.9)$$

The high frequency counts of different phases are identified by subscripts A, B and C. Substituting for the rate of change of frequency of the individual phases from Equation 4.8, the following equation is obtained.

$$\left(\frac{df}{dt}\right)_{av} = \frac{fo^2}{3\ pf_c\ \Delta t}\left((N_{A1}+N_{B1}+N_{C1})-(N_{A2}+N_{B2}+N_{C2})\right) \qquad (4.10)$$

4.3.2 Second order approximation

The first order approximation techniques have been presented in Section 4.3.1. These approaches use only two terms of the Taylor series expansion of $\frac{1}{f}$. A second order approximation can be similarly obtained by using the first three terms of the Taylor series. Taylor series expansion of $\frac{1}{f}$ in the neighborhood of f_o as already given in Equation 3.3 is

$$\frac{1}{f} = \frac{1}{f_o} - \frac{(f - f_o)}{f_o^2} + \frac{(f - f_o)^2}{f_o^3} - \cdots \qquad (4.11)$$

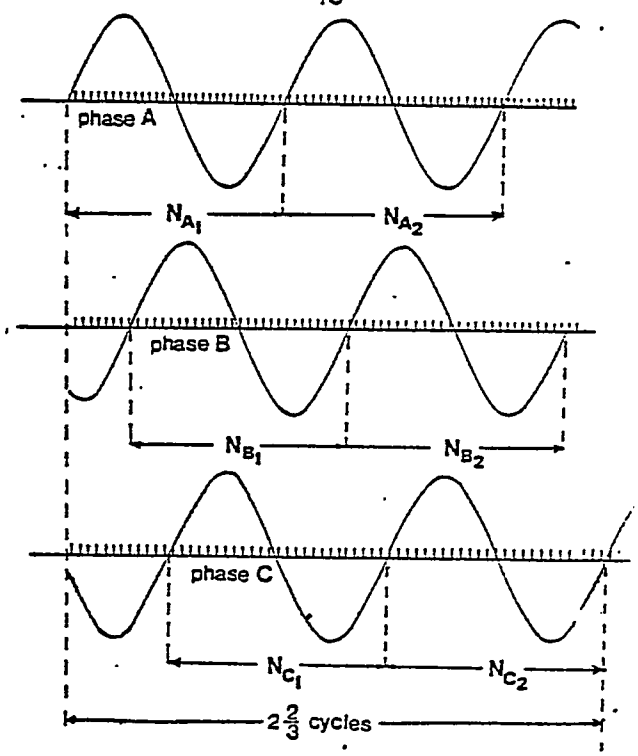

Figure 4.1 Pulses recorded in different phases of a three phase system.

Considering only the first three terms and substituting $f = \frac{pf_c}{N}$ on the left hand side of this expansion, the following equation is obtained.

$$\frac{N}{pf_c} = \frac{1}{f_o} - \frac{(f - f_o)}{f_o^2} + \frac{(f - f_o)^2}{f_o^3} \qquad (4.12)$$

Differentiating both sides of this equation with respect to t, provides the following equation.

$$\frac{1}{pf_c}\frac{dN}{dt} = -\frac{df}{dt}\cdot\frac{1}{f_o^2} + \frac{2f}{f_o^3}\frac{df}{dt} - \frac{2f_o}{f_o^3}\frac{df}{dt} \qquad (4.13)$$

Solving for $\frac{df}{dt}$ from Equation 4.13, provides the following expression for the rate of change of frequency.

$$\frac{df}{dt} = \frac{f_o^3}{pf_c}\cdot\frac{dN/dt}{(2f-3f_o)} \qquad (4.14)$$

Equation 4.15 is obtained by substituting $\frac{dN}{dt}$ with $\frac{(N_2 - N_1)}{\Delta t}$ in the above equation. Δt can be approximated as the measurement period at the base frequency, $\frac{1}{f_o}$.

$$\frac{df}{dt} = \frac{f_o^4}{pf_c} \cdot \frac{(N_2 - N_1)}{(2f - 3f_o)} \quad \text{Hz/sec} \qquad (4.15)$$

This equation is not computationally acceptable because it involves a division of a variable by another variable.

Another possible approach is to use the Taylor series expansion of function $f = \frac{pfc}{N}$ in the neighborhood of N_o. This expansion can be written as follows.

$$f = \frac{pfc}{N_o} - \frac{pfc}{N_o^2} (N-N_o) + \frac{2pfc}{N_o^3} \frac{(N-N_o)^2}{2!} - \cdots \qquad (4.16)$$

Considering the first three terms of this series and differentiating both sides with respect to time, Equation 4.17 is obtained.

$$\frac{df}{dt} = - \frac{3f_o^2}{pf_c} \cdot \frac{dN}{dt} + \frac{2f_o^3}{p^2 f_c^2} \cdot N_2 \cdot \frac{dN}{dt} \qquad (4.17)$$

Substituting $\frac{dN}{dt}$ with $\frac{N_2 - N_1}{\Delta t}$ in Equation 4.17, the following equation is obtained.

$$\frac{df}{dt} = - \frac{3f_o^2}{pf_c.\Delta t} \cdot (N_2 - N_1) + \frac{2f_o^3}{p^2.f_c^2.\Delta t} \cdot N_2.(N_2 - N_1) \qquad (4.18)$$

In Equation 4.18, Δt can be approximated as the time period of the base frequency, $\frac{1}{fo}$. $\frac{3f_o^2}{pf_c\Delta t}$ and $\frac{2f_o^3}{p^2 f_c^2 .\Delta t}$ are, therefore constants; p and f_c can be selected in such a manner that one of these terms is multiples of two. In this form, Equation 4.18 is simpler than Equation 4.15.

4.3.3 Curve fitting approach

The measurements of frequency are subject to variations due to the presence of noise. Frequency and rate of change of frequency measurements can, therefore, be improved by an averaging procedure. Consider that the frequency of a signal has been measured at four regular intervals as shown in Figure 4.2. Assuming that the frequency is changing at a uniform rate, it may be expressed as a function of time as follows.

$$f = a + bt \tag{4.19}$$

The values of the coefficients a and b can be obtained by using the least error squares approach. The coefficient a is the frequency and the slope b is the rate of change of frequency. If four measurements are used and the measurements are assumed to have been obtained at equal intervals of time, the frequency and the rate of change of frequency are given by

$$f = a = \frac{-2f_1 + f_2 + 4f_3 + 7f_4}{10} \tag{4.20}$$

$$f' = b = \frac{-3f_1 - f_2 + f_3 + 3f_4}{10.\Delta t} \tag{4.21}$$

In this equation, Δt represents the time interval between successive frequency measurement.

Substituting $f = \frac{f_o^2}{pf_c}(2No-N)$ from Equation 3.5 into Equation 4.20. and 4.21, the frequency and the rate of change of frequency are given by Equations 4.22 and 4.23.

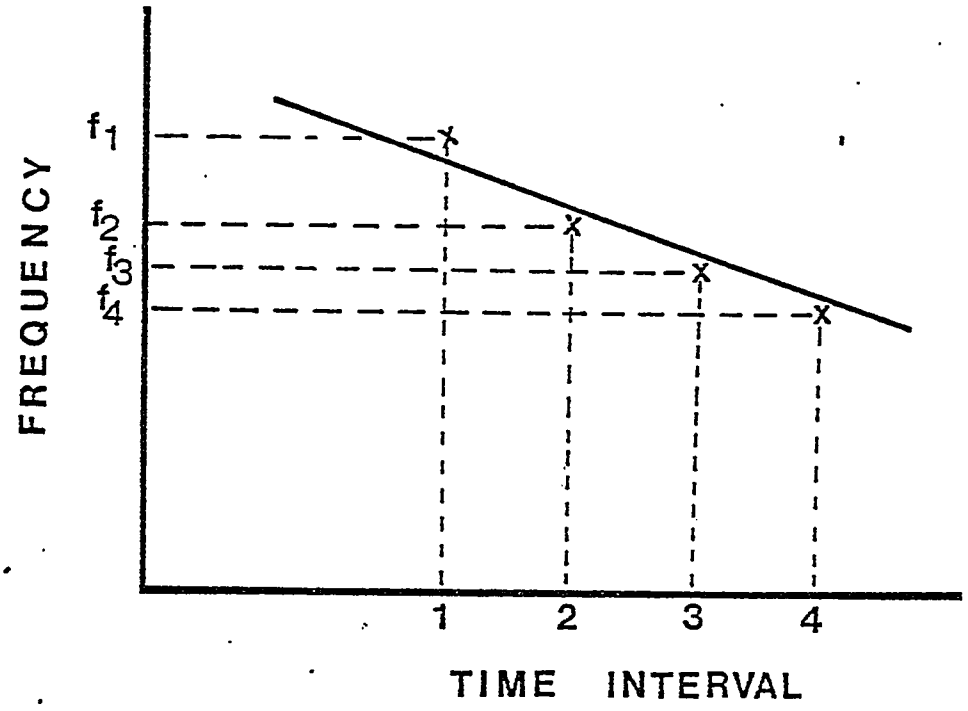

Figure 4.2 Curve fitting using four samples.

$$f = a = \frac{f_o^2}{10pfc}\,(2N_1 - N_2 - 4N_3 - 7N_4 + 20N_o) \qquad (4.22)$$

$$f' = \frac{fo^2}{10\ \Delta t\ pfc}\,(3N_1 + N_2 - N_3 - 3N_4) \qquad (4.23)$$

If 5 successive samples are used, the frequency and the rate of change of frequency are given by Equations 4.24 and 4.25

$$f = a = \frac{f_o^2}{5\ pf_c}\,(N_1 - N_3 - 2N_4 - 3N_5 + 10N_o) \qquad (4.24)$$

$$f^1 = \frac{f_o^2}{10.\Delta t.pf_c}\,(2N_1 + N_2 - N_4 - 2N_5) \qquad (4.25)$$

Assuming that Δt is approximately equal to the measurement time at nominal frequency, $\frac{f_o^2}{10.\Delta t.pf_c}$ becomes a constant. The value of p and f_c can be chosen such that the factor $\frac{f_o^2}{10.pf_c\ \Delta t}$ is a multiple

of two. In this manner, both Equations 4.23 and 4.25 require additions, subtractions and a division by multiples of two(which can be performed by bit shifts in the computer). These operations are computationally convenient and, therefore, Equations 4.23 to 4.25 can be used to measure frequency and rate of change of frequency.

4.4 Off-Line Testing

To determine their effectiveness, the techniques described in the preceeding sections were tested off-line. The measurements of the rate of change of frequency were simulated in software programs. Test procedures and results for each technique are presented in this section.

4.4.1 Measuring time periods of successive cycles of the signal and calculating the rate of change of frequency

This method uses Equations 4.2 and 4.3 to determine the rate of change of frequency. To test this approach, a 60 Hz signal decreasing at 2 Hz/sec was simulated in a software program. Measurement periods of 1, 2, 3 and 4 cycles and clock frequencies of 144, 288 and 360 kHz were used. The calculations were continued for three seconds. The minimum and maximum values of the observed rate of change of frequency are given in Table 4.1 and 4.2 respectively. As expected, the calculated rate of change of frequency is less accurate when Equation 4.3 is used. The use of this equation, however, requires less computation time compared to the time required when Equation 4.2 is used. These results also indicate that the accuracy of the measurements improves as the clock frequency and the duration of measurement are increased.

Table 4.1 Maximum and Minimum Values of the Rate of Change of Frequency Calculated by Equation 4.2 for an Input Signal Changing at 2 Hz/sec.

fc	144 kHz		288 kHz		360 kHz	
	Min.	Max.	Min.	Max.	Min.	Max.
p = 1	0	3.81	1.26	2.98	1.09	2.89
p = 2	1.45	2.55	1.74	2.29	1.78	2.24
p = 3	1.87	2.12	1.93	2.08	1.93	2.06
p = 4	1.93	2.06	1.96	2.02	1.97	2.02

Table 4.2 Maximum and Minimum Values of the Rate of Change of Frequency Calculated by Equation 4.3 for an Input Signal Changing at 2 Hz/sec.

fc	144 kHz		288 kHz		360 kHz	
	Min.	Max.	Min.	Max.	Min.	Max.
p = 1	0	4.25	1.41	2.99	1.16	2.96
p = 2	1.48	2.97	1.83	2.83	1.87	2.7
p = 3	1.76	2.96	1.95	2.93	1.98	2.7
p = 4	1.93	2.96	1.96	2.81	1.96	2.62

4.4.2 First Order Approximation

The first order approach, which uses Equation 4.8 to calculate the rate of change of frequency, was also tested by computer simulations. As in the last section, a 60 Hz signal decreasing at 2 Hz/sec was simulated and the rate of change of frequency was calculated. The maximum and minimum calculated values are given in Table 4.3. As expected, the measurements obtained by this approach are less accurate than those obtained by using Equations 4.2 and 4.3. The computation effort was, however, considerably smaller.

Table 4.3 Maximum and Minimum Values of the Rate of Change of Frequency Calculated by Equation 4.8 for an Input Signal Changing at 2 Hz/sec.

fc	144 kHz		288 kHz		360 kHz	
	Min.	Max.	Min.	Max.	Min.	Max.
p = 1	0	4.3	1.32	3.37	1.18	3.57
p = 2	1.48	3.12	1.83	3.02	1.86	3.02
p = 3	1.81	2.92	1.97	2.93	1.96	2.86
p = 4	1.93	2.9	1.96	2.86	1.96	2.86

This method was also tested by simulating the rate of change of frequency measurements of three phase voltages by using Equation 4.10. Three balanced 60 Hz signals each displaced by 120 degrees with respect to the other two signals decreasing at 2 Hz/sec were simulated. Measurement periods of one cycle (p=1) and clock frequencies of 144,288 and 360 kHz were used. The rate of change of frequency were calculated for 180

cycles of the input signals. Table 4.4 depicts the maximum and minimum values of the rate of change of frequency observed during this test. A comparison of Tables 4.3 and 4.4 shows that the use of information from all three phases considerably improves the accuracy of measurements.

Table 4.4 Maximum and Minimum Values of the Rate of Change of Frequency Measured Using the Information from all Three Phases.

fc (kHz)	144		288		360	
	Min.	Max.	Min.	Max.	Min.	Max.
p = 1	1.3	3.9	1.5	2.9	1.6	2.9

4.4.3 Second order approximation

This approach uses Equations 4.15 and 4.18 to determine the rate of change of frequency. In this test, a signal starting at 60 Hz and decreasing at 2 Hz/ sec was simultated in a software program as in the previous sections. Measurement periods of one, two, three and four cycles and clock frequencies of 144, 288 and 360 kHz were used. As in other tests, the measurements were continued for 180 cycles of the input signal. Minimum and maximum values of the rate of change of frequency calculated during this test are given in Tables 4.5 and 4.6. A comparison of the measurements given in Tables 4.5 and 4.6 and the results given in the previous sections shows that the accuracy of the second order method is better than the previous

approach. The accuracies of the measurements by Equations 4.15 and 4.18 are similar; Equation 4.18 is, however, much simpler and straight forward to use in a digital relay.

Table 4.5 The Maximum and Minimum Values of the Rate of Change of Frequency Calculated by Equation 4.15 for an Input Signal Changing at 2 Hz/sec.

fc	144 kHz		288 kHz		360 kHz	
	Min.	Max.	Min.	Max.	Min.	Max.
p = 1	0	4.13	1.215	3.3	1.13	2.93
p = 2	1.35	2.94	1.46	2.73	1.7	2.34
p = 3	1.48	2.7	1.8	2.42	1.79	2.37
p = 4	1.7	2.43	1.82	2.29	1.87	2.3

Table 4.6 The Maximum and Minimum Values of the Rate of Change of Frequency Calculated by Equation 4.18 for an Input Signal Changing at 2 Hz/sec.

fc	144 kHz		288 kHz		360 kHz	
	Min.	Max.	Min.	Max.	Min.	Max.
p = 1	0	4.08	1.1	3.24	1.12	2.93
p = 2	1.33	1.94	1.45	2.68	1.69	2.34
p = 3	1.48	2.67	1.77	2.42	1.79	2.34
p = 4	1.7	2.4	1.81	2.28	1.87	2.26

4.4.4 Curve fitting approach

The effectiveness of the curve fitting approach, which is explained in Section 4.3.3, was also tested. Signals starting at 60 Hz and decreasing at rates ranging from 0.2 Hz/sec to 4 Hz/sec were simulated. The rates of change of frequency were calculated using a clock frequency of 360 kHz and the Equations 4.23 and 4.25. The maximum errors observed are summarized in Table 4.7. A perusal of this table and a comparison of the results reported in the previous sections reveal that:

i) The accuracy of the curve fitting approach is much better than the first and second order approximations. This can be observed when the comparisons are made at 2 Hz/sec for 360 kHz clock frequency.

ii) The accuracy of the five samples approach is better than the accuracy of the four samples approach.

Table 4.7 Maximum Error in the Rate of Change of Frequency Calculated by the Curve Fitting Approach

Rate of change of frequency (Hz/sec.)	Maximum error in the rate change of frequency calculated from n samples	
	n = 4	n = 5
0.2	0.218	0.099
0.4	0.225	0.135
1	0.43	0.14
1.4	0.225	0.118
2	0.178	0.15
4	0.201	0.103

Different approaches for determining the rate of change of frequency have been discussed in this chapter. The effectiveness of these methods has been tested by off-line simulations and the test results have been presented. The advantages of using the three phase approach and curve fitting technique have also been proved.

5. DESCRIPTION AND ON-LINE TESTING OF THE DIGITAL RELAY

Methods for determining frequency and its rate of change have been described in Chapters 3 and 4. The effectiveness of those methods and their suitability for use in software programs have also been examined. Advantages of the three phase approach have been outlined. Out of all the approaches discussed in Chapters 3 and 4, first order approach to determine frequency and curve fitting techniques for determining the rate of change of frequency were selected and used in a software based digital frequency cum rate of change of frequency relay.

Essential details of the hardware and software of the proposed relay are described in this chapter. The relay was tested; the test results are also presented in this chapter.

5.1 Hardware Description of the Relay

The hardware of the proposed digital relay consists of a counter circuit, an interprocessor buffer and a digital computer. This equipment is arranged as shown in the block diagram of Figure 5.1. The counter circuit counts the number of high frequency pulses in prespecified periods of the input signal. The count is then transferred to the computer via the interprocessor buffer. A computer program processes the incoming data and decides if load shedding is necessary or not. Essential details of the hardware are briefly described in this section.

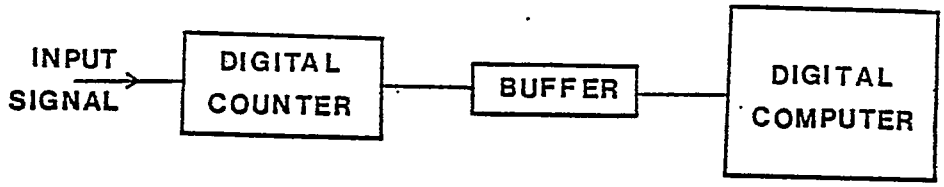

Figure 5.1 The conceptual arrangement of the digital counter and a digital computer

5.1.1 Counter circuit

This circuit counts the high frequency pulses between zero crossings of the input signal. At the end of each cycle, the count is transferred to the accumulator of the computer with the aid of an interprocessor buffer. This approach relieves the computer from the task of counting pulses.

A block diagram of the counter circuit is given in Figure 5.2. The incoming signal is applied to a detector which generates a pulse at every zero crossing of the input signal. Multiple zero crossings can occur due to noise in the vicinity of the zero crossings. This process adversely affects the measurement of frequency and its rate of change. To avoid this problem, a monostable multivibrator with a pulse width of 1 msec has been included at the output of the zero crossing detector. The output of the multivibrator is applied to a bi-stable multivibrator which produces square wave pulses at half the input frequency. The output of the bi-stable multivibrator (Q) and its complement $\overline{Q}$, are applied to separate AND gates. Output from a high frequency clock is also applied to these AND gates. The outputs of the AND gates are applied to seperate 12-bit counters which count the high frequency pulses in alternate cycles. At the end of each cycle, the count is transferred to the computer via the interprocessor

buffer. Two groups of four multivibrators are provided in this circuit. One group operates in conjunction with Counter I, the other group functions with Counter II. The purpose of each multivibrator is as follows.

A monostable multivibrator, MSMV I, is used to transfer the content of the Counter I to Register I at the end of each cycle. This is done by applying the output (L_1) of the MSMV I to the Register I. Similarly the output (L_1') of MSMV V is used to transfer the output of Counter II to the Register II. $\overline{L}_2$, the complement output of the multivibrator, MSMV II, produces a pulse to set the buffer flag, as soon as the information in Register I is ready to be transferred to the accumulator of the computer. The complementary output of the MSMV VI ($\overline{L}_2'$) sets the buffer flag as soon as the information in Register II is ready to be transferred. The outputs of the multivibrators MSMV III and MSMV VII, L_3 and L_3' clear the outputs of the Counters I and II respectively, after the information is transferred from the counters to registers. The outputs of MSMV IV and MSMV VIII, L_4 and L_4', clear the outputs of Register I and Register II respectively, after the information in these registers have been provided to the computer. The voltage waveforms associated with this circuit are shown in Figure 5.3 A detailed schematic diagram of the counter circuit is given in Appendix II.

5.1.2 Interprocessor buffer

The interprocessor buffer (DB8-E) assists in the transfer of information from the user designed circuit to the PDP-8/E computer. In this project,the interprocessor buffer was used to transfer the output of the counter circuit to the accumulator of the computer. A maximum of 12-bits can be transferred at one time; the maximum

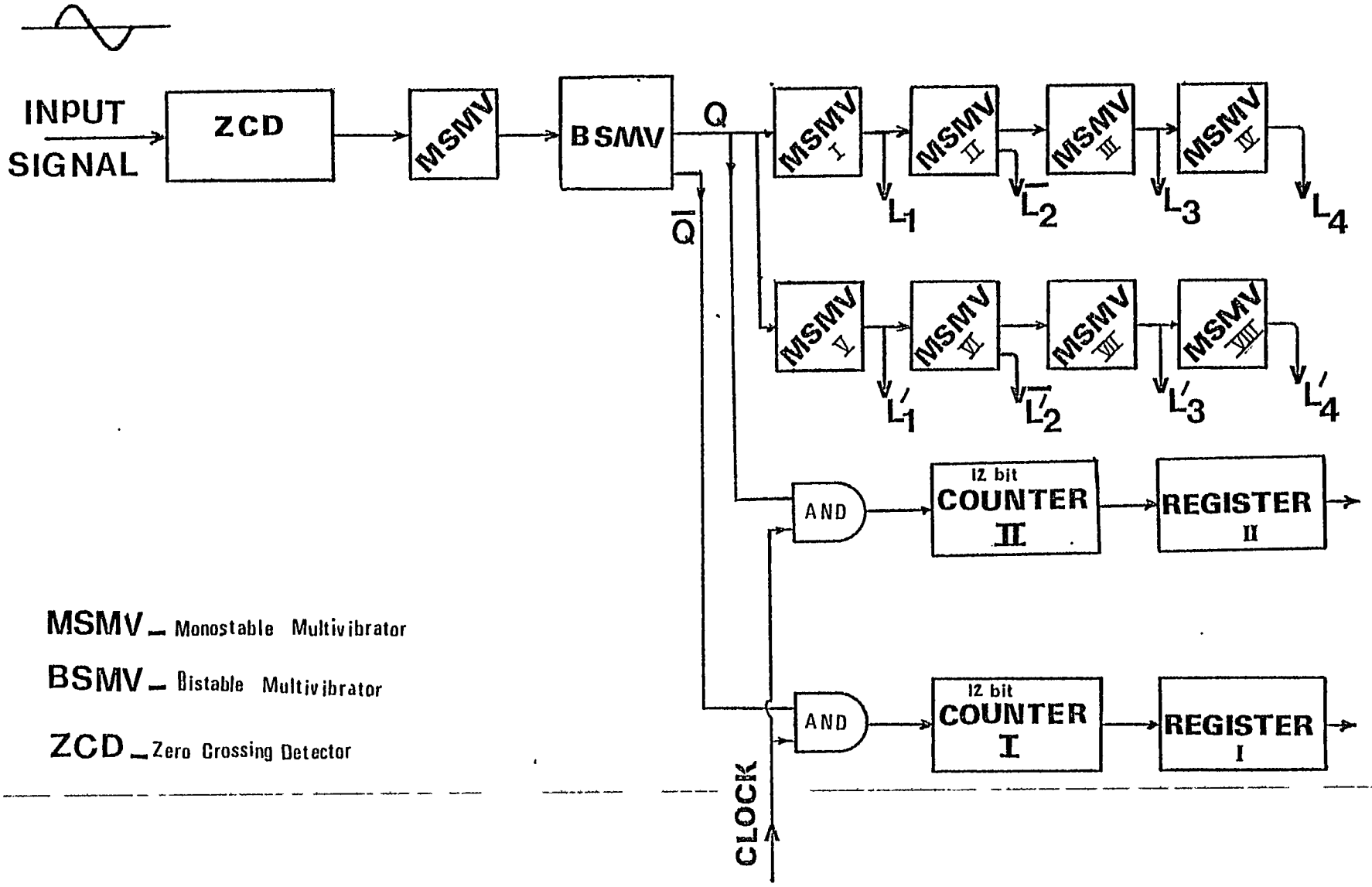

Figure 5.2 Logic block diagram of the counter circuit.

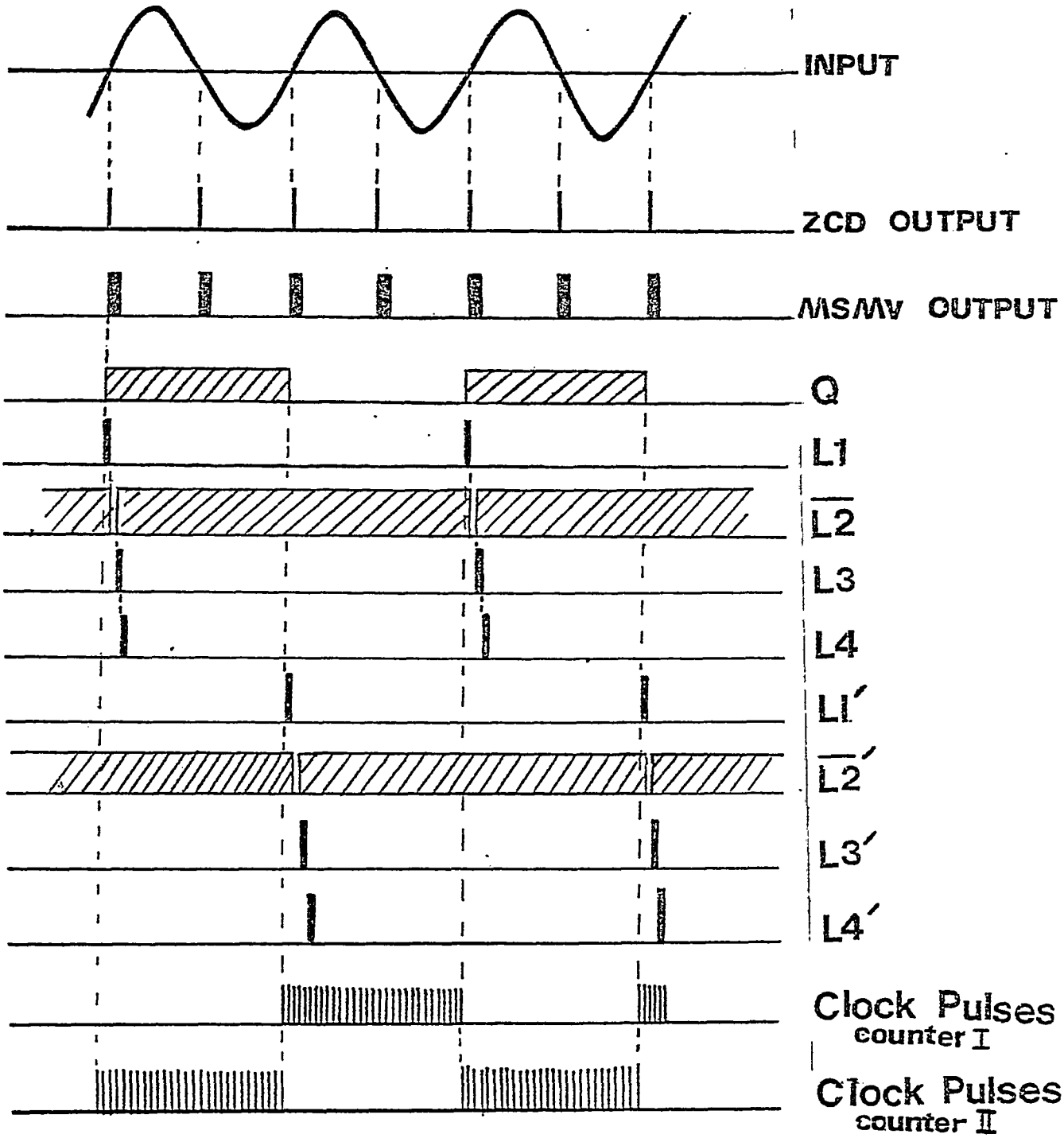

Figure 5.3 Voltage waveforms of the counter circuit.

transfer rate is 60 k bits/sec. It is also possible to transfer information from the accumulator of the computer to an outside circuit with the aid of the output buffers. A block diagram showing the transfer of information between the computer and the user circuits is given in Figure 5.4

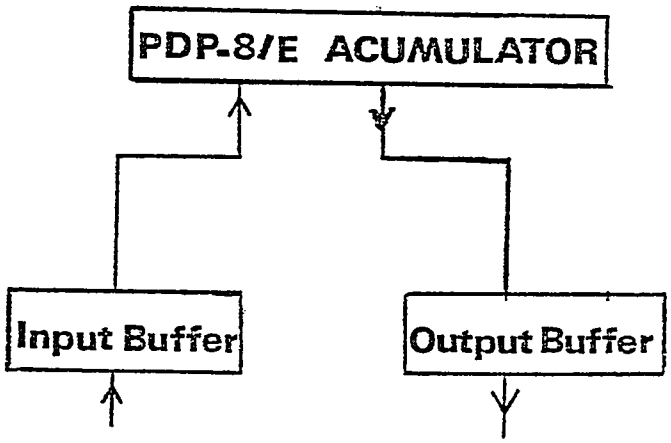

Figure 5.4 Block diagram showing the transfer of information between the computer and outside circuit.

5.1.3 Digital computer

On receipt of information from the counter circuit, the digital computer calculates the frequency and its rate of change, then initiates the corrective action if necessary. A PDP-8/E digital computer was used in this work. Some of the salient features of this computer are given in this section.

The PDP-8/E is a single address, fixed word length, parallel transfer, programmable general purpose digital computer. It uses 2's complement arithmetic and has a word length of 12-bits. Its cycle time is 1.2 μ seconds;an addition requires 2.6 μ seconds while a subtraction takes 5 μ seconds. Multiplication is usually

performed in 25.6 μ seconds or less by a subroutine that operates on two signed 12 bit numbers to produce a 24 bit product, leaving the most significant bits in the accumulator. A division of two signed 12 bit numbers is performed in 342 μ seconds. The use of the KE8-E Extended Arithmetic Element enables the central processor to perform multiplications and divisions at considerably high speeds; the cpu time for these operations is approximately 40 μ seconds. The basic memory of the computer is 4096 words which can be extended up to 32k. The processor has, among others, features of indirect addressing, skipping and program interrupts which can be performed by instructions provided by the I/O devices.

5.2 Testing the Counter Circuit

After designing the counter circuit described in Section 5.1, it was fabricated and tested. A sinusoidal signal of known frequency, 60 Hz, was applied to the counter circuit as shown in Figure 5.5. The count accumulated in the counter at the end of each cycle of the input signal was transferred to the computer via the interprocessor buffer. The software program which resided in the computer, stored the incoming data for one hundred successive cycles. The frequency of the input signal was calculated by the software and was also measured by a digital frequency meter. The readings of the frequency meter were compared with those calculated by the computer. The procedure was repeated with the clock frequencies ranging from 100 to 500 kHz. The results of this test given in Table 5.1 indicate that the counter circuit operated satisfactorily.

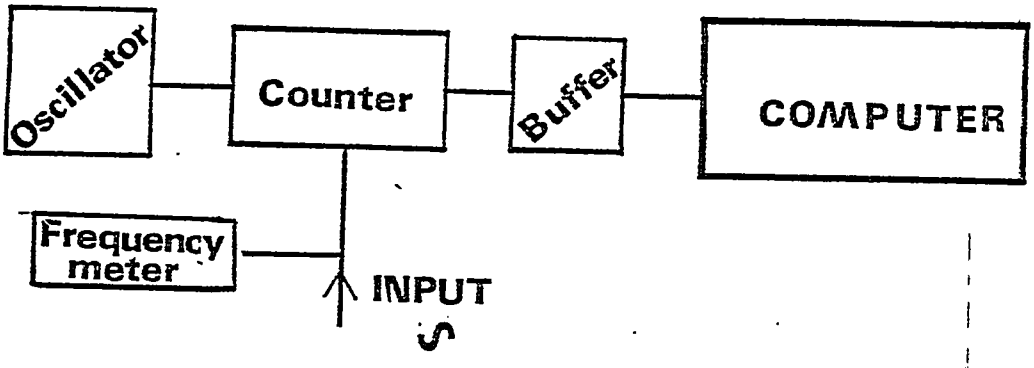

Figure 5.5 Equipment configuration for testing the counter.

Table 5.1 Results of Testing the Counter by Measuring 60 Hz Frequency of a Signal Using Different Clock Frequencies.

Clock frequency (KHz)	Actual number of clock pulses at 60 Hz	Number of pulses recorded by the counter at 60 Hz	Calculated frequency
100	1666.66	1666 or 1667	60.02 or 59.988
200	3333.33	3333 or 3334	60.006 or 59.988
400	6666.66	6666 or 6667	60.006 or 59.997
500	8333.33	8333 or 8334	60.002 or 59.995

5.3 On-Line Measurements of the Rate of Change of Frequency

Before testing the performance of the proposed digital frequency relay, accuracy of the rate of change of frequency measurements was checked. A circuit was first set up for generating sinusoidal signal changing at specified rates of change of frequency. The rate of change of frequency was then measured. The method of generating the signal and the rate of change of frequency measurement tests are described in this section.

5.3.1 Simulation of the rate of change of frequency

Dynamic changes of frequency were simulated by using two voltage controlled oscillators in tandem as shown in Figure 5.6. The first voltage controlled oscillator (VCO) was adjusted to provide an output similar to a ramp. This output voltage was applied to the input of the second VCO which was adjusted to provide a sinusoidal

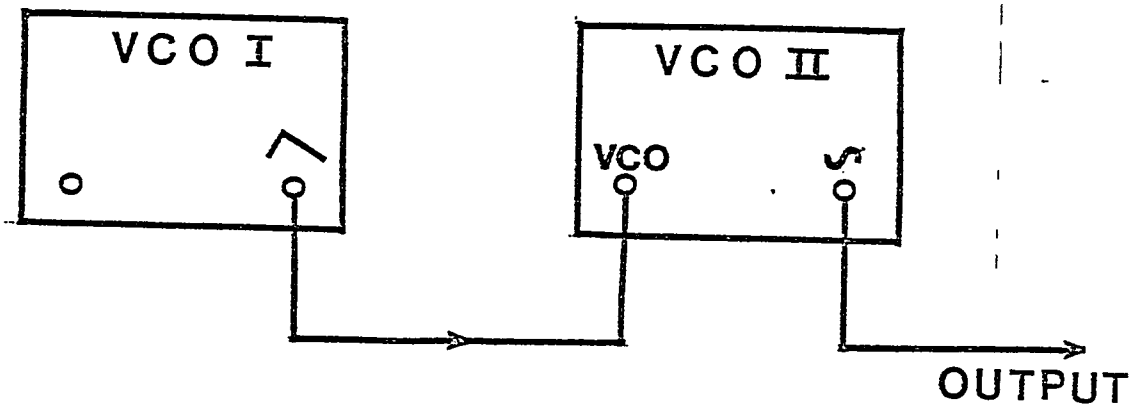

Figure 5.6 Equipment configuration for the simulation of rate of change of frequency.

output. In this manner, the frequency of the output of the second oscillator changes at a rate which depends on the slope of the input ramp voltage. An increase of the slope of the ramp increases the rate of change of the frequency of the sinusoidal output. A relationship between the input ramp voltage and the rate of change of frequency of the sinusoidal output was first established. A small DC voltage was first applied as input to the second VCO and the frequency of the output was measured. This procedure was repeated many times and it was found that a 0.1V change of the input voltage causes the frequency of the output to change by 4.78 Hz. This relationship

was used to select the characteristics of the ramp for generating sinusoidal voltages whose frequency would change at desired rates.

5.3.2 On-line determination of the rate of change of frequency by the second order approximation technique.

A sinusoidal voltage of 60 Hz initial frequency and decaying at pre-selected rates was generated as explained in the last section. This voltage was applied to the counter circuit which was set to use 100 kHz clock pulses. The output of the counter was provided to the PDP-8/E computer via the interprocessor buffer. The computer calculated the rate of change of frequency of the signal using the software program. This program uses Equation 4.15 and measurement durations of four cycles for calculating the rate of change of frequency. The measurements were repeated for seven different rates of change of frequency for about 180 cycles of the input signal in each case. The maximum and mininum values of the rate of change of frequency calculated for each case are given in Table 5.2. These experiments were repeated using 1 MHz clock frequency. The maximum and minimum values of the rate of change of frequency calculated in this case are given in Table 5.3. A comparison of Tables 5.2 and 5.3 indicates that the use of 1 MHz clock frequency considerably improves the accuracy of the measurements of the rate of change of frequency.

5.3.3 On-line determination of the rate of change of frequency by the curve fitting approach.

Another version of the software program, which uses

Table 5.2 The Maximum and Minimum Values of the Rate of Change of Frequency Determined by the Second Order Approximation Technique using a Clock Frequency of 100 kHz.

Rate of change of frequency	Maximum and Minimum values calculated when p=4	
(Hz/sec)	MIN.	MAX.
0.42	0	0.5
0.67	0.5	0.99
0.96	0.5	0.99
1.72	0.99	1.5
2.4	1.93	2.57
3.35	3.2	3.7
4.79	4.2	4.68

Table 5.3 The Maximum and Minumum Values of the Rate of Change of Frequency Determined by the Second Order Approximation Technique using a Clock Frequency of 1 MHz.

Rate of change of frequency	Maximum and Minimum values calculated when p=4	
(Hz/sec)	MIN.	MAX.
0.48	0.33	0.63
0.62	0.48	0.8
0.96	0.74	1.16
1.92	1.82	2
2.87	2.77	3.03
3.83	3.73	3.96
4.79	4.73	4.98

Equation 4.25 for calculating the rate of change of frequency was also prepared and tested. The tests are similar to those explained in Section 5.3.2. The results of these tests are given in Tables 5.4 and 5.5. A study of these tables reveals that the accuracy of the rate of change of frequency measurements improves somewhat when the clock frequency is increased from 100 kHz to 1 MHz.

Table 5.4 The Maximum and Minimum Values of the Rate of Change of Frequency Determined by the Curve Fitting Approach using a Clock Frequency of 100 kHz.

Rate of change of frequency	Maximum and Minimum values calculated using a clock frequency=100 kHz	
Hz/sec.	MIN.	MAX.
0.42	0.36	0.53
0.67	0.56	0.82
0.96	0.68	1.1
1.72	1.53	1.73
2.4	2.05	2.5
3.35	3.1	3.33
4.79	4.54	4.91

A comparison of the results given in this and the previous section shows that the curve fitting approach is slightly more accurate than the second order approximation when a clock frequency of 1 MHz is used. The curve fitting approach is, however, considerably more accurate than the second order technique when a clock frequency of 100 kHz is used. The measurements have an error of 16% when the rate of change of frequency is more than 1 Hz/sec.

Table 5.5 The Maximum and Minimum Values of the Rate of Change of Frequency Determined by the Curve Fitting Approach using a Clock Frequency of 1 MHz.

Rate of change of frequency	Maximum and Minimum values calculated using a clock frequency =1 MHz	
	MIN.	MAX.
0.48	0.41	0.56
0.62	0.54	0.73
0.96	0.83	1.06
1.92	1.83	2
2.87	2.84	2.95
3.83	3.78	3.93
4.79	4.75	4.95

For smaller values of the rate of change, the errors are up to 25%.

5.4 Software Program

The counting circuit described in the preceeding sections counts the high frequency pulses in every p cycles of the input signal, say, a system voltage and places the count in the interprocessor buffer. This information is then received by the computer and is processed using a software program. This program calculates the frequency and the rate of change of frequency and includes the logic for a frequency cum rate of change of frequency relay. The state of the power system is examined by the program and in case of abnormality, suitable action is initiated.

A continuous response trip characteristic as shown in

Figure 5.7 was chosen for the proposed protection scheme. This characteristic has been represented in the program by the following equation.

$$F = F_1 - ROCOF.x \qquad (5.1)$$

where: F is the trip initiation frequency;

F_1 is the upper level of the frequency, no load shedding before that;

x is the slope of the characteristic;

ROCOF is the rate of change of frequency.

The choice of F_1, F_2 and X, which determine the trip characteristic, depends on the requirements of each individual system. Basic advantage of using a characteristic of this type is that when frequency declines rapidly during severe disturbances, load shedding is initiated at higher values of frequency. This assists in preventing the frequency from decreasing to dangerously low values. In case of minor disturbances when the frequency decays at a slow rate, the proposed characteristic allows enough time for the governor to respond and restore the system frequency to near normal values before any load shedding is initiated.

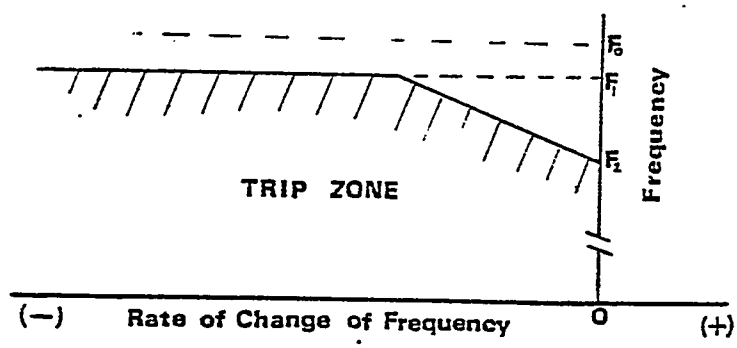

Figure 5.7 Proposed trip characteristic of the underfrequency protection scheme.

The program simulating the relay characteristics uses integer arithmetic to reduce computation time requirements. Some truncations during divisions will, however, cause inaccuracies, when calculating the frequency and its rate of change. The problem was alleviated by multiplying the equations used to calculate these parameters with a large constant (K). In some cases multiplication by a large constant might generate large numbers which will make the programming more complex on the PDP-8/E computer. To overcome this problem, Δf, the deviation of system frequency from its rated value was calculated instead of the frequency. The trip characteristic was, therefore, modified as shown in Figure 5.8.

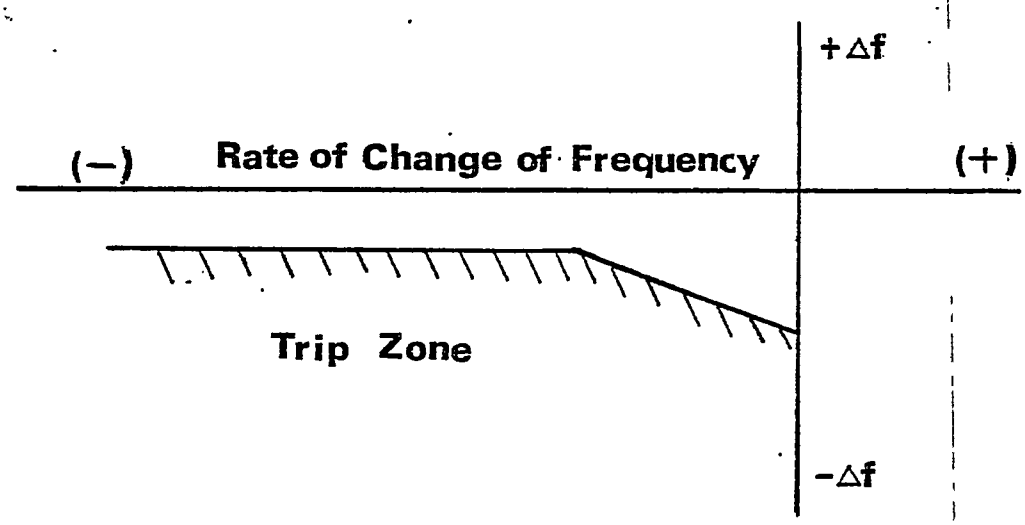

Figure 5.8 Trip characteristic.

The basic logic of the frequency cum rate of change of frequency relay is shown in Figure 5.9. Assume that the program is in a wait mode, waiting for a new value of count to become available. When the count becomes available, the software program checks if its value deviates substantially from the nominal value. If the deviation

is small, the program returns to wait-mode. Should the count not be close to the nominal value, there would be two possibilities. The first possibility is that the system is experiencing a transient disturbance. The second possibility is that the deviation of the high frequency count is caused by an unbalance between the level of generation available in the system and the load it is supplying. If the abnormality lasts a few cycles only, the condition is treated as a transient. Otherwise, the frequency and the rate of change of frequency are calculated and checked against the desired relay characteristic. A load trip logic is initiated if the calculated frequency and rate of change of frequency combination lies in the trip zone.

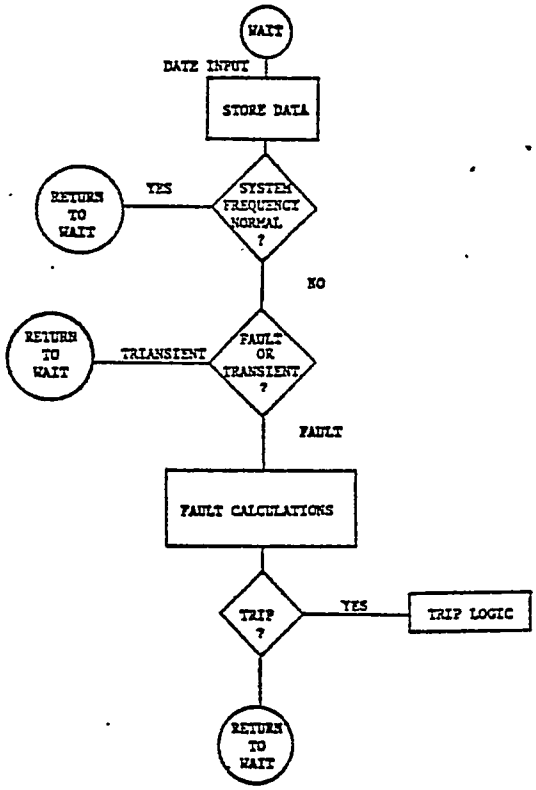

Figure 5.9 A conceptual flowchart of the frequency cum rate of change of frequency relay.

5.5 Testing the Frequency cum Rate of Change of Frequency Relay

The effectiveness of the segments developed for measuring frequency and rate change of frequency were tested; the results of these tests have been previously discussed in this chapter. It has also been demonstrated that the counter circuit, the proposed hardware configuration and the software programs function properly. These segments were combined in an underfrequency-cum-rate of change of frequency relay. The operation of this relay was tested; the tests and their results are described in this section.

The underfrequency protection scheme which responds to both, the frequency and its rate of change was developed in the form of a software program. Details of the software program, such as, logic and trip characteristic have been described in Section 5.4. In the digital relay, Equation 3.5 has been used for determining frequency of the input signal. The rate of change of frequency is determined by using Equation 4.25. The low frequency and rate of change of frequency conditions were simulated as described in Section 5.3. The initial frequency was set at 60 Hz and was regulated to decay at preselected rates. This signal was applied to the counter circuit after initiating the software program.

The software program transferred the data accumulated in the counter to the accumulator of the computer at the end of each cycle of the input signal. On the receipt of data, the computer processed it to determine if any action is warranted. A message was printed on the computer arriving at the conclusion that the load shedding was warranted. The operating frequency and its rate of

change were also printed. The test was repeated six to seven times using five different values of the rate of change of frequency. The values of frequency and its rate of change which deviated most from the relay characteristic are given in Table 5.6. A clock frequency of 115200 Hz and measurement duration of four cycles were used in these studies. The relay characteristic and frequency at which the relay operated in the selected cases of maximum deviations are depicted in Figure 5.10. In this figure a dot represents the frequency and rate of change of frequency at which the relay should have

Table 5.6 Test tesults Showing the Desired Operating Values and Relay Operation.

Preselected values of rate of change of frequency Hz/sec	Desired values of operating frequency (Hz)	Relay operation values with maximum deviation from the desired value (Rate of change of frequency and corresponding frequency)
0.35	58.59	0.69 Hz/s 58.6 Hz
0.96	58.74	1.1 Hz/s 58.68 Hz
2	59	2.2 Hz/s 58.9 Hz
2.87	59.22	2.63 Hz/s 59.1 Hz
3.83	59.46	4 Hz/s 59.37 Hz

operated ideally. Actual parameters at the time of relay operation are represented by x's. A study of Figure 5.10 reveals that the proposed relay adequately performs its intended function.

More details of the software program, a flowchart and listing of the program are given in Appendix III.

Essential details of the hardware and software of the proposed digital underfrequency-cum-rate of change of frequency

relay have been briefly outlined in this chapter. The performance tests, the various segments of the relay tested individually and of the relay in total have been described. The results of the tests have also been presented.

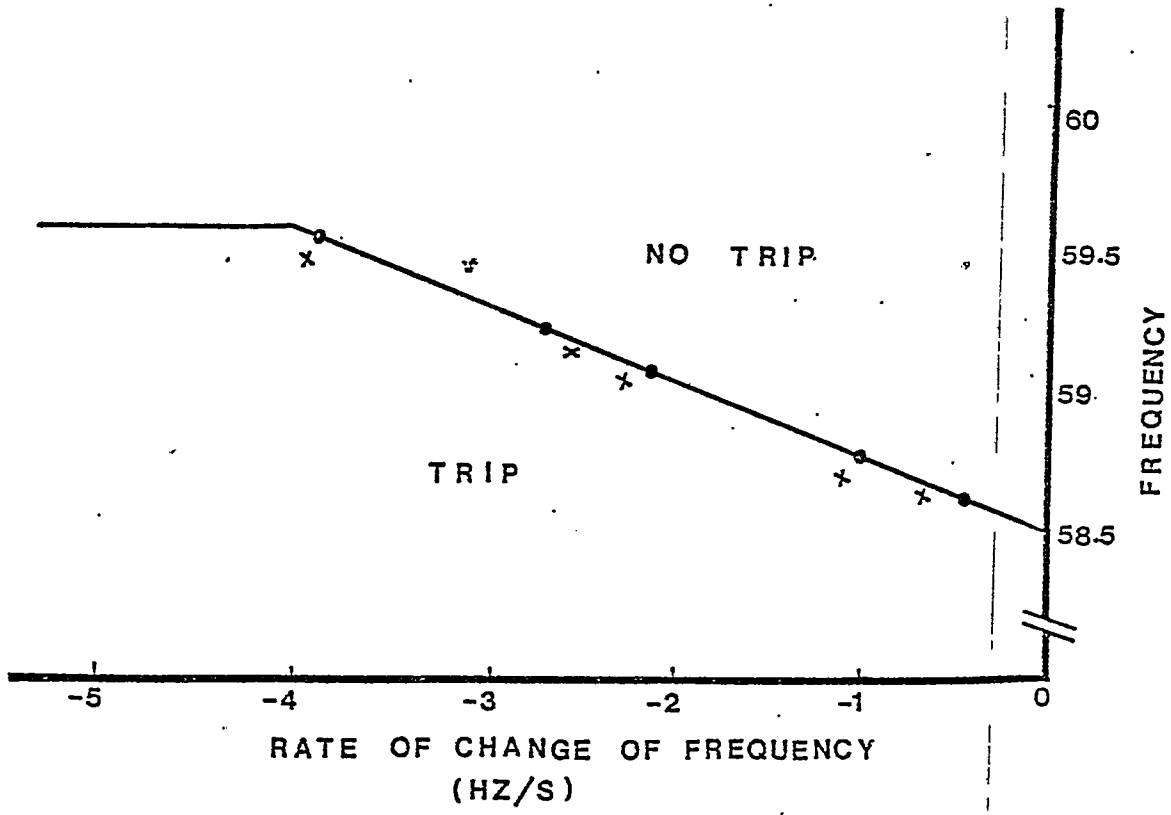

Figure 5.10 Under frequency cum rate of change of frequency relay characteristic and test results.

6. CONCLUSIONS

This thesis presents some techniques of measuring frequency and the rate of change of frequency. The suitability of the use of these techniques in software based frequency relays has also been examined. It has also been demonstrated that an on-line digital computer can be used to determine the system frequency and its rate of change by timing the voltage waveforms. A digital computer was used in this study because a computer program can include considerable logic and flexibility; any form of tripping characteristic can be provided easily. This approach also allows the characteristics to be changed by modifying the input parameters of the software. A multiplicity of actions for load shedding is also possible by this approach.

The general philosophy of protecting power systems has been described in Chapter 2. The hazards of operating a system at sub-normal frequencies and the necessity of frequency relaying have been discussed. The advantages of using relays which respond to a combination of frequency and the rate of change of frequency have been enumerated. The commercially available frequency relays have also been described.

Methods of determining frequency have been examined in Chapter 3. The effectiveness of these methods and their suitability for use in software programs have also been examined. The study has demonstrated that out of all the methods discussed in this chapter, the first order and second order approaches are suitable for using

in software programs because these approaches do not require much computation effort. A three phase approach of measuring frequency has also been introduced. This approach improves the accuracy of measurements when they are required to be computed in short duration of time (1-2 cycles).

The four different approaches of determining the rate of change of frequency have been described in Chapter 4. The accuracy of these approaches was tested and their suitability for use in software programs was examined. Two of these approaches were developed by Taylor series expansion. Out of these two approaches, the first order approximation is quite inaccurate and is, therefore, unsuitable for use in digital relays. The second order approximation has been shown to be more suitable for using in the software; the accuracy of the measurements is considerable but it requires more computation effort than that necessary for using the first order approach. A curve fitting approach is also proposed in Chapter 4. It has also been demonstrated that this approach is suitable for measuring the rate of change of frequency. The possibility of using the three phase approach for determining the rate of change of frequency has also been discussed.

Essential details of the hardware and software of the proposed digital frequency cum rate of change of frequency relay have also been described in Chapter 5. One version of the relay was developed using the methods described in Chapters 3 and 4. In this relay, first order approximation technique is used for measuring frequency and the curve fitting approach is used for measuring the rate of change frequency.

The overall relay operation was tested; the test results are also reported in this chapter. The tests have revealed that the proposed relay operates adequately.

From the studies reported in this thesis,it may be concluded that frequency and the rate of change of frequency can be measured adequately by digital methods using approximation techniques. It can also be concluded that these techniques are suitable for implementing in a software based frequency-cum rate of change of frequency relay.

7. REFERENCES

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8. APPENDICES

APPENDIX I - Effect of the Presence of a D.C. offset on Frequency Measurements

The voltage and current waveforms at a relay location during faults consist of two parts; a steady state component and transients. Transient components include an exponentially decaying D.C. and high frequency components. High frequency components can be blocked from reaching the relay by using low pass filters but the D.C. component can not be filtered out. The effect of the decaying D.C. component on the voltage waveforms was investigated to determine if the frequency measurements would be affected by the presence of this component in the signal provided to the relays. The results of this study are presented in this appendix.

For the system shown in Figure I.1, the current and voltage waveforms at the location P during a fault may be expressed as:

$$i(t) = \frac{V}{Z}.\ \sin(wt + \Theta_f - \Theta) - K_1.e^{-\frac{R}{L}t} + \Sigma\ \text{h.f. component} \qquad (I.1)$$

$$v(t) = Z_L.\frac{V}{Z}\sin\ (wt + \Theta_f + \Theta_L - \Theta) - K_2\ e^{-\frac{R}{L}t} + \Sigma\ \text{h.f. component} \qquad (I.2)$$

where;

$$K_1 = \frac{V}{Z}\ \sin\ (\Theta_f - \Theta),$$

$$K_2 = \frac{V}{Z}.Z_L\ \sin\ \frac{(\Theta - \Theta_L).\ \sin\ (\Theta_f - \Theta)}{\sin\ \Theta},$$

$$\Theta_L = \tan^{-1}\ \frac{X_L}{R_L},$$

$$\Theta\ = \tan^{-1}\ \frac{X}{R},$$

Θ_f is the angle which determines the magnitude of the voltage at the instant of the fault,

Z_s is the total impedance on the sourse side of the relay and is equal to $R_s + jwL_s$

Z_L is the impedance from the relay location to the fault and is equal to $R_L + jwL_L$.

Z is the total impedance from the source to the fault and is equal to $Z_s + Z_L = R + jX$.

This system also represents one phase of a three phase system experiencing a three phase fault. Now consider the two machine system

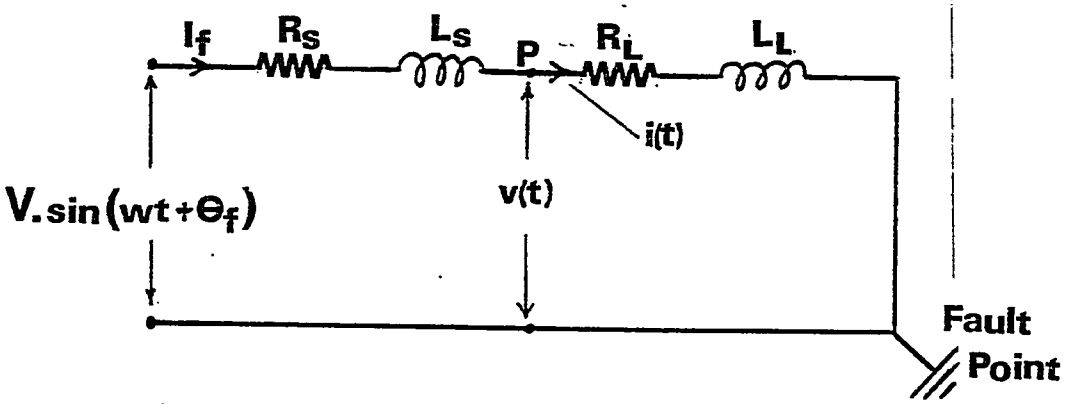


Figure I.1 A single phase faulted circuit

shown in Figure I.2, experiencing a three phase fault at P. The voltages of the three phases at the relay location, T, are given by

$$v_a(t) = 14044 \sin (wt + 14.5^0 + 83.12^0 - 85.4^0) + 453e^{-30t}$$

$$= 14044 \sin (wt + 12.22^0) + 453e^{-30} \qquad (I.3)$$

$$v_b(t) = 14044 \sin [(wt-120^0) + 14.5^0 + 83.12^0 - 85.4^0)] - 195e^{-30t}$$

$$= 14044 \sin (wt - 107.78^0) - 195e^{-30t} \qquad (I.4)$$

$$v_c(t) = 14044 \sin [(wt - 240) + 14.5^0 + 83.12^0 - 85.4^0] - 258e^{-30t}$$

$$= 14044 \sin (wt - 227.78^0) - 258e^{-30t} \qquad (I.5)$$

In these equations, the first term represent the 60 Hertz component of the voltage waveforms. Θ_f is assumed to be 14.5^0, θ_L and θ are determined to be 83.12 and 85.4 degrees.

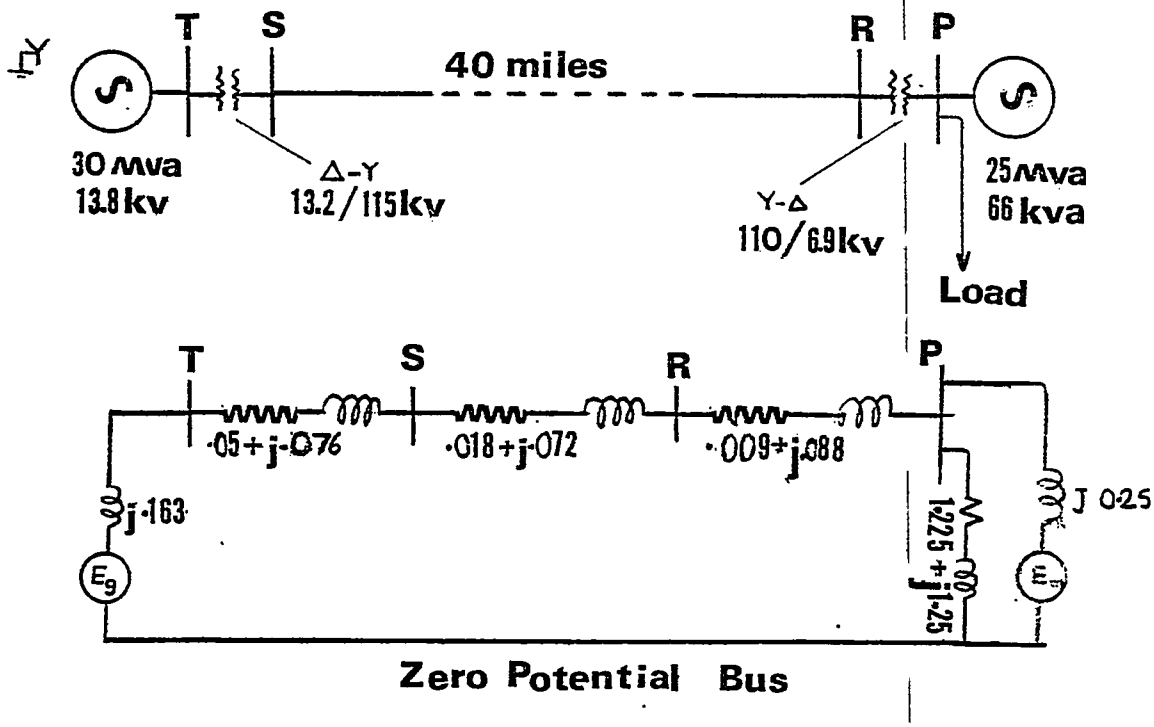


Figure I.2 One line diagram of a transmission system and its positive sequence diagram 25000 kVA and 6.6 kV base values.

The voltages described by Equations I.3 to I.5 were simulated in a software program and were sampled at 100 kHz. The voltage waveforms and their zero crossings determined by the software program are depicted in Figures I.3 to I.5. An examination of these figures shows that there is no difference in the time durations of the successive full cycles. This is not true for half cycle durations because the variations in the time durations of successive half cycles are significant. It is also apparent that the time duration is substantially different for the cycles in which the fault occurred. In Figure I.3,

the time duration of the phase A cycle in which fault occurred is approximately 0.2 msec less than the nominal value. These deviations for the B and C phases are also 0.2 msec.

This study shows that the system frequency determined by measuring the time durations of the full cycles is not affected by the presence of the decaying D.C. component.

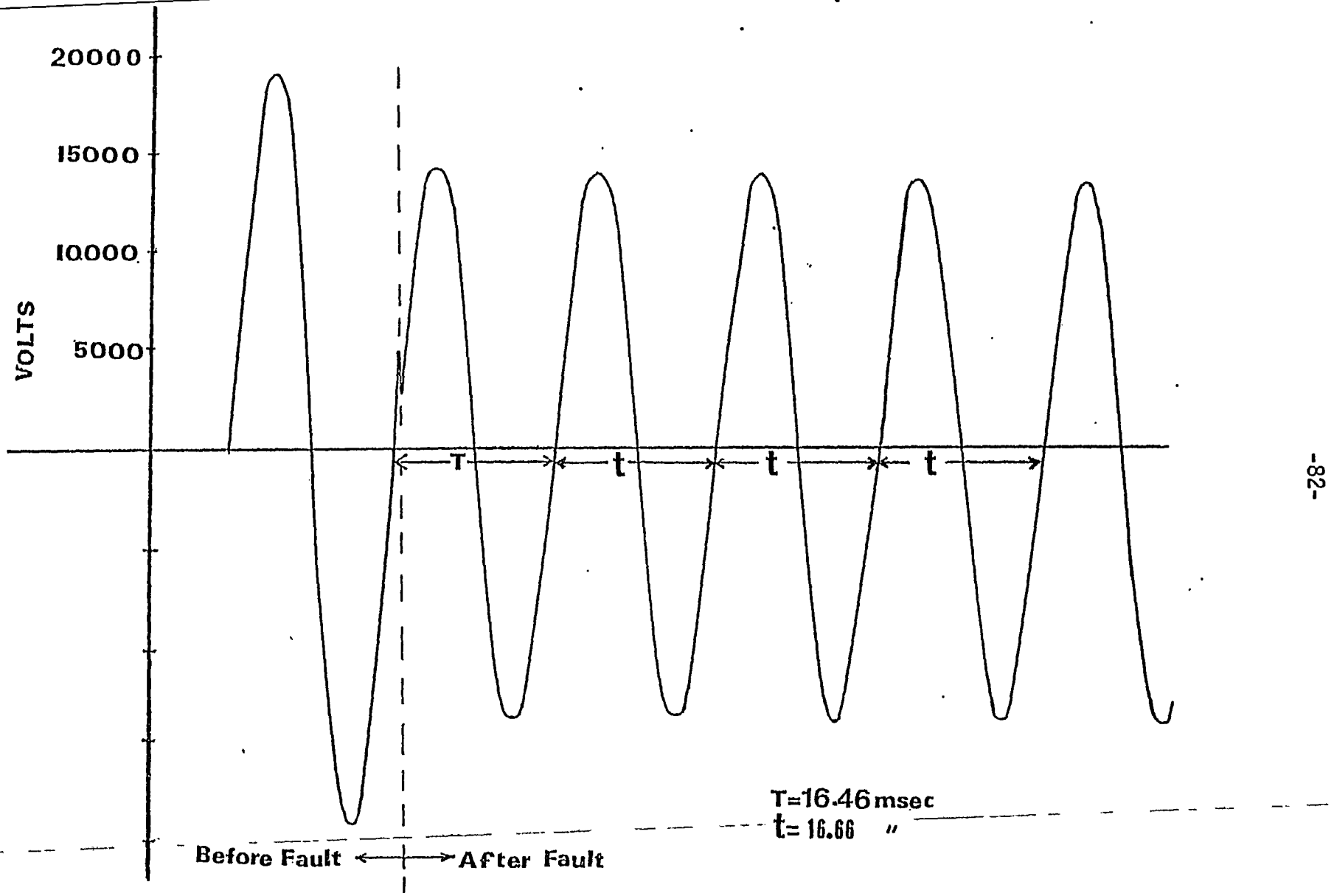


Figure I.3 Voltage waveform of Phase A at point T.

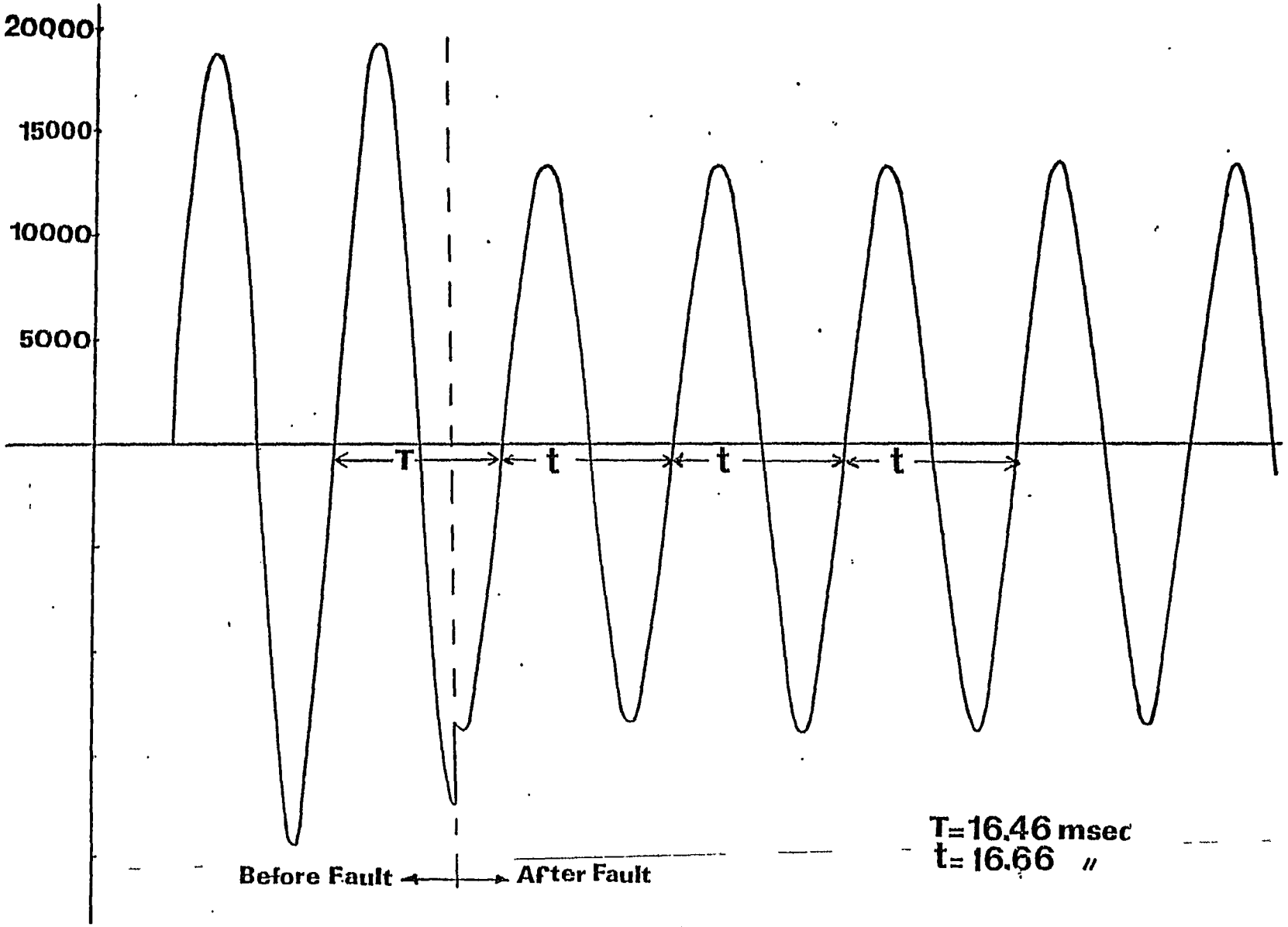


Figure I.4 Voltage waveform of Phase B at point T.

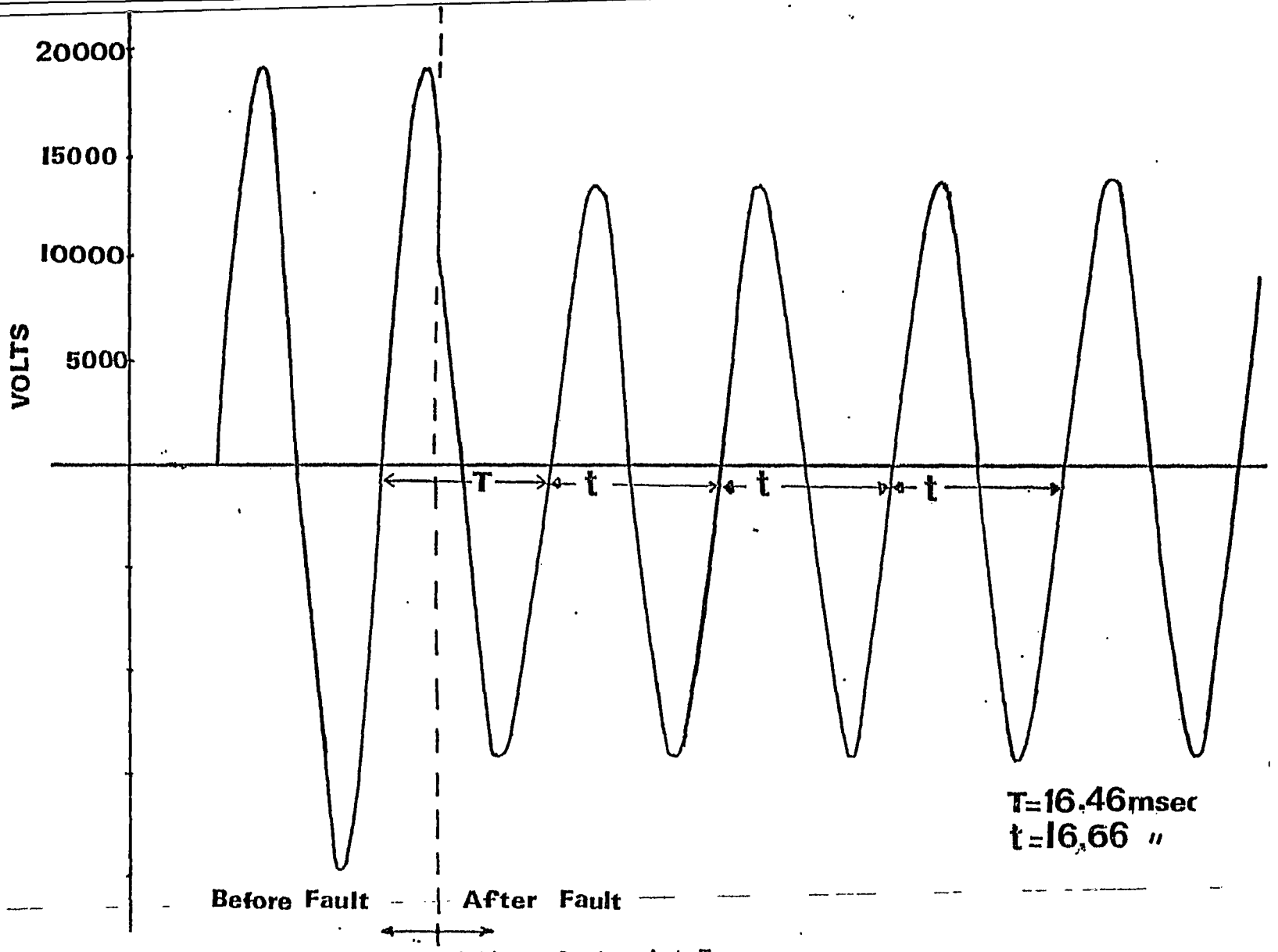


Figure I.5 Voltage waveform of Phase C at point T.

APPENDIX II Counter Circuit

The schematic diagram of the counter circuit is given in this Appendix. The purpose for which each integrated circuit is used, is also briefly described.

II.1. Description of the Circuit Elements

Zerocrossing Detector (CA 3059)

This integrated circuit detects zero crossings and produces a pulse at each zero crossing of the input signal.

Monostable Multivibrator (74121)

A monostable multivibrator has a single stable operating state but can be triggered into unstable operation by the application of an input signal. Once triggered, the output is independent of further transitions of the input but is a function of the timing components. By choosing appropriate components (resistors and capacitors), the width of output pulse can be controlled to be from 40 nano-seconds to 40 seconds.

A monostable multivibrator pulse width of approximately 1 msec was achieved by using R_1 of 33 kΩ & C_2 of 47nF. This multivibrator was used at the output end of the zerocrossing detector to prevent multiple operations due to the noise in the vicinity of the zerocrossings. The other multivibrators used in the circuit generate pulses to clear the output of the binary counter; to transfer information from the counter to the registers to clear the register output and to set the buffer receive flag.

Dual D-Type Edge Triggered Flip-Flop (7474)

This bi-stable circuit changes the unit state when triggered. A removal of the input signal leaves the unit state unchanged. The D-Flip-Flop, thus, generates a square wave output at half the input frequency.

4-Bit Binary Counter (7493)

Three high speed 4-bit binary counters are connected in series to form one 12-bit counter. Two 12-bit counters formed in this manner are used in the circuit.

Hex Quadruple D-Type Flip-Flops with Clear Inputs (74174)

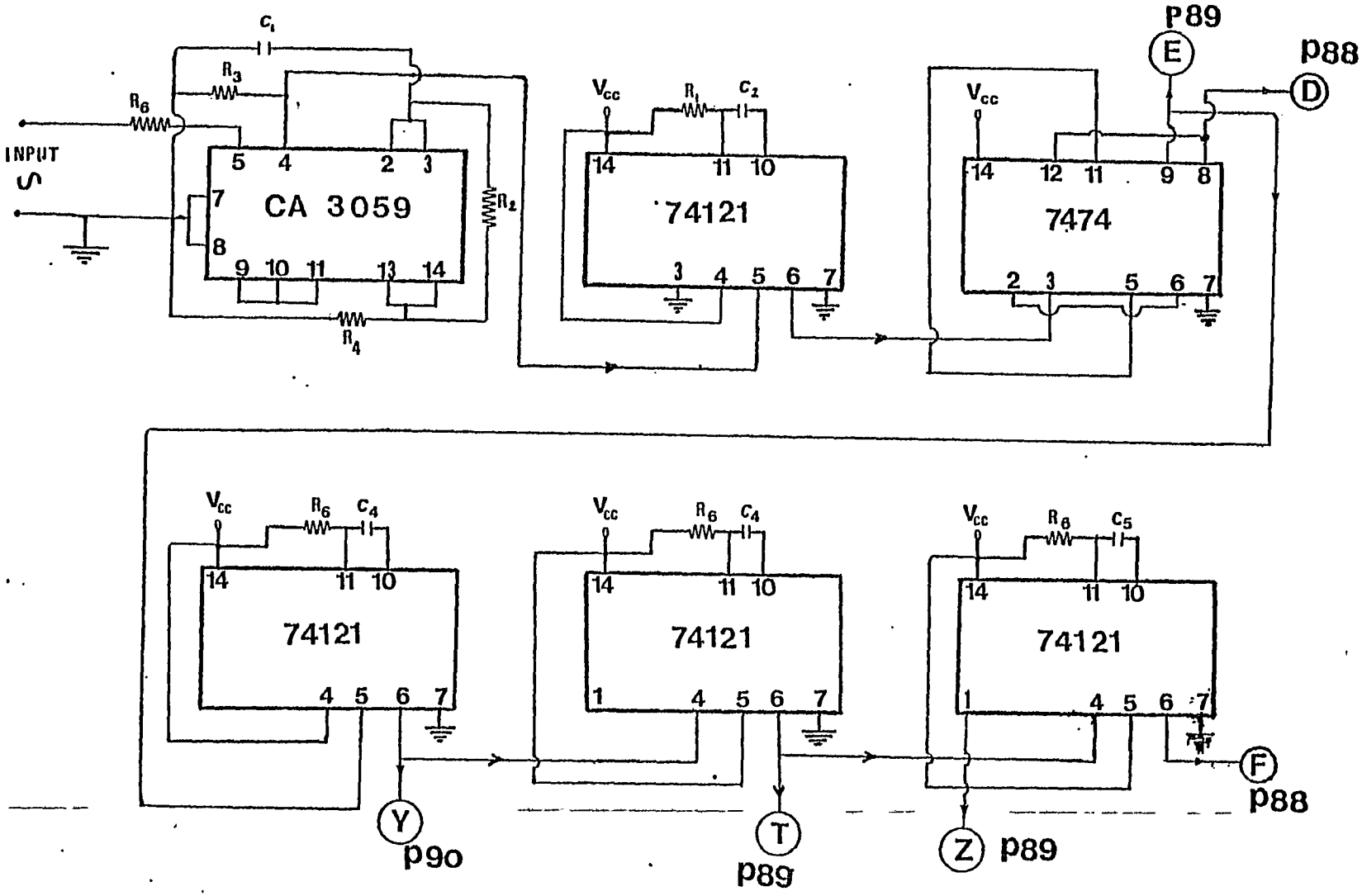
These positive edge triggered flip-flops are used in the circuit as registers.

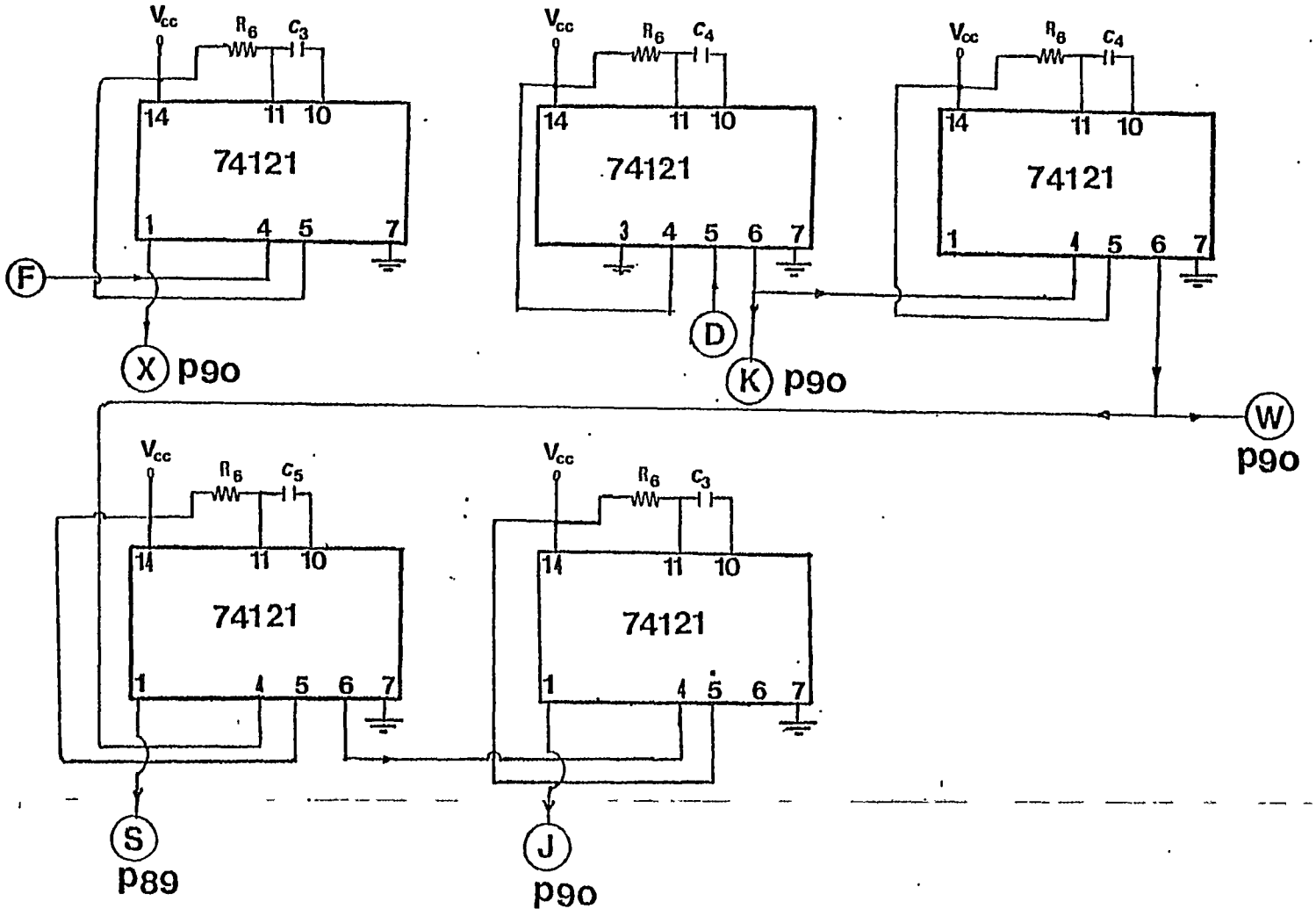
Hex Buffer/Driver with Open Collector High Voltage Output (7407)

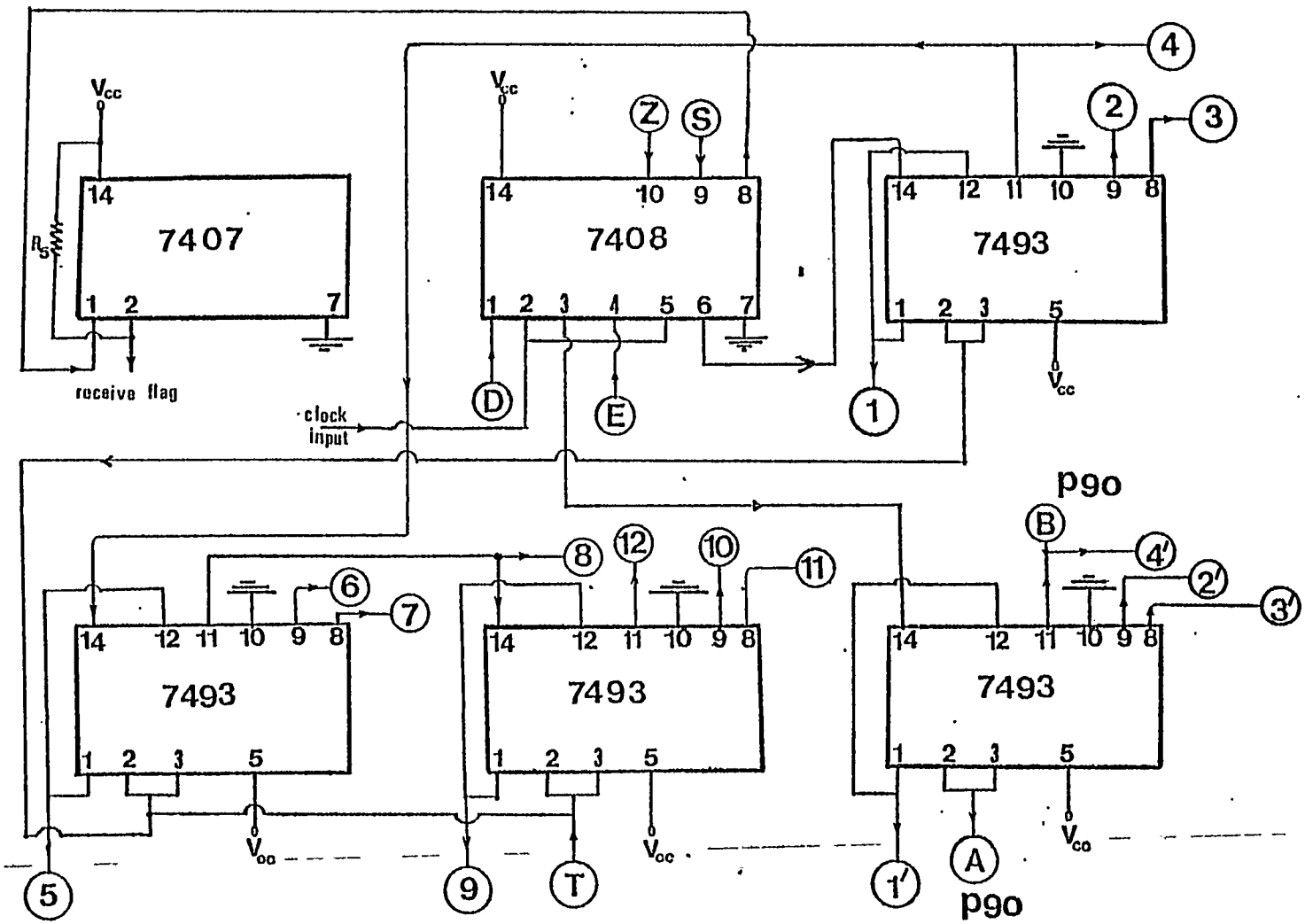
This circuit provides high current open collector output to drive sufficient current for setting the receive flag of the interprocessor buffer. This flag is set as soon as the computer is ready to receive the information for the counter circuit.

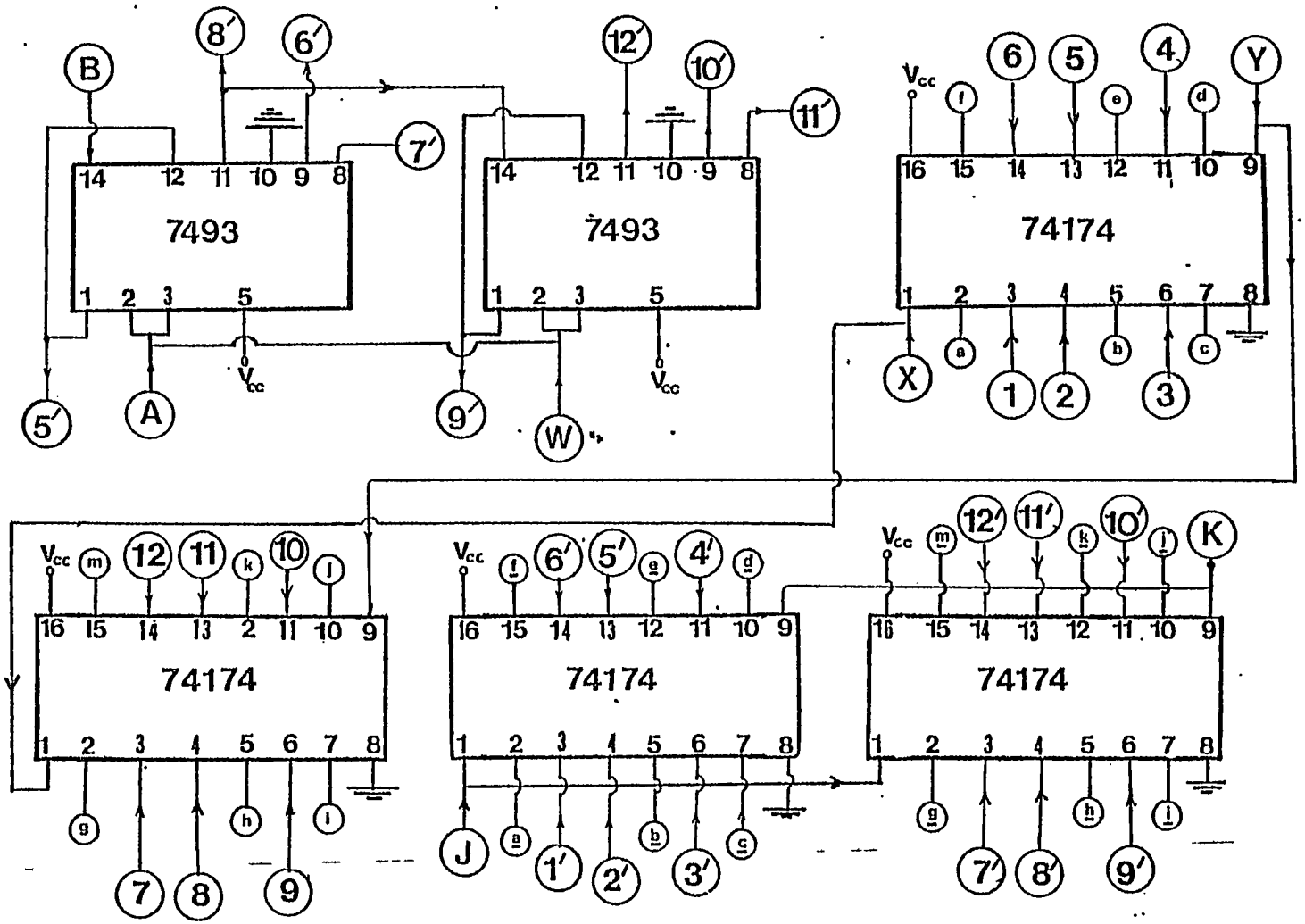
Quadruple 2-input positive AND gates (7408) and Quadruple 2 input positive OR gates are also used in the circuit.

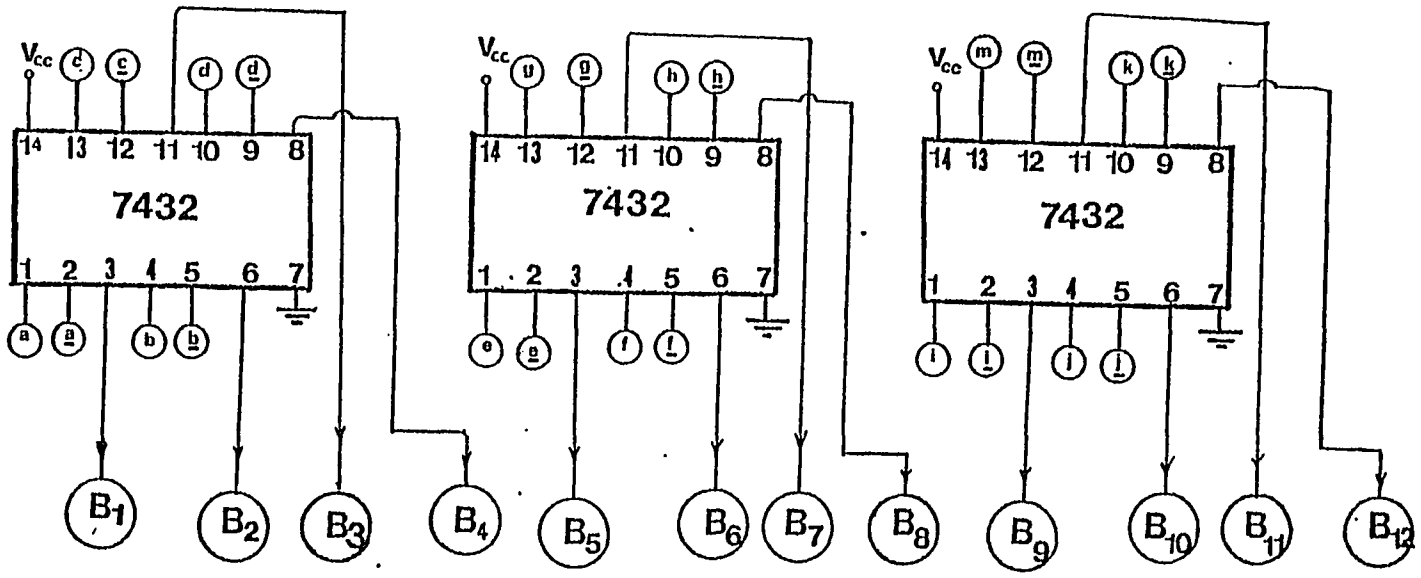
II. 2 Schematic Diagram of the Counter Circuit




Vcc
R6
C3
14
11
10
74121
1
4
5
7
F
X
p90
Vcc
R6
C4
14
11
10
74121
3
4
5
6
7
D
K
p90
Vcc
R6
C4
14
11
10
74121
1
4
5
6
7
W
p90
Vcc
R6
C5
14
11
10
74121
1
4
5
6
7
S
p89
Vcc
R6
C3
14
11
10
74121
1
4
5
6
7
J
p90


7407
7408
7493
7493
7493
7493
V_{cc}
R_S
receive flag
clock input
p90
p90
Z
S
D
E
T
A
1
2
3
4
5
6
7
8
9
10
11
12
1'
2'
3'
4'
B


7493
7493
74174
74174
74174
74174
B
A
W
X
Y
J
K
V_{cc}



B1, B2, ----, B12 is connected to the interprocessor buffer input

B12 is the most significant bit

B1 is the least significant bit

Figure II.1 A schematic diagram of the counter circuit.

II. 3 Part List

Integrated Circuits

Quantity	I.C. No.	Description
9	74121	Monostable multivibrator
1	CA3059	Zerocrossing detector
6	7493	4-Bit binary counter
4	74174	Hex-quadruple D-Type flip-flops with clear inputs
1	7474	Dual D-type edge triggered flip-flop
1	7407	Hex buffer/driver with open collector high voltage output
1	7408	Quadruple 2-input positive and gates
3	7432	Quadruple 1-input positive or gates

Discrete Components

Quantity	Values	Description
1	33 kΩ	Resistor (R_1)
1	3.3 kΩ	Resistor (R_2)
1	1 kΩ	Resistor (R_3)
1	4.7 kΩ	Resistor (R_4)
1	470 kΩ	Resistor (R_5)
9	2.2 kΩ	Resistor (R_6)
1	100 μF	Capacitor (C_1)
1	47 nF	Capacitor (C_2)
2	68 pf	Capacitor (C_3)
4	10 pf	Capacitor (C_4)
2	0.018 μF	Capacitor (C_5)

APPENDIX III. Description of the Software of the Digital Relay

The software of the frequency cum rate of change of frequency relay is described in this Appendix. A flowchart of the software program and its listing are also given.

III.1 Software Program

Initialization of Variables

All variables used in this program are first initialized. Two arrays, one of four locations and the other of five locations, are set up and initialized. An array of four locations (L_1, L_2, L_3, L_4) is used for storing the last four values of the input data and another array of five locations (X_1, X_2, X_3, X_4, X_5) is used for storing the sum of the four successive inputs ($L_1 + L_2 + L_3 + L_4$) as they are received. Two variables, M4 and M5, are initialized to -4 and -5 respectively. The relay operation is delayed for two cycles to avoid operation by transients. A variable, DELAY, is initialized to -2 for this purpose.

Storing the Incoming Data and Setting the Arrays

In the next step, the program starts checking the arrival of the information from the counter circuit. On the receipt of data, a receive flag is set. The data is transferred to the accumulator and the receive flag is cleared. The incoming data is then compared with its nominal value (1920) and their difference is determined and stored in location XC temporarily [A clock frequency of 115200 Hz was used and, therefore, the nominal value of the incoming data is 1920 for one cycle of the 60 Hz signal.] The value of XC is then positioned

in the array (L_1, L_2, L_3, L_4). The program then checks if the first four values of the data have been received or not. This is done by incrementing by one the value of M4 at the receipt of each sample and checking if it is zero. If four samples have not yet been received, the program waits for the next sample. On receipt of the four values of this data, they are added and stored in locations XVAL. The array (X_1, X_2,...,X_5) is then prepared from the successive values of XVAL. The completion of the array of XVAL's is checked by incrementing M5 and checking if its value has reached zero. This array is later used to calculate the rate of change of frequency.

Checking the System Frequency

Once the array of XVAL's (X_1, X_2, ...,X_5) is completed, the next step is to check whether the system frequency is in normal limits or not. According to the trip characteristic given in Figure III.1 and used in this work, the system frequency is considered normal if it is more than 59.5 Hz. Truncations during division cause inaccuracies when integer arithmetic is used. To avoid this problem and to enable the measurement of low values of frequencies, the equation used for calculating the deviation of frequency from its nominal value is multiplied by 256. A 0.5 Hz frequency difference, thus, corresponds to 128 in the software program. The following procedure was, therefore, used to determine the deviation of frequency from its normal value.

Equation 3.5 which was developed for determining the frequency is reproduced below.

$$f = \frac{fo^2}{pfc} \cdot (2\ No-N) \qquad \text{(III.1)}$$

Δf, the deviation of frequency from normal is given by

$$\Delta f = f-fo = \frac{fo^2}{pfc} \cdot (2\ No-N) - fo$$

$$= \frac{-fo^2}{pfc} \cdot (No-N) = \frac{-fo^2}{pfc} \cdot \Delta N \qquad \text{(III.2)}$$

Multiplying both sides by 256 and substituting 115,200 for fc, 4 for p and 60 for fo, Equation III.2 reduces as following

$$\Delta F = K.\Delta f = 2.\Delta N \qquad \text{(III.3)}$$

The software evaluates $2.\Delta N$ and stores in XVAL. XVAL is then compared with 128; if it is less than 128, the system frequency is considered to be normal and the program returns to get the next sample. If the system frequency is below the normal value, the possibility of a transient condition distinctly exists. The variable, DELAY, initially set to -2, is incremented by one. If DELAY is less than zero, the program returns to get a new sample. Finding DELAY to be zero is concluded as a condition of subnormal frequency; and the program proceeds to determine the rate of change of frequency.

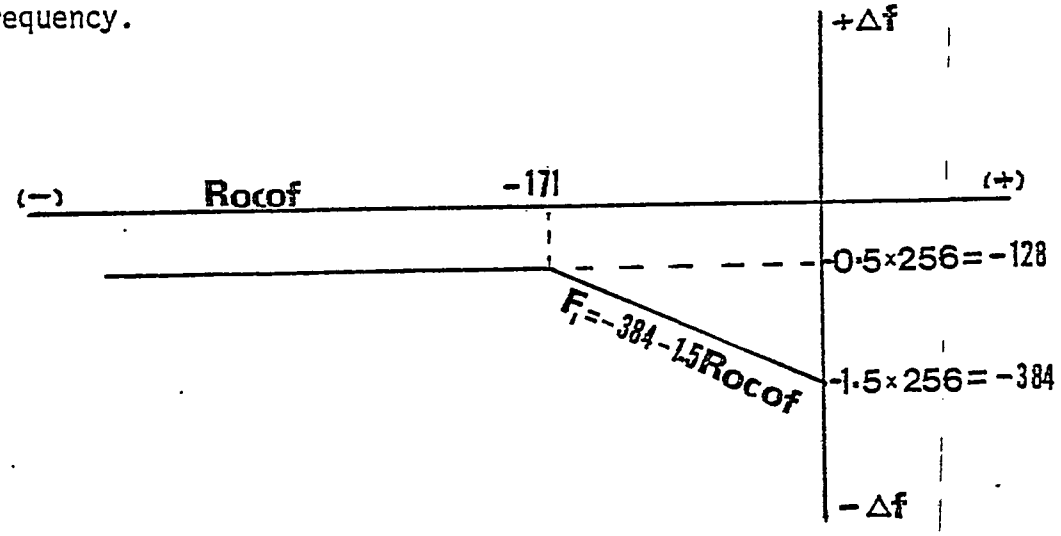


Figure III.1 Trip characteristic of the relay

Determination of the Rate of Change of Frequency

On detecting low frequency, the program determines the rate of change of frequency using the approach of Equation 4.25 which is reproduced below.

$$f^1 = \frac{fo^2}{10.\Delta t.p.fc} (2 N_1 + N_2 - N_4 - 2N_5) \qquad \text{(III.4)}$$

This equation can be rewritten as:

$$f^1 = \frac{fo^2}{10.\Delta t.pfc} \left\{ 2(N_o + \Delta N_1) + (N_o + \Delta N_2) - (N_o + \Delta N_4) - 2(N_o + \Delta N_5) \right\} \qquad \text{(III.5)}$$

In the software program the values of X_1, X_2, X_3, X_4, X_5 correspond to twice the values of ΔN's. Making these substitutions in Equation III.5, provides Equation III.6.

$$2f^1 = \frac{fo^2}{10.\Delta t.pfc} \{ 2X_1 + X_2 - X_4 - 2X_5 \} \qquad \text{(III.6)}$$

Substituting the values fo, Δt, and fc in Equation III.6, and rearranging, the following expression is obtained.

$$\frac{128}{3} f^1 = 2X_1 + X_2 - X_4 - 2X_5 \qquad \text{(III.7)}$$

In the software program, $\frac{128}{3}$ times the rate of charge of frequency is calculated by Equation III.7 and is stored in location ROCOF.

Trip Decision

After determining the rate of change of frequency, it is compared with the limiting value of -4Hz/s. This rate of change of frequency is represented by ROCOF having a value of -171. If ROCOF is found to be less than -171, a decision to shed load is immediately taken. Otherwise, the deviation of trip frequency from nominal value corresponding to the determined rate of change is calculated using

Equation III.9 which represents the relay characteristic.

$$F1 = -384 - (1 + 1/2)\ ROCOF \qquad (III.9)$$

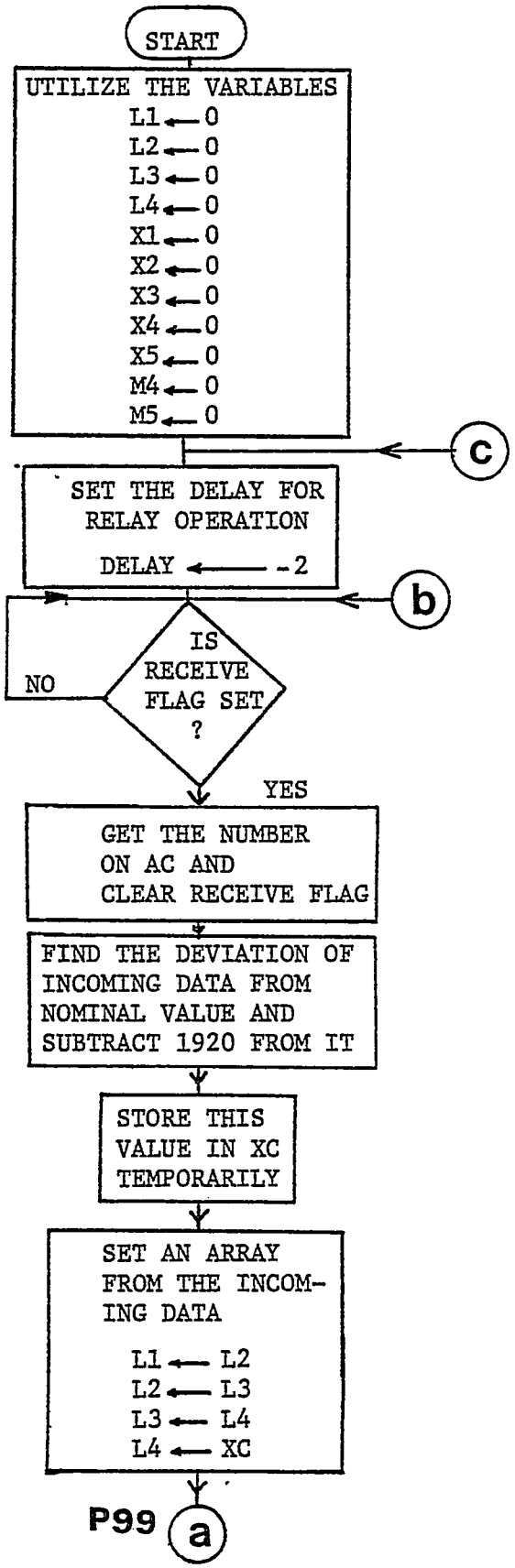
where: F_1 is the required deviation of frequency from the nominal value for shedding load;

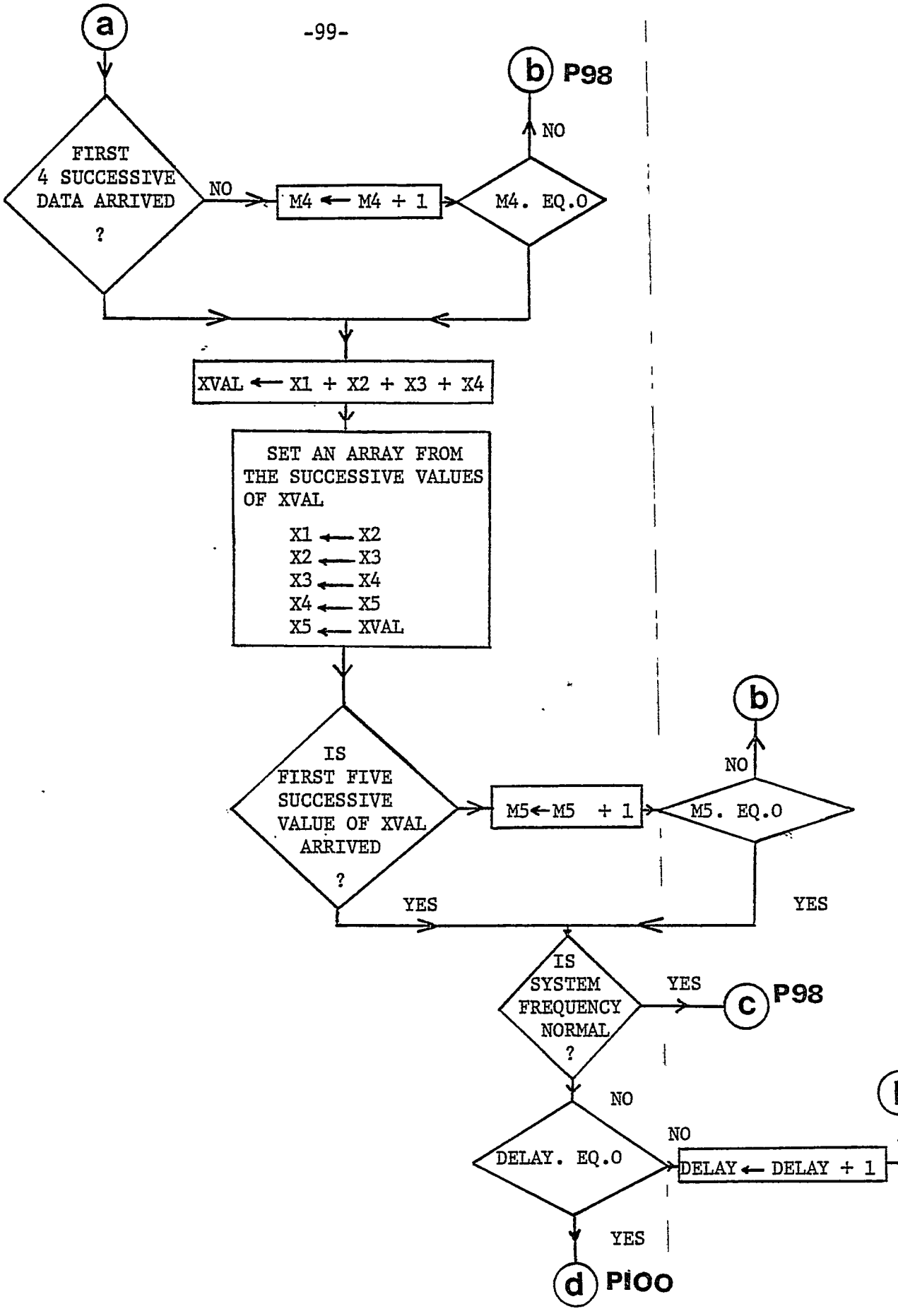
ROCOF is the number stored in location ROCOF.

F1 is now compared with the value of XVAL; the deviation of system frequency from its normal value. If XVAL is found to be equal or less than required value,decision to shed load is taken. If not, the program returns and waits for the next sample.

In the lab testing of this relay, the load shedding decisions were provided as a message printed on the teletype by the computer. The calculated frequency and its rate of change were also printed.

III.2 Flowchart of the Software Program




a
b P98
NO
FIRST 4 SUCCESSIVE DATA ARRIVED ?
NO
M4 ← M4 + 1
M4. EQ.0
XVAL ← X1 + X2 + X3 + X4
SET AN ARRAY FROM THE SUCCESSIVE VALUES OF XVAL
X1 ← X2
X2 ← X3
X3 ← X4
X4 ← X5
X5 ← XVAL
IS FIRST FIVE SUCCESSIVE VALUE OF XVAL ARRIVED ?
M5 ← M5 + 1
M5. EQ.0
b
NO
YES
YES
IS SYSTEM FREQUENCY NORMAL ?
YES
c P98
NO
DELAY. EQ.0
NO
DELAY ← DELAY + 1
b
YES
d P100

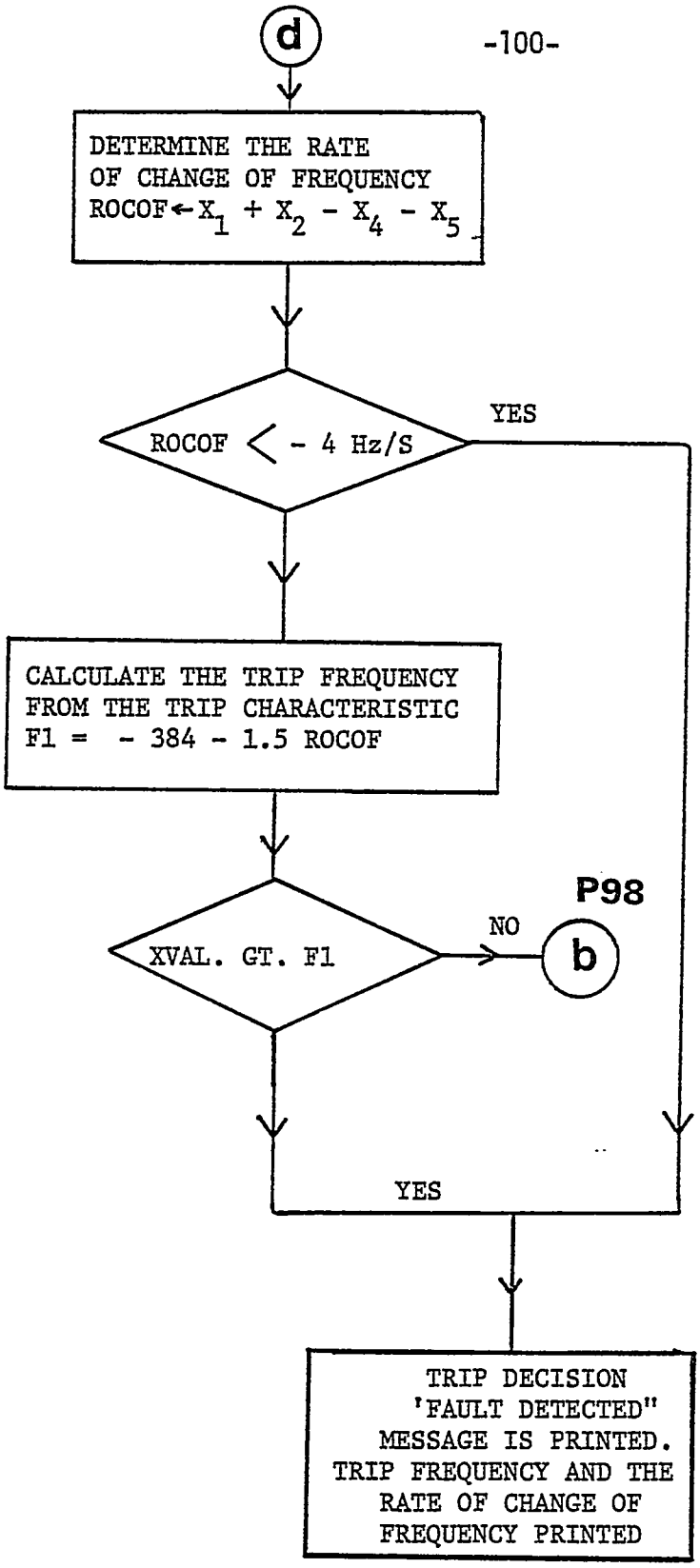


Figure III.2 Flowchart of the software program.

III.3 Listing of the Software Program

```
        /
        /FREQUENCY CUM RATE OF CHANGE OF FREQUENCY RELAY
        /
        /
        /
        DBRF=6501       /SKIP IF RECIEVE FLAG IS SET
        DBRD=6502       /READ INCOMING DATA INTO AC
                       /AND CLEAR RECIEVE FLAG


        /INITILIZATION OF THE VARIABLES
        /THIS PART OF THE PROGRAM SETS THE CONTENTS
        /OF THE LOCATIONS L1,...,L4,X1,...,X5 TO
        /ZERO.ALSO M5 AND M4 ARE SET TO -5 AND -4
        /DELAY IS SET TO -2
*200
START,  TLS         /MAKE SURE TTY FLAG IS SET
        CLA CLL
        TAD CONST
        DCA COUT        /SET COUT TO -9
        TAD TTABLE
        DCA STABLE
        ISZ STABLE
        ISZ COUT
        JMP .-3
        CLA
        TAD MFOUR
        DCA M4          /SET M4 TO -4
        TAD MFIVE
        DCA M5           /SET M5 TO -5
BAC,    CLA CLL         /CLEAR AC AND LINK
        TAD M2           /SET THE TIME DELAY FOR RELAY
        DCA DELAY       /OPERATION

        /THIS SECTION STORES THE LAST FOUR SUCCESSIVE DATA
        /IN LOCATIONSL1,L2,L3,L4 TO SET AN ARRAY
BACK,   CLA
        DBRF             /A LOOP WAITING FOR THE
        JMP .-1          /INCOMING DATA
        DBRD              /READ  INCOMING DATA INTO AC
        TAD M4200         /SUBTRACT 1920
        CLL RAL          /MULTIPLY BY TWO
        DCA XC
        TAD L2
        DCA L1
        TAD L3
        DCA L2
        TAD L4
        DCA L3
        TAD XC
        DCA L4
```

```
        /THIS SECTION CHECKS IF THE ARRAY IS FORMED OR NOT
        TAD M4
        SNA
        JMP GEL         /ARRAY IS SET. PROCEED.
        IAC
        DCA M4
        TAD M4
        SZA
        JMP BACK        /ARRAY IS NOT SET YET . RETURN

        / THIS SECTION ADDS THE  FOUR SUCCESSIVE DATA AND STORES
        /IN XVAL
GEL,    CLA
        TAD L1
        TAD L2
        TAD L3
        TAD L4
        DCA XVAL

        /THIS SECTION SETS AN ARRAY FROM THE LATTEST FIVE
        /SUCCESSIVE  VALUES OF XVAL
        TAD X2
        DCA X1
        TAD X3
        DCA X2
        TAD X4
        DCA X3
        TAD X5
        DCA X4
        TAD XVAL
        DCA X5

        /THIS SECTION CHECKS IF THE ARRAY IS FORMED OR NOT
        TAD M5
        SNA
        JMP YER         /ARRAY IS FORMED. PROCEED.
        IAC
        DCA M5
        TAD M5
        SZA
        JMP BACK        /ARRAY IS NOT FORMED YET. RETURN.

        /THIS SECTION CHECKS IF THE SYSTEM FREQUENCY IS
        /NORMAL OR NOT
YER,    TAD X5
        TAD M128
        SPA
        JMP BAC         /NORMAL.RETURN AND GET THE NEXT DATA

        /THIS SECTION DELAYS THE RELAY OPERATION AGAINST
        /TRANSIENTS
CHECK,  CLA CLL
        TAD DELAY
        SNA
        JMP RATE
        IAC
        DCA DELAY
        JMP BACK
        PAGE
```

```
        /THIS SECTION CALCULATES THE RATE OF CHANGE
        /OF FREQUENCY
RATE,   CLA  CLL
        TAD X4
        CIA
        TAD X2
        DCA XM
        TAD X5
        CIA
        TAD X1
        SMA
        CLL RAL
        SMA
        JMP HERE
        CIA
        CLL RAL
        CIA
HERE,   TAD XM
        DCA ROCOF       /RATE OF CHANGE OF FREQUENCY DETERMINED

        /THIS SECTION  CHECKS IF THE RATE OF CHANGE OF
        /FREQUENCY IS GRATER THAN 4HZ/SEC OR NOT
        CLA CLL
        TAD ROCOF
        TAD N171
        SPA
        JMP TRIP        /YES,GRATER THAN 4HZ/SEC

        /THIS SECTION CALCULATES THE TRIP FREQUENCY
        CLA
        TAD ROCOF
        SMA
        JMP ILERI
        CIA
        DCA ROCO
        TAD ROCO
        CLL  RAR
        TAD ROCO
ILERI,  TAD M384
        DCA F1        /TRIP FREQUENCY DETERMINED

        /THIS SECTION COMPARES THE SYSTEM FREQUECY WITH THE TRIP
        /FREQUENCY.TRIP DECISION IS MADE IF SYSTEM FREQUENCY
        /IS LESS THAN TRIP FREQUENCY
        TAD F1
        TAD X5
        SPA
        JMP BACK
        JMP TRIP
        PAGE

        /THIS SECTION TYPES A MESAGE INDICATING THAT A FAULT
        /IS DETECTED.ALSO TRIP FREQUENCY AND RATE OF CHANGE OF
        /FREQUENCY IS PRINTED
TRIP,   CLA CLL
        TLS
        TAD HEAD1
        DCA POINTR
        TAD AMOUNT
        DCA COUNT
```

```
          TAD I POINTR
          JMS TYPE
          ISZ POINTR
          ISZ COUNT
          JMP .-4
          JMS CRLF
          CLA CLL
          TAD X5
          CIA
          DCA 44
          JMS I FLOTP
          JMS I FDIVP
          NUM256
          JMS I FADDP
          NU60
          JMS I FOUTP
          TAD ROCOF
          DCA 44
          JMS I FLOTP
          JMS I FMPYP
          N3
          JMS I FDIVP
          NUM128
          JMS I FOUTP
          HLT
HEAD1,    HEAD
POINTR,   0
HEAD,     306
          301
          325
          314
          324
          240
          304
          305
          324
          305
          303
          324
          305
          304
AMOUNT,   -16
COUNT,    0
K215,     215
K212,     212
TYPE,     0
          TSF
          JMP .-1
          TLS
          CLA CLL
          JMP I TYPE
CRLF,     0
          TAD K215
          JMS TYPE
          TAD K212
          JMS TYPE
          JMS I CRLF
NUM128,   10
          2000
          0
```

```
NUM256, 11
        2000
        0
N3,     2
        3000
        0
NU60,   6
        3600
        0
FLOTP,  5533
FDIVP,  6722
FADDP,  7000
FMPYP,  6600
FOUTP,  5600
M2,     7776
IN,     0
M4200,  4200
XC,     0
M4,     0
M5,     0
MFOUR,  7774
MFIVE,  7773
XVAL,   0
M128,   7600
XM,     0
ROCOF,  0
DELAY,  0
ROCO,   0
N171,   253
N60,    74
M384,   7200
F1,     0
CONST,  7767
COUT,   0
TTABLE, L1
STABLE, 0
*2000
L1,     0
L2,     0
L3,     0
L4,     0
X1,     0
X2,     0
X3,     0
X4,     0
X5,     0
        $
```