3D-IC Technology Characterization and Test Chip Design

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by

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Abstract

With sub-micron silicon processing technology reaching under 30nm, it becomes more difficult for integrated circuits to achieve higher integration through the scaling down of the transistor size. Three-dimensional integrated circuit (3D-IC) technology stacks multiple dies together and connects them using through-silicon vias (TSVs). This is a low cost and highly efficient way to increase integration. TSVs and stacked dies are two major features of the 3D-IC technology. However, the stacked structures using TSV interconnects induce concerns in reliability such as TSV strain effect, heat problem, and TSV coupling at high frequency, etc. The reliability concerns need to be carefully addressed before 3D-IC technologies can be widely adopted by the industry. Many studies have been carried out in this field, but there has not been much significant work done for testing electrical, mechanical and thermal issues of the 3D-IC technology simultaneously on a single test chip. In this work, a test chip including various test structures was designed to study and analyze these issues in a 3D-IC technology. An accurate resistance and capacitance (RC) model of the TSV for low frequency design was developed, high frequency electrical performance of the TSVs was characterized, coupling between TSVs was modeled, and the stress effect and the heat dissipation method were analyzed in the 3D-IC technology. The TSV model could be added to the design kit for future 3D-IC design and other results could be used to improve the reliability of 3D-IC designs and optimize the performance.

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List of Abbreviations

BEOL	Back End of Line
BGA	Ball Grid Array
CMP	Chemical-Mechanical Polishing
CTE	Coefficient of Thermal Expansion
DIBL	Drain-Induced Barrier Lowering
ELR	Extrapolation in the Linear Region
ESD	Electrostatic Discharge
FEOL	Front End of Line
KOZ	Keep Out Zone
MCM	Multi-Chip-Modules
TSPC	True Single-Phase Clock
TSV	Through Silicon Via
WLP	Wafer-Level Packaging

1. Background and Motivation

Nowadays, there are increasing demands for low power, high speed, multi-function electronic devices. A good example is mobile phone. When it first came in about twenty years ago, cellular phones served one purpose only: sending and receiving voice communications. Today, mobile phones are equipped with customized software, Internet access, digital cameras, portable music players, GPS functions and there are many more options. People are used to fast development of electronic devices and expect further improvement with every generation of products. The commercial market demands faster, smaller and more powerful electronic devices which drive semiconductor industry to pursue for low-cost and low-power integration. For power saving and faster speed, a single chip needs to implement more function. This could be achieved by the fast development of deep sub-micron electronic technologies.

The Moore's Law, which predicted that the number of components in integrated circuits would double every two years, has been proven to be uncannily accurate. The law is now used in the semiconductor industry to guide long-term planning and to set targets for research and development. Much effort has been made to keep following the Moore's Law as the IC industry develops. The most advanced CMOS technology currently is 20nm; however, as the transistor channel length is now only a few tens of nanometers in current technology, it is getting harder and harder for CMOS technology to follow the Moore' Law. There are two major difficulties in keeping scaling down the transistor size, one is the semiconductor physics property limitation and the other is the process technology limitation.

It's getting harder for IC technology to continually reduce the transistor size. In order to meet the growing demand for integration improvement, 3D-IC packaging was invented with

the involvement of many manufacturers. This is the future trend for chip packaging.

1.1 3D-IC Technology Introduction

3D-IC(Three-Dimensional Integrated Circuit) technology is not a new idea. It was first proposed by Jim Early [1] in 1960. However, after that, few people paid attention to it since the speed of development of semiconductor fabrication process can keep up with the demand for chip integration. Not until 2008 did engineers realize that it would be impossible for the semiconductor process technology to continually shrink the transistor size. The 3D-IC came to their mind and developed very fast since then.

3D-IC technology basically stacks different dies together and connects them using Through Silicon Vias(TSV). This will not only improve the integration in 2D by scaling, but also in 3D by stacking dies. There is no theoretical limitation on how many dies can be stacked, so the 3D-IC technology is now becoming a trend to solve the IC integration problem and more chips would use 3D-IC technology in the future. The typical structure of 3D-IC chip is shown in Figure 1.1.

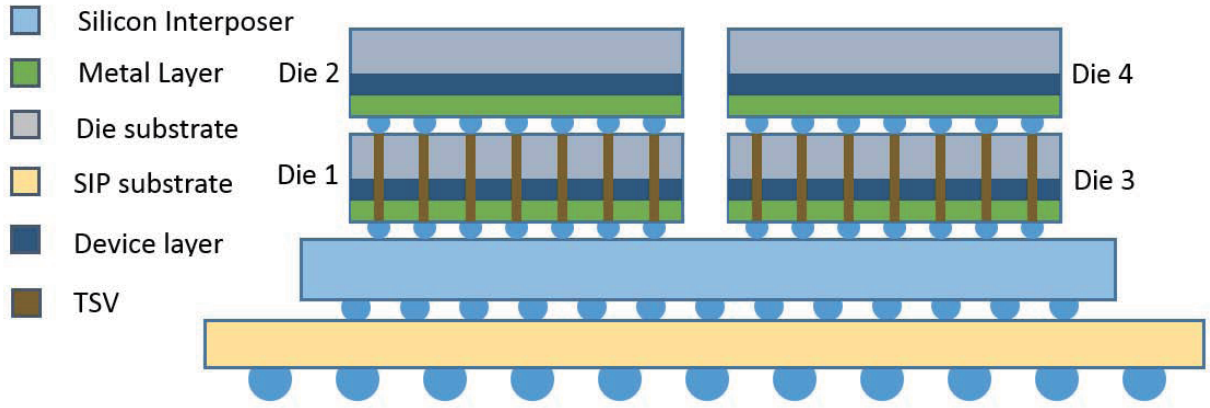


Figure 1.1: Typical 3D-IC Structure

There are several stack IC package methods available, for example, multi-chip-modules (MCM), wire-bonded stacks, ball grid array (BGA) stacks, wafer-level packaging (WLP), face-to-face microbump and 3D-IC [2–4]. Among them, the 3D-IC technology is the most suitable method, considering the cost and the performance. Compared to the traditional 2D-IC, 3D-IC has the following advantages:

- Heterogeneous Integration:

  Even dies from different technologies can be integrated together by 3D-IC.

- High Degree of Integration in a Small Form Factor.

- Improved Power Consumption.

- Low cost:

  Capable of implementation on any current technologies by adding some extra processing steps.

- Speed improvement: Figure 1.2 shows how a 3D-IC improves timing and occupies less space compared to a 2D-IC.

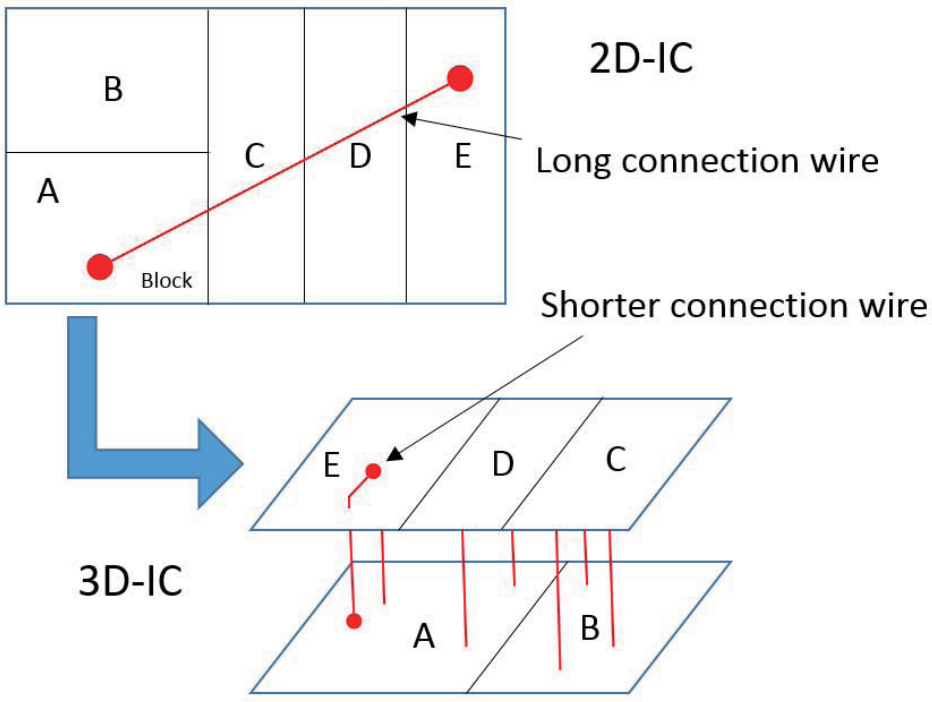


Figure 1.2: Timing improvement: 3D-IC compares to 2D-IC

According to the published paper [5], 3D-IC can significantly improve the IC performance as shown in Table 1.1.

Performance Factor (Area * Timing * Power) = 14

Table 1.1: Comparison between 3D and 2D designs

	2D Design	3D Design
Area(mm)	18.238*15.92 = 290.35	(6.4*6.227)*3 = 119.56
Total Wire Length(mm)	182.42	67.42
Max WL Before Buffer Insertion(mm)	13.82	8.68
Max WL After Buffer Insertion(mm)	4	4
Buffer Used	32900	24636
Clock Skew(ns)	2.33	1
Power Dissipation(mw)	646.2	260.2

1.2 Motivation

3D-IC is regarded as an emerging and promising solution to increase the integration. However, the stacked structure has the potential impact on the electrical performance and reliability of the advanced CMOS technologies. There are two major reliability concerns associated with the 3D-IC technologies. The first one is the heat transfer in the stacked structures. Careful study has to be conducted to ensure that no overheating occurs inside of the structures. The second one is related to the reliability concerns induced by the TSV interconnects. This is mainly caused by the high coefficient of the thermal expansion (CTE) mismatch between the metal TSV and the Si. This will lead to an accumulation of irreversible strains in the TSVs, and hence, a failure under thermal cycling conditions can occur. That local strain and deformation in TSV and TSV/Si interface will affect the process and properties of the surrounding devices. A Keep-out Zone (KOZ) has to be properly defined around the TSVs. In addition, the electrical properties of the TSVs should be characterized so that the high-speed signals will be able to pass through the TSVs without significant attenuation.

To efficiently implement the 3D-IC technology, these impacts should be carefully studied. Some research was carried out before; however, most focused on analyzing individual elements instead of the full-chip/package, and were not validated with experimental measurements. Thus, it is very important to have a test chip to determine all these impacts on

a chip level.

1.3 Objectives

The main objective of this research project is to design a test chip to characterize the 3D-IC technology and analyze some related reliability issues. This research project will not only fill the gap of the 3D-IC design kit but also helps designers to better understand the possible reliability issues in 3D-IC design. The following test circuits were designed and simulated:

1. TSV array test circuits were designed to develop an accurate RC model of the TSV for low frequency design and analyzed the possible TSV leakage current.
2. RF test circuits were used to characterize the high frequency electrical performance of TSVs and the coupling between TSVs.
3. Transistor array test circuits were used to analyze the TSV induced strain effect on nearby transistors.
4. Heater and thermal sensor were designed to analyze the heat dissipation method in 3D-ICs.

1.4 Thesis Outline

The rest of the thesis is organized as follows:

In Chapter 2, a brief introduction of the electrical issues that the 3D-IC technology may encounter will be given, followed by the analysis of electrical models of TSVs such as TSV resistance, capacitance and leakage current. The RF performance of TSVs will also be analyzed.

In Chapter 3, transistors' electrical characterization will be discussed; the TSV impact on them will be analyzed and the TSV impact on digital circuits will be introduced.

In Chapter 4, thermal effect of the stacked dies along with diode thermal sensor principle

will be discussed.

In Chapter 5, detailed design of the test chip will be presented, including TSV and transistor arrays, ring oscillator, RF circuits and thermal measurement circuit.

In Chapter 6, simulation results of the circuits will be given including results for test blocks, high frequency and TSV leakage current.

In Chapter 7, conclusion will be given and future work on 3D-IC design will be discussed.

2. Basic Electrical Characterization of TSV

The key feature of the 3D-IC technology is the TSV. In this chapter, TSV structure is introduced, followed by the basic electrical characterization of the TSV. Test structures are given to measure the capacitance, resistance and the leakage current of the TSV. This chapter will also analyze and discuss the high frequency electrical performance of TSVs and the coupling between TSVs.

2.1 3D IC Process and TSV Architecture Introduction

Normally, TSV is built after the FEOL(Front End Of Line) step and before the BEOL(Back End Of Line) step. The first step is called TSV patterning, when plasma is used to etch a deep hole in the silicon substrate. The second step is TSV isolation, this step uses chemical method to form a thin dielectric layer over the etched hole surface. The third step is TSV metallization, when metal is deposited into the hole. The final step is TSV CMP(Chemical-Mechanical Polishing), which polishes the metal overburden [6]. After these steps, TSV is formed and the normal BEOL steps can be done. Notice that the etched hole does not penetrate the wafer, so the wafer needs to be attached on a temporary carrier and thinned to a few tens or a few hundreds of microns. This allows TSV to be accessed from both sides of the die.

TSV consists of a conductor (which could be copper (Cu), tungsten (W), or polysilicon) and a dielectric layer (usually SiO_2) that electrically insulate the conductor from the Silicon substrate as shown in Figure 2.1.

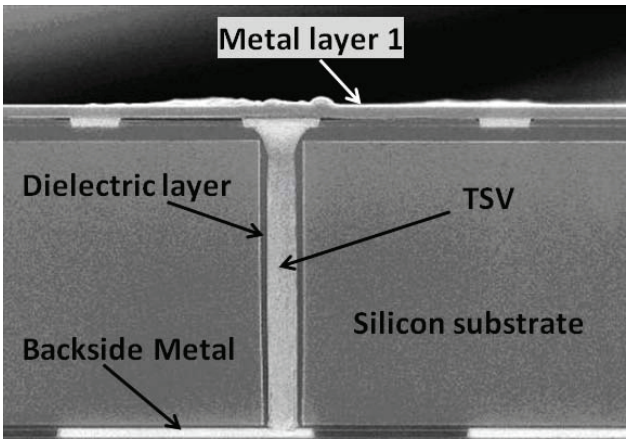


Figure 2.1: TSV cross section [7]

The top view of a TSV may have a different shape depending on the process; it can be a square, circle or polygon. The diameter and the width of the TSV are also determined by the process. The diameter is usually a few microns while the height is a few tens of microns. When the technology is fixed, placement and number of TSVs determine the electrical performance of the TSV. For example, if two adjacent TSVs are connected together, the resistance will be lower compared to a single TSV since they are connected in parallel, but the coupling effects will be bigger as two parallel TSVs will have larger parasitic capacitance. This is a real challenge faced by a 3D-IC designer. One of the objectives of this thesis is to find out the resistance and capacitance of the TSV under certain technology to give advice on the 3D-IC designing.

There are several approaches to bind the dies together, they are face-to-face, face-to-bottom and bottom-to-bottom (face refers to the metal routing layers of the die and the bottom refers to substrate side) depending on the 3D-IC processing technologies. Each approach has different processing steps, but they all need one important step, ie, the die thinning. Die thinning reduces the length of TSV in order to reduce the resistance and capacitance of the TSV and to improve the circuit performance. This step is important, but because of the thin die, it may also have negative effects on the circuit, such as possible increase in heat density.

2.2 TSV Resistance, Capacitance, Inductance and Leakage Current

Resistance, capacitance and inductance are basic electrical properties of the TSV and need to be accurately characterized. 3D-IC designs can be more reliable with accurate TSV RCL models. Resistance and capacitance of the TSV affect circuit performance under low frequency. For high frequency, the inductance effect needs to be counted. Leakge current of the TSV was also analyzed in order to study its impact on TSV's reliability.

2.2.1 TSV Resistance

The resistance of a single TSV could be given as

$$R = \frac{\rho L}{A} \tag{2.1}$$

where ρ is resistivity of the conductor material, L is the TSV length and A is the area of the TSV cross section.

If TSV diameter is D, the thickness of the dielectric layer is S, and the equation becomes

$$R = \frac{4\rho L}{\pi(D-2S)^2} \tag{2.2}$$

Based upon this equation, the TSV resistance can be calculated easily. Table 2.1 showing the relation between the resistance and TSV's geometry [8], the conductor used here is copper and its ρ is $1.75\times10^{-8}(\Omega\cdot\text{m})$.

Table 2.1: TSV resistance calculation

TSV Diameter(μm)	TSV Dielectric Thickness(nm)	TSV Length(μm)	Calculated Resistance(mΩ)
2	50	20	118.491
2	100	20	132.023
5	50	50	44.961
5	100	50	46.853

Besides the theoretical calculation method, simulation models can be setup in TCAD for comparison with theoretical calculation. Another and more accurate way to obtain the

resistance is to conduct a measurement on the real device. Katti et al built a TSV chain by connecting hundreds of TSVs together to make the resistance measurable, they compare the measured resistance with the simulated value, and both were matched well [8]. The schematic of the TSV chain is shown in Figure 2.2.

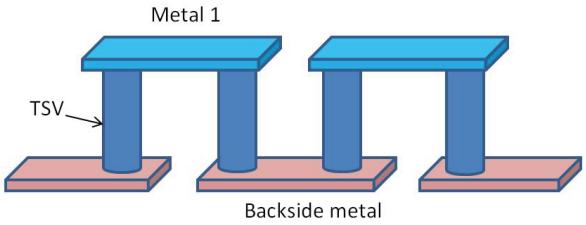


Figure 2.2: TSV Chain

This method is not suitable for real testing because it cannot eliminate the resistance of the connecting metal wires which connect the TSVs. Another way to make an accurate measurement on the resistance of TSVs is by using Kelvin test structure [9] as shown in Figure 2.3. The resistance of the connecting wires will have minimal effects on the measurement of TSV's resistance.

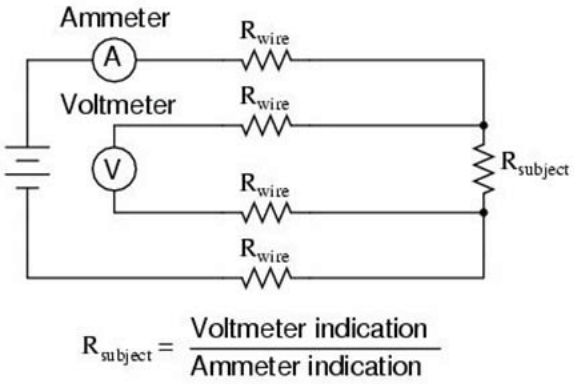


Figure 2.3: Kelvin test structure principle

In this diagram, $R_{Subject}$ is the resistance of the target TSV, R_{wire} is the resistance of the connecting wire, V is the voltage meter and A is the ampere meter. Because the resistance of the voltage meter is ∞, it can read the very accurate voltage added on the TSV. The Ampere meter will show the exact current flowing through the TSV. Using this method the

resistance of a single TSV can be accurately measured. The point is that different pads are needed for voltage and current measurement.

2.2.2 TSV Capacitance

Because of the dielectric layer between the TSV and the silicon substrate, TSV will introduce additional capacitance. This property of the TSV needs to be accurately characterized. Figure 2.4 shows the components of the TSV capacitance.

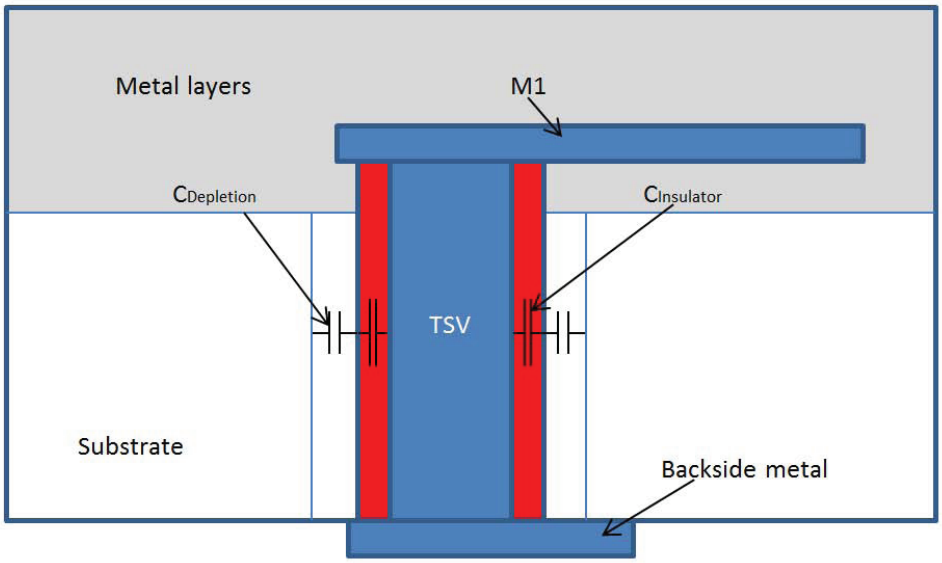


Figure 2.4: Components of TSV capacitance

Figure 2.4 shows that the capacitance of the TSV has two components, $C_{Insulator}$ and $C_{Depeletion}$. To calculate the capacitance, the equation for capacitance calculation: C=q/V can be used. Consider that TSV has the cylinder structure as shown in Figure 2.5.

The $C_{Insulator}$ can be calculated as follows. According to Gauss theorem, the following equations can be used:

$$\begin{cases} E = \dfrac{q}{\varepsilon_0 A} \\ A = 2\pi r L \end{cases} \tag{2.3}$$

where ε_0 is the dielectric constant, E is the electric field intensity and A is the cylinder side area. Since $A = 2\pi rL$, where r (d/2<r<D/2) is the radius of the cylinder), L is the cylinder length, and the following equations can be derived:

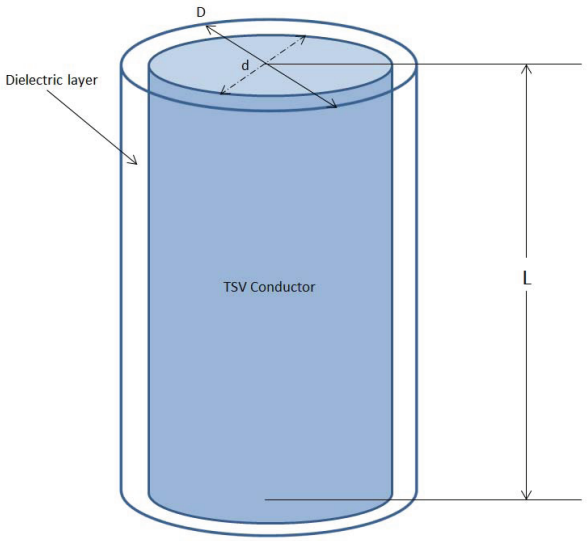


Figure 2.5: TSV cylinder structure

$$\begin{cases} E = \dfrac{q}{2\pi\varepsilon_0 L r} \\ V = ER = \displaystyle\int E dr = -\frac{q}{2\pi\varepsilon_0 L}\int_a^b \frac{dr}{r} = \frac{q}{2\pi\varepsilon_0 L} ln\frac{b}{a} \\ C = \dfrac{q}{V} \end{cases} \tag{2.4}$$

Here a=d/2 and b=D/2, V is the voltage between the TSV and the insulate layer. The equation for calculating $C_{Insulator}$ is:

$$C = \frac{2\pi\varepsilon_i L}{ln(D/d)} \tag{2.5}$$

Another part of TSV capacitance was contributed by the depletion region of the p type substrate that surrounds the TSV. As the voltage on the TSV becomes high enough, a depletion region will be formed between the TSV and the substrate. This is because the majority carriers will be pushed away from the TSV insulator. As a result, a parasitic capacitance will also be formed as shown in Figure 2.4. Since the $C_{Insulator}$ and $C_{Depeletion}$ are connected in sequence, the total capacitance will be smaller than with $C_{Insulator}$ alone. The depletion capacitance can be modeled and solved by 1-D Poisson's equation with proper boundary conditions [10]. It can also be calculated from the following equation, similar to

the equation for $C_{Insulator}$:

$$C = \frac{2\pi\varepsilon_i L}{ln(D_{dep}/D)} \tag{2.6}$$

Where D_{dep} is the diameter of the depletion region, other parameters are the same as those in the previous equation(2.5).

As both $C_{Insulator}$ and $C_{Depeletion}$ can be calculated, the total capacitance can be obtained using the following equation:

$$C_{TSV} = \frac{C_{Insulator}C_{Depeletion}}{C_{Insulator} + C_{Depeletion}} \tag{2.7}$$

The diameter of the depletion region is dependent on the TSV bias voltage causes $C_{Depeletion}$ to be voltage dependent and creates problems. Figure 2.6 shows that the C_{TSV} has three region: Accumulation, Depletion and Inversion region [11].

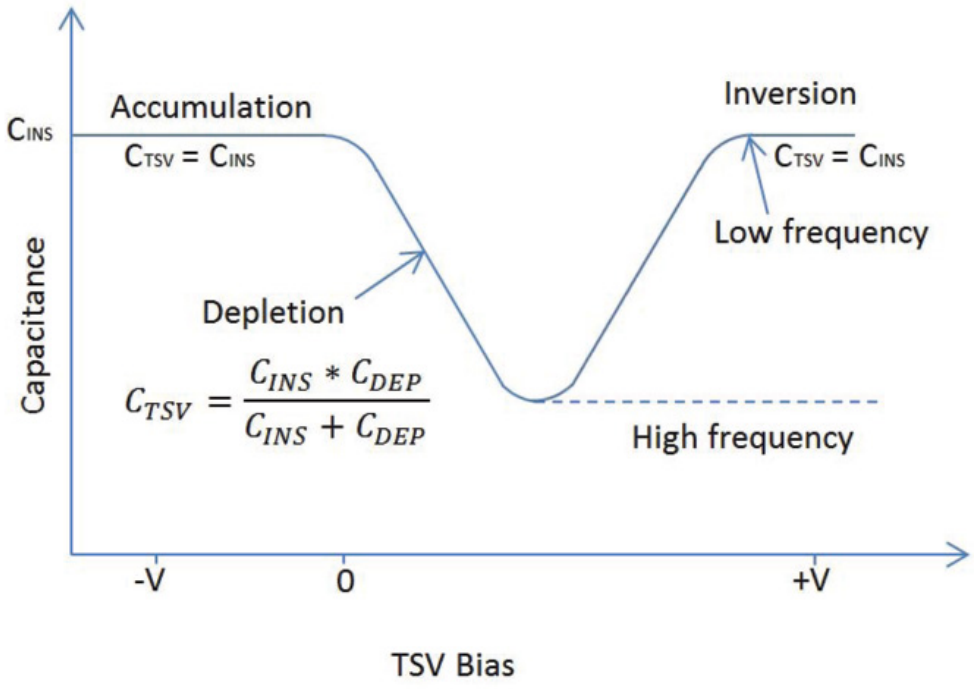


Figure 2.6: TSV C-V curve

Accumulation occurs when a negative voltage is applied on the TSV. The negative charge on the TSV attracts holes from the substrate to the dielectric interface. In this region, no depletion region will be formed so C_{TSV}=$C_{Insulator}$.

With the TSV bias voltage rising, the majority of carriers will be pushed away from the TSV insulator and the depletion region will be formed, so C_{TSV} will become small.

As the TSV bias voltage keeps increasing, another type of negative charge emerges at the dielectric interface. This charge is due to minority carriers, which form a so-called inversion layer. As the TSV voltage is further increased, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential, so the width of the depletion region will reach the maximum. For low frequency signals, electrons will accumulate on the dielectric layer, eventually will convert the P type substrate to an N type one. As a result, this isolation will increase the C_{TSV}. For high frequency signals, the inversion layer will not be formed because it does not have enough time for electrons to respond to the high frequency voltage change in the TSV, the width of the depletion region will remain maximum and the minimum C_{TSV} can be achieved.

From the above discussion, it is clear that if the TSV operates only between VSS and V_{DD}, the C_{TSV} will change as the voltage changes. This is not suitable since designers of the 3D-IC circuits will have to be conservative to only the maximum C_{TSV} situation to avoid timing issue. However, if it is fixed at the maximum C_{TSV}, it will consume more power than the design focuses on smaller C_{TSV} according to the equation

$$P = fCV_{DD}^2 \tag{2.8}$$

Where f is the operation frequency of the TSV signal, V_{DD} is the supply voltage and C is the TSV capacitance. It is evident that the lower TSV capacitance ensures less power consumption. Figure 2.7 shows three possible TSV C-V relationship.

In Figure 2.7, (a) shows the ideal C-V relationship, the C_{TSV} will always be the minimum for high frequency signal; (b) shows the normal C-V relationship which C_{TSV} is varying depending on the TSV voltage; (c) is the worst C-V relationship where C_{TSV} will always be the maximum. In 3D-IC technology, the requirement is to achieve (a) and avoid (b) or (c).

To minimize the C_{TSV}, several methods have been developed. In one of the approaches [12], a negative voltage is applied on the silicon substrate, so even the zero bias on TSV is high enough to achieve the maximum C_{TSV}. However, such a negative bias voltage on the

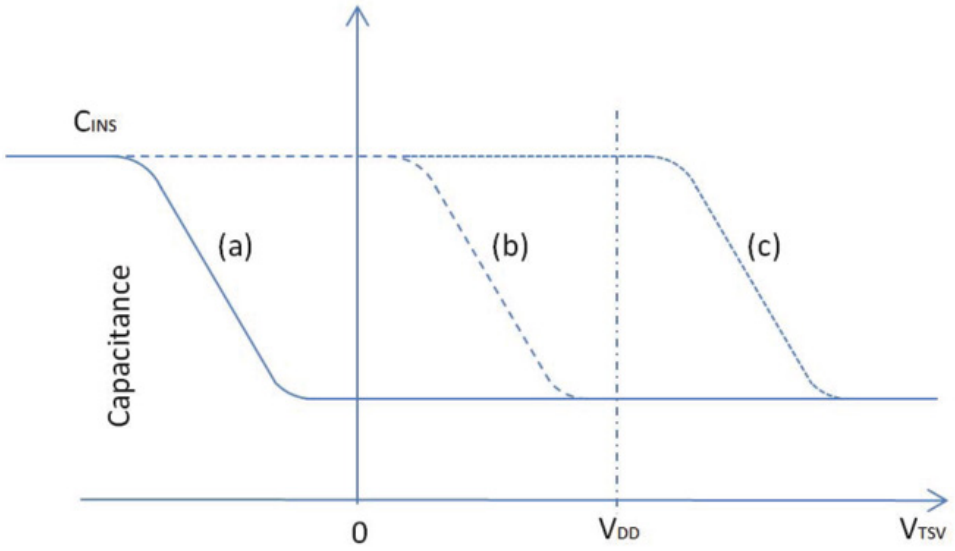


Figure 2.7: Different voltage dependent depletion region

substrate may change the electrical property of the transistor, thus could cause problems in the circuit design. Another possible approach [13] is by tailoring oxide charges in the dielectric layer during the oxidation module. By adding a lot of extra positive charges in the dielectric layer, a depletion region will be formed even though there is zero bias on the TSV. Doping concentration of the positive charge in the dielectric layer can be changed to achieve the minimum C_{TSV}. The problem of this approach is that it makes the process more complicated, however, it is a good method to lower the TSV capacitance since it does not need additional circuit design effort.

2.2.3 TSV Inductance

Unlike the resistance and the capacitance, the inductance of a TSV is not only determined by TSV itself but also by other factors. It is composed by two parts: self inductance and mutual inductance. The self inductance part is fixed, it depends on the technology used because certain TSV physical parameters such as TSV length, diameter are the same for a particular technology. However, the mutual inductance part can vary, as the pitch of TSVs and current direction in TSVs all have big influence on the total TSV inductance. Figure 2.8 shows the cross section of a typical power/ground TSV structure.

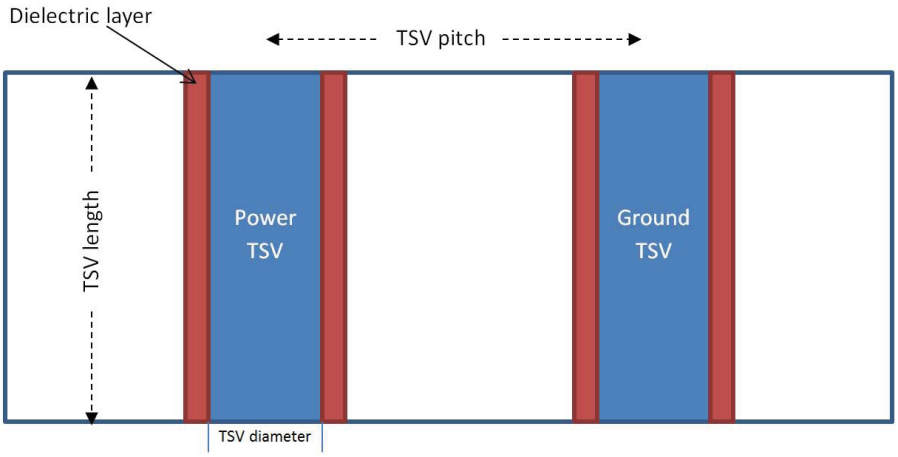


Figure 2.8: Cross section of P/G TSV structure

The inductance of a pair of power and ground TSVs can be calculated by the following equations [14]:

$$L_{TSVself} = \frac{\mu_0 TL}{2\pi}\left[ln\left(\frac{2TL}{TD/2}\right) - 1\right] \tag{2.9}$$

$$L_{TSVmutual} = \frac{\mu_0 TL}{2\pi}\left[ln\left(\frac{TL}{TP} + \sqrt{1+\left(\frac{TL}{TP}\right)^2}\right) - \sqrt{1+\left(\frac{TP}{TL}\right)^2} + \frac{TP}{TL}\right] \tag{2.10}$$

Where $L_{TSVself}$ is the self inductance of the TSV and $L_{TSVmutual}$ is the mutual inductance of the TSV, TL, TD and TP are the length, diameter and pitch of the TSV.

The final TSV could be $L_{TSV} = L_{TSVself} + L_{TSVmutual}$ (if the current direction are the same in the two TSVs) or $L_{TSV} = L_{TSVself} - L_{TSVmutual}$ (if the current direction are different in the two TSVs, as in the Power/Ground TSVs).

According to the equation, it can be seen that as the TSV pitch (which means the distances between TSV) decrease, the L_{TSV} will increase. It means that in case of using TSV array to transfer the signals, TSVs should be placed as far as possible from each other to decrease the inductance.

2.2.4 TSV Leakage Current

The leakage current of the TSV is a vital part of the TSV electrical characteristic; it determines how much static energy the TSV will waste and thereby causing a voltage drop on transferring the signals. Moreover, if the leakage current is too big, it will cause a TSV breakdown, a situation which should be avoided.

The leakage occurrs between the TSV and the substrate because of the process defection in the dioxide dielectric layer [9]. In Figure 2.9 it can be seen that some conductor is

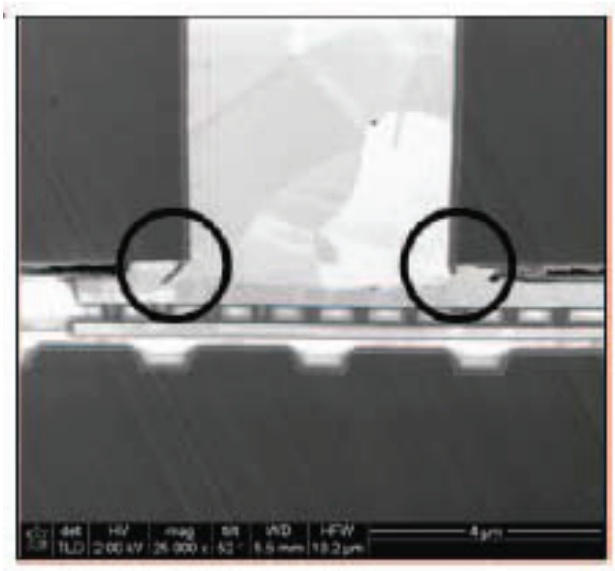


Figure 2.9: X-section analysis of TSV [9]

overwhelming the TSV sidewall, this forms the short circuit between the bottom of the TSV and the substrate. Depend on how big is the short circuit, the leakage current can vary. If it is too big (for example >1nA), it is called a TSV failure. Likewise, if the TSV resistance is too big because of the process defect, it will also be a TSV failure. The dielectric layer plays an important role in TSV yield. Depending on different 3D-IC technology it varies from a few tens of nanometer to hundreds of nanometer, the most important part is that it should be uniformly covered sidewall which holds the TSV. If the quality of the dielectric layer is not good enough, it will not only make the TSV leaky or has big resistance, but also lower the breakdown voltage of the TSV. If an ESD(Electrostatic Discharge) event occurs, the TSV with poor quality of the dielectric layer will likely be damaged while the TSV with

good quality can tolerate high current and voltage [15].

Very few reliability experiments are done on TSVs. To determine the leakage, a TSV array structure can be used. In previous work [9], a 6*6 TSV array was used to measure the TSV failure rate. Each TSV in the array was accessible by two pads, one connected to the top of the TSV and the other connected to the bottom of the TSV. By measuring the resistance and leakage of each TSV, the TSV yield for their 3D-IC process was obtained. The problem of this method is that it needs too many pads (for a 6*6 TSV array, it needs 72 pads) and the resistance and the leakage current of a single TSV was too small to get an accurate measurement.

2.2.5 TSV Electrical Modeling for Low Frequency

Now that the resistance, capacitance and inductance of the TSV are known, the basic electrical model of the TSV can be developed [11].

Figure 2.10 shows a RC model of a single TSV, R_{TSV} causing the voltage drop when signals pass through the TSV and C_{TSV} causing the delay. R and C can be calculated using equations 2.2 and 2.5 in previous sections. Equation 2.2 gives value of R_{TSV} around 387.63mΩ where S is 0.25μm and the length and diameter of TSV are 8 and 1.2μm respectively. Using equation 2.5, the TSV maximum capacitance can be calculated as 5.63μF. For low frequency(<3GHz), the model is accurate enough for circuit simulation. For high frequency, the electrical model will be more complicated.

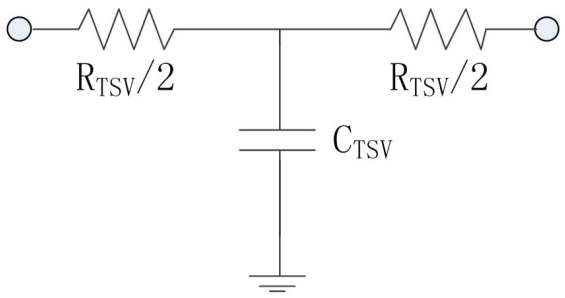


Figure 2.10: TSV impedance model

2.3 TSV RF Characterization

Previous sections are focused on the electrical characterization of TSVs working under low frequencies. This section is focused on high frequency electrical performance of TSV.

According to [16], the diameter of the TSV ranges from 1μm to 5μm, and the density of the TSV on dies can be as high as 10000/mm^2. With such a high density, some problems will arise and affect the 3D-IC RF performance, such as crosstalk. Therefore a careful study of the RF performance is necessary. In this section much attention is focused on the TSV S-Parameter measurement and the crosstalk of two TSVs, and on some techniques to reduce the TSV crosstalk.

2.3.1 TSV S-parameter

To measure the S parameter of the TSV, the simplest way is to connect the network analyzer to both ends of the TSV. However, because the die which contains the TSV is very thin and one end of the TSV is connected to the metal layers, probes to measure from both sides of the die cost very high and are not suitable for a such thin die. An alternative way is proposed [17] to measure S parameters of TSVs from only one side. The test structure is shown in Figure 2.11, two sets of different connecting line length are used.

Test structure set1 has connecting line length L1, and two ports are connected with Via-Line-Via configuration and Line only configuration. Test structure set2 has the same test structure as set1 but with different connecting line length L2. So there are totally four test structures needed for extracting the TSV S parameters, as shown in Figure 2.11, the S_{11}, S_{12}, S_{21}, S_{22} of S_{TL1}, S_{L1}, S_{TL2} and S_{L2} are measured and the S_{TSV} is extracted using a set of equations.

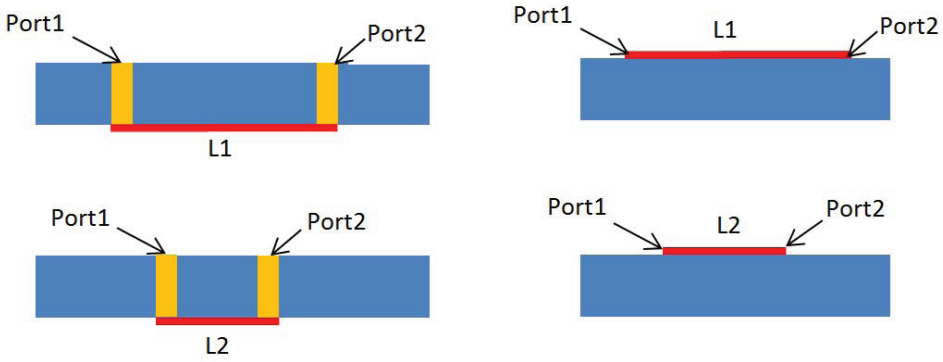


Figure 2.11: Test structure to extract S parameter

The S parameter of the TSV can be represented with an array as follows:

$$S_{TSV} = \begin{bmatrix} S_{11V} & S_{12V} \\ S_{21V} & S_{22V} \end{bmatrix}$$

And

$$S_{TL1} = \begin{bmatrix} S_{11TL1} & S_{12TL1} \\ S_{21TL1} & S_{22TL1} \end{bmatrix} \quad S_{L1} = \begin{bmatrix} S_{11L1} & S_{12L1} \\ S_{21L1} & S_{22L1} \end{bmatrix}$$
$$S_{TL2} = \begin{bmatrix} S_{11TL2} & S_{12TL2} \\ S_{21TL2} & S_{22TL2} \end{bmatrix} \quad S_{L2} = \begin{bmatrix} S_{11L2} & S_{12L2} \\ S_{21L2} & S_{22L2} \end{bmatrix}$$

To extract the S_{TSV} with the 4 sets of measured S parameter, the measured S parameters need to be converted to T parameters first by using the following equation:

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} -\frac{S_{11}S_{22}-S_{12}S_{21}}{S_{21}} & \frac{S_{11}}{S_{21}} \\ -\frac{S_{22}}{S_{21}} & \frac{1}{S_{21}} \end{bmatrix} \tag{2.11}$$

Since the T parameter can be calculated by multiplying its internal parts as $T_{TL} = T_T \times T_L \times T_T$, and with measured S_{L1} and S_{L2}, two sets of equations are available, $T_{TL1} = T_T \times T_{L1} \times T_T$ and $T_{TL2} = T_T \times T_{L2} \times T_T$ and by solving them, the S parameters can be

calculated as follows:

$$S_{11TSV} = S_{22TSV} = \frac{\begin{matrix} S_{12TL1}S_{11L1}S_{12L2} \\ -S_{12TL2}S_{12L1}S_{11L2} \end{matrix} \pm \sqrt{\begin{matrix} S_{12L1}S_{12L2}[S_{12TL1}S_{12TL2}\left(S_{11L1}-S_{11L2}\right)^2 \\ -S_{12TL1}S_{12TL2}\left(S_{12L1}^2+S_{12L2}^2\right) \\ \left(S_{12TL1}^2+S_{12TL2}^2\right)S_{12L1}S_{12L2}] \end{matrix}}}{S_{12TL1}S_{12L2}\Delta_{L1} - S_{12TL2}S_{12L1}\Delta_{L2}} \tag{2.12}$$

And because $S_{12} = S_{21}$, then

$$S_{21V} = S_{12V} = \sqrt{\frac{S_{12TL1}}{S_{12L1}}\left(1 - 2S_{11L1}S_{22V} + \Delta_{L1}S_{22V}^2\right)} \tag{2.13}$$

By using the above method, the S_{TSV} can be extracted by probing from one side. This method was reported to be valid up to 10GHz which is good for our 3D-IC RF characterization. Since the equation gave two sets of results, they need to be plotted and be compared with the simulation result for a single TSV. The correct set of results should match the simulation result quite well [17].

2.3.2 TSV Crosstalk

TSV coupling is one of the most significant impact on TSV RF performance when multiple TSVs are close to each other and transfer different signals. Taigon Song proposed a circuit model to calculate and measure the TSV S-parameter [18]. Here, based on the basic TSV electrical model developed previously, a circuit model of two TSVs can be set up as shown in Figure 2.12.

Here, TSV1 is the aggressor and TSV2 is the victim. Port1 and Port3 are connected to the ground, Port2 is connected to the signal and the voltage on the Port4 can be measured to determine the coupling between these two TSVs. The coupling between the two TSVs is related to the impedance of the ports and the impedance between them. Assume the port impedance are the same and Z_1 is the input impedance, Z_5 is the impedance between two TSVs, equation 2.14 can be used to calculate the coupling between two TSVs. Detailed calculation can be found in [18].

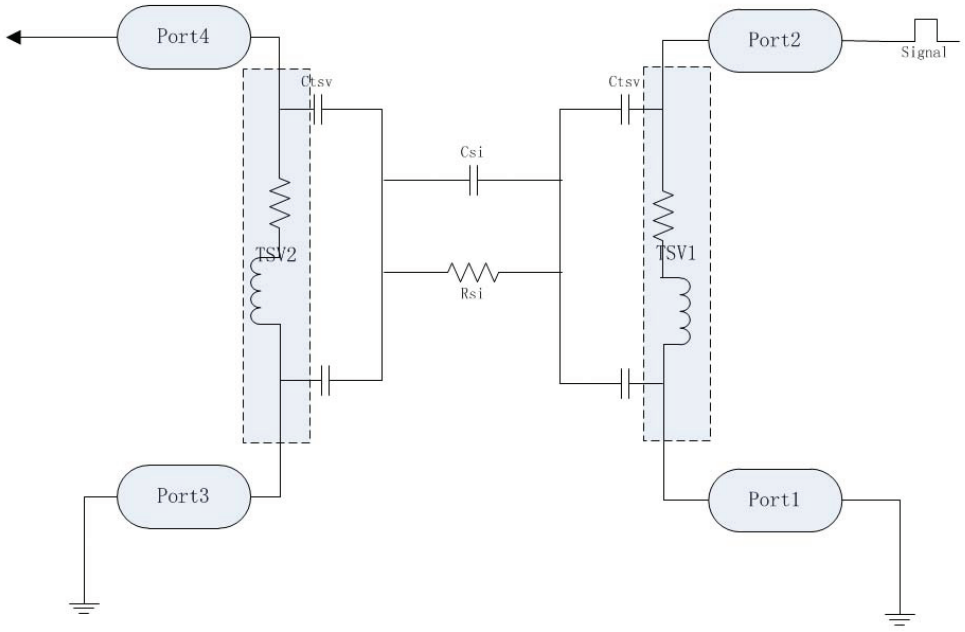


Figure 2.12: Circuit model for TSV coupling

$$V_{coupling} = V_{in} \times \frac{Z_{port}^2}{Z_{port}^2 + Z_{port}\left(3Z_1 + 2Z_5\right) + 2Z_1 Z_5} \tag{2.14}$$

From the equation, it can be seen that if Z_5 which is the impedance between two TSVs becomes bigger, the voltage on the victim TSV will be lower, which means the coupling will be reduced. To make this impedance bigger, K.Yoon proposed two effective ways: TSV guard ring and TSV wall [19]. Figure 2.13 shows the structure for reduce TSV coupling.

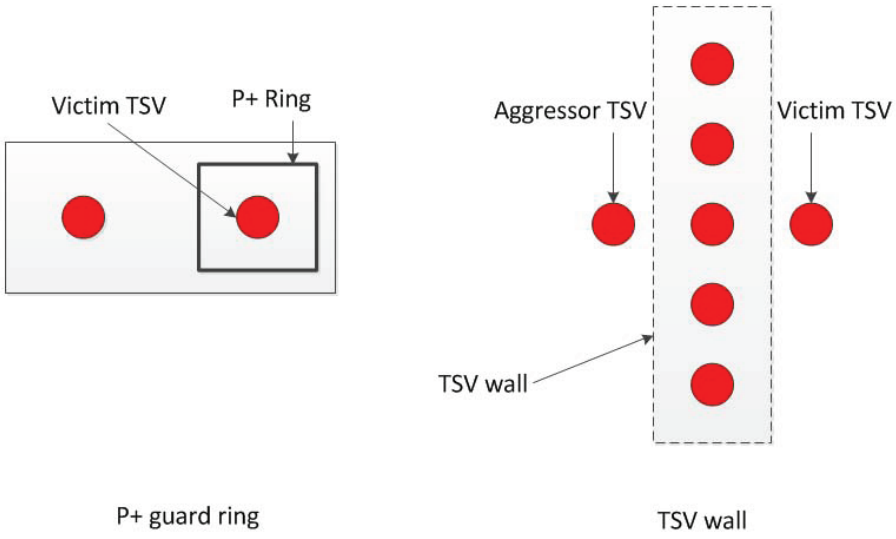


Figure 2.13: Techniques to reduce TSV coupling

This section is mainly focused on the extraction of TSV S parameters and coupling between the two TSVs, and methods to reduce the TSV coupling. The implementation of these circuits and test methods are shown in details in chapter 5.

3. TSV Impact on Transistors and Digital Circuits

In chapter 2, the electrical characteristics of the TSV are discussed. In this chapter, TSV impact on nearby transistors and digital circuits is discussed.

3.1 TSV Impact on Nearby Transistors

In digital designs,the real circuit performance such as time delay and power consumption depends on the basic transistor properties. Influence of TSV on these properties in 3D-IC is an important parameter that needs to be fully analyzed to predict overall performance.

3.1.1 Transistor Characteristic

In this section, important transistor parameters such as threshold voltage V_{th}, saturation current I_{ds}, leakage current I_{leak} are discussed. V_{th} determines the voltage that the transistor will be "ON". It is very important for the digital circuit since it will determine the speed of the integrated circuit. The saturation current I_{ds} is important for the transistor driving ability. The leakage current I_{leak} contributes to a large portion of the transistor power consumption.

(a) Threshold Voltage

The threshold voltage of a MOSFET is the gate voltage which forms an inversion layer at the interface between the gate insulating layer and the substrate of the transistor. When the transistor gate voltage is higher than the V_{th}, the transistor will be "on" and current will flow from the drain to the source. The equation to calculate the V_{th} is [20]:

$$V_t = V_{t0} + \gamma \left(\sqrt{\phi_s + V_{sv}} - \sqrt{\phi_s} \right) \tag{3.1}$$

where V_{to} is the threshold voltage when the source and the substrate are at the same potential, γ is the body effect coefficient, ϕ_s is the threshold surface potential.

The equation for ϕ_s is

$$\phi_s = 2\upsilon_T ln\frac{N_A}{n_i} \tag{3.2}$$

The equation for γ is

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} \tag{3.3}$$

where t_{ox} is the thickness of the transistor gate oxide, ε_{ox} and ε_{si} are the permittivity of the gate oxide and the silicon, N_A is the acceptor doping concentration and n_i is the intrinsic carrier concentration, which is related to band gap width.

(b) Saturation Current

The saturation current is the current flowing from the drain to the source under certain gate voltage. When the gate voltage is fixed, the current will reach its maximum at a certain voltage between the source and the drain(V_{dsat}), then it will remain the same even the V_{ds}(voltage between the source and the drain) becomes larger. This is because that if the V_{ds} is large enough, the channel will no longer be inverted near the drain, it is called "pinched off" and the resistance of the channel will become bigger with the V_{ds} rising. The saturation current is a key feature that affects the speed of the circuit since it is an indicator of driving capability.

Figure 3.1 shows the typical I-V curve of a MOS transistor, it is evident that after V_{ds} reach as V_{dast}, I_{ds} will stay the maximum at I_{dsat}. The equation for I_{dsat} is calculated as follows [20]:

$$I_{ds} = C_{ox}W(V_{GT} - V_{dsat})\nu_{sat} \tag{3.4}$$

Where C_{ox} is the capacitance per unit area of the gate oxide, W is the width of the channel, $V_{GT} = V_{GS} - V_{th}$, V_{dsat} is the voltage under which the carrier velocity reach its maximum and the current becomes I_{dsat}. In a real device, the channel length variation

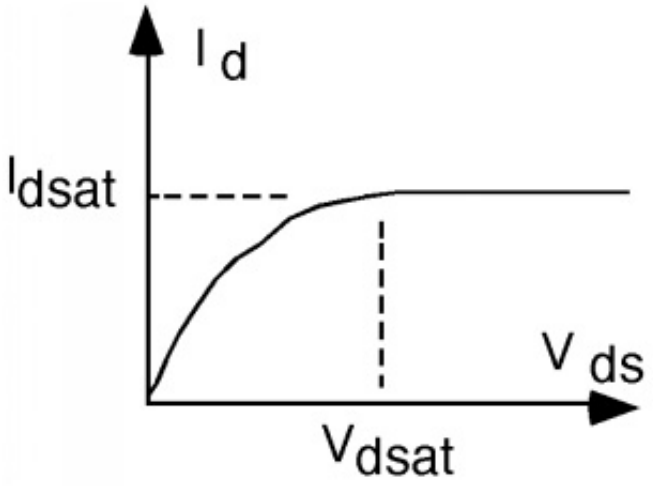


Figure 3.1: CMOS I_{ds} - V_{ds} curve

caused by V_{ds} also has an influence on the saturation current. The shorter channel will result in a larger saturation current, because it is a non-linear relationship between the saturation current and the channel length.

(c) Leakage Current

There is current flowing through the transistor even when the transistor is "OFF". In the past, such leakage current was ignored since it was normally 5 or 6 orders smaller than the saturation current. However, as the transistor size become smaller with the scaling of the CMOS technology, the leakage currents will have to be considered in the total power consumption.

There are mainly 3 kinds of leakage currents:

1. Subthreshold Leakage
2. Gate Leakage
3. Junction Leakage

(c.1) Subthreshold Leakage

The subthreshold leakage is the current flows from drain to source when $V_{gs} < V_{th}$. It is ignored in the MOS transistor model, but actually the current is not zero. The current drops exponentially when V_{gs} decreases. Figure 3.2 shows the I_{ds} - V_{gs} curve with constant V_{ds}, it can be seen that the leakage current drops exponentially when V_{gs} falls below the threshold voltage.

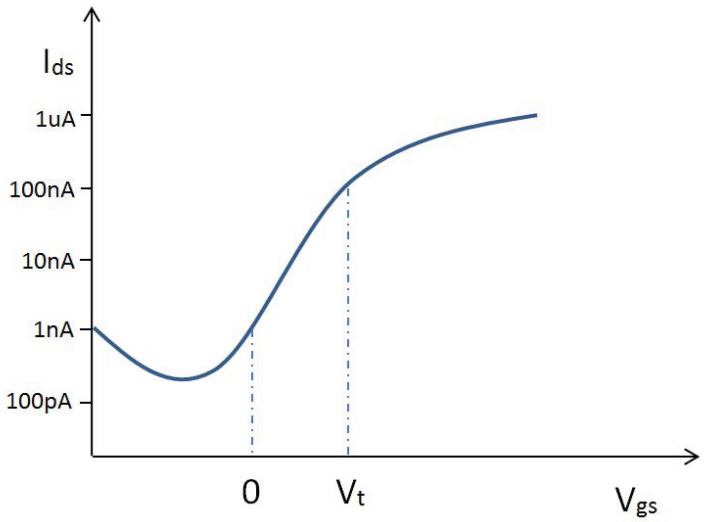


Figure 3.2: I_{ds} - V_{gs} curve with constant V_{ds}

To calculate the subthreshold leakage current, the following equation [20] can be used:

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} V_{t0} + \eta V_{0ds} k_\gamma V_{sb}}{n \nu_T}} \left(1 - e^{\frac{V_{ds}}{\nu_T}}\right) \tag{3.5}$$

where I_{ds0} is the current at the threshold voltage, η is the DIBL coefficient, k_γ is the coefficient related with the body effect, ν_T is the thermal voltage which is in linear with the temperature. This equation shows that leakage is 0 when V_{ds} is 0 and it reaches its full value when V_{ds} is a few times larger of the thermal voltage. Subthreshold leakage depends on the threshold voltage strongly, it exponentially increases as V_{th} decreases. The power consumption could be a problem for circuits implemented low V_{th} transistors.

(c.2) Gate Leakage

There is a leakage current between the gate and the channel, due to the thin gate oxide that are in advanced CMOS technologies. This leakage current is mainly affected by the gate oxide thickness because it drops exponentially as the gate oxide increases.

(c.3) Junction Leakage

The p-n junction between the source/drain and the substrate forms diodes. These diodes are reverse-biased in normal operations, they still conduct a small amount of current. This leakage is mainly dependent on the reverse bias and the doping levels.

3.1.2 Analysis of TSV Induced Effects

The steps to process the TSV and the physical characteristic of the TSV generate mechanical stress. This stress will stretch or squeeze nearby transistors as shown in Figure 3.3:

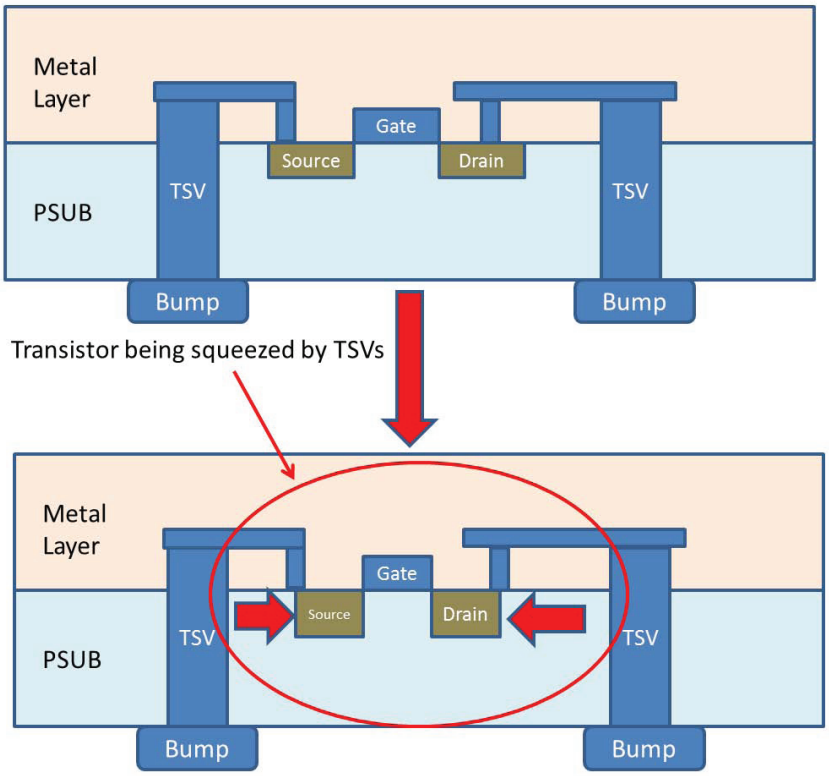


Figure 3.3: TSV stress effect on transistors

The TSV stress is mainly introduced in the processing step because of the difference in the coefficient of thermal expansion(CTE) between the silicon and the TSV material. For example, the CTE of copper is 17(ppm/°C) and silicon is only 3(ppm/°C) [21]. Because of the stress, the material will be distorted and it will change the geometry of the nearby transistor as well as the mobility of the carrier. K. H. Lu evaluated the stress introduced by a single TSV by using a 2D plane-strain analytical solution (Lamé stress solution) [22]:

$$\sigma = -\frac{B\Delta\alpha\Delta T}{2}\left(\frac{R}{r}\right)^2 \tag{3.6}$$

Where σ is the stress, B is biaxial modulus, and $\Delta\alpha$ refers to the CTE difference between TSV material and silicon, ΔT is the differential thermal load, R is the radius of TSV and r is the distance from the center of the TSV.

From equation 3.6, it is clear that the thermal stresses around a TSV is largely dependent on the ratio of the distance to the TSV radius. Stress increases with the square of the TSV radius and decreases the same way as the distance from the TSV increase.

According to the solid-state electronics theory [23], material will have some deformation under stress to keep the balance of force. The deformation will make the distance between atoms change so to change the energy band structure and the band gap.

Based on the TSV introduced stress analysis, Jae-Seok Yang further analyzed the TSV stress effects on the mobility of carriers [24]. The relationship between the mobility change and the applied stress has been proposed by the following equation:

$$\frac{\Delta\mu}{\mu} = -\Pi \times \sigma \tag{3.7}$$

Where Π is the piezo-resistive tensor coefficient and σ is the stress in silicon. Tensile stress results in a positive σ and compressive stress results in a negative σ. The carrier mobility in transistors depends on the distance from the TSV and on the angle between the direction of the stress and the transistor channel. The equation 3.7 can be rewritten for transistors as:

$$\frac{\Delta\mu}{\mu}(\theta) = -\Pi \times \sigma \times \alpha(\theta) \tag{3.8}$$

Where $\alpha(\theta)$ is a directional factor, it is a function of θ which is defined as a degree between the center of TSV and the center of a transistor channel when a transistor is vertically placed as shown in Figure 3.4

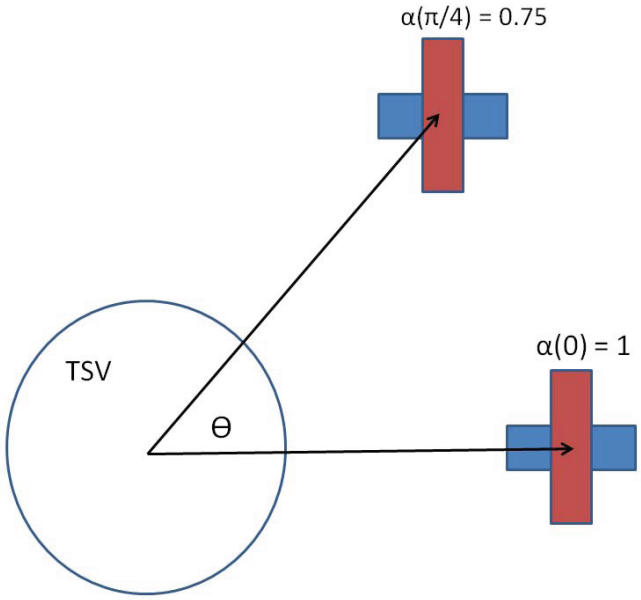


Figure 3.4: Carrier mobility of NMOS transistors under TEV stress

When the transistor is placed in the right of the TSV and θ is zero, the $\alpha(\theta)$ will be 1 which maximize the electron mobility in the transistor. For PMOS transistor, the enhancement of the electron mobility means the reduction of the hole mobility. This means that the maximum hole mobility for PMOS will happen when θ is 90 degree. The situation becomes more complicated when multiple TSV's have effect on one transistor. However, the main point is that the position and channel direction do have an effect on transistor's carrier mobility.

The stress introduced by the TSV will also have effects on the permittivity of dielectric materials, such as silicon dioxide [25] and it has a linear relationship with strain. The deformation of the gate dioxide caused by TSV stress will change its dielectric constant. According to equation 3.1 and 3.3, if the silicon dioxide permittivity changes, the threshold

voltage will consequently change.

The saturation current of the transistor is also influenced by the TSV stress. There is a relationship between parameters mentioned in equation 3.4 and stress. For example, V_{GT} is related to the threshold voltage, transistor width W is directly affected by the TSV stress and ν_{sat} is determined by the carrier mobility which is highly related to the stress discussed before. As a result, the saturation current of the transistor highly depends on the TSV introduced stress.

As equation 3.5 shows, the leakage current is mainly related to the current at the threshold voltage, and at the same time it is also related to the intrinsic carrier concentration, which is indirectly related to the stress.

Since the stress of TSV has so many effects on the transistor electrical behavior, a KOZ must be defined to keep the transistors working properly. Test structures will be used to experimentally measure the transistors near the TSVs so the KOZ can be precisely defined.

3.2 TSV Impact on Digital Circuit

TSVs affect both the transistors' performance and the digital circuits by introducing additional resistance, capacitance and inductance into the interconnection. It is not easy to estimate the TSV impact on digital circuits design, because the TSV model was not available in design kits yet and if a circuit uses TSVs for inter connection, the delays added by TSVs can not be simulated, thus the digital circuit may have timing issue. To study the TSV effects on digital circuits, ring oscillator is a good choice to start with [26] because its simplicity and the TSV impacts can be determined from the change of the output frequency.

A ring oscillator is composed of a chain of inverters, the frequency of it depends on the delay of the inverters and the wire delay. Ring oscillators can be used on 3D-IC to analyze the TSV impact and the thin die impact on digital circuits. The schematic of a typical ring oscillator in 2D-IC is shown in Figure 3.5.

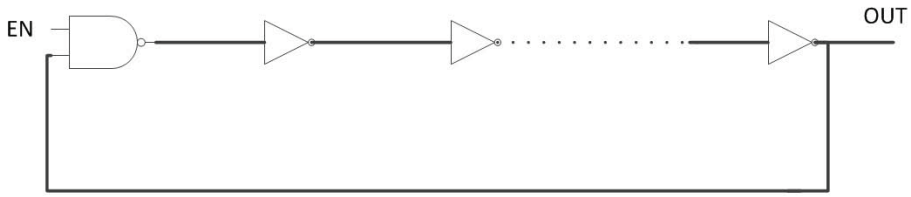


Figure 3.5: Schematic of a ring oscillator

Ring oscillators with different transistor sizes and stages can be implemented together on the 3D-IC test chip. Each set of ring oscillators should be implemented in both dies, with and without TSV. The schematic of ring oscillator used in 3D-IC is shown in Figure 3.6.

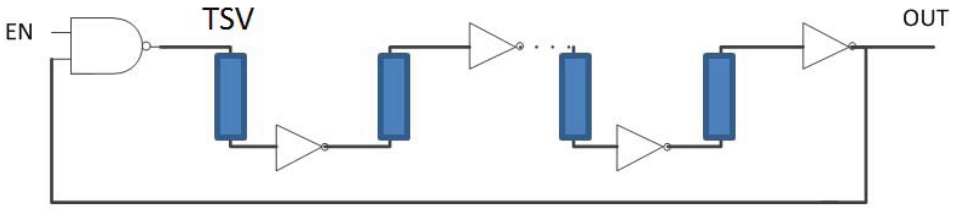


Figure 3.6: Schematic of a ring oscillator used in 3D-IC

By comparing the outputs of the two ring oscillators (Figure 3.5 and Figure 3.6), the difference of the output frequency can be obtained to determine the TSVs' impacts on digital circuits.

4. 3D-IC Thermal Analysis

4.1 3D-IC Thermal Issue

As the feature size becomes smaller, the chip speed becomes faster, as a result, the chip power consumption is much greater than before and the chip generates more heat. Thermal effects cause reliability issue in today's sub-micron ICs. If the heat can not be dissipated efficiently, the increased temperature can cause problems like an increase in leakage currents and reliability degradation.

The key feature of 3D-IC is the stacking of multiple dies; because it affects the power density and the capability of the chips to dissipate heat. A conventional 2D-IC usually has only one die which is comparatively thicker and occupies a relatively larger area than the die of a 3D-IC. It can dissipate the heat easily through the chip surface. A 3D-IC, on the contrary, is composed of multiple dies that are thinned and bonded together in a small volume. The heat generated by the bottom die has to be dissipated through another die. If the heat can not be dissipated fast enough, it will accumulate in the die and generate hot spots which would degrade the performance of the chip. It could damage the chip in the worst case. Thermal issues in 3D-ICs are much more serious than in 2D-ICs. It is very important to characterize the heat dissipation method in 3D-ICs. The heat dissipation method in 2D-IC and 3D-IC is illustrated in Figure 4.1.

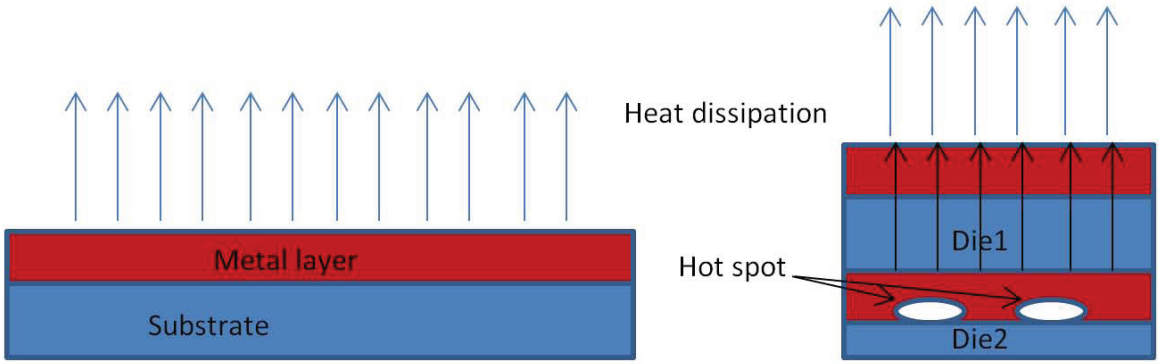


Figure 4.1: Heat dissipation: 2D V$_S$ 3D

Because of the complexity of heat dissipation in 3D-IC, thermal control is now a major challenge in 3D-IC [27]. Accurate characterization of the thermal distribution in 3D-IC is needed to prevent over-heating. Some work is already on the thermal characterization with uniformly distributed power [28] while some researchers are focused on hot spot dissipation [29]. Methods for alleviating the 3D-IC heat problem also have been reported, such as conduction-convection based method [30] and embedded liquid cooling system [31]. Since the biggest thermal problem in 3D-IC is the hot spot, a test structure needs to be developed to characterize the heat dissipation related to hot spot in a 3D-IC test chip. Detailed design is given in Chapter 5.

4.2 Diode Thermal Sensor Principle

In order to accurately characterize the thermal property of the 3D-IC technology, an accurate thermal sensor is needed. Because the die is so small, it is very challenging to put probes directly on it through package, on-chip sensors are needed to measure the temperature. Diodes are widely used as on-chip thermal sensors because they are easily adapted with normal CMOS processing technology and there is a good linearity between the forward voltage drop and the temperature.

For an ideal P-N junction, the forward current I$_F$ and forward voltage V$_F$ has the fol-

lowing relationship:

$$I_F = I_n e^{\left(\frac{-qV_F}{kT}\right)} \tag{4.1}$$

I_n is the reversed saturation current, it can be calculated by

$$I_n = CT^{\gamma} e^{\left(-\frac{qV_{g(0)}}{kT}\right)} \tag{4.2}$$

In this equation, C is a coefficient related to the junction area, doping level and so on. γ is a small constant, $V_g(0)$ is the potential difference between bottom of conduction band and top of valence band which is also a constance for a given material.

Substitute I_n in equation 4.1 with 4.2 and apply logarithm on both side of the equation, equation 4.1 can be rewritten as

$$V_F = V_{g(0)} - (\frac{k}{q} ln \frac{C}{I_F})T - \frac{kT}{q} ln T^{\gamma} \tag{4.3}$$

And because γ is very small, the non-linear part can be neglected if temperature is not too high and equation 4.3 can be rewritten as

$$V_F = V_{g(0)} - (\frac{k}{q} ln \frac{C}{I_F})T \tag{4.4}$$

As shown in equation 4.4, the forward voltage is linear to temperature change. This is the principle of the diode thermal sensor which is used in our thermal sensor design.

5. Test Chip Design

5.1 Design Overview

The test chip designed has two dies. Each single die was designed and simulated in GlobalFoundries' 0.13μm CMOS LP technology which has six metal layers. The 3D integration was done using Tezzaron's SuperContact technology. Two dies are integrated in the chip with "face-to-face" configuration, which means that the metal layers of the two chips will be stuck together and the pads are connected to the interposer through TSVs in the bottom die. Architecture of the 3D-IC test chip is shown in Figure 5.1.

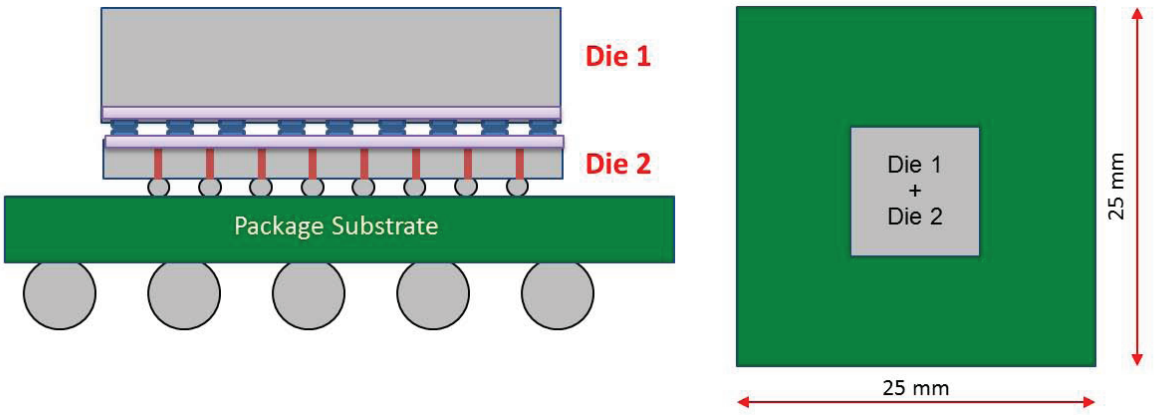


Figure 5.1: Chip package architecture

Die1 and die2 are connected and stack together through mini bumps using metal6. Die2 connects to the interposer by micro bumps using backside metal and the interposer has C4 bumps for package.

The cross section of the die2 with TSVs is shown in Figure 5.2. Figure 5.2 shows that devices are connected by micro bumps. First they are routed to TSVs using five front metal

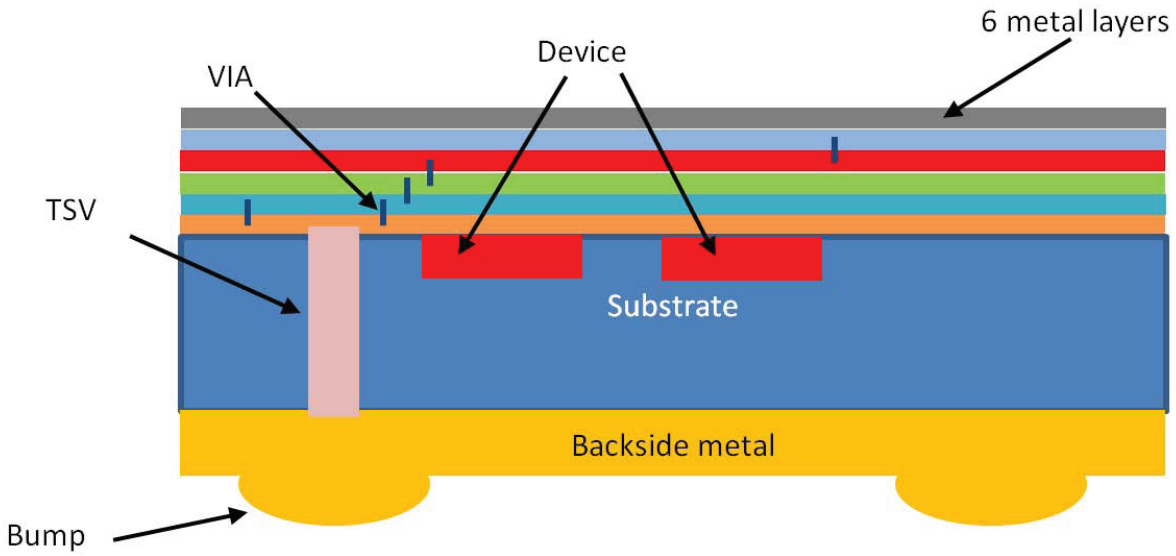


Figure 5.2: Cross section of the die with TSV

layers(the 6th metal layer is reserved for the die connection), through TSVs, they can be routed to bumps with backside metal; the size of the bumps are 100μm by 100μm and the pitch is 250μm which is good to be packaged on the interposer.

Some key properties of the test chip are:

- Chip die size: 3mm $\times$ 3mm
- Interposer size: 25mm $\times$ 25mm
- Die thickness: Chip 1: 600μm; Chip 2: 15μm;
- TSV diameter: 1.2μm, TSV length: 8μm;
- Die 1: Pad size 100μm, bump pitch 250μm
- Die 2: Pad size 100μm, bump pitch 250μm
- Metal layer: 6 + 1 backside meatal
- Power supply: 1.5V
- IO: 105

The chip die size is big enough for implementing all the test structures and other parameters are defined by the vendor.

The test chip contains TSV arrays, transistor arrays, ring oscillators, RF test circuits, heaters and thermal sensor circuits. Brief description of these function blocks are listed as follows:

- TSV array set1: To measure the capacitance, resistance and leakage current of TSV.
- TSV array set2: To measure the transistor leakage near the TSV.
- Transistor array: To measure the saturation current and threshold voltage of transistors at different distance from the TSV to analyze the TSV effects on transistors.
- Ring oscillator: To study how TSVs affect the performance of digital circuits.
- RF circuit: To measure the S parameter of the TSV and study coupling between TSVs, then test some special structures to mitigate the coupling effects.
- Heater and thermal sensor: Mimic the thermal behavior of the real 3D chip, and monitor the temperatures in different places of the chip, both in die1 and die2.

To accurately study the TSV and thin die effect, the same test circuits at the same place are placed in both dies if applicable to make comparison. For example, transistor arrays without TSVs are placed in the top die and transistor arrays with TSVs are placed in the bottom die, the TSV's impacts on transistors can be obtained by comparing the two arrays' outputs. The floor plan of the whole test chip is shown in Figure 5.3 and 5.4.

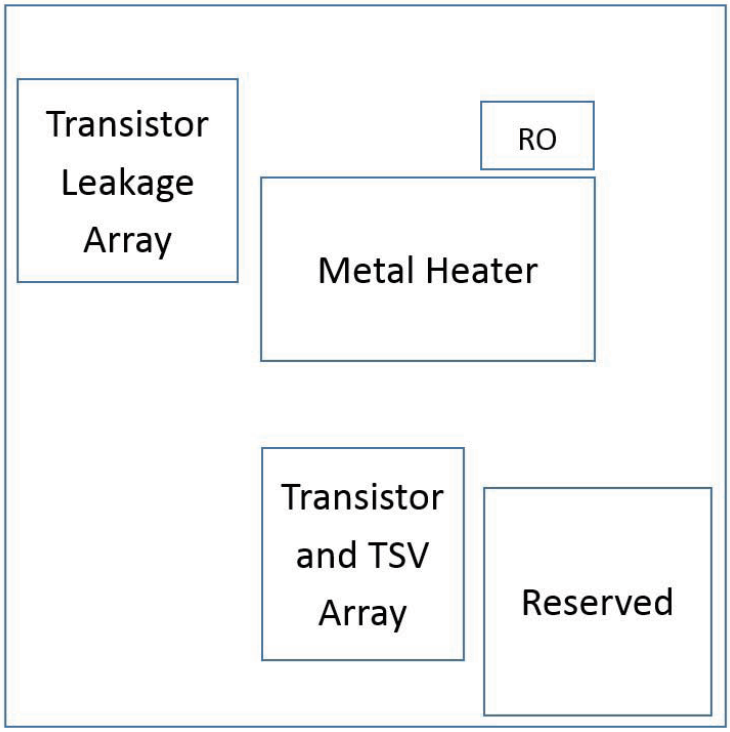


Figure 5.3: Die 1 floor plan

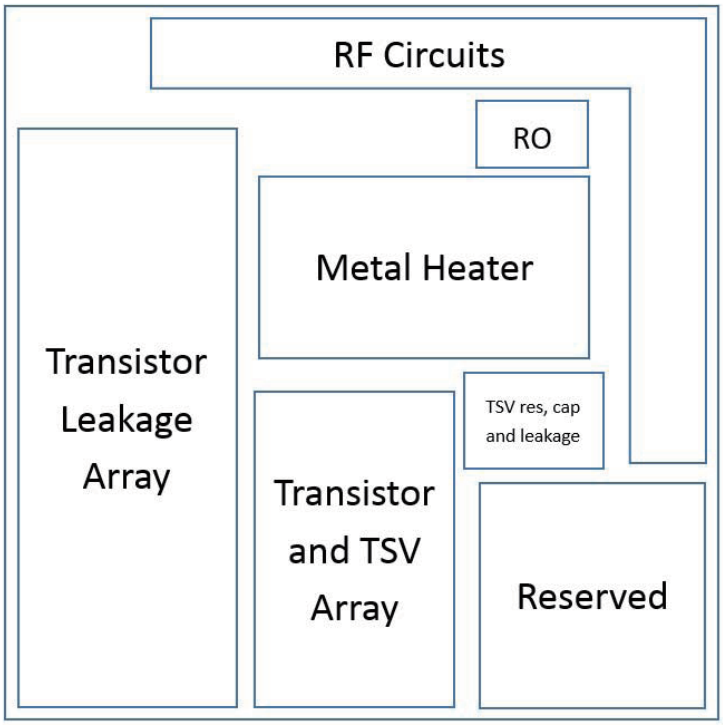


Figure 5.4: Die 2 floor plan

5.2 Detailed Test Block Design

In this section, the detailed test block designs are presented. The working principle of the test circuits are analyzed, schematics and layouts are also displayed.

5.2.1 Test Structure to Measure the Capacitance, Resistance and Leakage Current of the TSV

Capacitance and leakage current of the TSV are measured by one test circuit. Resistance of the TSV is measured by a different test circuit.

(a) Test Circuit for Resistance Measurement

To measure the resistance of the TSV accurately, the test circuit uses Kelvin structure as discussed in Chapter 2. As shown in Figure 5.5, total four pads are used to measure the TSV resistance, two of them will connect to ampere meter and other two will connect to voltage meter in the test.

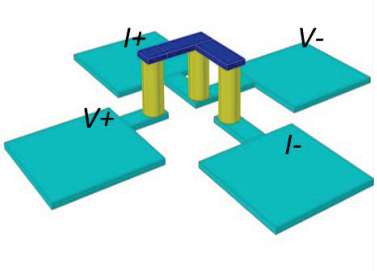


Figure 5.5: Test structure to measure TSV resistance

The final layout of this block is shown in Figure 5.6.

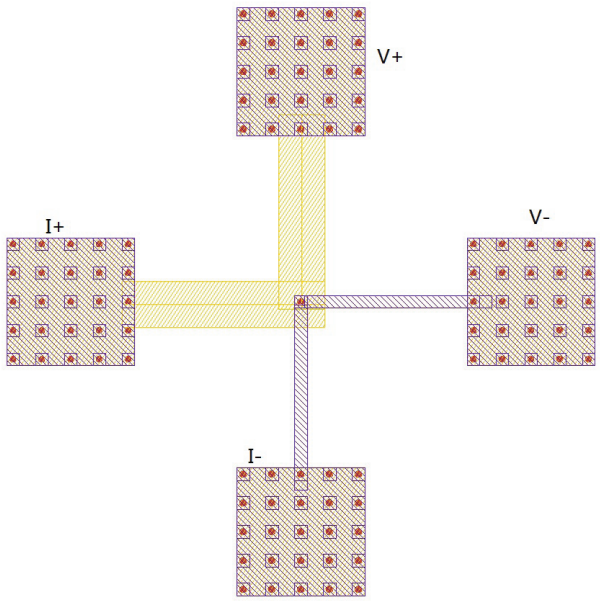


Figure 5.6: Layout of the test structure to measure TSV resistance

Larger pads are used for connecting the circuit to the outside. By connecting voltage meter on the V+ and the V- pads and ampere meter on the I+ and the I- pads, an accurate voltage and current through the TSV can be obtained. Resistance of the TSV can be calculated from I and V values obtained.

(b) Test Circuit for Capacitance and Leakage Measurement

To measure the capacitance of the TSV, an 8 by 8 TSVs are connected together as a TSV array to ensure an accurate measurement of capacitance and leakage. Each TSV in the TSV array is surrounded by a P+ ring, all the TSVs in the TSV array are connected together and all P+ rings are connected together. The test structure is shown in Figure 5.7.

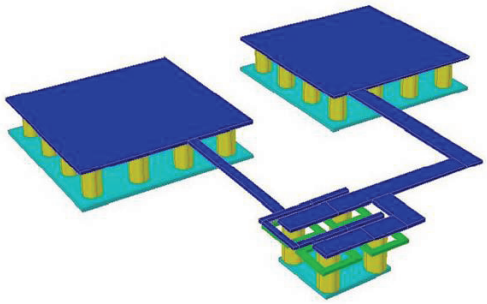


Figure 5.7: Test structure to measure TSV capacitance and leakage current

The final layout of this block is shown in Figure 5.8.

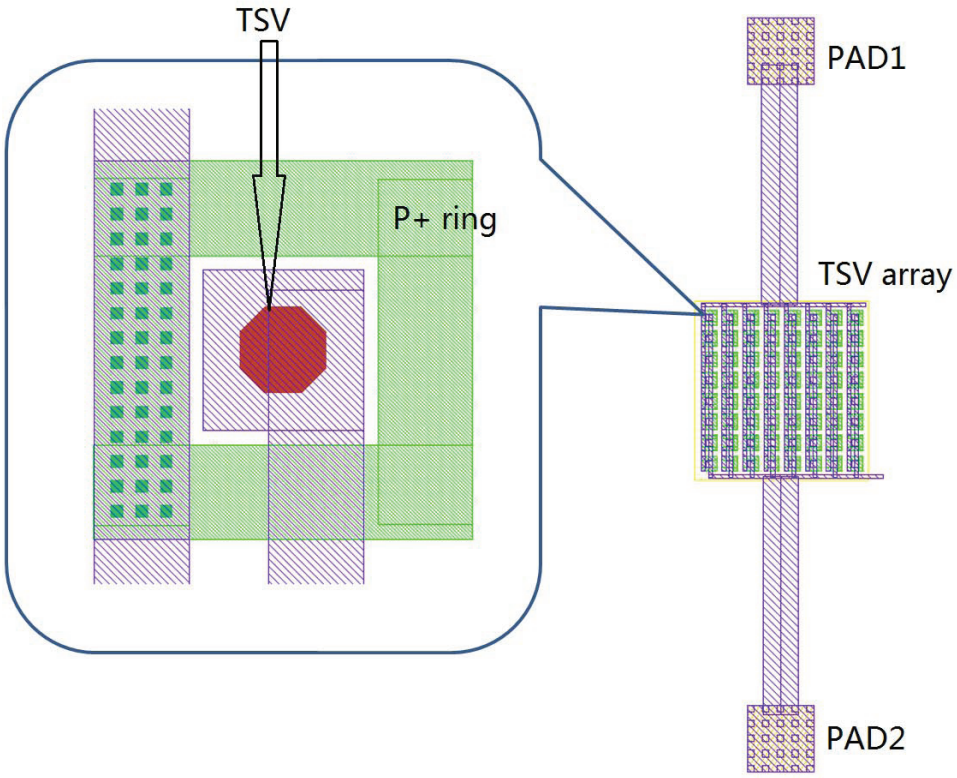


Figure 5.8: Layout of the test structure to measure TSV capacitance and leakage current

All the TSVs are connected to the PAD1 and all the P+ rings are connected to the PAD2, the capacitance between PAD1 and PAD2 consists of the PADs capacitance, wire capacitance and TSV array capacitance. However, the pad and wire capacitance contributions are eliminated by subtracting the value measured on an identical version of the same structure

but without TSVs. The accurate capacitance of a single TSV can be obtained by dividing the final result by 64.

TSV leakage can be found in the same manner. By measuring the current between PAD1 and PAD2 and divide it by 64, the accurate leakage of a single TSV can be obtained.

5.2.2 Test Structure of TSV Array to Measure the Transistor Leakage Near the TSV

As discussed in Chapter 2, the TSV induces an additional stress to silicon devices, such as NMOS transistors and PMOS transistors. This additional stress has an impact on the electrical characteristic of transistor, such as leakage currents that are very important in modern CMOS technologies.

Two sets of test structures are used to measure the TSV impact on leakage currents of transistors. One set of the test structure deals with NMOS transistors and the other set deals with PMOS transistors. In each set, several TSV and transistor arrays which have a different distance between the TSV and the transistor are defined. In the design 20*6 TSV and transistor pairs are used to construct the basic test array. For each PMOS and NMOS test set, five different distances between the TSV and the corresponding transistor are used: 0.7μm, 1.7μm, 3.7μm, 5.7μm, 7.7μm. So there are five NMOS-TSV test structure sets and five PMOS-TSV test structure sets, together there are ten test structure sets. In each test set, the drains, the sources, the gates and the substrates of 120 transistors are connected together. Each test structure has four pads to connect out, drain, gate, source and substrate. By adding different voltages on these pads, I_d can be measured under any V_s, V_{gs}, V_{sb} and V_{ds}. Thus through the I-V plot, the threshold voltage V_{th} and leakage can be obtained.

The final layout of the test circuit is shown in Figure 5.9.

The big red octagon is the TSV, and transistors in this case are very close to the TSV. The surrounding dummy transistors are implemented for immunity fabrication influence:diffusion impact and so on. These are the basic elements of the TSV-transistor pair array. Each array consists of 120 TSV-transistor pairs and there are 10 arrays. Each array has four pads so

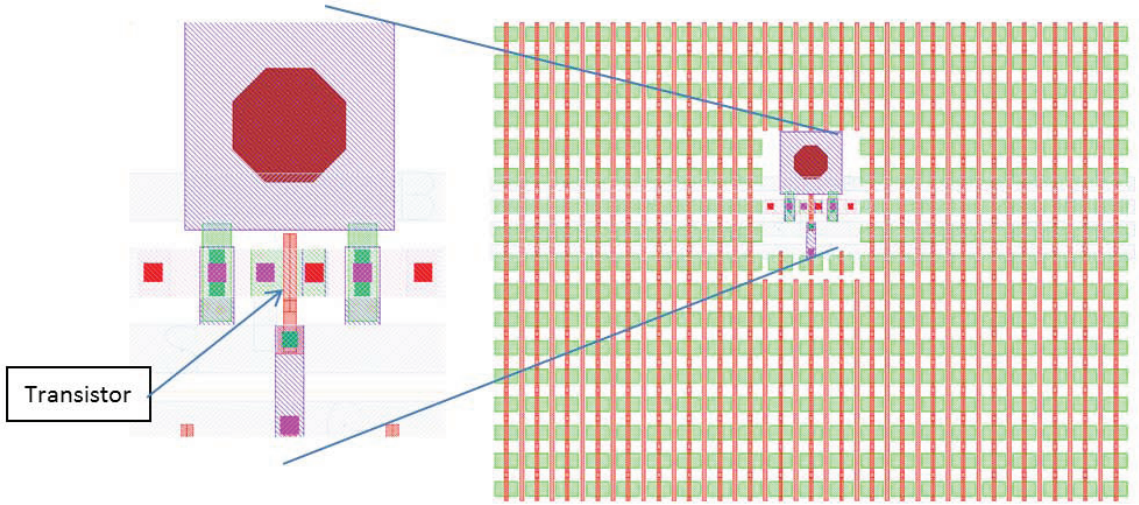


Figure 5.9: Layout of the test structure to measure transistor leakage near TSV

this block will need 40 pads totally.

5.2.3 Transistor Array

In chapter 3 the TSV impacts on nearby transistors are discussed. For the test chip, transistor arrays are used to measure V_{th} and I_{dsat} around TSV, both for nFETs and pFETs.

There are totally 20 transistor arrays implemented, ten of them are NMOS transistor arrays and another ten are PMOS transistor arrays. Each array consists 4 identical Transistor array cells and in each cell at most 16*16 FETs are wired out and others are not connected out.

(a) Description of the Architecture of the Transistor Array Block

The inputs for the transistor array test block are shown in Table 5.1:

Table 5.1: Transistor array inputs definition

Input Name	Description	Usage
D[3:0]	Drain selector	The selected transistor drain is connected to V_d, unselected drains are connected to the ground
G[3:0]	Gate selector	The selected transistor gate is connected to V_g, for unselected NMOS transisor gates, it ties to the ground; for unselected PMOS transisor gates, it ties to the Vdd
S[4:0]	Array selector	The transistors' sources in seleceted transistor array are connected to V_s, all transistors' sources in unseleceted transistor array are connected to Vdd
V_d	Connect to I/O PAD V_d	Supply the drain voltage and measure the drain current
V_g	Connect to I/O PAD V_g	Supply the gate voltage
V_s	Connect to I/O PAD V_s	Supply the source voltage

The architecture of the transistor array is shown in Figure 5.10.

The Drain Select Blocks has five inputs: D[3:0] and V_d; 16 outputs V_d[15:0]. By using a 4-16 decoder and some switch cell, the output selected by D[3:0] is connected to the input V_d, the other 15 output are connected to the ground. The outputs of the Drain Select Blocks connect to the 20 transistor array block directly.

The Array Select Block has six inputs: S[4:0] and V_s; 20 outputs V_s[19:0]. By using a 5-32 decoder and similar switch cells as used in the Drain Select Blocks, the output selected by S[4:0] is connected to the input V_s, other outputs are connected to the Vdd. Each of the outputs connects to a V_g Select Block accordingly.

There are total 20 V_g Select Blocks. Each V_g Select Block has six inputs: G[3:0], V_s[i](i means it is the ith V_g select block) and V_g; 16 outputs V_g[i][15:0]. By using a 4-16 decoder

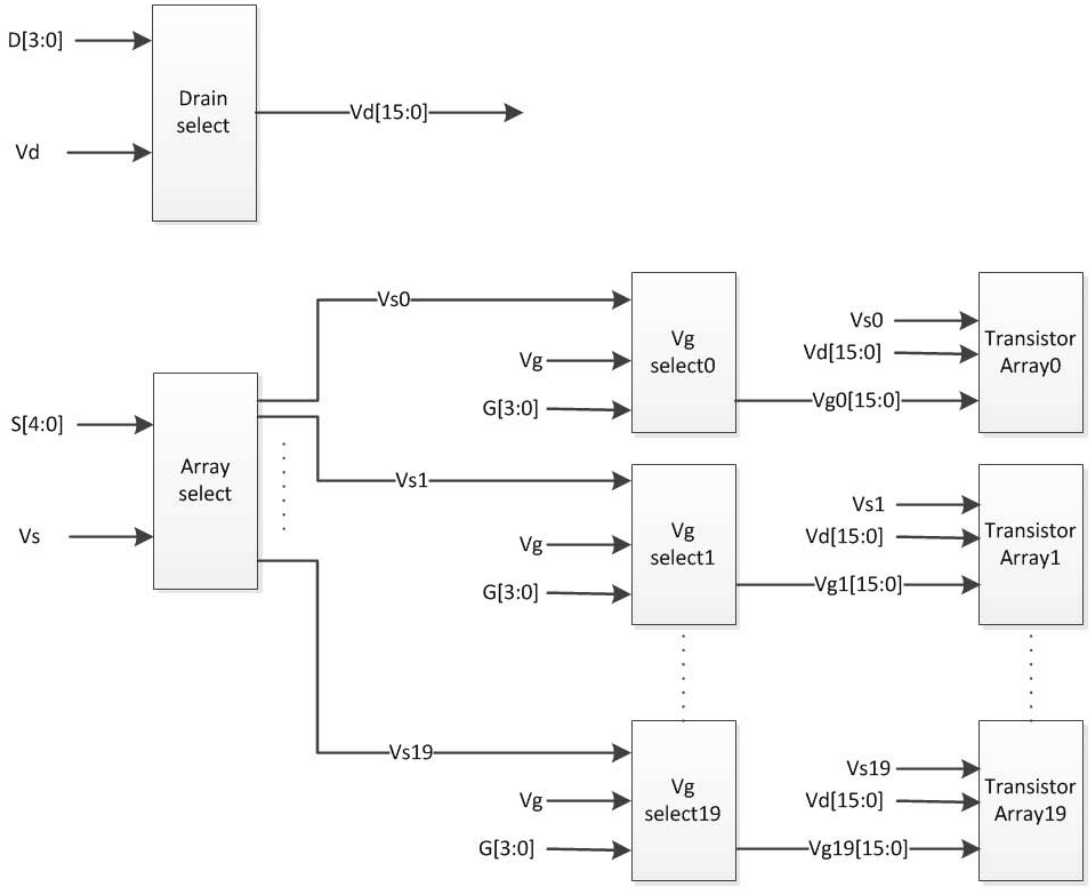


Figure 5.10: Architecture of the transistor array test circuit

and similar switch cells as used in the Drain Select Blocks, the output selected by G[3:0] is connected to the input V_g if the input V_s[i] is low, other outputs are connected to the Vdd. If the input V_s[i] is high, the array is unselected and all the outputs are high. Each V_g Select Block connects to the corresponding transistor array block directly.

There are total 20 transistor arrays. The arrays have at most 31 inputs, V_d[15:0] from the Drain Select Block, V_g[i][15:0] from V_g select block and V_s[i] from the array select block. The number of inputs is various depending on the number of transistors in the transistor array cells. The drain, gate and source of the transistors selected by the V_d[15:0], V_g[i][15:0] are connected to the input V_d, V_g and V_s, thus the I_d-V_g or I_d-V_d curve can be measured and plotted to get the saturation current and the threshold voltage.

(b) Transistor Array Cell

Each transistor array is composed of four identical transistor array cells which are connected in parallel. If the array is selected, the same transistor in each array cell will be selected simultaneously and the current will be the sum of the four transistors, thus it makes the current larger and more accurate for measurement. There are ten different configurations for transistor arrays. Detailed configuration is shown in table 5.2.

Table 5.2: Transistor array configurations

Gate length	Wired out transistor number	Cell pitch (μm)	Configuration
500nm	47	10	Square
130nm	75	10	Square
500nm	190	20	Square
130nm	250	20	Square
500nm	30	10	Line
130nm	75	10	Line
500nm	190	20	Line
130nm	250	20	Line
500nm	190	40	Square
130nm	250	40	Square

The layout for the transistor array cell is shown in Figure 5.11 where the transistor gate length is 500nm and array configuration is square. The red octagon in the middle is the TSV, transistors with vias on drain and source are wired out and others are dummy. The selected transistor's drain connects to the V_d, source connects to the V_s and gate connects to the V_g. Thus the I-V curve of the transistors with different distances and angles to the TSV can be measured from the outer pads.

There are also two configurations for the transistor array to place the cell arrays, namely, line and square configurations. Each array configuration has four array cell elements. The layout of the line configuration is shown in Figure 5.12. The layout of the square configuration

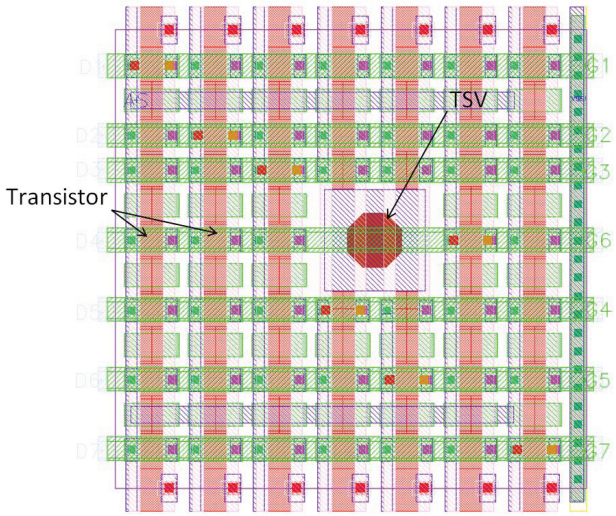


Figure 5.11: Array cell with 500nm gate length and square configuration

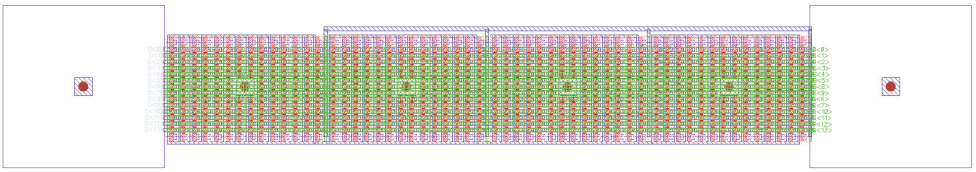


Figure 5.12: Transistor array with line configuration

is shown in Figure 5.13

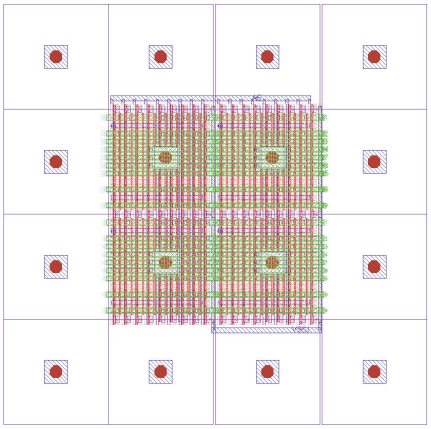


Figure 5.13: Transistor array with square configuration

Different TSV placement will also have different impact on nearby transistors. It can be verified that which placement has smaller effects on transistors by testing these two different

configuration.

(c) Decoder and Switch Cell

4-16 and 5-32 decoders are used to generate the enable signals for the signal switch cells. 4-16 decoders are used in the Drain Select Block and the Gate Select Block, while 5-32 decoders are used in the Array Select Block. The decoders implemented in this design are one leveled. They decrypt the 4 or 5 bits input and make the corresponding output enable signal high which will enable the transmission gate in the switch cell.

The schematic of the 4-16 decoder is shown in Figure 5.14, 5-32 decoder has the similar structure.

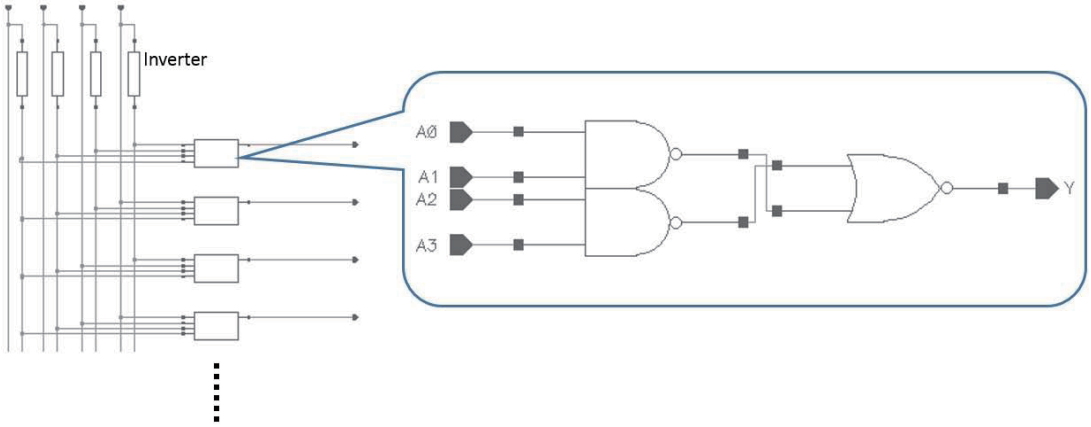


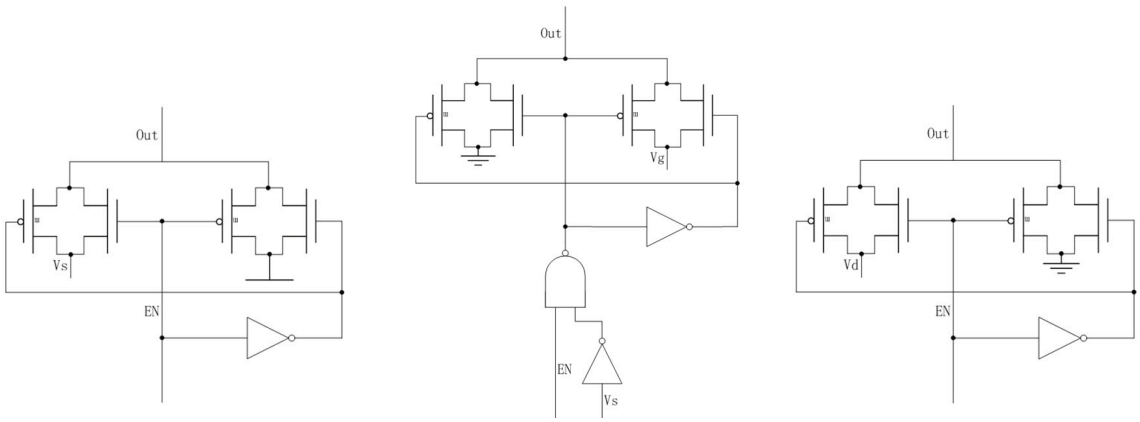
Figure 5.14: 4-16 decoder design

Each decoder output connects to a switch cell which is like a transmission gate. There are three kinds of switch cells, Switch cell-V_s, Switch cell-V_d and Switch cell-V_g. The cell functions are shown in Table 5.3.

Table 5.3: Switch cell function

Cell Name	En (Gate Select)	V_s (Array select)	Out
Switch Cell - V_s	1	N/A	V_s
	0		Vdd
Switch Cell - V_d	1	N/A	V_d
	0		0
Switch Cell - V_g (NMOS)	1	0	V_g
		1	0
	0	X	
Switch Cell - V_g (PMOS)	1	0	V_g
		1	1
	0	X	

The schematic of switch cells are shown in Figure 5.15



(a) Switch cell - V_s (b) Switch cell - V_g (c) Switch cell - V_d

Figure 5.15: Switch Cells

Figure 5.16 shows how the switch cells control the transistor connection. The big transistor symbol in the center is a transistor in the transistor array cell to be tested. Once the transistor is selected, the drain, source and gate are connected out through switch cells.

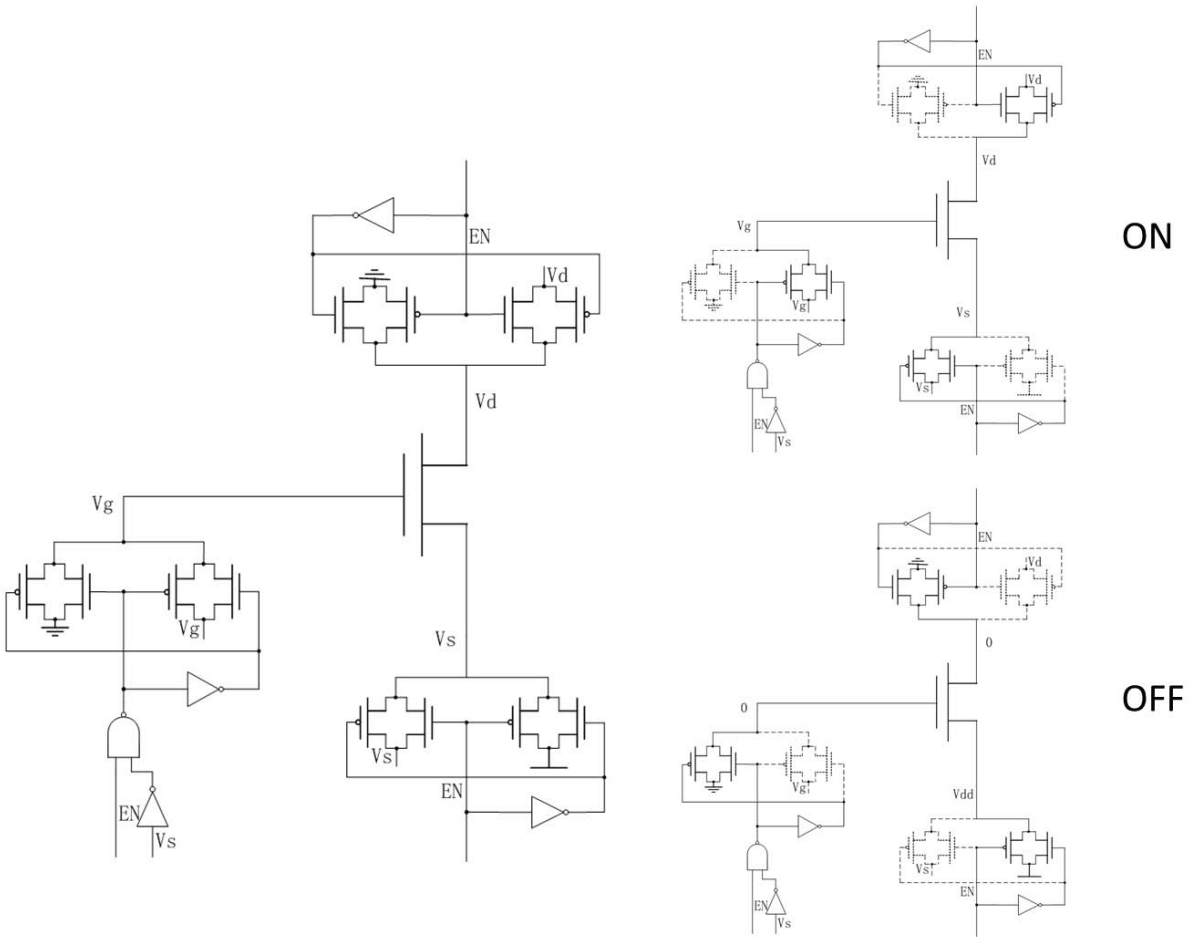


Figure 5.16: Switches for the transistor array

(d) Design Consideration

To accurately measure the current and voltage on the transistors, the voltage drop through the transmission gate needs to be carefully considered, that is the reason V_g control block is added. If the V_g control block is not added, the transistor array block should also be functional. The reason is that even all the drains and gates of transistors that are in the same place of the different arrays are connected together, their sources are connected differently. For example, the transistor in row 1 and column 1 in the first array is connected with the transistor in row 1 and column 1 in the second array, but their sources are connected differently. The sources of the transistors in the selected array are connected to the pad V_s while in the unselected array they are connected to the Vdd. The I_d can be found out

by measuring the current on the V_s pad. As there is no V_g control block, space is saved. However, the simulation result shows that there's a problem in this design caused by leakage currents which made it almost impossible to read out the accurate I_d from the V_s pad.

The problem is caused by the limited driving capability of the transmission gate. Without the V_g control block, for unselected arrays, the sources of the transistors are tied to ground while the unselected drain are tied to Vdd. Since the column of the array is selected by V_g and the row of the array is selected by V_d, the transistors on the same column with the selected V_g will also be on. The V_d is connected to the arrays through a transmission gate, if it supplies the drain current to too many transistors, the voltage output through the transmission gate will drop dramatically. As the result, it is impossible to supply the correct voltage on the selected transistor's drain. In the end, we added the V_g select bolck and solved the problem.

5.2.4 Ring Oscillator

The ring oscillator is an important part of the test chip. It is used not only to study the TSV impacts on digital circuits but also to validate the RC model of the TSV and the thin die effects on the 3D-IC technology. The basic schematics for ring oscillators in both traditional 2D-IC and in 3D-IC were introduced in chapter 3. In the real design, the schematic of the ring oscillator implemented with TSV interconnection needs to be changed to adapt to the designed test chip because there is no device layer on the backside of the bottom die and TSVs are only used to connect the IO to the package. In order to use TSVs as interconnection in this case, connection wires are routed to the backside of the die and then routed back to the front through TSVs. The schematic of the ring oscillator with the TSV connection is shown in Figure 5.17.

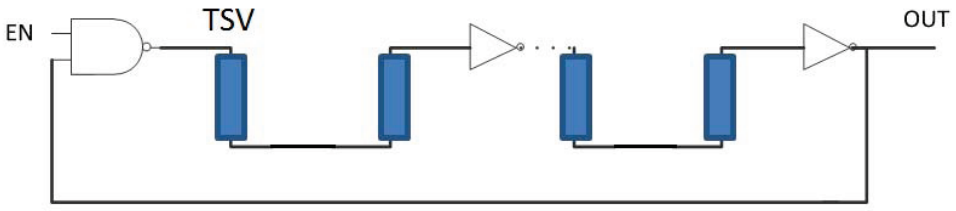


Figure 5.17: Schematic of the ring oscillator with TSV

The ring oscillator designed for the test chip has 21 stages and the output is connected to a 256 frequency divider. The reason for using the frequency divider is that the ring oscillator's frequency is too high to be measured accurately. The inverters are placed $40(\mu m)$ away from the TSV to minimize the effects of the TSV on the performance of the transistors. The layout of the ring oscillator using TSV as interconnection is shown in Figure 5.18.

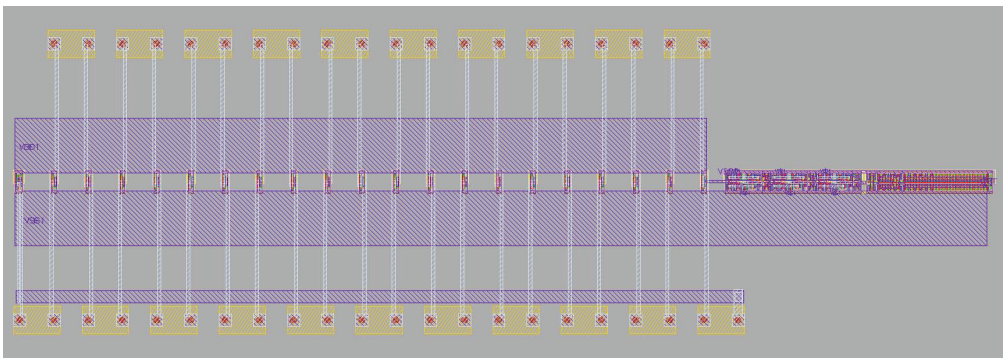


Figure 5.18: Layout of the ring oscillator with TSV

The ring oscillator without the TSVs is also implemented for comparison purpose. It has exactly the same size as the ring oscillator with the TSVs but removed the TSVs and connected the inverters with metal layer 2. In total, there are three ring oscillators implemented: on the top die: 21 stages RO without TSV; on the bottom die: 21 stages RO with and without TSV. By comparing the frequency of the RO from the top die and the frequency from the bottom die without TSV, the die thinning effects for digital circuits can be obtained; by comparing the frequency of the RO with TSVs and without TSVs from the bottom die, the TSV effects on digital circuits can be obtained and to the RC model we set up previously can be validated.

(a) Frequency Divider

The frequency divider is used to divide the output frequency of the ring oscillator by 256. To achieve a stable output frequency, we choose the True Single-Phase Clock(TSPC) type nine-transistor D-FF [32] as the divede-by-2 frequency divider. This type of flip flop uses dynamic logic which means that each internal output is stored on parasitic device capacitance during operation. Therefore it consumes less power and is suitable for high frequencies. The transistor sizes can be adjusted according to [33]. The schematic of the frequency divider is

shown in Figure 5.19. The simulation result shows that it gives an accurate output.

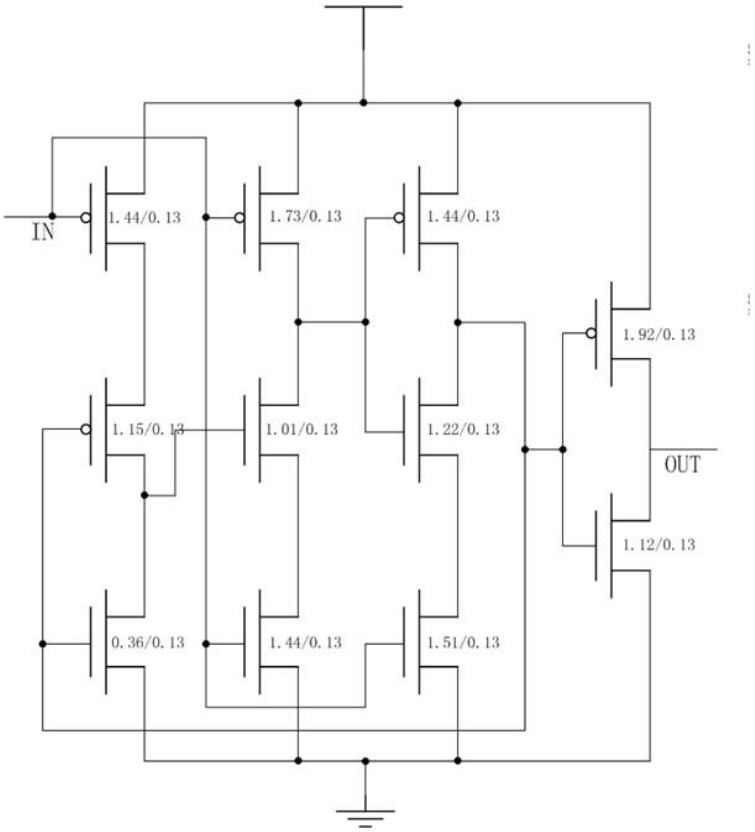


Figure 5.19: Schematic of the frequency divider by 2

By connecting six of the TSPC frequency divider in series, the accurate frequency divided by 256 can be obtained. The direct output frequency of the RO is 7GHz and the divided frequency is about 27MHz which is low enough for accurate measuring from external of the chip.

5.2.5 RF Test Circuits

The RF test circuits in this test chip, as mentioned in Chapter 2, are designed for measuring the S-parameters of the TSV and determine the coupling between TSVs. The schematics for the test circuits were given in Chapter2. The layout and implementation are discussed in the following sections.

(a) Test Circuit for S-parameter Extraction

The S-parameter extraction requires two sets of distances, with and without the TSV. Figure 5.20 shows the layout of the S-parameter extraction circuit with the TSV distance of 100μm.

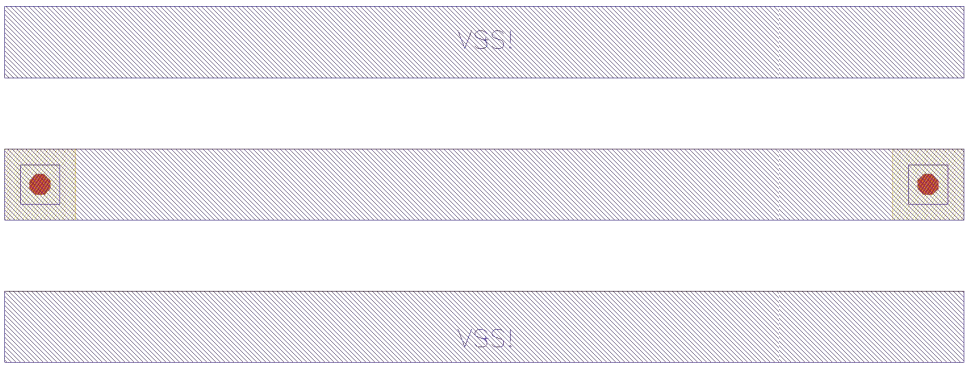


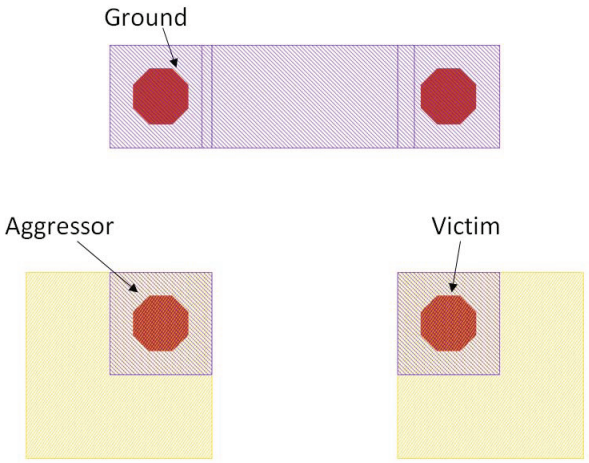
Figure 5.20: Layout of the S-parameter extraction circuit

The other test circuits for S-parameter extraction are similar, the distance of two ports is 300μm. By measuring the four sets of S-parameters between two ports (S_{11} and S_{21} for each set), the S-parameter of the TSV can be extracted by using the one-side TSV S-parameter extraction method discussed in chapter 2.

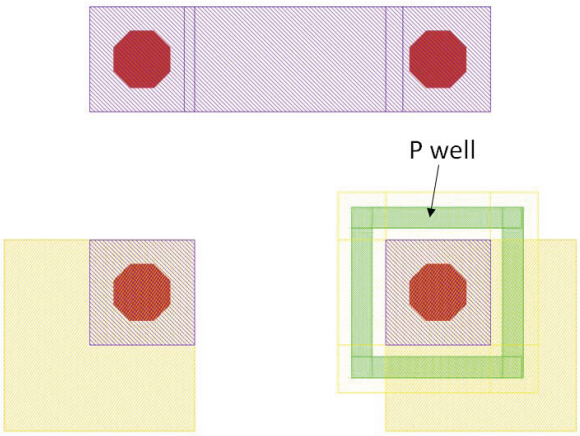
(b) TSV Coupling Test Circuit

There are three test structures for the TSV coupling measurement. The layout of the test structures are shown in Figure 5.21.

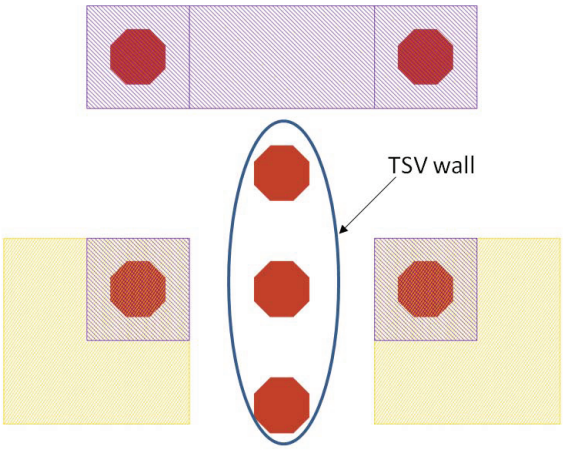
The pitch of the TSV is 6.2 μm which is the minimum pitch defined by the Tezzaron 3D-IC technology. The aggressor is connected with the signal, the victim is floating, and the coupling voltage can be measured to determine the coupling between the TSVs. With the three sets of the TSV coupling test circuits, the coupling coefficient between the two TSVs can be measured. In additional, the efficiency of the two TSV coupling reduction methods can be verified: TSV guarding and TSV wall. Another set with TSV pitch 10 μm is also implemented to study the distance effects on TSV coupling.



(a) Basic TSV coupling circuit



(b) TSV coupling circuit with guard ring



(c) TSV coupling circuit with TSV wall

Figure 5.21: Test circuit for TSV coupling

(c) Implementation

RF test circuits need to be well implemented and all ports need to be wired out properly so we can attach the probes of the network analyzer on them and conduct the testing. This RF test block needs a total of 34 pads, 16 of them are for signal and other 18 pads are for ground. The ground pads are needed because the test probe is a three pin probe with ground-signal-ground configuration. The pad size is 50μm and the pitch is 150μm. The signal pads are listed in table 5.4. Ports are routed to the pads using backside metal.

Table 5.4: Signal pads needed for RF block

Block	pads
S-parameter	8
TSV coupling	4
TSV guarding	2
TSV wall	2

5.2.6 Heater and Thermal Sensor

In chapter 4, the 3D-IC thermal issue and the principle of the diode thermal sensor were analyzed. In this chapter, the detailed design is given. Through the heater and thermal sensor circuits, the heat dissipation capabilities of conventional 2D chip versus 3D chip are compared. Two major work was done, heat generation and temperature measurement.

(a) Heater

The metal heater is used in the test chip to raise the temperature. The heater is implemented with metal 2. It is composed of 16 heater cells connecting in parallel. Each cell is formed by a 5μm wide metal and it is routed to be a square. The typical resistance of metal 2 is 55mΩ/sq, accordingly, the resistance of the heater cell that can be calculated becomes 32.725Ω. Since the 16 heater cells are connected parallel, the total resistance of the heater is about 2Ω. By adding proper voltage on it, we can get the heating power by

$$P = \frac{V^2}{R} \tag{5.1}$$

Assuming the voltage is 5V, then the heating power is 12.5W. The layout of the heater is shown in Figure 5.22

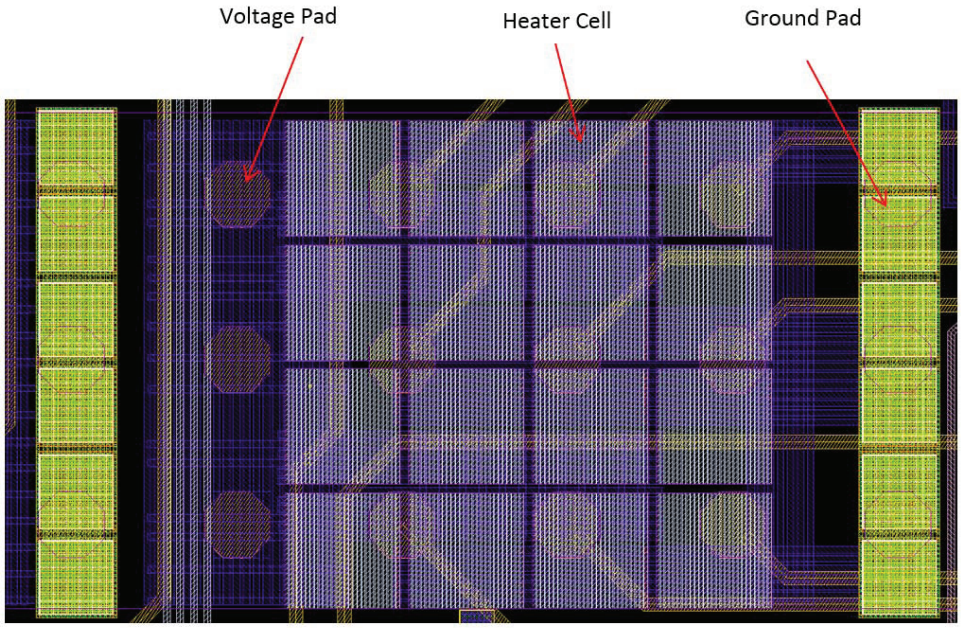


Figure 5.22: Layout of the heater

(b) Thermal Sensor

The thermal sensor implemented in the test chip is diode sensor which was introduced in Chapter 4. In order for the diode to act as the thermal sensor, the forward current I_F should be a constant so the forward voltage V_F is linear to the temperature. Normally this current can be supplied from outside by a current supplier. However forward current I_F should be as small as possible to make the voltage change range bigger. Therefore, an internal current source is used to provide the small forward current. This current is generated by a current mirror circuit. The schematic of the diode sensor is shown in Figure 5.23.

Diode sensors designed in this project only need one pad to measure the voltage while those in other designs [34] [35] need more pads to supply a frequency input or a differential input. This is very important for the design since our test chip is I/O limited so it can

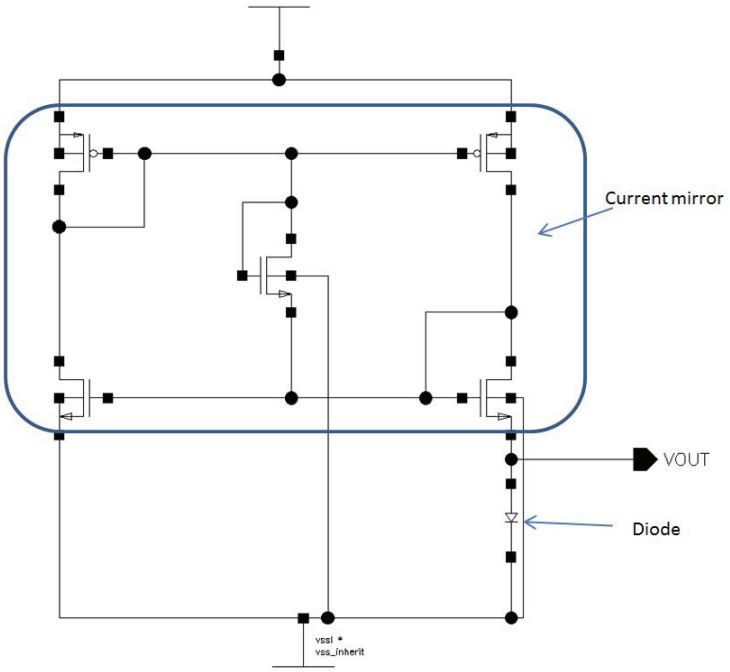


Figure 5.23: Schematic of the diode temperature sensor

implement more sensors at various places to measure the thermal dissipation. The layout of the thermal sensor is shown in Figure 5.24.

The diode size designed is 20μm by 50μm considering the area it occupies and the output voltage range of it for measurement. The gradient of the forward voltage change by temperature is about -2.09mV/K. The results of the temperature simulation can be found in Chapter 6.

5.3 I/O Pads and ESD Design

The I/O pads are very important parts of the test chip, they both connect the pins of inner blocks to outside and provide the ESD protection to the whole chip. In this section, analysis of the I/O requirements is made. Design of I/O pads with ESD protection is made. Normally, the I/O pads are provided by the design kit. But in this case, the pads from the kit are not suitable. The reason is that most of the inputs and outputs in our test chip are analog signals and all the devices we used are working under 1.5V while the analog pad provided by the kit is working under 3.3V. They are not compatible so we need to design

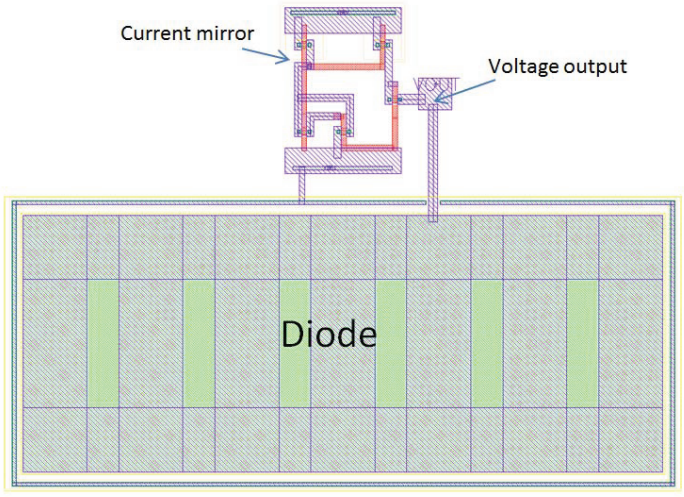


Figure 5.24: Layout of the diode temperature sensor

our own I/O pads for inputs and outputs. The power pads from the design kit can be used by adding TSVs on them.

5.3.1 ESD Design

The ESD is the sudden flow of electricity between the two objects caused by contact [36]. For micro chips, it can generate very large current and flow through the chip pin in a very short period of time and damage the inner circuits. There are several discharge modes for ESD [37] that are defined as follows: I/O to VDD positively and negatively(PD and ND),I/O to GND positively and negatively(PS and NS), VDD to GND(DS). ESD protection circuits are needed to protect the circuits from these ESD circumstances.

Diodes are widely used in the ESD protection circuits. The schematic of the basic diode protection circuit is shown in Figure 5.25.

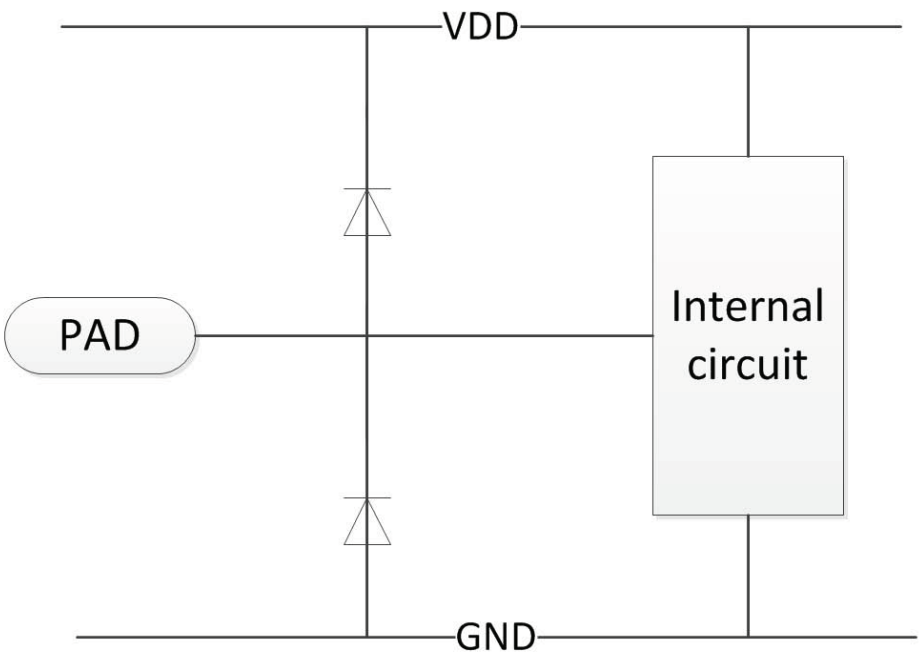


Figure 5.25: ESD protection using diode

The basic principle of the diode ESD protection is simple. When ESD occurs, the voltage between the PAD and the VDD or GND will be high enough to turn on the diode and the charge will flow to the VDD or VSS through the diode. Therefore, little current will go into the internal circuit; furthermore, the voltage on the pad will be clamped to the VDD plus the diode forward voltage which is about 0.6V. By implementing the diodes in the I/O pads, it can provide ESD protection to our inner test blocks.

5.3.2 Pad Cell Design

The pad frame supplied by the kit was revised by adding mini bumps to cover the pad cell for die stacking and connection. In addition, TSVs were added to the pad so it can be connected to the backside metal and routed to the micro bump. The pad cell we designed can be used both in wire bonding and flip chip package; it also contains diodes to provide ESD protection. The layout of the pad cell is shown in Figure 5.26. The size of the pad cell is 90μm by 210μm,

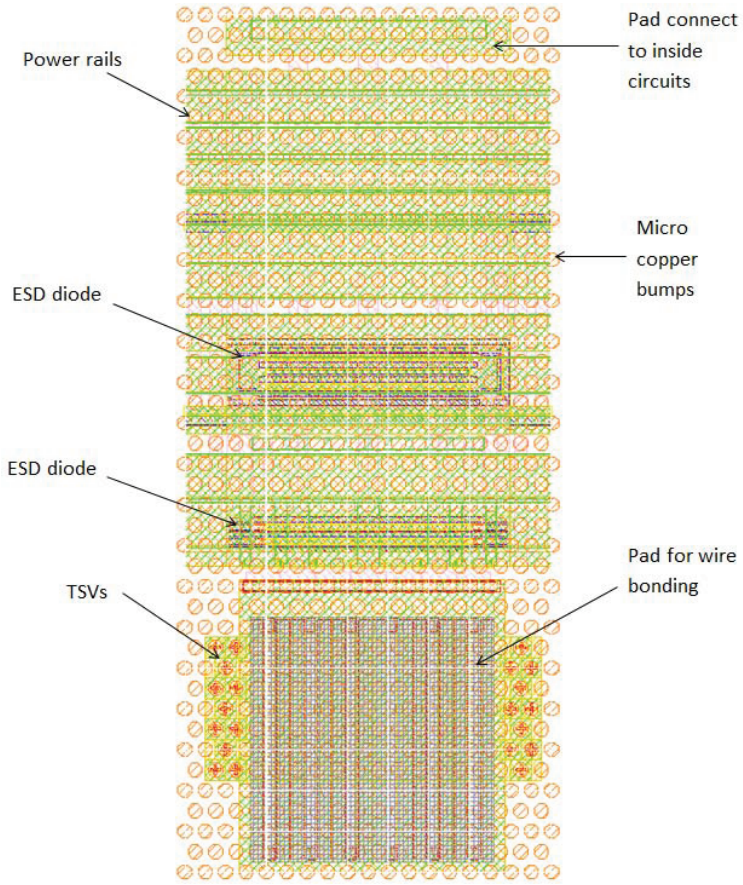


Figure 5.26: Pad layout

5.4 Chip Integration

After all the test blocks and the pad cells are done, the final step is to put them together and route the block pins to I/O cells then to the bumps through the backside metal. Two dies are stacked together using mini copper bump (size 3.4μm by 3.4μm, octagon shape) array implemented with metal 6.

Figure 5.27 shows the evenly distributed metal 6 copper bump array for die stacking, both dies have the exact same bump array configuration so they can attach to each other and stick together.

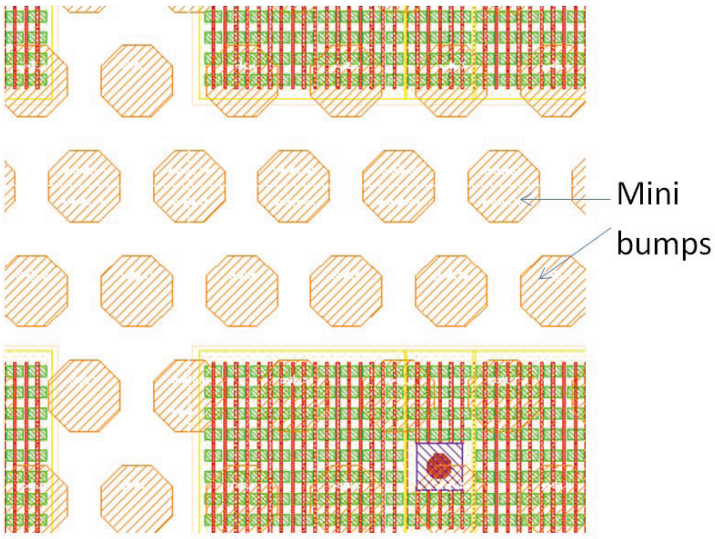


Figure 5.27: Mini copper connection bump array

The final layout of die1 and die2 are shown in Figure 5.28 and Figure 5.29.

Die2: The right bottom 1mm by 1mm space is reserved for other's design. The upper and right sides with different pads are for RF testing. The big block in the center is the heater, left side is TSV arrays to measure the transistor leakage, the block in the bottom is the transistor array to measure the I-V curve, other test blocks are distributed in the space between these blocks.

Die1: The up left corner is TSV arrays to measure the transistor leakage, the big block in the center is the heater, the block in the bottom is the transistor array to measure the I-V curve, other test blocks are distributed in the space between these blocks.

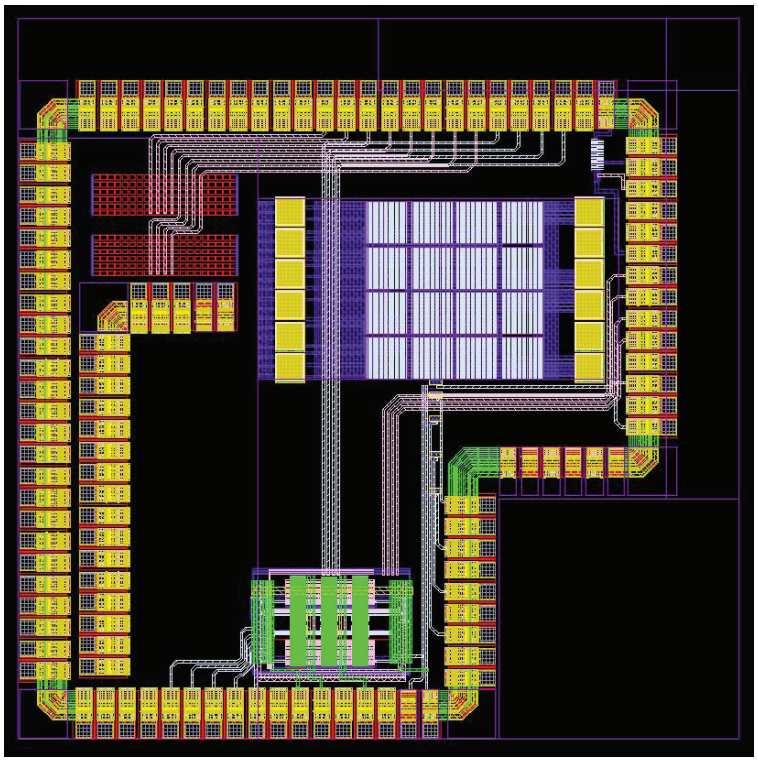


Figure 5.28: Die1 layout

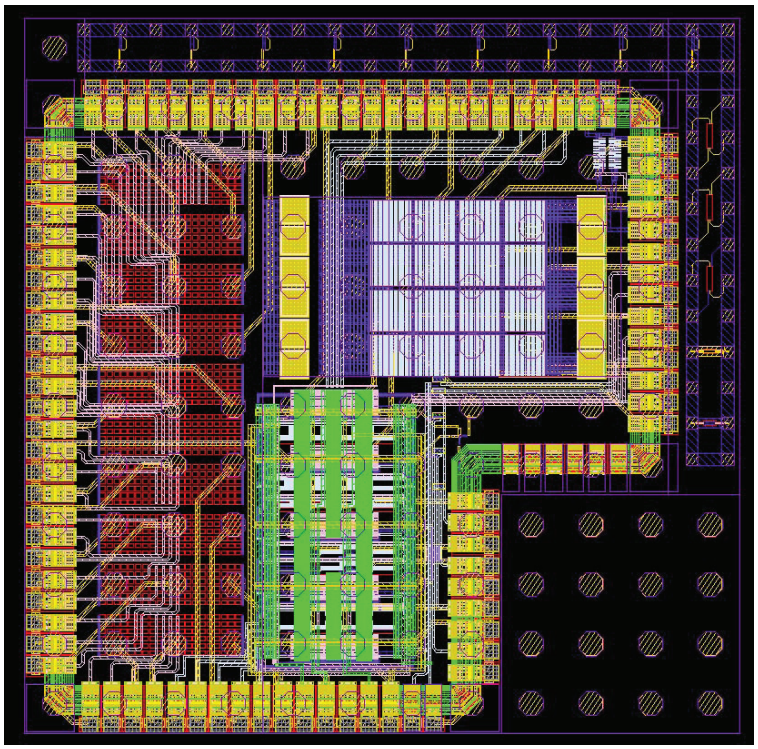


Figure 5.29: Die2 layout

6. Simulation and Verification

To verify the design, simulations are carried out to check and rectify errors. Schematics (TSV array to measure transistor leakage, transistor array, ring oscillator and thermal sensor) are developed and simulated in Cadence with device models provided by Global Foundary 130nm kit. After verification, the layout was finalized accordingly. DRC (Design Rule Check) and LVS (Layout Versus Schematic) were performed to make sure the layout is the correct representation of the schematic and meet the fabrication requirements. The post-layout simulation was done with the consideration of additional parasitic resistances, capacitances and inductances. Other test blocks (TSV array to measure resistance, capacitance and leakage, RF circuit) were focused on the basic electrical characters. Since there is no TSV model available from the kit, it needs to be set up and simulated. The TSV leakage current was simulated in the Sentaurus TCAD while RF circuits were simulated with the HFSS.

6.1 Circuit Simulation

In order to verify the functionality of the designed test circuits, circuits simulation were carried out using Cadence Virtuoso Artist Analog Design Environment(ADE) tools. The simulation results were verified to be correct and could be used for comparison with the real chip test results.

6.1.1 TSV Array to Measure Transistor Leakage Current

To verify the test circuit to measure transistor leakage works, one group of transistors were simulated in the top die without TSV. After the fabrication of the test chip, comparison will be made between simulation and measured results of the TSV arrays in the top and bottom

die. The simulation result of a typical I_d-V_g curve is shown in Figure 6.1.

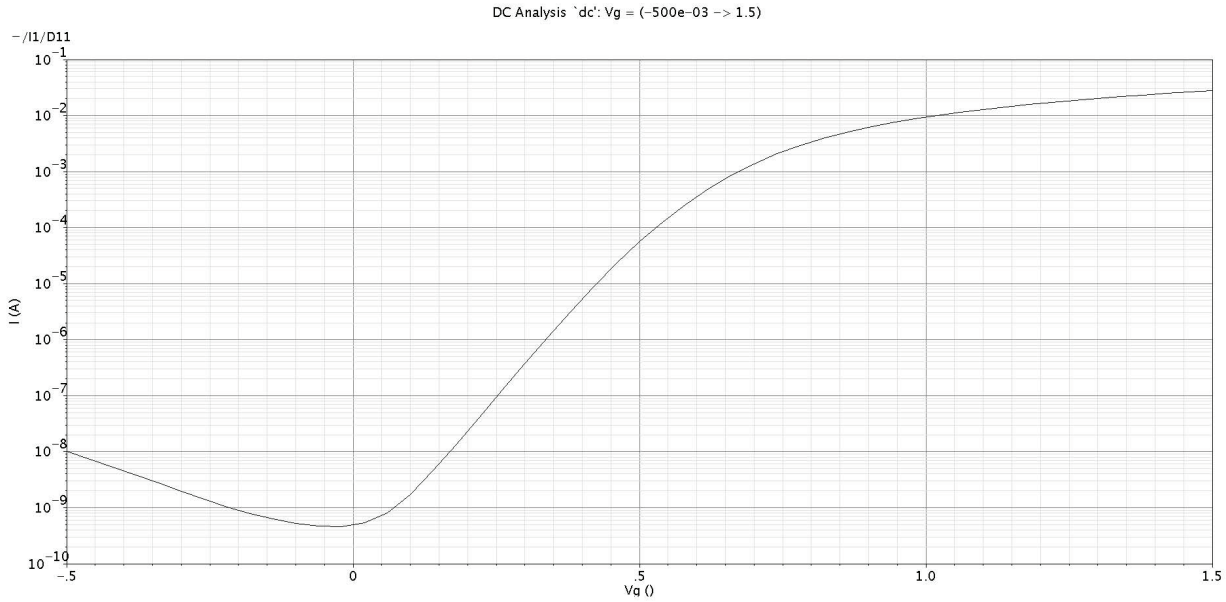


Figure 6.1: Typical I_d-V_g simulation

In order to obtain the leakage current, the V_{th} should be obtained first. The current flow from drain to source where V_g is smaller than the V_{th} is the leakage current. The extrapolation in the linear region(ELR) method [38] could be used to extract the V_{th}. An I_d-V_g simulation for a single NMOS transistor was done with the NMOS biased in the linear region. By finding the maximum first derivative (slope) point (the point of maximum transconductance) of the I_d-V_g curve and drawing the tangent line, the interception with the gate voltage axis could be found. The V_{th} is the intercept value adds $V_{ds}/2$.

The simulation result is shown in Figure 6.2. V_{ds} is 100mV, the maximum first derivative point is at $V_g = 0.86$V, the calculated V_{th} is 0.73V.

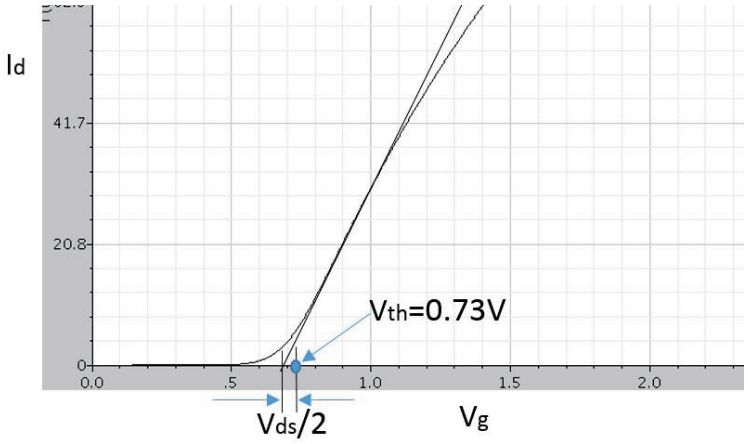


Figure 6.2: Threshold voltage extraction simulation

6.1.2 Transistor Array

This simulation is to verify the function of the test block and to check if the current on the pad is the same as the current flow through the selected transistor. If they match it means that the measured current on the pad is not altered by the transmission gate so the future test result will be reliable. The simulation result is shown in Figure 6.3.

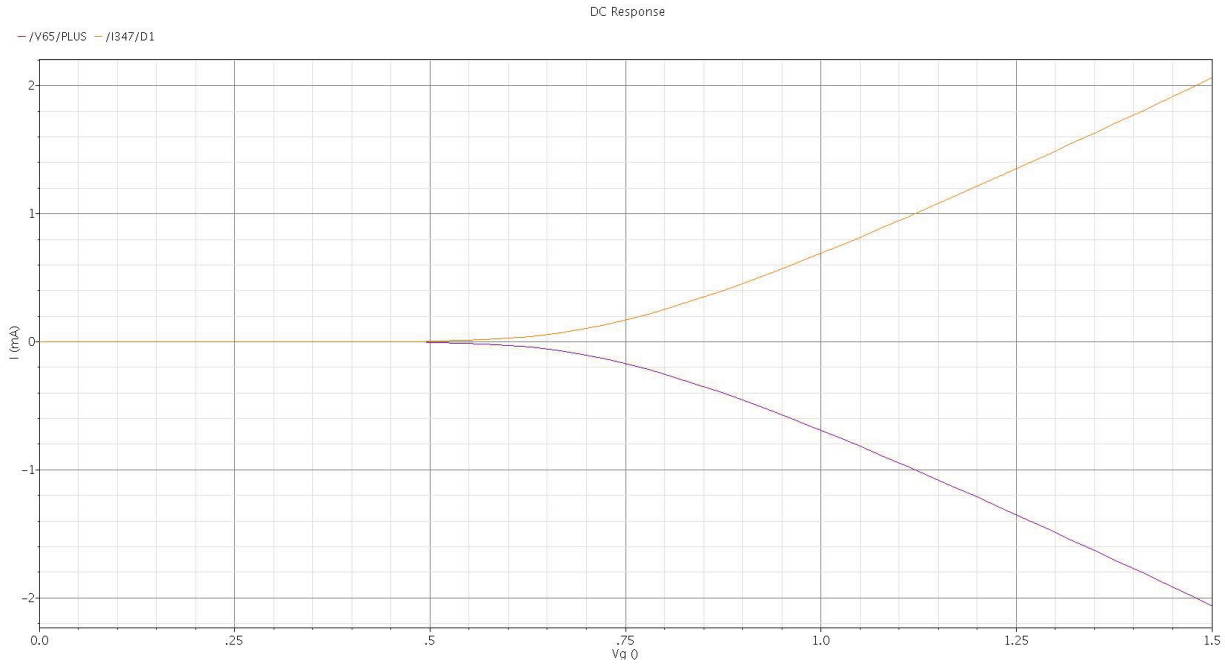


Figure 6.3: I_d-V_g curve of transistor array

The positive I_d current curve represent the current flow through the drain of the selected

transistor, the negative current curve represents the current flow through the V_d pad. For selected transistor, the V_d is 1.5V, source is 0V. V_g is varied from 0V to 1.5V and its impact on I_d is noted. From the simulation result it is evident that these two currents (I_{pad} and I_{drain}) are equal and only the direction is different, which means that the current measured on the pad is the same as the current flow through the drain of the transistor. The simulation result proves that the transistor array block will work fine.

6.1.3 Ring Oscillator

The ring oscillator measures the TSV impact on the digital circuits. Whole ring oscillator simulation is performed to check if it oscillates as designed. Frequency divider simulation, is carried out to check if the frequency generated by the ring oscillator is divided correctly. The whole ring oscillator block is also simulated for future comparison.The simulation result of the frequency divider by 2 is shown in Figure 6.4 and the whole block simulation is shown in Figure 6.5.

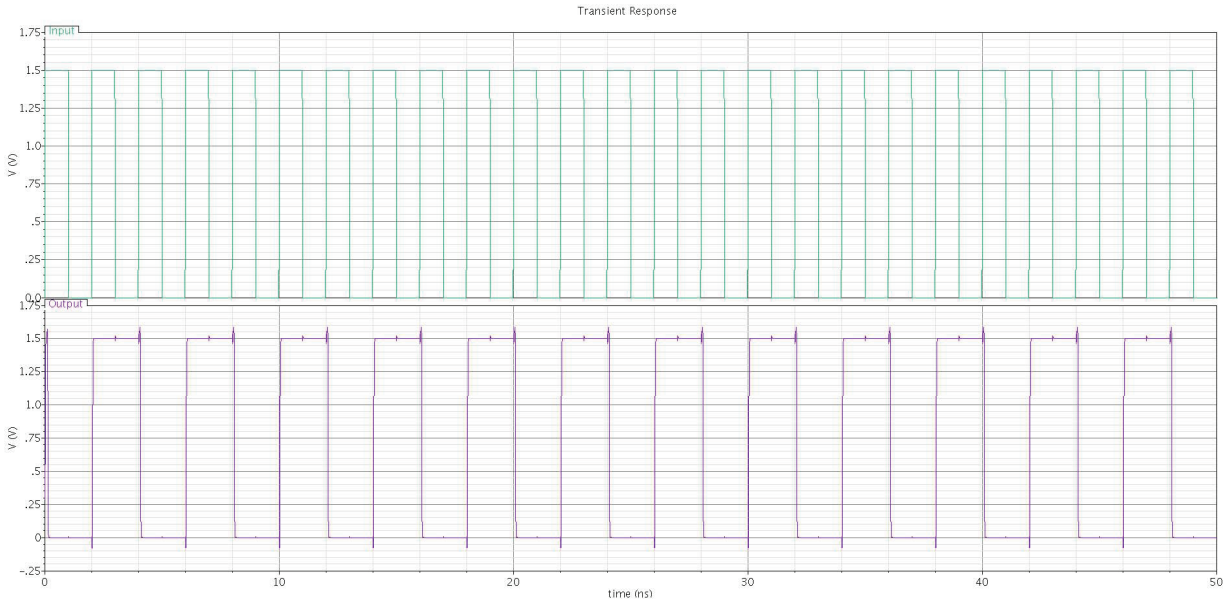


Figure 6.4: Simulation result of frequency divider

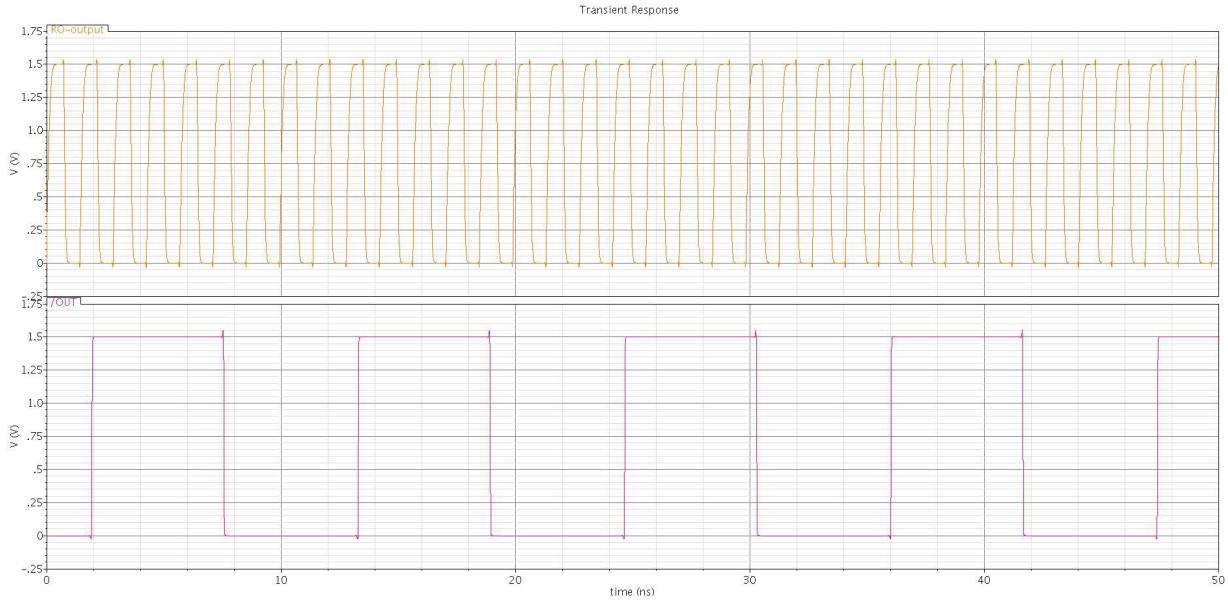


Figure 6.5: Simulation result of ring oscillator

The upper part in Figure 6.5 is the 21 stage ring oscillator output and the bottom part is the final output after the frequency divider and the buffer.

6.1.4 Thermal Sensor

The thermal sensor simulation is done to verify the sensor design and to check the sensor accuracy. The temperature varied from 0°C to 100°C, the diode forwarding voltage changed linearly with the temperature. Matlab is used for processing and analysis of the simulation data. Maximum error of less than 2% is seen which means the temperature read from the sensor will have less than 2°C difference from the actual temperature, this will be good enough for the designed test chip. Figure 6.6 shows the result of the thermal sensor simulation and its comparision with the ideal V-T curve.

It can be seen that the error is bigger around 50°C. The reason is that the current generated by the current mirror is also affected by the temperature and is not a purely constant. It has very small deviation which causes the relatively bigger error around 50°C. However, since the maximum error is still in the acceptable level, it can be used in the test chip.

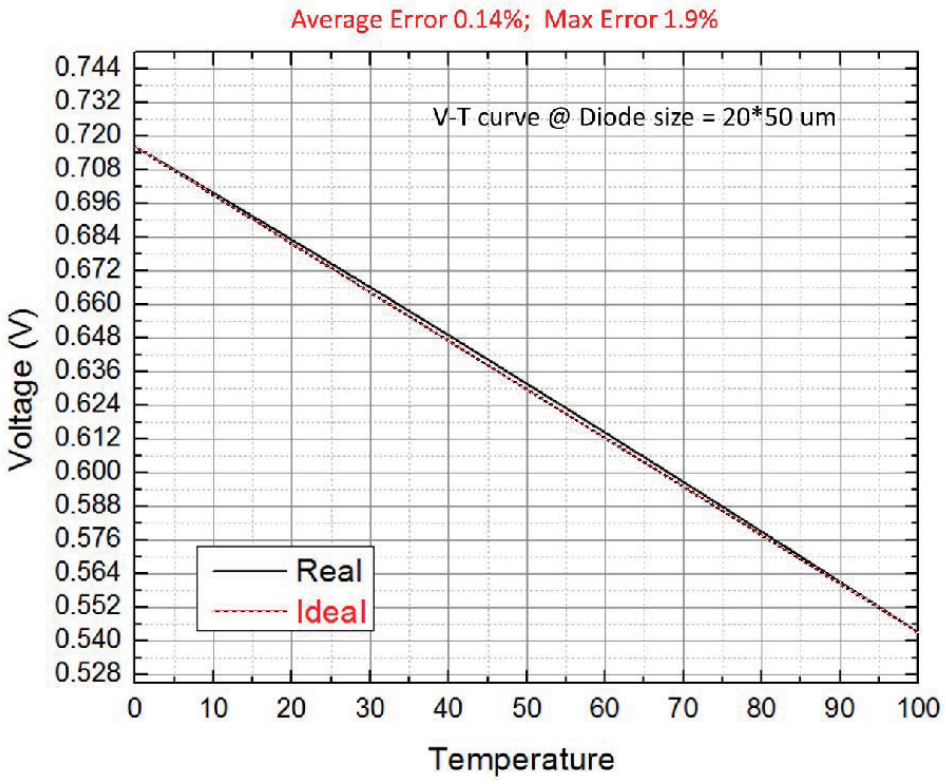


Figure 6.6: Simulation result of diode sensor

In a real test, the diode sensor needs to be calibrated under two different temperatures. This could be easily done by putting the test chip in the temperature room and measuring the output voltage at certain temperature. The heater should not be connected during calibration.

The designed thermal sensor may not be so accurate when comparing it with other published thermal sensor design, but it is simple and only one pad for measurement is required. This thermal sensor design is suitable for I/O constraint chip design where accuracy requirement is not very high.

6.2 TSV Coupling Simulation

The simulations of the RF test block were done with HFSS. Simulations were used to verify the effectiveness of the employed coupling reduction methods. The first step was to setup the TSV model in the HFSS, the parameters are shown in table 6.1. After the model was setup, three sets of simulations were done with different distances between two TSVs

and with and without TSV walls.

Table 6.1: TSV model parameters

TSV Diemeter	1.2μm
TSV height	8μm
Thickness of Silicon dioxide	0.25μm
Substrate height	8μm

Now the TSV model has been set up and can be used in simulation.

Figure 6.7 shows the model of the TSV coupling test structure, there are four TSVs: aggressor, victim and two ground TSVs. The distance between the TSVs is 6.2μm which is the minimum distance that the technology allowed and is the same as the test structure we implemented in our test chip.

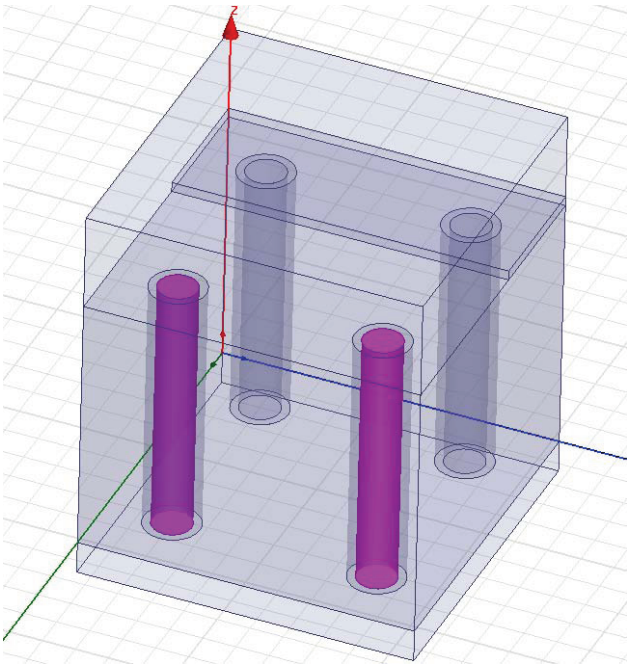


Figure 6.7: Test structure1 for TSV coupling measurement

Figure 6.8 shows the insertion loss of the test structure1. One of the selected TSVs (red ones) is the aggressor and the other is the victim, we can see from 5GHz to 10GHz that the coupling is increasing with the frequency.

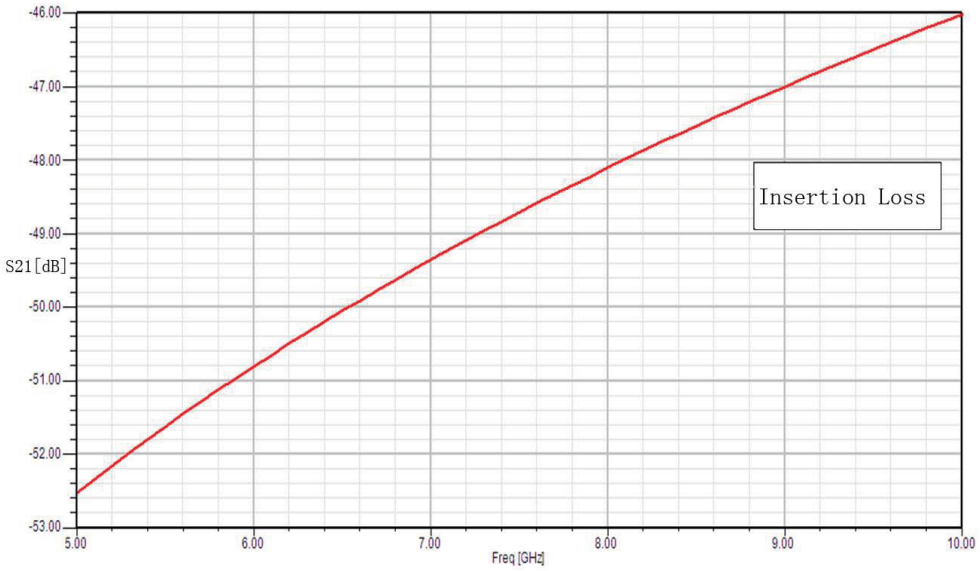


Figure 6.8: Insertion loss for test structure1

Figure 6.9 shows the TSV coupling test structure with guarding TSVs. The structure is almost the same as the test structure1 but with three added TSVs between two ports as TSV wall.

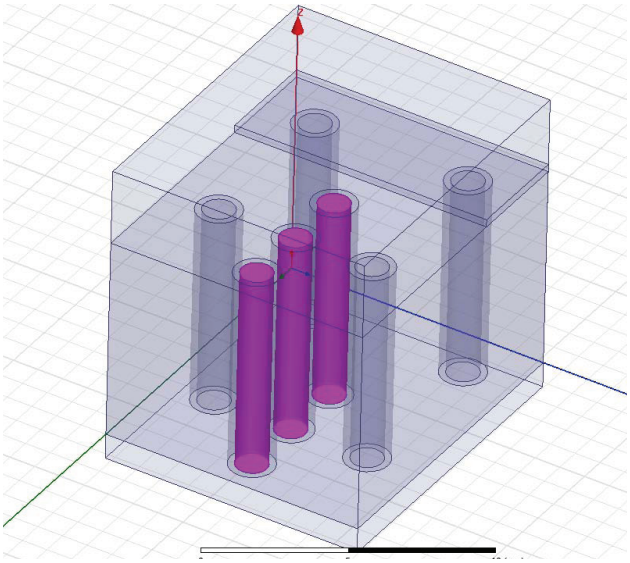


Figure 6.9: Test structure2 for TSV coupling measurement

Figure 6.10 shows the insertion loss of the test structure1. The selected TSVs are guarding TSVs, it is evident that from 5GHz to 10GHz, the coupling is much smaller comparing with

the simulation result without guarding TSVs.

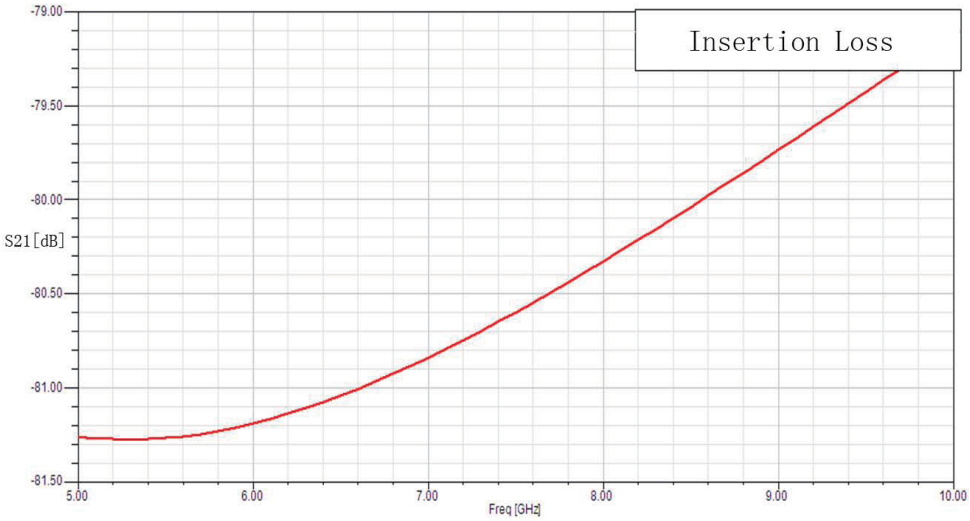


Figure 6.10: Insertion loss for test structure2

Figure 6.11 shows the TSV coupling test structure with longer distance between the TSVs. The structure is almost the same as the test structure1 but the distance between the two TSVs was changed to 10μm.

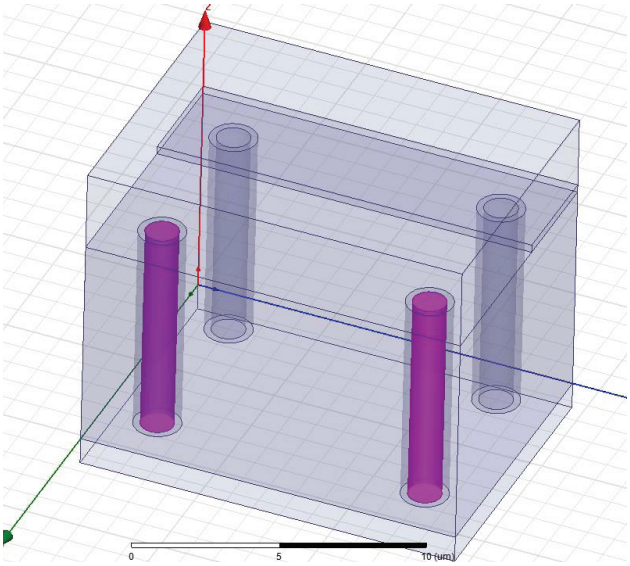


Figure 6.11: Test structure3 for TSV coupling measurement

Figure 6.12 shows the insertion loss of the test structure3. The simulation result reveals

that from 5GHz to 10GHz, the coupling is a bit smaller comparing with the simulation result with smaller TSV pitch.

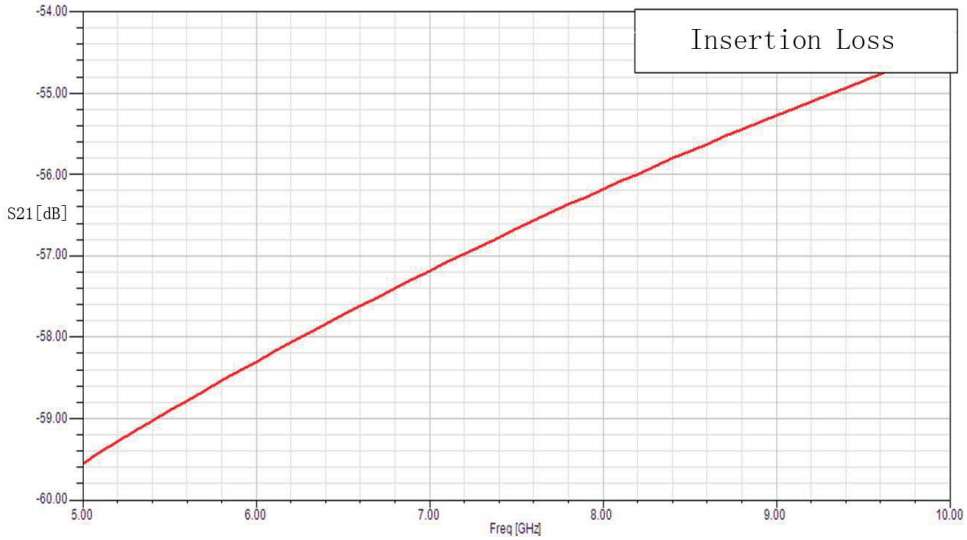


Figure 6.12: Insertion loss for test structure3

The simulation results show that the method used to decrease TSV coupling with guarding TSVs is effective and the distance between the signal TSVs also have some influence on the TSV coupling. Although the TSV coupling is relatively small in the Tezzaron 3D-IC technology, for other technology with longer TSV length, it may become a reliability issue and the guarding TSVs can be used to decrease the coupling. In addition, TSVs can be placed as far as possible to minimize the TSV coupling.

6.3 TSV Leakage Current Simulation

The TSV leakage simulation was carried out by using the Sentarus TCAD. This tool is good for device modeling and simulation. In Chapter 2, the reason of the TSV leakage was analyzed, but simulations revealed that how serious it was with reasonable process defects. Figure 6.13 shows the simulation structure of the TSV leakage current.

This model assumes that there is a 0.1μm overwhelming of conductor to the TSV sidewall and the TSV voltage sweeps from 0 to 1.5V. Figure 6.14 shows the cross section of the

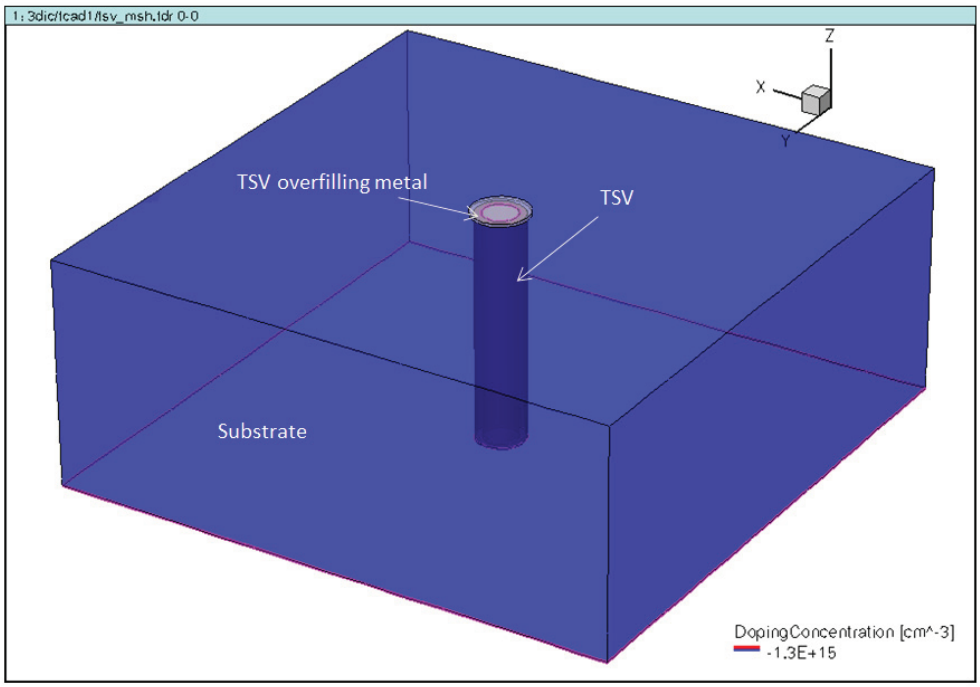


Figure 6.13: Simulation structure of TSV leakage

simulation structure.

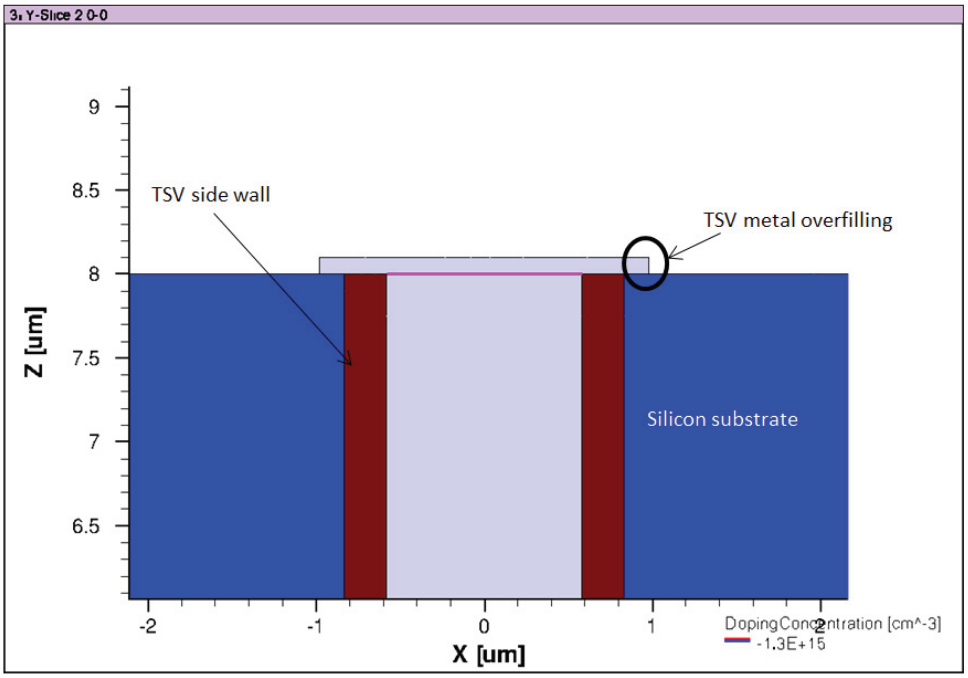


Figure 6.14: Cross section of the simulation structure

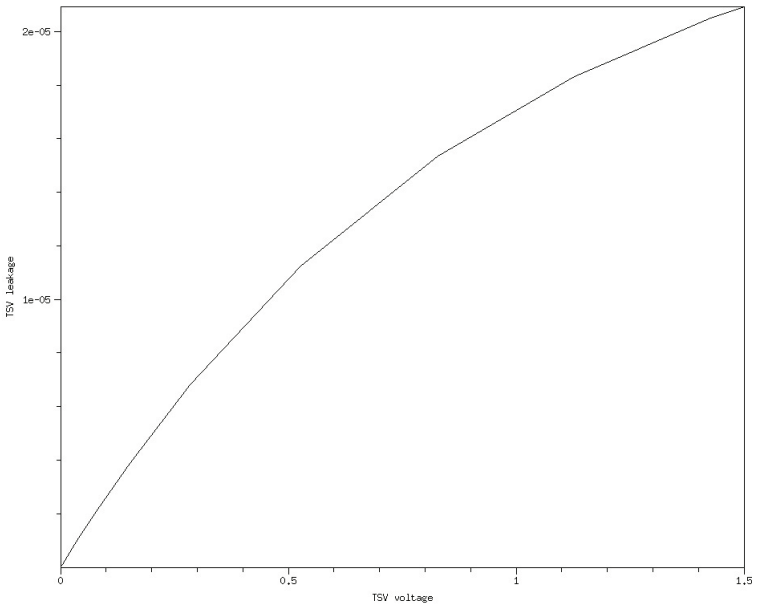


Figure 6.15: Simulation result of the TSV leakage

The simulation result is shown in Figure 6.15. It is evident that even with only a 0.1μm overwhelming of the conductor, the leakage current of the TSV will be as large as 20μA and this is only for one single TSV. If multiple TSVs are used as TSV arrays, the situation could be much worse and it would significantly increase the static power consumption and degrade the circuit performance or even make the chip not work at all. The yield of the TSV is still a big problem in the development of the 3D-IC technology.

7. Conclusion and Future Work

7.1 Summary and Conclusion

The 3D-IC technology has shown potentials to alleviate the performance limitations that the current CMOS scaling is facing at relatively low cost. However, the lack of accurate TSV models and some major reliability concerns constrain the development of the 3D-IC technology. In order to solve these problems, the following work has been done through this thesis:

1. The electrical properties of the TSV (resistance, capacitance, inductance and leakage current) were analyzed with presentation of a lumped RC model of the TSV which can be used in the design kit to help 3D-IC circuit designers.

2. The TSV impact on nearby transistors induced by the CTE mismatch stress was studied. This stress affects the properties of nearby devices within a zone and this zone can be measured and defined through the test circuit presented in this work.

3. Thermal heaters and on-chip diode sensors were designed and implemented to study the thermal dissipation methodology in 3D-IC chips.

4. The performance of high frequency signals in 3D ICs was studied. The S-parameter of the TSV and coupling among the TSVs were analyzed; some techniques (TSV guard ring and TSV wall) to reduce the TSV coupling were implemented. The TSV wall was simulated and the result showed that it could greatly reduce the TSV coupling.

A test chip was designed and simulated with the Tezzaron 3D-IC technology. The simulation results showed that all the test blocks had met the design specifications and would

work well. After the testing of the designed chip, the TSV parameters could be obtained and the KOZ could be defined. In addition, the electrical performance of the TSVs working under high frequency could be characterized which will provide useful information on the placement of the TSVs; techniques to reduce the TSV coupling will also be verified.

7.2 Future Work

The test chip has been designed, verified and is ready for fabrication. The next step is to do the interposer design. In a stacked package, the TSVs connect the dies together and the interposer connects the stacked dies to the package through a redistribution layer (RDL) inside the Si interposer. After designing the interposer, a proper package should be chosen and the final package will be done.

After the test chip is received, a test plan will be followed as follows:

1. Measure the TSV resistance, capacitance and leakage using the test circuit.
2. Measure the transistor's leakage near the TSV to see the TSV impact on transistor leakage
3. Measure the transistor's threshold voltage, saturation current near TSVs with different distances and angles, a KOZ could be defined.
4. Measure the temperature on both dies at different spots to see the thermal dissipation.
5. Measure the RF parameters of the TSV.

In addition, the hard X-ray micro-diffraction mapping (XRD) facility at the VEPERS beamline, Canadian Light Source (CLS) and the Raman micro-spectroscopy (IRS) equipment at the Saskatchewan Structural Science Centre (SSSC) will be used to experimentally map and study the stresses and strain in the test samples, investigate the stress at the full chip/package level.

The designed test chip is to measure the basic electrical parameters of the TSV and to study some critical 3D-IC reliability issues, it does not have any useful functions. Therefore,

designing a 3D-IC chip with real function (for example, a SRAM chip) and testing it to see the performance improvement will also be an interesting work.

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