COMPUTERIZED GENERATOR DIFFERENTIAL PROTECTION

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"COMPUTERIZED GENERATOR DIFFERENTIAL PROTECTION"

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ABSTRACT

This thesis presents a computerized scheme which detects the presence of phase to ground and phase to phase stator faults on power system generators. The fault/no-fault decisions are based on the amplitude ratio of the "fault" and "average-through" currents from a selected generator phase. Techniques for fast amplitude extraction from sampled inputs are evaluated. The proposed protection scheme is amenable to a time-shared digital computer approach.

An analog input data pre-processor, used to reduce the sampling requirements of the digitizer, is described. An input data monitor is included to activate the more sophisticated software only when required. Fast acting software is included to restrict subsequent calculations to the data from the faulted phase. Special attention is directed towards making valid amplitude comparisons during the transient period immediately following fault incidence. A data logging function, which retains and returns information from any conditions analyzed by the software, is included to permit reconstruction of the pre-fault and post-fault currents. The operation of the hardware and software is also reported. The results of extensive tests, performed on single and three phase versions, were used to evaluate the performance of the scheme. Approximately 800 case studies including internal and external faults using a three phase generator, are presented.

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1. INTRODUCTION

Protective devices, as used by electrical utilities, avert further deterioration of the system which might be caused by a prolonged deviation from the expected behaviour of its components.[25,43,45] The history of automatic protection began with the development of fuses. These isolate the source from its load when an abnormality, current in excess of the rated value, is present. In power system applications, fuses have been supplanted by improved devices. This can be attributed to the inability of fuses to discriminate between various malfunctions and their (the fuses') required replacement before the isolated element can be restored to service.

The first major improvement on fuses was provided by automatic circuit-breakers with trip coils energized by system currents and voltages.[43] Soon afterwards, the selective functions of automatic switchgear were transferred from the breakers to separate protective relays, whose contacts initiated tripping. The first relays, designed to respond to short-circuit conditions, were attracted armature devices. Some of these operated only after a time delay provided by a pre-set dashpot mechanism. As power systems increased in size and complexity, relays with more precise operation and inverse-time characteristics (operating time inversely proportional to fault severity) were developed. Relays based on the induction disc principle, commonly used in watt-hour meters, provided a viable solution in the early 1920's.[43] As requirements for greater sensitivity, selectivity and speed increased further, a trend towards the use of fast differential relays for primary protection developed. By the late 1920's, the induction disc relays had been replaced with balanced beam and induction cup types.[43]

Since these pioneering developments, many improvements have been selectively incorporated but power system relaying has, until recently, been slow to implement electronic fault sensing equipment. In their early stages of development, electronic protection schemes relied on the operation of vacuum tubes as comparators, amplifiers, logic switches and pulse generators. Designs incorporating thermionic emission devices could not be extensively implemented, in practice, due to their fragile construction and unreliable operation.[39] The advent of solid state (semiconductor) devices enabled the present trend towards electronic relays. Many designs of phase and amplitude comparators have since been developed for use in power system protection. The demand for improved protection and control techniques has continued to increase. This is due to the growth of generating capacities and interconnections of individual systems to form regional power pools.

Continuing rapid advances in digital computer technology have prompted a re-evaluation of protective devices and techniques. The use of real-time digital computers for system protection was advocated in 1966 by Last and Stalewski.[21] In 1967, Rockefeller discussed the use of on-line digital computers for substation protection.[27] Mann and Morrison demonstrated the feasibility of the digital computer application to transmission line protection in a laboratory environment.[22,23] Rockefeller and his associates have subsequently applied a digital computer to protect the Tesla-Bellota, 230 kV line.[12,28] Computerized transformer protection has also been proposed.[41]

The digital computer protection of generator stators, as reported in this thesis, is a new application in the power systems area. The project was undertaken to realize two distinct but closely related aims. First,

the work was to provide much needed experience in digitizing and processing power system variables. Secondly, it was to demonstrate the feasibility of providing generator differential protection using a real-time computer.

The dynamic behaviour of a generator stator, while it is experiencing a fault, must be understood to appreciate the operation of both the conventional electromechanical relays and the proposed alternative. A suitable qualitative examination of stator fault currents and the resulting relay response are presented in chapter 2. Other generator faults are also briefly described to relate percentage differential current relays to overall plant protection philosophy.

Two digital techniques, advanced by other researchers and used to accelerate power system data processing, are examined in chapter 3. The analysis for both, the cycle to cycle comparison of input parameters and the instantaneous sample to peak value conversion, are presented. These processing techniques are examined, with particular emphasis on the requirements of the digital protection scheme described in this thesis; the analysis is generally applicable to other digital protection and control problems in power systems.

The general characteristics of digital computers, which might be advantageously used in protection schemes, are outlined in chapter 4. Analog pre-processing of input data is proposed to alleviate analog to digital conversion problems. The advantages of the multi-use digital computer approach are discussed. Several alternative design concepts for the proposed scheme are also explained. Included in the descriptions are, (i) parameter selection and data processing considerations for the fault monitor, (ii) the requirement for and a description of, software to

determine the most probable originating phase of the fault symptoms and (iii) a method to modify input parameters to permit evaluation of data in the immediate post inception period.

Implementation of these and other concepts, to obtain a viable digital percentage differential protection scheme, is described in chapter 5. Relevant characteristics of the hardware selected are outlined. The operation of the analog pre-processor, and the fault monitor, phase allocation and fault verification segments are described in detail.

The performance of the digital percentage differential protection scheme is evaluated in chapter 6. The reactions of a single phase and a three phase software version to controlled D.C. and A.C. inputs from an analog computer are described. A three phase generator was deliberately faulted in the laboratory to provide the data required to evaluate the performance of the complete protection scheme. Some 800 case studies of both internal and external faults were examined. The reaction of the protection scheme has been reconstructed for typical examples of each type of fault. Important details, concerning scheme's reaction to the fault data, are explained with the aid of these examples.

2. PRESENT PROTECTION TECHNIQUES

This chapter is included to acquaint the reader unfamiliar with power system protection to the philosophy and techniques commonly applied. Generator protection is discussed with particular emphasis on differential current relaying. The transient characteristics of stator fault current and differential relay response are qualitatively examined.

2.1 Protection Philosophy

Switching and fault sensing devices are provided in a power system to limit equipment damage during faults and overloads, and to minimize their effects on the remainder of the system.[25,43,45] This is accomplished by dividing the system into protective zones separated by circuit breakers as shown in Fig. 2.1. The protective equipment is deployed such that a faulted zone is isolated from the serviceable system elements. This divides the protection problem into two components. One is the problem of circuit-breaker selection which primarily consists of specifying its performance characteristics for proper application at each location. The second component is the application of relays which detect a fault in a protective zone and initiate appropriate measures ranging from alerting an operator to isolating the faulted equipment. The relay's decision making criteria are provided by currents, voltages and their derived functions. Relays based on power, power factor, current comparison, power comparison, impedence, reactance, modified reactance, current ratio, and sequence components are available. Relays may incorporate time delays before initiating breaker operation. An auxilliary source provides the energy required to initiate circuit-breaker operation. In power systems, the continuity of supply is an important consideration and

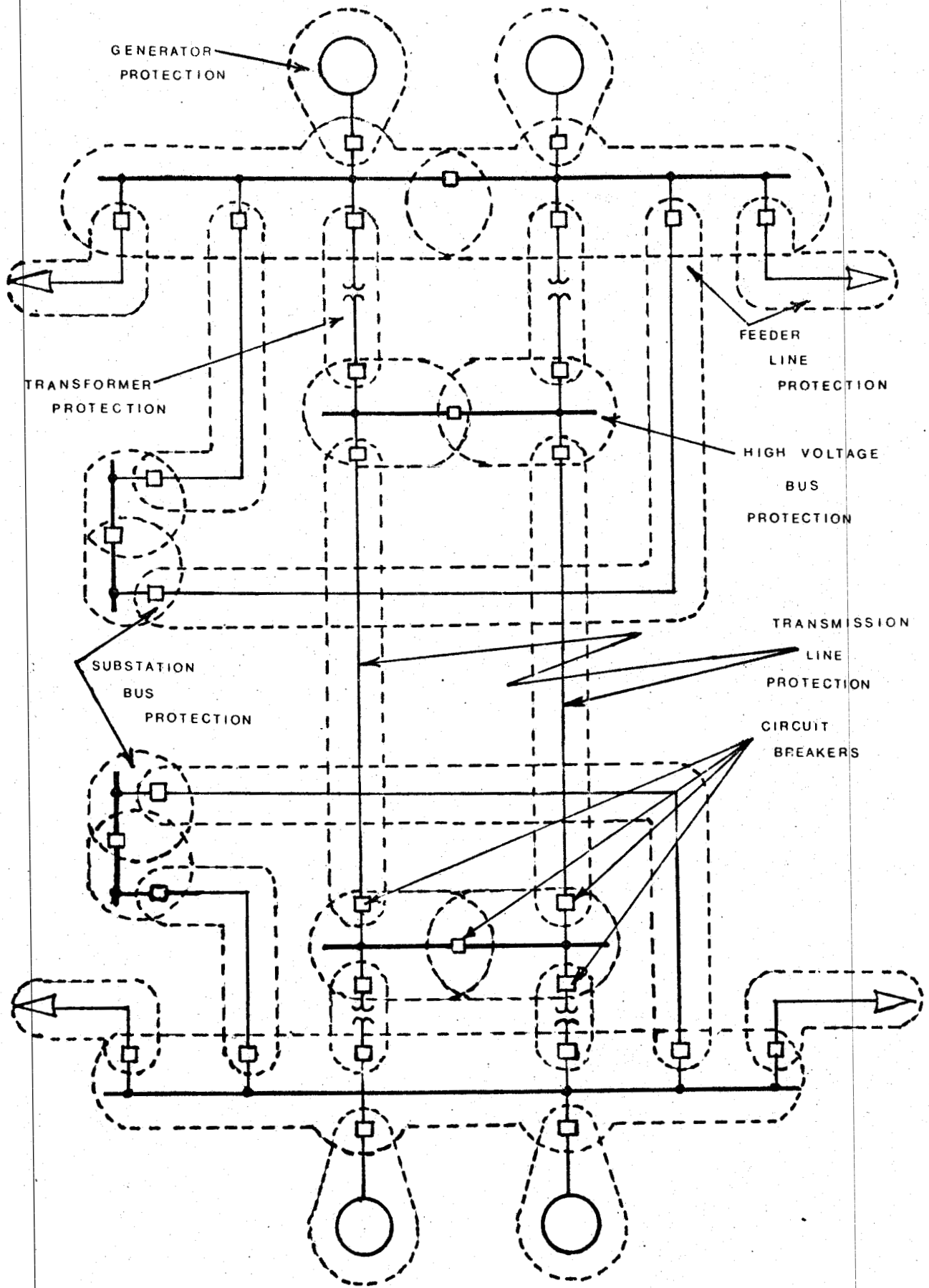

Fig. 2.1 The protective zones commonly employed in power systems.

under no circumstances can excessive unwarranted isolation of system elements be permitted.

2.2 Generator Protection

Alternators employed by electrical power utilities are provided with separate protective zones as indicated in Fig. 2.1. The equipment in these zones is protected for all contingencies likely to cause serious damage to either the generator or the system to which it is connected. Adequate measures must be employed to protect alternators which are susceptable to many types of faults. In this respect the generator protective zones are rather more complex than other zones such as transmission lines, transformer, motors, and bus bars. Two types of conflicting demands must be balanced to achieve the aim stated previously. The expected damage to the machine, caused by operating under adverse conditions, must be balanced against the disturbance which its immediate removal from the system might cause. To achieve the most favourable trade off, various techniques have been adopted which allow continued operation at reduced system capability in contingency situations.[9,45] This variability in operating configuration leads also to variety in the protection schemes employed to detect these contingencies. The situation is further complicated by the different types of prime movers presently available. An attempt will be made to describe the more usual situations with the realization that the situation will vary in particular applications.

2.2 a) Ground fault protection

Many electrical faults involve ground return loops. Generators are, therefore, provided with protective devices sensitive to the flow of current in the ground path. These relays are also sensitive to some ground faults outside the protective zone.[25] In addition, third harmonic currents could

also cause undesireable relay operation. Where discrimination between in zone and out of zone ground faults is not inherrent in the system, the ground current relays are provided with an adjustable delay so that they may be used as back-up protection in conjunction with primary protective schemes. High frequency filtering is employed to limit the relay's response to the third harmonic currents. In addition, the time delays also reduce their tendency to operate during fast transients. In many European installations, where lightly grounded generators are used, ground fault currents are allowed to flow for considerable periods of time.[9] The relays warn an operator of the presence of the condition. The affected generator is disconnected from the system with minimal disturbance after its load is transferred to other units. Though no serious malfunction is expected while operating with this contingency, the development of a second ground fault could cause serious damage.

2.2 b) Unbalanced faults

Negative sequence currents flow in the alternator windings for considerable time when the protective relays in other zones fail to operate for an asymmetrical fault.[45] These currents induce a second harmonic component in the rotor causing its temperature to rise. If the unbalance persists, the rotor may deform due to excessive heating. Because asymmetrical faults are normally due to conditions external to the generator, protection against these faults is provided as a back-up function. Relays, whose operation is based on the negative sequence current component, are employed. Suitable time delays are incorportated to coordinate the breaker tripping with the operation of protective equipment in other zones.

2.2 c) Overload protection

Current-overload protection is also required as back-up for the

failure of protective equipment in other zones.[45] AIEE Standard specifies that "a machine shall be capable of withstanding without injury a 30 second three phase short circuit at its terminals when operating at rated kva and power factor and with fixed excitation at 5 percent overvoltage". Voltage regulators increase the excitation to maintain the terminal voltage, and significantly higher currents are experienced during a fault. An inverse time, overcurrent relay, set at 120 percent of rated full load, can be employed. The terminal voltage collapse, which is inherent in overloads due to faults, is quite often used as an additional criteria for relay operation. The voltage controlled, inverse time, overcurrent relays allow operation when overcurrent and undervoltage conditions are simultaneously present. The time delays, incorporated in these relays, are also coordinated with the other protective elements.

2.2 d) Overheating protection

Many factors can contribute to overheating of the generator windings. Thermocouples and thermistors, imbedded in the stator, give a reasonable indication of the winding temperature.[45] The output from these devices is arranged to indicate the temperature, actuate an alarm and/or operate a relay.

2.2 e) Overspeed protection

Two types of overspeed protection are available. A detector based on the centrifugal action of a rotating device, mechanically coupled to the shaft, may be provided.[43] Alternatively, an overfrequency device excited by the generator terminal voltage, may perform the same function. These relays can be adjusted to operate at different overspeed levels, and protect the rotating equipment from mechanical damage.

2.2 f) Loss-of-excitation protection

Loss of excitation (either partial or complete) of synchronous machines increases the reactive power drawn from the system. Since the prime mover continues to supply power at the pre-fault level, the generator power output remains essentially the same.[45] The reduction in excitation is compensated by the reactive power drawn from the system. The machine will continue to operate as an induction generator if the system is large and able to supply the required reactive power. This mode of operation is inherently hazardous. Depending on the system, either the machine may be taken out of service through operator intervention or it may be tripped by a loss of excitation relay.

2.2 g) Protection against motoring of a generator

Motoring results from the inability of the prime mover to supply even the losses of the generating unit and the deficiency is then supplied by the system. In many cases, serious damage to the prime mover may result.[25] For example, in diesel engines an explosion hazard may exist due to unburned fuel in the exhaust while in hydraulic turbines the reverse power flow can result in serious cavitation of the turbine blades. Motoring of an alternator is detected by a relay which operates on reversal of power flow. Limit switches and temperature sensors are used for back up protection.

2.2 h) Field ground protection

A serious fault condition exists when two or more rotor insulation failures are present. Such faults cause local heating due to the flow of current in the core and excessive vibrations due to the resulting magnetic asymmetries.[45] A balanced bridge technique, depicted in Fig. 2.2, is used to detect the presence of the first insulation failure in the field

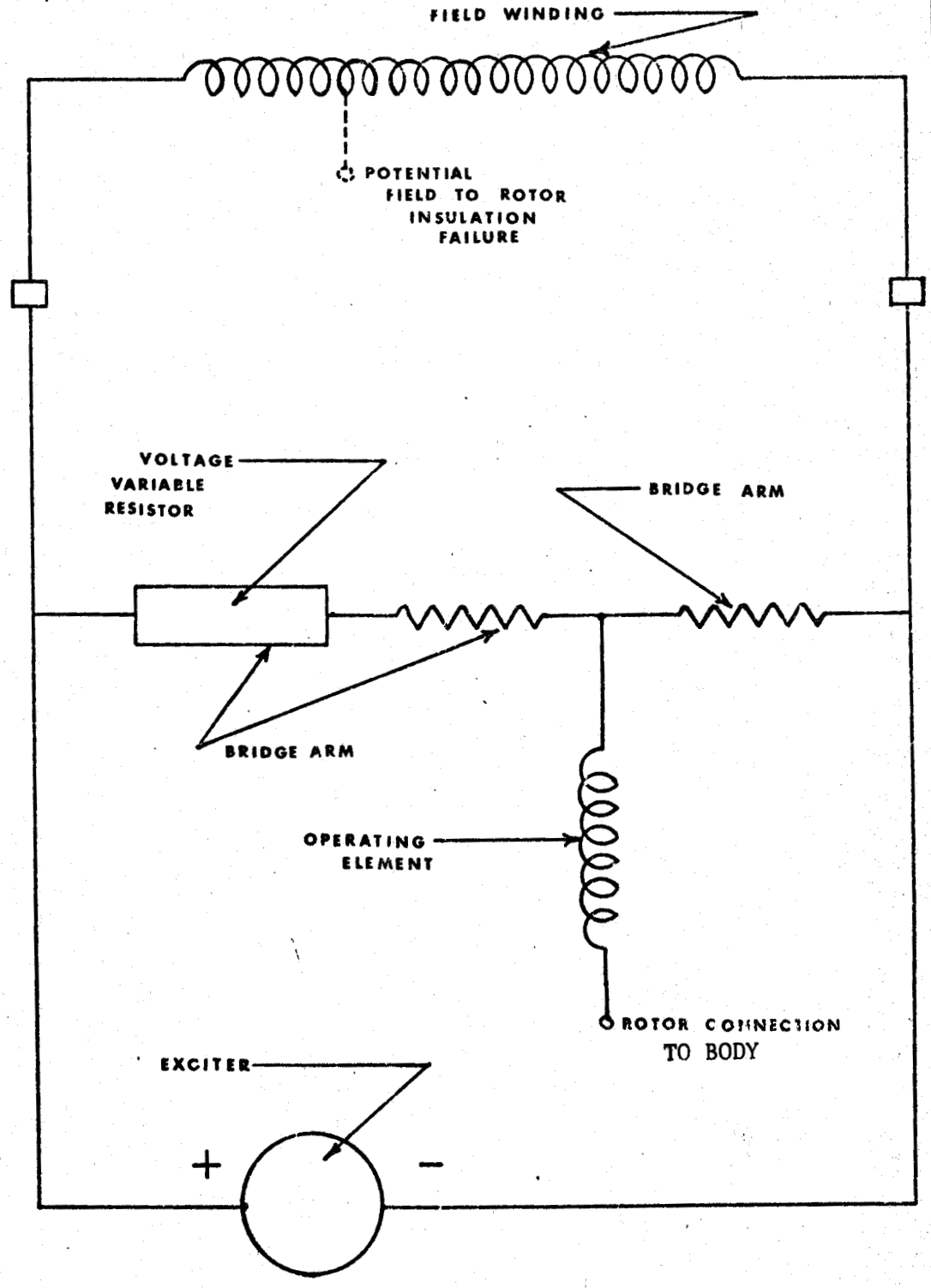

Fig. 2.2 A field ground fault detector using an unbalanced bridge technique.

circuit. The excitation for the bridge is provided by the field supply itself. The bridge, as such, does not exist until the first insulation failure. When it does occur, the bridge will only be balanced if the failure is located at the electrical center of the field winding. This is not a likely occurrence and the resulting imbalance manifests as a difference in potential across the detector. An alarm warns the operator who takes remedial action in due course.

2.3 Differential Protection of Generator Stators

The generator stator consists of three individual windings which deliver power to the system. The three phases are identical except that they are symmetrically displaced around the rotor of the machine. All other differences are usually incidental and of negligible consequence to the electrical characteristics of the individual stator phase. A stator winding consists of a number of turns of conductor , electrically insulated from, but physically imbedded in an iron core which is, under normal circumstances, connected directly to ground. Should the insulation between a conductor and the iron core fail, a serious fault condition will exist on the generator.[9,25,43,46] This fault establishes a new current path from the stator winding, through the iron core to ground. The new current loop is closed through any neutral point grounding impedance, which may be present, to the shorted stator winding. Significant amounts of this current, flowing for a given period of time, will result in localized heating of the stator core. This can cause irreparable damage to the generator. An obvious method, to detect the fault, is to sense the presence of current in the described fault loop. This approach has been successfully employed for many years as a matter of standard practice. The problems associated with measuring the current flowing in

the fault loop, which is not directly accessable, have been solved. The method used, in effect, treats each phase of the stator winding as a node with three branches. Any difference between the currents entering and leaving the node by the two established routes is taken to be the amplitude of the current flowing in the fault loop. Most relays react to significant amounts of this current at speeds which make the action dependent on its root mean squared value.

The severity of the stator ground faults, as previously described, tends to increase with time and may eventually involve additional phases. The most effective protection afforded against irreparable damage, caused by such faults, is differential current protection.[25,43,45] In these schemes, current entering and leaving a winding is compared in a differential circuit and the difference is used to operate a relay. Differential protection as applied to one phase of a generator is depicted in Fig. 2.3. During normal operation, or for faults outside the two current transformers, the current, I_1, entering the winding is equal to the current, I_2, leaving the winding if leakage and transducer mismatch is neglected. The operating current, which is proportional to (I_1-I_2), is small and the restraint may be adjusted such that this difference does not operate the relay. When an in-zone fault occurs, one of the currents will increase while the other will decrease. The increase of the relay operating current will depend on the severity of the fault.

External faults produce an increase of the same magnitude in both I_1 and I_2, but the asymmetries in the differential circuit and the transducers produce a considerable change in the magnitude of the difference current. Undesirable tripping may still be avoided by increasing the

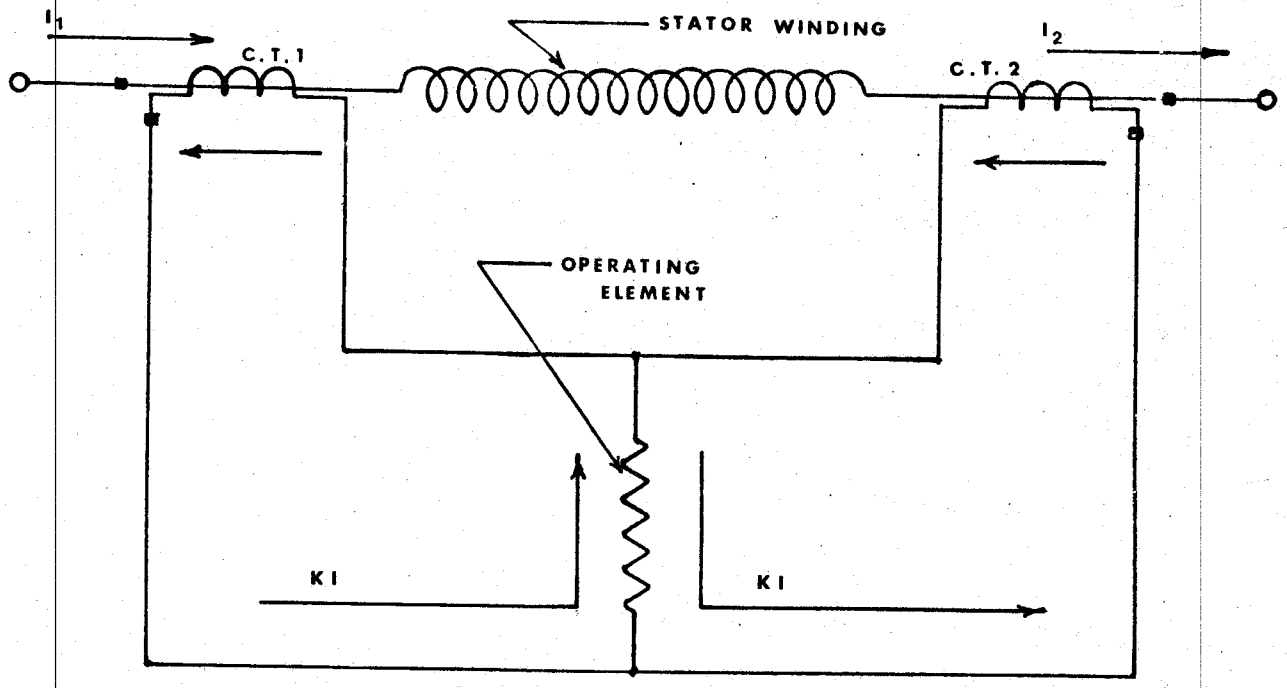

Fig. 2.3 A differential current protection scheme for one phase of a generator.

mechanical restraint of the relay. This desensitizes the protection scheme, a consequence which is quite undesirable. To overcome this disadvantage, a method of electrical restraint, whereby the restraining torque is provided by the currents, I_1 and I_2, is employed. The restraining windings are polarized to provide torque proportional to the vector sum of the two currents, I_1 and I_2. As the amount of current passing through the stator winding increases, either due to changing load conditions or external faults, the magnitude of the restraint increases proportionally. This type of protection is referred to as percentage differential protection and a single phase connection of the relay elements and current transformers is given in Fig. 2.4. Two types of percentage differential protection schemes are available. One is a fixed percentage type, while

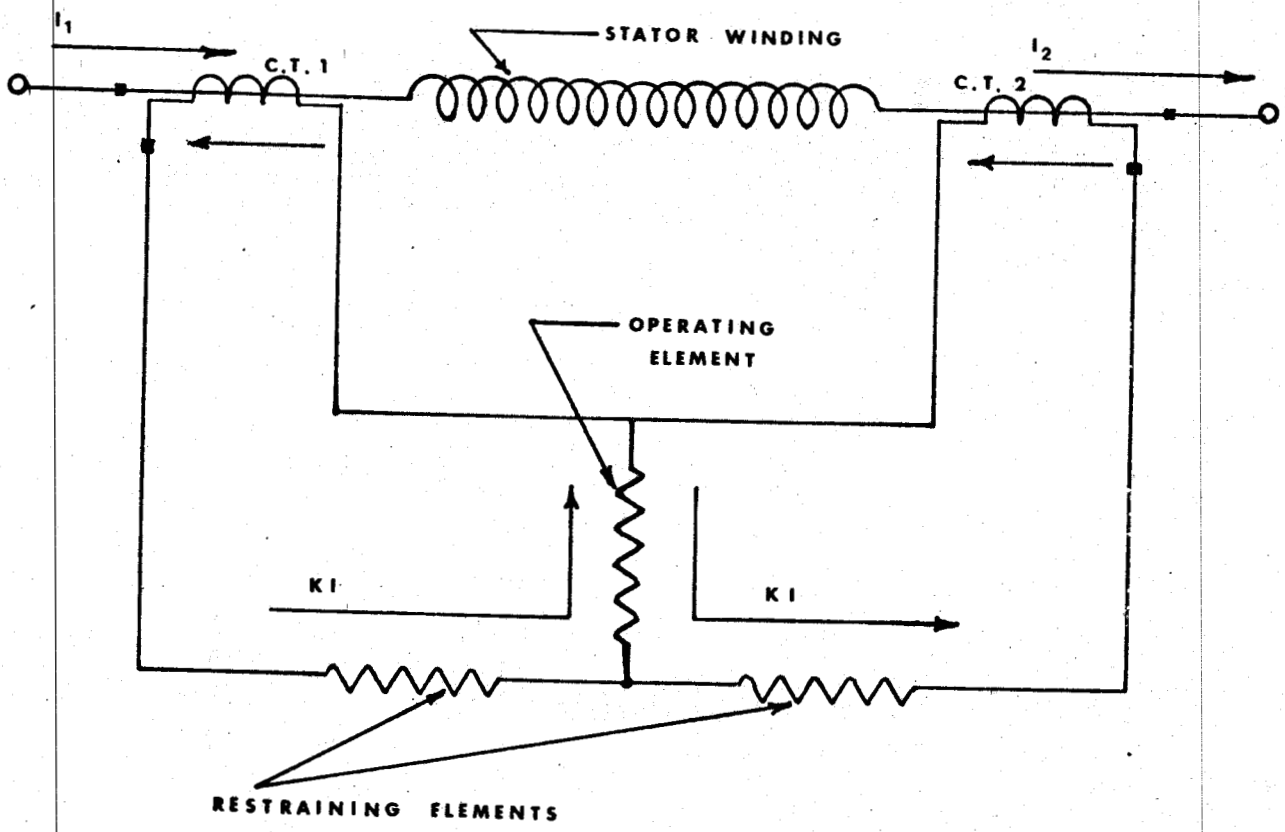

Fig. 2.4 Connection diagram of one phase of a percentage differential protection scheme.

the other is of variable percentage[45] (greater percentage at higher currents). The fixed percentage type is slower and is able to overide the d-c transients in all but the most extreme cases. The variable percentage relay is, due to its greater speed, inherrently more susceptable to misoperation caused by d-c transients. Specific measures, such as including high-pass filters, are therefore employed to overcome this difficulty.

2.4 Transient Characteristics of the Fault Current

An understanding of the transient behaviour of the fault current is essential to appreciate the dynamic performance of a percentage differential relay. The analysis of a short circuited generator is well under-

stood and documented.[43] The following can be assumed to obtain a describing function for the fault current:

i) the capacitive components of the difference current are negligible,

ii) the speed of the generator remains essentially constant during the interval being considered,

iii) the mutual inductive effects are balanced,

iv) the excitation remains constant during the interval being considered.

This describing function, I_f, may be written as:

$$I_f = (F_1(t) - F_2(t) + F_3(t) - F_4(t))\ U(t-t_o); \qquad (2.1)$$

where

$$F_1(t) = A\ e^{-\frac{t-t_o}{T_1}} \quad ; \quad F_2(t) = B\ e^{-\frac{t-t_o}{T_2}} \quad ;$$

$$F_3(t) = C\ \mathrm{Sin}\ (\omega t-\phi) \quad ; \quad F_4(t) = D\ \mathrm{Sin}(\omega t+\theta) \quad ;$$

and $A = G\ \mathrm{Sin}(\omega t_o) - C\ \mathrm{Sin}(\omega t_o-\phi)$; $B = G\ \mathrm{Sin}(\omega t_o) - D\ \mathrm{Sin}(\omega t_o+\theta)$;

t_o is the time of fault incidence

$F_5(t) = G\ \mathrm{Sin}(\omega t)$

The restraining current I_r may be similarly described as:

$$I_r = (F_1(t) + F_2(t) + F_3(t) + F_4(t))\ U(t-t_o) \qquad (2.2)$$

The function $F_1(t)$ is the exponentially decaying offset component of the current in one portion of the shorted stator; $F_2(t)$ is the exponentially decaying component of current in the other portion of the shorted stator; $F_3(t)$ is the alternating current in the first portion of the stator; $F_4(t)$ is the alternating current flowing in the other portion of the stator; and $F_5(t)$ is the pre-fault steady state current in the

stator. These currents are exemplified in Fig. 2.5.

Both the time constants and phase angles of the post fault stator currents depend upon the inductance to resistance ratios of the stator and the system. The current in the shorted portion of the stator will usually exhibit the longest time constant and the greatest deviation in phase from the prefault stator current except for marginal fault conditions. During marginal faults, when only a very small portion of the stator is shorted or when a large impedance (usually resistive) exists somewhere in the fault current loop, the time constant of the offset in the shorted stator winding is quite small. In addition, practically no change would be experienced in the load current and the fault current will be nearly in phase with it.

2.5 Percent Differential Relay Response

A qualitative analysis of a percentage differential relay will establish its deviation from the ideal response due to the transient behaviour of the stator.

As was previously indicated, present relay schemes rely on the fault current to produce the operating torque and on the through current to provide the restraining torque. An additional torque may also be provided by a spring to slightly bias the relay in the restraint direction. The torque equation may be expressed as:

$$T_o = T_f - T_s - T_r \qquad (2.3)$$

where T_o is the net operating torque and T_f, T_r and T_s are the torques due to the fault current, restraining current and spring respectively.

Although a certain amount of variation exists from one manufacturer to another, the torques acting are normally derived either as a direct or as a second order proportionality to the currents indicated. A qualitative

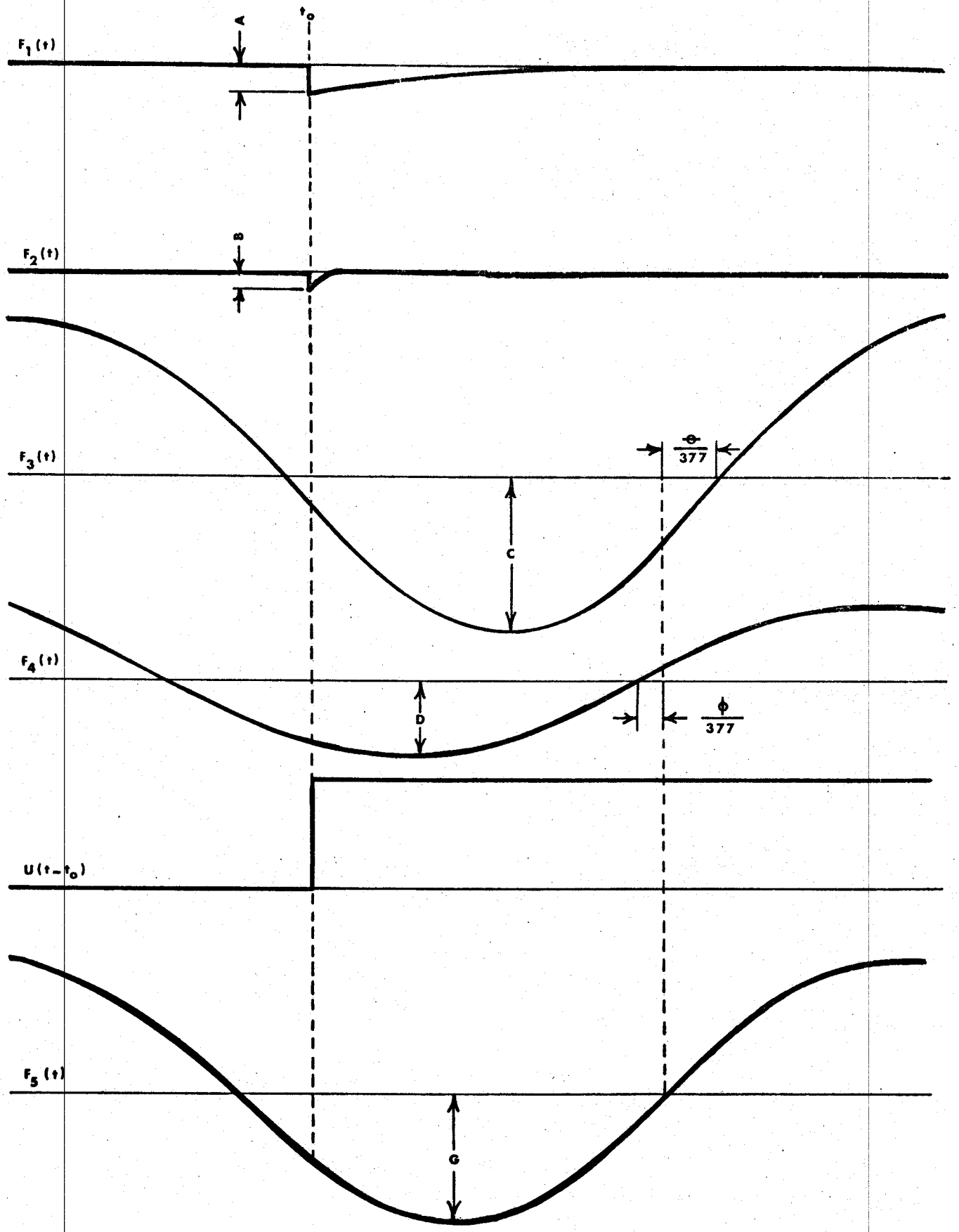

Fig. 2.5 Typical current describing functions encountered during a fault.

first order proportionality treatment is presented to permit comparison between the schemes used at present and the one proposed in this thesis.

In relays employing first order proportionality, a relatively uniform magnetic field in which the other elements may act is provided. Full wave rectifier circuits are provided in series with the relay elements to remove the polarity characteristics from the applied currents. The operating torque given by equation 2.3 may be expressed as a function of time in the following form:

$$T_o(t) = K_1|I_f(t)| - K_2|I_r(t)| - T_s \tag{2.4}$$

K_1 and K_2 are constants of proportionality relating the currents and torques. $I_f(t)$ and $I_r(t)$ are the fault and restraining currents respectively. These currents are defined in equations 2.1 and 2.2 and may be expressed as:

$$I_f(t) = (Ae^{-\frac{t-t_o}{T_1}} - Be^{-\frac{t-t_o}{T_2}} + C\sin(\omega t - \phi) - D\sin(\omega t+\theta))\, U(t-t_o) \tag{2.5}$$

$$I_r(t) = (Ae^{-\frac{t-t_o}{T_1}} + Be^{-\frac{t-t_o}{T_2}} + C\sin(\omega t-\phi) + D\sin(\omega t+\theta))\, U(t-t_o). \tag{2.6}$$

The sinusoidal portion of these functions may be reduced to a single sinusoid. Equations 2.5 and 2.6 may be modified as follows:

$$I_f(t) = (Ae^{-\frac{t-t_o}{T_1}} + Be^{-\frac{t-t_o}{T_2}} + R_1 \sin(377t + \alpha_1))\, U(t-t_o) \tag{2.7}$$

$$I_r(t) = (Ae^{-\frac{t-t_o}{T_1}} + Be^{-\frac{t-t_o}{T_2}} + R_2 \sin(377t + \alpha_2))\, U(t-t_o) \tag{2.8}$$

Several approximations are customarily made to determine the operating characteristic of a percentage differential protection relay. The transient portion of the driving function and the restraining torque

of the spring are usually neglected. The remaining sinusoidal functions define the long term tendency of the relay. The following balancing equation gives the ideal relay characteristic:

$$\frac{1}{T}\int T_f(t)\,dt = \frac{1}{T}\int T_r(t)\,dt. \tag{2.9}$$

or

$$\frac{\omega K_1}{2\pi}\int_{t_o}^{t_o+2\pi/\omega} |\, I_f(t)\,|\,dt = \frac{\omega K_2}{2\pi}\int_{t_o}^{t_o+2\pi/\omega} |\, I_s(t)\,|\,dt \tag{2.10}$$

This equation indicates that the operating characteristic is defined by "the ratio of the steady-state average values of I_f and I_r is constant." This ideal characteristic is depicted as in Fig. 2.6. Had the restraining spring constant been included in the equation, the characteristic would have to be modified as also shown in Fig. 2.6. This approach, however, neglects the presence of the transients and the phase displacements between the operating and restraining sinusoidal currents.

The transient, if it is slow enough, may be described as a variable D.C. added to the sinusoidal cycle. The absolute value of the resulting function may be used to describe the generated torque for any cycle as follows:

$$T(\theta) = K\,|\,\sin(\theta) + x\,|. \tag{2.11}$$

where

K is proportionality constant including the amplitude of the sinusoid,

x is the ratio of the D.C. offset to the amplitude of the sinusoid,

$x < 1$.

An average value of this torque is given by:

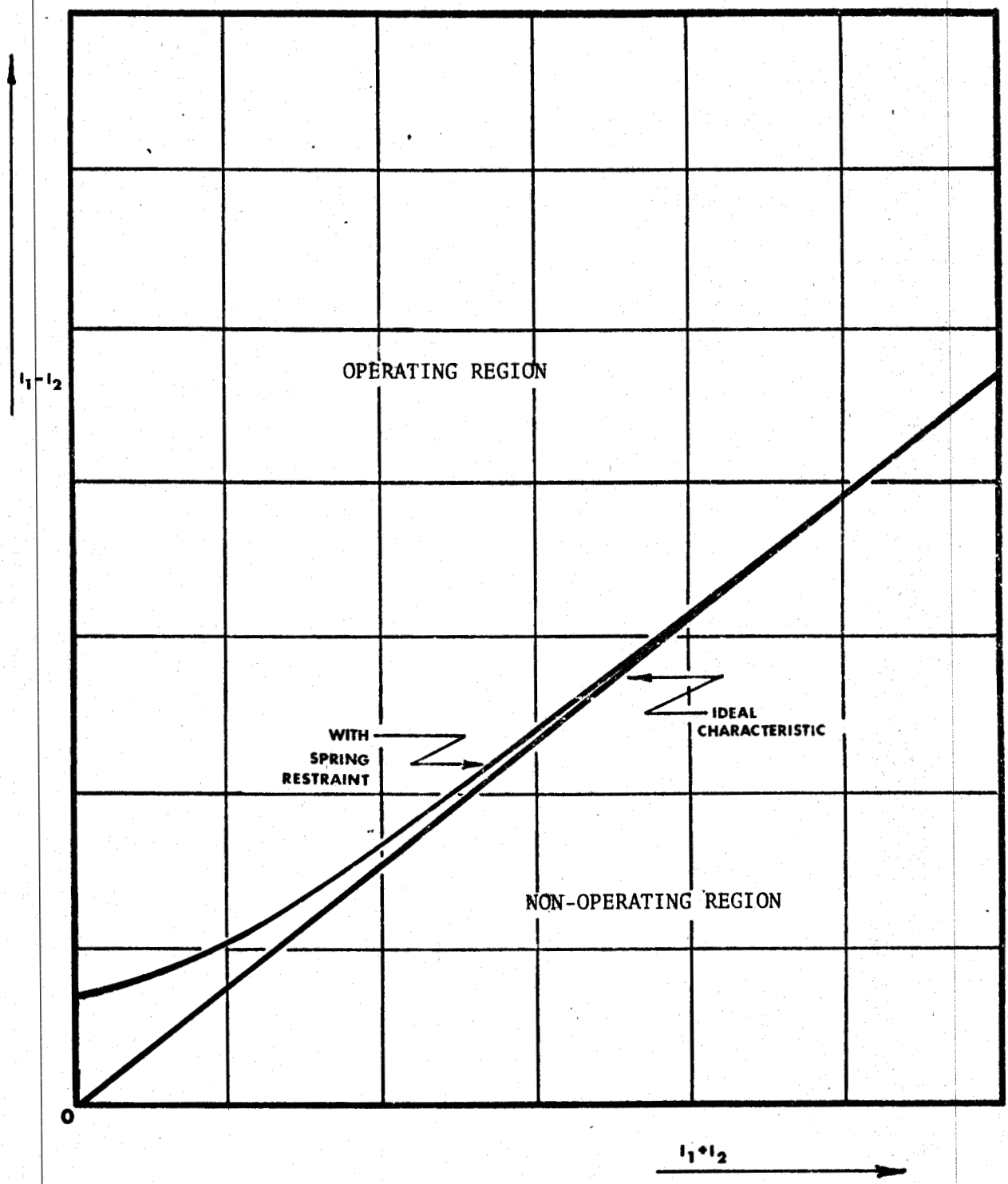

Fig. 2.6 Percentage differential protection characteristics illustrating the effect of spring restraint.

$$T(\theta) = \frac{K}{2\pi}\int_{-\Psi}^{\pi + \Psi} (\sin(\theta) + x)\, d\theta - \frac{K}{2\pi}\int_{\pi + \Psi}^{2\pi - \Psi} (\sin\theta + x)\, d\theta. \qquad (2.12)$$

where $\Psi = \arcsin(x)$

This indicates that the transients always provide additional torque. With the realization that the fault current must always start from zero, and that for marginal fault conditions the fault current transient will always be relatively more significant than the transient on the through current, it is evident that the transient will reduce the criteria required for relay operation. Further, the effect of the transient is not consistant. Fig. 2.7 illustrates the reduction in the precision with which the relay characteristic can be defined when the transient and other effects are included. One factor, which makes the operating characteristic even more obscure, arises from the difference in phase which may exist between the fault current and the through current. Any phase displacement will introduce another element of inconsistency of relay operation. The effect of the transients on relay operation is small in cases where averaging movements are used. In fast acting schemes, these effects can be quite significant.

A brief survey of the important protection requirements of generators with the traditional relay solutions has been presented. Differential current relay operation is particularly stressed to provide a reliable means of demonstrating the results contained in chapter six. In addition, the qualitative analysis of the stator fault current's transient behaviour will provide background information useful for understanding the principles on which the operation of the digital protection scheme, presented in this thesis, relies.

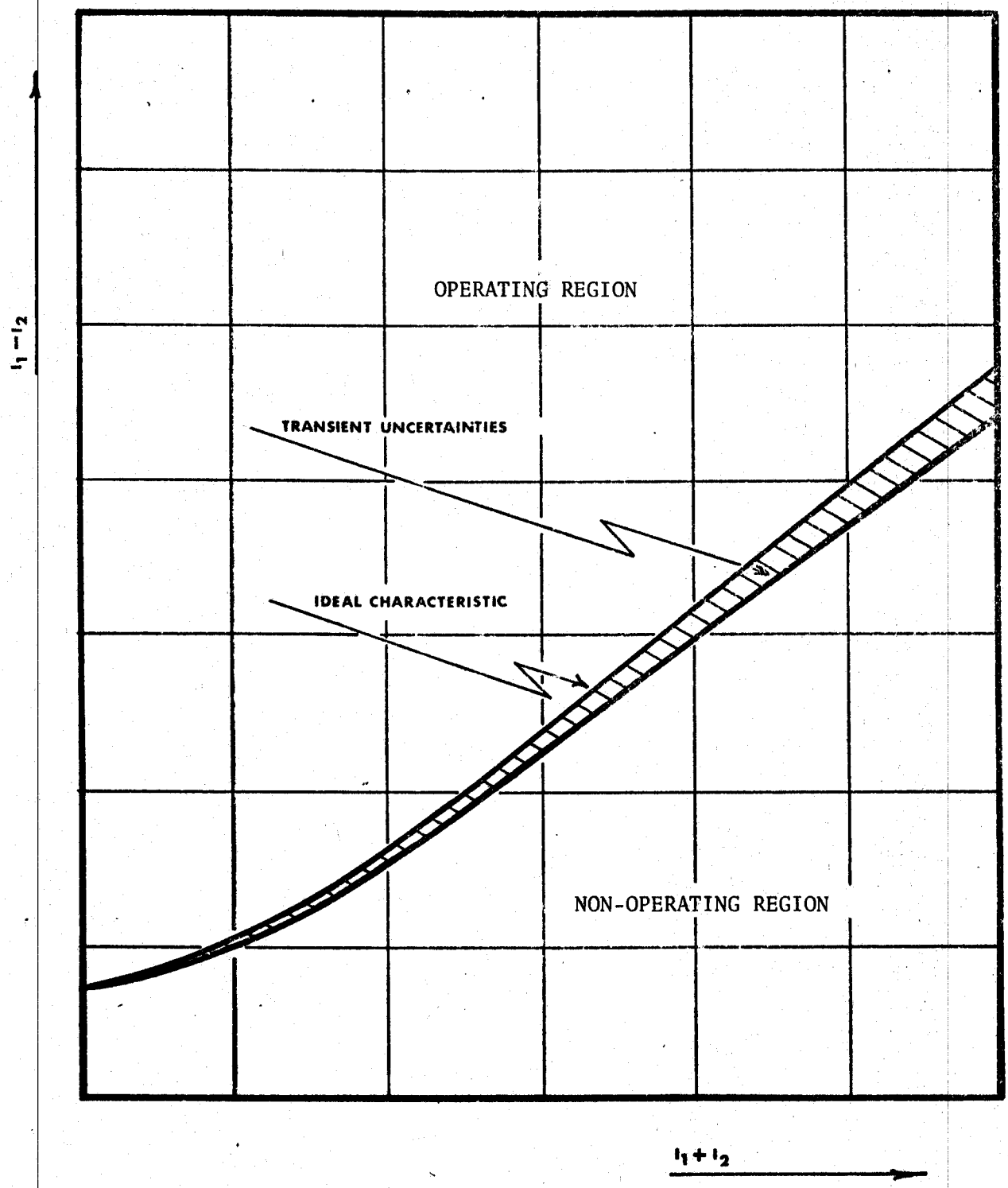

Fig. 2.7 Percentage differential protection characteristic including the faulted stator transient current effects.

3. ON-LINE COMPUTER PROTECTION TECHNIQUES

Practical application of on-line digital computers has been confined to data logging[7,24], distance protection of transmission lines[12,22,23,28] and differential protection of transformers[41]. System protection by on-line digital computers requires that sufficient information, which is available in the analog form, be digitized and used in decision making. The systems adopted by Mann and Morrison[22,23] and Gilcrest, et al,[12,28] consist of estimating the peak squared values from the samples of instantaneous voltages and currents. The presence of a system fault is detected by cycle to cycle comparison. These techniques, used for extraction of information from sampled parameters, form the core of the protection schemes developed to date and are examined in this chapter.

3.1 Cycle to Cycle Comparison

Mann and Morrison[23] utilized this technique to provide distance protection for a three phase transmission line using a digital computer. In this scheme, voltage and current data is sequentially sampled fifteen to forty times per cycle and is stored in the computer memory for at least one electrical cycle. The sampled values of the line current are compared with those stored during the previous cycle. Any deviations of sufficient magnitude cause the program to enter a mode where it suspects the existence of a possible fault. The program attempts to classify the fault while the computer continues to update the transmission line parameter information. Suitable calculations then determine the validity of the suspected fault condition and an appropriate action is initiated.

The technique appears attractive but it does have several drawbacks for differential protection applications. For adequate differential

protection sensitivity, the protection scheme must be able to distinguish between faulted and non-faulted conditions with cycle to cycle differences in the order of one percent. To achieve this sensitivity, the sampling must either be carried out at high speed or it must be synchronized to the system frequency. For instance, in a non-synchronized data sampling system, the reciprocal of the maximum rate of change of the sampled parameter,multiplied by the maximum allowable error in absolute terms,will yield the maximum permissible time between samples. For an accuracy of one percent on a sixty Hz sine wave, the time between samples should not exceed thirty microseconds. Because this sampling rate is excessive for practical systems, a synchronized scheme should be considered.

The emphasis now shifts to the problem of accurately determining the zero crossings of a parameter for synchronized sampling. The data may be sampled at any rate and suitable corrections computed to relate its value to fixed times with respect to the zero crossings of the parameter. Alternatively, suitable synchronized sampling would insure that each sample retains a fixed orientation to the zero crossing. This method will make no additional demands on the computer if the required sampling control is provided externally. In either case, synchronization would have to be applied to each parameter separately, especially where unbalanced fault conditions may be experienced.

For the system under consideration, the fault current has such ill-defined zero crossings as to render it unsuitable for synchronized data aquisition. The stator current would generally include a D.C. transient component and any synchronized sampling scheme would be susceptible to serious error. On these grounds the synchronized sampling scheme is not suitable for differential protection.

3.2 Computation of Peak Values

Gilcrest, Rockefeller and Udren[12] and Mann and Morrison[22,23] estimate the peak values from the samples of instantaneous voltages and currents. The technique is based on the trigonometric algorithm, $\mathrm{Sin}^2\theta + \mathrm{Cos}^2\theta = 1$. This equation may be expressed as $(A\sin(\omega t))^2 + (A\cos(\omega t))^2 = A^2$ in terms of amplitude, frequency, and time variables. The sampled value of the sinusoid at time, t_1, provides the term, $A\sin(\omega t_1)$. The term, $A\cos(\omega t_1)$, is computed from the rate of change of the sinusoid at t_1 and the angular velocity, ω. The technique relies on the computer's ability to generate the derivative of a given parameter.

In theory, the algorithm works fine except that the accuracy of this technique depends on the sampling rate. This aspect is not fully reported in the published literature. The accuracy of the generated time derivative and the computed peak squared values were investigated.

The following assumptions were made for computing the time derivative of an input sinusoid:

i) The sampling frequency, F_s, is constant.

ii) The input function is an undistorted, constant amplitude and frequency sinusoid.

The samples are subscripted such that the lowest subscript denotes the latest sample as illustrated in Fig. 3.1.

The algorithm used to calculate the latest value of the first differential, f'_n, was based on the equation,

$$f'_n = (f_n - f_{n+1})F_s + 0.5((f_n - f_{n+1})F_s - (f_{n+1} - f_{n+2})F_s)$$

$$= (1.5f_n - 2.0f_{n+1} + 0.5f_{n+2})F_s. \qquad (3.1)$$

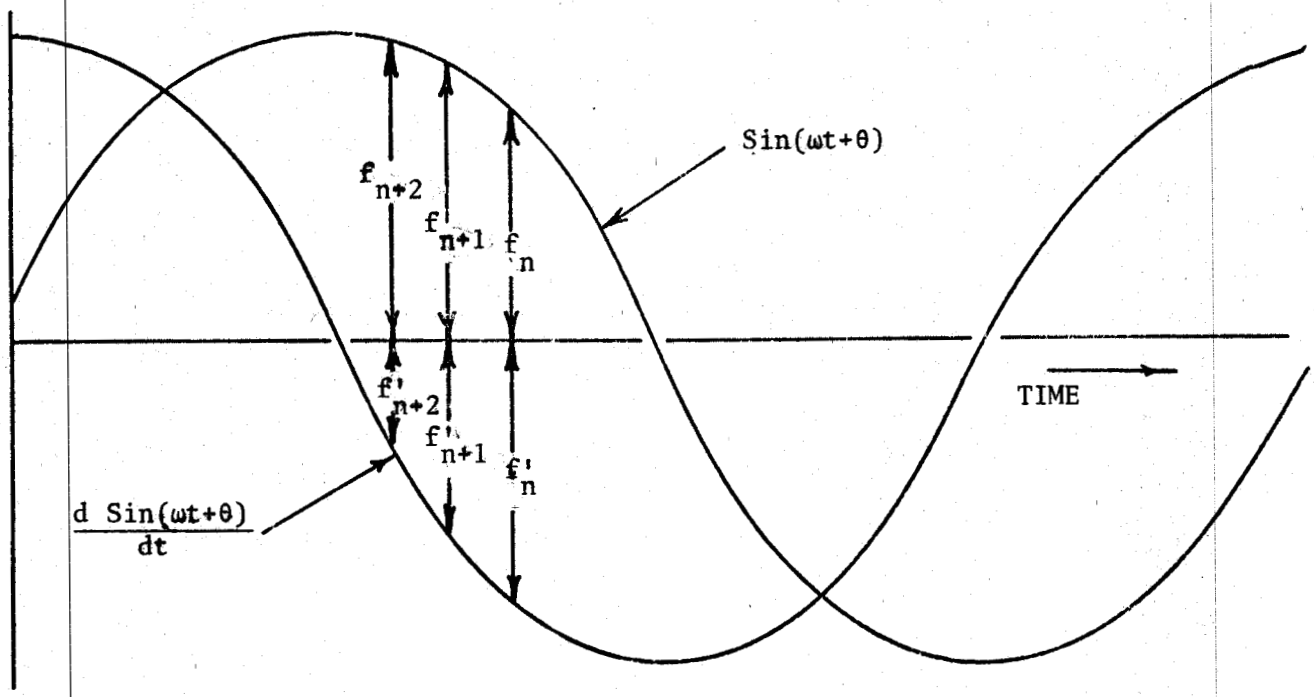

Fig. 3.1 A typical segment of an input parameter and its first difference.

3.3 Evaluation of Computation Technique

An input function, 10 sin 377t, was generated in the digital computer. The sampling frequency was increased from 100 Hz to 10 kHz and equation 3.1 was used to compute the first derivative at each sampling time. The first derivative of the input, (3,770)Cos 377t, was also generated. For each sampling frequency, the computed and generated first derivatives were compared and percentage errors were calculated. The maximum percentage error as a function of sampling frequency is shown in Fig. 3.2. This study indicates that sampling frequencies of 2 KHz or higher should be employed.

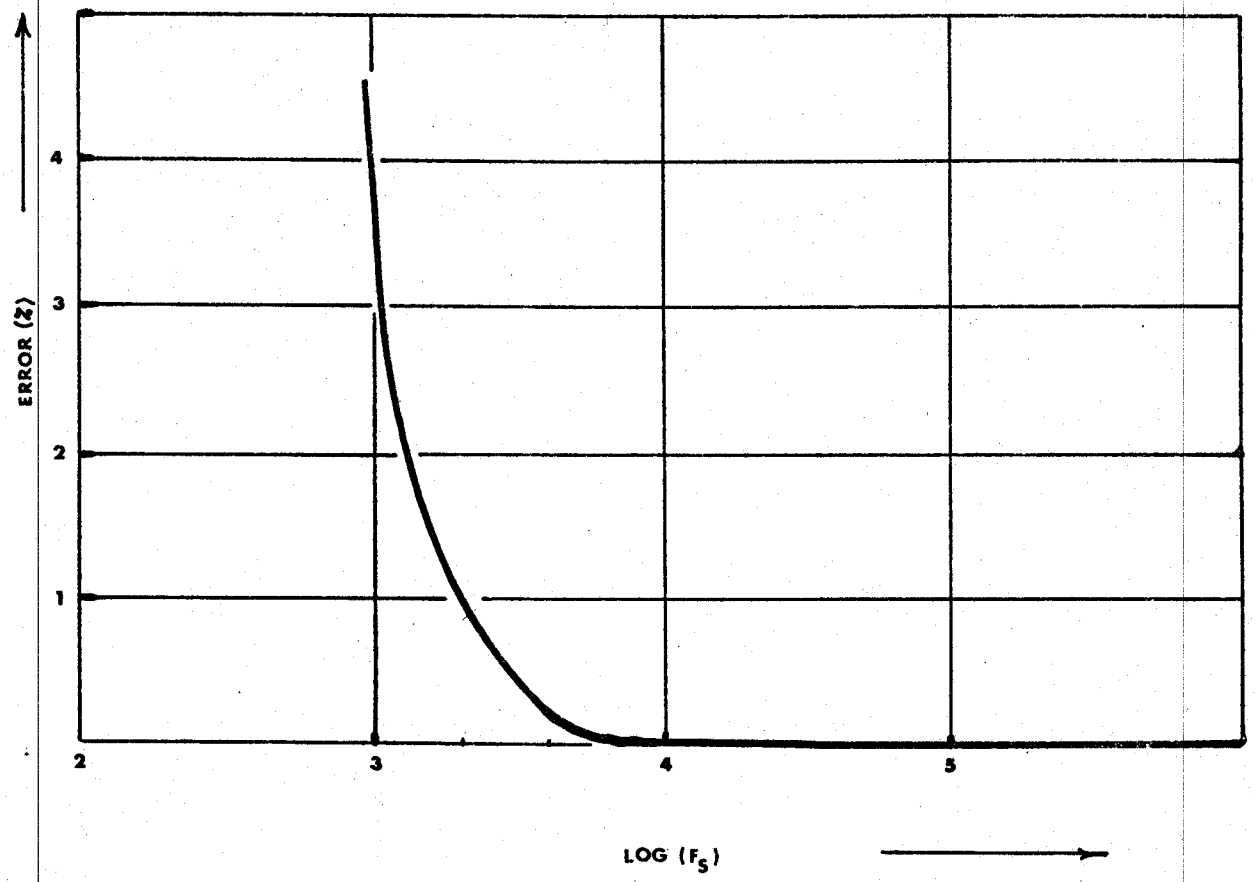

Fig. 3.2 The maximum percentage error of the computed first derivatives versus sampling frequency.

The accuracy of the peak values computed from sampled data was then examined. An input of 0.5 Sin 377t volts was applied to the computer through an analog to digital (A/D) convertor as shown in Fig. 3.3. The peak squared value of the input was calculated using equation 3.2.

$$A^2 = (f_n)^2 + \left(\frac{f'_n}{\omega}\right)^2 \qquad (3.2)$$

Substituting the value of f'_n from equation 3.1, equation 3.2 becomes

$$A^2 = (f_n)^2 + (1.5f_n - 2.0\, f_{n+1} + 0.5\, f_{n+2})^2 \left(\frac{F_s}{\omega}\right)^2 . \qquad (3.3)$$

A sampling frequency of 8.5 kHz was used to make $\left(\frac{F_s}{\omega}\right)^2$ equal to 2^9, a mathematical software convenience. The peak squared values were calculated at each sampling time for about two cycles of the input voltage. These

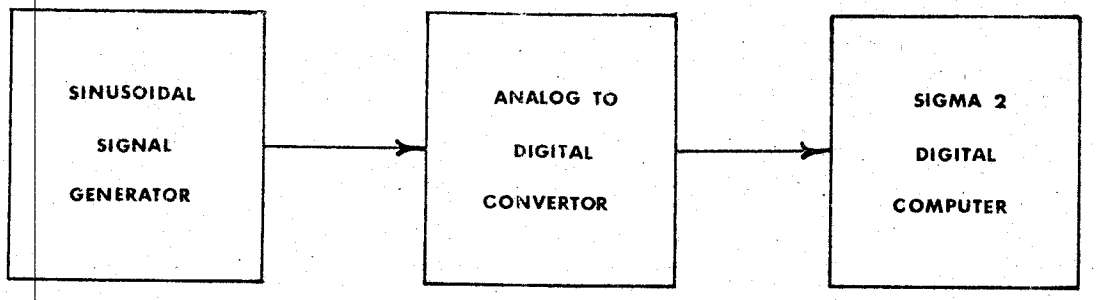

Fig. 3.3 Equipment configuration to compute the peak squared value of a 60 Hz sinusoid.

values were stored in the computer memory and printed at the end of the test period. The calculated peak squared values are plotted as a function of time in Fig. 3.4. The input wave form is also shown to correlate the errors with the sampling points on the wave. The digital computer program written in extended-symbol is given in Appendix I for reference.

The excessive errors, those ploted off scale in Fig. 3.4, resulted from missed samples. This was attributed to the sampling frequency being too fast for the digital computer to handle at times. The missing sample caused a pseudo-discontinuity in the input function, which illustrates a serious inadequacy of the technique. This method is based on the assumption that the input is a single frequency function which, of course, is not true for most power system parameters, especially during fault transients. The technique may be used in cases where the frequency components can be separated and handled individually, or where action

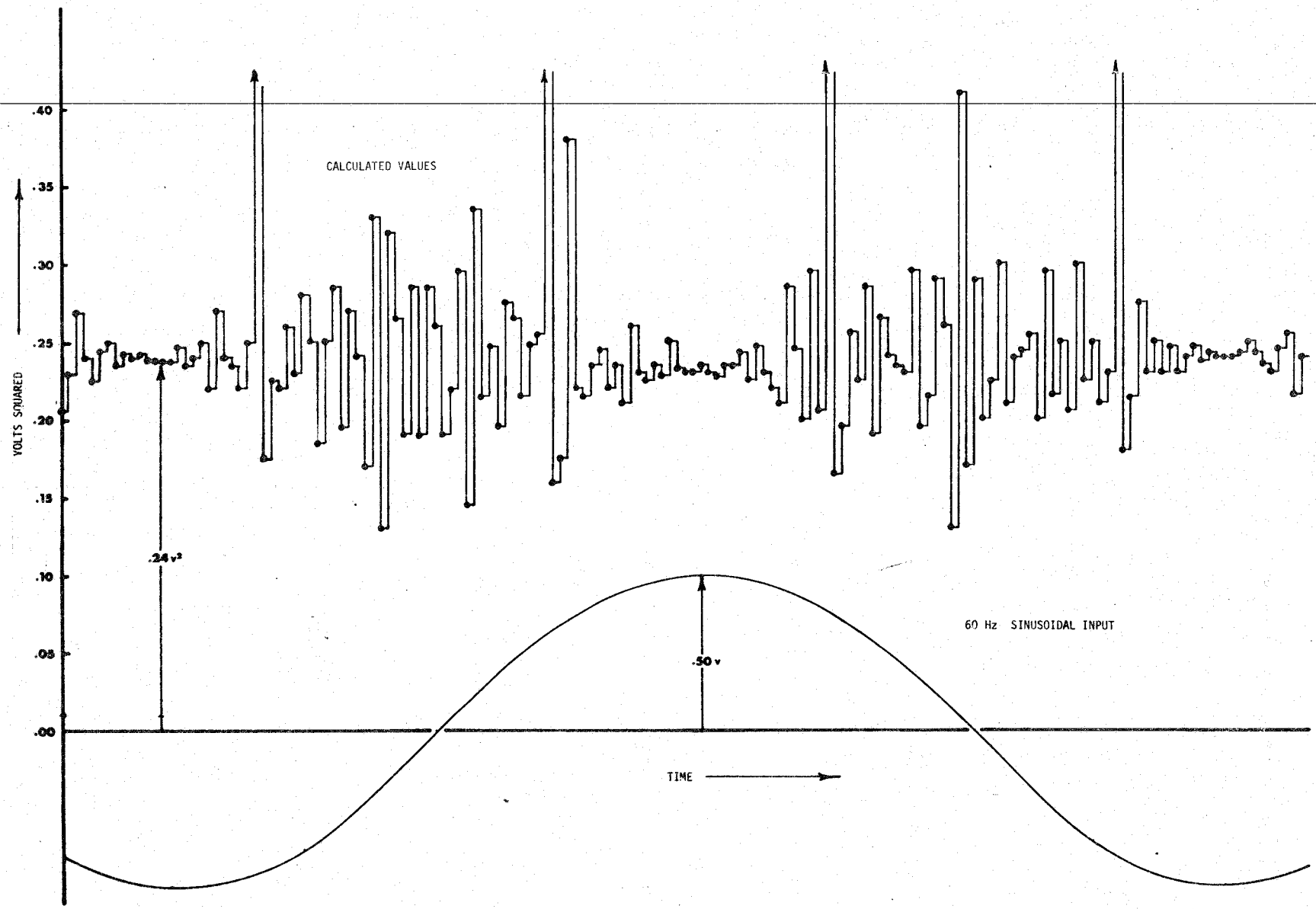

Fig. 3.4 Correlation diagram of the 60 Hz input sinusoid and the computed peak squared values.

can be delayed until all the undesirable frequency components have attenuated. In view of these difficulties, this technique was not used for differential protection of generators.

The perusal of Fig. 3.4 shows that the errors are of two levels of significance. The smaller errors are due to the inaccuracies of the A/D convertor used. The error associated with the least significant bit is two percent of the peak value of the applied input voltage. It is noticed that the errors of the calculated peak squared values are relatively greater when the rate of change of the input signal is maximum. This is due to the input signals being quite small near the zero crossings when the error associated with the least significant bit becomes increasingly important. The solution to this problem lies in optimizing the conversion rates and in using a more accurate A/D convertor.

The cycle to cycle comparison concept for fault detection has been examined. A method for calculating the peak squared values from sampled information has been presented and investigated. Both techniques proved to be unsuitable for differential protection of generators.

4. ON-LINE COMPUTER PROTECTION DESIGN CONCEPTS

Several possibilities were examined to efficiently harness the inherent digital computer characteristics. Those important to power system protection applications, are outlined. A time shared concept is presented as an alternative to a dedicated digital protection approach. Advantages of analog pre-processing of input information are also discussed. The adopted organization of the stator protection scheme is presented along with various conceptual options applicable to on-line digital computer protection design.

4.1 Digital Computer Characteristics

A digital computer is a device which manipulates numbers according to established rules. Recent developments have increased the data handling speed and it is now possible to process a large number of parameters as they are generated. A system may be controlled by an on-line digital computer using outputs derived from these parameters. The input information handling capability and the control function generation is limited by the computation and conversion speeds. Although there is no basic difference between the digital computers used on-line and those used off-line, variations do exist in the form of number and types of input devices provided, the relative sizes of the direct access memory, and the speed and flexibility of the central processor.

The major advantage of modern electronic digital computing machines is their inherent flexibility which arises from an ability to perform conditional branches. Conditional branching, based on the comparison between two numbers, enables the computer to change the sequence or priorities in executing different functions in a plant. Digital computers are also able to choose the events for analysis based on decisions made

using the criteria provided. A digital computer is not limited only to performing manipulations on numbers according to established algorithms based on conventional mathematics. It may, therefore, be able to generate control functions which may not be realizable in analog devices. Another advantage of considerable importance is the computer's ability to selectively store information and subsequently reproduce it in various hard and/or soft copy forms. Off-line analysis may also be incorporated to provide a more sophisticated output.

The computation and conversion speeds, as already mentioned, are finite and it is, therefore, impossible to generate all conceivable control functions within the time available in an on-line application. However, a very simple technique may often be used to approximately generate an otherwise complicated function to reduce the computation requirements. The computer may have to be located away from the plant to provide a stable operating environment. Some means of communication between the computer and the plant is required. The information processing rate is now also governed by the communications facility provided. Also, the exclusive use of a digital computer for power system protection may not be economically justifiable and a time shared approach has, therefore, been advocated.

4.2 Multi-purpose Computer Rationale

Protection systems are required to operate only occasionally. The flexibility of digital computers enables their application to power system protection in a time shared mode. A considerable amount of computing capability is required during faults. On other occasions, a major part of this capability could be assigned to other on-line and/or off-line applications. Also, communication between the various computer tasks could be advantageously implemented to improve system operation. The

design of the protection scheme should, therefore, be such that it can be adapted to a time shared computer. Fig. 4.1 shows a protection scheme based on this multi-purpose concept.

4.2 a) Executive program

The primary element linking a protection program to the computer software will be a control sequence. It should select the various tasks on the basis of their importance to improve the system performance. The decisions should be made by considering the information, provided by an operator, calculated by the computer and/or provided by the protected system. Since the protection function will, of necessity, be the highest priority in the computer hierarchy, the control sequence must be closely linked to the various fault monitors.

4.2 b) Fault monitors

The monitors should be continually called upon to examine pertinent parameters to determine the possibility of the system being abnormal. If so detected, the controller would execute the required fault determining routines. This technique would be modified to adopt a system's approach as the technology develops. The controller should also communicate useful information between the monitor and the other programs in the computer memory. In addition, it must save the data which may be required by the monitor on a subsequent pass.

4.2 c) Zone and phase allocation

In case of an abnormality, a routine to localize the fault condition would be initiated. The zone allocation routines should determine the most likely involved element and the affected phases. These routines can receive data from the system at much higher rates than would be advisable

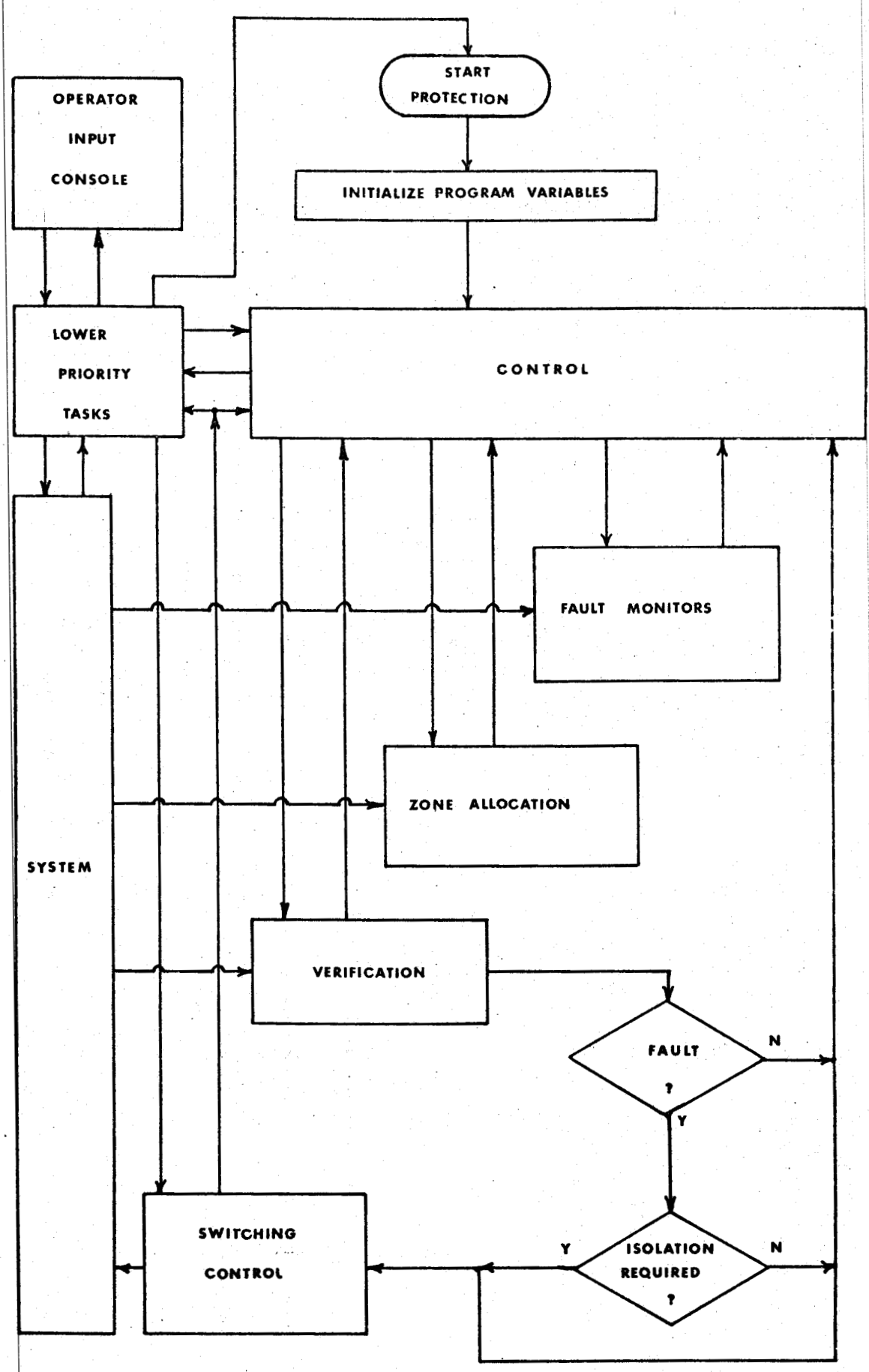

Fig. 4.1 The logic organization of a digital protection scheme in a time shared mode.

for the monitor. The allowable decision making time will be the main criteria for this speed. Allocation routines should simplify the fault monitors and improve the overall computer efficiency. While the disturbance is being allocated a zone,the protection of other system elements should not be completely neglected. The allocation should be indicated to the control which will then activate the appropriate fault verification routines.

4.2 d) Fault verification

The fault verification routine must establish whether the condition warrants any action. A large variety of verification routines will have to be incorporated to provide for all possible faults. The routines relating to severe faults should reside in core memory while others could be stored on magnetic tape and/or disc for transfer to the active memory as and when required. The continuity of protection provided for all elements must be ensured while a particular possible fault is being verified.

4.3 The Hybrid Computer Rationale

Employing analog computing techniques could simplify the overall protection scheme. This would be an especially important consideration in monitor design. The operating functions of protection schemes should be derived from the available system parameters. For example, the relay operating current in a differential protection scheme may either be computed or derived using analog methods. If it is digitally generated, some error will result. On the assumption that the system is operating without a stator fault, the line and neutral end currents, of a particular stator phase, have the same amplitude and phase angle. The minimum error is similar to that due to sequential sampling of a single sinusoid. The maximum error will occur as the function passes through zero. The

sampling frequency would have to be greater than 100 kHz for accuracies better than one percent. The percentage differential protection schemes have operating characteristics which demand such accuracies. Using sampling rates of this order will not leave sufficient time for computation. A sample and hold circuit used in conjunction with the A/D convertor is one possible solution while a parallel A/D conversion system is another. An analog device could also be used to process the line and neutral end currents in parallel. The phase delays are similar for both channels and as such do not result in significant errors. Analog devices may, therefore, be used to reduce the sampling frequency requirements.

4.4 Design Concepts Applied to Differential Protection

The digital stator protection scheme was adapted to a time shared approach by structuring the organization as shown in Fig. 4.2. Various operating alternatives ranging from parameter selection to data processing were examined for the fault monitor, the phase allocation and fault verification sequences. The explanations, which accompany the selected alternatives form the theoretical framework for the digital protection scheme.

4.4 a) Fault monitor

As already discussed, the monitor sequence execution time should be as small as possible. Several options were available when the monitor was being designed. The most basic option was the choice between parameters on which to base its operation. Only two parameters, stator currents and terminal voltages, were readily available on which a simple monitor could be based. Several different combinations of both the current and voltages were also possible. For example, either the terminal voltage of each individual phase could be checked periodically or the instantaneous sum

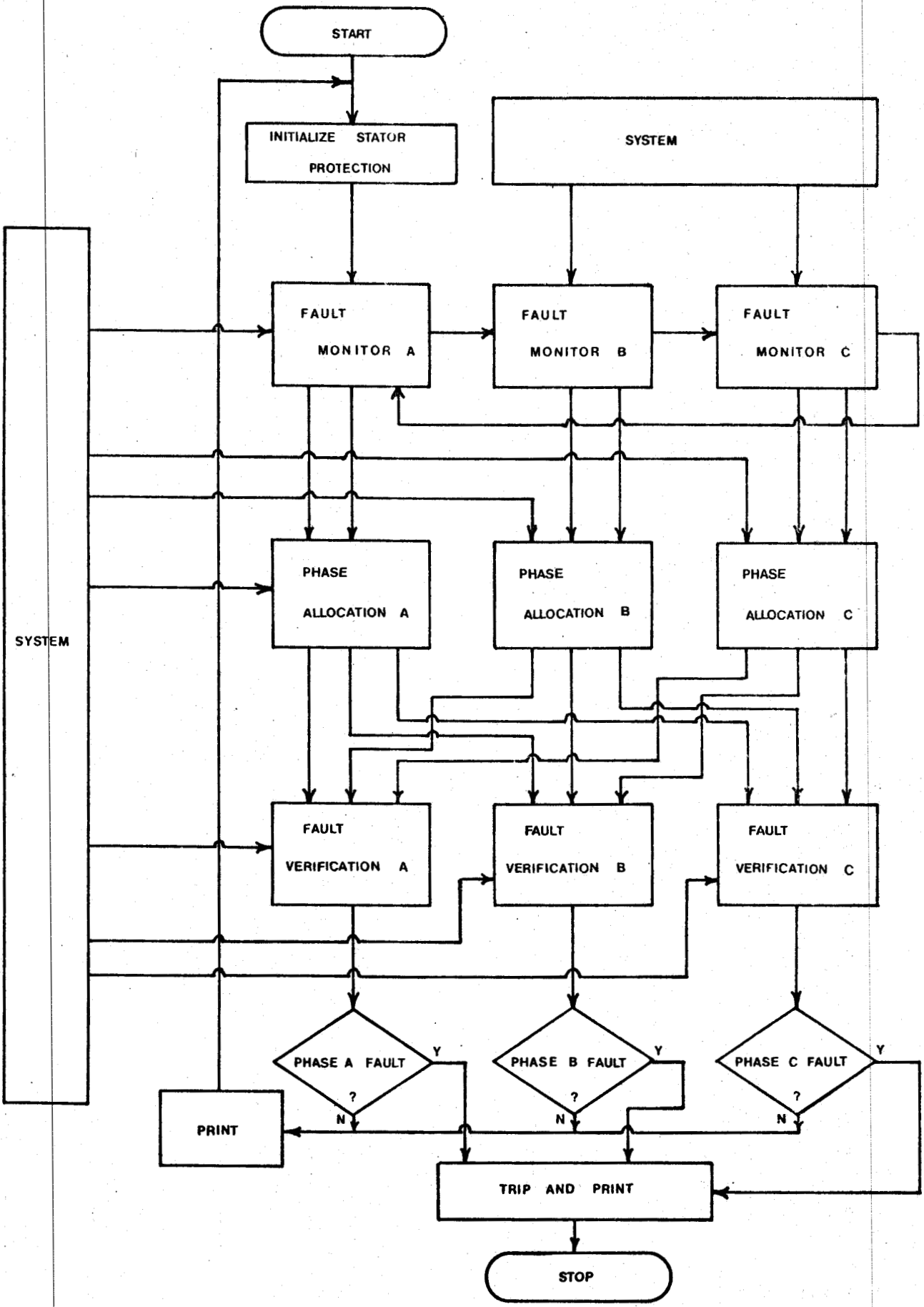

Fig. 4.2 The logic organization of the proposed digital percentage differential protection scheme.

of the three terminal voltages could have been used in a detection scheme. The generator terminal voltages will include a zero sequence component during unbalanced faults. A sample to sample comparison technique or an amplitude threshold detection system might be employed. Balanced faults and faults involving only a small percentage of the winding will have only a small zero sequence component. In addition, external unbalance would have similar effects. The individual phase voltage variation would also be experienced due to internal and external changes. Also, using voltages as the detecting parameters would involve digitizing more signals. This parameter was therefore rejected for fault incidence detection.

The methods using the stator currents for detecting the incidence of a fault were then examined. Using the currents at the line and neutral end of the generator winding which are both available, the following options are possible for the monitor design.

i) The instantaneous sum of the three phase currents (equal to zero for normal balanced conditions) at the line end, the neutral end, or their sum could be monitored as one parameter.

ii) The currents in each phase either at the line end, the neutral end, or their sum, could be periodically examined.

iii) The instantaneous difference between the line and neutral end currents, in each phase, could be checked.

iv) The instantaneous sum of the three difference currents measured in option iii) could be periodically examined.

Both i) and ii) above are sensitive to changes internal and external to the generator. This could be used when a monitor is required to detect external as well as internal disturbances. In this application, the monitor will initiate checking even when the system load changes. To avoid this, the detection criteria will have to be increased thereby compromising the sensitivity of the scheme. Method iii), employed in percentage differential protection schemes, overcomes this difficulty and is more suited to

protect against stator faults. The principles of this scheme have already been discussed in Chapter 2. Its basic operation is similar to that of a differential amplifier. The principle of instantaneous summation of the three difference currents, iv), has some merit because it is as sensitive to stator ground faults as is method iii). In addition, the monitor requires only one operating parameter instead of three as for iii): but it is insensitive to faults not involving the ground loop. This problem might be solved by making the currents of each phase artificially different from other phases. While most faults will involve ground, a distinct possibility exists that the generator may experience a two phase fault. For these reasons, method iii) was implemented in the monitor design.

A cycle to cycle comparison technique was discussed in paragraph 3.1. It was noticed that, though it has been used in transmission line protection, it is not suited to stator differential protection. The change of difference current between consecutive samples could be an alternate detection principle. The increase of this current at the inception of a fault may be quite small. Should the terminal voltage be passing through zero at the time, the change in the initial difference current will be difficult to detect. The condition is alleviated somewhat because the parameter will undergo its maximum rate of change four milliseconds later. The technique was tested to examine its ability to detect the onset of a fault. The detection time was found to be variable and depends on the incidence angle and fault severity.

The monitor could also be based on the amplitude of the difference current being in excess of a software threshold. This technique is also subject to delays due to the nature of the stator fault current describing function presented in Chapter 2. However, these delays are significant

only for marginal fault conditions. The estimated maximum delay would be similar to that in the operation of a monitor based on the first difference of the fault current. The software threshold technique is simpler and was therefore adopted for the monitor design.

4.4 b) Phase allocation sequence

In generators, capacitive coupling exists between the stator phases. At the inception of a fault, high frequency leakage currents flow in all stator phases while the capacitors discharge. These currents bear a proportional relationship to the severity of the fault and the first evidence of a severe fault may, therefore, appear on a healthy phase. By simply allowing the first sample which exceeds the monitor threshold, to indicate the possible faulted phase, verification may commence incorrectly.

A fault allocation sequence was included in the protection package to improve the utilization of computer time by increasing the probability of correctly selecting the faulted phase. This sequence, beginning with the first sample of difference current that exceeds the monitor threshold, compares consecutive samples from the three phases. In each set of three, the largest sample is taken as an indication that its originating phase is faulted. The first phase to indicate the largest difference current on two occasions is selected as the phase most seriously involved in the fault.

4.4 c) Fault verification

As indicated in paragraph 4.2, the fault verification sequence executes the sampling and calculations necessary to adequately determine the existence of a fault. The difference current, which represents the fault current, and the restraint proportional to the average through current were used to verify the presence of stator faults in view of the advantages

of this approach discussed in Chapter 2. While designing the computerized percentage differential protection scheme, techniques to minimize the errors due to fault transients were incorporated. In addition, the decision time for serious faults was reduced as much as possible. It was, therefore, essential to process as much of the frequency spectrum of a fault signal as possible.

The transient response analysis of the fault current, also presented in Chapter 2, indicates that, while the difference current must rise from zero with a rate restricted by machine and fault parameters, the sum current ($I_1 + I_2$ of Fig. 2.4) does not. A modified function was generated from the sum current to match the transient response of the difference current. This function enables a comparison of the operating and restraining currents even during the transient period. An approximate first order transfer function was used to generate the modified sum current parameter. The desired transfer function may be written as $G(s) = \frac{1}{1+Ts}$. For a given sampling rate, R(n), the sum current modified by the transfer function at the end of the nth sampling interval, for the input, I(n), is given by:

$$R(n) = R(n-1) + K(I(n) - R(n-1)) \qquad n = 0, 1, 2, 3, \ldots\ldots$$

$$= 0 \qquad ; \qquad n < 0 \qquad ; \qquad 0 < K < 1 \qquad (4.1)$$

If a step input of amplitude A, is applied at n = 0, the output, R(n), may be expressed as:

$$R(n) = \frac{A + (P-1)\,R(n-1)}{P} \qquad ; \qquad P = \frac{1}{K} \qquad ; \qquad P > 1 \qquad (4.2)$$

This function is depicted in Fig. 4.3 for a sampling interval of s seconds and for P = 2. It is apparent that the output approximates the exponential,

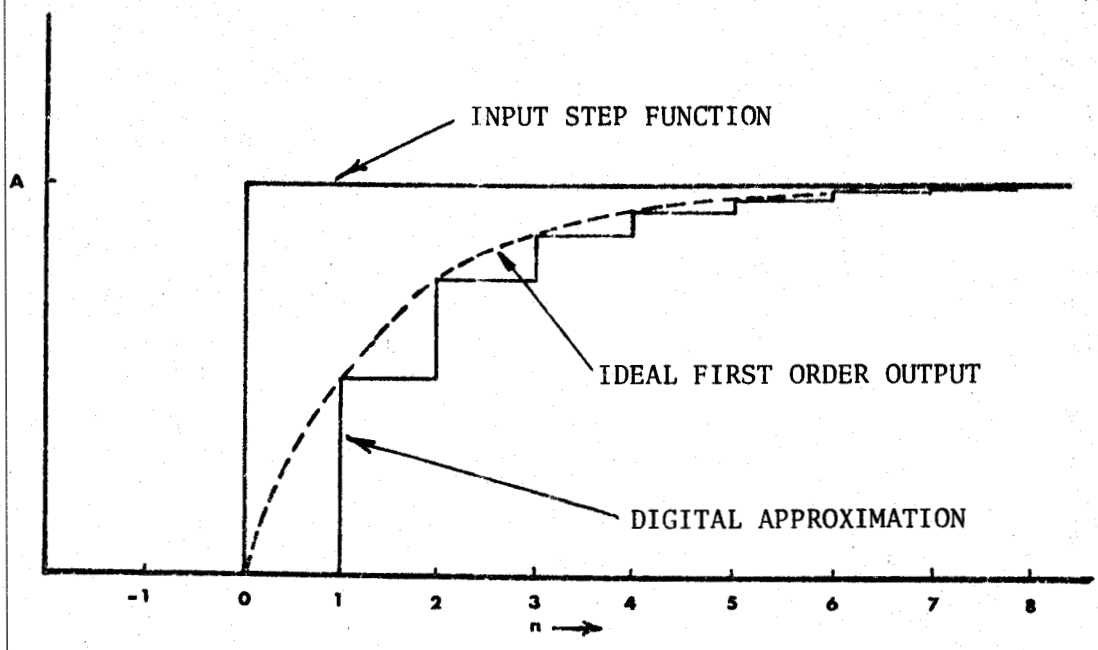

Fig. 4.3 The digital and ideal outputs of the first order system for a step input.

$A(1-e^{-\frac{sn}{T}})$. The time constant, T, depends on the sampling rate and the value of P used. It may be derived by equating the output at n=1 and the value of the exponential at t = s and is given by

$$T = \frac{s}{\ln(\frac{P}{P-1})}$$

The generated transfer function is very easy to implement and its accuracy is governed by the sampling rate and the time constant required. The difference current accuracy is also governed by similar factors. Errors in the difference current and the simulated function tend to cancel because they are of the same type and are governed by the same factors.

The technique, advanced above, will allow the processing of stator input data without waiting for the transients to attenuate. Fig. 4.4 illustrates the modified sum and the difference currents for a marginal fault. The sum current is also shown for comparison with the modified function. The modification of the sum current is provided to overcome the

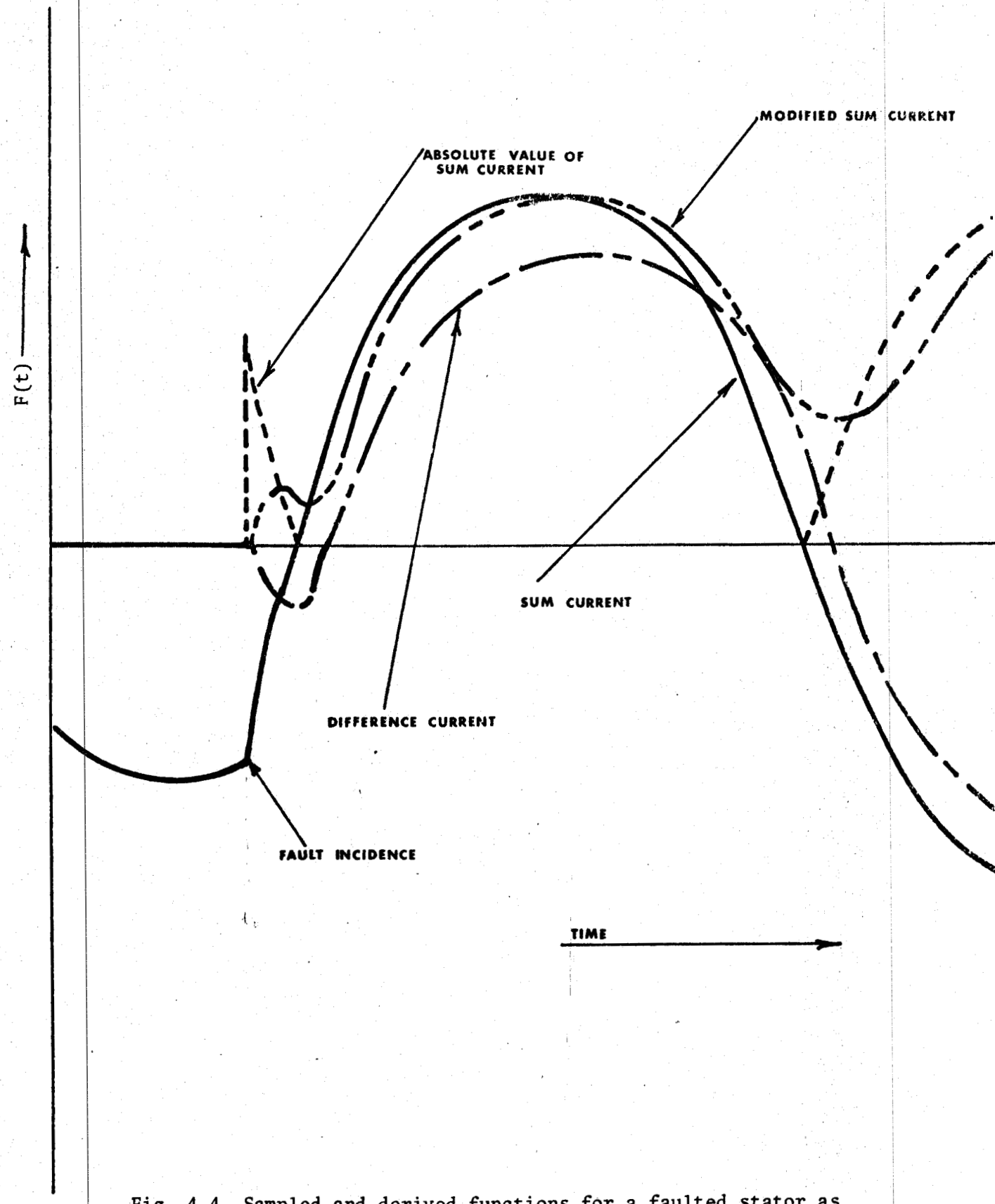

Fig. 4.4 Sampled and derived functions for a faulted stator as used by the protection scheme.

difficulties presented by transients generated during marginal fault conditions. For more severe faults, the fault current transients do not influence the computer's decision.

Time sharing the facilities, either among the various protection functions, required by a power system, or among on-line protection and control functions, may economically justify the application of computers to system protection. Analog pre-processing the input information may still be needed to reduce the digitizing capability of computers applied in this area. A judicious blend of both types of information handling will ultimately provide an attractive computer package for on-line power system protection and control. The proposed organization for the stator protection scheme is conveniently adaptable to the time shared hybrid concept. The adopted fault monitor design is simple yet efficient. Its sampling rate and detection threshold may be adjusted to meet the eventual needs. The design principles of the phase allocation and fault verification functions will commit more computation capability to the protection function as the need arises. In addition, these sequences have been conceived to take advantage of digital computer data processing speeds to ascertain the existence of stator faults faster than conventional relays.

5. DIGITAL PROTECTION SYSTEM DESCRIPTION

The purpose of this project was to examine the feasability of using general purpose computers for percentage differential protection of alternators. Secondly, it was to provide experience in digitizing and processing power system parameters for future on-line computer applications. The SDS Sigma 2/AEI TR-48, situated in the Control Engineering Laboratory, was employed and is described in this chapter. Concepts, presented in Chapter 4, are explained in terms of the hardware and software used in their implimentation.

5.1 Digital Computer Facility

The SDS Sigma 2 was selected for the work reported in this thesis. This computer is located in the Engineering Building and includes a multi-channel, 11 bit, signed, analog to digital convertor. The maximum A/D conversion rate is 15 kHz and the converted information is accurate to one part in a thousand. The digital computer, SDS Sigma 2, is a sixteen bit machine able to handle programs on a priority interrupt basis. It is also associated with an analog computer, the EAI TR-48, which was used to pre-process the input information. Technical advice on operating the computer facility was copious and readily available. All these features, contributed towards the selection of the SDS Sigma 2/EAI TR-48 hybrid facility, for this work.

5.2 Analog Pre-Processing System

The main function provided by the analog computer is the derivation of the sum and difference currents of each generator phase from its line and neutral end currents. The analog circuit for a single phase is shown in Fig. 5.1. The circuits of the other two phases are identical. Amplifiers, A1 and A2, in conjunction with potentiometers, 1 and 2, comprise the variable

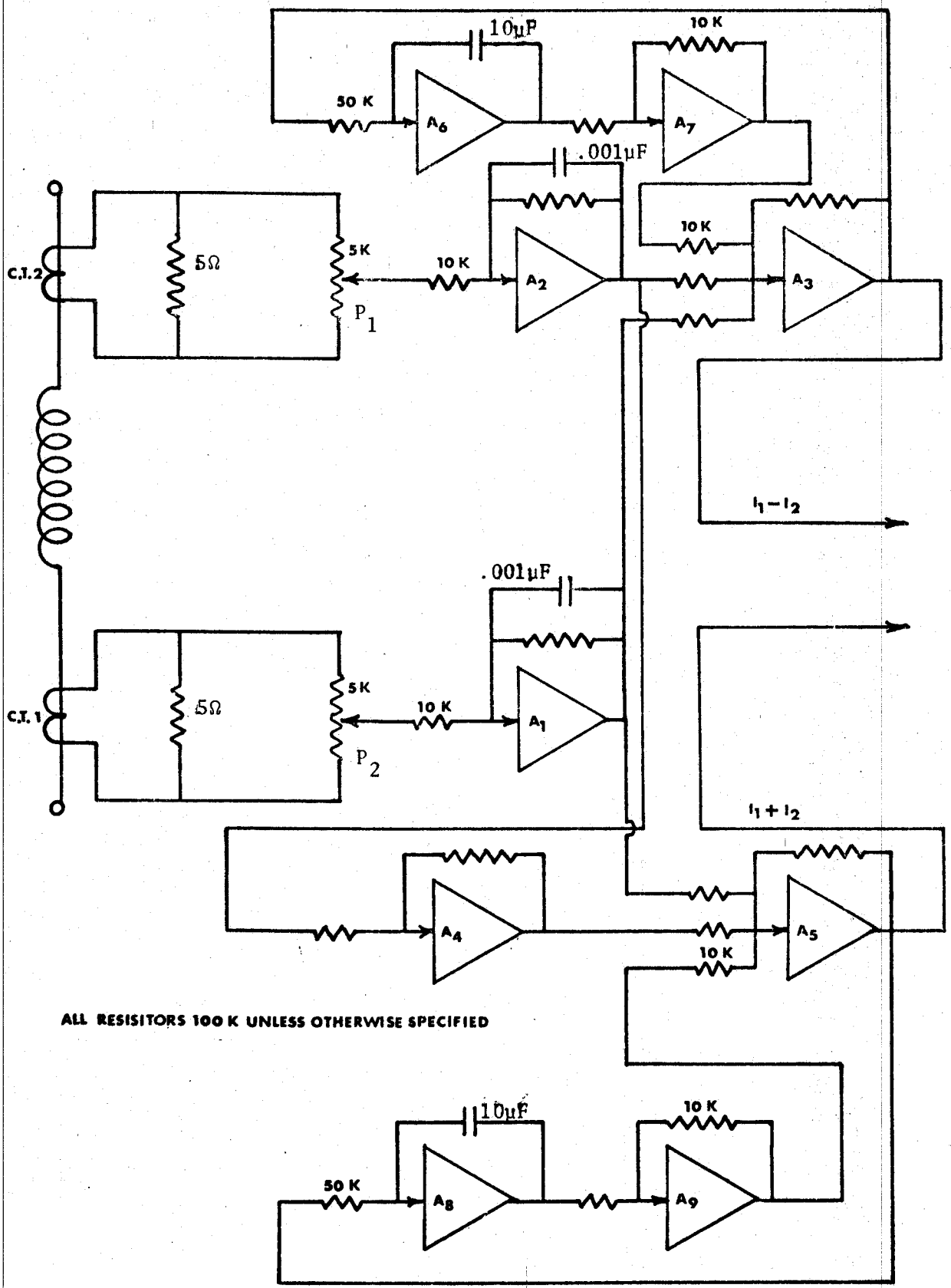

Fig. 5.1 Analog pre-processor schematic diagram.

gain amplifiers to compensate for any imbalance in the current transformer circuits. The amplifiers also provide full utilization of the dynamic range to improve the signal to noise ratio. Amplifier, A3, is a summing amplifier whose output is proportional to the difference current. Any tendency towards a D.C. offset error at the output terminal of A3 is compensated by integrator, A6, in conjunction with inverting amplifier, A7. Integrator, A8, and inverting amplifier, A9, provide a similar function for summing amplifier, A5. Amplifier, A4, inverts the phase of the current, I_2, to facilitate its addition to the current, I_1, in the summing amplifier, A5. High and low frequency roll offs are provided at 1.59 kHz and 0.318 Hz by the 0.001 μF and 10 μF capacitors respectively. The frequency response for both the sum and difference currents is flat between .318 Hz. and 1.59 kHz. and rolls off at 20 db per decade as depicted in Fig. 5.2.

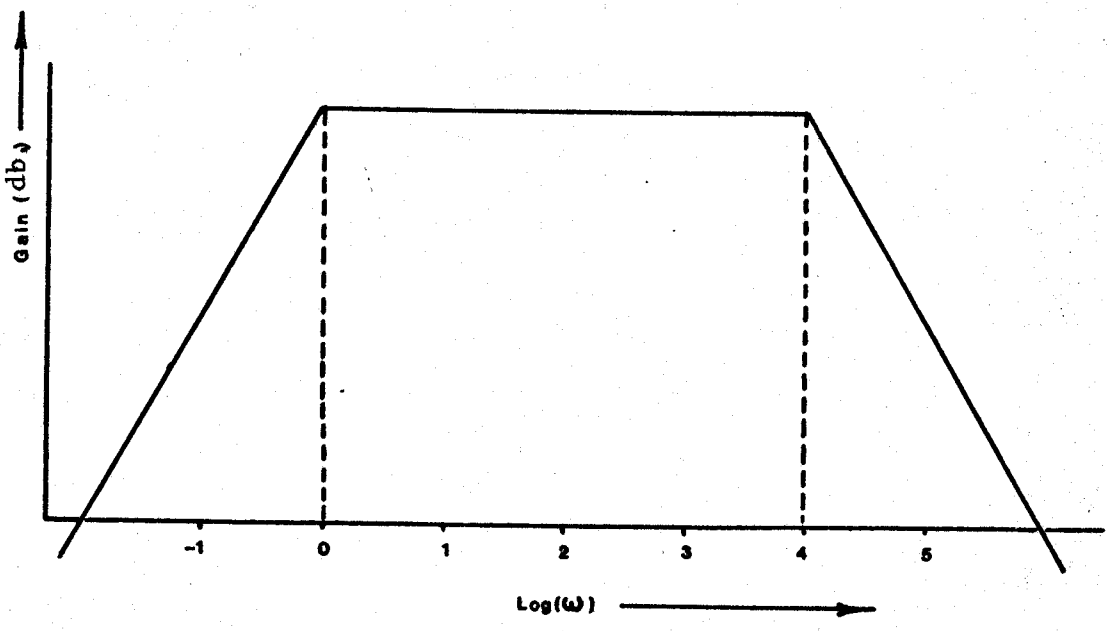

Fig. 5.2 Frequency response for both the sum and difference currents generated on the analog computer.

The maximum signal swing, that the analog computer and the A/D convertor can handle, is from -10 to +10 volts. The gain setting is related to the maximum sum and difference currents for linear signal processing. The worst case internal fault condition will depend to a certain extent on the system to which the generator is connected. The total difference current is the sum of the fault currents contributed by the generator and the system. For zero impedance fault just outside the differential protection zone, the sum current is twice the current contributed to the fault by the generator. In addition to the A.C. components D.C. offsets of comparable magnitude may also be present. This could double the maximum current which might otherwise be expected. The gain in the analog computer must be set so that this peak amplitude does not exceed 10 volts to avoid saturating the analog computer elements. The error in the A/D convertor is based on the maximum value which it can convert. In absolute terms, it cannot distinguish between voltages differing by less than 10 millivolts. Failure to use the full dynamic range of the A/D convertor will decrease the signal to noise ratio and, therefore, adversely affect the performance of the protective scheme especially for marginal faults.

5.3 Digital Fault Monitor

The fault monitor issues read directs to the A/D convertor to sample the three difference currents from the analog pre-processor sequentially at 15 kHz and handles this information according to the flow chart of Fig. 5.3. These samples are used to update a table containing the 32 latest samples of the difference current of each phase so that the conditions immediately preceding a fault may be reconstructed to determine what actually happened. The absolute value of the sample just received is stored in

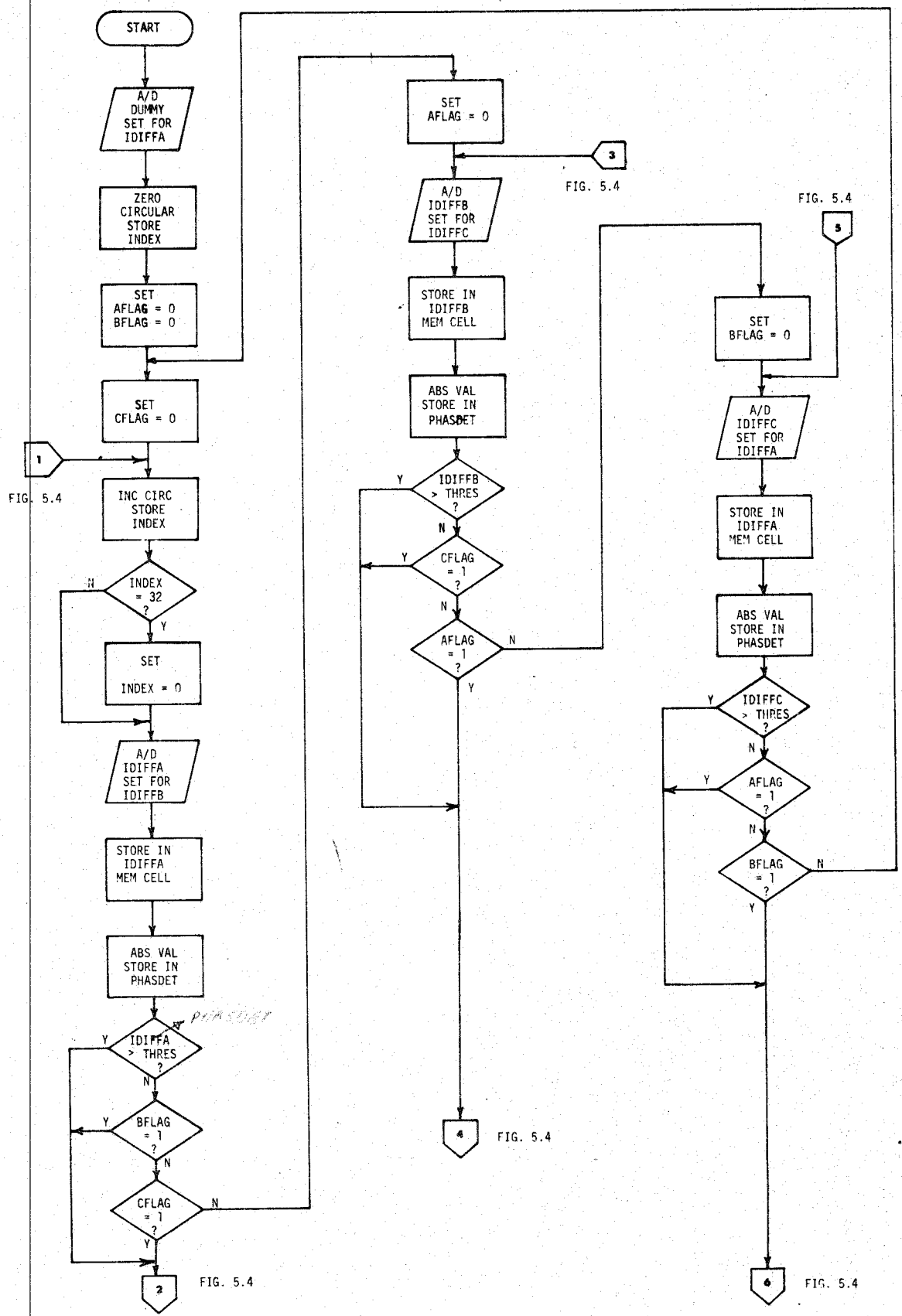

Fig. 5.3 Digital logic flow chart of the three phase fault monitor sequence.

memory location PHASDET and is compared to a provided threshold. Should the amplitude of the sample exceed the threshold, the monitor relinquishes control to the phase allocation sequence.

If the sample is within the threshold limits, control determines whether it was taken as part of the phase allocation routine. If not, the monitor remains active. The next difference current sample is read and the procedure described above is repeated for the next stator phase. After once processing the difference current samples of the three phases, the difference current storage location index is incremented. Every time the location index is 32, it is reset to zero, an action which establishes a circular storage pattern.

5.4 Phase Allocation Sequence

On activation by the monitor, the phase allocation sequence, described by the flow chart of Fig. 5.4, determines the faulted phase (A, B or C). The monitor could have relinquished control if the difference current was in excess of the threshold in a phase, say phase B. This would activate the phase B segment of the allocation sequence. The phase allocation sequence issues a read direct to the A/D convertor to sample the difference current of the next phase, C. The sample is placed in the circular store and its absolute value is calculated. The difference current sample of the next phase, A, is similarly processed. The absolute values of the three samples are compared and the originating phase of the largest is determined. Sequentional sampling continues and the procedure described above is repeated for the next set of samples of the three stator phases. This is continued until the largest samples from different passes twice indicate the same phase as probably faulted. The phase allocation sequence then branches to the appropriate fault verification routine. It is possible

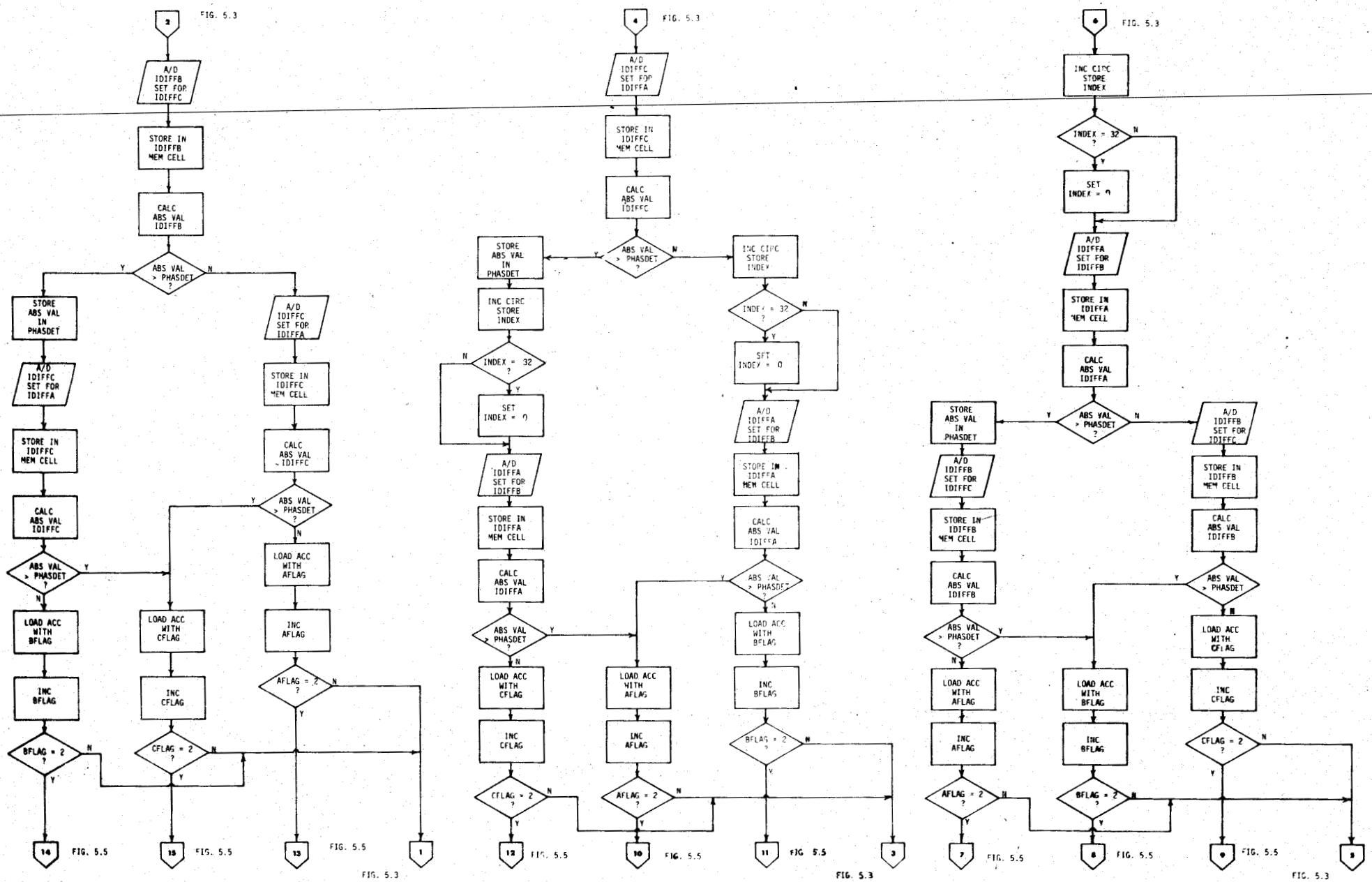

Fig. 5.4 Digital logic flow chart of the phase allocation sequence.

that the difference current of a particular phase, say B, was detected to be greater than the threshold by the monitor and this is also the largest value detected by the phase allocation sequence in the first pass. If the first sample of the second pass, which is also of phase B, is less than the threshold value, the phase allocation is aborted and the monitor is re-activated. Inclusion of this option reduces the scheme's detection sensitivity for high frequency transients.

The three phase allocation routines are similar except that the order of sampling and the point, at which the circular store location index is incremented are rotated. Incrementing the circular store is consistantly carried out just prior to sampling the phase A difference current.

5.5 Fault Verification Sequence

The verification sequence decides whether the generator stator is actually faulted or not. It is presented in the logic flow charts of Figs. 5.5 and 5.6. One verification sequence is provided for each phase and each sequence is only slightly different from the others. On commencement of verification the sampling is aligned with the phase chosen by the allocation sequence, if necessary, by using dummy read directs. Sampling is restricted to the sum and difference currents of the phase selected. The difference current samples are still stored in the circular tables as discussed in paragraph 5.3. Three additional circular storage arrays are included for the sum current samples. Presetting the control parameter, COUNT, and the modified sum current function, SUMSAMP, completes the initialization of the segment. The difference current sample is then read from the A/D convertor. This sample is placed in the circular store and its absolute value is computed. This latest absolute value of difference current is stored in memory location IBCKUP for possible later use in the verification sequence.

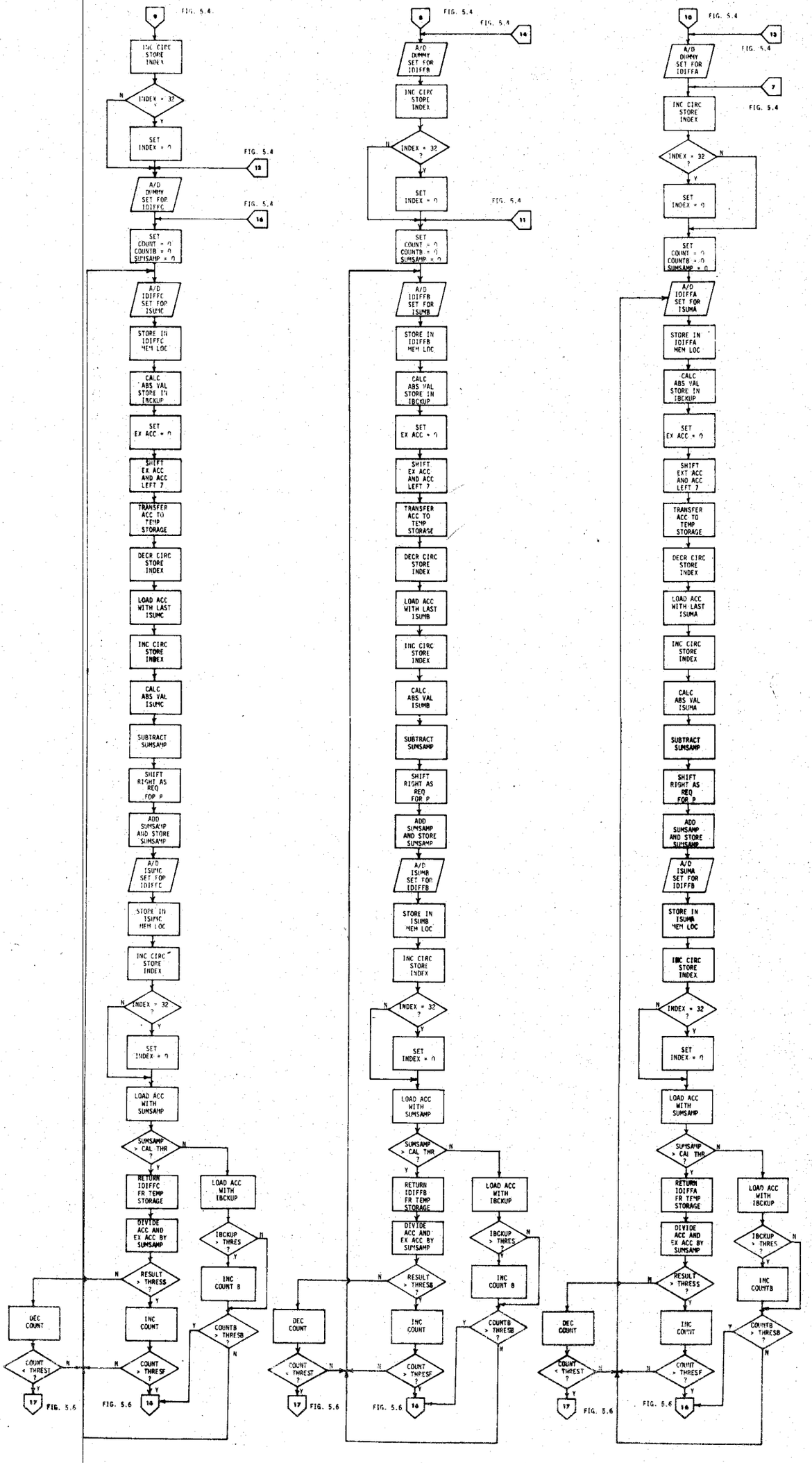

Fig. 5.5 Digital logic flow chart of the fault verification sequences.

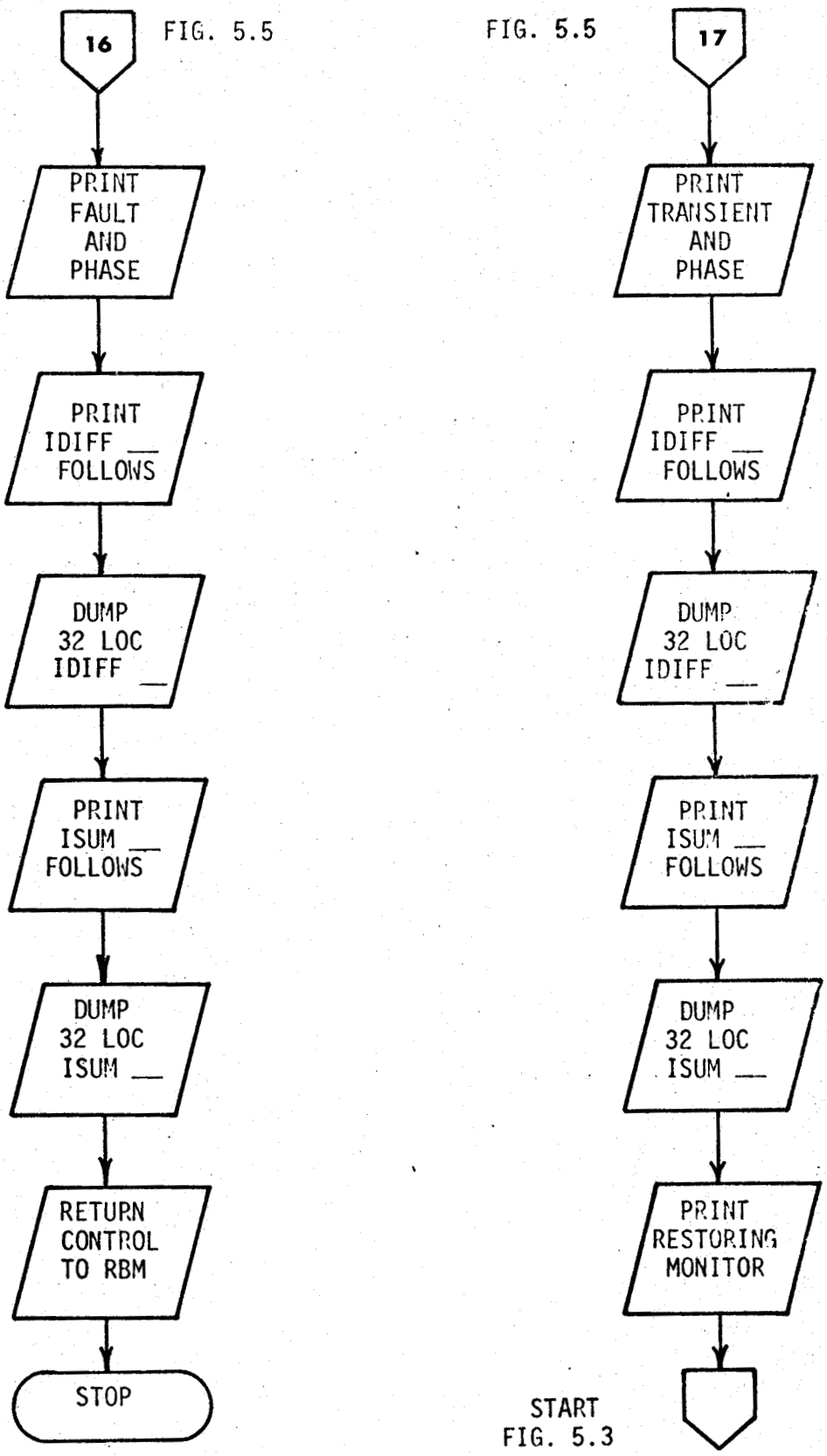

Fig. 5.6 Digital logic flow chart of printing action following verification.

The additional bits provided to extend the accumulator are set to zero and the absolute value of the difference current sample is then multiplied by 128 using an arithmetic left shift of seven bits. Now the contents of the accumulator are temporarily stored in an available register and the value of the last sum current sample is retrieved from the appropriate location in its circular storage table. Using the algorithm described in paragraph 4.4 c), the new modified sum current value is computed. Next, the sum current sample is read from the A/D convertor. In the initial few passes, the value of the modified sum current could be small and any division by this number could generate register overflows. A deadband is, therefore, provided and divisions are not allowed unless SUMSAMP exceeds a threshold. Should SUMSAMP be less than the calculations governing threshold, called "calculation threshold", the sequence returns for the next difference current sample. If the threshold is exceeded on any pass subsequent to the first, the least significant part of the difference current sample, which had previously been stored in a temporary storage register, is returned to the accumulator. The contents of the extended accumulator and the accumulator, 128 times the absolute value of the last difference current sample, is then divided by SUMSAMP. The result is compared with a percentage threshold. Should the threshold be exceeded, the trial is evidence of a faulty stator and the counter, COUNT, is incremented. Should the result not exceed the threshold, the counter is decremented. After COUNT has been either incremented or decremented, it is compared with a positive and a negative threshold value. If the value of this counter is between the two threshold values, the issue is undecided and the sequence returns for another verification pass. Should COUNT be less than the negative threshold, it is concluded that the allocation

and verification routines were triggered by some transient condition. The sum current storage is initialized and the monitor is reinstated. If the positive threshold is exceeded, by COUNT, the system is indicated to be experiencing a fault and an appropriate trip command is issued. Inclusion of the counter provides evidence averaging and reduces the possibility of an incorrect conclusion from the verification sequence. The information in the computer indicating what transpired is printed. For the purposes of testing the program even in the case of transients the information contained in the appropriate memory locations was returned. The actions ensuing from a fault decision are presented in the flow chart of Fig. 5.6.

With the inclusion of the calculation threshold feature, a possibility for error was introduced. In-zone faults are conceivable where the contributions to the fault current from the generator and the connected system are in phase and approximately equal in magnitude. For these rare occurences, the sum current would be small while the difference current would be very large. This condition, if present, could prevent the modified sum current from ever exceeding the calculation threshold and thereby hang up the verification sequence. A second counter, COUNT B, is therefore incremented and checked if the absolute value of the difference current exceeds a back up threshold. Should the ensuing check of the counter reveal that it has exceeded an upper limit, the verification sequence concludes that a valid fault condition exists.

6. TESTING THE DIGITAL PROTECTION SCHEME

The concepts and designs, as presented in the previous two chapters, were implimented in two versions of the digital percentage differential protection scheme. A single phase version, constructed primarily as a developmental stage of the ensuing three phase version, was used to evaluate the viability of the concepts. Tests using both D.C. and A.C. input signals are described. The reaction of the subsequent three phase version to similar inputs is also presented. In addition, this version was tested with simulated generator faults. The reaction of the proposed percentage differential protection scheme is reconstructed for several simulations, to evaluate its performance during system faults.

6.1 Single Phase Version

A single phase version of the digital differential relay, based on the concepts discussed in Chapters 4 and 5, was prepared. Since single phase inputs were to be handled, phase allocation segment was not included and the monitor and verification segments were simplified. The analog computer was used to generate the sum and difference currents. This version was tested with D.C. and then with A.C. inputs to gain some experience in this technology and to examine the incorporated concepts and logic.

6.1 a) D.C. tests

Variable D.C. voltages were applied to the A/D convertor for input to the digital computer. The input voltage representing the difference current was varied from 10 to 150 millivolts. The information received by the digital computer from the A/D convertor was found to be within ±5 millivolts of the analog input. The monitor threshold was also checked using the same inputs and found to be functioning satisfactorily. This software variable was set at 10 millivolts for the remaining single phase tests.

For fixed values of difference current, the sum current inputs were gradually increased and the minimum restraints required to prevent operation of the protective device were determined. This study was conducted for 0.8, 1.6, 2.3, 3.1, 3.9 and 4.7 percent relay settings. The observed relay characteristics are shown in Fig. 6.1. The calculation threshold was set at 0.625 volts while the constant P, defined in paragraph 4.4 c), and the inter-sampling time were 16, and 70 microseconds respectively. The evidence averaging counter, which stored the results of calculations until a sufficient number had been shown to indicate a definite bias, had thresholds set such, that a count of minus five or less indicated a valid non-fault transient condition, while a count of six indicated a verified fault condition. The difference currents were step functions while the modified sum currents were similar to the output shown in Figure 4.3 with a time constant of 2.16 millisecs. This transient mismatch caused the increased sensitivity of the characteristics especially at increased values of the sum current. The reason that restraining inputs of amplitudes near the calculation threshold give sensitivities approaching the ideal, is that for such cases the transient component of the modified sum current is severly attenuated before the calculation threshold was exceeded. The nonlinearity of the characteristic is caused by the discrete steps in which the parameters are converted to digital form.

These results indicated that the scheme was workable as shown by the nearly linear, if not properly oriented, characteristics. Further, the analysis of these results indicated that the situation could be improved by adjusting the software variables, like P, for example.

6.1 b) A.C. tests

The system used for D.C. tests described above, was now subjected to

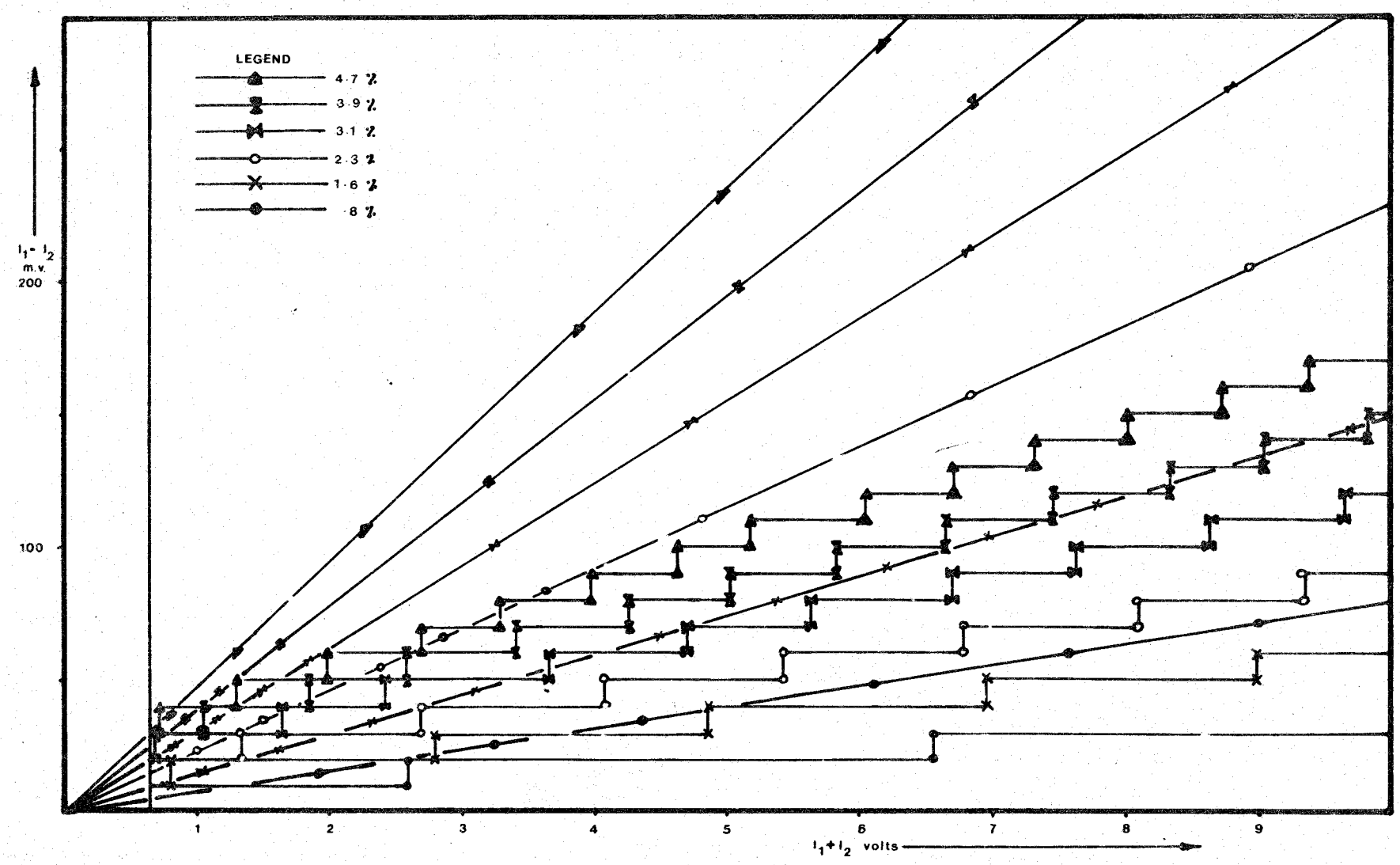

Fig. 6.1 Ideal and measured relay characteristics for various sensitivity settings.

A.C. inputs. A fault simulator was prepared using the TR-48 analog computer to provide the required A.C. inputs. A single phase generator winding with its associated load and transmission line was modeled as in Fig. 6.2. No attempt was made to represent an active load or to include mutual effects from other stator phases. The model is very simple and the change of reactance, with the duration of a fault, is neglected. The model, as constructed on the analog computer, is depicted in Fig. 6.3. Its most prominent feature is that the incidence of the fault is controlled by using the sweep circuits of an oscilloscope. The delayed trigger permitted the relative amplitude of the transient to be fixed and enabled easy viewing of the generated waveforms. The main components of the fault simulator are:

i) a triggered monostable multivibrator,

ii) a sinusoidal excitation source,

iii) an oscilloscope with a variable delay trigger output,

iv) an analog computer.

The gating, accomplished by the multiplier, is governed by the multivibrator. During the time the multivibrator is in the quiescent state, the stator is represented in its non-faulted condition. With the excitation of the one shot, provided from the delayed trigger output of the oscilloscope, the changing conditions at the output of the multiplier indicated the onset of a fault. The multivibrator output had to be designed to be at zero volts when it was in the excited state. A wave shaping limiter provides this function. The multivibrator and the limiter were built from discretes and their schematic diagrams are presented in Fig. 6.4. These two circuits were powered from the reference supplies provided in the TR-48.

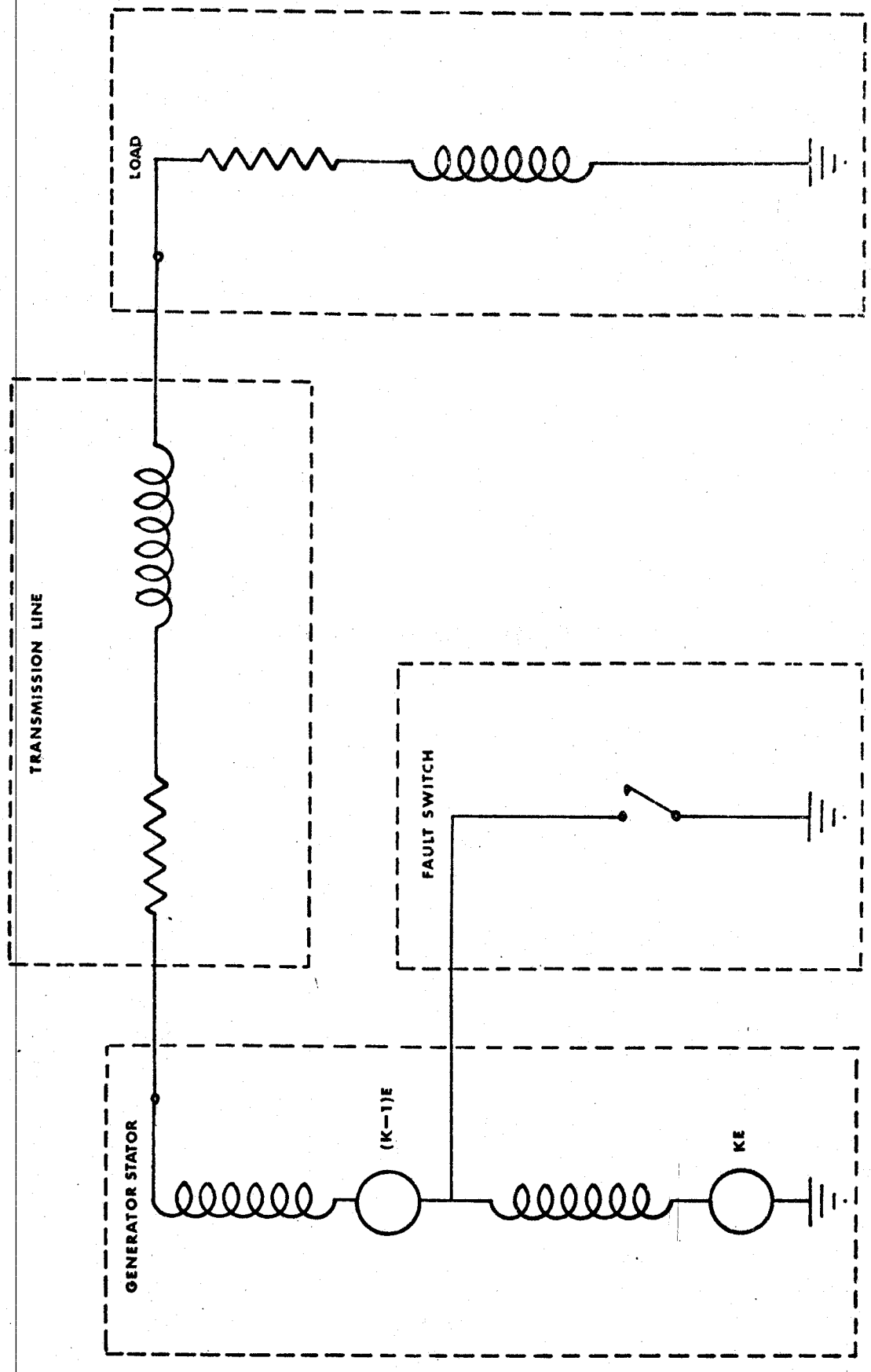

Fig. 6.2 The representation of a single phase stator and its connected system as used by the analog fault simulator.

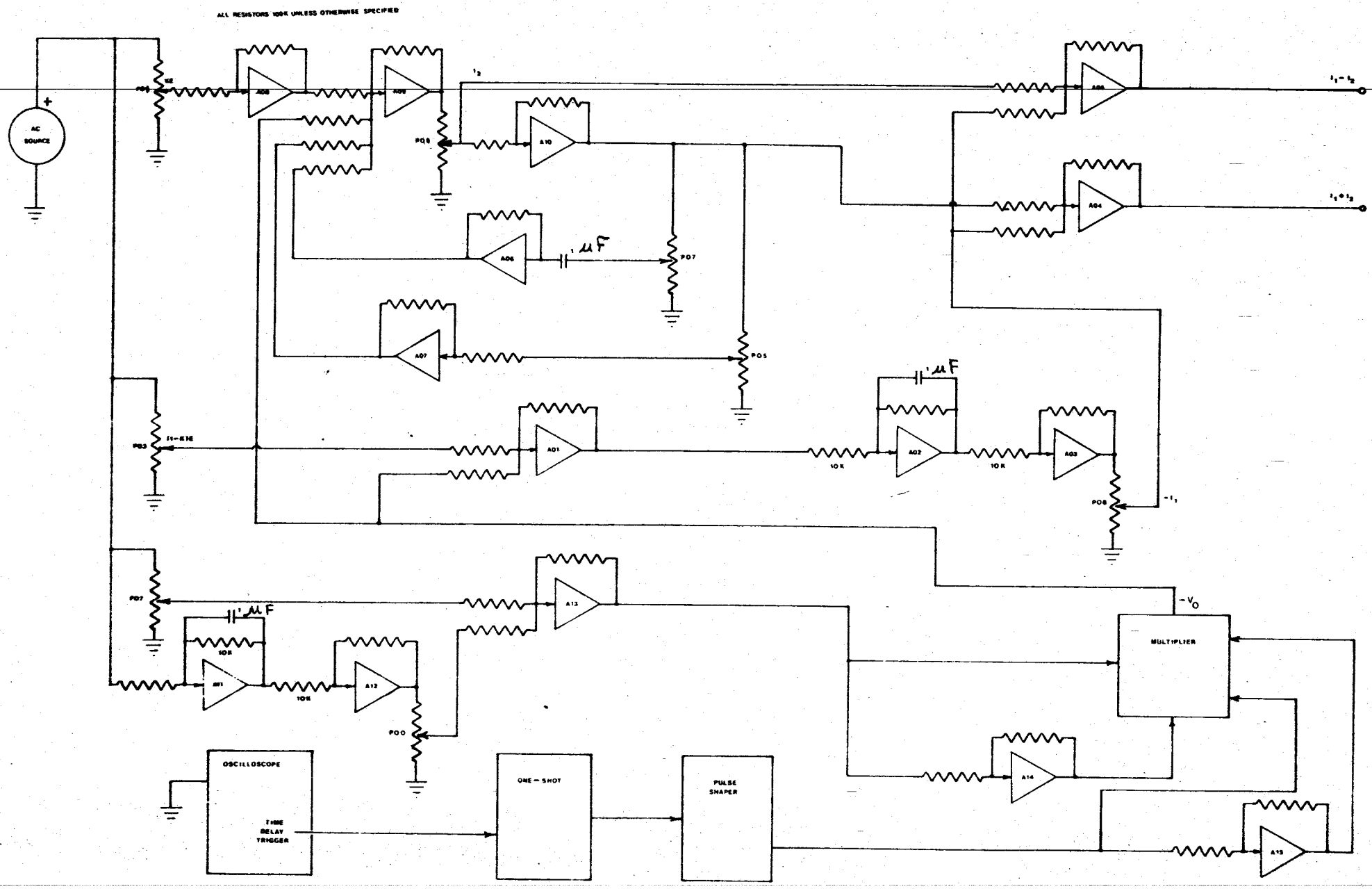

Fig. 6.3 Analog fault simulator.

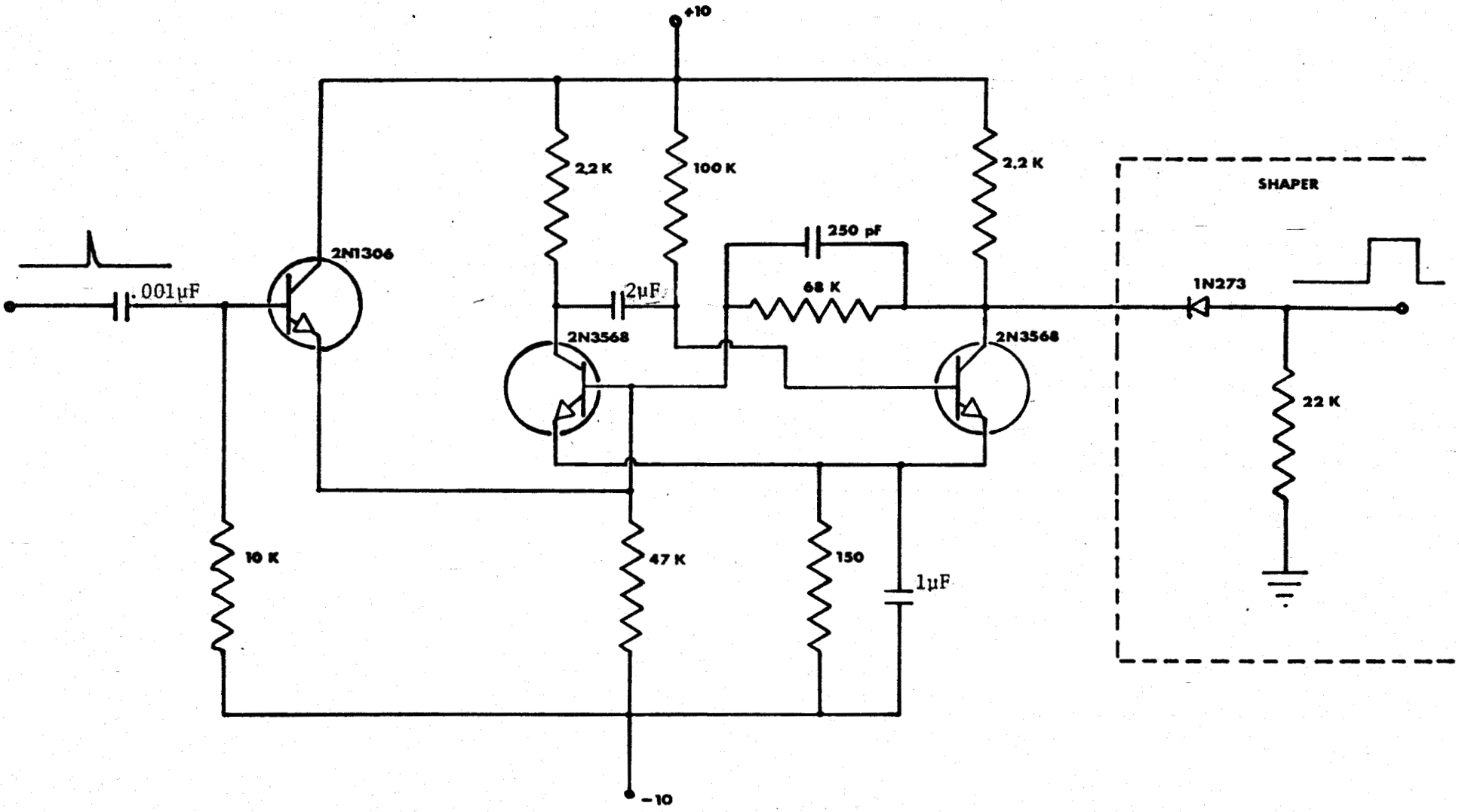

Fig. 6.4 Synchronized fault gating function multivibrator.

The generator stator parameters, which were represented and switched by the TR-48, were modeled using an algorithm based on Kirchhoff's laws. The difference between the normal and faulted condition of the stator is controlled by a coupling voltage, V_o, the output from the multiplier shown in Figure 6.3. The zero impedance fault is simulated by multiplying V_o - with the gating function provided by the multivibrator. During normal operation the phase and amplitude of V_o is adjusted so that the difference current is zero. This arrangement generated suitable functions to determine the validity of the protection principles. Two sample fault conditions, generated in terms of the difference current, are presented in Fig. 6.5.

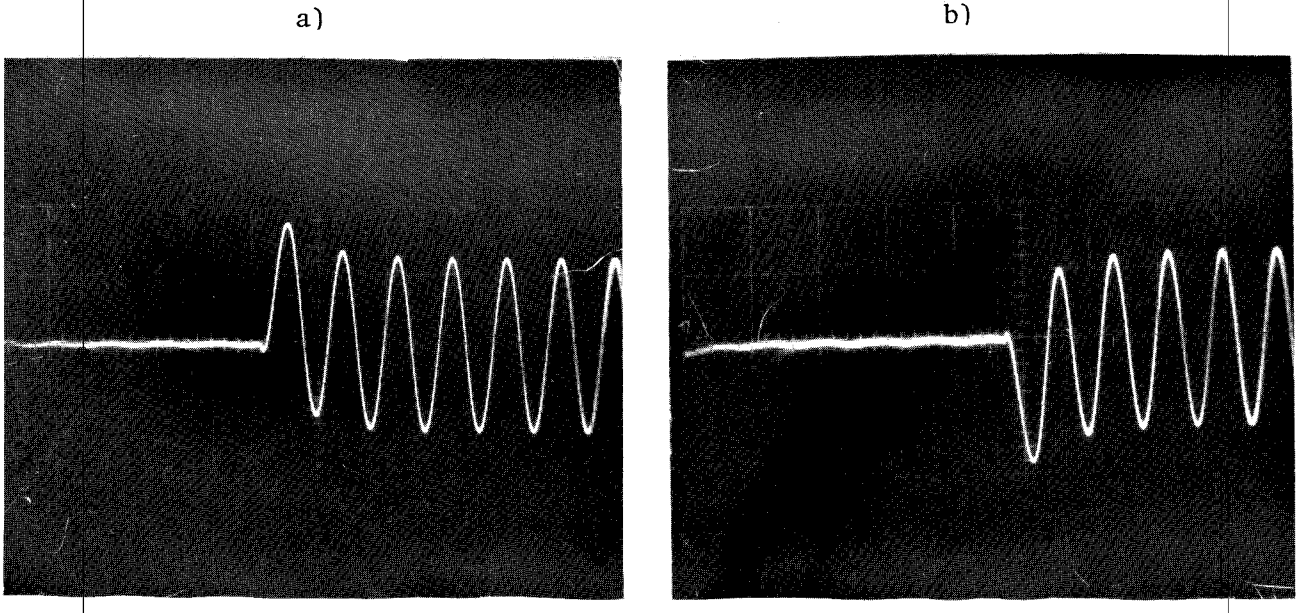

Fig. 6.5 Difference current generated for fault incidence during (a) the negative half cycle and (b) the positive half cycle of the prefault current.

While the analog computer model was sufficient to simulate short circuit faults, it could not adequately simulate marginal conditions. These conditions were, therefore, represented by detuning the coupling

voltage, V_o, and removing the delayed trigger supplied by the oscilloscope. This technique did not simulate the transients of marginal conditions at their inception. Marginal faults for different values of sum currents were simulated for different relay settings. The observed characteristic for the 4.7 percent setting is shown in Fig. 6.6. The characteristics for 3.9, 3.1, 2.3, 1.6 and 0.8 percent relay setting are similar including the "ambiguity" for marginal faults. The protective system parameters described in paragraph 6.1 a) were left unchanged.

The A.C. tests did not demonstrate the sharp delineation between faulted and non-faulted decisions as was desired. This was due to the method chosen to simulate the marginal conditions for analysis by the computer. Though there was some uncertainty of operation for marginal faults, the more serious faults and the healthy conditions were correctly discriminated. Any ambiguities for the marginal faults were eventually removed due to subsequent re-evaluations of the situation by the protection scheme on automatic reactivation of the monitor for non-fault decisions.

6.2 Three Phase Version

A three phase version of the digital differential relay was then prepared based on the concepts discussed in this thesis. This version was tested with D.C. and then with A.C. inputs before applying it to a physical machine. Again, the analog computer was used to generate the required sum and difference currents. All the software parameter settings were adopted from those of the single phase version without change.

6.2 a) D.C. tests

Input data for the D.C. tests was generated and examined in a manner similar to that used for the single phase version. In addition to locating software errors, these tests were conducted to check for bias in

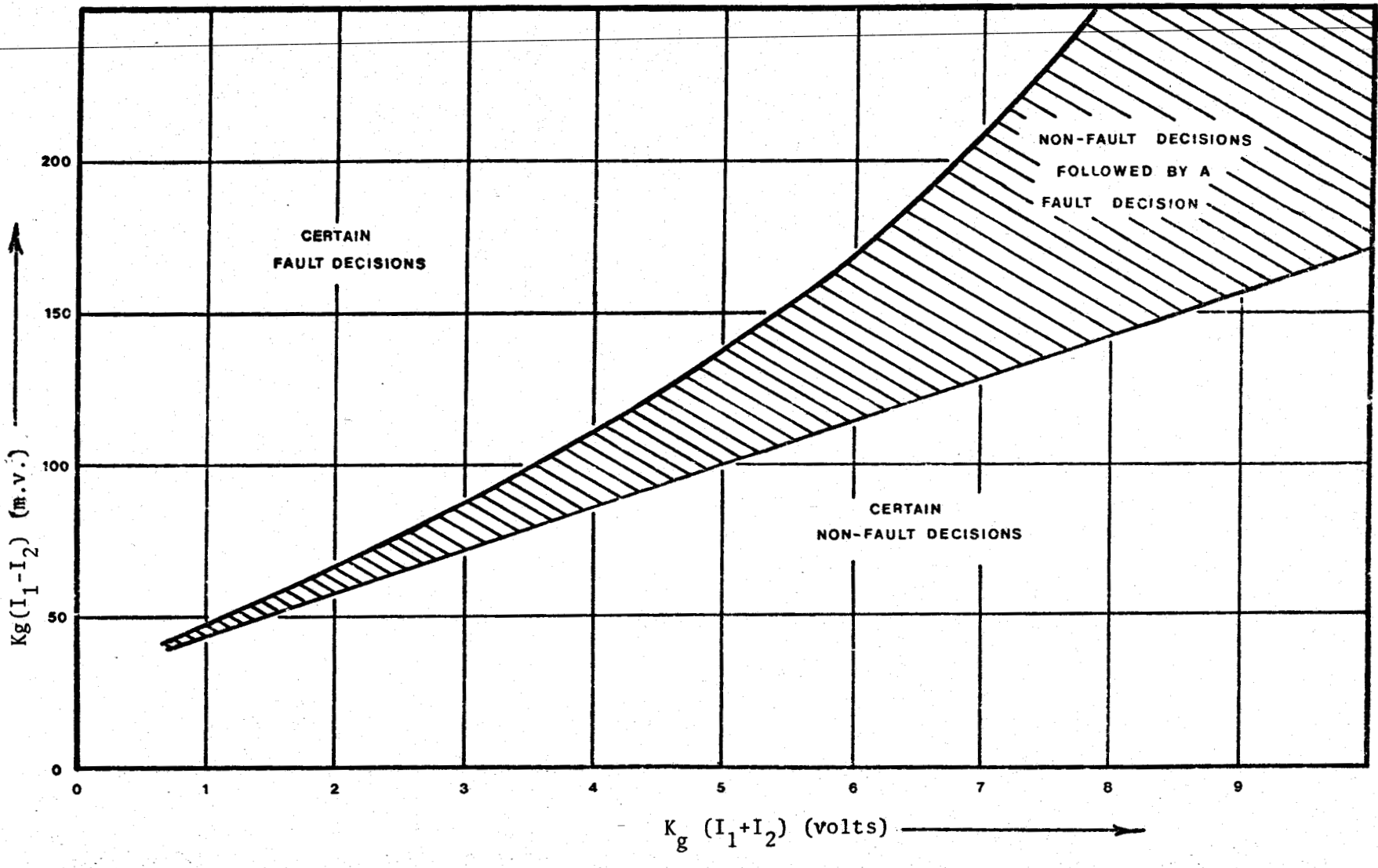

Fig. 6.6 Characteristic response of the single phase version to A.C. excitation at 4.7% sensitivity setting.

the phase allocation sequence. Nominal sum currents were applied to each of the three verification sequences but controlled difference currents,greater than the ten millivolt monitor threshold,were provided for each phase. The smallest difference current was increased until its originating phase was selected as the one most seriously involved. Then, while the magnitudes of the difference currents were maintained, they were reapplied with their phase sequence rotated. In all six such procedures were attempted, three with clockwise rotation of the phases and three with counter clockwise rotation. In all cases, the phase allocation segment selected the appropriate phase for fault verification. The software was therefore demonstrated to be unbiased.

The three phase version of the program was also tested to determine if the inclusion of the phase allocation routine affected the operating characteristics derived earlier. These tests were also conducted using the method described in paragraph 6.1 a) and indicated no change in the characteristics of the protective system.

6.2 b) A.C. tests - analog model

Two methods were used to provide fault data for testing the three phase version. One of these utilized the TR-48 analog computer while the other used a representative machine to generate the required input currents. The single phase A.C. fault simulator described in paragraph 6.1 b) was again employed in the first series of three phase A.C. tests. The two sum currents of the healthy phases were maintained at their prefault levels while the difference current signals of these phases were fixed at zero potential. Five zero impedance ground faults involving 20%, 40%, 50%, 60% and 80% of the winding were simulated. These faults were introduced on different phases by rotating the sequence of the input signals. The computer

relay sensitivity setting was again varied from 0.8 to 4.7 percent as in the previous tests. Other software parameters remained unchanged. All the simulated conditions were correctly identified and decided. Eighteen marginal faults were, then, simulated by detuning V_o. The results indicated that the sensitivity change, due to the inclusion of the phase allocation sequence in the three phase version, was insignificant.

6.3 System Tests - Selection of Equipment

Until digital percentage differential protection is actually implemented in the field, laboratory tests, which can only approximate the true operating conditions, must be employed to evaluate the relay performance. The tests, described in this and the following section, were devised to represent the actual circumstances as closely as was reasonably possible. The considerations involved in selecting the test equipment and its configuration are discussed in this section. Some factors affecting the accuracy of the test system are also examined.

6.3 a) The generator

The TR-48 analog computer is not large enough to accurately represent the characteristic behaviour of alternators during stator faults. Relocation of the hybrid computer facility to a typical generation plant seemed too ambitious an undertaking. Telemetry of the required current signals from a generating station also seemed very complex. In addition, an alternator operating in a power system could not be used expressly to simulate internal faults. As a compromise solution, a small machine was selected to approximate the behaviour of larger units. The particulars of the alternator chosen and its driving motor are given in Appendix III.

The selected machines are located in the Electrical Engineering Undergraduate Laboratory where suitable D.C. power is available for the motor generator unit. The 5kVA alternator is provided with split stator phase windings which may be connected either in series or in parallel. For the system tests, the windings were connected in series as shown in Fig. 6.7. When the generator is operated in this configuration, its rated full load current is 13 amps. With the winding terminals all brought out to a front panel, simulation of internal faults was facilitated with minimum risk to personnel and the equipment.

6.3 b) The current transformers

Six current transformers (C.T.'s) were required to convert the line and neutral end currents from each generator stator phase to a suitable voltage signal. The Saskatchewan Power Corporation made seven suitable C.T.'s available. Three of these were of the 9JS 1HAR3 type, manufactured by General Electric, and four were of the H15 model, manufactured by Packard Electric. Both types were operated at the 100/5 transformation ratio. Linearity and excitation specifications, which are important in applications where the C.T.'s are used in a differential mode, was lacking. To gain some insight into their performance, the excitation characteristics, shown in Fig. 6.8, were plotted from lab tests, for both the General Electric and Packard Electric transformers.

Reasonably light loads (5 ohms) were provided in the secondary of each C.T. to ensure linear operation for the largest anticipated alternator currents. With this loading, one per unit current was now represented by 3.25 rms volts across the load resistor. For symmetry, two General Electric C.T.'s were installed in one alternator phase while the remaining four Packard Electric C.T.'s were installed in the other phases as is also shown

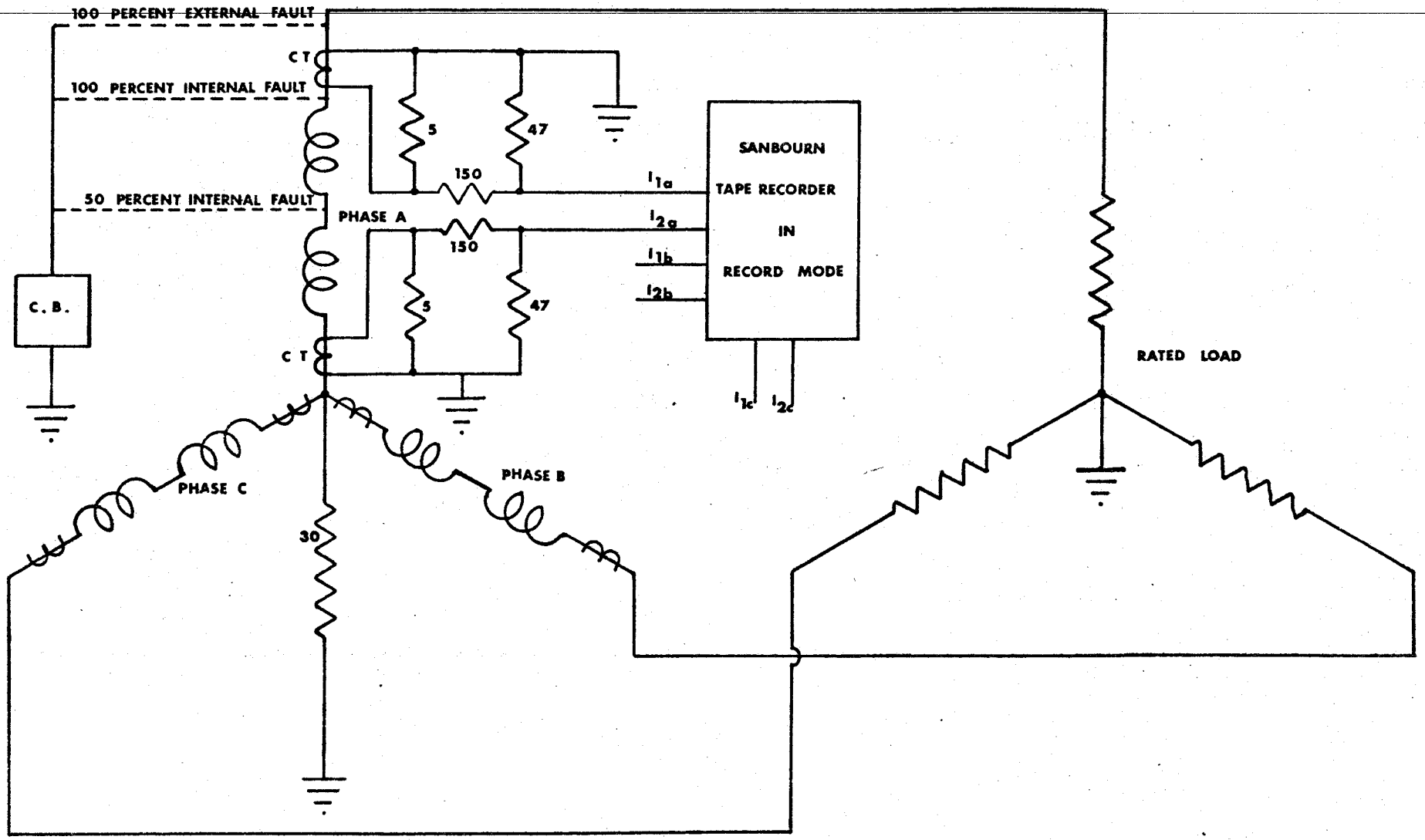

Fig. 6.7 Test equipment configuration for fault simulations.

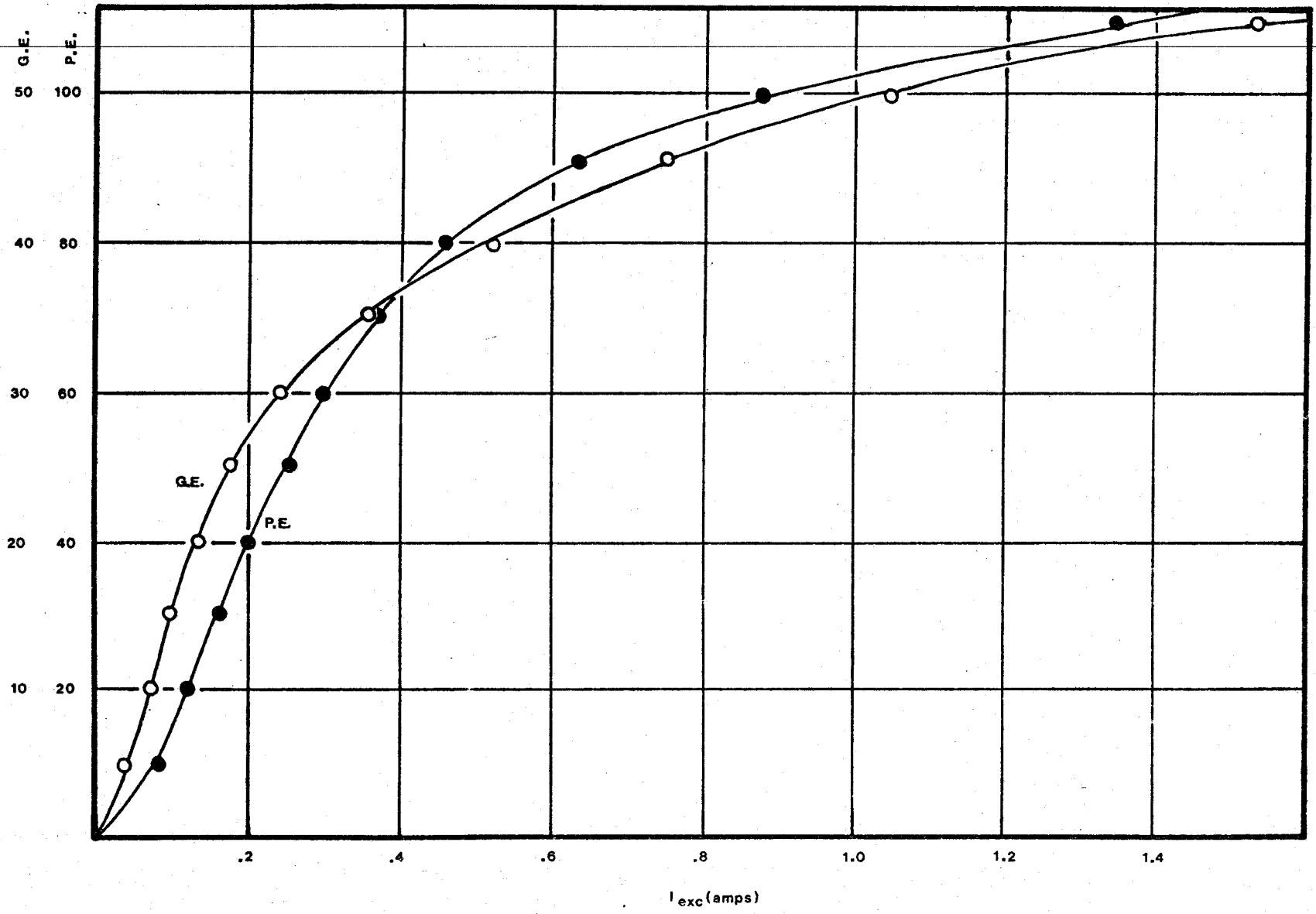

Fig. 6.8 Excitation characteristics for both the Packard Electric, P.E., and the General Electric, G.E., C.T.'s.

in Fig. 6.7.

6.3 c) The tape recorder

The selected rotating equipment as indicated in paragraph 6.3 a), was still located remote from the Sigma 2/TR-48 hybrid computer facility. Relocating either of the two test equipments could be avoided if suitable means to transmit the six signals from the alternator to the TR-48 analog computer could be devised. A Sanborn, model 3907A, magnetic tape recorder is available with the Cardio-Pulmonary Laboratory at the University Hospital and could be used for this work. This analog recorder consists of a multi-speed tape transport assembly with optional, interchangable, record/playback electronics for each speed. Eight channels (seven signal and one voice) can be simultaneously recorded or played back. The seven signal channels have a bandpass from zero to ten kHz at the 60 inch/sec tape speed. As listed in the instruction manual, the input and output impedances are 600 ohms each and the signal to noise ratio is specified at 44 db. Record/playback electronics was not available for other suitable tape speeds.

The recorder's dynamic range is specified from -2.5 to +2.5 volts with one percent linearity in this region. Consequently, the signal output from the C.T.'s had to be reduced in amplitude. A voltage divider, consisting of a 150 ohm and a 47 ohm resistor, was employed. This reduced the representation of one per unit generator current from 4.6 volts peak across the C.T. load resistor to approximately one volt peak at the input of the tape recorder. This maintained the line and neutral end current signals within the linear operating region of the tape recorder, during the simulated fault conditions, but reduced the signal to noise ratio from 44 db. to 36 db. As stated in paragraph 5.2, the frequency response of the analog pre-processor rolls off at 20 db per decade below 0.318 Hz and above 1.59 kHz.

Assuming white noise, this reduction in bandwidth effectively improved the signal to noise ratio of the system by about eight db.

The test equipment configuration, depicted in Fig. 6.7, shows that a 30 ohm resistance is inserted in the neutral ground return of the generator. Dry runs preceding the actual tests indicated that fault currents of eight per unit could be expected during the simulation. Fault currents of such magnitudes are far greater than the three to four per unit maximum fault currents expected from generators employed in power systems. The neutral grounding resistance was, therefore, included to limit the fault currents to less than two per unit. This may appear as a drastic step but the inclusion of this impedance reduces the difference between the faulted and healthy states of the stator and consequently increases the demands on the protective system.

6.4 System Tests-Results

The equipment, described in paragraph 6.3, was used to provide more accurate fault data to test the digital percentage differential protection scheme. The types of faults simulated and the protective system's reaction to this information are presented in this section.

The operating portion of the digital scheme was tested with four types of faults simulated by using the alternator:

i) internal single phase faults involving 50 percent of the stator winding,

ii) internal single phase faults involving 100 percent of the stator winding,

iii) internal two phase faults involving 50 percent of the stator windings,

iv) external single phase faults.

Fourty-five type (i) internal fualts were simulated. In twenty of these, the inception of the fault was controlled by using a synchronous switch[47]

in place of the circuit breaker of Fig. 6.7. Four groups of five faults, each were recorded with incidence delayed approximately 0^{o}, 30^{o}, 60^{o} and 90^{o} from the zero crossing of the terminal voltage waveform. The remaining twenty-five type (i) simulations were recorded without incidence control. Twenty-five each of types (ii), (iii) and (iv) faults were also simulated in this manner. In the two phase fault simulations, the 50 percent points of the stator windings were shorted through a 6.5 ohm current limiting resistor. The line and neutral end currents in the three phases during the faults and in pre and post fault periods were recorded on magnetic tape.

The functional organization of the equipment used in the system tests is presented in Fig. 6.9. After a particular type of fault had been simulated and recorded,the tape recorder was relocated at the hybrid computer facility and the playback procedure began. The tape drive was started in the playback mode. The digital computer software was initiated by the operator after an eight second delay, required to permit the recorder outputs to stabilize. With this action, the monitor segment of the protection program began to execute. It continued to operate until its difference current inputs, derived by the TR-48 analog computer from the information supplied by the magnetic tape recording, dictated that the monitor should do otherwise. At the moment the digital computer indicated that it had arrived at a decision the tape transport was manually stopped. The pertinent information, stored in the appropriate circular storage arrays, was then automatically printed for reference. At the termination of the print out the computer was put into a wait condition either by an operator, or, in the event of a fault conclusion, by the software. The tape transport mechanism was then restarted by the operator. Reactivation of the software was delayed until the fault simulation data from the concluded case had

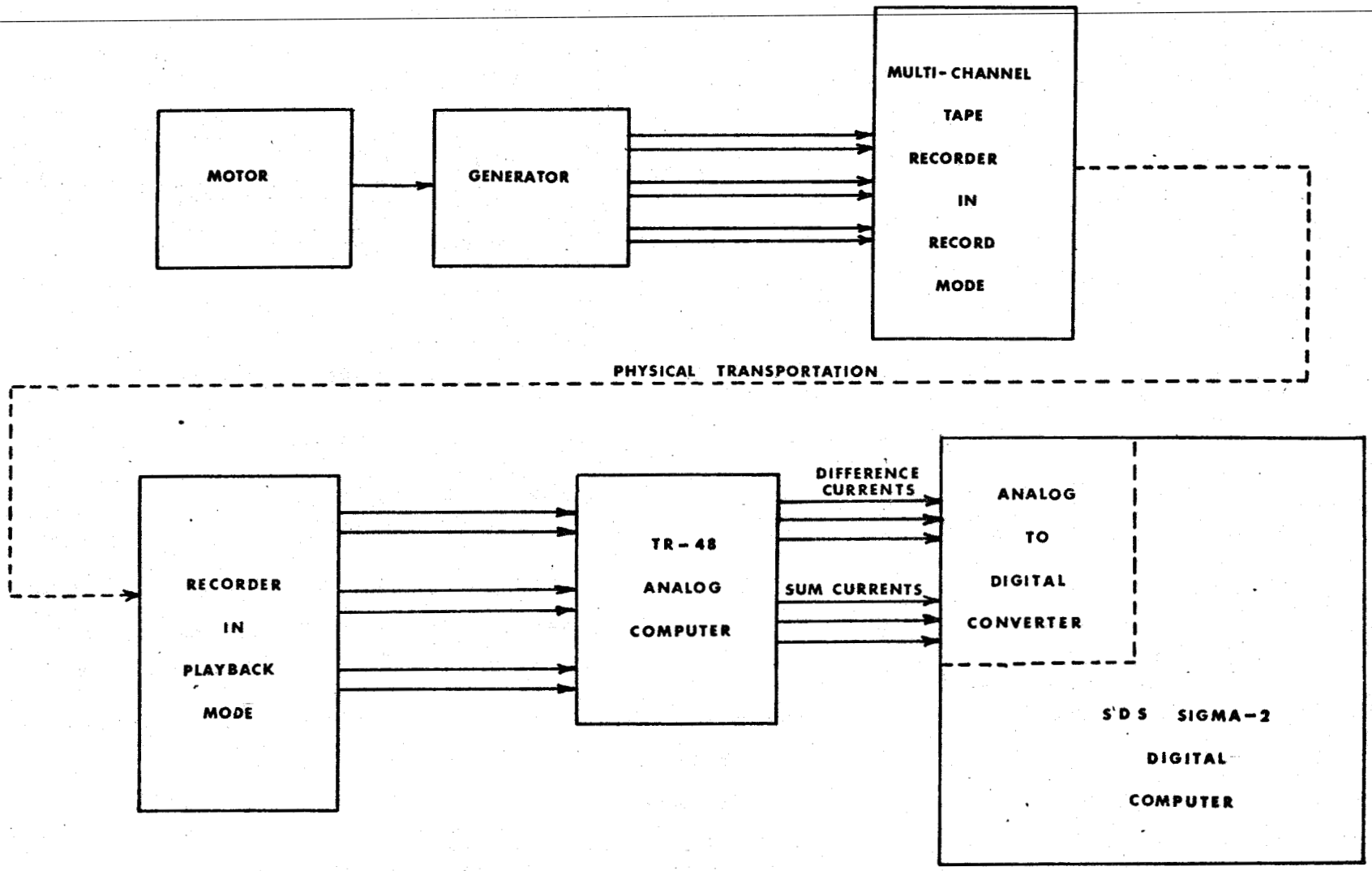

Fig. 6.9 Test equipment configuration for the machine tests of the digital protective system.

cleared the tape reading heads. The fault monitor then awaited the next possible fault indication.

For these tests, most software variables remained set as they were previously. The exceptions were P, the parameter which governs the modified sum current transient's time constant, and the monitor threshold. The monitor threshold was set at 50 millivolts while P was set at two, which is equivalent to a 202 microsecond time constant. The analog computer gains were adjusted so that one per unit generator current, which was represented by 1.0 volt peak output from the tape recorder, was amplified to 2.5 volts peak.

6.4 a) Type (i) faults

The data from each magnetic tape recording was examined by the protection scheme several times. All the type (i) fault simulations were examined with the software relay sensitivity set at 2.3 percent, 3.1 percent and 3.9 percent. In addition, the orientation of the phase, which carried the fault data, was rotated to facilitate testing of all the software with the same simulations. This phase sequence rotation permitted the examination of faults, which were only simulated on one phase of the generator stator, as if they had been duplicated on the other two. In this manner 75 cases, 25 for each sensitivity setting were examined as faults on each stator phase. A total of 225 case studies were therefore derived from this one tape recording.

The scheme's reaction to one of the type (i) faults as reconstructed from the printed data, is represented in figure 6.10. All functions are plotted in the time sequence in which they are sampled or generated. The reconstructed difference current function indicates that the fault probably occurred just after the second sample shown, and

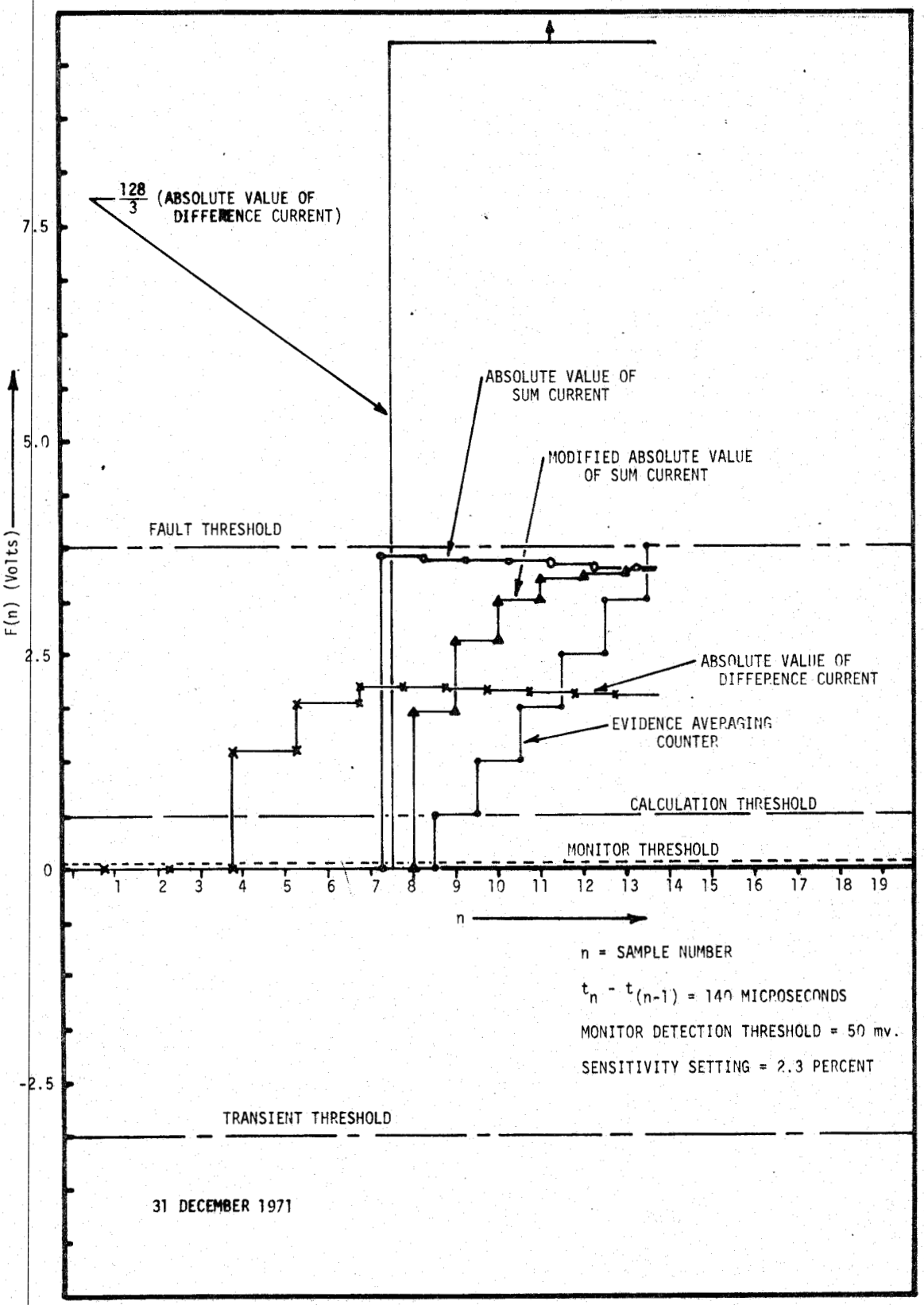

Fig. 6.10 Reconstructed protection system reaction to a type (i) fault without incidence control.

exceeded the monitor threshold in sampling interval 3. With such a large difference current, this sample was the largest of the three compared in the first pass through the phase allocation sequence. The second post fault sample of the difference current was again determined as the largest and the phase allocation sequence then called the proper verification routine. The next sample of difference current was taken as part of the fault verification sequence. During the first pass through this routine, the modified absolute value of sum current was generated as zero because no sum current samples had been read prior to the first calculation. The difference current was multiplied by 128. No comparison between the modified sum current and the difference current was made since the former had not yet exceeded the calculation threshold. On the second and subsequent passes, through the verification sequence, the modified sum current does exceed the calculation threshold and subsequent comparisons, between this function and 128/3 times the absolute value of the difference current, supported a fault decision. Every time a fault decision was indicated, the evidence averaging counter was incremented. On the pass where the counter reaches the fault threshold, printing was initiated. In a power system application a trip command would be issued at this stage. The fault and transient thresholds shown bear no relationship to the voltage scale. A voltage increment of 0.675 volts is chosen for convenience.

In all the 225 cases mentioned above, the phase allocation sequence of the protection scheme correctly selected the faulted phase for verification. The decision making in each of these cases was correctly concluded in less

than three milliseconds. The various sensitivity settings did not affect the decisions or their timing.

Attempts were also made to determine the protection scheme's performance at 1.6 percent sensitivity. Voltage spikes, which at times exceeded one volt in amplitude, were discovered at the tape recorder outputs. While these were correctly diagnosed as transients at the 2.3 percent and higher sensitivity settings, some were verified as faults at the 1.6 percent setting. Degaussing and re-recording the data to remove the spikes failed. Similar conditions were also encountered with a second magnetic tape although the frequency and severity of the spikes, concluded to be caused by abrasions on the tape surface, diminished somewhat. The difficulty encountered in distinguishing between decisions concluded from the spikes and the fault simulations invalidated the test results at the 1.6 percent sensitivity setting.

The twenty type (i) faults, in which the incidence of the fault was controlled, were examined with similar relay settings and phase rotations. The reaction of the protection scheme to one each of the 0^{o}, 30^{o}, 60^{o} and 90^{o} incidence angle faults is shown by Figs. 6.11, 6.12, 6.13 and 6.14. These illustrate the change in the transient response of the fault current with the angles of incidence. The reconstructed data also demonstrates the accuracy to which the sum current is modified to match the transient response of the difference current. It is apparent that for alternators, whose fault current will contain fast transients (characteristic behavior for small machines), some additional modification of the sum current might be advisable. The significant error in these cases is caused by the delay associated with executing the phase allocation sequence. The controlled incidence simulations provided an additional 180 type (i) cases in which

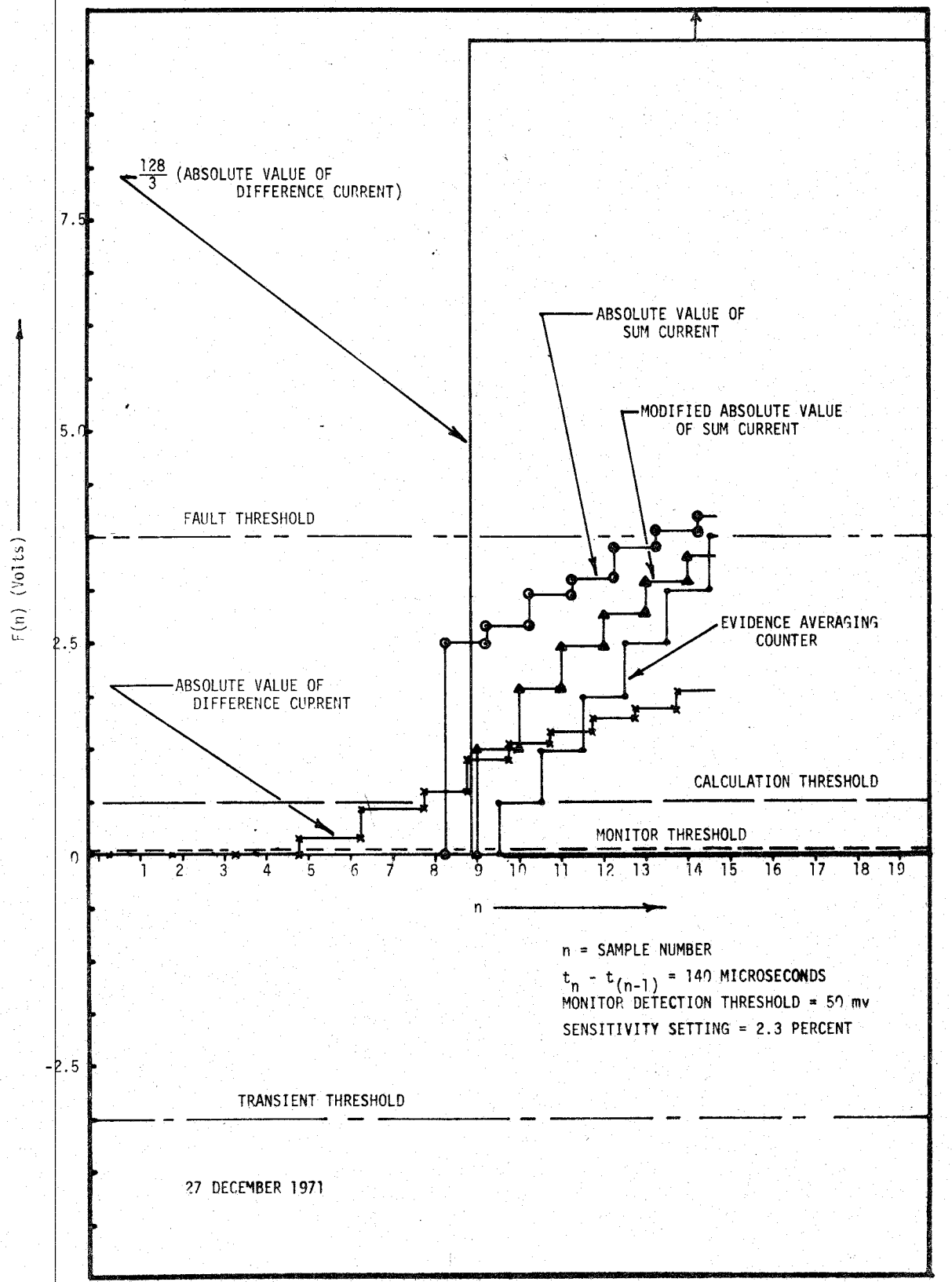

Fig. 6.11 Reconstructed protection system reaction to a type (i) fault with incidence at 0°.

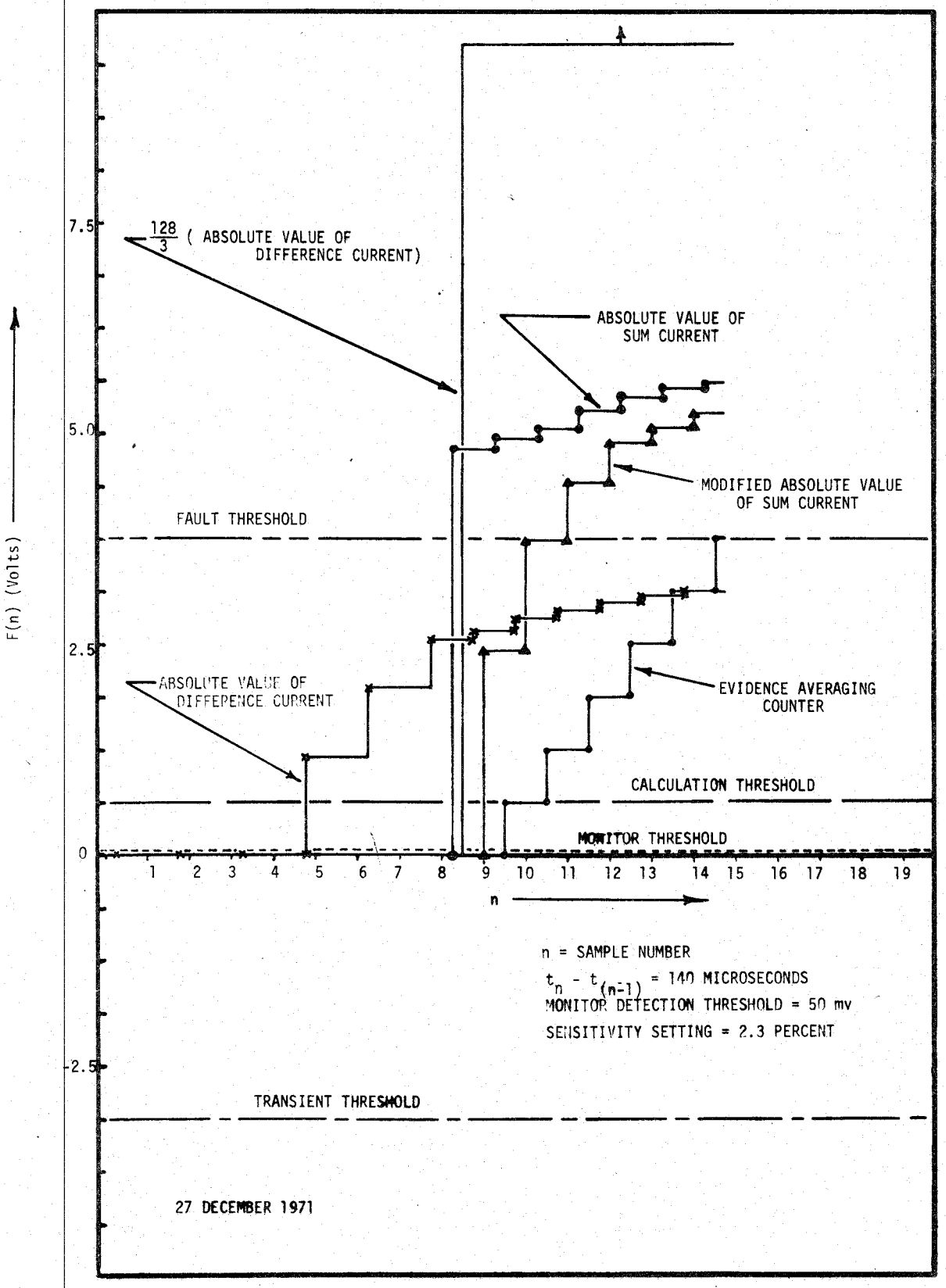

Fig. 6.12 Reconstructed protection system reaction to a type (i) fault with incidence at 30°.

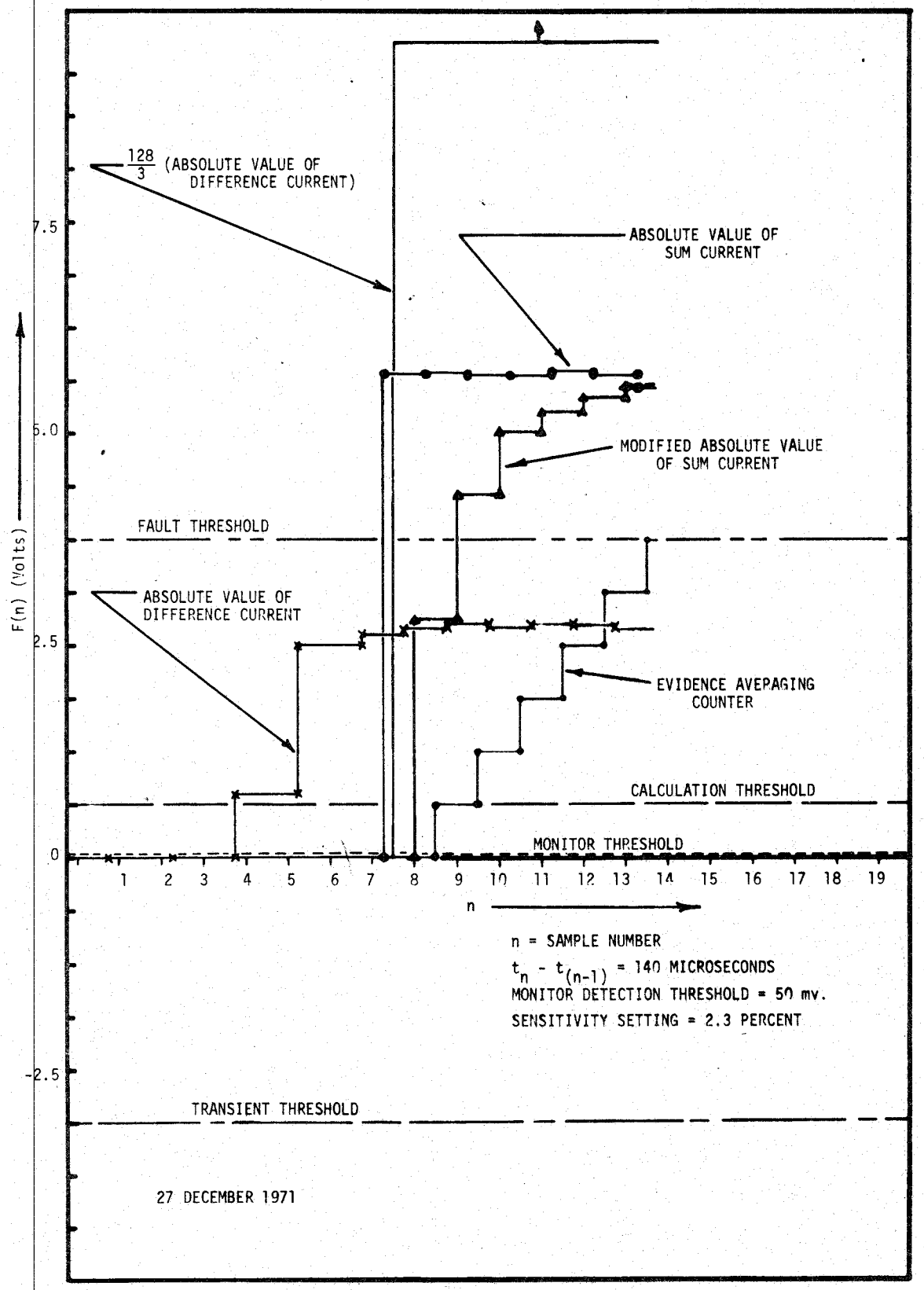

Fig. 6.13 Reconstructed protection system reaction to a type (i) fault with incidence at 60°.

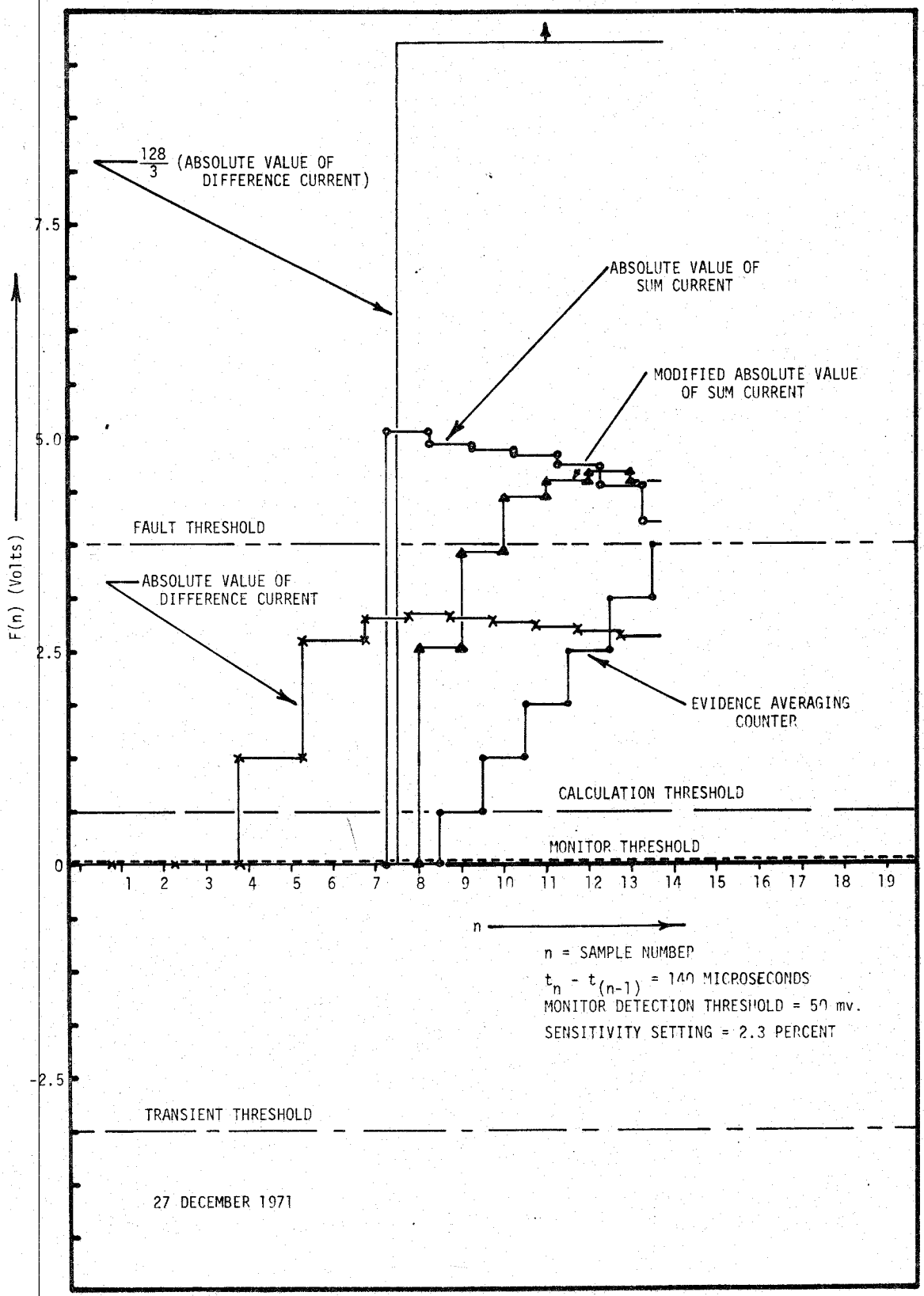

Fig. 6.14 Reconstructed protection system reaction to a type (i) fault with incidence at 90°.

verification was correctly initiated. All fault simulations were verified as faults in less than two milliseconds irrespective of the relay setting and the phase orientation of the particular case.

6.4 b) Type (ii) faults

The relay settings employed for the internal single phase faults at the line end of the stator were 2.3 percent, 3.1 percent and 3.9 percent. Phase rotation of the simulated faults, similar to that used for the previous cases, was again used. The protection scheme responded to these relatively more serious fault simulations as was expected. All faults were correctly verified in less than three milliseconds. Typical responses are reconstructed in Figs. 6.15 and 6.16. The response of Fig. 6.15 shows the increased time (2.3 milliseconds) required to verify a fault when incidence occurs just before a stator current zero crossing. This figure also indicates that the phase displacement between the sum and difference current is reduced if the modified sum current function is used. The reconstructed response, shown in Fig. 6.16, illustrates the relatively shorter time (1.5 milliseconds) required to verify a fault when its incidence occurs near a stator current maximum. Again the close correlation between the transient characteristics of the restraining and operating functions is evident. These simulations provided an additional 216 cases which were verified without error. One case was rendered unsuitable because a noise spike consistently activated the verification sequence just prior to the occurrence of a valid simulated fault. When the computer had completed verification of this spike as a transient, the print cycle was initiated to output the "desired" data as described earlier. Because the printing was executed as a foreground task before reactivation of the monitor, the incidence of the following fault was missed. In a power system application, printing would be

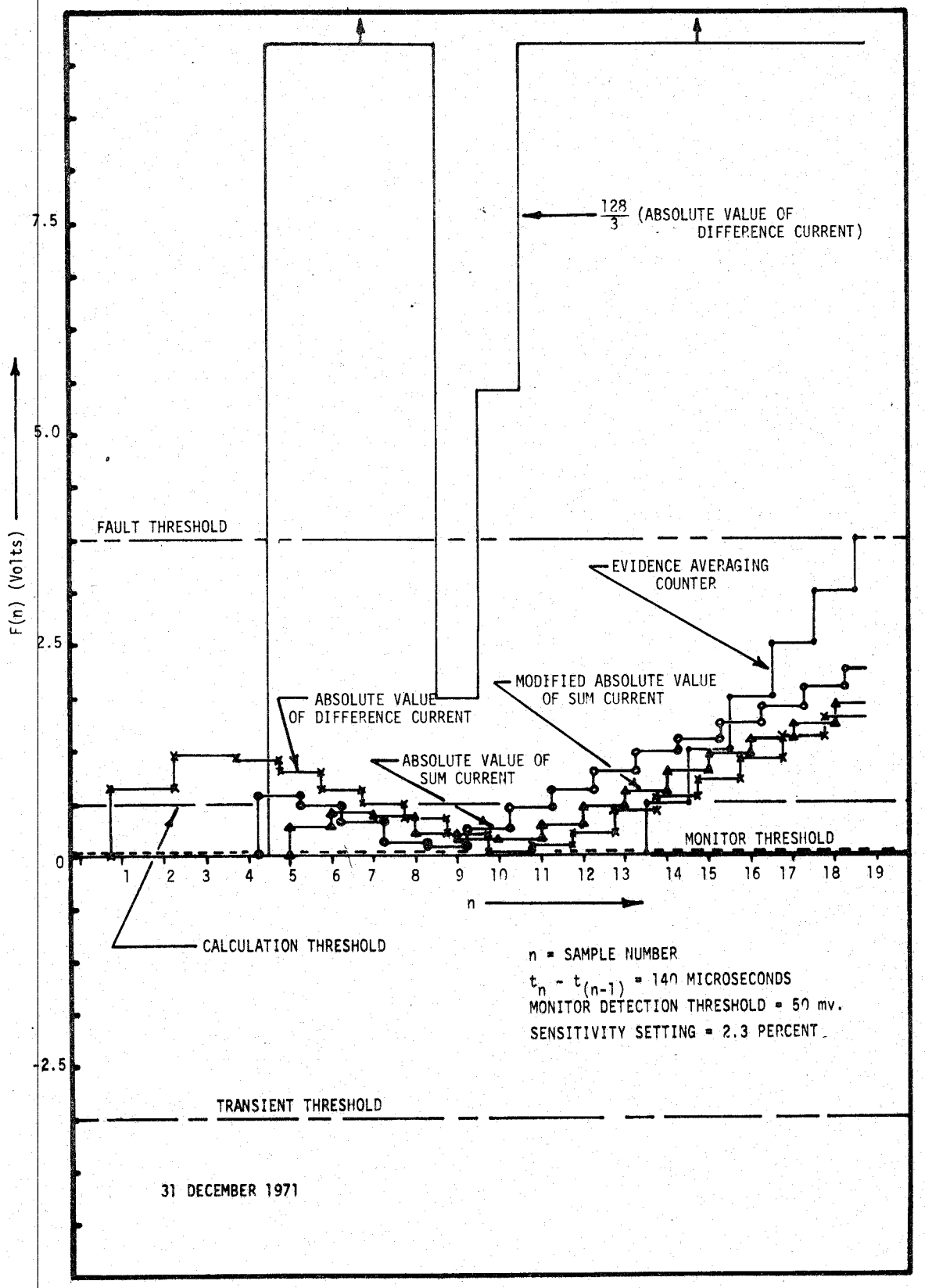

Fig. 6.15 Reconstructed protection system reaction to a type (ii) fault with incidence just prior to current zero crossing.

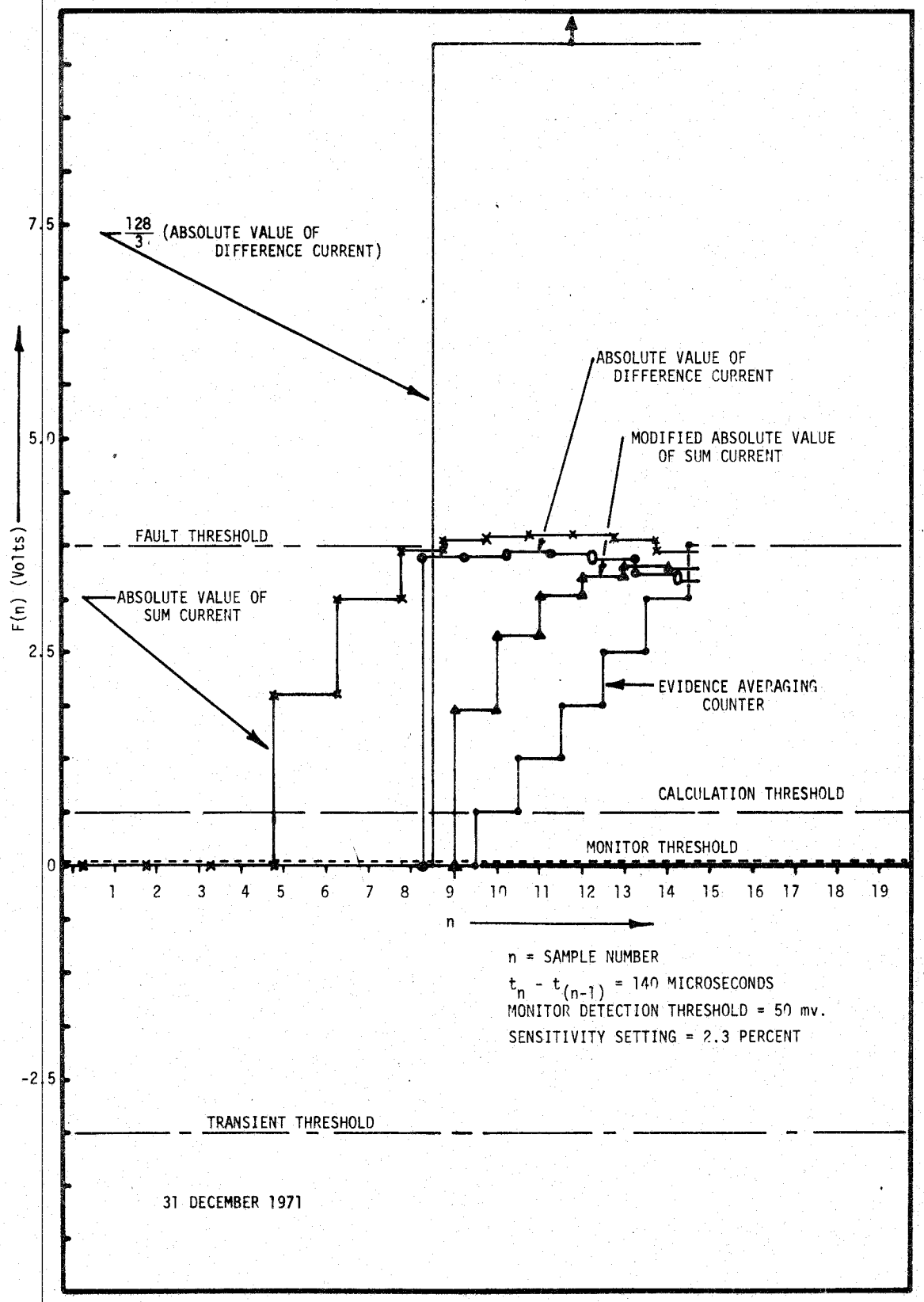

Fig. 6.16 Reconstructed protection system reaction to a type (ii) fault with incidence near current maximum.

relegated to a lower priority and the monitor would be reactivated immediately after the transient's verification. The tape recorder and digital computer could not be restarted in such a way that the transient would be missed. The case data drived from this simulation was, therefore, disqualified.

6.4 c) Type (iii) faults

Two phase internal faults formed the last catagory of simulations where a positive fault verification was the desired response. The previous tests had demonstrated the invariability of the result with relay setting. Therefore, the type (iii) simulations were all examined with 2.3 percent sensitivity. The phase sequence was again rotated to further test the bias of the phase allocation sequence. Seventy-five cases were therefore examined with the type (iii) fault simulations.

Two typical reconstructions of the protection scheme's response are presented in Fig. 6.17 and 6.18. Again in Fig. 6.17, the modification to the current decreased the phase displacement between the restraining and operating functions. For these cases, the time constants are not as accurately matched as for single phase in-zone faults. The increase in the time constant is undoubtedly due to the change in the inductance to resistance ratio provided by the different fault configuration and the reduction in the current limiting resistance.

Some bias was shown in selecting the faulted phase. Consideration of the symmetry of two phase faults indicates that the fault current flowing in each phase should be equal but in opposing directions. No preference should therefore, exist in selecting one of the two phases for fault verification. One phase was selected ninteen times while the other was allocated 56 times. Since the bias rotated with the phase sequence, it

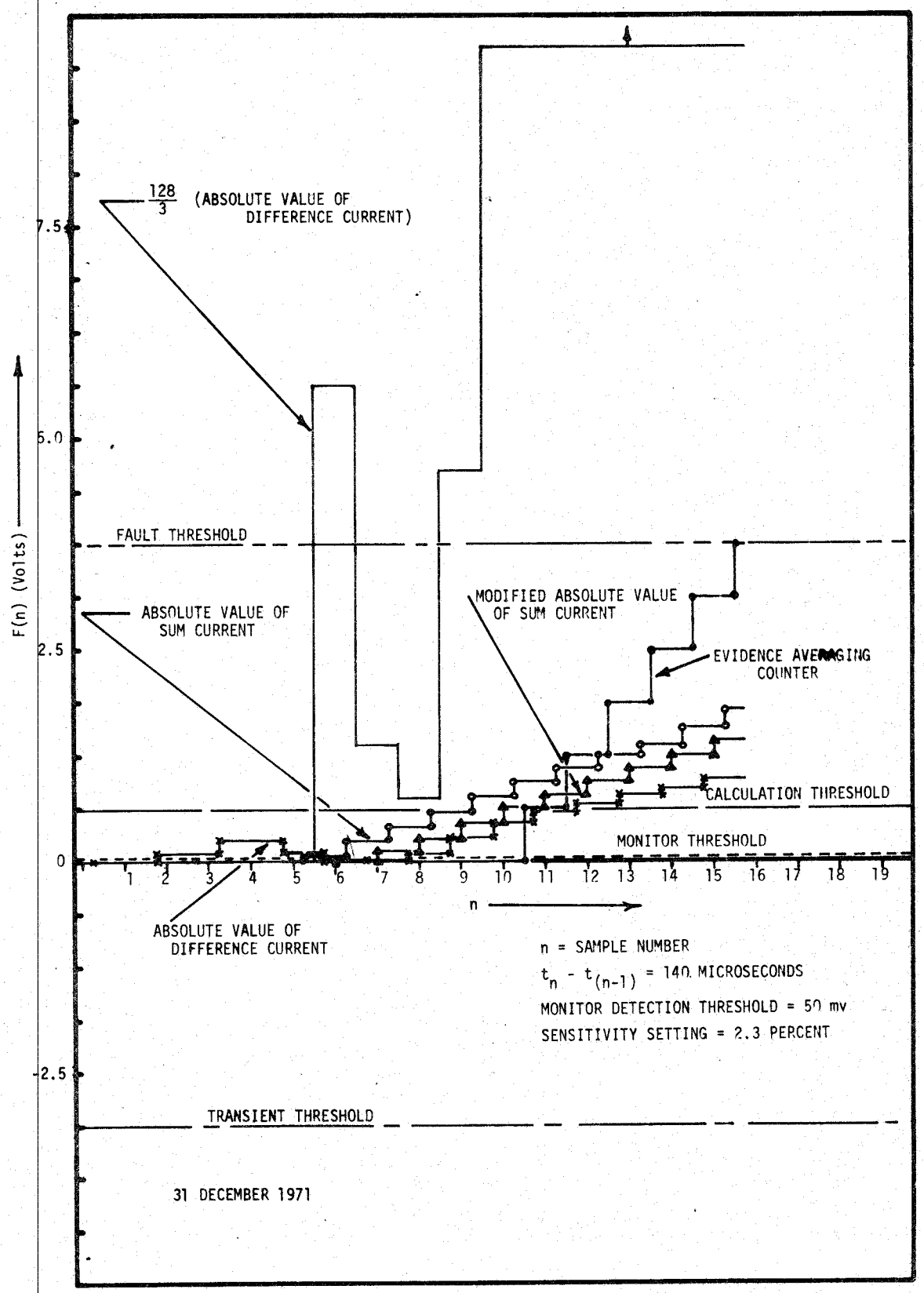

Fig. 6.17 Reconstructed protection system reaction to a type (iii) fault with incidence just prior to current zero crossing.

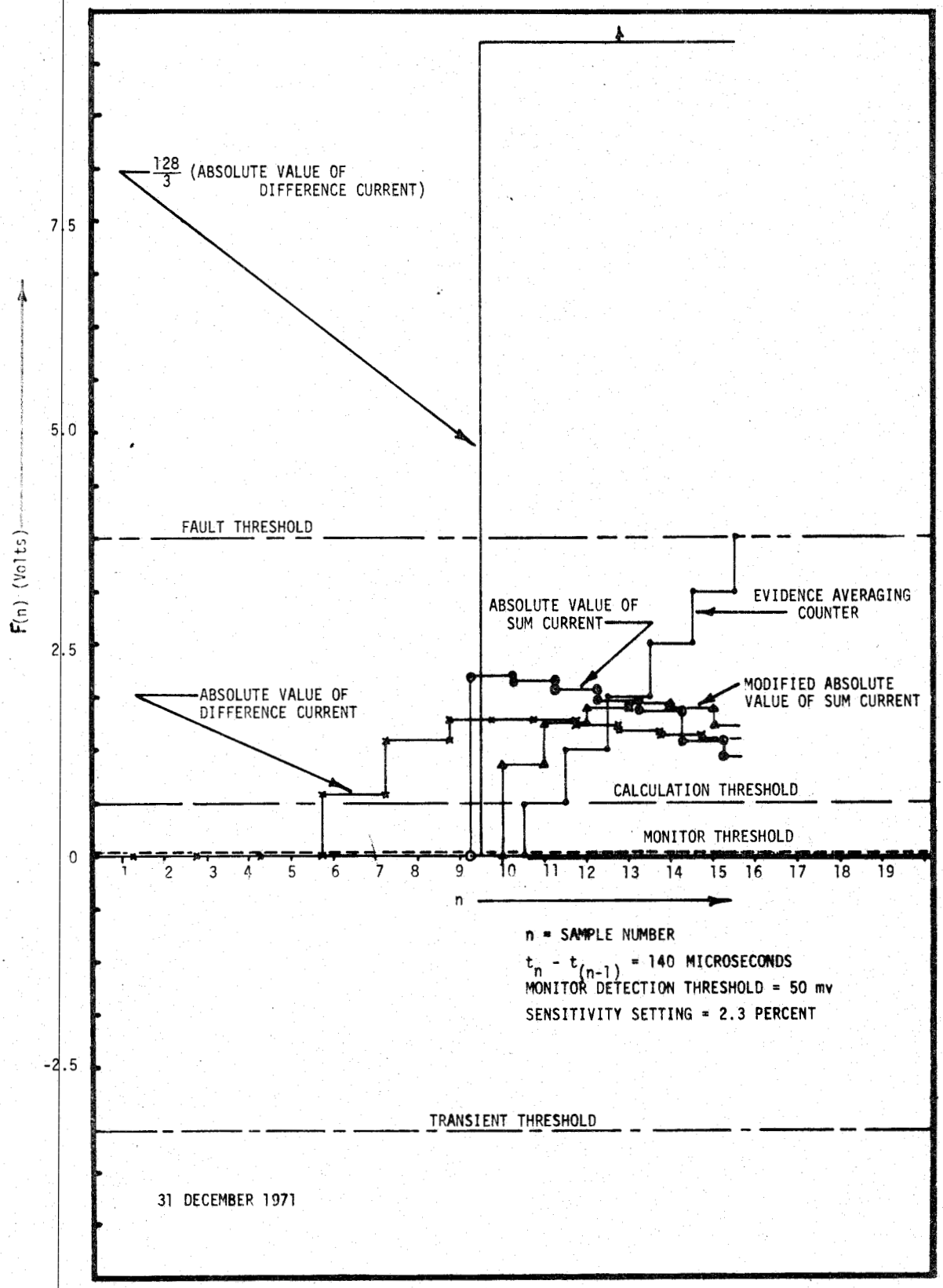

Fig. 6.18 Reconstructed protection system reaction to a type (iii) fault with incidence near current maximum.

is attributed to the unavoidable differences in gain provided for the signals of the three phases. As was previously indicated, 75 fault simulations were examined and all were correctly verified as faults on one or the other of the involved phases.

6.4 d) Type iv) faults

External faults were simulated and examined to test the protection scheme's ability to descriminate between in-zone and out of zone faults. As indicated earlier, one generator terminal was short circuited to ground which is a very severe external single phase fault. The operation of the protective scheme, using the sensitivity settings of 1.6, 2.3, 3.1 and 3.9 percent, was tested. The reconstruction of a typical case is presented in Fig. 6.19. As indicated by the reconstructed response, imperfect cancellation provided some error signal. When the relay sensitivity was set at 2.3 percent, all 25 cases were correctly verified as transients not warranting trip initiation. Predictably, the cases examined with 3.1 percent and 3.9 percent relay settings were also correctly verified. When the sensitivity setting was decreased to 1.6 percent, nine of the 25 cases resulted in an erroneous, faulted stator, conclusion. If better discrimination than that offered by the 2.3% relay setting is desired, equipment with better linearity will have to be selected. In all cases verification was executed on the correct phase. The test provided 91 correct conclusions out of 100 sample cases.

The results of the tests using the fault data provided by the generator definitely prove the fault detection ability of the proposed protection scheme. Of the 796 fault cases examined, an overwhelming 787 were correctly decided. As indicated in Table 6.1, the nine erroneous conclusions resulted when the discrimination limits of the test equipment

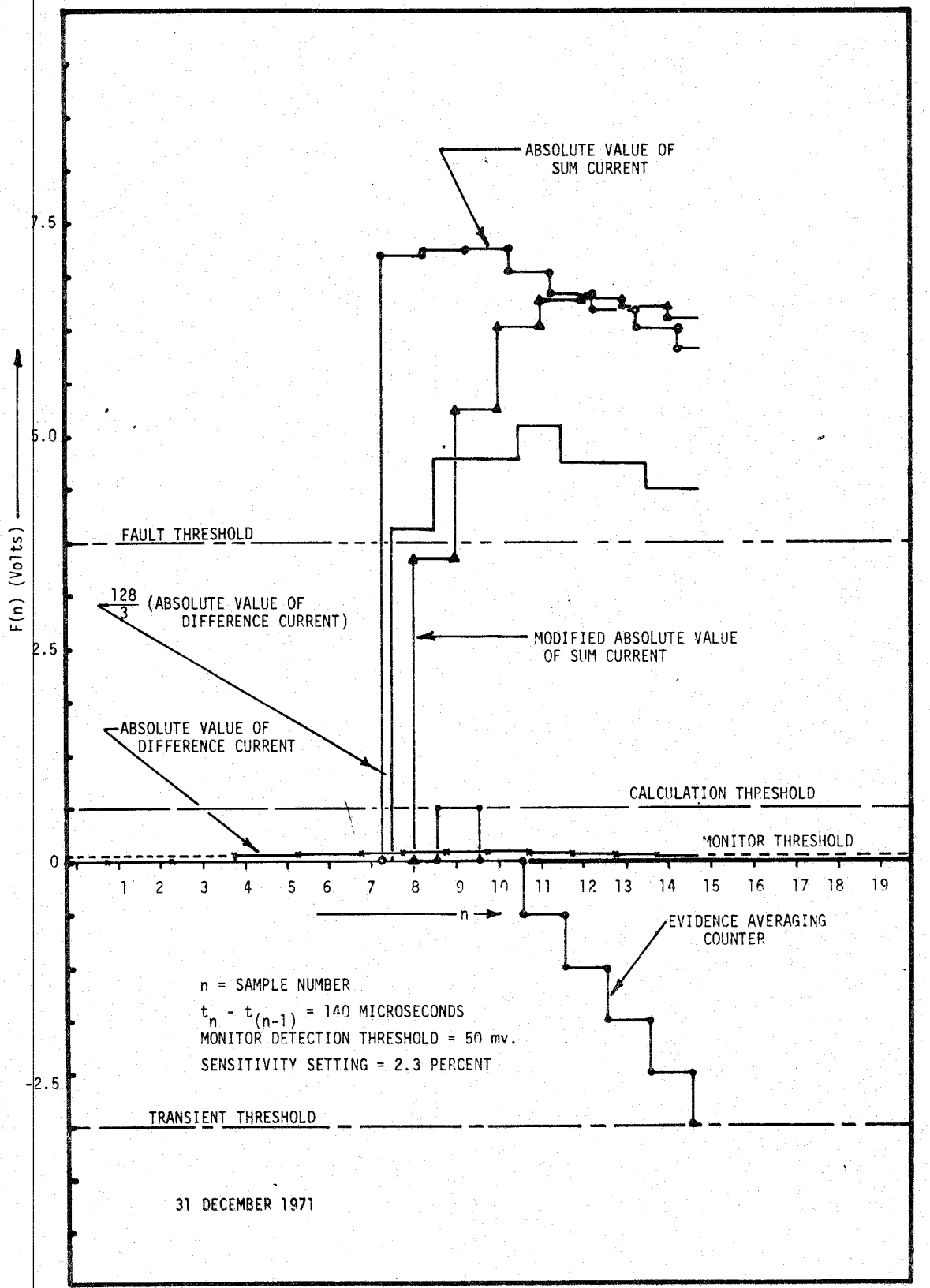

Fig. 6.19 Reconstructed protection system reaction to a type (iv) fault.

Table 6.1

Summary of the

MACHINE TEST RESULTS

FAULT TYPE	RELAY SETTING	NO. OF TRIALS	NUMBER INITIATED CORRECTLY	ERRORS		NO. OF CORRECT DECISIONS
				Undesired Tripping	Failure to Trip	
	3.9%	135	135	0	0	135
i	3.1%	135	135	0	0	135
	2.3%	135	135	0	0	135
	3.9%	72	72	0	0	72
ii	3.1%	72	72	0	0	72
	2.3%	72	72	0	0	72
	3.9%	25	25	0	0	25
iii	3.1%	25	25	0	0	25
	2.3%	25	25	0	0	25
	3.9%	25	25	0		25
iv	3.1%	25	25	0	N/A	25
	2.3%	25	25	0		25
	1.6%	25	25	9		16

were probed. These errors were of the "unwarranted tripping" type which are undesirable from the power system operation and reliability viewpoints. The discrimination limits for the test equipment was affected by three factors. First, the fault simulated was of a very serious nature. Secondly, no attempt was made to match the characteristics of the C.T.'s. Thirdly, the tape recorder introduced additional non-linearities. All these factors tend to decrease the discrimination ability but the linearity mismatches of the C.T.'s and the communications channels are controlled design parameters. As such, their error contributions to the difference current signal may be reduced by careful equipment matching in future

applications. As also indicated in Table 6.1 no "failure-to-trip" error was encountered throughout these tests. All verifications were properly initiated on a phase, which was involved in the fault, and all decisions were made less than three milliseconds after the incidence of the fault.

7. CONCLUSIONS

The percentage differential protection scheme, as presented in this thesis, provides several significant improvements over available electro-mechanical devices. This digital system is based on many parameters which can be easily varied, and is, therefore inherently more flexible. Programming the computer to modify the software variables, based on changing generating conditions, provides an additional dimension to fault detection and verification. On this basis, the traditional relatively fixed relationships, between the protective devices and their associated generator, can in future be replaced by dynamic interaction.

Adjusting the various thresholds and time constants, manually for the digital scheme presented in this thesis, demonstrated that a large variety of relay operating characteristics are possible. The single phase D.C. tests described in paragraph 6.1 (a), illustrate that the operating characteristics depend on the time constant of the modified sum current transient. It is obvious that the verification time can be altered by adjusting the evidence averaging limits. The monitor threshold determines the amplitude, which must be exceeded, before a more detailed examination of the conditions is initiated. Increasing the number of times a faulted phase must provide the largest of three difference current samples, increases the probability that it (the faulted phase) will be correctly selected for fault verification.

In the machine tests, described in paragraph 6.4, a fault/no fault decision was rendered in less than three milliseconds for almost 800 examined cases. This is significantly faster than the operating time of conventional devices. Continuing re-evaluation of marginal cases reduces the ambiguity in defining the operating condition although decision times

will be increased.

The relay performance, as evaluated by faults simulated on a machine, demonstrated the effectiveness of analog pre-processing the input data. As explained in Chapter 4, sequential digitizing of the line and neutral end currents could result in significant errors. The maximum sampling frequency of the SDS Sigma 2 computer, 15 kHz., would result in a maximum error of 7 percent in calculating the difference current. These errors were avoided by pre-processing the input information in parallel as described in Chapter 5. The resulting simple monitor design is further evidence of the effectiveness of the technique.

The organization of the proposed protection scheme lends itself to a time shared approach. The fault monitor only uses 40 percent of the available computation time between sucessive A/D conversions. Lower priority tasks could be executed during the remaining time. In addition, the execution of each pass of the monitor sequence could be intersperced with fixed intervals allocated to processing other programs.

The project also provided valuable experience in digitizing analog power system information for protection purposes. It demonstrated that digital computers can be applied to provide improved protection for generator stators and it supported the case for digital protection generally. When the digital protection scheme, described in this thesis, is applied to a generator operating in a power system, the settings of the software variables will have to be defined. To achieve accurate and efficient operation of the monitor, its threshold will have to be set as low as component mismatch and other noise will allow. The calculation threshold should be adjusted low enough to commence fault verification without excessive delay but high enough to prevent register overflows during division.

A compromise will be advisable, when setting the evidence averaging limits, to ensure that decisions are made quickly but with certainty.

Several means to improve the operation of the digital percentage differential protection scheme might be examined for future applications. The computer can be programmed to adjust the monitor threshold. Means might be employed to make the monitor threshold dynamically dependent on component mismatch and average noise. Evidence integration could be incorporated instead of evidence averaging. This may be implimented by subtracting the relay setting threshold from the quotient generated from the division of the amplified difference current by the modified sum current. The result could then be added to COUNT for each pass through the verification sequence. In this way the rate of approach to the threshold will be proportional to the weight of the evidence of each pass. Such a feature will permit fast reaction to serious faults and improved analysis of marginal conditions.

In the software used to test the proposed protection scheme, no provision was made to reactivate the monitor while the desired data was printed after a verified disturbance. The return branch to the monitor was simply delayed until printing was completed. In a power system time shared application, printing will have to be relegated to a lower priority routine. Establishing a hierarchy of execution priorities could be examined while extending the scope of digital protection for application to power plants.

Analog pre-processing of the input signals simplified the monitor and improved its accuracy and efficiency. This concept might be extended to provide an analog monitor with a digitally controlled threshold.

Sampling and digitizing data will not be required for stator protection unless the monitor indicated that a fault might be present. This solution would increase the efficiency of the digital computer assigned to generator protection and still permit the flexibility and speed of the tested scheme.

The concepts incorporated in the proposed digital percentage differential protection scheme are quite general. Future development could be directed to provide similar schemes to replace existing transformer and bus protection equipment. In transformer applications, the restraining function may have to be modified further to include an additional component, proportional to the second and higher harmonic currents. The additional restraint could be provided either in the fault verification sequence or in the analog pre-processor. Bus differential protection is conceivable with suitable adjustments to the software variables already provided. Of course, some duplication of the software and hardware will be required to process the additional inputs from the various transmission and feeder lines connected to the bus.

8. REFERENCES

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APPENDIX I

A listing of the program used to determine the viability of computing peak squared values from a sampled input sinusoid follows.

```
*  DIFFERENTIAL PROTECTION PROGRAM FREQUENCY ANALYSIS
*              IN XSYMBOL
*  THIS IS RUN WITH PROTECT OFF
DIFFSQ          COMMON    256
                COMMON    256
                REF       M:WRITE,M:TERM,L:DUMP
BEGIN           RD        *EAD
                BNO       $+2
                B         $-2
                LDA       =X'FFFO'
                RCPY      7,3
                RD        *EAD
                BNO       $+2
                B         $-2
                RAND      3,7
                STA       I+2
                RD        *EAD
                BNO       $+2
                B         $-2
                RAND      3,7
                STA       I+7
RECS AMP        RD        *EAD          RECURRENT SAMPLING BEGINS
                BNO       $+2
                B         $-2
                RAND      3,7
                STA       I
                LDX       COUNT
                STA       ISAMP,1
                LDA       I+2
                STA       I+3
                LDA       I+1
                STA       I+2
                LDA       I
                STA       I+1
                SARS      1
                ADD       I+1
                STA       IP+1
                LDA       I+2
                SALS      1
                STA       IP+2
                LDA       I+3
                SARS      1
                SUB       IP+2
                ADD       IP+1
```

```
                STA         IP
                MUL         IP
                SALD        9
                RCPY        6,7
                STA         IP
                LDA         I+1
                MUL         I+1
                RCPY        6,7
                ADD         IP
                STA         IP
                LDX         COUNT
                STA         DIFFSQ,1
                IM          COUNT
                LDA         COUNT
                SUB         =250
                BAZ         $+2
                B           RECS AMP
                RCPYI       1,2
                B           L:DUMP
                DATA        X'5000'
                ADRL        DIFFSQ
                ADRL        DIFFSQ+249
                RCPYI       1,2
                B           L:DUMP
                DATA        X'5000'
                ADRL        ISAMP
                ADRL        ISAMP+249
                RCPYI       1,2
                B           M:TERM
COUNT           RES         1
I               RES         4
IP              RES         3
EAD             DATA        X'AA01'
                LPOOL
                END         BEGIN
!EOD
```

APPENDIX II

The following is a listing of the three phase version of the digital percentage differential protection scheme proposed in this thesis. The software variables are set at:

i) monitor threshold - 50 m.v.,

ii) sensitivity setting - 2.3 percent,

iii) calculation threshold - 0.625 volts

iv) P - 2, equivalent to an imposed transient with 202 microsecond time constant,

v) back up threshold - 3.75 volts,

vi) back up counter limit - 10,

vii) evidence averaging counter limits - +6 and -5.

LISTING

```
                REF       M:TERM,M:WRITE,L:DUMP
IDIFFA          COMMON    32
IDIFFB          COMMON    32
IDIFFC          COMMON    32
ISUMA           COMMON    32
ISUMB           COMMON    32
ISUMC           COMMON    32
BEGIN           RCPY      0,4
 SET            RCPY      0,7
                STA       IDIFFA,1
                RCPY      4,7
                CP        -191
                BXN0      ZSET
PROTECT         RD        *EADDA
                BN0       $+2
                B         $-2
                RCPY      0,4
                RCPY      0,7
                STA       AFLAG
                STA       BFLAG
PTECTA          RCPY      0,7
                STA       CFLAG
                RCPYI     4,7
                CP        -32
                BXN0      $+2
                RCPY      0,4
                RD        *EADDB
                BN0       $+2
```

```
                B       $-2
                STA     IDIFFA,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                STA     PHASDET
                CP      =X'00A0'
                BN0     FLAGCKA
                B       ALL0CA
FLAGCKA         RCPY    0,7
                CP      BFLAG
                BN0     ALL0CA
                CP      CFLAG
                BN0     ALL0CA
                B       PTECTB
ALL0CA          RD      *EADDC
                BN0     $+2
                B       $-2
                STA     IDIFFB,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     $+2
                B       BLARGERA
                RD      *EADDA
                BN0     $+2
                B       $-2
                STA     IDIFFC,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     AM0STA
CM0STA          LDA     CFLAG
                IM      CFLAG
                CP      =1
                BN0     PTECTA+2
                RCPYI   4,7
                CP      =32
                BXN0    $+2
                RCPY    0,4
                B       VERIFYC
AM0STA          LDA     AFLAG
                IM      AFLAG
                CP      =1
                BN0     PTECTA+2
                RCPYI   4,7
                CP      =32
                BXN0    $+2
                RCPY    0,4
                B       VERIFYA
BLARGERA        STA     PHASDET
                RD      *EADDA
                BN0     $+2
                B       $-2
                STA     IDIFFC,1
                BAN     $+2
                B       $+2
```

```
                RCPYI   *7,7
                CP      PHASDET
                BN0     BM0STA
                B       CM0STA
BM0STA          LDA     BFLAG
                IM      BFLAG
                CP      -1
                BN0     PTECTA+2
                RCPYI   4,7
                CP      -32
                BXN0    $+2
                RCPY    0,4
                B       VERIFYB
PTECTB          RCPY    0,7
                STA     AFLAG
                RD      *EADDC
                BN0     $+2
                B       $-2
                STA     IDIFFB,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                STA     PHASDET
                CP      =X'00A0'
                BN0     FLAGCKB
                B       ALL0CB
FLAGCKB         RCPY    0,7
                CP      CFLAG
                BN0     ALL0CB
                CP      AFLAG
                BN0     ALL0CB
                B       PTECTC
ALL0CB          RD      *EADDA
                BN0     $+2
                B       $-2
                STA     IDIFFC,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     $+2
                B       CLARGERB
                RCPYI   4,7
                CP      -32
                BXN0    $+2
                RCPY    0,4
                RD      *EADDB
                BN0     $+2
                B       $-2
                STA     IDIFFA,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     BM0STB
                LP00L
AM0STB          LDA     AFLAG
                IM      AFLAG
```

```
                CP      =1
                BNZ     PTECTB+2
                RCPYI   4,7
                CP      =32
                BXNZ    $+2
                RCPY    0,4
                B       VERIFYA
BMZSTB          LDA     BFLAG
                IM      BFLAG
                CP      =1
                BNZ     PTECTB+2
                B       VERIFYB
CLARGERB        STA     PHASDET
                RCPYI   4,7
                CP      =32
                BXNZ    $+2
                RCPY    0,4
                RD      *EADDB
                BNZ     $+2
                B       $-2
                STA     IDIFFA,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BNZ     CMZSTB
                B       AMZSTB
CMZSTB          LDA     CFLAG
                IM      CFLAG
                CP      =1
                BNZ     PTECTB+2
                B       VERIFYC
PTECTC          RCPY    0,7
                STA     BFLAG
                RD      *EADDA
                BNZ     $+2
                B       $-2
                STA     IDIFFC,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                STA     PHASDET
                CP      =X'00A0'
                BNZ     FLAGCKC
                B       ALLZCC
FLAGCKC         RCPY    0,7
                CP      AFLAG
                BNZ     ALLZCC
                CP      BFLAG
                BNZ     ALLZCC
                B       PTECTA
ALLZCC          RCPYI   4,7
                CP      =32
                BXNZ    $+2
                RCPY    0,4
                RD      *EADDB
                BNZ     $+2
```

```
                B       $-2
                STA     IDIFFA,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     $+2
                B       ALARGERC
                RD      *EADDC
                BN0     $+2
                B       $-2
                STA     IDIFFB,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     CM0STC
BM0STC          LDA     BFLAG
                IM      BFLAG
                CP      -1
                BN0     PTECTC+2
                RCPYI   4,7
                CP      -32
                BXN0    $+2
                RCPY    0,4
                B       VERIFYB
CM0STC          LDA     CFLAG
                IM      CFLAG
                CP      -1
                BN0     PTECTC+2
                B       VERIFYC
EADDA           DATA    X'AA00'
EADDB           DATA    X'AA01'
EADDC           DATA    X'AA02'
EADSA           DATA    X'AA03'
EADSB           DATA    X'AA04'
EADSC           DATA    X'AA05'
                LP00L
ALARGERC        STA     PHASDET
                RD      *EADDC
                BN0     $+2
                B       $-2
                STA     IDIFFB,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                CP      PHASDET
                BN0     AM0STC
                B       BM0STC
AM0STC          LDA     AFLAG
                IM      AFLAG
                CP      -1
                BN0     PTECTC+4
                RCPYI   4,7
                CP      -32
                BXN0    $+2
                RCPY    0,4
```

```
VERIFYA     RD      *EADDA
            BN0     $+2
            B       $-2
            RCPY    0,7
            STA     C0UNT
            STA     C0UNTB
            STA     SUMSAMP
            RD      *EADSA
            BN0     $+2
            B       $-2
            STA     IDIFFA,1
            BAN     $+2
            B       $+2
            RCPYI   *7,7
            STA     IBCKUP
            RCPY    0,6
            SALD    7
            RCPY    7,3
            RCPY    4,7
            RCPY    4,2
            CP      =1
            BN0     $+2
            B       $+2
            ADD     =32
            SUB     =1
            RCPY    7,4
            LDA     ISUMA,1
            RCPY    2,4
            BAN     $+2
            B       $+2
            RCPYI   *7,7
            SUB     SUMSAMP
            SARS    1
            ADD     SUMSAMP
            STA     SUMSAMP
            RD      *EADDA
            BN0     $+2
            B       $-2
            STA     ISUMA,1
            RCPYI   4,7
            CP      =32
            BXN0    $+2
            RCPY    0,4
            LDA     SUM SAMP
            CP      =X'0800'
            BN0     UNDEFSA
            B       DEFSA
UNDEFSA     LDA     IBCKUP
            CP      =X'3000'
            BN0     VERIFYA+7
            IM      C0UNTB
            LDA     C0UNTB
            CP      =X'000A'
            BN0     VERIFYA+7
            B       FAULTA
DEFSA       RCPY    3,7
            DIV     SUMSAMP
```

```
                CP      =3
                BNZ     DECRA
                IM      COUNT
                LDA     =5
                CP      COUNT
                BNZ     FAULTA
                B       VERIFYA+7
DECRA           LDA     COUNT
                SUB     =1
                STA     COUNT
                RCPYI   *7,7
                CP      =5
                BNZ     VERIFYA+7
                B       TRANSA
VERIFYB         RD      *EADDB
                BNZ     $+2
                B       $-2
                RCPY    0,7
                STA     COUNT
                STA     COUNTB
                STA     SUMSAMP
                RD      *EADDB
                BNZ     $+2
                B       $-2
                STA     IDIFFB,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                STA     IBCKUP
                RCPY    0,6
                SALD    7
                RCPY    7,3
                RCPY    4,7
                RCPY    4,2
                CP      =1
                BNZ     $+2
                B       $+2
                ADD     =32
                SUB     =1
                RCPY    7,4
                LDA     ISUMB,1
                RCPY    2,4
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                SUB     SUMSAMP
                SARS    1
                ADD     SUMSAMP
                STA     SUMSAMP
                RD      *EADDB
                BNZ     $+2
                B       $-2
                STA     ISUMB,1
                RCPYI   4,7
                CP      =32
                BXNZ    $+2
                RCPY    0,4
```

```
                LDA     SUMSAMP
                CP      =X'0800'
                BNO     UNDEFSB
                B       DEFSB
UNDEFSB         LDA     IBCKUP
                CP      =X'3000'
                BNO     VERIFYB+7
                IM      COUNTB
                LDA     COUNTB
                CP      =X'000A'
                BNO     VERIFYB+7
                B       FAULTB
DEFSB           RCPY    3,7
                DIV     SUMSAMP
                CP      =3
                BNO     DECRB
                IM      COUNT
                LDA     =5
                CP      COUNT
                BNO     FAULTB
                B       VERIFYB+7
DECRB           LDA     COUNT
                SUB     =1
                STA     COUNT
                RCPYI   *7,7
                CP      =5
                BNO     VERIFYB+7
                B       TRANSB
                LPOOL
VERIFYC         RD      *EADDC
                BNO     $+2
                B       $-2
                RCPY    0,7
                STA     COUNT
                STA     COUNTB
                STA     SUMSAMP
                RD      *EADSC
                BNO     $+2
                B       $-2
                STA     IDIFFC,1
                BAN     $+2
                B       $+2
                RCPYI   *7,7
                STA     IBCKUP
                RCPY    0,6
                SALD    7
                RCPY    7,3
                RCPY    4,7
                RCPY    4,2
                CP      =1
                BNO     $+2
                B       $+2
                ADD     =32
                SUB     =1
                RCPY    7,4
                LDA     ISUMC,1
                RCPY    2,4
                BAN     $+2
```

```
                B       $+2
                RCPYI   *7,7
                SUB     SUMSAMP
                SARS    1
                ADD     SUMSAMP
                STA     SUMSAMP
                RD      *EADDC
                BN0     $+2
                B       $-2
                STA     ISUMC,1
                RCPYI   4,7
                CP      =32
                BXN0    $+2
                RCPY    0,4
                LDA     SUMSAMP
                CP      =X'0800'
                BN0     UNDEFSC
                B       DEFSC
UNDEFSC         LDA     IBCKUP
                CP      =X'3000'
                BN0     VERIFYC+7
                IM      COUNTB
                LDA     COUNTB
                CP      =X'000A'
                BN0     VERIFYC+7
                B       FAULTC
DEFSC           RCPY    3,7
                DIV     SUMSAMP
                CP      =3
                BN0     DECRC
                IM      COUNT
                LDA     =5
                CP      COUNT
                BN0     FAULTC
                B       VERIFYC+7
DECRC           LDA     COUNT
                SUB     =1
                STA     COUNT
                RCPYI   *7,7
                CP      =5
                BN0     VERIFYC+7
                B       TRANSC
                LPOOL
FAULTA          LDX     =LISTAF
                RCPYI   1,2
                B       M:WRITE
                LDX     =LISFDA
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    IDIFFA
                ADRL    IDIFFA+31
                LDX     =LISFSA
                RCPYI   1,2
                B       M:WRITE
```

```
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    ISUMA
                ADRL    ISUMA+31
                RCPYI   1,2
                B       M:TERM
TRANSA          LDX     =LISTAT
                RCPYI   1,2
                B       M:WRITE
                LDX     =LISFDA
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    IDIFFA
                ADRL    IDIFFA+31
                LDX     =LISFSA
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    ISUMA
                ADRL    ISUMA+31
                LDX     =LIST
                RCPYI   1,2
                B       M:WRITE
                B       BEGIN
FAULTB          LDX     =LISTBF
                RCPYI   1,2
                B       M:WRITE
                LDX     =LISFDB
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    IDIFFB
                ADRL    IDIFFB+31
                LDX     =LISFSB
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    ISUMB
                ADRL    ISUMB+31
                RCPYI   1,2
                B       M:TERM
                LPOOL
TRANSB          LDX     =LISTBT
                RCPYI   1,2
                B       M:WRITE
                LDX     =LISFDB
                RCPYI   1,2
```

```
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    IDIFFB
                ADRL    IDIFFB+31
                LDX     =LISFSB
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    ISUMB
                ADRL    ISUMB+31
                LDX     =LIST
                RCPYI   1,2
                B       M:WRITE
                B       BEGIN
FAULTC          LDX     =LISTCF
                RCPYI   1,2
                B       M:WRITE
                LDX     =LISFDC
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    IDIFFC
                ADRL    IDIFFC+31
                LDX     =LISFSC
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    ISUMC
                ADRL    ISUMC+31
                RCPYI   1,2
                B       M:TERM
TRANSC          LDX     =LISTCT
                RCPYI   1,2
                B       M:WRITE
                LDX     =LISFDC
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    IDIFFC
                ADRL    IDIFFC+31
                LDX     =LISFSC
                RCPYI   1,2
                B       M:WRITE
                RCPYI   1,2
                B       L:DUMP
                DATA    X'5000'
                ADRL    ISUMC
```

```
                ADRL    ISUMC+31
                LDX     =LIST
                RCPYI   1,2
                B       M:WRITE
                B       BEGIN
LISTAF          DATA    X'2005','CC',MESS1,18
MESS1           TEXT    '0A STATOR FAULTED!'
LISTBF          DATA    X'2005','CC',MESS2,18
MESS2           TEXT    '0B STATOR FAULTED!'
LISTCF          DATA    X'2005','CC',MESS3,18
MESS3           TEXT    '0C STATOR FAULTED!'
LISFDA          DATA    X'2005','CC',MESS4,40
MESS4           TEXT    '0DUMP F I DIFFERENCE A SAMPLES FOLLOWS!'
LISTAT          DATA    X'2005','CC',MESS6,38
MESS5           TEXT    '0DUMP OF I SUM A SAMPLES FOLLOW!'
LISFSA          DATA    X'2005','CC',MESS5,32
MESS6           TEXT    '0TRANSIENT CAUSED DROP INTO A VERIFY!'
LISTBT          DATA    X'2005','CC',MESS7,38
MESS7           TEXT    '0TRANSIENT CAUSED DROP INTO B VERIFY!'
LISTCT          DATA    X'2005','CC',MESS8,38
MESS8           TEXT    '0TRANSIENT CAUSED DROP INTO C VERIFY!'
                LPOOL
LIST            DATA    X'2005','CC',MESS9,38
MESS9           TEXT    '0RETURNING TO MONITOR SYSTEM OKAY????'
LISFDB          DATA    X'2005','CC',MESS10,40
MESS10          TEXT    '0DUMP OF I DIFFERENCE B SAMPLES FOLLOWS!'
LISFSB          DATA    X'2005','CC',MESS11,32
MESS11          TEXT    '0DUMP OF I SUM B SAMPLES FOLLOW!'
LISFDC          DATA    X'2005','CC',MESS12,40
MESS12          TEXT    '0DUMP OF I DIFFERENCE C SAMPLES FOLLOW!'
LISFSC          DATA    X'2005','CC',MESS13,32
MESS13          TEXT    '0DUMP OF I SUM C SAMPLES FOLLOW!'
COUNT           RES     1
AFLAG           RES     1
BFLAG           RES     1
CFLAG           RES     1
PHASDET         RES     1
SUMSAMP         RES     1
COUNTB          RES     1
IBCKUP          RES     1
                LPOOL
                END     BEGIN
!EOD
```

APPENDIX III

The name plate data for the A.C. generator and motor used in the machine tests are as follows:

a) Generator

kVa	5	CYCLES	60
VOLTS	110/220	RPM	1200
AMPS	26/13	EXC. AMPS	3
P.F.	.90	EXC. VOLTS	125
PHASE	1/3/6	SO	53N157

SERIAL 6-53N157

MANUFACTURER WESTINGHOUSE

b) Motor - varying speed, compound wound.

HP	7.25	PPM	850-1200
AMPS	2.7	HOURS	24
VOLTS	230	STYLE	53N158

SERIAL 6-53N158

MANUFACTURER WESTINGHOUSE