Hardware-in-the-Loop Prototype of a Negative Sequence Based Scheme for Turn-to-Turn Fault Detection in Transformers

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by

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Abstract

During the course of a transformer's operational life, it experiences many challenges to its insulation. Chemical stresses, such as moisture in insulating oil, deteriorate insulation chemically. Mechanical stresses and thermal stresses, such as those experienced during a large external fault, also contribute to weakening a transformer's insulation. Once these stresses have weakened the insulation to the point of breakdown, a fault may occur between windings of the transformer. These faults, known as turn-to-turn faults, are difficult to detect electrically at the terminals of the transformer until they have grown to the point of damaging the transformer beyond repair.

Current differential transformer protection is a simple, reliable, and cost effect method of detecting turn-to-turn faults. This method of protection is only able to detect faults involving 10% of the windings or more. The sensitivity of current differential protection is limited as not to cause false tripping due to normal imbalances in current. Such imbalances in current may occur when a tapchanger is used to increase or decrease the voltage on one side of the transformer. Digital current differential relays, which monitor tap changer position, compensate for current imbalances due to tapchanger operation. Other causes of current imbalance include current transformer saturation, magnetizing inrush current, and overexcitation. A transformer is designed to operate continuously at 10% above its rated voltage. In this overexcited state, a current imbalance appears which causes a differential current to be sensed by the current differential relay. This limits the current differential relay's sensitivity as it must be designed to ignore current imbalances due to the aforementioned causes.

The current differential transformer protection algorithm, which only makes use of the current magnitude, is based on the principles of an electromechanical relay. Digital relays are capable of computing the negative sequence current on both primary and secondary sides of the transformer along with the phase difference between these two negative sequence currents. By using both phase and magnitude information, negative sequence current could be used to detect turn-to-turn faults involving 3% of the transformer's windings or more.

Turn-to-turn faults may still occur even if no current is flowing on one side of the trans-

former, such as during energization. With no current flowing in the secondary windings of the transformer, negative sequence current based algorithms become insensitive. A transformer is particularly likely to experience a turn-to-turn fault during this time due to the stresses of energization. This thesis introduces a relay prototype, using both negative sequence current and negative sequence voltage, which retains its sensitivity during energization.

This prototype was constructed using a micro-controller and an analog-to-digital conversion board. The transformer protection relay algorithm, including all hardware interface code and signal processing code, was then designed to suit the prototype's hardware. A 3-phase transformer real-time simulation model, capable of simulating turn-to-turn faults as well as the magnetic properties of the transformer's core, was developed. The voltage and current waveforms generated by the transformer model, running in the real-time simulator, were used to test the relay prototype.

The sensitivity and speed of the relay algorithm proposed in this thesis was then tested, for faults involving 1%, 3%, 5%, 10%, 15%, and 25% of the windings along with two commonly encountered transformer winding configurations. The relay's performance for several commonly encountered system scenarios such as over-excitation, current transformer saturation, non-zero fault resistance, transformer energization, and external faults were also examined for several turn-to-turn fault severities. A fault resistance of one Ohm is typical for transformer turn-to-turn faults. These test results were compared to current differential protection with second harmonic restraint. The experimental results presented in this work indicate that the algorithm proposed in this thesis is faster and more sensitive than restrained current differential protection and capable of detecting turn-to-turn faults occurring during transformer energization.

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List of Symbols and Abbreviations

(int)	Integer Cast
$>>$	Bit-Shift Operator
$\mathcal{R}$	Magnetic Reluctance
$\mathfrak{F}$	Magneto-motive Force
$\mathfrak{F}_p$	Magneto-motive Force produced by Primary Windings
$\mathfrak{F}_s$	Magneto-motive Force produced by Secondary Windings
μ	Magnetic Permeability
μ_o	Magnetic Permeability of Vacuum
ω	Angular Frequency ($2\pi 60$ Hz)
ϕ	Time varying flux
Θ	Phase Shift
$\vec{B}$	Leakage Flux Density Vector
$\vec{B}x$	Radial Leakage Field Vector
$\vec{B}y$	Axial Leakage Field Vector
$\vec{F}$	Force Vector
$\vec{I}$	Current Phasor
$\vec{I}_a$, $\vec{I}_b$, $\vec{I}_c$	Phase Currents
$\vec{I}_{0_{Pr}}$, $\vec{I}_{1_{Pr}}$, $\vec{I}_{2_{Pr}}$	Zero, Positive, and Negative-sequence Primary Currents

$\vec{I}_{0_{Sec}}$, $\vec{I}_{1_{Sec}}$, $\vec{I}_{2_{Sec}}$	Zero, Positive, and Negative-sequence Secondary Currents
$\vec{I}_{2P}$, $\vec{I}_{2S}$	Primary, Secondary Negative Sequence Current
$\vec{V}_{0_{Pr}}$, $\vec{V}_{1_{Pr}}$, $\vec{V}_{2_{Pr}}$	Zero, Positive, and Negative-sequence Primary Voltages
$\vec{V}_{0_{Sec}}$, $\vec{V}_{1_{Sec}}$, $\vec{V}_{2_{Sec}}$	Zero, Positive, and Negative-sequence Secondary Voltages
A	Area of Magnetic Core
a	$1\angle 120°$
A_w	Area of Excited Winding
a_{XFMR}	Transformer Ratio
ARG	Argument Operator of Complex Number
B_r	Residual Flux Density
$CCVT$	Coupling Capacitor Voltage Transformer
e_p, e_s	Primary, Secondary Electromotive Force
EPV	Extended Park's Vector
H	Magnetic Field
H_c	Coercive Force
h_w	Height of Excited Winding
i_{m1}, i_{m2}	Magnetizing Currents
i_1, i_2, i_3, i_4	Four Winding Transformer Model Current
I_d	Differential Current
i_p, i_s	Primary, Secondary Current
I_r	Restraining Current

I_{-ve}	Negative Sequence Current
$I_{PrThres}$	Primary Negative Sequence Current Threshold
I_{pu}	Pick-up Current
I'_P	Primary Current on Secondary of Current Transformer
$I_{S.C.}$	Short-Circuit Current
$I_{SecThres}$	Secondary Negative Sequence Current Threshold
I'_S	Secondary Current on Secondary of Current Transformer
Im	Imaginary Component of Complex Number
JAH	Jiles-Atherton Hysteresis
K	Slope of the Percentage Differential Characteristic
L	Magnetic Inductance
l	Magnetic Core Length
L_w	Winding Length
L_{11}, L_{22}, L_{33}, L_{44}	Four Winding Transformer Model Self Inductances
L_{12}, L_{21}, etc	Four Winding Transformer Model Self Inductances
L_{air}	Knee Voltage
MMF	Magneto-Motive Force
N	Number of Winding Turns
N'_p	Primary Turns Ratio, given Turn-to-Turn Fault
N'_s	Secondary Turns Ratio, given Turn-to-Turn Fault
N_p, N_s	Primary, Secondary Winding Turns

N_{eff}, N_A, N_C	Turns Ratios in Faulted Transformer
$NSCA$	Negative Sequence Current based Algorithm
$NSVA$	Negative Sequence Voltage based Algorithm
$OLTC$	On-Load Tap-Changer
R_{11}, R_{22}, R_{33}, R_{44}	Four Winding Transformer Model Winding Resistance
Re	Real Component of Complex Number
ROA	Relay Operating Angle
$RTDS$	Real Time Digital Simulator
S_B	Rated Power
$SF6$	Sulfur Hexafluoride
V_s'	Secondary Voltage, given Turn-to-Turn Fault
V_1, V_2, V_3, V_4	Four Winding Transformer Model Voltages
V_c	Volume of Magnetic Core
V_p, V_s	Primary, Secondary Voltage
V_d	Negative Sequence Differential Voltage
V_{knee}	Knee Voltage
$V_{Peak,LG}$	Peak Voltage, measured line-to-ground
V_{Pf}	Primary Voltage on Faulted Transformer
V_{PP}	Primary Source Voltage
V_r	Negative Sequence Restraining Voltage
V_{Sf}	Secondary Voltage on Faulted Transformer

V_{SS}	Secondary Source Voltage
W_H	Hysteresis Loss
X_f	Short Circuit Reactance of Faulted Transformer
$X_{SourcePr}$	Primary Source Impedance
$X_{SourceSec}$	Secondary Source Impedance
X_{XFMR_P}	Faulted Transformer Matrix Referred to Primary
X_{XFMR}	Short Circuit Transformer Reactance

Chapter 1

Introduction

1.1 Background

The electric power transformer is a vital component of the modern AC power grid. Invented at the end of the nineteenth century, transformers have allowed for more efficient production of electrical power. High current, low voltage generators can be located close to a source of energy, such as water or coal. Generator transformers step up the voltage of this freshly generated electrical power allowing it to be transmitted efficiently to the load which can be located a great distance from the generators [1].

As a technology that has been refined for more than a hundred years, large power transformers are rarely the cause of a power outage. But when a failure does occur, the results can be disastrous. An arc burning inside a large, oil-filled transformer produces hydrogen gas. The time between the striking of an arc and catastrophic failure depends on the type of fault and the size of the fault involved [2]. One of the leading causes of an arc is a turn-to-turn fault. Such a fault can develop when the insulation between turns breaks down. Insulation can deteriorate due to excessive heat, oxidation, acidity of the insulating oil, and the presence of moisture in the insulating oil. Electrical faults, occurring external to the transformer, also contribute to the aging of the transformer's insulation. The mechanical stresses accumulated during years of external faults can weaken the transformer's insulation to the point where the insulation dielectric-withstand strength fails and a turn-to-turn fault occurs. [3].

Turn-to-turn faults are particularly insidious in that they can elude the transformer's

protection system until much damage has been done. There can be a large current flowing between a small group of shorted windings while there is little change in the magnitude of the current at the transformer's terminals. Currently, the best defense against such faults is the sudden pressure relay. This relay will signal a trip before the arcing, inside the transformer's tank, releases enough gas to cause an explosion. This action may prevent damage to the area surrounding the transformer but it may not save the transformer core from irreparable damage [4]. The concept of turn-to-turn faults will be explored in more detail in Section 1.3.

1.2 Transformer Basics

1.2.1 Single-Phase Transformer Theory

A model of an ideal single phase transformer is given in Figure 1.1. An ideal transformer has the following characteristics [5]: the core is made of a material with nearly infinite permeability, there are no losses due to eddy currents or hysteresis, all the flux generated by the windings is contained within the core, and the winding resistance is nearly zero Ohm. A sinusoidal voltage, V_p is applied across N_p windings. A current, i_p, flows through the windings which creates a magnetomotive force (MMF), given by Equation 1.1. This flux induces an electromotive force (emf) in the primary windings according to Faraday's Law of Induction, given by Equation 1.2. The assumption of an ideal transformer ensures that the flux circulates around the ideal core without losses. Therefore, the emf induced in the secondary winding is given by Equation 1.3.

$$\mathfrak{F} = Ni \tag{1.1}$$

$$e_p = -N_p \frac{d\Phi}{dt} \tag{1.2}$$

$$e_s = -N_s \frac{d\Phi}{dt} \tag{1.3}$$

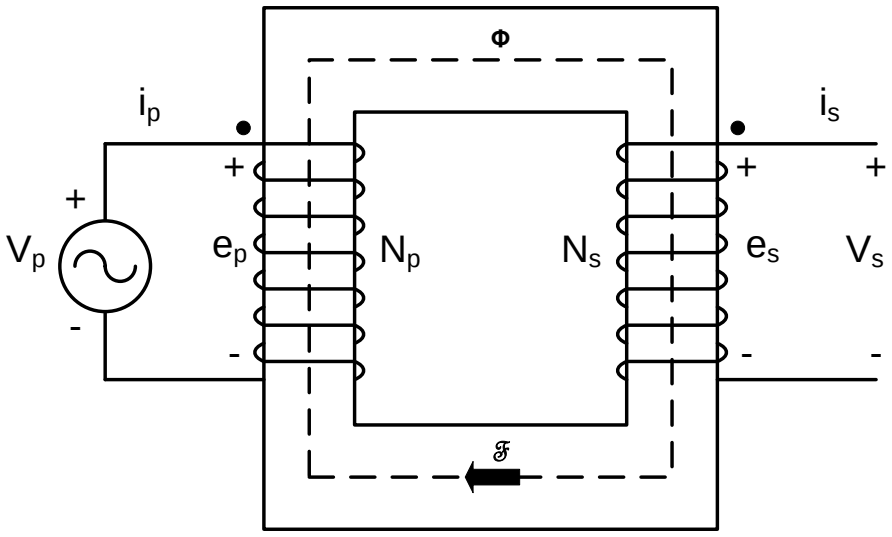

Figure 1.1: Single Phase Transformer Model

Since the rate of change of flux is the same in both primary and secondary windings, the transformer's voltage ratio, given by a_{XFMR}, may be derived using the primary and secondary windings as given by Equation 1.4. The current flowing through the transformer's load, Z_L, must be considered in order to derive the transformer's current ratio. Current flowing through the secondary windings causes an equal MMF in the opposite direction to the MMF induced by the primary windings, as shown in Figure 1.2. $\mathfrak{F}_s$ and $\mathfrak{F}_p$ represent the MMF produced by the primary windings and the scondary windings respectively. From this observation the transformer's current ratio, Equation 1.5, may be constructed.

$$\frac{V_p}{V_s} = a_{XFMR} = \frac{N_p}{N_s} \tag{1.4}$$

$$\frac{i_s}{i_p} = a_{XFMR} = \frac{N_p}{N_s} \tag{1.5}$$

In order for Equation 1.1 to be valid, each winding must completely enclose the core as required by Ampere's Law described by Equation 1.6 [5]. The magnetic field along closed loop "c" is equal to the current density incident upon a surface area "s". Surface "s" is defined by a perimeter defined by the closed loop "c". The vectors associated with this equation are shown in Figure 1.3. Contour "c" is shown as a dashed line while surface "s"

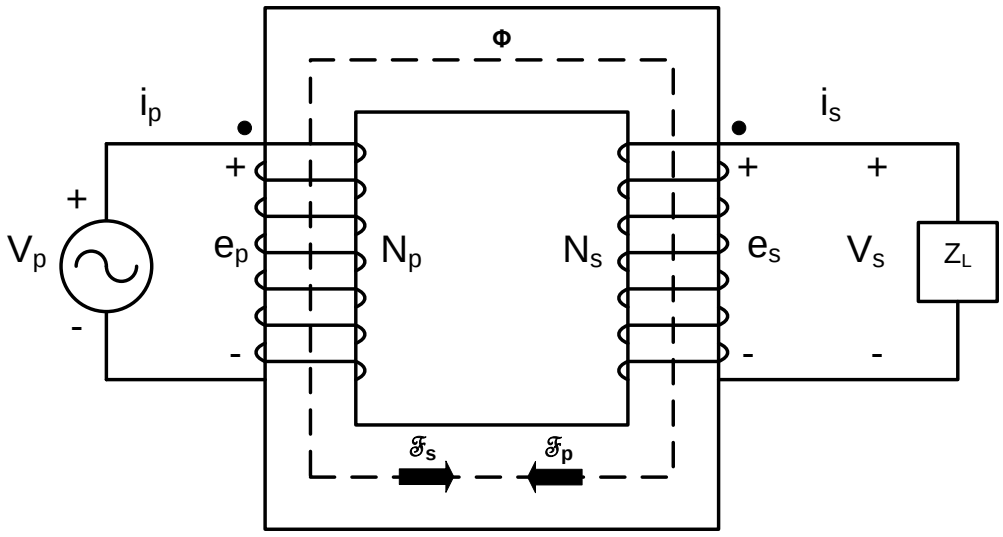

Figure 1.2: Single Phase Transformer Model with Load

is depicted as crosshatched fill. Note that only a current density, given by J_p and J_s, that is parallel to the surface's normal vector, ds, will contribute to the MMF. This concept is essential to understanding why the transformer's turn ratio changes should a turn-to-turn fault occur.

$$\mathfrak{F} = \oint_c \vec{H} \bullet \vec{dl} = \int\int_s \vec{J} \bullet \vec{ds} = Ni \tag{1.6}$$

1.2.2 Windings

The structure of a transformer's windings will be discussed in detail in order to give a clearer picture of the turn-to-turn fault scenario. Transformers are compromised of at least two sets of electrically conductive windings wound around a common steel core. For the purposes of this illustration, a single phase, two winding distribution transformer will be discussed: one set of windings designated the low voltage (LV) winding while the of the other set of windings will be called the high voltage (HV) winding. The low-voltage (LV) windings of a transformer carry a higher current load than the high-voltage (HV) windings. The low voltage windings are situated closest to the core and wound in a simple helix [1]. The LV windings are thick, and are constructed of typically 14 insulated parallel strands in order to

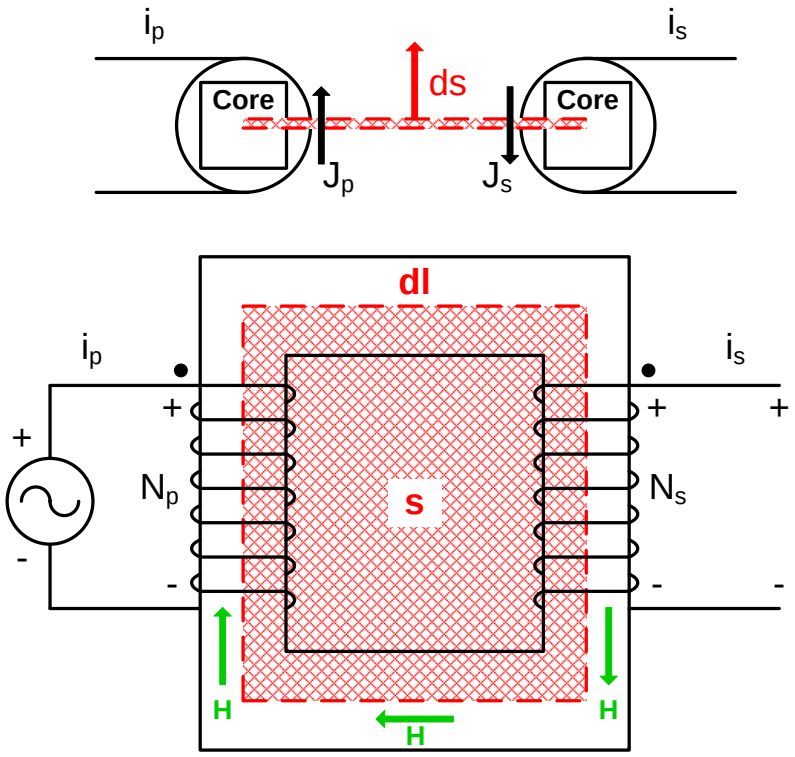

Figure 1.3: Ampere's Law

reduce eddy current losses. Stranding also allows for easier winding of what would otherwise be a single, thick conductor.

Press-board, rolled to form cylinders, are fitted over the LV windings in order to separate them from the HV windings. Annular spaces are left between successively larger radius of press-board cylinder to allow for oil flow. HV windings have a much lower cross-sectional area than LV windings and are typically composed of two strand conductors. Since the HV winding is composed of more turns than the LV windings, HV windings must be wound several layers deep in order to have the same axial length as the LV windings. This ensures good coupling between the two sets of windings.

A multi-layered helical winding configuration would create a large voltage difference between successive layers. Therefore a method of winding called Continuous Disc Winding is used for HV windings. Transformer winding conductor has a rectangular cross-section. This allows the conductor to be wound around the press-board cylinder, surrounding the LV windings, each turn stacked upon the next to form a disk. The disks, each being approximately

5 windings wide, are stacked along the long axis of the press-board cylinder. Each disk is separated by spacers from its neighbors. This method of winding can be accomplished by assembling the first winding out from the press-board cylinder and then winding the second winding in reverse, from the outside most winding in to the press-board cylinder. This allows a single unbroken conductor to create successive layers of a winding disk which also represent successive steps of voltage. Therefore, the voltage per turn ratio on either LV and HV side is the same in a continuously disc wound transformer.

1.2.3 Mechanical Forces acting On Windings

A transformer's windings conduct current while exposed to a magnetic field. This results in a force, described by the Lorentz Force Law [6] , acting on the winding.

$$\vec{F} = L_w \vec{I} X \vec{B} \tag{1.7}$$

The leakage flux density vector is best described using two components: a radial leakage field (B_x) and an axial leakage field (B_y) [7]:

$$\vec{B} = \vec{B}_x + \vec{B}_y \tag{1.8}$$

The axial leakage field subjects the windings to radial forces. The inner LV windings experience a compressive radial force, acting to crush the windings toward the core. The outer HV windings experience a tensile radial force as a result of the axial leakage field. A radial leakage field is created at each winding end and subjects the winding to axial forces. Under ideal conditions, the axial force at one end of the winding coil is exactly opposed by the axial force at the other end of the winding. Both the LV and HV windings experience this compressive force along their long axis.

How these forces affect the winding insulation is of particular interest. A potential for insulation damage exits if the tensile radial force is sufficient to stretch the outer winding. Compressive radial forces may also stress insulation by buckling the windings. Resonance effects due to radial forces is a very remote possibility as the elasticity of copper is large and the mass is small, making the natural frequency much higher than 50 or 60 Hz.

This is not so in the axial direction. The natural frequency in this direction is affected by insulation. Since insulation is easily compressible, the axial natural frequency may come close to frequencies present during short circuit events. If a winding within a disk is not wound tightly enough, vibration induced by axial forces can damage the winding's insulation leading to a turn-to-turn fault.

Axial forces can also damage insulation by pushing windings down between radially placed insulation spacers. Tilting of conductors however is one of the most common causes of transformer failure [8]. Forces acting to compress the windings axially can twist rectangular windings as shown in Figure 1.4. High-voltage windings have been found to be more susceptible to turn-to-turn faults [2], [1].

Figure 1.4: Example of Conductor Tilting (Cross-Section)

1.3 Insulation Failure and Turn-to-Turn Faults

1.3.1 Insulation Failure

Before a turn-to-turn fault can occur, the insulation separating a transformer's turns must fail electrically. Therefore a closer look at insulation failure is warranted. Insulation failure of a transformer's winding is associated with older transformers. Due to a transformer installation boom in the 1970's, there are a significant number of older transformer in operation today [9]. But for a power transformer, age is not just a matter of chronological passage of time.

Excessive heat stress and excessive mechanical stress experienced during external faults are the main contributors to insulation damage. Other factors, such as moisture trapped in insulation, greatly amplify the damage done at a higher than normal temperature [10]. Points of higher temperature within a transformer's winding are known as hot spots.

As discussed in Section 1.2.3 mechanical forces result from the interaction of the leakage flux and the current flowing through the windings. Large external faults can mechanically strain the windings of the transformer. As electrical infrastructure expands its short circuit capacity increases. This increases the fault current flowing through a transformer during an external fault. The increased fault current increases the mechanical stresses experienced by the transformer coils during a fault. Insulation stresses work in concert with mechanical stresses [11] until the transformer fails.

A hot spot is location inside the transformer that is hotter than the measured temperature of the transformer [1]. There are many factors that contribute to the formation of a hot spot. The type of oil circulation used to cool the transformer, the pattern of the leakage flux, and the eddy current losses can vary in different parts of the windings. While the method of cooling is determined at manufacturing, the leakage flux pattern and eddy current losses, within the windings, vary with the electrical current flowing through a transformer at any given moment.

Harmonics present in the currents flowing through a transformer produce a rise in temperature, particularly in the windings [12]. These harmonics are associated with losses due to eddy currents. The effect of eddy currents can be modeled as a change in effective resistance of the winding called A.C. resistance. The coil's A.C. winding resistance is dependent on leakage flux cutting the conductor [13]. The presence of harmonics in electric power currents is not unusual and can have a variety of sources such as transformer inrush or the presence of power electronic devices on the line.

The chemistry of the oil and insulation interaction also plays a role. The insulating oil penetrates the paper, cloth, and wood insulation used to separate the transformer's windings. Therefore changes to the insulating oil's chemical properties will affect how it interacts with

the solid insulation inside the transformer tank. Due to the presence of oxygen inside the tank, oil oxidizes even under ideal conditions. Oil, oxygen and moisture react to form acidic compounds that attack cellulose fibers comprising the insulation. Heat acts to accelerate this process [14]. Oil conservators with dehydrating breathers can be used to reduce the amount of oil exposed to air but this only serves to slow the oxidation process, not stop it [1]. Even with an effective breather dehydration system, water produced by insulation degradation will enter the transformer oil and contaminate it. This degradation of insulation occurs in a normally loaded transformer and is unavoidable [1].

1.3.2 Turn-to-Turn Faults

A Turn-toTurn fault can be visualized and modeled as a short between windings as shown in Figure 1.5 [15]. The familiar two winding single phase transformer is used as a starting point. The secondary winding is split into three separate windings. Under normal operation, these windings would be connected in series and the transformer would function as an unfaulted two winding single phase transformer. During a turn-to-turn fault a current, I_F, is allowed to flow due to an insulation failure between the windings. The secondary current, I_S, would show very little change for a fault involving a small number of turns, N_B, as the effective turns ratio during fault, given by equation 1.9 would be very close to the specified turns ratio.

$$N_{eff} = N_A + N_C \tag{1.9}$$

A transformer suffering from a turn-to-turn fault, no matter how few turns are involved, should be taken out of service immediately. At present, such faults must grow to the point of seriously damaging the transformer beyond repair before they can be detected. The detection methods, which will be discussed in Section 1.6, serve to protect the area surrounding the transformer by preventing a catastrophic explosion.

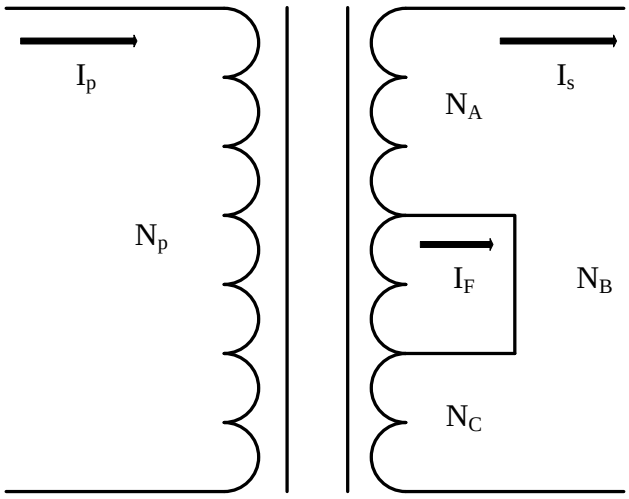

Figure 1.5: Schematic of Turn-to-Turn Fault

1.4 Inrush Current

During energization of a transformer, the primary side of the transformer is connected to a voltage source while the secondary side of the transformer is open circuited. If the voltage on the primary side windings is given by equation 1.10 [16]:

$$v(t) = Vsin(\omega t + \Theta)\,, \tag{1.10}$$

The resulting flux in the transformer core is given by equation 1.11 were N is the number of winding turns.

$$\phi(t) = \frac{1}{N}\int Vsin(\omega t + \Theta)dt \tag{1.11}$$

The flux is proportional to the MMF in the core. The MMF is proportional to the winding current which must therefore be in phase with the flux waveform. Under steady state operation, the flux and winding current lag the voltage sinusoid by 90°. Therefore, when the voltage wave is at zero, both the flux and current will be at their negative peak. If energization of the transformer occurs when the voltage wave is at its zero crossing, the flux and current wave will proceed to increase as if they were at their negative most peak. However, at energization the flux in the transformer is zero (assuming no remnant flux) and not at its negative peak. Therefore the flux and current will rise to twice its normal peak-to-peak value before settling to its steady state value. This would be the case in an ideal transformer,

whose core does not saturate.

In a real-world transformer the core saturates well before the flux contained in its core can reach twice its normal operating value. Once saturated, large amounts of MMF are required to accomplish a small increase in flux. Therefore, the winding current will rise to as much as 8 to 10 times its rated value as the core saturates in an effort to generate enough MMF to achieve double its normal operating flux. The saturation of the transformer's core will be examined in greater detail in subsection 1.4.1.

If the transformer is energized when the voltage waveform is at its peak, the flux and current waveforms are at zero and no inrush event occurs. The current waveform at the terminals of the transformer appear as they would in steady state. The obvious solution would be to always energize a transformer when the voltage wave is at its peak. This is very difficult to accomplish in practice as remnant flux would also need to be accounted for. Inrush mitigation is an active topic of research in its own right and is outside the scope of this thesis. Currents generated during the energization of a transformer, shown in Figure 1.6, must be accounted for in any protection scheme to prevent erroneous tripping.

Remnant flux will also be considered outside the scope of this thesis. When a transformer is de-energized, the magnetic field reduces to zero. But as can be seen in Figure 1.7, a flux can exist without a magnetic field due to the hysteresis properties of magnetic materials. This limitation of scope is justified as the transformer model presented in this thesis produces inrush current of sufficient magnitude for the purpose of testing a new transformer protection algorithm. A rigorous method of modeling remnant flux, requiring a more complex model of a non-linear transformer, is given in [17].

The first five peaks of inrush current, generated by the RTDS Model are shown in Figure 1.6. This wave shape compares well with the result of a similar model given by [18] and [19]. A spectral analysis performed on Phase A of this waveform, given in Table 1.1, shows a predominant second harmonic content.

Harmonic	Magnitude (% Fund Freq)
1	100.0
2	34.7
3	5.1
4	6.3
5	2.9
6	2.3
7	1.9

Table 1.1: Harmonic content of first peak of Inrush current shown in Figure 1.6

1.4.1 Core Saturation

Under steady state conditions, the core provides a low reluctance path to magnetic flux thereby reducing magnetizing current [7]. When the core is saturated during energization, it approaches the permeability of air. The magnetizing inductance of the transformer decreases drastically as the permeability decreases, allowing a large magnetizing current to flow. This can be compactly described using the equation for inductance L, given in Equation 1.12, were N is the number of winding turns:

$$L = \frac{N^2}{\mathcal{R}} \tag{1.12}$$

Where $\mathcal{R}$ is the magnetic reluctance given by:

$$\mathcal{R} = \frac{l}{\mu A} \tag{1.13}$$

Where μ is the material's magnetic permeability which relates the flux density (B) to a magnetic field (H):

$$B = \mu H \tag{1.14}$$

Intuitively, μ is the slope of the hysteresis curve shown in Figure 1.7. As the transformer's core is driven into saturation, the hysteresis curve flattens and the magnetic permeability of the material decreases. This in turn increases the reluctance. Therefore by Equation 1.12,

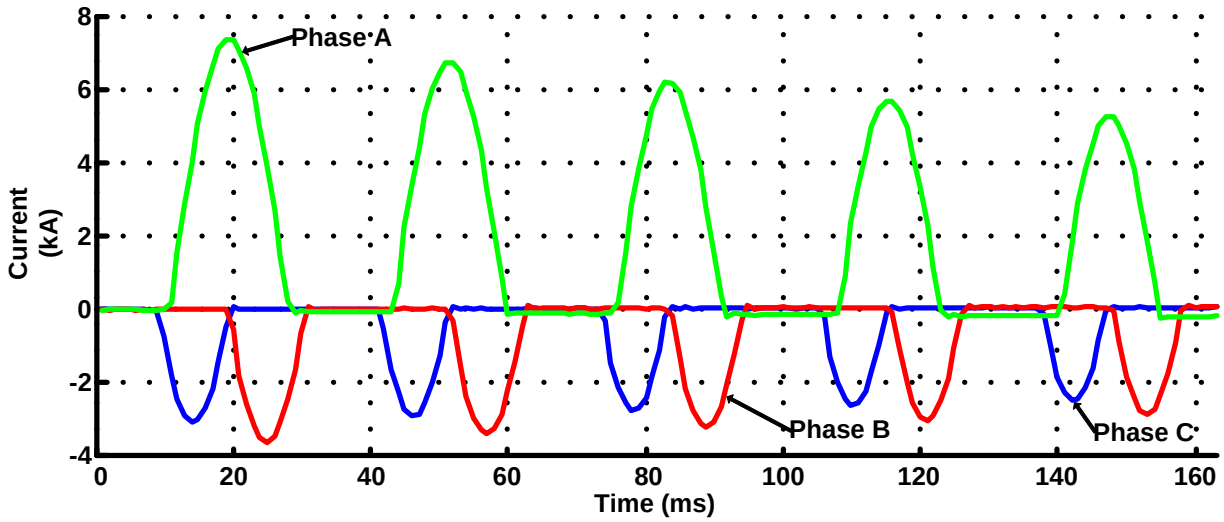

Figure 1.6: Typical Inrush Current

the magnetizing inductance will decrease when the transformer saturates. The non-linear behavior of the core makes constructing an accurate model of a three phase transformer under inrush very challenging [17]. The development of a non-linear transformer model will be further discussed in Chapter 3.

1.4.2 Magnetic Properties of a Transformer Core

The response of a magnetic material to a magnetic field can be described by a B-H curve. As this response is vital to the understanding of inrush phenomena, the B-H curve will be described in detail. Figure 1.7 shows the flux density of a magnetic material that has been exposed to a magnetic field, generated by a sinusoidal current of constant amplitude and frequency, for a long time. The residual flux density, B_r, shows the hysteresis of the material. Though the field intensity is zero, B_r is non-zero. Similarly the coercive force, H_c, is the magnetic field intensity required to reduce the magnetic flux to zero.

Energy is expended each time the hysteresis loop is traversed when driven by a sinusoidal excitation current. The hysteresis loss, W_H, that occurs over one cycle is given by Equation 1.15 for a core of volume V_c [6].

$$W_H = V_c \oint H dB \tag{1.15}$$

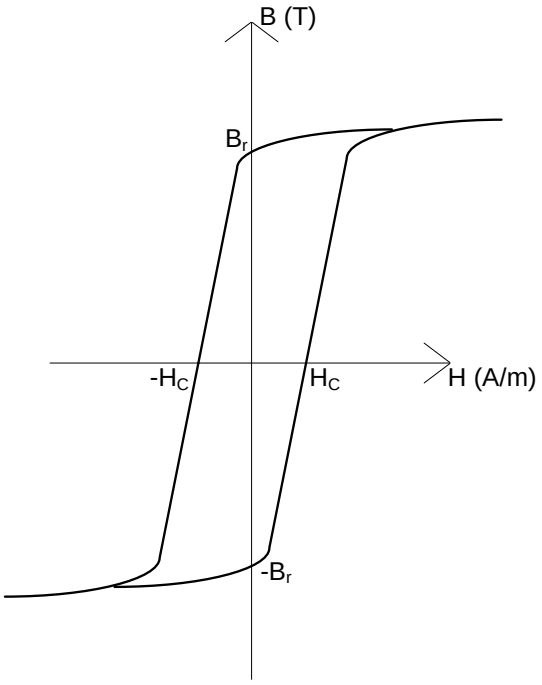

Figure 1.7: Hysteresis Loop [20]

Therefore, the area contained within the hysteresis curve is proportional to the hysteresis loss experience by a given material. The closer the core material resembles the initial saturation curve, shown in Figure 1.8, the lower it's losses. The hysteresis curve embodies two phenomena: magnetic saturation and magnetic hysteresis loss. These can be modeled as a saturating inductor and a non-linear resistor respectively [21]. The eddy current losses may be added to the hysteresis losses for a more complete representation of magnetic losses in a transformer [17]. However, saturation is the dominant non-linear magnetic effect [22], [23]. Therefore, the scope of this thesis will not include losses due to hysteresis and eddy currents in determining the shape of the inrush current wave. Transformer over-excitation is closely related to core saturation and will be discussed in Section 1.5.

1.5 Transformer Over-Excitation

Transformer core over-excitation occurs when the terminal voltage limit is exceeded or the frequency of the terminal voltage decreases below rated frequency [7]. Completing the inte-

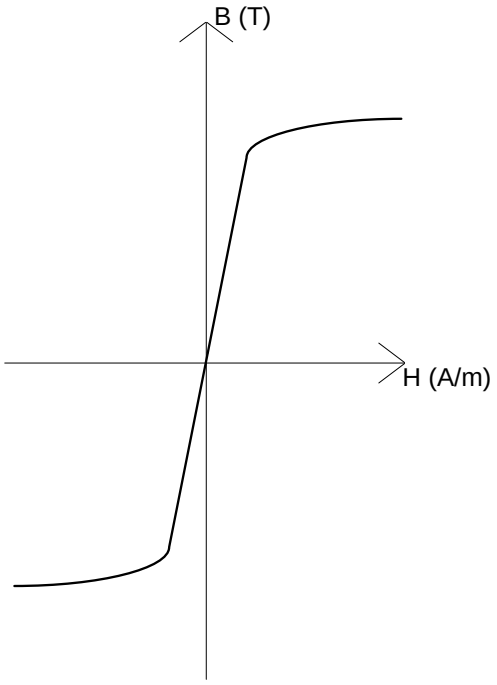

Figure 1.8: Saturation Curve

gration shown in Equation 1.11 shows this relationship mathematically as shown in Equation 1.16. Both situations increase flux in the transformer core and can cause the core to saturate. This saturation allows a large amount of current, rich in 5^{th} harmonic content, to flow. According to [24], a 5^{th} harmonic content exceeding 30% with respect to the fundamental indicates over-excitation. Harmonic analysis conducted on the transformer model over-excited with 120% of rated voltage, constructed in the real-time simulator, is given in Table 1.2. A 5^{th} harmonic content of 73.3% is a strong indication of over-excitation. Other odd harmonics, as given in Table 1.2, are also produced during transformer over-excitation. Third harmonic content is also produced by current transformer saturation due to a heavy internal fault [25] and is therefore not considered a reliable indication of over-excitation. Seventh-harmonic current content also increases during transformer over-excitation but to a lesser extent than fifth-harmonic current [26]. The wave on which the harmonic analysis was conducted is given in Figure 1.9.

$$\phi(t) = \frac{-V_M}{\omega N_P} \int cos(\omega t + \theta) dt \tag{1.16}$$

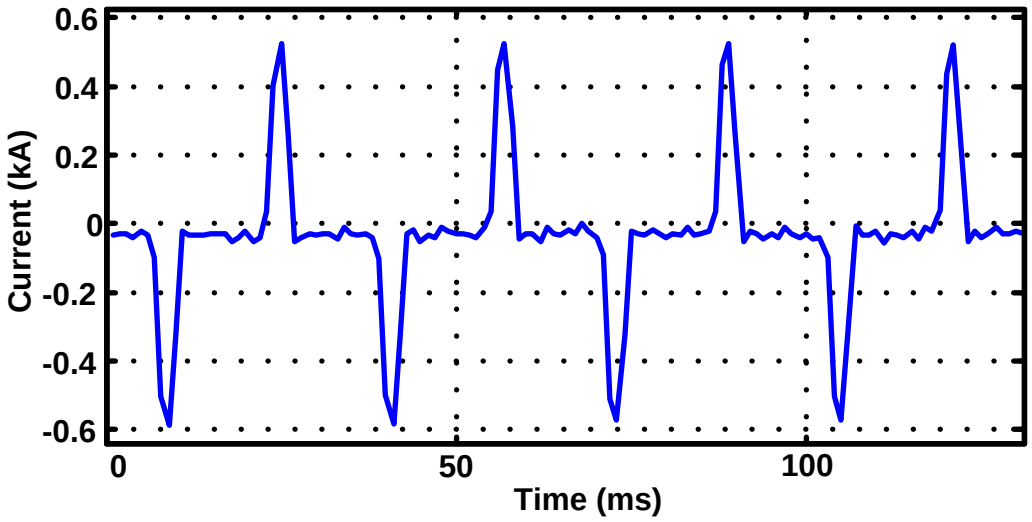

Figure 1.9: Current during 120% Over-Excitation on Primary

Over-excitation data was collected by directly sampling the current waveforms of the primary side current. The secondary terminals of the real-time transformer model were disconnected from the load in order to measure excitation current. In this configuration, the only current flowing was magnetization current. Without the inclusion of core non-linearity, the magnetization current would not change even if terminal voltage was changed.

Harmonic	**Magnitude (% Fund. Freq.)**
1	100.0
2	1.9
3	92.6
4	0.3
5	73.3
6	1.4
7	53.5

Table 1.2: Harmonic content of 120% Over-Excited Transformer

Transformer over-excitation is not a rare occurrence: 20% of generator step-up transformers in a study cited in [27] could expect an over-excitation event in a given year. Transformers are designed to continuously withstand the heating associated with an excitation voltage of

110% of it rated voltage [27], [7]. Therefore the protection system protecting the transformer must be capable of operating correctly for an over-excitation of at least 110%.

1.6 Current Methods of Turn-to-Turn Fault Protection

Though turn-to-turn faults are electrical in nature, some of the most reliable methods of detecting these faults rely on chemical or mechanical methods of detection. The following methods of turn-to-turn fault protection were drawn from [28].

1.6.1 Gas Accumulation Relays

As mentioned in Section 1.1, burning transformer oil produces gas. This gas can be collected by a gas accumulation relay. Also known as Buchholz relays, this detector is placed in the pipe between the transformer tank and the conservator tank. As gas is evolved from turn-to-turn fault, it rises through the oil in the tank and becomes trapped by the relay.

Though gas accumulation relays eventually detect turn-to-turn faults, it may take a long time to accumulate enough gas in order to issue a trip signal [4]. By the time the fault is detected, the transformer can be irreparably damaged. Transformers filled with sulfur hexafluoride (SF6) gas are of great interest in highly populated area where the fire hazard posed by oil filled transformers is too great [29]. As this type of transformer is insulated and cooled by SF6 gas, a Buchholz relay is not an option. For this type of transformer, a sudden pressure relay must suffice.

1.6.2 Sudden Pressure Relays

It is important to distinguish between a sudden change in pressure and the production of small amounts of gas. Pressure relays are meant to prevent a transformer tank rupture by detecting sudden changes in oil pressure or gas pressure. Unfortunately, any event that

causes a high current in the windings of a transformer, such as an external fault, can activate this relay. In sensitivity, the sudden pressure relay is similar to that of the differential relay as both have been observed to operate for the same types of faults [28].

1.6.3 Oil analysis

Though oil analysis is used to identify the cause of a trip, it can be used to detect small turn to turn faults before they are registered by other protection devices. Transformer oil is analyzed during routine maintenance testing. When subsequent test results are compared to a set of baseline data, the chemical signature of the thermal decomposition of insulation can be detected [30]. The transformer can then be taken out of service for repair.

1.6.4 Differential Protection

This is an electrical method of protection. If the amount of current entering the transformer differs from the amount of current leaving the transformer above a given threshold, a trip signal is issued. This method of protection is sensitive enough to detect faults involving 10% or greater turns [31]. The proposed method of turn-to-turn fault detection will be compared to differential protection. Differential current protection requires six current transformers. Three are placed on each phase of the primary side with another three current transformers placed on corresponding phases of the secondary side of the transformer. Since the differential protection scheme for each phase is identical, a single line diagram describing the differential current protection of phase A is sufficient. Note that all quantities in Figure 1.10 are magnitudes. The arrows shown in the figure indicate the direction of current flow of an unfaulted system. In this case, the difference in sensed current is below a threshold and no trip would be indicated.

A restraining current, I_r, setting is essential to the proper operation of this protection scheme. The differential current, I_d, is then compared to the restraining current. If the differential current is greater than the pick-up current, I_{pu}, and Equation 1.19 is true, a fault is signaled. K is known as the slope of the percentage differential characteristic and

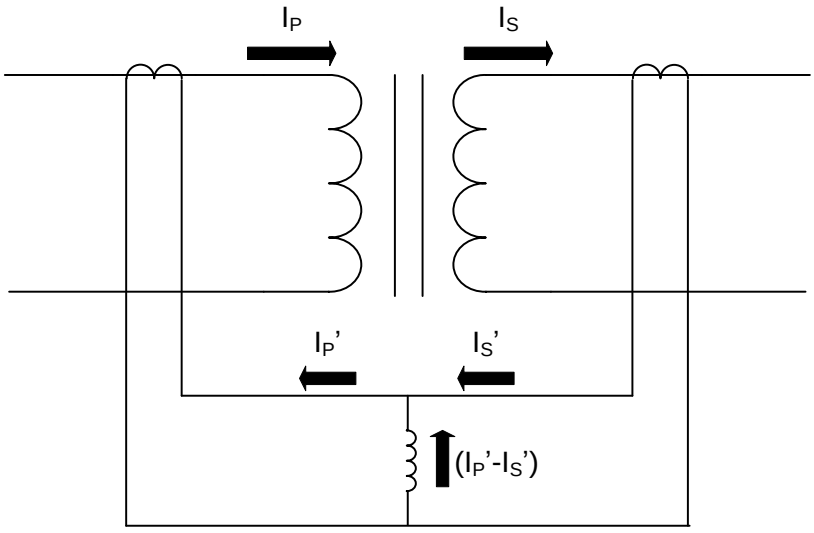

Figure 1.10: Schematic of Differential Current Protection

is expressed as a percent. Typical values are 10%, 20% and, 40%. The pickup current is typically set to 0.25A to account for CT errors at low load [32]. This relationship is shown graphically in Figure 1.11

$$I_r = \frac{I'_P + I'_S}{2} \tag{1.17}$$

$$I_d = \mid I'_P - I'_S \mid \tag{1.18}$$

$$I_d \geq K I_r \tag{1.19}$$

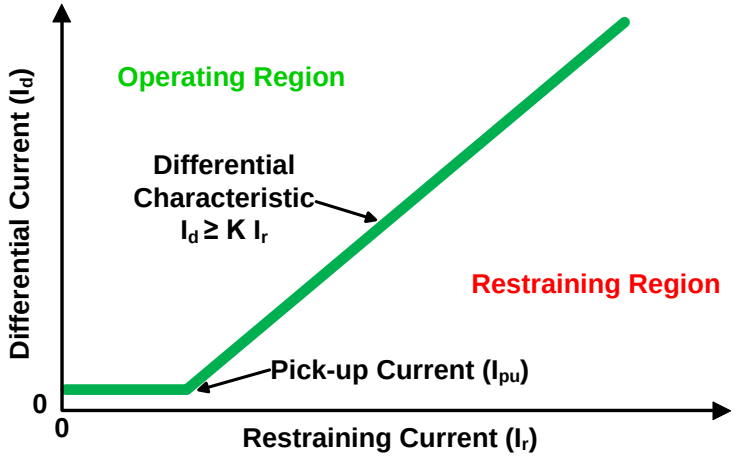

Figure 1.11: Differential Current Protection Characteristic Curve

It should be noted that no use is made of phase information in this protection scheme. Only current magnitudes are used in differential protection. As will be discussed in Section 2.3, negative sequence fault detection makes use of current magnitude and phase information.

The differential method of protection must be blocked during energization. A transformer is energized with its secondary side disconnected from the load. Since a large inrush current can be drawn on the primary side of the transformer when it is connected to its voltage source, Equation 1.19 would be satisfied. This means that without proper supervision, the differential relay would issue an erroneous trip during transformer energization. Differential transformer protection must be actively blocked during energization as the differential current resulting from inrush current would otherwise cause a false trip. As the inrush current is rich in second harmonics, the following method of blocking is recommended for differential protection [32]:

$$\left| \frac{I_{Second\ Harmonic}}{I_{Fundamental}} \right| \times 100\% > 15\% \tag{1.20}$$

If Equation 1.20 is satisfied, the differential relay blocks as the magnitude of the second harmonic of a given phase exceeds 15% of the fundamental current magnitude. The decision to trip or block is decided on a per phase basis [28]. Each of the phases issues a trip signal, 1 to signal a trip and 0 to signal a block. These signals are combined using logical OR statements. Blocking may mask faults should they occur during energization [33], a time when the transformer is particularly vulnerable to turn-to-turn faults. Large currents flowing through the transformer windings result in large mechanical forces on the windings as discussed in Section 1.2.3. These forces strain the windings, making faults more likely. The effect of on-load tap-changers (OLTC), current transformer saturation, and overexcitation on the differential current algorithm must also be considered. An OLTC may be employed to vary the voltage on the secondary side of the transformer by approximately 10% [28]. A 10% change in voltage results in a 10% change in current. Since the voltage on the primary side of the transformer is not affected by OLTC operation, no change in primary current occurs. This current mismatch, between primary and secondary sides of the transformer, is sensed by the current differential relay. In order to prevent false tripping, the relay must be

set to ignore differential currents resulting from a 10% mismatch in current. Digital current differential relays, which monitor tap changer position, compensate for current imbalances due to tapchanger operation [28]. Other causes of current imbalances, which can not be compensated for, include current transformer saturation, magnetizing inrush current, and overexcitation. A transformer is designed to operate continuously at 10% above its rated voltage. In this overexcited state, a current imbalance appears which causes a differential current to be sensed by the current differential relay. This limits the current differential relay's sensitivity as it must be designed to ignore current imbalances due to the aforementioned causes.

Current transformer saturation may also cause a differential current to flow [28]. A fault occurring outside the transformer's zone of protection may cause a large current to flow through the transformer. For example: if the fault current, due to an external fault, results in the current transformer on the primary side of the transformer to be saturated while the secondary side current transformer is not saturated, the differential protection relay will sense a differential current. Therefore, the sensitivity of the differential current relay must be adjusted to allow for current transformer saturation.

An overexcited power transformer will also generate a differential current [28]. If the voltage applied to the primary terminals of the transformer exceeds its rated voltage, a large current will flow to ground. This current does not appear on the secondary side of the transformer. The differential relay must not trip due to transformer over-excitation. This situation must also be accounted for in determining the differential relay's sensitivity.

1.6.5 Commercially Available Transformer Protection Relays with Negative Sequence Current Based Elements

Negative sequence current protection is in use in commercially available transformer protection relays such as the SEL-487E, manufactured by Schweitzer Engineering laboratories. This applies the differential algorithm, as outlined in Section 1.6.4, but with negative sequence current magnitudes [34]. The negative sequence current phase information is not

utilized in the SEL-487E's protection algorithm. The algorithm is sensitive enough to detect faults involving 2% of the transformer's windings. However, during inrush conditions, this relay blocks the negative sequence current differential element. Therefore the SEL-487E will not detect turn-to-turn faults that occur during transformer energization.

The RET650, which is manufactured by ABB[1], makes use of the primary and secondary negative sequence currents along with their phase difference [35]. This algorithm is described in Section 2.3. Figure 1.12 describes this algorithm visually. Both primary and secondary negative sequence currents magnitudes must be larger than I_{Min} in order for a phase comparison to occur. If either or both negative sequence currents is less than I_{Min}, a phase of 120° is mapped. This ensures no trip signal is issued if the negative sequence current is too small to obtain an accurate phase angle. If the negative sequence currents magnitudes are larger than I_{Min}, the phase difference between the primary and secondary negative sequence currents is examined. This phase difference must fall within the region described by the Relay Operating Angle (ROA).

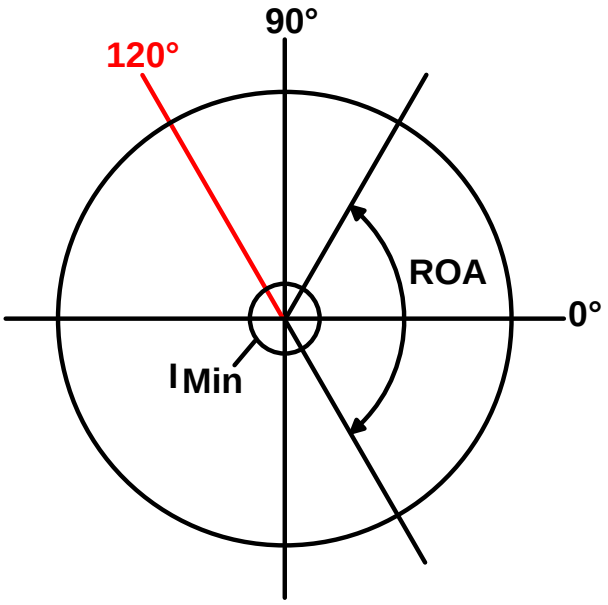

Figure 1.12: Negative Sequence Current Fault Detection

[1]ABB Group is a corporation based in Zurich, Switzerland

1.7 Literature Review

Several methods of turn-to-turn fault protection proposed in literature were examined. Each method will be summarized and a brief analysis given.

As was discussed in Section 1.3, the likelihood of a turn-to-turn fault is determined by a transformer's insulation. And while extremely serious and damaging, turn-to-turn faults are a rare occurrence [9] which are closely related to the stresses a transformer has suffered over its lifetime. Therefore fault prediction, by careful monitoring of a transformer's stresses as suggested in [10], would be an effective way of preventing turn-to-turn faults. The transformer would then be taken out of service prior to the likely occurrence of a turn-to-turn fault. This monitoring method would also reduce the amount of unscheduled down-time as a transformer likely to suffer a turn-to-turn fault could be replaced during a regularly scheduled maintenance shutdown. While this monitoring method may be particularly attractive from a risk management point of view, it does suffer from a major drawback. This type of relay must be installed when the transformer is first brought into service as thermal damage is cumulative. Therefore a larger number of older transformers, though most likely to be afflicted with insulation malfunctions, could not be protected due to lack of data.

The monitoring of insulation health by observing the transient behavior of the primary current was outlined in [36]. A discrete wavelet transform (DWT) was used to analyze the primary current of a single phase transformer under test. DWT analysis involves the successive high-pass and low-pass filtration of the incoming signal, followed by down-sampling. Each stage of filtration results in two sets of data: the detail set and the approximation set resulting from the high-pass filtration and low-pass filtration respectively. For this experiment, four detail data sets were generated ranging from 120 Hz to 240 Hz, 240 Hz to 480 Hz, 480 Hz to 960 Hz, and 960 Hz to 1920 Hz.

Data for analysis was collected from a specially constructed transformer which had been stressed to the point of failure over a period of months. It was observed that prior to failure randomly occurring current spikes appeared in all four of the detailed frequency ranges. Though this method has the advantage of providing early warning of failure, it's criteria

for signaling impending insulation failure depends on the appearance of a random series of current spikes whose characteristics are not well described. Furthermore, more study is required as to how the observed pattern of current spikes may vary with transformer size, voltage and winding configuration.

Huang et al. [37] proposed a method of identifying small changes in currents resulting from a turn-to-turn fault during transformer no-load energization. In order to accomplish this, the Jiles-Atherton parameters, used to model the non-linear magnetic core, are estimated from the transformer's phase current. These parameters are then compared to parameters collected from the same transformer in its normal state. This comparison is performed by a correlation performed over ten cycles or 167 ms for a 60 Hz signal.

When a turn-to-turn fault occurs, the transformer's electrical characteristics change. This change will cause a lack of correlation with the parameter collected from the normal transformer. The effectiveness of this algorithm depends on the accuracy of the Jiles-Atherton model over a wide range of normal transformer operating conditions. Furthermore, [37] outlines parameter estimation for a single phase transformer. Jiles-Atherton parameter estimation becomes extremely complex for a three-phase transformer with common core [17].

A method of turn-to-turn fault detection, based on zero sequence currents, is proposed in [33]. A model of a faulted Delta-Wye transformer is derived in which the voltage across the faulted turns is calculated. Should a fault occur, a sinusoidal voltage signal is calculated based on several input parameters: total leakage inductance, total winding resistance, zero sequence current and zero sequence voltage and the turn ratio. For a more precise indication it is suggested that a current transformer be placed on the Wye's grounding path in order to measure zero sequence current directly. Another current transformer would be used to measure the current circulating in the Delta.

This method's advantage is that it could detect faults during energization when the transformer is particularly vulnerable to developing turn-to-turn faults. There are however drawbacks to this method. Unless this method is applied to a transformer bank, it is difficult to measure the current circulating in the Delta. Also, an external fault generating zero

sequence current would be indistinguishable from a turn-to-turn fault. Since the occurrence of a turn-to-turn fault is rare, a complex blocking scheme would need to be developed.

Reference [38] proposes a method of turn-to-turn fault detection based on calculating the magnitude of the Extended Park's Vector (EPV) for the DC, fundamental frequency, and second harmonic. The ratio of the EPV magnitude at fundamental frequency over the DC EPV magnitude acts as the blocking quantity. EPV magnitude at the second harmonic over the DC EPV magnitude acts as the tripping quantity. The differential current is inserted into the Extended Park's Vector equation. In other words, the primary and secondary current present in each phase of the transformer are subtracted and processed in the EPV equation.

The major draw-back of this algorithm was that inrush current affected the response time of the algorithm. It is assumed in [38] that inrush current decays in approximately seven (50 Hz) cycles. As can be seen in Figure 1.6, inrush current can last for several seconds. This means that the EPV based algorithm would be delayed by several seconds. This is an unacceptable delay according to [2] and [33].

Reference [39] proposed a method of modeling a transformer, using only its name-plate data and estimating the expected line voltages based on measured line currents, based on a simple linear transformer model. These calculated line voltage values were then compared to the measured line voltage values. Large currents associated with inrush would cause a mismatch between the measured line voltages and the predicted line voltages as inrush would not be taken into account by the linear transformer model. Due to the nature of inrush current, this mismatch would only exist for part of the fundamental cycle. As can be seen in Figure 1.6, inrush current is zero for part of the fundamental cycle.

This is not the case for an internal fault. In this case, the mismatch between estimated and measured line current is always present. However, a mismatch between mode estimated and measured line voltages may also be the result of an aging transformer. Over time, a transformer's nameplate information will change with age. This change is significant enough to be noticeable at the transformer's terminals [40]. Therefore, the cost of transformer testing is a significant consideration in the implementation of this relay.

The existing algorithm, proposed in [4], could be applied in conjunction with an inrush mitigation scheme. According to [41], energizing the transformer into a large resistive load significantly reduces the peak inrush current. Therefore, a 100MW transformer would require a 100MW load with power factor of unity. The use of large braking resistors in order to improve system stability is not without precedent in power systems. [42] describes the use of three 200MW braking resistor banks in order to stabilize a transmission system under fault. When a fault is detected, the braking resistors are brought online. This type of braking resistor could be applied for inrush mitigation purposes, allowing current to flow on the secondary side of the transformer during energization. Since non-zero currents would be present on both the primary and secondary side of the transformer, the algorithm proposed in [4] would still be able to generate a trip signal. While a braking resistor may offer a theoretically simple solution, it is not the most cost effective solution. The purchase, installation and maintenance of a 100MW braking resistor bank would be large. In addition, a switching system would be required in order to switch from the braking resistor to the load. This scheme was tested using a transformer simulation with a YY winding arrangement and detected faults involving more than 3% of windings. Though these results are promising, this scheme will not be considered further due its high cost.

Babiy [31] explores the sensitivity of the algorithm proposed in [4]. A negative sequence current based relay algorithm was implemented on PSCAD® / EMTDC™ [2] along with a transformer model capable of simulating turn-to-turn faults. This model allowed for the sensitivity of the negative sequence current algorithm to be tested over a range of turn-to-turn faults, for faults with non-zero resistance, and current transformer saturation. Upon analysis of the algorithm tested in [31], it was revealed that it could not detect turn-to-turn faults occurring during a transformer's energization.

Reference [24] proposes a 12-criteria Fuzzy Logic Protective Relay for detecting turn-to-turn faults. Criteria are required to ensure the relay does not issue a false trip signal under conditions that may exist in a field installed transformer. The following situations were considered: transformer energization, over excitation, external fault coupled with cur-

[2] PSCAD®/EMTDC™ is a Trademark of Manitoba HVDC Research Center

rent transformer saturation, and ill-matched current transformer ratios. Twelve criteria were used to distinguish a healthy transformer from one suffering a turn-to-turn fault. The assumption is made that the development of a three-phase turn-to-turn fault is nearly impossible. This algorithm requires terminal currents on both the primary and secondary side of the transformer be sensed and input to the measurement unit along with the terminal voltage on the primary side of the transformer. The output of each criteria is input to a series of weighted sums. If each of the weighted sums is above a minimum threshold, the transformer is deemed to be suffering a turn-to-turn fault and a trip signal is issued. In testing, the relay algorithm described in [24] was able to detect turn-to-turn faults involving 16% of the windings and issue a trip signal within 16 milliseconds. The complexity of the fuzzy logic approach make this protective relay difficult and costly to implement. Due to its insensitivity, this algorithm was not considered further.

Stator winding protection is described in [43]. This protection scheme made use of third-harmonic voltage in order to protect generator stator windings. The third-harmonic voltage magnitude present at the terminals of the winding's terminals was compared to the third-harmonic voltage magnitude present at the neutral grounding transformer. The presence of a fault was indicated when the difference between these two voltages became larger than a preset threshold value. This method of stator winding protection has been implemented in the SEL-300G [3]. Unlike generators, transformers do not produce third harmonic voltage during normal operation. However, the concept of using voltage differential algorithm to protect windings was extended to a negative sequence voltage based algorithm (NSVA) in this work.

1.8 Objectives of this Thesis

- Develop a negative sequence algorithm capable of detecting turn-to-turn faults during transformer energization in a fast and reliable manner. This algorithm's response must be tested to the effects of instrument transformers, over-excitation, and non-zero fault

[3] SEL® is a Trademark of Schweitzer Engineering Laboratories

resistance.

- Design and build a prototype of a negative sequence based relay for the purpose of detecting turn-to-turn faults in transformers.
- Develop a real-time digital simulator model of a transformer in order to provide realistic input to the relay under test.

1.9 Organization of the Thesis

This work consists of five chapters and one appendix. Chapter 1 reviews the theory of linear transformers. This review provides the theoretical basis for the novel method of detecting turn-to-turn faults during energization inrush. The behavior of the transformer during energization is also discussed in detail. The characteristics of a transformer's terminal currents during an over-excited state are briefly presented as well. The differential protection method as applied to power transformers is described in detail. This is necessary as the novel method proposed in this work will be compared to differential protection for speed and sensitivity. Chapter 1 also introduces the causes for the occurrence of turn-to-turn faults in power transformers. Several methods of detecting these faults, which are in current use, are examined briefly. A literature review was performed in order to gain an overview of research being conducted in the area of transformer protection. The results of this review are summarized in Chapter 1.

Chapter 2 provides a brief review of symmetrical components. The proposed turn-to-turn fault detection algorithm for transformers is then presented in detail. Example calculations are given in order to demonstrate how the proposed algorithm detects turn-to-turn faults under two situations: transformer energization and normal operation. Flow charts are also provided to demonstrate the logic of the proposed algorithm.

Chapter 3 describes the construction of the prototype as well as the real time simulator model. The modeling of turn-to-turn faults and transformer core non-linearity are discussed. The effect of current transformers, voltage transformers and capacitively coupled voltage

transformers is also included in the model. The relay prototype, consisting of an analog-to-digital conversion board and micro-controller are described in detail. The relay algorithm, executed on the micro-controller is also presented in this chapter.

Chapter 4 presents the results of the novel turn-to-turn fault detection algorithm under various conditions. Results for the differential protection algorithm are also presented to allow for comparison. The relay's measurement accuracy is also tested to ensure good quality test results.

Chapter 5 presents conclusions based on the collected data. Difficulties are highlighted and suggestions for future research are presented.

Appendix A provides the parameters used to construct the real time simulator model.

Chapter 2

The Proposed Algorithm: Improving Negative Sequence Detection

2.1 Introduction

An overview of symmetrical components will be given in this chapter. Of the three sets of symmetrical components, the negative sequence will be discussed in detail. In order compare this new method of fault detection to a currently accepted method of turn-to-turn fault detection, differential transformer protection will also be described in detail. A numerical example will be given in order to clearly demonstrate the proposed method of turn-to-turn fault protection.

2.2 Symmetrical Components

The concept of symmetrical components was first described by Charles L. Fortescue in 1913 in an effort to describe the operation of induction motors under unbalanced conditions [44]. In 1933 the technique was further refined by C.F. Wagner and R.D. Evans into the method of symmetrical components so well known today [45]. Symmetrical components are comprised of three sets: zero, positive, and negative sequence as shown in Figure 2.1 for an original phase sequence with counter-clockwise rotation. Each set is composed of three vectors, one for each phase. Within a given set, the three vectors are of the same magnitude with a phase relationship that is based only on whether it describes phases A, B, or C. The positive sequence is comprised of three vectors of equal length, separated by 120° and rotating in the

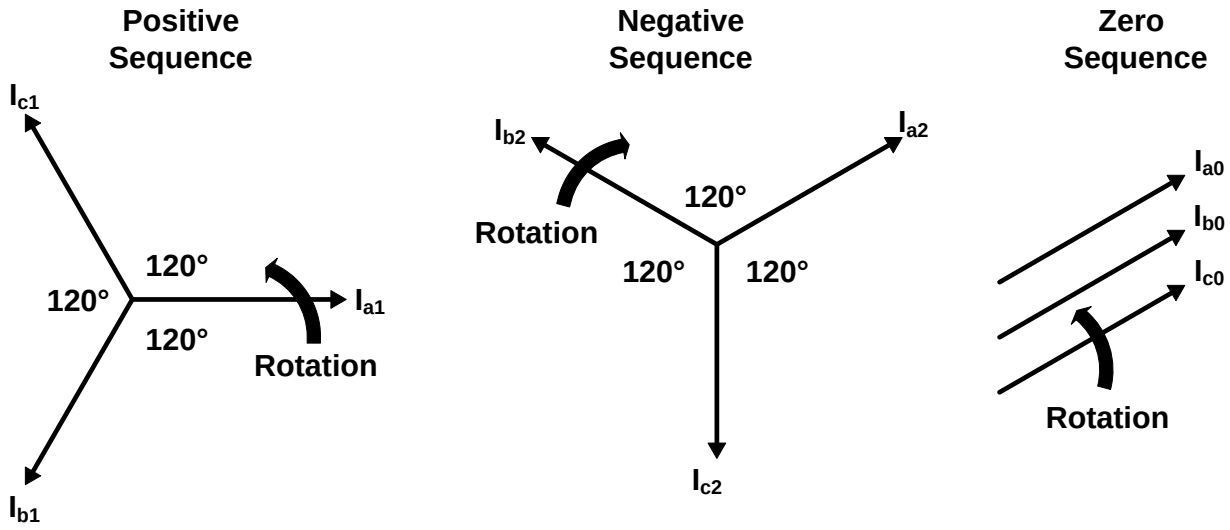

Figure 2.1: Negative Sequence Phasors

same direction as the original phase sequence. The negative sequence vectors, all of equal magnitude, are also separated by 120° but rotate in the direction opposite to the original phase sequence. All three zero sequence vectors are in phase and equal in magnitude. These relationships apply to three-phase voltages (line to neutral) and currents alike. Since the relationship between vectors within a given set are defined, the system can be completely specified by describing phase A as shown in Equation 2.1 [46]. The phase relationship between $\vec{I_a}$, $\vec{I_0}$, $\vec{I_1}$, $\vec{I_2}$ depends on the magnitudes of $\vec{I_a}$, $\vec{I_b}$, $\vec{I_c}$ as shown in Equation 2.1.

$$\begin{bmatrix} \vec{I_0} \\ \vec{I_1} \\ \vec{I_2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \vec{I_a} \\ \vec{I_b} \\ \vec{I_c} \end{bmatrix} \tag{2.1}$$

Here $\vec{I_0}$, $\vec{I_1}$, $\vec{I_2}$ represent the zero, positive, and negative-sequence currents respectively. The value of symmetrical components to the field of power system protection can be intuitively recognized by studying a balanced three phase system. In such a system the following relationship holds true:

$$\vec{I_a} = \mid I \mid \measuredangle 0^\circ \tag{2.2}$$

$$\vec{I_b} = \mid I \mid \measuredangle -120^\circ \tag{2.3}$$

$$\vec{I_c} = \mid I \mid \measuredangle + 120^\circ \tag{2.4}$$

If equations 2.2 to 2.4 are inserted into 2.1, all but the positive sequence component will be equal to zero. This is the key to the sensitivity of negative sequence protection. Since negative sequence current are unaffected by a balanced load, a lower detection threshold is permitted [47]. The sensitivity of negative sequence based methods of fault detection will be discussed in greater detail in Chapter 4 where experimental results are presented.

2.3 Application of Negative Sequence Current Scheme to Turn-to-Turn Fault Detection

A negative sequence current based algorithm (NSCA) for sensing turn-to-turn faults is proposed in [4]. First, the negative sequence current is calculated for both the primary side and secondary side of the transformer. This is accomplished by using Equation 2.1 and computing $\vec{I_2}$, the negative sequence current magnitude and phase, from the line current phasors. $\vec{I_0}$ and $\vec{I_1}$ are not required for this algorithm.

Two negative sequence current phasors are obtained from the above analysis. Let $\vec{I_{2P}}$ and $\vec{I_{2S}}$ denote the negative sequence current phasors calculated for the primary and secondary side of the transformer. The next step of this algorithm is to check the magnitudes of $\vec{I_{2P}}$ and $\vec{I_{2S}}$ to ensure that they are both above a minimum threshold as shown in Equations 2.5 and 2.6. This is important not only to prevent false tripping due to minor imbalances but also to ensure that the phase angle of the negative sequence currents are reliable.

$$\mid \vec{I_{2P}} \mid > 1\% \; Primary \; Base \; Current \tag{2.5}$$

$$\mid \vec{I_{2S}} \mid > 1\% \; Secondary \; Base \; Current \tag{2.6}$$

Phases of $\vec{I_{2P}}$ and $\vec{I_{2S}}$ are compared if the magnitudes satisfy the above equations. If Equation 2.7 is also satisfied, a trip is warranted. The current transformers (CT) are arranged such that negative sequence current caused by external faults result in phase differences of 180°.

Ideally, an internal fault would result in a 0° phase difference. CT saturation is the main cause of excursions from the ideal phase difference [4], making it necessary to allow for a range of angles from 0° to 60°. This may be visualized by setting the relay operating angle (ROA) equal to 60° in Figure 1.12

$$| ARG(\vec{I}_{2S}) - ARG(\vec{I}_{2P}) | < 60° \tag{2.7}$$

2.3.1 Example of Proposed Algorithm: Fault Occuring during Steady-State Operation

A simplified turn-to-turn fault model was developed in order to give a step-by-step example of the proposed negative sequence based protection scheme. A turn-to-turn faulted transformer was modeled as a small change in leakage impedance in the faulted phase [26]. This example applied to a transformer that has suffered a turn-to-turn fault after it has been operating for a long period of time without large changes in the transformer's terminal voltages or currents. In order to simulate a turn-to-turn fault, a four winding transformer model was constructed. This transformer model allowed one winding to be shorted, simulating a turn-to-turn fault. For the purposes of this example, the leakage impedance of a faulted three-phase transformer was determined using a short-circuit test [7]. To perform this test, the circuit shown in Figure 2.2 was simulated using PSCAD®/EMTDC™. The short-circuit test simulation, performed with the primary winding shorted, yielded the following results:

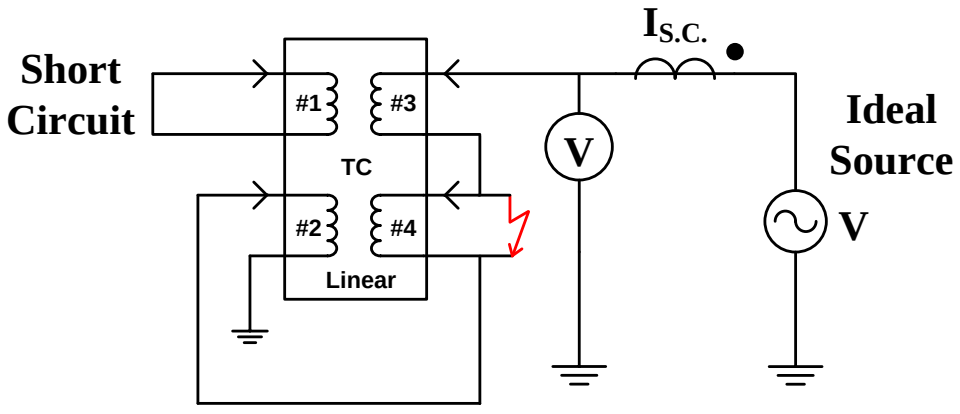

Figure 2.2: Short Circuit Test (5% Turn-to-Turn Fault)

$$X'_f = \frac{V}{I_{S.C.}} = \frac{132.79kV}{1.793kA} = j74.10\Omega \quad (5\%\, TT\ Faulted\ Phase) \tag{2.8}$$

Since the voltage source was simulated to be ideal, the voltage across the windings was equal to the source voltage. The turn-to-turn faulted transformer's short circuit reactance, X'_f, is given in Equation 2.8. This test was repeated for an unfaulted transformer yielding X'_{XFMR}:

$$X'_{XFMR} = \frac{V}{I_{S.C.}} = \frac{132.79kV}{1.660kA} = j79.99\Omega \tag{2.9}$$

Both X'_f and X'_{XFMR} must be referred to the primary side of the transformer, using the

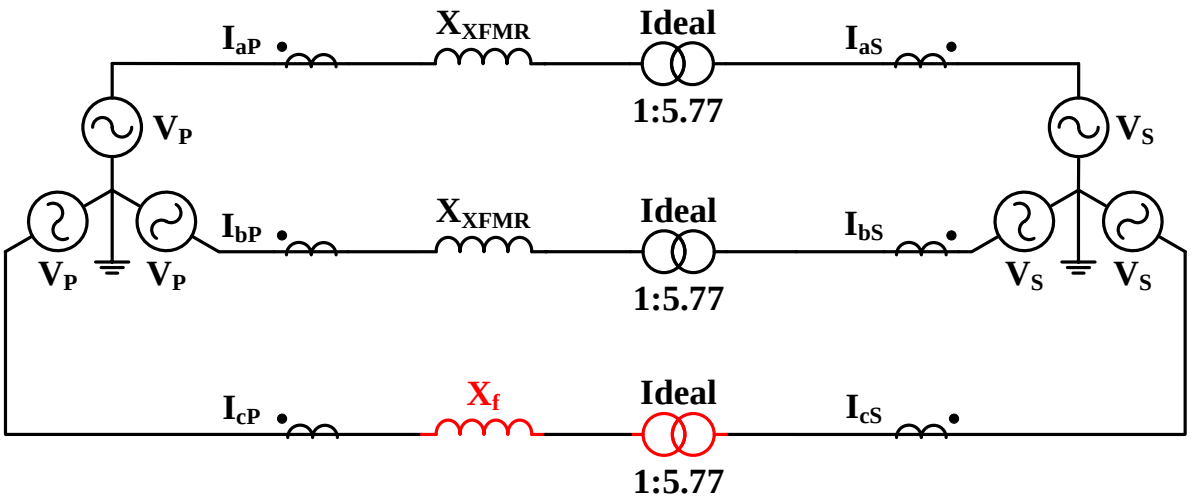

Figure 2.3: Example of Negative Sequence Current Based Protection

transformer ratio, a_{XFMR}. The same ratio is used for both faulted and unfaulted phases. The sources shown in Figure 2.3, V_P and V_S, are non-ideal sources with a positive sequence impedance of $1.6\angle 80°\,\Omega$ and $52.9\angle 80°\,\Omega$ respectively. The source elements are described in greater detail in Section 3.2.9. In order for a current to flow, V_P leads V_S by 18.5° as shown in Equation 2.10. Both primary and secondary circuit breakers are closed as shown in Figure 2.3. Due to the phase difference between sources V_P and V_S, current flows toward the secondary source simulating a load. The three-phase voltages for the primary and secondary sources are given in Equation 2.10. Equations 2.11 and 2.12 represent the primary and secondary source impedances. Transformer impedances, found using the short-circuit test simulation circuit in PSCAD/EMTDC, are referred to the primary side in Equations 2.14

and 2.15. These impedances are inserted into a matrix, Equation 2.16, representing a three-phase transformer undergoing a turn-to-turn fault. The currents in each phase may be found using Equation 2.18.

$$V_{PP} = \begin{bmatrix} 39.83 \angle 18.5^\circ \, kV \\ 39.83 \angle -101.5^\circ \, kV \\ 39.83 \angle -221.5^\circ \, kV \end{bmatrix} \quad V_{SS} = \begin{bmatrix} 229.72 \angle 0^\circ \, kV \\ 229.72 \angle -120^\circ \, kV \\ 229.72 \angle -240^\circ \, kV \end{bmatrix} \tag{2.10}$$

$$X_{SourcePr} = \begin{bmatrix} 1.6 \angle 80^\circ \, \Omega & 1 & 1 \\ 1 & 1.6 \angle 80^\circ \, \Omega & 1 \\ 1 & 1 & 1.6 \angle 80^\circ \, \Omega \end{bmatrix} \tag{2.11}$$

$$X_{SourceSec} = \begin{bmatrix} 52.9 \angle 80^\circ \, \Omega & 1 & 1 \\ 1 & 52.9 \angle 80^\circ \, \Omega & 1 \\ 1 & 1 & 52.9 \angle 80^\circ \, \Omega \end{bmatrix} \tag{2.12}$$

$$a_{XFMR} = \frac{39.83kV}{230.0kV} = 0.1734 \tag{2.13}$$

$$X_{XFMR} = X'_{XFMR} \, a^2_{XFMR} = 79.99\Omega(0.1734)^2 = j2.4051\Omega \tag{2.14}$$

$$X_f = X'_f \, a^2_{XFMR} = 74.10\Omega(0.1734)^2 = j2.2280\Omega \tag{2.15}$$

$$X_{XFMR\_P} = \begin{bmatrix} X_{XFMR} & 1 & 1 \\ 1 & X_{XFMR} & 1 \\ 1 & 1 & X_f \end{bmatrix} = \begin{bmatrix} j\,2.4051\,\Omega & 1 & 1 \\ 1 & j\,2.4051\,\Omega & 1 \\ 1 & 1 & j\,2.2280\,\Omega \end{bmatrix} \tag{2.16}$$

$$I_{Pr} = (V_{PP} - V_{SS} \, a_{XFMR})(X_{SourceSec} \, a^2_{XFMR} + X_{XFMR\_P} + X_{SourcePr})^{-1} \tag{2.17}$$

The phase currents found by Equations 2.18 and 2.19 may be used to find the negative sequence current on both the primary and secondary sides of the faulted transformer. A 5% turn-to-turn fault (fault involving 43 windings) is sustained on the secondary windings of

the transformer which is comprised of a total of 866 windings. Negative sequence current flow toward the fault, resulting in the negative sign seen in Equation 2.23. This creates the 180° phase shift seen between Equations 2.18 and 2.19.

$$I_{Pr} = \begin{bmatrix} 1.3263 \measuredangle 14.9538^\circ \, kA \\ 1.3263 \measuredangle -105.0462^\circ \, kA \\ 1.3696 \measuredangle 135.1406^\circ \, kA \end{bmatrix} \tag{2.18}$$

$$I_{Sec} = -I_{Pr}\, a_{XFMR} = \begin{bmatrix} 0.22995 \measuredangle -165.0462^\circ \, kA \\ 0.22996 \measuredangle 74.9538^\circ \, kA \\ 0.23746 \measuredangle -44.8594^\circ \, kA \end{bmatrix} \tag{2.19}$$

$$\begin{bmatrix} \vec{I}_{Pr\,0} \\ \vec{I}_{Pr\,1} \\ \vec{I}_{Pr\,2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} * \begin{bmatrix} 1.3263 \measuredangle 14.9538^\circ \, kA \\ 1.3263 \measuredangle -105.0462^\circ \, kA \\ 1.3696 \measuredangle 135.1406^\circ \, kA \end{bmatrix} \tag{2.20}$$

$$\vec{I}_{Pr\,2} = 0.01451 \measuredangle -15.0174^\circ \, kA \tag{2.21}$$

$$\begin{bmatrix} \vec{I}_{Sec\,0} \\ \vec{I}_{Sec\,1} \\ \vec{I}_{Sec\,2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} * \begin{bmatrix} 0.22995 \measuredangle -165.0462^\circ \, kA \\ 0.22996 \measuredangle 74.9538^\circ \, kA \\ 0.23746 \measuredangle -44.8594^\circ \, kA \end{bmatrix} \tag{2.22}$$

$$\vec{I}_{Sec\,2} = -0.002514 \measuredangle 164.9826^\circ \, kA = 0.002514 \measuredangle -15.0174^\circ \tag{2.23}$$

Now that the negative sequence currents for the primary and secondary side of the transformer have been calculated, the negative sequence relay algorithm may be applied. First, the negative sequence current magnitudes are checked to ensure each is above the threshold. These are calculated to be 1% of the rated current for the primary and secondary side of the transformer as given in Equations 2.24 and 2.26.

$$I_{Pr\,Thres} = 0.01 \, \frac{S_B}{V_{Pr}\sqrt{3}} = 0.01 \, \frac{100\,MVA}{39.83\,kV\sqrt{3}} = 0.01450\,kA \tag{2.24}$$

$$| \, 0.01451 \measuredangle -15.0174^{\circ} \, kA \, | > 0.01450 \, kA \tag{2.25}$$

$$I_{SecThres} = 0.01 \, \frac{S_B}{V_{Sec} \sqrt{3}} = 0.01 \, \frac{100 \, MVA}{229.72 \, kV \sqrt{3}} = 0.002513 \, kA \tag{2.26}$$

$$| \, 0.002514 \measuredangle -15.0174^{\circ} \, | > 0.002513 \, kA \tag{2.27}$$

Since Equations 2.25 and 2.27 are true, the algorithm proceeds to the phase comparison. The phase comparison indicates a trip as shown in Equation 2.28. Recall that the reasoning behind the trip criteria used in Equation 2.28 was outline in Equation 2.7.

$$| \, ARG(0.002514 \measuredangle -15.0174^{\circ}) - ARG(0.01451 \measuredangle -15.0174^{\circ} \, kA) \, | = 0^{\circ} < 60^{\circ} \quad TRIP \tag{2.28}$$

2.4 Proposed Method of Detecting Turn-to-Turn Faults During Inrush

The requirement that both equations 2.5 and 2.6 be satisfied for a valid phase comparison is an inherent weakness of the algorithm proposed in [4]. Both primary and secondary negative sequence current magnitudes must be greater than the threshold described in equations 2.5 and 2.6 in order for a reliable phase comparison between primary and secondary negative sequence currents. Since no current flows in the transformer's secondary windings during energization, the negative sequence based turn-to-turn fault detection method blocks for any severity of fault. The stresses of energization make the transformer particularly vulnerable to turn-to-turn faults [33]. This deficiency of the negative sequence current algorithm will be addressed in this section.

A turn-to-turn fault not only affects the currents seen at a transformer's terminals, but also the voltages. As shown in Figure 1.5, a turn-to-turn fault changes the transformer's turns ratio as turns are bypassed by the fault. This causes a voltage imbalance amongst the phases. As discussed in Section 2.2, a non-zero negative sequence current or voltage appears

should an imbalance appear in a three-phase system. The negative sequence current method of turn-to-turn fault detection is excellent when the transformer is loaded. But as there is no load current flowing during energization, this method is blind to turn-to-turn faults.

Voltage exists on the load side of the transformer whether current is flowing or not. The terminal voltages, while affected by inrush current, quickly recover allowing for accurate voltage readings almost immediately after energization. Since the phase voltages are readily available, the negative sequence voltages for the primary and secondary side of the transformer can be accurately calculated. The algorithm for comparing these two negative sequence voltages is similar to the differential current algorithm described in Section 1.6.4. The pick-up negative sequence voltage is set to 1% of the rated phase voltage.

In order to illustrate how a voltage imbalance is detected, a single phase transformer with a turn-to-turn fault will be discussed in detail. It represents one phase of a 3-phase transformer experiencing a turn-to-turn fault. Two scenarios will be discussed: a turn-to-turn fault on the primary side or a turn-to-turn fault on the secondary side. The primary side turn-to-turn fault is shown in Figure 2.4. A small portion of the primary windings are shorted causing a small amount of additional current i_p to be drawn. This does not create a significant change in e_p since the source resistance is assumed to be low. Therefore the negative sequence voltage contributed by the primary side, given by $V_{1_{Pr}}$ in Equation 2.29, will be negligible.

$$\begin{bmatrix} \vec{V}_{0_{Pr}} \\ \vec{V}_{1_{Pr}} \\ \vec{V}_{2_{Pr}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \vec{V}_{a_{Pr}} \\ \vec{V}_{b_{Pr}} \\ \vec{V}_{c_{Pr}} \end{bmatrix} \tag{2.29}$$

As discussed in Section 1.2.1 the current traveling through the short circuit is not able to contribute to the mmf causing an effective reduction in the turns ratio: $N'_p < N_p$. Therefore the secondary side contributes a large amount of negative sequence voltage, as given by $V_{1_{Sec}}$ in Equation 2.31. The two negative sequence voltage magnitudes $V_{1_{Pr}}$ and $V_{1_{Sec}}$ are compared in a manner similar to differential current protection.

$$V'_s = \frac{N'_p}{N_s} V_p \tag{2.30}$$

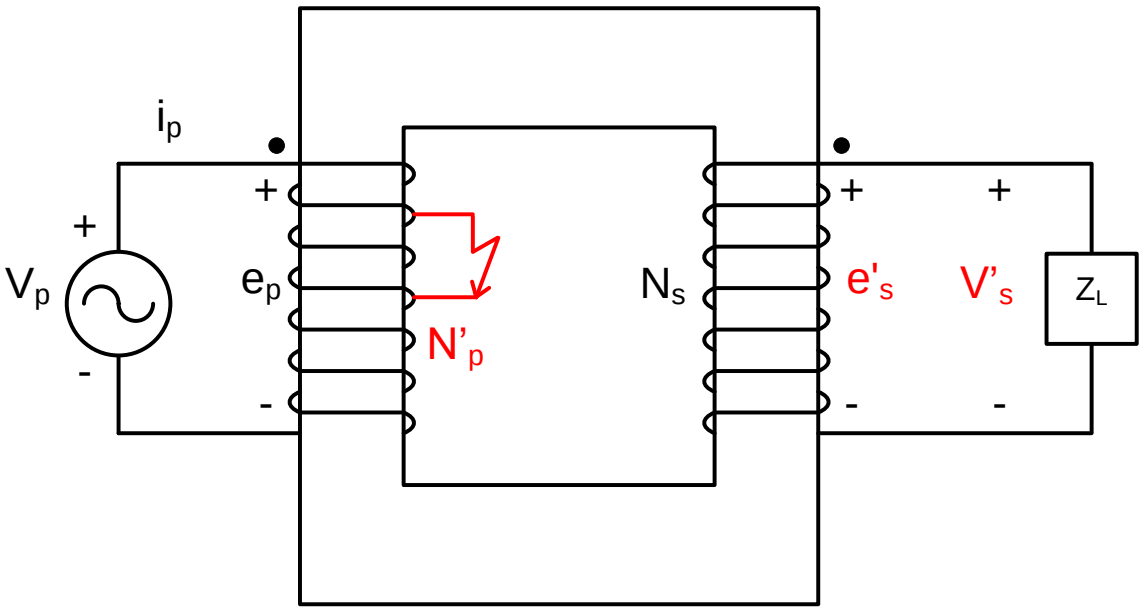

Figure 2.4: Primary Turn-to-Turn Fault, Phase C

$$\begin{bmatrix} \vec{V}_{0_{Sec}} \\ \vec{V}_{1_{Sec}} \\ \vec{V}_{2_{Sec}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \vec{V}_{a_{Sec}} \\ \vec{V}_{b_{Sec}} \\ \vec{V}'_{c_{Sec}} \end{bmatrix} \tag{2.31}$$

The secondary side turn-to-turn fault is shown in Figure 2.5. The effective reduction in the turns ratio on the secondary side causes an increase in the secondary voltage of the faulted phase since $N'_s < N_s$ as shown in Equation 2.32. Equation 2.31 will yield a non-zero negative sequence voltage as an imbalance in voltage amongst phases is present. A fault on the primary side causes a decrease in secondary phase voltage while a fault on the secondary side causes an increase in phase voltage. Both scenarios caused an imbalance with respect to other phase voltages, resulting in negative sequence voltage. An example of this method is provided in the next subsection in order to clarify this method.

$$V'_s = \frac{N_p}{N'_s} V_p \tag{2.32}$$

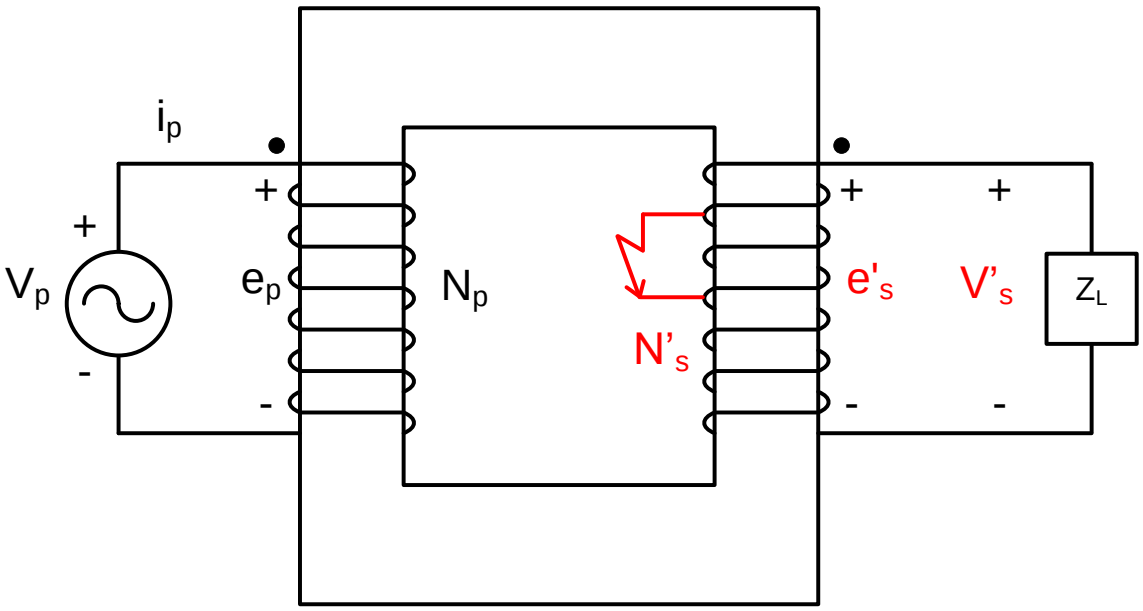

Figure 2.5: Primary Turn-to-Turn Fault, Phase C

2.4.1 Example of Proposed Algorithm: Fault Occuring during Transformer Energization

The following numerical example examines a system that is in an energization configuration with the secondary open circuited. The simple example does not address the presence of inrush current during energization and is meant to demonstrate the affect of a turn-to-turn fault on the a three-phase transformer's primary and secondary voltage. The model, shown in Figure 2.6, is used to simulate a transformer suffering a 5% turn-to-turn fault while the secondary breakers are open in an enegization configuration. Phase-to-neutral voltages, given in Equation 2.33 were found using a short-circuit test simulation circuit in PSCAD/EMTDC.

$$V_{Pf} = \begin{bmatrix} 22.9929 \angle 0° \, kV \\ 22.9929 \angle -120° \, kV \\ 21.8218 \angle -240° \, kV \end{bmatrix} \quad V_{Sf} = \begin{bmatrix} 132.715 \angle 0° \, kV \\ 132.715 \angle -120° \, kV \\ 116.346 \angle -240° \, kV \end{bmatrix} \tag{2.33}$$

The negative sequence is computed on both the primary and secondary sides of the transformer voltages collected from the PSCAD model. Only the magnitude of the negative sequence voltage is of interest in this portion of the algorithm. The transformer ratio must

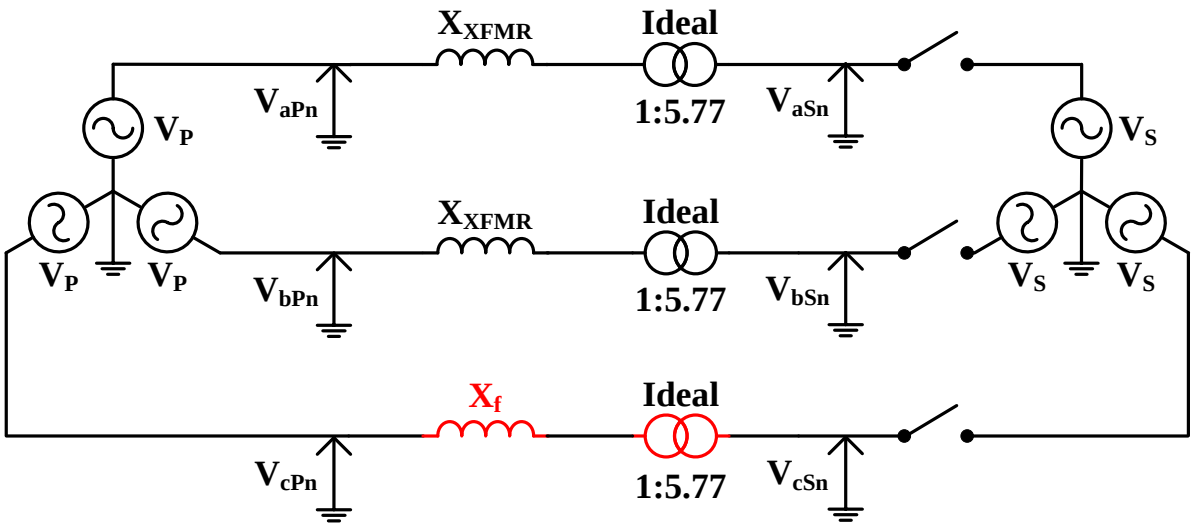

Figure 2.6: Example of Negative Sequence Voltage Protection

be applied to Equation 2.36 so that the secondary side negative sequence voltage can be compared to the primary negative sequence voltage found using Equation 2.34.

$$\begin{bmatrix} \vec{V}_{Pr\,0} \\ \vec{V}_{Pr\,1} \\ \vec{V}_{Pr\,2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} * \begin{bmatrix} 22.9929\angle 0°\,kV \\ 22.9929\angle -120°\,kV \\ 21.8218\angle -240°\,kV \end{bmatrix} \tag{2.34}$$

$$\vec{V}_{Pr\,2} = 0.390\angle -78.50°\,kV \tag{2.35}$$

$$\begin{bmatrix} \vec{V}_{Sec\,0} \\ \vec{V}_{Sec\,1} \\ \vec{V}_{Sec\,2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} * \begin{bmatrix} 132.715\angle 0°\,kV \\ 132.715\angle -120°\,kV \\ 116.346\angle -240°\,kV \end{bmatrix} * \frac{22.99kV}{132.79kV} \tag{2.36}$$

$$\vec{V}_{Sec\,2} = 0.946\angle -60.00°\,kV \tag{2.37}$$

$$|\,\vec{V}_{Pr\,2}\,| = 0.390\,kV \qquad |\,\vec{V}_{Sec\,2}\,| = 0.946\,kV \tag{2.38}$$

Once the primary and secondary negative sequence voltages have been found, the relay algorithm is implemented. The restraining negative-sequence voltage is found in Equation 2.39

along with the differential negative-sequence voltage given in Equation 2.40. This voltage is must be larger than the pick-up voltage in order to prevent false trips due to small voltage imbalance. In this example, the differential voltage is larger than the pick-up level, as shown in Equation 2.41. The differential and restraining negative sequence voltage must be compared as shown in Equations 2.43. This comparison indicates that a fault has occured and a trip signal is issued.

$$V_r = \frac{|\,\vec{V}'_{Pr\,2}\,| + |\,\vec{V}'_{Sec\,2}\,|}{2} = \frac{0.390\,kV + 0.946\,kV}{2} = 0.668\,kV \tag{2.39}$$

$$V_d = |\,V'_P - V'_S\,| = |\,0.390\,kV - 0.946\,kV\,| = 0.556\,kV \tag{2.40}$$

$$0.556\,kV \geq 1\% V_{Sec} = 0.01 * 22.9929kV = 0.230\,kV \tag{2.41}$$

$$V_d \geq KV_r \quad K = 0.2 \tag{2.42}$$

$$0.556\,kV \geq 0.2 * 0.668\,kV = 0.134\,kV \quad TRIP \tag{2.43}$$

This method of fault detection was found to accurately detect turn-to-turn faults during energization while rejecting line-to-ground, line-to-line, and line-to-line-to-ground faults that occurred external to the transformer's zone of protection. When combined with the algorithm described in Section 2.3, a comprehensive negative sequence turn-to-turn fault protection algorithm is constructed that is valid from the moment the transformer is energized.

The use of negative sequence voltages in place of negative sequence currents, to protect the transformer at all times not just during inrush was also examined. The negative sequence magnitudes of both voltage and current certainly exhibited similar reaction to the presence of a fault. But the phases were a different matter.

Negative sequence currents present on the primary and secondary side of the transformer can be said to flow toward a fault [45]. Therefore, the negative sequence phase difference will ideally sum to 0° for an external fault and 180° for a turn-to-turn fault. Such a relationship

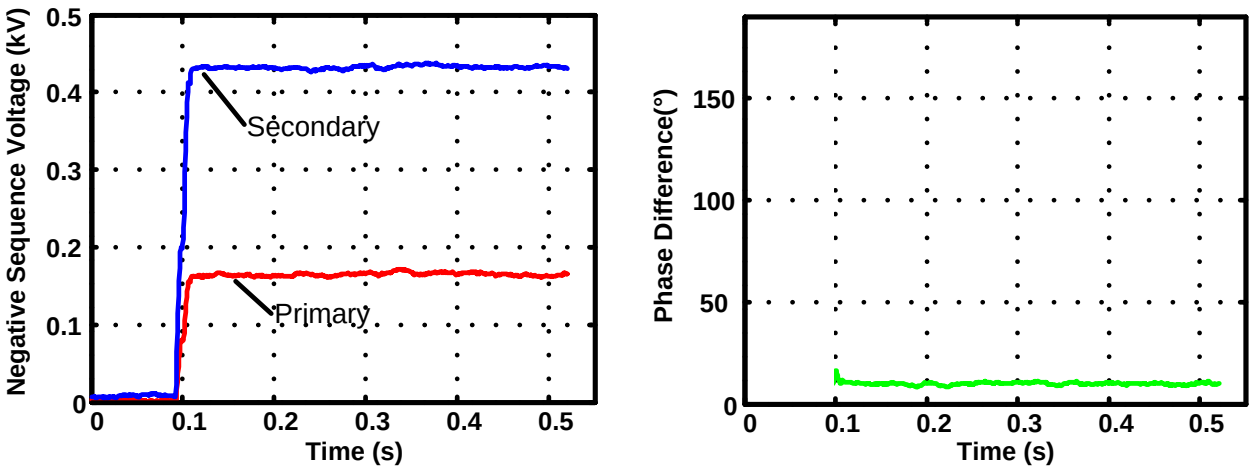

Figure 2.7: 25% Turn-to-Turn Fault Negative Sequence Voltage

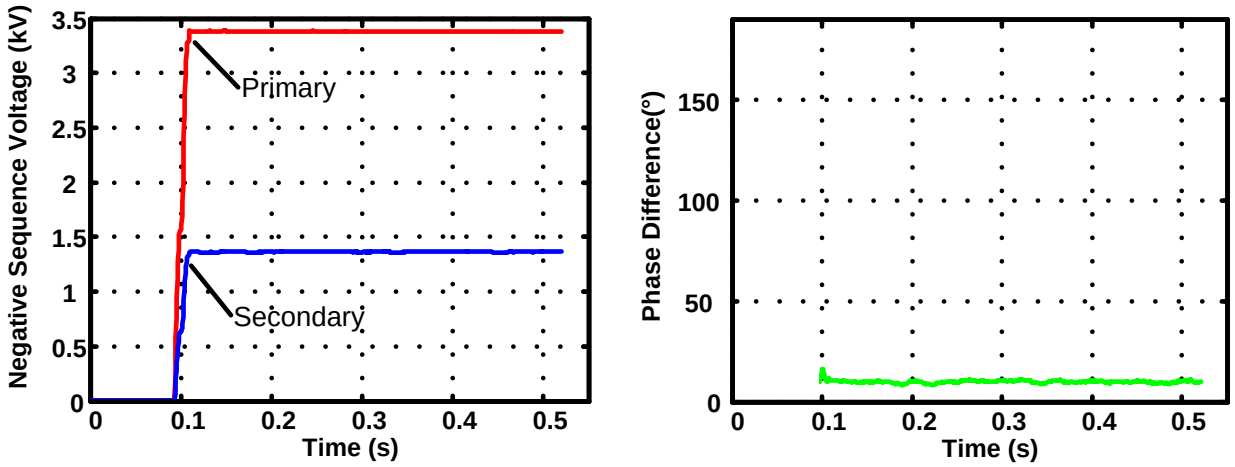

Figure 2.8: External Fault Negative Sequence Voltage

does not exist between negative sequence voltages present on the primary and secondary side of the transformer. A 25% turn-to-turn fault is shown in Figure 2.7 while an external fault is shown in Figure 2.8. Both types of fault occurred in a system which were previously in a steady-state condition. The phase difference did not change significantly from turn-to-turn fault to external fault. Therefore a hybrid algorithm, using negative sequence voltage during energization of the transformer and negative sequence current at all other times, is the optimal solution. The proposed hybrid solution of combining negative sequence current and negative sequence voltage is described in subsection 2.4.2

2.4.2 The Proposed Negative Sequence Algorithm

The novel algorithm proposed in this thesis will be summarized in this subsection. Negative sequence current, existing on the primary and secondary side of the transformer is considered first, as shown in Figure 2.9. If the negative sequence current magnitude, detected on both primary and secondary sides of the transformer, is above the prescribed threshold, a phase comparison is warranted. If negative sequence current exists only on the primary side of the transformer but not on secondary side, the primary side of the transformer is being energized. In this case the algorithm proceeds to the negative sequence voltage algorithm. An energization on the secondary side of the transformer also results in the selection of the negative sequence voltage algorithm shown in Figure 2.10.

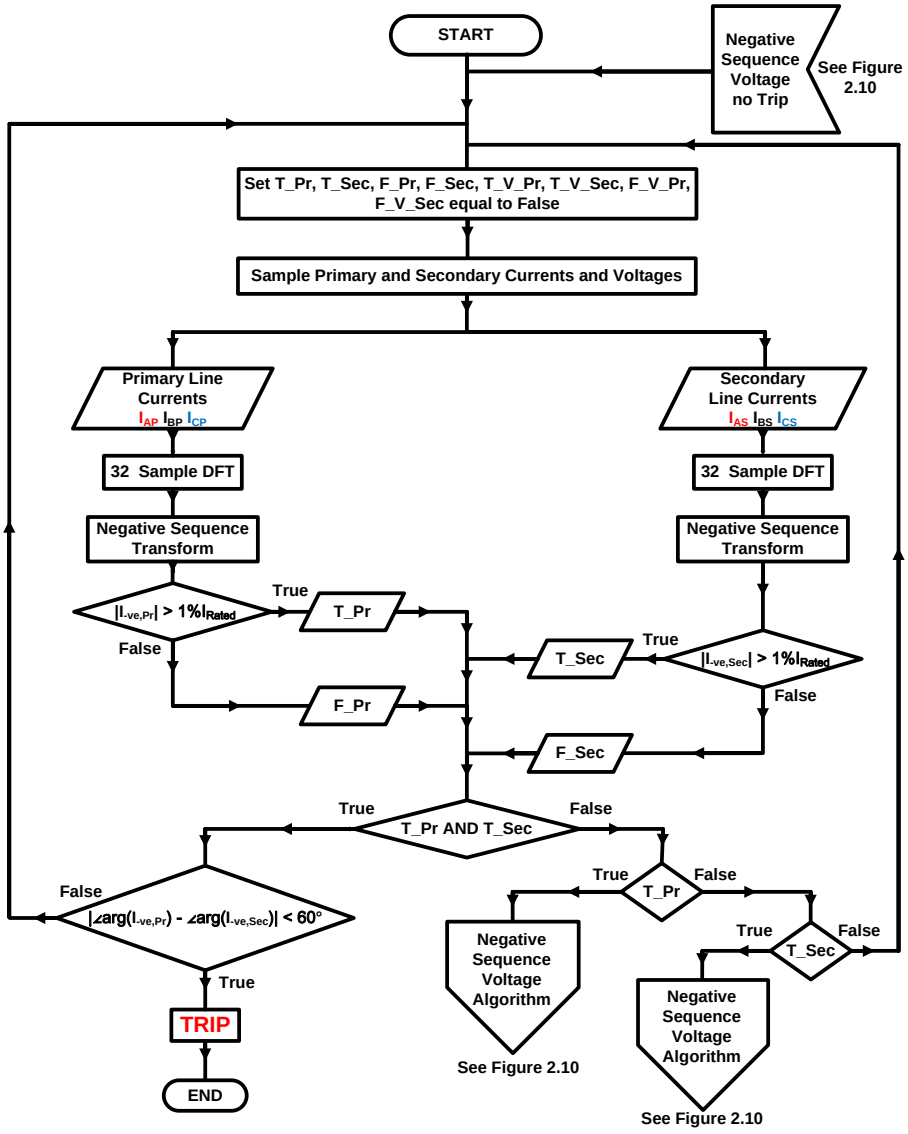

Figure 2.9: Proposed Algorithm: Negative Sequence Current

The negative sequence voltage algorithm takes as input the primary and secondary phase voltages. Only the magnitude of the primary and secondary negative sequence voltage is of interest in this case. Notice that the secondary negative sequence voltage is transformed to the primary side of the transformer. Both the primary negative sequence voltage and the secondary negative sequence voltage, transformed to the primary side of the transformer, must be larger than 1% of the rated primary voltage. This prevents erroneous tripping due to small imbalances found in an unfaulted transformer. The restraining and differential

voltages are calculated as shown in Equations 2.39 to 2.43. If the differential voltage exceeds the restraining voltage equation, a trip is warranted. The algorithm shown in Figure 2.10 is only executed under certain conditions outlined in Figure 2.9. In other words, when the transformer's negative sequence currents indicate that the transformer is being energized, negative sequence voltages are used to determine if the transformer is experiencing a turn-to-turn fault.

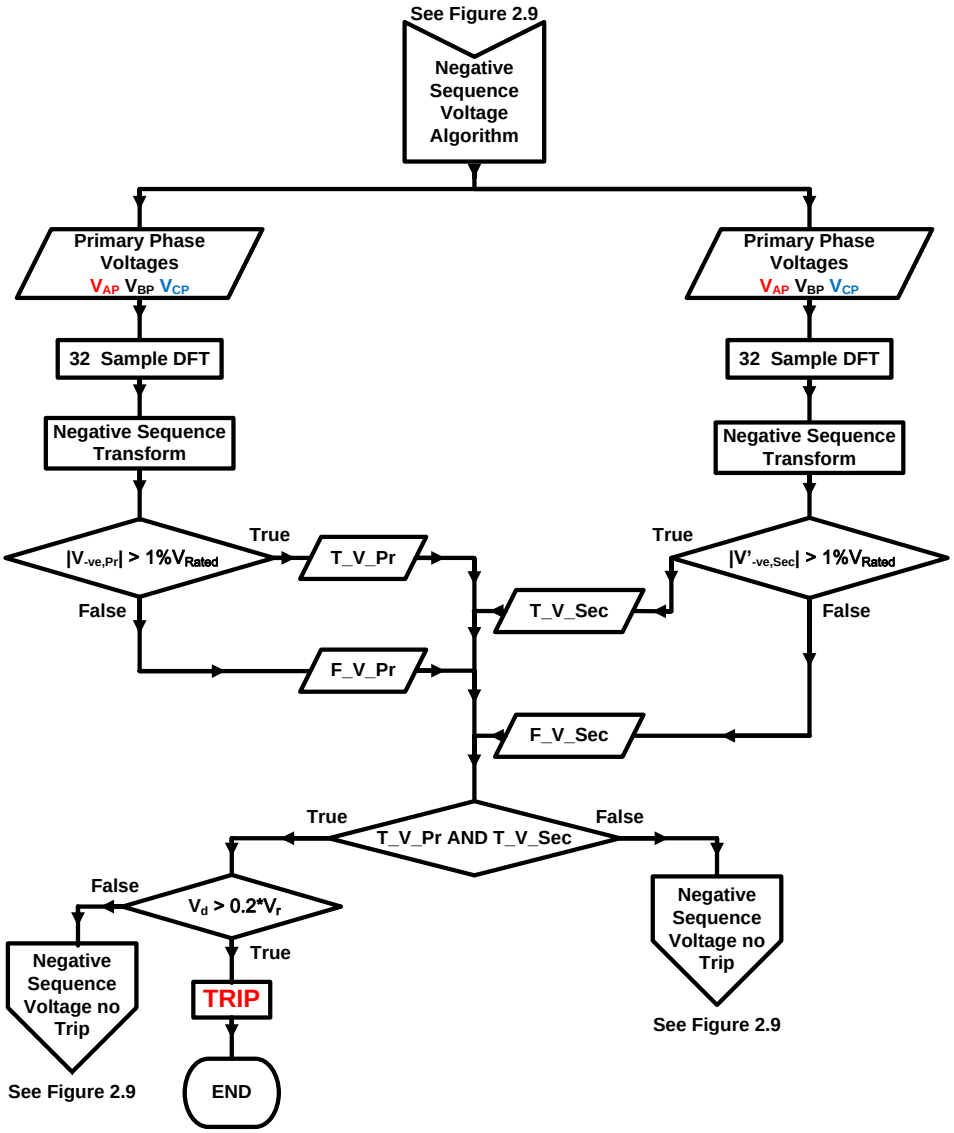

Figure 2.10: Proposed Algorithm: Negative Sequence Voltage Algorithm

Voltage changes due to on-load tap changer (OLTC) operations are not a concern as the

negative sequence voltage algorithm is only on-line during transformer energization. OLTC is common on many modern transformers and are used to compensate for voltage drops due to current flowing in a line supplying a load some distance away from the transformer [46]. However, during energization, the transformer's secondary is open and no current is flowing to the load. Therefore, no OLTC operation will occur.

IEEE standard [48] requires that the transformer winding voltages, at no load, be within 0.5% of the nameplate voltage. If a 0.5% imbalance is introduced to the otherwise healthy system described in Subsection 2.4.1, it produces a negative sequence voltage well below the threshold. A 1% imbalance in phase voltage shown in Equation 2.44. The resulting negative sequence voltage 0.077 kV is much less than the threshold negative sequence voltage of 0.230 kV found in Equation 2.41.

$$\begin{bmatrix} \vec{V}_{Sec\,0} \\ \vec{V}_{Sec\,1} \\ \vec{V}_{Sec\,2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} * \begin{bmatrix} 132.715 \angle 0^\circ\, kV \\ 132.715 \angle -120^\circ\, kV \\ 1.01 * 132.715 \angle -240^\circ\, kV \end{bmatrix} * \frac{22.99kV}{132.79kV} \tag{2.44}$$

$$\vec{V}_{Sec\,2} = 0.077 \angle 120^\circ\, kV \tag{2.45}$$

$$\mid \vec{V}_{Sec\,2} \mid = 0.077\, kV \tag{2.46}$$

2.5 Summary

Symmetrical components were briefly reviewed in this chapter. A numerical example of the proposed algorithm was presented in order to demonstrate the operation of the proposed algorithm during energization and normal operation. These examples showed how the proposed algorithm made use of negative sequence voltages and currents to protect the transformer. Commercially available relays that make use symmetrical components were briefly discussed. Flow charts of the proposed algorithm were given in order to demonstrate how the proposed algorithm would function to protect a transformer.

Chapter 3

Construction of a Relay Prototype

3.1 Introduction

A prototype was constructed in order to test the novel method of turn-to-turn fault detection, valid during energization, proposed in Section 2.4. In order to obtain current and voltage signals that can be processed by the prototype, a model of a three phase transformer was constructed using an RTDS™ [1]/RSCAD[2] Real Time Digital Simulator (RTDS) developed by RTDS Technologies [49]. These signals are then fed to the prototype which consists of an Analog to Digital Conversion (ADC) board and a Microchip micro-processor. In this chapter, the RTDS model, the ADC board, and the microprocessor will be discussed in detail. These three components are vital to the testing of a realistic relay prototype as shown in Figure 3.1.

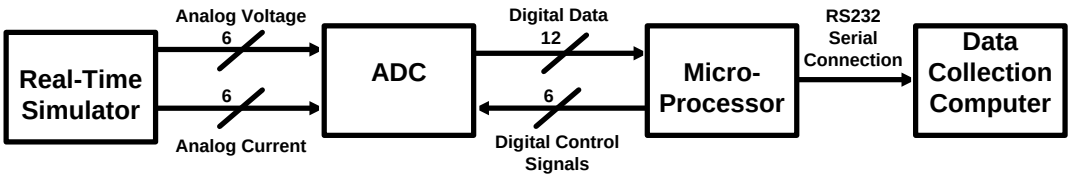

Figure 3.1: Overall Schematic of Prototyping Setup

3.2 The RTDS Transformer Model

A schematic of the entire RTDS model is given in Figure 3.2. The function of each component and their relationship will be discussed throughout this chapter. A transformer model with

[1]RTDS™ is a Trademark of RTDS Technologies Inc., Manitoba Canada

[2]RSCAD is a user interface, created by RTDS Technologies Inc., used to design models for the RTDS

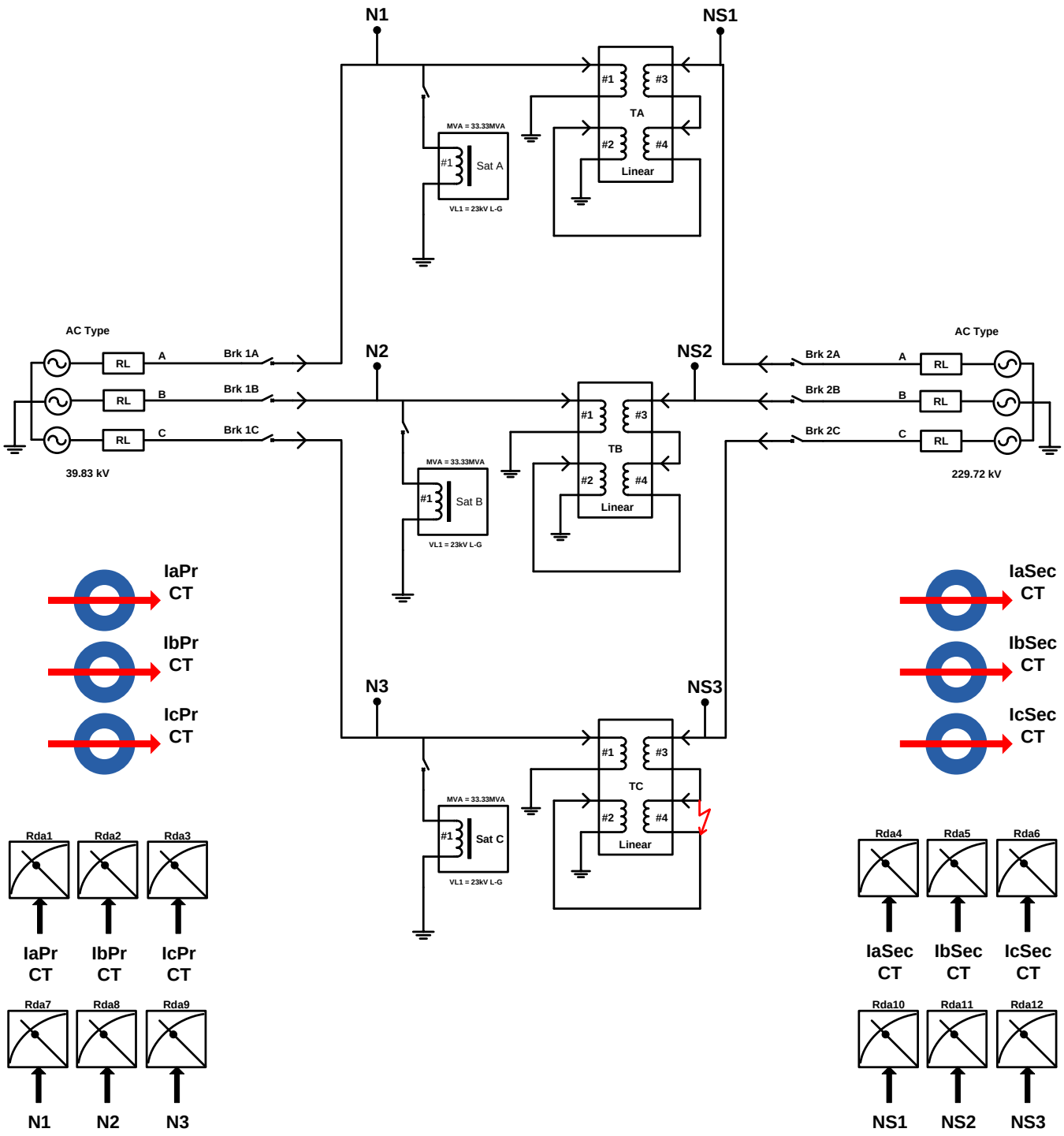

Figure 3.2: RSCAD Model Schematic

two major capabilities was required. First, a model capable of representing a transformer undergoing a turn-to-turn fault was required. Secondly, the non-linear characteristics of the transformer's core had to be adequately represented during energization. A bank of three, magnetically independent single phase transformers was used for this purpose. As described by Yacamini et al. such a model is a good approximation to three-limb or five-limb transformer, whose phases are not magnetically independent, during inrush when the core is heavily saturated. During heavy saturation, the flux will flow in parallel air paths and will not be confined to the core [23]. This effectively isolates each phase magnetically.

3.2.1 Modeling Turn-to-Turn Faults

The method of modeling turn to turn faults will be addressed first. As outlined in Subsection 1.3.2, a turn to turn fault in any given phase can be simulated using a linear, single phase, four winding transformer [15]. The voltages across each winding of this transformer can be related to their respective winding currents using Equation 3.1 [50].

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} R_{11} & 0 & 0 & 0 \\ 0 & R_{22} & 0 & 0 \\ 0 & 0 & R_{33} & 0 \\ 0 & 0 & 0 & R_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \tag{3.1}$$

V_x = voltage across each winding
i_x = current through each winding
R_{xx} = winding resistances
L_{xx} = winding self-inductances
L_{xy} = winding mutual-inductances
x, y = 1,2,3,4

As the winding resistance of a power transformer are extremely low, setting R_{xx} equal to zero is a good approximation. The remaining part of Equation 3.1 is represented by a linear model of a 4 winding transformer, available in the RSCAD library, shown in Figure 3.3. Winding #1 acts as the primary winding while windings #3, #4, and #2 have been con-

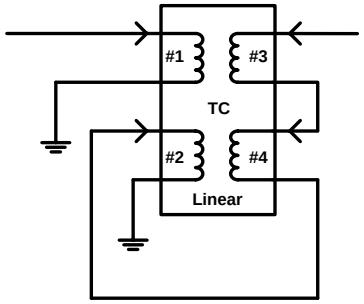

Figure 3.3: RSCAD Model of a Linear 4 Winding Transformer

nected in series to act as the secondary winding. A short circuit placed across winding #4 can be used to simulate a turn to turn fault. The inductance parameters required for this linear transformer model were sourced from [31].

Before Equation 3.1 may be used, leakage reactances between windings must be converted to mutual inductances. The necessary equations for this conversion were derived with the aid of Figures 3.4 and Figures 3.5. Equations 3.2 and Equation 3.3 hold true for both figures. Open circuiting V_2 as shown in Figure 3.4, results in Equation 3.4. The magnetizing current is given by I_{m1}. L_{22} is found by open circuiting the primary side of the transformer and repeating the calculations. Note that $L_{12} = L_{21}$.

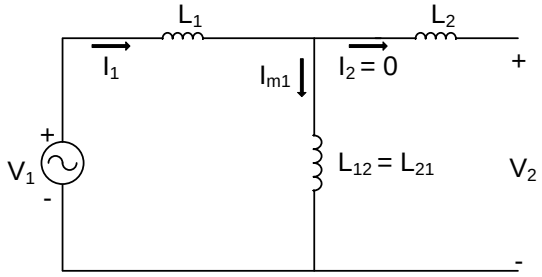

Figure 3.4: RSCAD Linear Transformer: Open Circuit

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \omega \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{3.2}$$

$$L_{11} = L_1 + L_{12} \quad L_{22} = L_2 + L_{21} \tag{3.3}$$

$$L_{11} = \frac{V_1}{\omega i_{m1}} \quad L_{22} = \frac{V_2}{\omega i_{m2}} \tag{3.4}$$

The circuit's impedances do not change, regardless of the circuit's configuration. Therefore, short circuiting V_2 as shown in Figure 3.5, and solving for the mutual inductance results in Equation 3.5. This derivation may be extended from a two winding transformer to a single phase, four winding transformer such as the one shown in Figure 1.5. The self inductances for each winding, L_{XX} may be calculated using the magnetizing current and Equation 3.4 with the voltage across the given winding, V_x. The magnetizing current is common to all windings. Mutual inductances, L_{XY}, required in Equation 3.1 may be calculated using the proper combination of self inductances and Thevenin impedances which are defined by Equation 3.6. Mutual inductances for the transformer model in this thesis were calculated by the Real Time Power Systems Laboratory in collaboration with the Manitoba HVDC Center engineers in 2010 and are shown in Tables A.3 and A.2

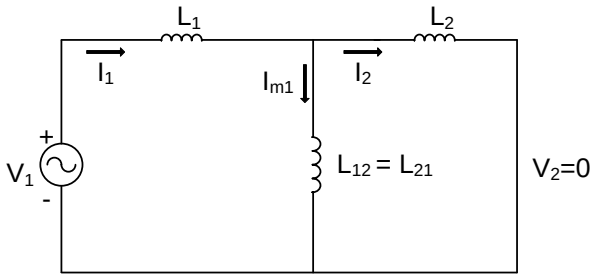

Figure 3.5: RSCAD Linear Transformer: Short Circuit

$$L_{12} = \sqrt{L_{11}L_{22}}\sqrt{1 - \frac{X_{12}}{\omega L_{11}}} \tag{3.5}$$

$$X_{12} = X_{21} = \frac{V_1}{I_1} \tag{3.6}$$

3.2.2 Inclusion of Core Non-linearity

The search for a non-linear model of a transformer began with the state-of-the-art of transformer modeling. A three phase transformer model developed specifically for the study of

inrush phenomena in transformers was developed by Dr. Nicola Chiesa in 2010 [17]. The construction of a Chiesa transformer model for a three winding transformer will be briefly outlined in this thesis. This procedure would apply to a 4 winding transformer as well.

A transformer consists of two distinct circuits: a magnetic circuit representing properties of the core and an electric circuit representing the windings. While the two are inextricably linked in a physical transformer, it takes considerable effort to link the magnetic circuit to the electric circuit when constructing a model. In order to include both the magnetic and electric circuit in the same model, the magnetic circuit is transformed into an electric equivalent. This transform, first described by Cherry [51], exploits the duality between electric and magnetic circuits in order to describe the magnetic circuit while accounting for the winding topology. Concentric, sandwich, or mixed windings topologies are accounted for in this model and result in different leakage flux arrangements. The application of the Duality Transform to a concentrically wound transformer, shown in Figure 3.6, results in the electric circuit shown in Figure 3.7.

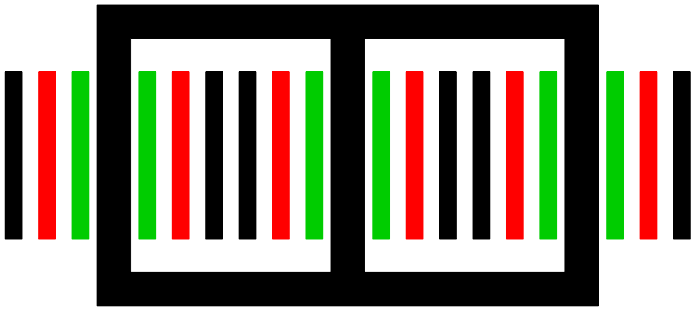

Figure 3.6: Three Winding, Concentrically Wound Transformer

The components shown in Figure 3.7 require explanation. L_{C1}, L_{12}, and L_{23} represent the leakage inductance between the core and the inner winding, the inner winding and the middle winding, and the middle winding and the outer winding respectively. R_1, R_2, R_3 represent the winding resistances of the inner winding, the middle winding, and outer winding respectively. L_0 represents the zero-sequence inductance. All inductances and resistances described thus far are linear. L_{Leg} and L_{Yoke} however are non-linear inductances, representing the legs and yoke that make up the transformer core.

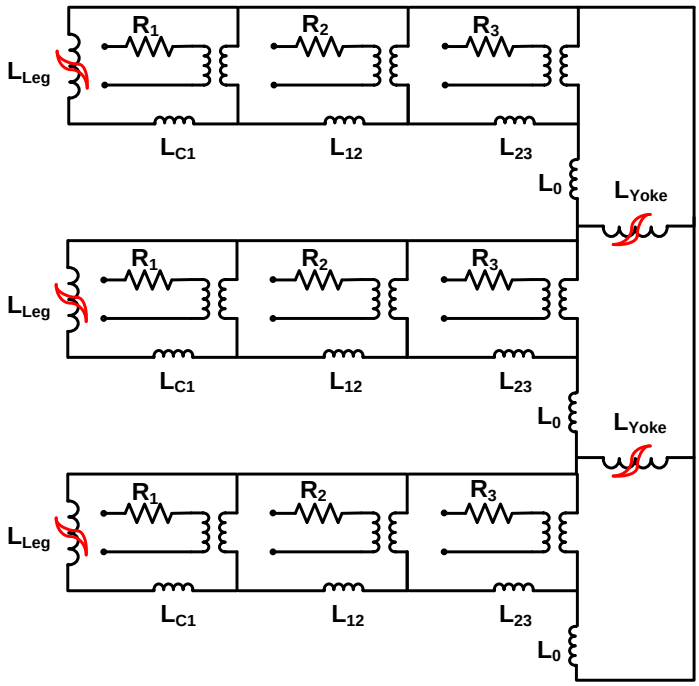

Figure 3.7: Chiesa Model of Three Winding, Concentrically Wound Transformer

The non-linear inductances are represented using the Jiles-Atherton hysteresis (JAH) model. Saturation, hysteresis loss, and eddy current losses can all be accounted for in the JAH model. Though this model represents L_{Leg} and L_{Yoke} with great accuracy, it is difficult to implement in a real time system as the JAH algorithm requires the iterative solution of differential equations. Implementation challenge is compounded by the lack of magnetic data needed to represent the transformer's core. The parameters required to implement the JAH must be estimated from experimental data. This is accomplished by curve fitting the JAH anhysteretic magnetization curves to one that is experimentally obtained. The equations representing the various losses must also be fit to losses found from experimental data. This fitting procedure is not trivial as the five JAH models, needed to represent the legs and yokes of the core, must be fit simultaneously.

The challenges associated with the implementation of the Chiesa model in a real-time system are beyond the scope of this thesis. A literature review was conducted in order to find a model of a non-linear transformer better suited to implementation in a real-time simulator.

Dommel reported the use of non-linear inductances across the terminals of auto-transformers

in order to simulate a non-linear core [50]. Yacamini et al. describe the use of a non-linear transformer bank in order to model a non-linear three phase transformer [23]. Each phase is identical and consists of a non-linear inductance in parallel with an ideal transformer as shown in Figure 3.8. The additional element, when compared to Figure 3.3, is the RTDS model of a non-linear inductor. This non-linear inductor is based on the two-slope approximation of the saturation curve.

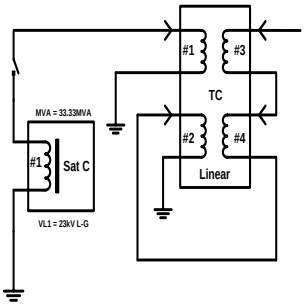

Figure 3.8: RSCAD Model of a Non-Linear 4 Winding Transformer

The saturation curve, shown in Figure 1.8, can be approximated by two lines of different slopes [50], [49]. From Equations 1.12, 1.13, and 1.14, it is clear that the slope of the saturation curve determines the value of the non-linear inductance. Therefore two slopes allow for two states: saturated and unsaturated. Below the saturation curve's knee, the core is unsaturated and the magnetizing inductance is large. Above the knee, the core is saturated the magnetizing inductance is low.

This sharp distinction between states allows the transformer to be modeled by the combination of two elements. When unsaturated, the behavior of the transformer is fully described by the linear model with the non-linear inductance considered to be an infinite inductance [50]. The saturation element allows current to flow only if the core is excited to the point of saturation. Therefore, the non-linear inductor's saturation curve can be fully described by two parameters: a knee voltage, V_{knee} [5], and an air-core reactance, L_{air} [7]:

$$V_{knee} = \frac{NBA\omega}{\sqrt{2}}\,, \tag{3.7}$$

$$L_{air} = \frac{\mu_o N^2 A_w}{h_w}\,, \tag{3.8}$$

N = Number of turn of excited windings

B = 1.9 Tesla, typical transformer core knee flux density [7]

A = Area of core

$\omega = 2\pi f, f = 60Hz$

A_w = Area of excited winding

h_w = Height of excited winding

μ_o = Magnetic permeability of vacuum

The data required to populate Equations 3.7 and 3.8 can be found in Table 3.1. The model used to test the proposed negative sequence based algorithm, shown in Figure 3.2, is similar to the model developed in [52]. This type of model allows the turn-to-turn fault detection program to be tested in situations which are known to cause mal-operation. The following situations [19], besides turn-to-turn faults, may be considered with this model: transformer energization, over-excitation, and external fault coupled with current transformer saturation.

3.2.3 Verification of Inrush Current Model

In order to verify the model constructed during the course of this thesis, the expected value of inrush current was calculated using the iterative procedure given in [53] and according to the example given in [7]. This calculation provided the maximum inrush current envelope that can be developed by the transformer under study. These calculated peak values were compared to the values obtained from the RTDS model in Figure 3.9. The iterative calculation, accurate for the first ten cycles [7], were used to find the inrush current envelope given below.

Three constants, specific to the calculation [7], are given in Equation 3.10. Equation 3.11 is used to determine the angle, in radians, which represents when the core saturates. First the air core reactance, X_{air}, must be calculated using the parameters given in Table 3.1 with Equation 3.9. Then the first energization current peak is calculated using Equation 3.12.

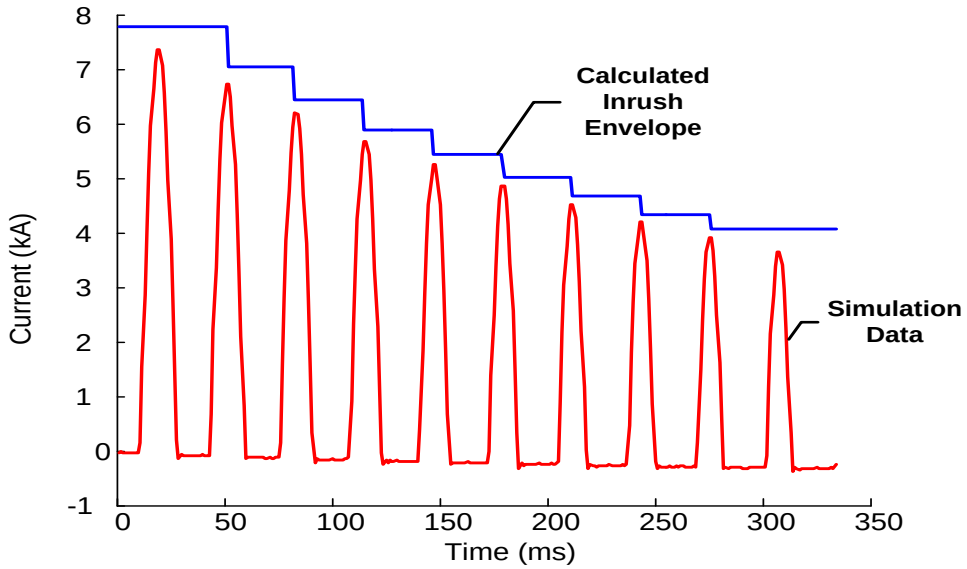

Figure 3.9: Comparison of Calculated to Model Peak Inrush Current

Parameter	**Symbol**	**Value**	**Units**
Primary Turns	N_P	150	Unitless
Winding Area	$A_{winding}$	0.6027	m^2
Winding Height	$h_{winding}$	1.80	m
System Frequency	f_{sys}	60	Hz
System Resistance	R_{sys}	0.10	Ω
Saturating Flux Density	B_{sat}	1.9	T
Peak Operating Flux Density	B_{op}	1.8	T
Residual Flux Density	B_{res}	0	T
Line-to-Ground Voltage	V_{LG}	23	kV

Table 3.1: Transformer Core Data

This current is used to plot the envelope shown in Figure 3.9. The residual flux density is calculated given in Equation 3.13, and passed to the next iteration, in order to calculate the next peak.

$$X_{air} = \frac{\mu_0 N_P^2 A_{winding}}{h_{winding}} 2\pi f_{sys} = \frac{4\pi x 10^{-7} \cdot 150^2 \cdot 0.6016 \cdot 2\pi \cdot 60}{1.8} = 3.5629\Omega \quad (3.9)$$

$$K_1 = 0.9 \quad K_2 = 1.15 \quad K_3 = 2.26 \quad (3.10)$$

$$\Theta = K_1 Cos^{-1}\left(\frac{B_{sat} - B_{op} - B_{res}}{B_{op}}\right) = 0.9 \cdot Cos^{-1}\left(\frac{1.9 - 1.7 - 0}{1.7}\right) = 1.308rad \quad (3.11)$$

$$I_{peak} = \frac{K_2 V_{LG}\sqrt{2}}{X_{air}} Cos\left(1 - Cos\Theta\right) = \frac{1.15 \cdot 23 \times 10^3 \cdot \sqrt{2}}{3.5629}\left(1 - Cos1.308\right) = 7.771kA \quad (3.12)$$

$$B_{res} = B_{res} - \frac{B_{op} K_3 R_{sys} 2\left(Sin\Theta - \Theta Cos\Theta\right)}{X_{air}} = 0 - \frac{1.8 \cdot 2.26 \cdot 0.1 \cdot 2\left(Sin1.308 - 1.308 \cdot Cos1.308\right)}{3.5629}$$
$$= -0.1429 \quad (3.13)$$

The fundamental and second harmonic current of inrush current data, collected from the unfaulted RTDS transformer model, is shown in Figure 3.10. These waveshapes were compared to the fundamental and second harmonic current of inrush current data shown in [38].

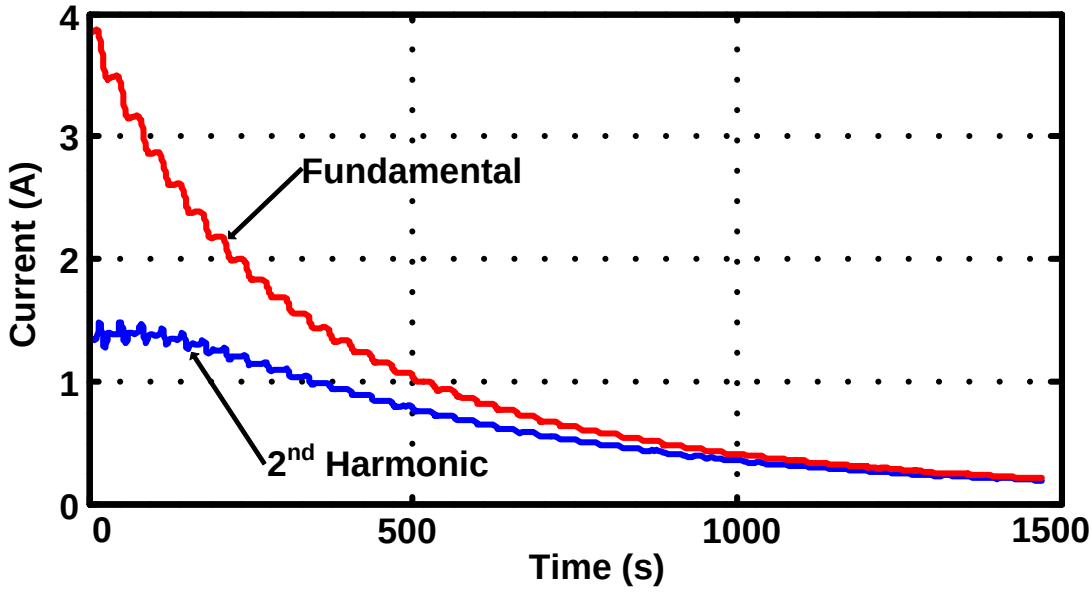

Figure 3.10: Fundamental and Second Harmonic Current Data

3.2.4 Sensing Elements: Current Transformers

Currents flowing in an electrical power circuit are higher than a relay can measure directly. Most relays accept a one Ampere or five Ampere current input. Therefore, the currents flowing in the electrical circuit must be stepped down. Current transformers (CT) must be installed in order to reduce the power system's current to a measurable level. These current transformers suffer from saturation as well. A large fault current or inrush current can therefore distort the current that is sensed by the relay. CT saturation must modeled in order to accurately represent a real-world application.

Figure 3.11: RSCAD Breakers

In order to add non-linear CTs to the model, the circuit breakers on the primary and secondary side of the transformer, shown in Figure 3.11, are used to sense current flowing through them. This undistorted current signal is stored in a variable which is read by the RTDS CT elements shown in Figure 3.12. These elements represent non-linear current transformers, one for each phase on the primary and secondary side of the transformer. The CTs are connected in a Y configuration.

Figure 3.12: RSCAD Current Transformer Elements

The current transformer model is very similar to the model of a saturable transformer. Therefore, it warrants closer examination. The secondary side of the CT is shown in Fig-

ure 3.13. I_{sec} represents the current flowing in the secondary of the winding which is the primary side current divided by the CT ratio. L_{mag} and R_{loss} represent the magnetizing branch inductance and loss respectively, both are non-linear. Saturation lowers the magnetizing inductance which allows for a large magnetizing current, I_{mag}, to flow. R_{loss} represents the hysteresis losses, described by Equation 1.15.

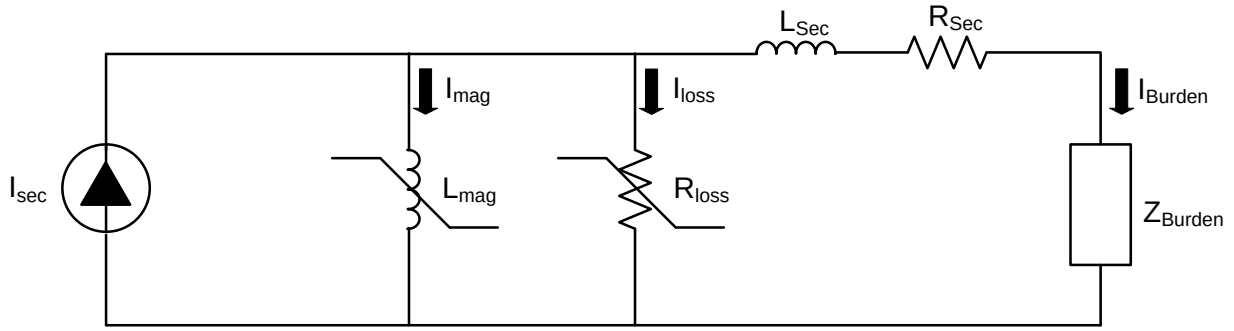

Figure 3.13: RSCAD Current Transformer Model

The leakage inductance of the CT's secondary winding is given by L_{Sec} while its winding resistance is given by R_{Sec}. Z_{Burden} represents the impedance offered by the cable connecting the CT to the relay along with the impedance of the relay's sensing circuit. Typical values for L_{Sec} and R_{Sec} are given by [54] along with a saturation curve and hysteresis loop width. These values are entered into the RTDS CT model where they determine L_{mag} and R_{loss} respectively.

A small burden means saturation distorts the CT's output to a lesser extent. This is obvious from the CT's model shown in Figure 3.13. A current divider exist between the burden branch and the magnetizing branch. Therefore, if Z_{Burden} is much smaller than the magnetizing branch of the CT, I_{Burden} will be much larger than I_{mag} and R_{loss}. Since I_{Burden} is sensed by the relay, a more accurate measurement can be obtained with a lower burden.

The CT ratios and burdens were chosen according to IEEE standard [55], taking the CT saturation curve into consideration: the maximum three-phase fault current will not exceed the CT's knee voltage for the given burden. The current transformer configuration, designed not to saturate, is given in Table 3.2:

Location	CT Ratio	Burden (Ω)
Low Voltage Side	300:1	0.5
High Voltage Side	50:1	0.5

Table 3.2: Current Transformer Ratios and Burdens

Location	CT Ratio	Burden (Ω)
Low Voltage Side	300:1	4.56
High Voltage Side	50:1	4.56

Table 3.3: Current Transformer Ratios and Burdens for Saturation

The behavior of negative sequence based protection and differential protection will also be examined in the event of CT saturation. In order to conduct such an examination, the CT burden is deliberately chosen such that the knee voltage of the CT is attained during a fault. Using the settings found in Table 3.3 would result in CT saturation during fault conditions.

The calculations used to obtain the CT burdens, on the primary side of the transformer, is given below. The ratio of the primary side CT is determined first. The simulated system's power flow has been arranged such that the transformer's rated current flows under steady-state conditions. This current was calculated, as shown in Equation 3.14, using the transformer's power and primary voltage. Using a standard CT ratio, this current must be transformed to a CT secondary that is acceptable to the relay protecting the transformer. The prototype relay's input current is 5A, therefore a 300:5 CT ratio is used. Using this ratio, a secondary current, denoted by $I'_{S,Rated}$ is obtained. Next, the CT's behavior during fault conditions is examined. The current transformer must not saturate during the heaviest expected faults.

$$I_{S,Rated} = \frac{100MVA}{\sqrt{3} \times 39.83kV} = 1.450\,kA \qquad I'_{S,Rated} = \frac{1.450\,kA}{300} = 4.83A \tag{3.14}$$

The CT's excitation curve knee voltage, shown in Figure 3.14, was found according to IEEE standard [55]. The excitation curve is based on several discrete data points producing an

excitation curve that is not smooth. Therefore the process of finding the knee voltage as shown in Figure 3.14 is an approximation to the process outlined in [55]. First, the non-saturating CT burden was calculated. The highest fault current that the transformer is expected to experience, due to a three-phase fault occurring on the secondary side of the transformer, was found using the RTDS simulation given in Equation 3.15. The secondary current, calculated in Equation 3.18, is used to calculate the voltage across the burden. For a burden of 0.5 Ω the burden is calculated in Equation 3.17, giving a voltage of 15.90V which is well below the knee voltage of 145V. Therefore the CT ratio and burden are acceptable, ensuring the current transformers will not saturate during the worst fault currents the system is likely to experience. In order to deliberately cause CT saturation, for the purpose of testing transformer protection algorithms, a CT burden, R_{Sat}, was chosen using the knee voltage of the CT's excitation curve. This calculation is shown in Equation 3.18.

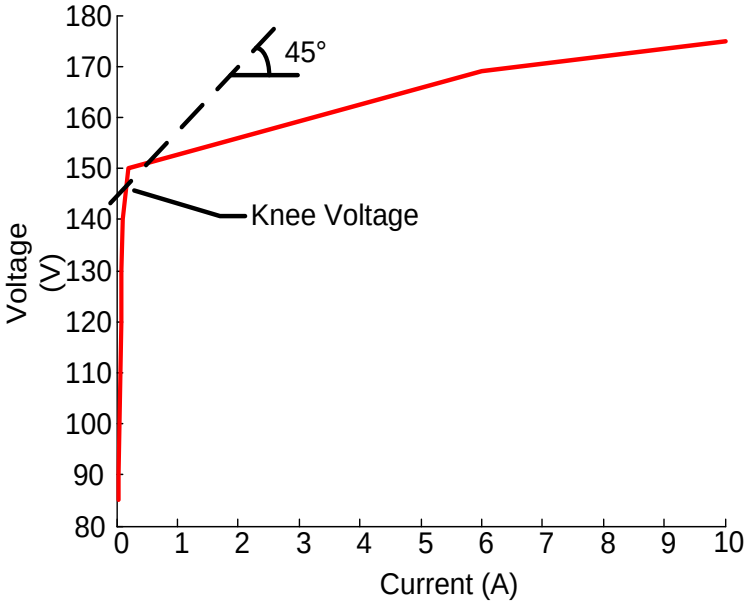

Figure 3.14: Simulation CT Excitation Curve

$$I_{S,3Ph} = 9.536kA \tag{3.15}$$

$$I'_{S,3Ph} = \frac{I_{S,3Ph}}{300} = \frac{9.536kA}{300} = 31.79A \tag{3.16}$$

$$V_{0.5\Omega} = 31.79A \cdot 0.5\Omega = 15.90V \tag{3.17}$$

$$V_{Knee} = I'_{S,3Ph} R_{Sat} \qquad R_{Sat} = \frac{145\,V}{31.79\,A} = 4.56\Omega \tag{3.18}$$

3.2.5 Sensing Elements: Coupling Capacitor Voltage Transformer (CCVT)

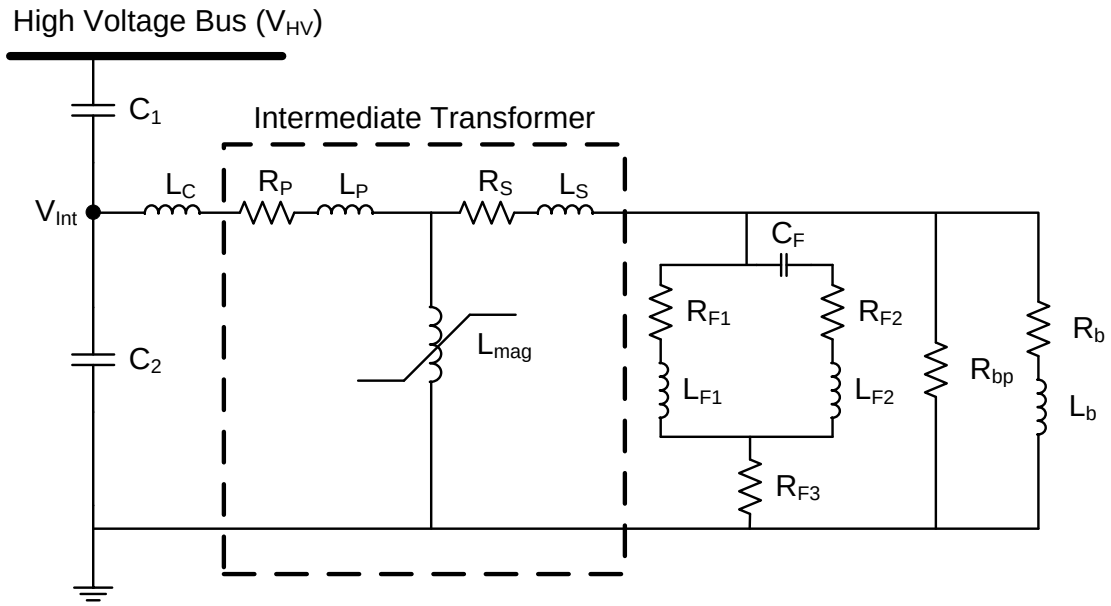

Figure 3.15: RSCAD CCVT Elements

Voltages present in an electric power system must be reduced using a CCVT prior to being fed into the relay's voltage input. Trench offers Coupling Capacitor Voltage Transformers for voltages greater than 72.5kV [56]. Therefore a CCVT will be used to sense the voltage on the 230kV side of the transformer model. The RTDS model used to simulate the CCVT is shown in Figure 3.15 [54] with settings given in Appendix A.

The components show in Figure 3.15 warrant a more detailed discussion. The capacitive voltage divider is composed of capacitors C_1 and C_2. This divider reduces the bus voltage, V_{HV}, to the intermediate voltage, V_{Int}, of approximately 17kV [57], [56]. These capacitors introduce an undesirable phase shift. Compensating inductor L_c is required to return the

impedance of the circuit to unity, removing the phase shift, as shown in Equation 3.19 [58]. The system frequency, f, is 60Hz . The capacitances form a voltage divider given by Equation 3.20. The inductance must be specified in order to solve Equations 3.19 and 3.20 for C_1 and C_2. Therefore an inductance of 42 H, which is typical for a CCVT of 230kV [59] is chosen.

$$L_c = \frac{1}{(C_1 + C_2)(2\pi f)^2} \tag{3.19}$$

$$\frac{V_{HV}}{V_{Int}} = \frac{C_1}{C_1 + C_2} \tag{3.20}$$

The intermediate transformer steps down the intermediate voltage of 11kV to 115V. It is modeled by specifying the primary winding resistance and leakage inductance, R_p and L_p respectively. The secondary winding resistance and leakage inductance is specified by R_s and L_s respectively. L_{mag} represents the intermediate transformer's saturable core as a non-linear inductance. This non-linear inductance can interact with the voltage divider capacitors causing ferro-magnetic resonance. A filter circuit, modeled by R_{F1}, L_{F1}, C_F, R_{F2}, L_{F2}, R_F damps out any oscillation associated with ferro-magnetic resonance. The burden is represented by R_{bp}, R_b, L_b.

The voltage on the CCVT's secondary side is calculated in Equation 3.21 using 3.20. The intermediate transformer's ratio is 11 kV: 115 V.

$$112V = 230,000V \times \frac{1.28962 \times 10^{-2}\,\mu F}{1.28962 \times 10^{-2}\,\mu F + 2.63974 \times 10^{-1}\,\mu F} \times \frac{115}{11,000} \tag{3.21}$$

The voltage at the secondary side of the voltage transformer must be further reduced in order to be sensed by the analog-to-digital conversion system. This function is performed by the output channel elements, described in Section 3.2.7, with settings listed in Table 3.4. The peak line-to-ground voltage output by the output element is given in Equation 3.22

$$5V = 112V \times \frac{\sqrt{2}}{\sqrt{3}} \times \frac{5}{91.45} \tag{3.22}$$

Location	Output Channel Ratio
Low Voltage Side	93.88:5
High Voltage Side	91.45:5

Table 3.4: Output Channel Ratios for use with CCVT

3.2.6 Point of Wave Control Logic

As described in Section 1.4, inrush current is most severe when the transformer is energized when the voltage wave is at its zero crossing. In order to control which phase experiences the most severe inrush, point-of-wave logic was used to control the circuit breaker energizing the transformer as shown in Figure 3.16. The breaker control switch is manually operated to start a simulation, its signal is logically conjugated with the zero crossing detector. The zero crossing detector monitors the energizing voltage wave. When both the breaker control switch signal and the zero crossing detector signal are HIGH, the AND gate outputs HIGH signal setting the S-R flip-flop which latches the breaker control signal HIGH. This keeps the breaker closed as the zero crossing detector outputs a single pulse when a voltage zero crossing is detected. Primary phase A voltage is shown to be the input to the zero crossing detector in Figure 3.16. The propagation delays of the zero-crossing detector, AND gate, and S-R flip-flop are 0.35μs, 0.275μs, 0.55μs respectively for a total propagation delay of 1.175μs [60].

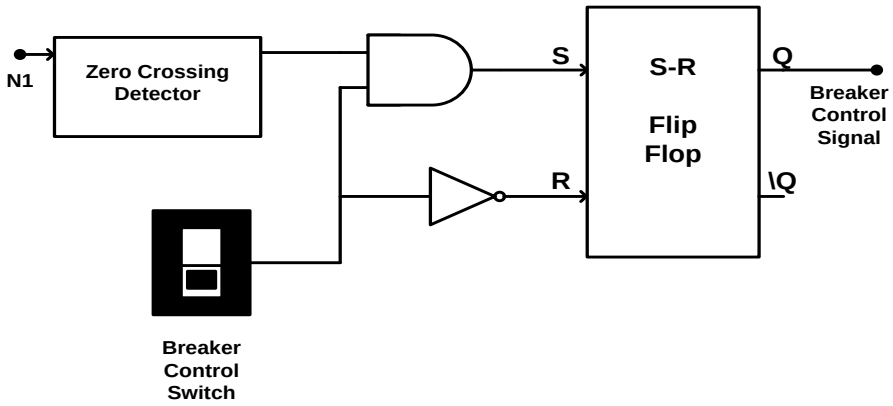

Figure 3.16: RSCAD Point of Wave Controller

3.2.7 Outputting a Signal: Analog Output Channels

The RTDS model is calculated in real time. These calculated values are presented to external equipment in the form of a voltage signal. Current data is processed by the current transformer algorithm, examined in Section 3.2.4, and sent to the analog output channels, shown in Figure 3.17. Voltage data is exported in a similar fashion but it is not processed through a voltage transformer prior to exporting the signal. The voltage signals sent to the analog output channels are a direct representation of the phase voltages.

Figure 3.17: Analog Output Channels

The need to translate the RTDS model's data into a voltage raises another concern: voltage clipping. Both the RTDS output channels and the analog-to-digital conversion (ADC) board have a limited voltage range. Therefore, the current and voltage parameters to be output must be mapped to a voltage range that can be accurately represented by both devices. Distortion due to clipping can not be avoided without sacrificing resolution: if the parameters to be output are mapped to a very large voltage range, no clipping will occur. However, as the full-scale measurement range of the ADC would rarely be utilized, the resolution of the ADC would effectively be reduced. Therefore, the system has been designed to allow a small amount of clipping for the largest possible currents such as during a three-phase to ground fault. Voltage signals do not suffer clipping as the voltage magnitude tend to sag as the result of a fault. The ability of the output channel element to reduce the simulated system's voltage to a measurable voltage level exhibit the properties of an ideal voltage transformer.

The method of voltage ratio calculation is discussed next. The peak line-to-ground

primary side voltage is calculated using Equation 3.23. This voltage must be reduced to 5V in order to be sensed by the relay's analog-to-digital converter.

$$V_{Peak,LG} = 39.83kV \times \frac{\sqrt{2}}{\sqrt{3}} = 32,521V \tag{3.23}$$

Location	Output Channel Ratio
Low Voltage Side	32,521:5
High Voltage Side	187,566:5

Table 3.5: Voltage Output Channel Ratios for Y-Y Transformer

An example of clipping of the current signal, experienced on the low voltage side of phase B during a symmetrical ground fault, is shown in Figure 3.18. The flat tops, indicative of clipping, are most obvious in the first two cycles. The relay algorithm must be robust enough as not to fail when presented with a signal distorted by clipping.

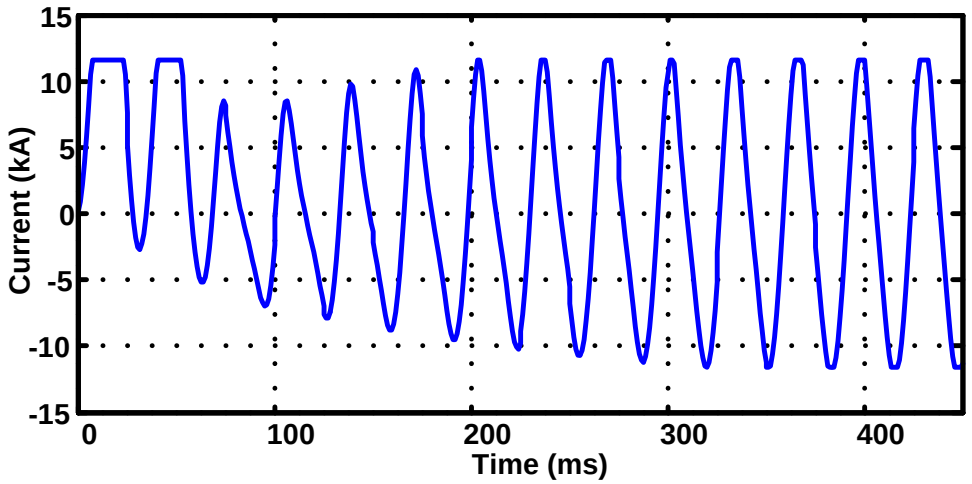

Figure 3.18: Clipping on Low Voltage Side of Phase B during Fault

3.2.8 Fault Resistance

It is unlikely that a turn-to-turn fault will present as a bolted fault. An arc, capable of absorbing large quantities of energy, is formed as the oil impregnated paper insulation breaks

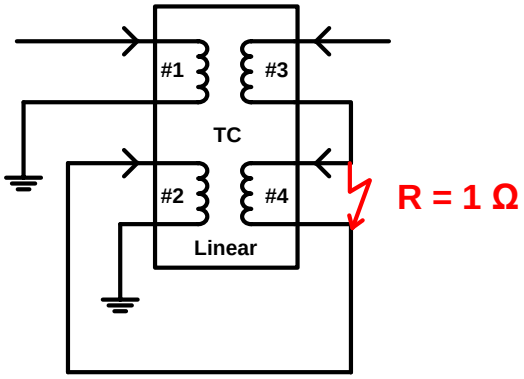

Figure 3.19: Turn-to-turn Fault Fesistance

down . A voltage of great than 50V/turn is required to strike an arc between damaged pieces of insulation [61]. The transformer simulated in this work has 866 turns on the 230 kV side of the transformer resulting in a per-turn voltage of 266V/turn, making a turn-to-turn fault likely. The arc's ability to absorb energy implies that it has resistive properties. The fault is made up of the arc and burned insulation left behind by the arc. The fault current is approximately 100 times of the transformer's rated current [62]. Enough heat is generated by fault current to affect the surrounding windings, propagating the fault to neighboring windings. The accurate modeling of fault resistance would require modeling the chemical properties of transformer insulation during a turn-to-turn fault. Since this is outside the scope of this work, a worst case resistance was derived from data collected by [63]. This data gives a fault resistance of 0.39 Ω for a 3% turn-to-turn fault. In order to give a consistent comparison, a 1 Ω resistance will be used for all faults tested in this work. Simulated results for a one Ohm turn-to-turn fault resistance and a bolted turn-to-turn fault, applied to phase C, will be compared in this work.

3.2.9 Source Model

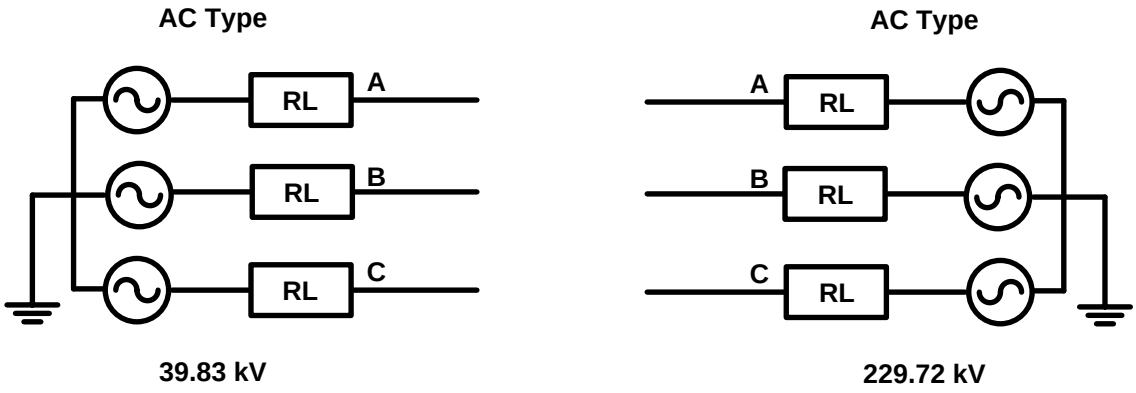

Figure 3.20: RSCAD Sources

Two voltage sources, complete with impedance, were used to simulate the flow of through the transformer model. Each phase of the source operated at the same voltage and the same impedance. Both source impedances were selected to be strongly inductive in order to simulate a high voltage transmission line. The power angle of the low-voltage source ensures that power flow from the low-voltage side to the high-voltage side establishing the low-voltage side as the primary side of the transformer and the high-voltage side as the transformer's secondary side [6].

3.3 Analog-to-Digital Conversion of Real-Time Simulator Output

The outputs generated by the model, executed in the real time digital simulator, are twelve analog voltage signals representing the currents and voltages present in the modeled system. The six signals representing current had to be sampled at precisely the same time in order to preserve their relative phase relationship. These sampled signals were then digitized and processed in the relay algorithm. The circuit board, shown in Figure 3.21, was utilized for this purpose.

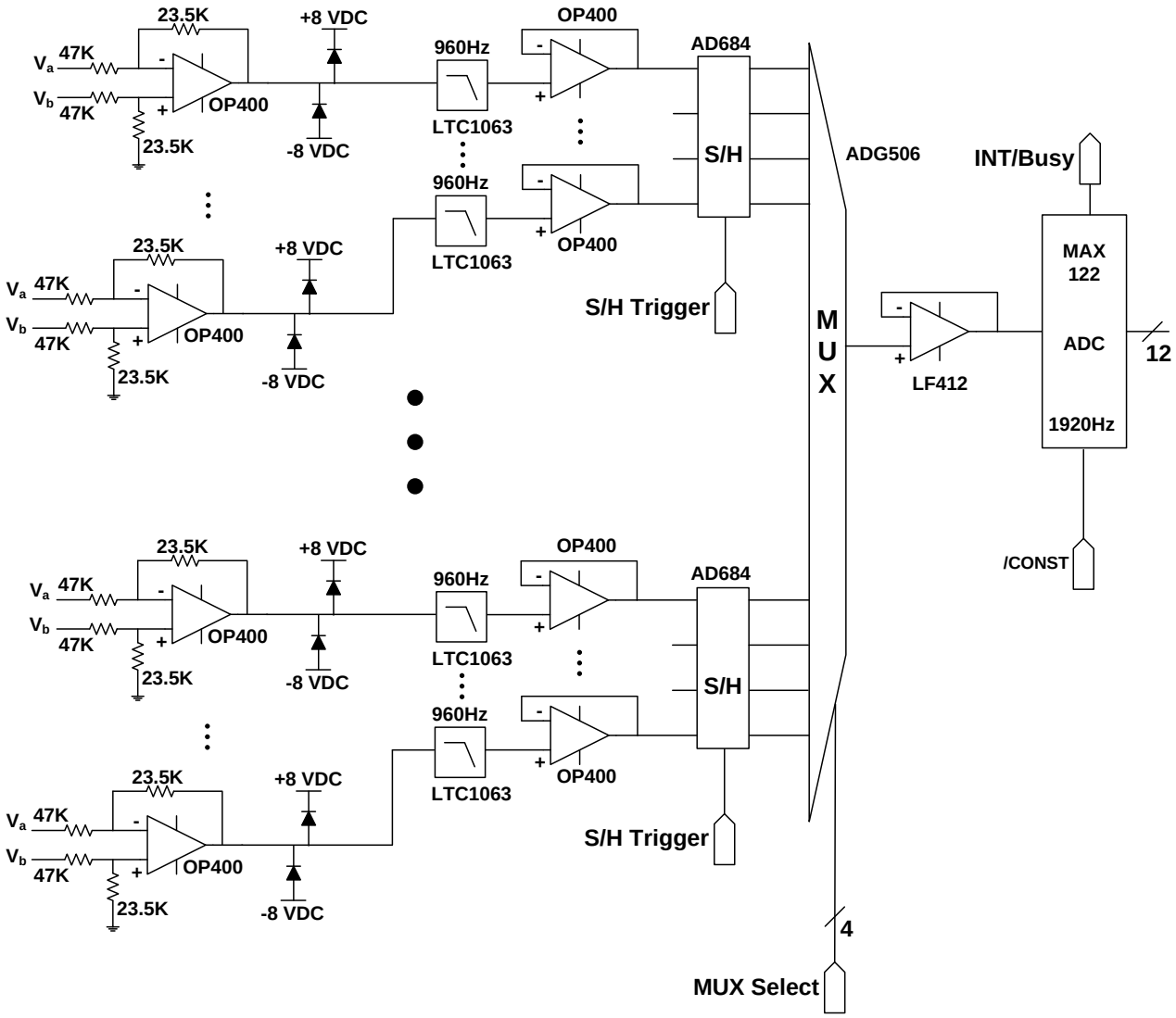

Figure 3.21: Analog-to-Digital Converter Circuit Schematic

There are many repeated elements in the analog-to-digital conversion circuit board shown in Figure 3.21. This repetition is indicated by the vertical ellipsis (⋮). There are four sample-and-hold (S/H) chips of part number AD684. Each of these chips supports four identical channels, allowing for the simultaneous sampling of 16 signals. It is therefore sufficient to describe the components in one channel as all other channels are composed of identical components. Beginning on the left side of the circuit, each channel driven by a pair of twisted wires originating from the real-time simulator. The twisted pair is connected to a differential amplifier [64] which is composed of an OP400 operation amplifier and four resistors. The

twisted pair signal is converted to a single signal through a subtraction and division by two as shown in Equation 3.24. This type of input is designed to receive differential signals where the original signal is sent to the non-inverting input of the op-amp, and the inverted signal is sent on the inverting input of the op-amp. This results in the inverted signal being subtracted from the original signal resulting in double the original signal. Since external noise is imposed on both wires of the twisted pair, the noise subtracts to zero.

$$V_{out} = (V_b - V_a)\frac{23.5K}{47K} \tag{3.24}$$

The real-time simulator model constructed for this work does not utilize this differential feature. This was done in order to simplify the real-time simulator model and utilize a single processor with twelve single-ended outputs. The inverting input, given by V_a in Equation 3.24, was connected to the simulator's ground.

Since the differential amplifiers are supplied by the +/- 12V differential rails, V_{out} could exceed the +/- 8V rail voltage supplying the chips downstream. Therefore diode voltage clamps ensured that the differential amplifier's output never exceeded the +/- 8V rail voltage. After the voltage clamp, the signal passed through an anti-aliasing filter.

The LTC1063 chip functions as a 5^{th}-order Butterworth filter and provides a flat frequency response in the pass band. Since the incoming signal is sampled at 1920 Hz, or 32 times per 60Hz cycle, the anti-aliasing filter's cut-off frequency is set to 960 Hz [25]. The choice of sampling frequency is addressed in Section 3.4. The setting of the cut-off frequency is accomplished by supplying a digital clock signal (0 to 5 Volts, 50% duty cycle) at ten times the desired cut-off frequency: 96,000 Hz. After the incoming signal is filtered, it passes through another operational amplifier configured to act as a voltage follower. It acts as a buffer with an extremely high input impedance and an extremely low output resistance. The voltage follower is suggested by the LTC1063 datasheet [65].

The signal is now ready to be sampled, a task accomplished by the AD684 Sample-and-Hold (S/H) amplifier. A digital input to the AD684, when driven HIGH, allows the sample-and-hold chip to sample the analog input signal. Then the digital input is driven LOW, the AD684's analog output is held constant, even if the analog input to the chip

varies. This is important as there is only one, single channel Analog-to-Digital converter (ADC) in the circuit (marked ADC in Figure 3.21). The S/H circuit allows all 16 channels to be sampled simutaneously, ensuring that the values do not change as they are digitized consecutively. The analog multiplexer (MUX) chip ADG506 allows each sampled value to be routed from the S/H circuit's 16 outputs to the ADC's single input. A single operational amplifier, configured as a voltage follower, acts as a buffer between the single MUX output and single ADC input. This configuration was recommended in the AD684 datasheet [66].

The MAX122 chip functions as the analog-to-digital converter. Provided a 5 MHz clock is supplied to the MAX122 ADC chip's clock input pin, it is capable of a 2.6 micro-second conversion time. The MAX122 is capable of digitizing a $\pm$ 5V signal with 12-bit resolution. The Microchip micro-controller controls the entire analog-to-digital conversion process. The micro-controller also receives, buffers, and processes all the data gathered by the ADC board. It is the platform which executes the relay algorithm.

3.4 Digital Relay Algorithm

The algorithm platform is a PIC32MX360F512L micro-controller running at 80Mhz. This clock frequency, along with a level-2 complier optimization setting is required to execute the relay algorithm given a sampling rate of 1920Hz. The algorithm was written in C and was compiled using Microchip's MPLAB XC.

According to Sidhu et al. [67], a sampling frequency of 1200 Hz is sufficient for transformer turn-to-turn fault protection. A sampling frequency of 1920Hz, or 32 samples per 60Hz cycle, was chosen for this work as it fully utilized the micro-processor's resources. Fully utilized, the system was capable of executing 12 Discrete Fourier Transforms (DFT) each sample period or once every 0.5208 ms for each channel. The result for each DFT is a complex number which can be represented in either magnitude/phase format or rectangular format. Though magnitude/phase format must be used for the relaying comparisons, the rectangular format allowed for faster computation in a 16-bit processor. Therefore, the negative sequence transform equation was designed to operate on rectangular co-ordinates.

To further increase computation speed, the DFT algorithm [25] was designed to perform integer multiplication. The real and imaginary components of the DFT are then defined, in integer form, by Equations 3.25 and 3.26.

$$I_{Re}[n] = \left(\sum_{k=0}^{32} i[n] * ReCoeff[k] \right) >> 16 \tag{3.25}$$

$$I_{Im}[n] = \left(\sum_{k=0}^{32} i[n] * ImCoeff[k] \right) >> 16 \tag{3.26}$$

Where:

$$ReCoeff[k] = (int) \left(\frac{2}{N} \right) Sin(2\pi fk\Delta T)2^{32} \tag{3.27}$$

$$ImCoeff[k] = (int) \left(\frac{2}{N} \right) Cos(2\pi fk\Delta T)2^{32} \tag{3.28}$$

$$N = 32, f = 60Hz, \Delta T = \frac{1}{1920Hz} \tag{3.29}$$

Cast to integer and bit-shift operators are shown as (int) and $\gg$ respectively. The negative sequence transform can now be computed using the real and imaginary components, found for each phase, by applying Equations 3.30 and 3.31. These components are then inserted into the following equations:

$$Re\{I_{-ve}\} = Re\{I_a\} - ((Re\{I_b\} + Re\{I_c\}) >> 1) + \frac{\sqrt{3}}{2}(Re\{I_b\} - Re\{I_c\}) \tag{3.30}$$

$$Im\{I_{-ve}\} = Im\{I_a\} - ((Im\{I_b\} + Im\{I_c\}) >> 1) + \frac{\sqrt{3}}{2}(Im\{I_b\} - Im\{I_b\}) \tag{3.31}$$

The magnitude and phase of the negative sequence transform result are then computed by Equations 3.32 and 3.33 respectively.

$$|I_{-ve}| = \sqrt{(Re\{I_{-ve}\}^2 + Im\{I_{-ve}\}^2)} \tag{3.32}$$

$$ARG(I_{-ve}) = atan2(Im\{I_{-ve}\}, Re\{I_{-ve}\}) + \pi \tag{3.33}$$

3.5 $\triangle$ - Y Transformer Model

The Y - Y transformer has been studied thus far as it allows for simple, intuitive relay settings. This type of winding configuration, if used without a Δ-connected tertiary winding, gives rise to third harmonics if the transformer is subjected to unbalanced loading. As three windings would be required in order to accomplish a Y-Δ-Y transformer, it is beyond the scope of this work. A two-winding Δ - Y or Y - Δ Transformer is the most common winding connection [46] due to its many advantages. The Δ-connected winding counteracts the third-harmonic current by allowing it to circulate in the Δ-connected winding. This winding configuration is commonly applied to the low-voltage side of the transformer in order to reduce copper costs since each phase of the Δ-connected experiences 58% of the line current. The Y-connected winding is well suited to act as the high-voltage winding since each phase experiences 58% of the line voltage thereby allowing for reduced insulation cost. A 30° phase shift is introduced due to the Δ - Y winding configuration. According to the American Standards Association (ASA), transformer windings must be arranged such that the line voltage on the high-voltage side leads the line voltage on the low-voltage side by 30° [46]. This means that a Dy11 winding arrangement [68], as shown in phasor diagram in Figure 3.22, must be used in order to satisfy ASA convention. Note that positive sequence phase rotation is counter-clockwise.

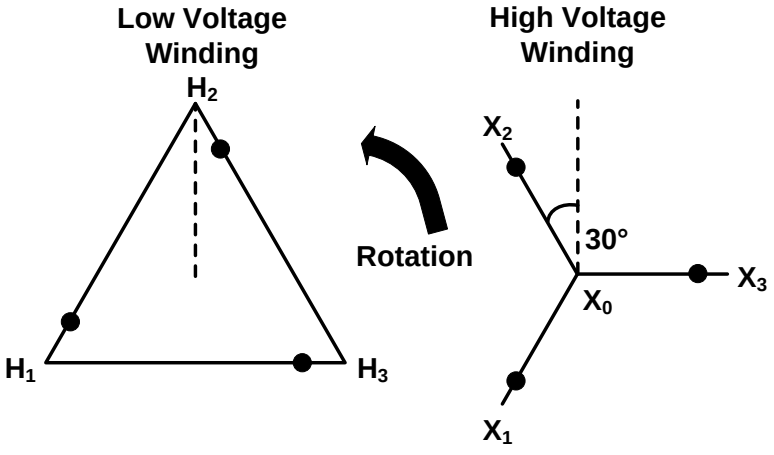

Figure 3.22: Dy11 Phasor Diagram

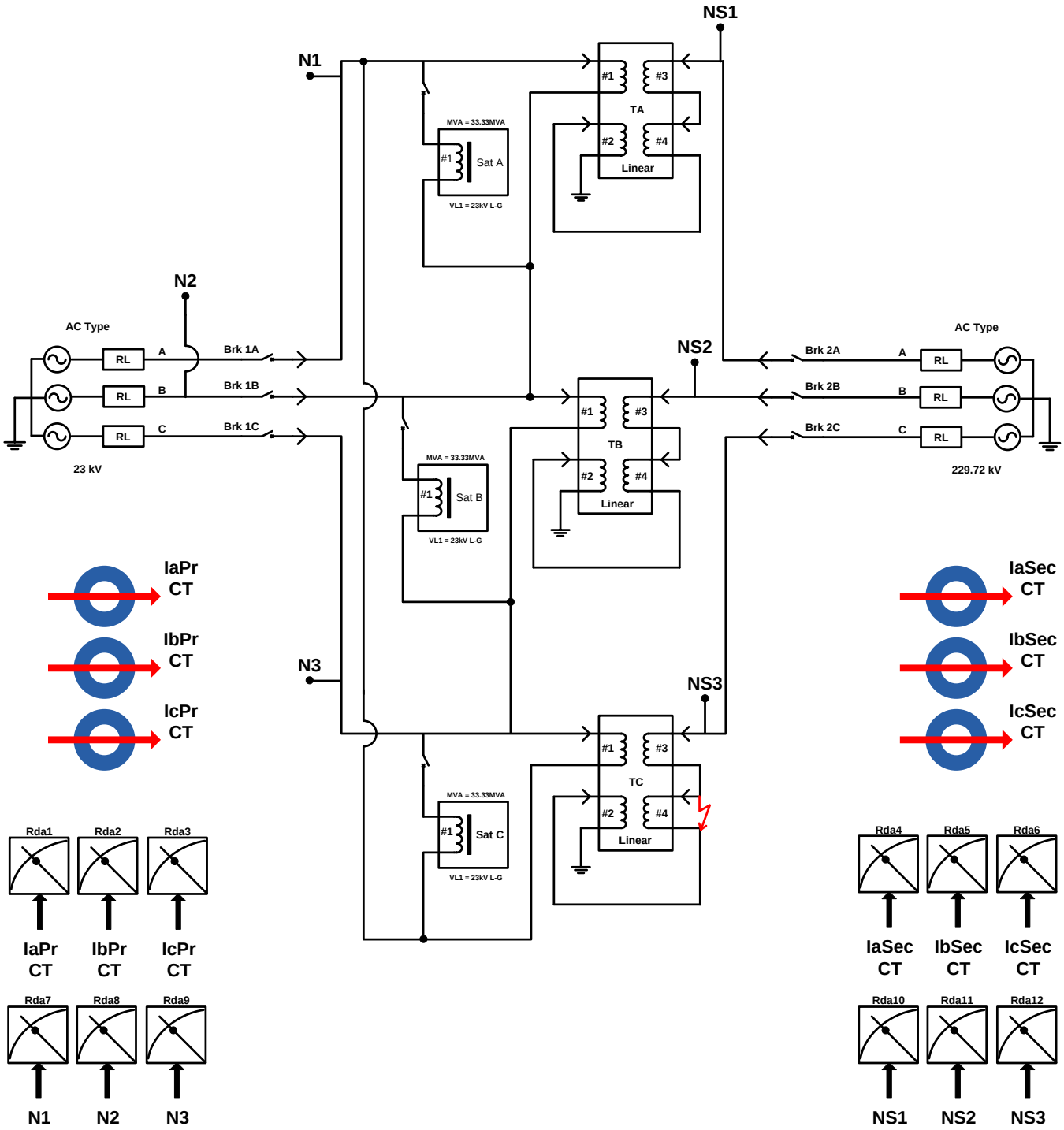

Figure 3.23: RSCAD Δ - Y Transformer Model Schematic

In order to simulate a Δ - Y Transformer, several changes must be made to the simulation model. The low-voltage side was Δ-connected as shown in Figure 3.23. The new winding

configuration results in a different transformer ratio as given by Equations 3.34. Therefore, the low-voltage was changed to 23kV, from 39.83kV as shown in Figure 3.2, in order to maintain the same line voltage on the high-voltage side. The current transformer ratio were also modified in order to account for the increased line current on the low voltage side, as given in Table 3.6. The ideal voltage transformer ratios, tailored to the Δ - Y transformer, are given in Table 3.7.

$$\frac{V_{HV}}{V_{LV}} = \sqrt{3}a_{XFMR}; \frac{I_{HV}}{I_{LV}} = \frac{1}{\sqrt{3}a_{XFMR}} \tag{3.34}$$

The RSCAD model allowed for only a Y-connection of current transformers to be modeled.

Location	**CT Ratio**	**Burden (Ω)**
Low Voltage Side	600:1	0.5
High Voltage Side	50:1	0.5

Table 3.6: Δ - Y Transformer: Current Transformer Ratios and Burdens

Location	**Output Channel Ratio**
Low Voltage Side	18,776:5
High Voltage Side	187,566:5

Table 3.7: Output Channel Ratios for Δ - Y Transformer

Therefore additional processing was needed before the currents from the low-voltage side of the transformer could be compared to the high-voltage side [68] by the differential protection algorithm. The phasor calculations, given in Equations 3.35, 3.36, and 3.37 were performed on the high-voltage side currents before the differential protection algorithm calculations, outlined in Section 1.6.4, could be applied. The second harmonic current present on the secondary side is also treated in the same manner. These calculations removed zero sequence current not present in the low-voltage side current, accounted for the factor of $\sqrt{3}$ of the transformer ratio in Equations 3.34, and compensated for the 30° phase shift introduced by the Δ-connected low-voltage windings. The negative sequence based algorithm also pre-

processes the incoming current phasor with Equations 3.35, 3.36, and 3.37.

$$\vec{I}_{AC_{HV}} = \vec{I}_{A_{HV}} - \vec{I}_{C_{HV}} \tag{3.35}$$

$$\vec{I}_{BA_{HV}} = \vec{I}_{B_{HV}} - \vec{I}_{A_{HV}} \tag{3.36}$$

$$\vec{I}_{CB_{HV}} = \vec{I}_{C_{HV}} - \vec{I}_{B_{HV}} \tag{3.37}$$

The line voltages, needed for the negative sequence voltage portion of the proposed relay are processed differently. A closer examination of these equations is warranted. The voltage portion of the negative sequence relay is concerned with only the voltage difference across each of the phases of the transformer. With the Y-Y winding configuration, this is easily determined as both the primary and secondary windings are grounded to form a grounded Y connection. The voltages measured by the voltage transformers are line-to-ground voltages which, in the case of a Y-Y connected transformer, may be used directly in the negative sequence algorithm. This is not the case for a Δ - Y Transformer. The primary voltage phasors must be processed by Equations 3.38, 3.39 and 3.40 prior to the negative sequence transform being applied while the secondary voltage phasors are processed by Equations 3.41, 3.42 and 3.43 prior to transformation.

$$\vec{V}_{LVWindingA} = \vec{V}_{ACn_{LV}} - \vec{V}_{BAn_{LV}} \tag{3.38}$$

$$\vec{V}_{LVWindingB} = \vec{V}_{BAn_{LV}} - \vec{V}_{CBn_{LV}} \tag{3.39}$$

$$\vec{V}_{LVWindingC} = \vec{V}_{CBn_{LV}} - \vec{V}_{ACn_{LV}} \tag{3.40}$$

$$\vec{V}_{HVWindingA} = \vec{V}_{ACn_{HV}} - \vec{V}_{BAn_{HV}} \tag{3.41}$$

$$\vec{V}_{HVWindingB} = \vec{V}_{BAn_{HV}} - \vec{V}_{CBn_{HV}} \tag{3.42}$$

$$\vec{V}_{HVWindingC} = \vec{V}_{CBn_{HV}} - \vec{V}_{ACn_{HV}} \tag{3.43}$$

Voltage transformers measure line-to-ground voltages in the Δ - Y connected Transformer simulation and contain an "n" in their subscript. The line-to-ground voltage measurement points, shown in Figure 3.23, are marked N1, N2, N3 on the primary side and NS1, NS2, NS3 on the secondary side. Polarity markings, shown on the linear transformer models, are indicated arrows.

3.6 Summary

The transformer model used to simulate inrush, in a real-time simulator, was developed in this chapter. First, a linear portion of a single phase transformer was developed. Then, the non-linear effect of the transformer's core was modeled. Finally the single phase transformer models were combined into a transformer bank. This transformer bank was used to test the relay prototype described in the latter portion of this chapter. The algorithm developed for the PIC32 microprocessor used to prototype the relay is described as well as the analog-to-digital converter used to digitize the real-time simulator's output. The transformer model and relay prototype were constructed for a Y-Y configured transformer and extended to a Δ - Y transformer. Data collected from the transformer model and prototype relay is analyzed in Chapter 4

Chapter 4

Full Negative Sequence Protection

4.1 Introduction

The test results gathered with a prototype executing the proposed transformer protection algorithm will be compared to a conventional current differential protection algorithm. These results were gathered for several scenarios: steady-state, energization, current transformer saturation, transformer over-excitation, and faulted conditions including the fault resistance. Results gathered for the proposed algorithm will be compared to differential relay results for a range of fault severities applied within each scenario. The development of turn-to-turn faults on the high-voltage side of the transformer and the low-voltage side of the transformer will also be examined. Unless otherwise stated, the impedance of the turn-to-turn fault was zero and the current transformer settings were as given in Table 3.2 in order to prevent current transformer saturation. This section begins with a check of accuracy of the prototype's analog-to-digital conversion system.

4.2 Analog-to-Digital Conversion System Accuracy Check of Prototype

All signals representing voltage and current were output by the real time simulator through analog output channels as described in Section 3.2.7. Before these signals could be processed by the relay, an analog-to-digital conversion process had to take place. This process had to preserve both the magnitude and phase of the incoming signal. In order to perform this accu-

racy check, the prototype system's normal operating currents and voltages were captured by a waveform capture routine written for the PIC32 microcontroller. Once captured, a discrete Fourier transform was performed on the waveforms in order to obtain their magnitude and phase. Waveform magnitudes were compared to expected values and a percent difference was obtained. Phase angle was verified by calculating the difference between Phase A and Phases B and C.

The magnitudes of the current and voltage signals did not vary by more than 4% with respect to their expected value with a variability not exceeding 1% across all twelve channels: six currents and six voltages. The phase varied by no more than 0.2° from the expected value across all twelve channels. This is well within the error limits established by the IEC for current transformers [69] which demands less than 5% error in current magnitude and less than 1° error in phase. In the time domain, normal operating currents are given in Figure 4.1 while normal operating voltages are given in Figure 4.2.

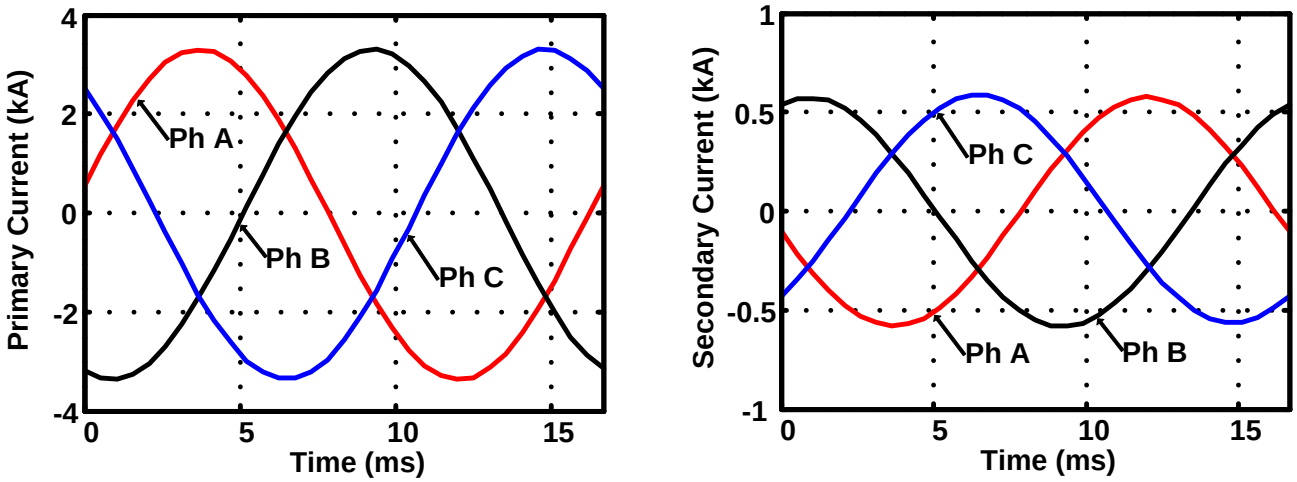

Figure 4.1: Normal Operating Currents

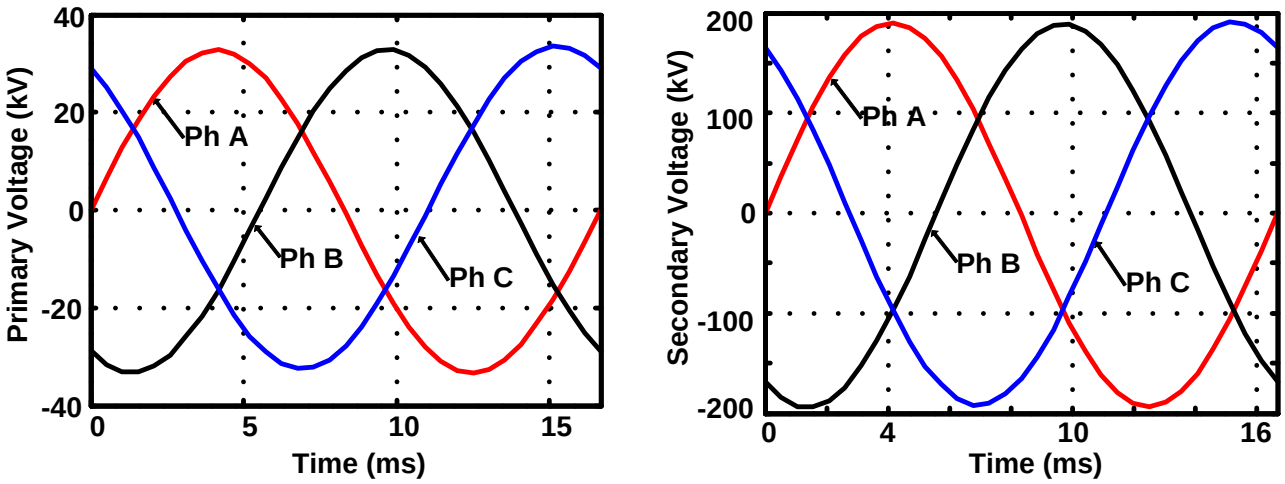

Figure 4.2: Normal Operating Voltages

4.3 Faults Occurring During Steady-State

4.3.1 High Voltage Winding Fault During Steady-State

The simulated system is considered to be in a steady state if it has been operating for a long time without changes to prevailing voltages and currents. This condition was observed in the system prior to the simulation of a fault. After data was collected, the relay and the simulator were reset in order to collect data at increasing severity of fault. Turn-to-turn faults involving 1%, 3%, 5%, 10%, 15%, 25% of the high voltage winding were simulated consecutively. Given these conditions, the proposed method detected faults involving 3% of the high voltage windings or more. The primary and secondary negative sequence current magnitudes are shown in Figure 4.3, along with the phase difference between the two currents. The trip signal issued by the algorithm is shown in the lower frame of Figure 4.3. The simulated fault occurred in phase C of the transformer.

The phase information displayed in Figure 4.3 warrants explanation. Prior to the fault's occurrence, the phase is undefined because the phasor's magnitude is too small for an accurate calculation of phase. Negative sequence phasor magnitudes were calculated using root mean square (RMS) line current. The negative sequence based relay did not pick up for

a 1% turn-to-turn fault since the negative sequence current magnitudes, generated due to the fault, were too low. However, it is obvious from Figure 4.4 that the negative sequence current magnitudes were large enough to allow for a phase measurement indicative of a fault.

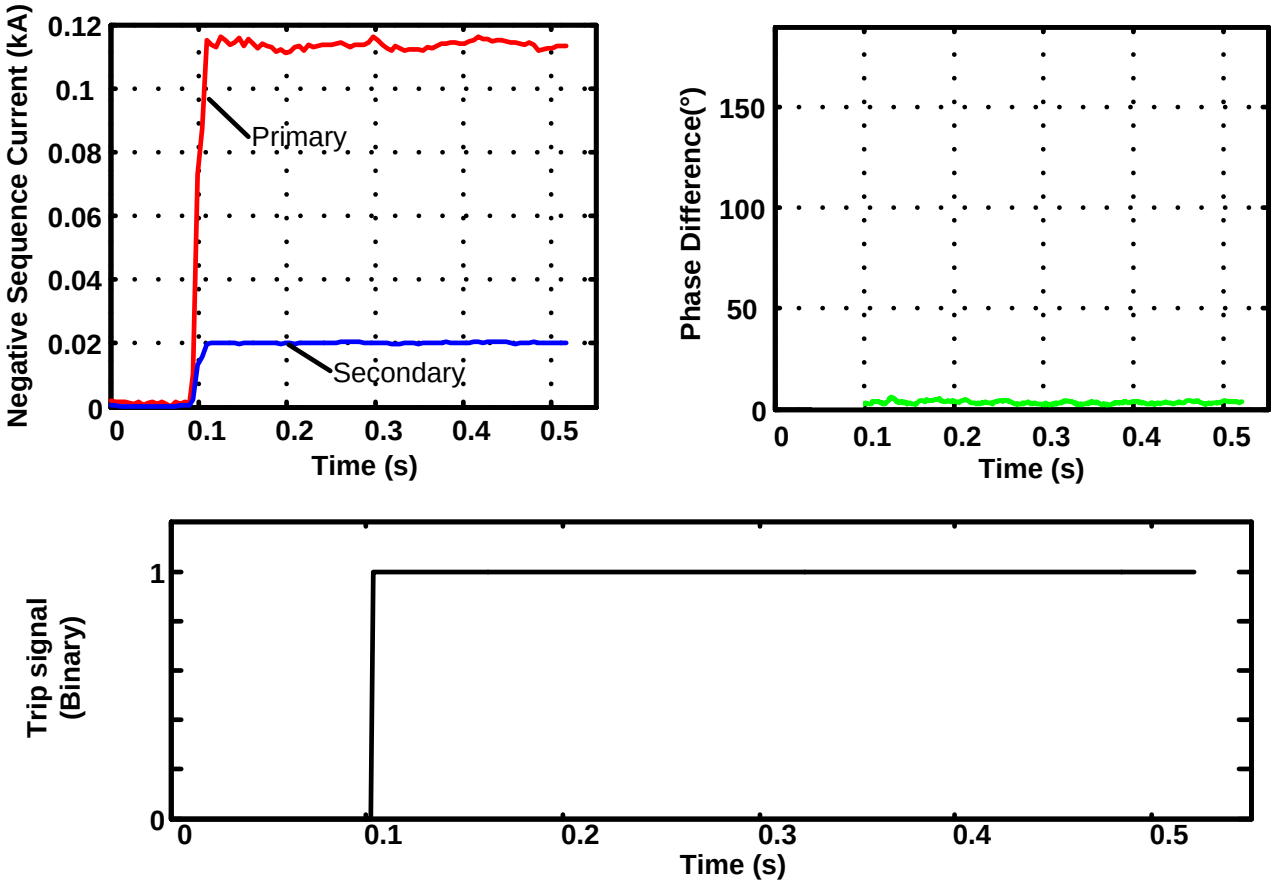

Figure 4.3: Proposed Algorithm: 3% Turn-to-Turn Fault, Steady-State

The differential algorithm picked up for a 10% turn-to-turn fault. The results depicted in Figure 4.5 show a differential current above the restraining current, for phase C, indicating a reliable trip signal is issued. Differential and restraining current data taken for Phases A and B, using the differential algorithm, indicated these phases were not affected by the turn-to-turn fault simulated in the phase C transformer. Since neither of these phases contributed to the relay's trip decision, differential data for phases A and B are not be shown.

The results obtained by [31] and [4] in the steady state scenario are confirmed for the differential algorithm. It did not pick up for faults less than 10%. The proposed algorithm

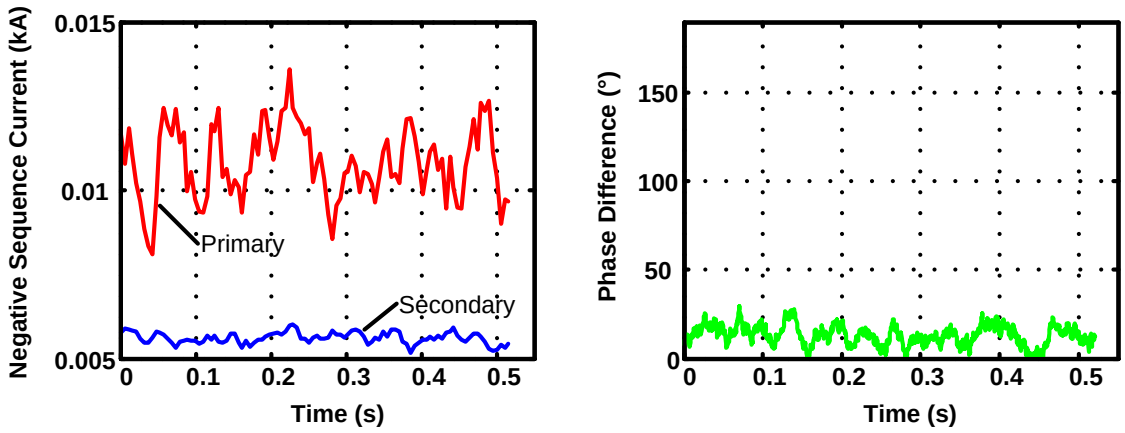

Figure 4.4: Proposed Algorithm: 1% Turn-to-Turn Fault TRIP Signal, Steady-State

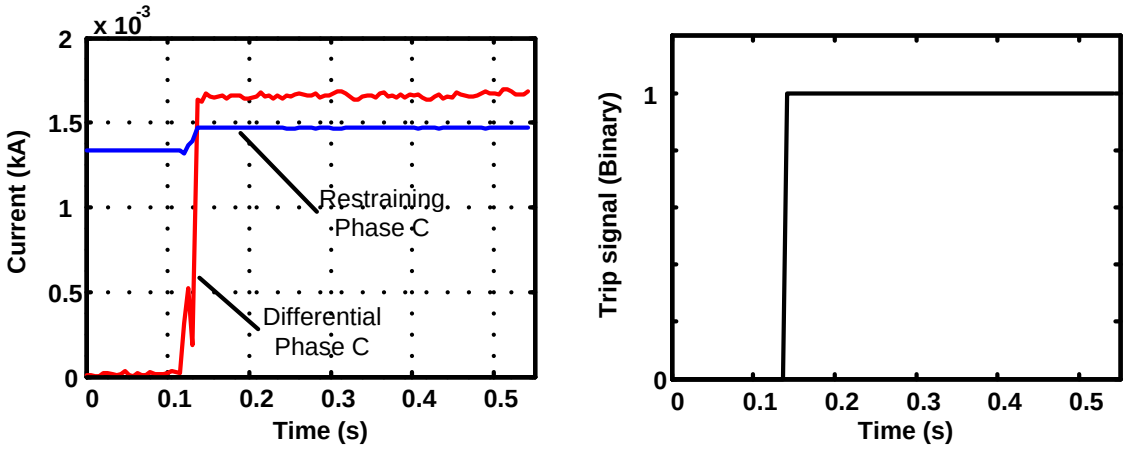

Figure 4.5: Differential Algorithm: 10% Turn-to-Turn Fault TRIP Signal, Steady-State

did not pick up a 1% turn-to-turn fault. On closer examination of the simulations performed in [31] it was discovered that the algorithm sensitivity was limited to detecting 3% turn-to-turn faults or larger. This is consistent with the proposed algorithm which was implemented in a relay prototype.

Reference [4] used both simulation and data logged during a turn-to-turn fault of an auto-transformer in order to confirm the sensitivity of the proposed algorithm during steady state. The simulations conducted in this work were completed using a transformer bank, not an auto-transformer. More investigation is required to determine how different types of transformers affects the sensitivity of this algorithm. To summarize, all faults involving 3%

or more windings were detected using the proposed algorithm. The differential algorithm detected all faults involving 10% or more windings. Both systems rejected bolted external faults. The system was in steady-state prior to the initiation of the fault simulation. Trip delay times for the proposed algorithm are given in Table 4.1 while the differential algorithm's trip delay time is given in Table 4.2.

% Turns Faulted	Trip Time (ms)
1	No Trip
3	11.98
5	15.10
10	11.46
15	10.42
25	9.38

Table 4.1: Neg. Sequence Algorithm: Steady-State, Fault on Phase C

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	21.35
15	20.31
25	19.79

Table 4.2: Differential Algorithm: Steady-State, Fault on Phase C

4.3.2 Low Voltage Winding Fault During Steady-State

It is unlikely for a fault to occur on the low voltage winding of a transformer [2], [1]. As discussed in Section 1.2, low voltage windings are thicker and consist of fewer turns. Low voltage windings are therefore better able to resist the magnetic forces they are subjected to due to their increased cross section and mass, making them less likely to twist or shift. Simulations involving low-voltage turn-to-turn faults are included to completely test the proposed algorithm. Low voltage winding faults, involving 3%, 10%, 15%, 25% of the low voltage windings, were performed.

As expected the negative sequence based protection algorithm detected faults involving 3% of the turns or more while the differential protection algorithm detected faults involving 10% of the windings or more. The real-time simulator was unable calculate a valid output given the impedance parameters associated with a 1% turn-to-turn fault on the low-voltage

side of the transformer. There were fewer turns on the low-voltage side of the transformer studied in this work than on the high voltage side. Therefore the real-time simulator was not able to generate output for the impedance matrix associated with a 1% turn-to-turn fault on the low-voltage side. Data collected for the scenario of turn-to-turn faults occurring on the low-voltage winding of the transformer is given in Tables 4.3 and 4.4.

% Turns Faulted	Trip Time (ms)
3	16.67
10	10.94
15	14.58
25	13.54

Table 4.3: Neg. Sequence Algorithm: Steady-State, Fault on Phase C LV Side

% Turns Faulted	Trip Time (ms)
3	No Trip
10	No Trip
15	340.63
25	19.27

Table 4.4: Differential Algorithm: Steady-State, Fault on Phase C LV Side

4.4 Faults Occurring During Transformer Energization

The method for the energization of the simulated transformer is described as follows: prior to energization no voltage existed across the primary and secondary terminals of the transformer, no currents flowed through the transformer's windings, and no remnant flux was present in the transformer core. Voltage was applied simultaneously to all three windings common to one side of the transformer, either the high-voltage windings or the low-voltage windings. The three windings opposite to the side of the transformer being energized were open-circuited for the duration of the simulation. Considering that turn-to-turn faults may occur on either the high-voltage side or the low voltage side, four possible combinations exist: low-voltage energization and high-voltage turn-to-turn fault, high-voltage energization and high-voltage turn-to-turn fault, low-voltage energization and low-voltage fault, and high-voltage energization and low-voltage fault. Though low-voltage turn-to-turn faults are unlikely to occur, these tests have been included in order to completely test the transformer model.

In order to simulate a high-voltage energization, a change must be made to the model shown in Figure 3.2 as it is built to model a low-voltage energization. According to [23], the saturating inductance used to model the non-linear core must be in parallel with the energizing source. Therefore, the saturating inductance model was attached to the side of the transformer that was being energized. Only the saturating inductance's voltage parameter was set to match the energization voltage, all other parameters remained unchanged.

4.4.1 High-Voltage Turn-to-Turn Fault During Low-Voltage Energization

Energization of a transformer gives rise to inrush current, a phenomena described in Section 1.4. Inrush current may result in erroneous tripping if its effect on the protection system is not taken into consideration. However, as discussed in Section 1.6.4 blocking may be undesirable as turn-to-turn faults are likely to occur during energization. In this subsection, all faults occurred on the high voltage side while energization took place on the low-voltage side.

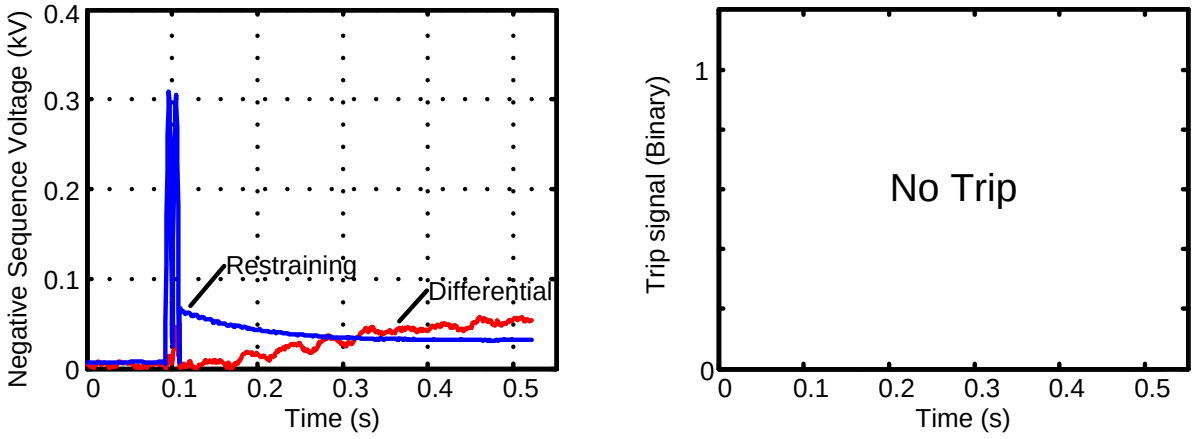

Figure 4.6: Proposed Algorithm: 1% Turn-to-Turn Fault TRIP Signal, Steady-State

A 1% turn-to-turn fault was not detected by the proposed negative sequence algorithm as shown in Figure 4.6. Though the differential negative sequence voltage moves above the restraining negative sequence voltage after approximately 0.2 seconds, the differential negative sequence voltage remains below the pickup voltage of 100 Volts. This blocks the

relay's operation. The sensitivity of this relay during inrush is consistent with the steady state results gathered in Section 4.3. The proposed negative sequence based algorithm detected all faults sustained to 3% of windings or more as shown in Figure 4.7. Both Figures 4.6 and 4.7 resulted from systems with a turn-to-turn fault located on the Phase C transformer and the peak inrush current occurring on phase A. Trip times varied with the number of turns involved in the fault and the fault's relationship to the phase experiencing the most severe inrush. This will be discussed in more detail later in this section. Inrush current severity and it's relationship to voltage is described in Section 1.4. All trip signal delays of the proposed algorithm were well below the trip times necessary to prevent a transformer tank rupture [2].

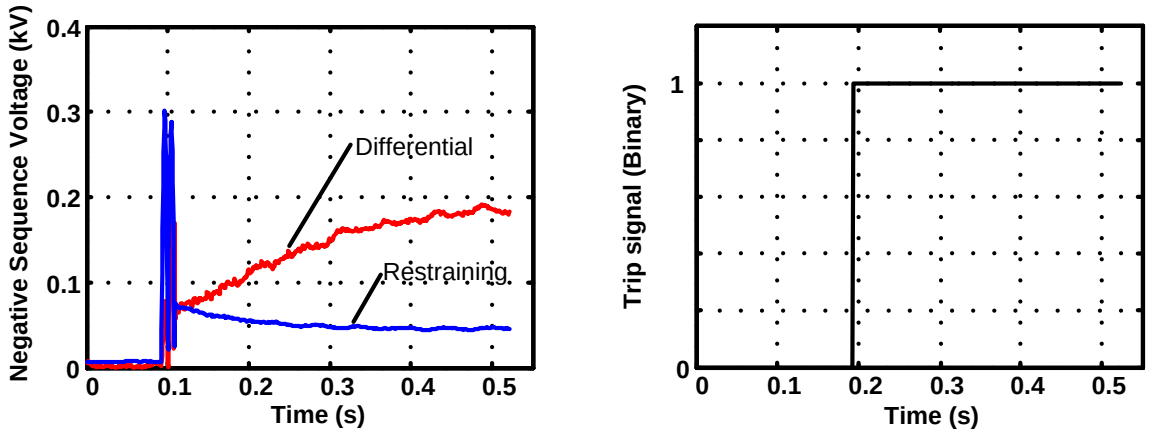

Figure 4.7: Proposed Algorithm: 3% Turn-to-Turn Fault TRIP Signal, Steady-State

The differential current algorithm becomes very sensitive during energization. This is obvious if $I'_S = 0$ is inserted into equations 1.17 and 1.18. This ensures that equation 1.19, the trip differential criteria, is always true. The second harmonic block criteria, described by equation 1.20, ensure no erroneous trip occurs during energization. When no turn-to-turn fault exists, the second harmonic content of the inrush current decays to zero at the same rate as the fundamental harmonic content of the inrush current, blocking the operation of the relay. A trip is signaled by the differential algorithm due to a 1% turn-to-turn fault, occurring in the phase C transformer, as show in Figure 4.8. The differential and restraining curves for Phases A and B tend to zero while the curves for Phase C tend to a non-zero

value due to the presence of a 1% turn-to-turn fault on Phase C.

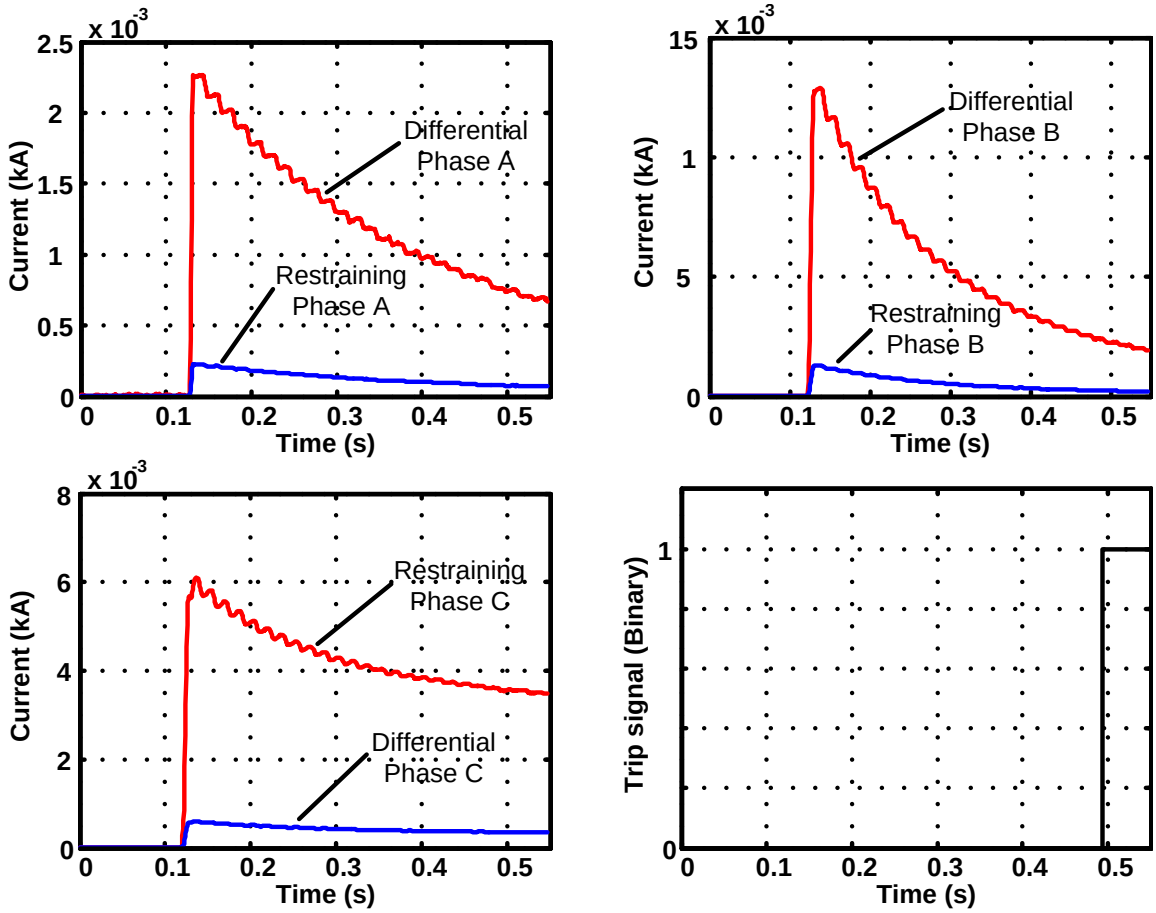

Figure 4.8: Differential Algorithm: 1% Turn-to-Turn Fault with Trip Signal, Severe Inrush on Phase B

% Turns Faulted	Trip Time (ms)
1	No Trip
3	102.08
5	35.42
10	21.35
15	21.35
25	19.27

Table 4.5: Neg. Sequence Algorithm: Inrush on Phase A, Fault on Phase C

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	177.60
15	263.54
25	74.48

Table 4.6: Differential Algorithm: Inrush on Phase A, Fault on Phase C

Due to second harmonic blocking, an unacceptable delay was introduced during severe turn-to-turn faults. Data taken during a 25% turn-to-turn fault on Phase A, with Phase A also experiencing the most severe inrush, is shown in Figure 4.9. The trip signal is delayed by 200ms. This delay is likely to result in a transformer tank rupture [2] if overpressure relays fail to operate. If the most severe inrush occurs on an unfaulted phase, as shown in Figure 4.9, the trip delay is reduced by approximately 140ms. The trip times for most severe inrush on phase A with turn-to-turn fault also on Phase A are given in Table 4.10. Data for a fault occurring on Phase C, with severe inrush on Phase A, is shown in Table 4.6.

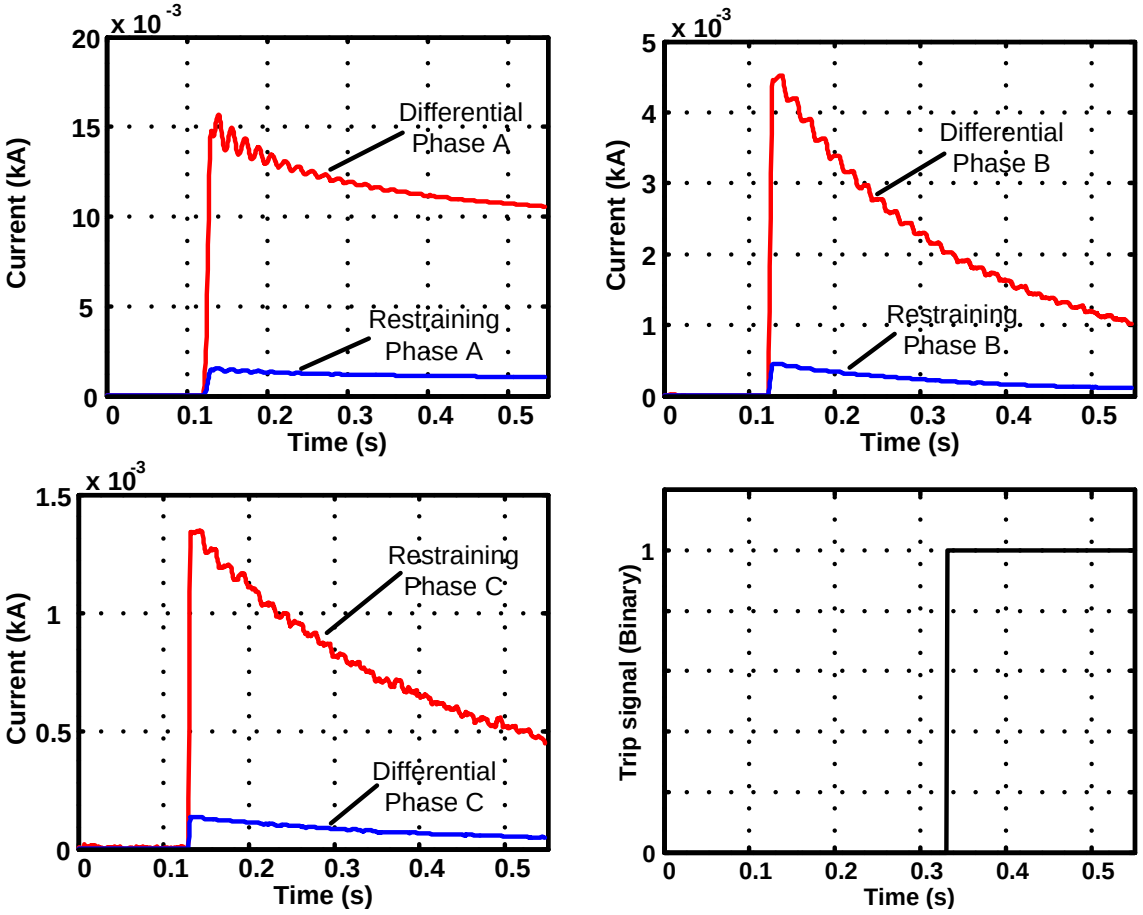

Figure 4.9: Differential Algorithm: 25% Turn-to-Turn Fault on Phase C, Severe Inrush on Phase A

In comparison, the negative sequence based algorithm showed no variation of trip time with severity of inrush, issuing a trip signal within 20ms of the fault occurring. This is shown

in Figure 4.10. The trip times for most severe inrush on phase A with turn-to-turn fault also on Phase A are given in Table 4.9. Data for a fault occurring on Phase C, with severe inrush on Phase A, is shown in Table 4.5. Since the negative sequence based algorithm is unaffected by which phase experiences the worst inrush current, the energization scheme will be chosen such that the differential current based algorithm performs with the shortest trip delay. Therefore energization was performed such that Phase A experienced the most severe inrush current while the turn-to-turn fault occurred in Phase C. For completeness, energization of the high-voltage windings with a low-voltage winding fault was also examined. These results are given in Tables 4.7 and 4.8. As discussed in Section 4.3.2, this type of fault scenario is unlikely.

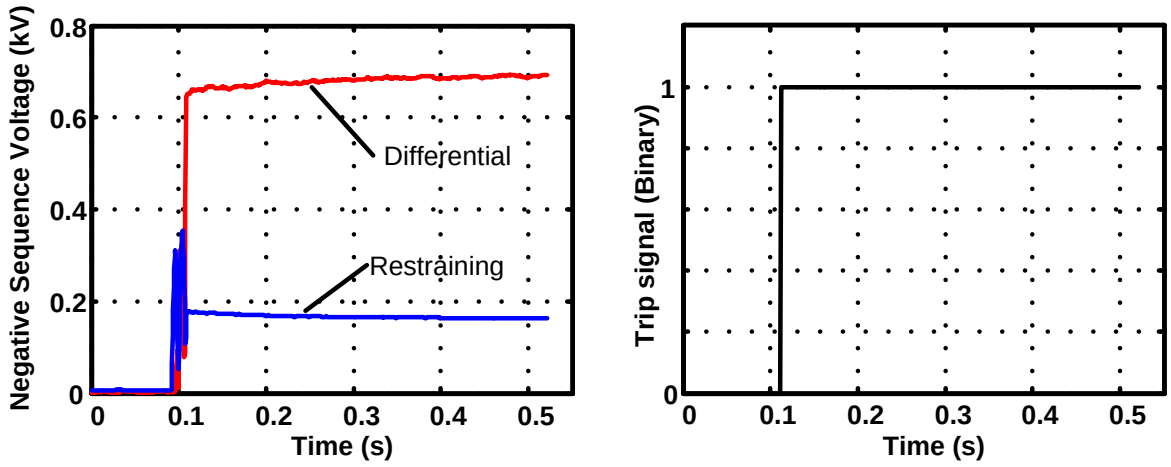

Figure 4.10: Neg Seq Algorithm: 25% Turn-to-Turn Fault on Phase A, Severe Inrush on Phase A

% Turns Faulted	Trip Time (ms)
3	21.35
10	21.88
15	21.88
25	19.27

Table 4.7: Neg. Sequence Algorithm: Inrush on HV Phase A, Fault on Phase C LV Side

% Turns Faulted	Trip Time (ms)
3	19.79
10	No Trip
15	No Trip
25	No Trip

Table 4.8: Differential Algorithm: Inrush on HV Phase A, Fault on Phase C LV Side

% Turns Faulted	Trip Time (ms)
1	No Trip
3	22.40
5	21.35
10	20.31
15	20.31
25	20.83

Table 4.9: Neg. Sequence Algorithm: Inrush on Phase A, Fault on Phase A

% Turns Faulted	Trip Time (ms)
1	122.92
3	No Trip
5	267.19
10	21.35
15	19.79
25	214.06

Table 4.10: Differential Algorithm: Inrush on Phase A, Fault on Phase A

4.4.2 High-Voltage Turn-to-Turn Fault During High-Voltage Energization

This subsection addresses the occurrence of a fault, along with energization, on the high-voltage side of the transformer. The data generated by the differential based relaying algorithm is given in Table 4.12. The proposed negative-sequence based relay did not pick up for any turn-to-turn faults, regardless of severity, as shown in Table 4.11 . This is not a flaw in the relay's algorithm. It highlights one of the limitations of the transformer model built to test the relay. In order to understand this phenomena, the linear transformer model must be examined in greater detail.

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	No Trip
15	No Trip
25	No Trip

Table 4.11: Neg. Sequence Algorithm: Inrush on HV Phase A, Fault on Phase C HV Side

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	No Trip
15	19.79
25	20.83

Table 4.12: Differential Algorithm: Inrush on HV Phase A, Fault on Phase C HV Side

As discussed in Section 1.2.1 if the high-voltage windings of a transformer are shorted, they no longer contribute to the production of flux. The shorting of high-voltage turns effectively reduces the transformer's winding ratio. This decreases the transformer's turns ratio, decreasing the voltage in the phase affected by the turn-to-turn fault. This is a magnetic phenomena that is not considered by the transformer model constructed for this work. The transformer simulation model that may be constructed for use in the real-time simulator [49] uses an equivalent circuit which includes a ratio changer which calculates the secondary voltage based on the primary voltage. The implications of this ratio changer is best described with the aid of Figure 3.3. Recall that the secondary windings of this transformer is composed of three windings connected in series, allowing winding #4 to be shorted in order to simulate a turn-to-turn fault. This reduces the overall windings impedance of the secondary side but does not affect the voltage of winding #1, the primary winding. Its voltage is calculated by the ratio changer which uses the voltage across the entire secondary winding. Therefore, a short across winding #4 will cause an increase in current to flow on the secondary side of the transformer but it will not cause a change in the voltage seen across the terminals of the primary and secondary sides of the transformer. This theory is supported by the voltage wave forms collected during a high-voltage side energization with a high-voltage side turn-to-turn fault shown in Figure 4.11. The voltage plots shown in

Figure 4.11 have been scaled with the transformer's ratio in order to make the waveforms easier to compare.

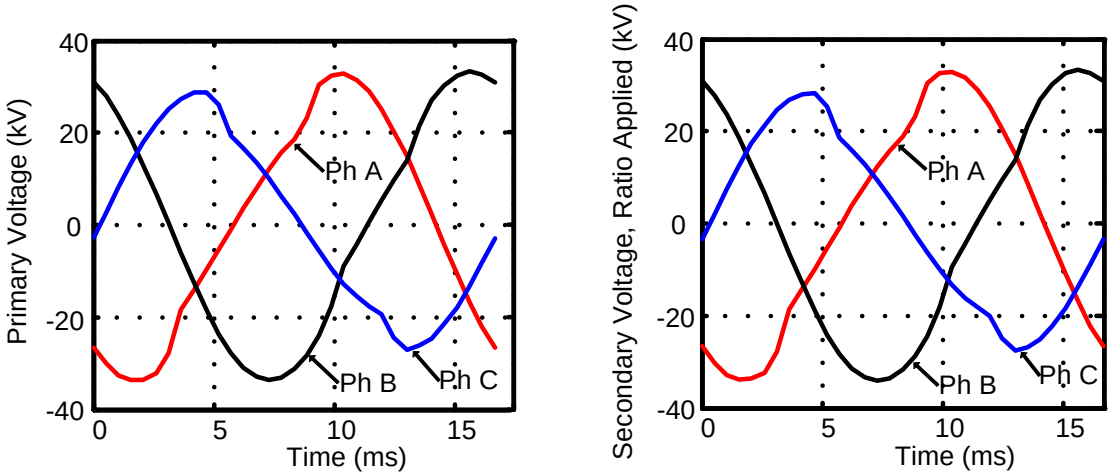

Figure 4.11: 25% Turn-to-Turn Fault on HV Phase C, Inrush on HV Phase A

A fault present on the low-voltage side of the transformer during a low-voltage energization produced similar data. Table 4.13 provides results obtained using the proposed algorithm. It showed that no turn-to-turn fault was detected regardless of severity. The reason for this apparent lack of sensitivity is described above for turn-to-turn faults present on the high-voltage side of the transformer during high-voltage energization. Table 4.14 gives trip times observed with the differential algorithm.

% Turns Faulted	Trip Time (ms)
3	No Trip
10	No Trip
15	No Trip
25	No Trip

Table 4.13: Neg. Sequence Algorithm: Inrush on LV Phase A, Fault on Phase C LV Side

% Turns Faulted	Trip Time (ms)
3	No Trip
10	178.65
15	85.94
25	19.79

Table 4.14: Differential Algorithm: Inrush on LV Phase A, Fault on Phase C LV Side

4.5 Current Transformer Saturation

A current transformer (CT) model was used to simulate the effect of CT saturation. The CT model is described in detail in Section 3.2.4. In order to ensure saturation, the CT burden was changed to the values given in Table 3.3. With this new, higher burden resistance, the tests described in Section 4.3.2 were repeated. The negative sequence based relay performed well, detecting turn-to-turn faults occurring in phase C of the transformer, involving 1% to 25% of the windings. More distortion occurs in the phase difference as can be seen in Figure 4.12, as predicted in [4]. Despite the distortion, the phase is well below the trip criteria of 60°. When Figure 4.12 is compared to Figure 4.4, it is clear that CT saturation increases the negative sequence current magnitude to a value above the detection threshold, allowing a 1% turn-to-turn fault to be detected. Trip delay times for the proposed algorithm are tabulated in Table 4.15. When this trip time data is compared to trip times without CT saturation, given in Table 4.1, it is clear that increased sensitivity to turn-to-turn faults comes at a price. The trip signal is delayed by 1.6 ms for a 15% fault, while the 25% fault is delayed by 0.5ms. All faults studied in this subsection occurred in the high-voltage windings of the transformer. The effect of a burden was not considered under energization conditions since the proposed negative sequence based algorithm utilizes line voltage data instead of line current data during energization.

% Turns Faulted	Trip Time (ms)
1	15.63
3	11.46
5	12.50
10	10.94
15	11.98
25	9.90

Table 4.15: Neg. Sequence Algorithm: 4.56 Ω CT Burden

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	21.35
15	20.31
25	No Trip

Table 4.16: Differential Algorithm: 4.56 Ω CT Burden

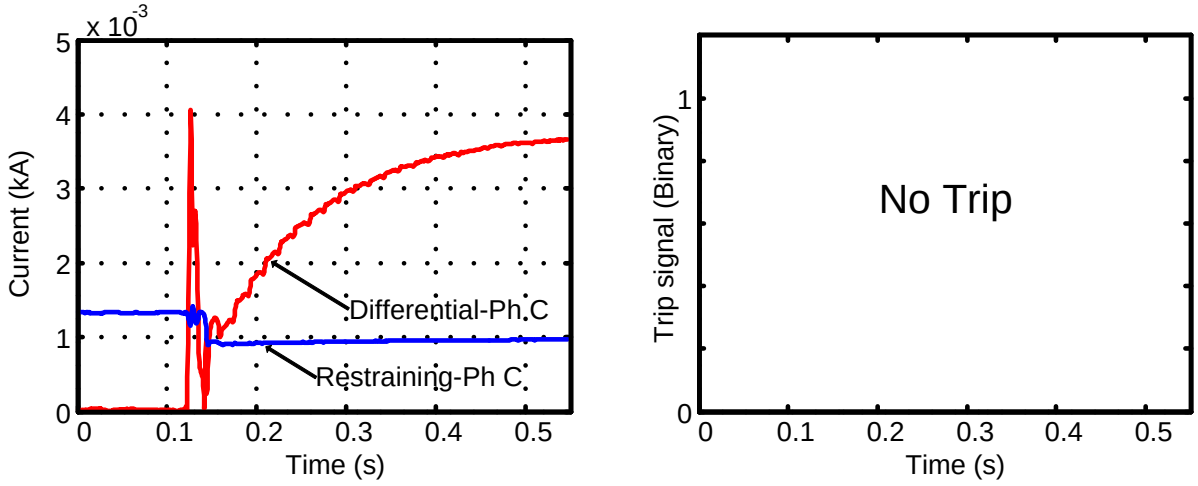

Figure 4.13: Differential Algorithm: 25% Turn-to-Turn Fault with 4.56Ω CT burden

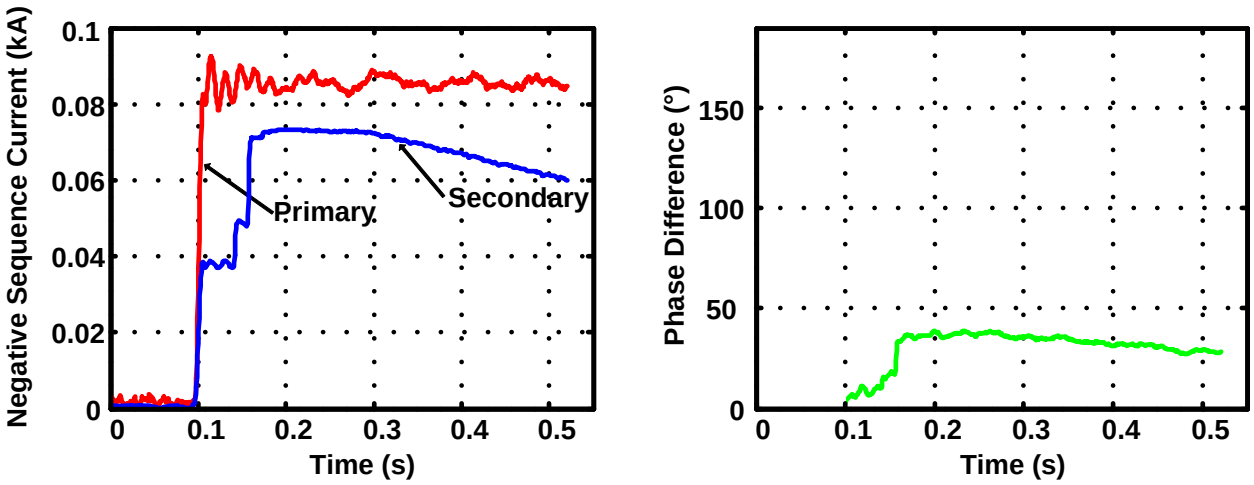

Figure 4.12: Proposed Algorithm: 1% Turn-to-Turn Fault with 4.56Ω CT burden

The differential relay performed poorly with the increased CT burden resistance. Trip delays were experienced for turn-to-turn faults involving 10% and 15% of the windings. The 25% turn-to-turn fault was not detected within an acceptable amount of time [2] as shown in Figure 4.13. This was due to the second harmonic current generated by the saturating CT, causing the differential relay to be blocked by the second harmonic restraint. The trip times obtained with the differential algorithm are tabulated in Table 4.16.

4.6 Fault Resistance

As described in Section 3.2.8 faults between windings are rarely bolted. In other words, turn-to-turn faults typically have a resistance. For the following simulations, a fault having a constant resistance of 1Ω was applied to the high voltage winding of the Phase C transformer. The effect of fault resistance was studied under both energization and steady-state conditions.

4.6.1 1Ω Turn-to-Turn Fault Resistance During Steady-State

During steady-state, the negative sequence based algorithm detected faults involving 3% of the high-voltage windings or more. Trip times, tabulated in Table 4.17 may be compared to Table 4.1. Compared to a bolted turn-to-turn fault, a 1Ω fault resistance caused a 10.4 ms delay in detection of a 3% turn-to-turn fault. The 25% fault detection was delayed by 0.5 ms. Trip delay times observed for the differential relay, with a turn-to-turn fault resistance of 1Ω, are given in Table 4.18. Differential trip times for 15% and 25% turn-to-turn fault were delayed by more than 9 ms when compared to the negative sequence based relay. When compared to trip delay data for a bolted fault, shown in Table 4.2, the inclusion of a fault resistance delayed tripping by 0.5 ms for 15% and 25% turn-to-turn faults.

% Turns Faulted	Trip Time (ms)
1	No Trip
3	22.40
5	16.15
10	15.10
15	11.46
25	9.90

Table 4.17: Neg. Sequence Algorithm: 1 Ω Fault Resistance

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	No Trip
15	20.83
25	20.31

Table 4.18: Differential Algorithm: 1 Ω Fault Resistance

4.6.2 1Ω Turn-to-Turn Fault Resistance During energization

Significant trip delays were introduced as a result of the 1Ω fault resistance. Figure 4.14 shows a 234 ms trip delay for a 3% turn-to-turn fault occurring during energization. But as can be seen in Table 4.19, the trip delay decreased remarkably with the 5% turn-to-turn fault and almost vanished for the 10% turn-to-turn fault. In comparison, the differential algorithm shows a 328 ms trip delay for a 10% turn-to-turn fault during energization as shown in Figure 4.15. As can be seen in Table 4.20, this trip delay improves slowly with increasing fault severity. As per reasoning outlined in Section 4.4.2 the most severe inrush occurred on Phase A while the turn-to-turn fault occurred on Phase C.

% Turns Faulted	Trip Time (ms)
1	No Trip
3	233.85
5	78.13
10	21.35
15	15.63
25	19.27

Table 4.19: Neg. Sequence Algorithm: 1 Ω Fault Resistance during Energization

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	328.13
15	244.27
25	20.31

Table 4.20: Differential Algorithm: 1 Ω Fault Resistance during Energization

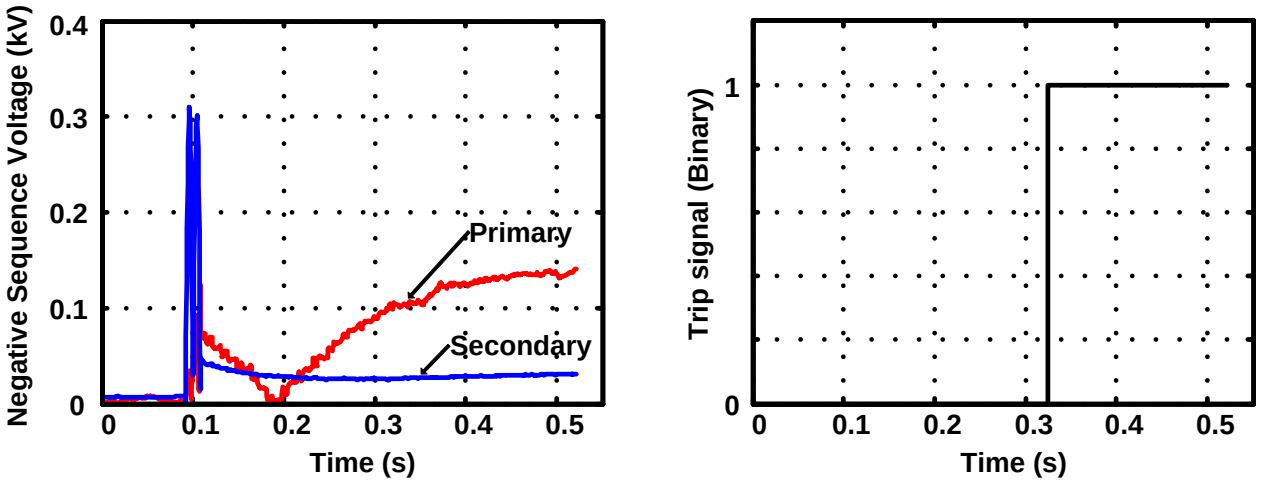

Figure 4.14: Proposed Algorithm: 3% Turn-to-Turn Fault with 1Ω Fault Resistance, Inrush

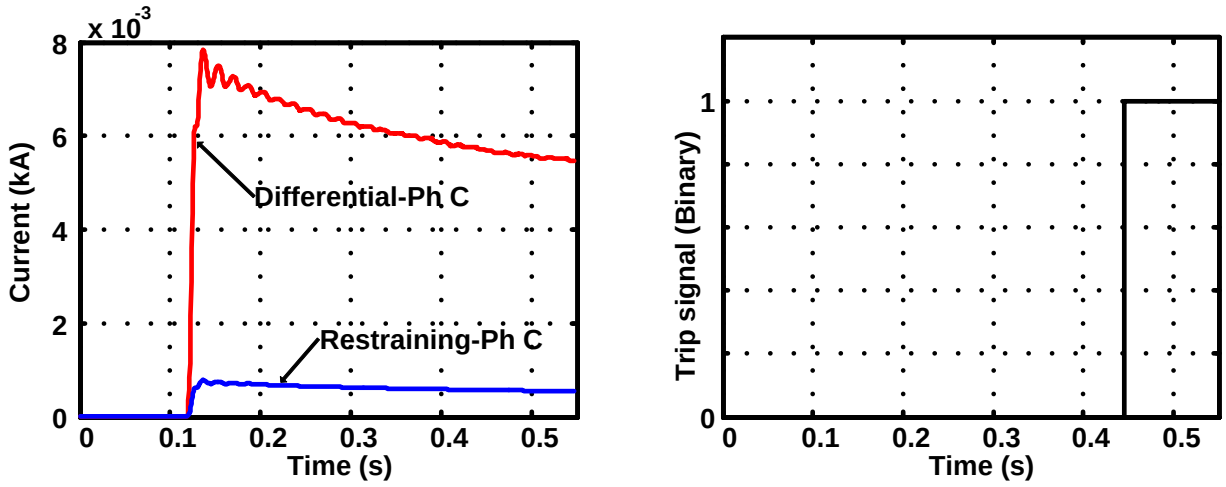

Figure 4.15: Differential Algorithm: 10% Turn-to-Turn Fault with 1Ω Fault Resistance, Inrush

Turn-to-turn faults occurring during energization contribute to the decay of second harmonic current [38]. As turn-to-turn fault resistance increases, the fault has a decreased impact on the currents and voltages observed at the transformer's terminals, meaning second harmonic current decays more slowly. Therefore, the differential relay's second harmonic block will act for a longer period of time. Since the negative sequence based relay does not depend on a second harmonic block during energization, it is able to react much faster to a turn-to-turn of non-zero resistance occurring during energization.

4.7 Transformer Over-excitation

As described in Section 1.5, the proposed algorithm must be tested to withstand an over-excitation of at least 110% of rated voltage. The transformer's primary current in an over-excited state is shown in Figure 4.16. From this figure it is evident that a primary voltage of 47.89 kV (line-to-line) is sufficient to cause significant over-excitation. This voltage, which simulates an over-excitation of 120%, was used to test both the proposed algorithm and the current differential algorithm during turn-to-turn fault conditions. An external line-to-ground fault on phase C (secondary) was also simulated. Neither algorithm mal-operated under external fault conditions. The effect of over-excitation of a Y-Y transformer, during steady-state and during energization, will be examined in the following subsections 4.7.1 and 4.7.2.

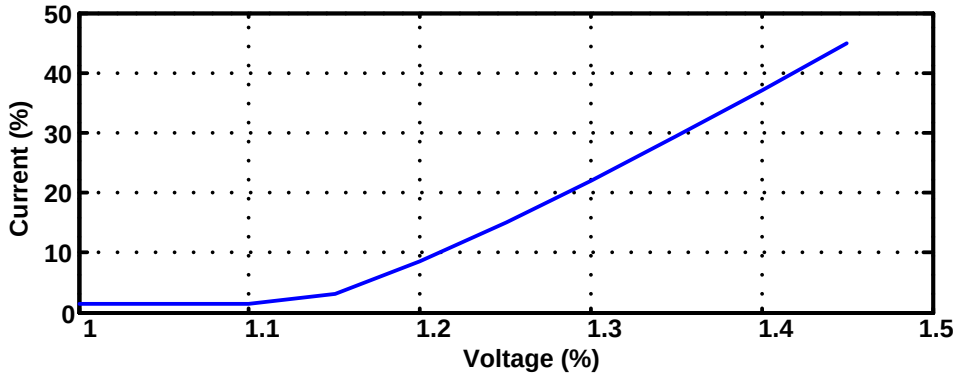

Figure 4.16: Current Over-Excitation on Primary

4.7.1 120% Over-excitation During Steady-State

Trip times collected at 120% overexcitation, as shown in Table 4.23, may be compared to trip times collected at rated voltage as given in Table 4.1. The proposed algorithm was able to detect 1% turn-to-turn faults in the over-excited transformer since the negative sequence currents on both the primary and secondary sides of the transformer were above the minimum threshold. The negative sequence phase difference showed a trip in both cases. The differential algorithm trip signal, given in Table 4.24, was delayed due to the

transformer's over-excited state. Upon examining the decision curves it is clear that the current transformers were severely saturated. Decision curves for a 15% turn-to-turn fault are shown in Figure 4.17. 10% and 25% turn-to-turn faults were not detected within 500 milli-seconds. The differential algorithm appeared to be more sensitive to smaller faults as a 5% turn-to-turn fault was detected.

% Turns Faulted	Trip Time (ms)
1	13.02
3	11.46
5	11.46
10	15.10
15	9.90
25	9.38

Table 4.21: Neg. Sequence Algorithm: Y-Y Transformer: 120% Over-Excitation

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	100.52
10	No Trip
15	339.06
25	No Trip

Table 4.22: Differential Algorithm:Y-Y Transformer: 120% Over-Excitation

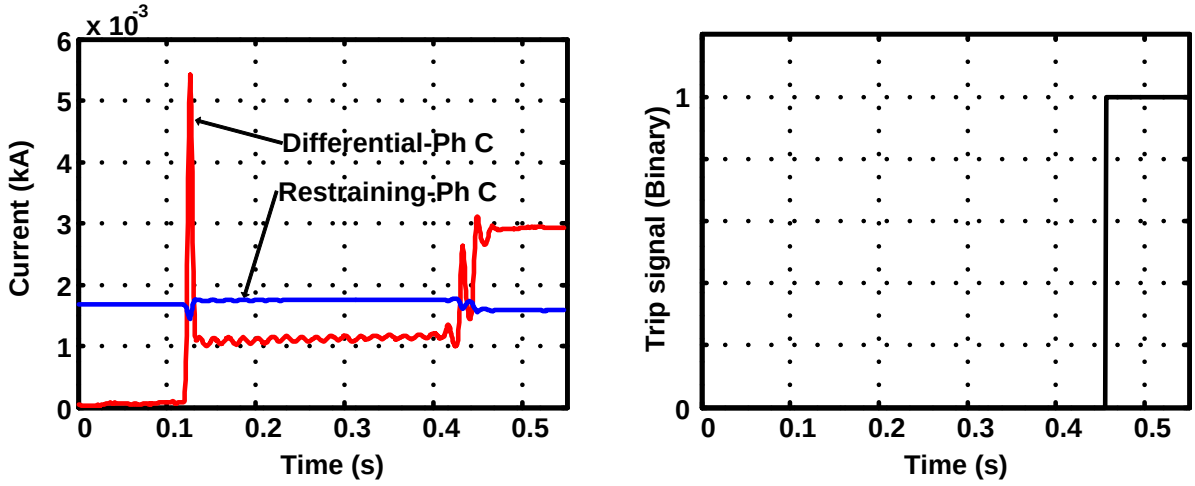

Figure 4.17: Differential Algorithm: 15% Turn-to-Turn Fault with 120% Over-Excitation

4.7.2 120% Over-excitation During Inrush

Energization occurred on the primary side in all cases described in this subsection with the most severe inrush occurring on phase A. In comparing trip times for energization at rated excitation voltage given in Table 4.5 with trip times for energization of a 120% over-excited transformer given in Table 4.23, there is little difference in trip times for most fault severities. Only the 3% turn-to-turn fault was detected 16ms faster in the over-excited case.

% Turns Faulted	Trip Time (ms)
1	No Trip
3	86.46
5	35.94
10	21.35
15	17.71
25	18.75

Table 4.23: Neg. Sequence Algorithm: Y-Y Transformer: 120% Over-Excitation and Inrush

% Turns Faulted	Trip Time (ms)
1	302.60
3	428.13
5	377.60
10	294.79
15	228.13
25	20.83

Table 4.24: Differential Algorithm:Y-Y Transformer: 120% Over-Excitation and Inrush

The differential algorithm appears sensitive to even 1% turn-to-turn fault, if overexcited by 120% of rated voltage, as shown in Table 4.24. While this appears to be an improvement in sensitivity over the transformer operating at rated excitation, given in Table 4.6, the differential relay was much slower in detecting turn-to-turn faults during energization when compared to the negative sequence based algorithm. In comparing Tables 4.23 and 4.24, only a 25% turn-to-turn fault was detected with comparable speed using either the differential algorithm or the negative sequence algorithm.

4.8 $\triangle$ - Y Transformer

As discussed in Section 3.5, the Δ - Y Transformer configuration is the most common winding connection in use today. Therefore any new protection algorithm must be tested with such a winding configuration. The negative sequence algorithm performed well, detecting faults involving 1% of the winding during steady state, as shown in Figure 4.18. Table 4.25 shows acceptable trip times for all fault levels simulated. The differential current based algorithm did not detect the fault, as shown in Table 4.26, until 10% of the windings had become involved. During energization, the negative sequence algorithm performed consistently faster than the current differential algorithm as shown in Table 4.27. The proposed algorithm's trip signal was issued 93 ms after a 5% turn-to-turn fault had occurred where as a 3% turn-to-turn fault was detected within 22 ms. This phenomena is discussed later in this chapter.

% Turns Faulted	Trip Time (ms)
1	18.23
3	19.79
5	15.10
10	13.02
15	13.02
25	9.90

Table 4.25: Neg. Sequence Algorithm: Δ-Y Transformer, Steady-State, Fault on Phase C

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	20.83
15	18.75
25	17.19

Table 4.26: Differential Algorithm:Δ-Y Transformer, Steady-State, Fault on Phase C

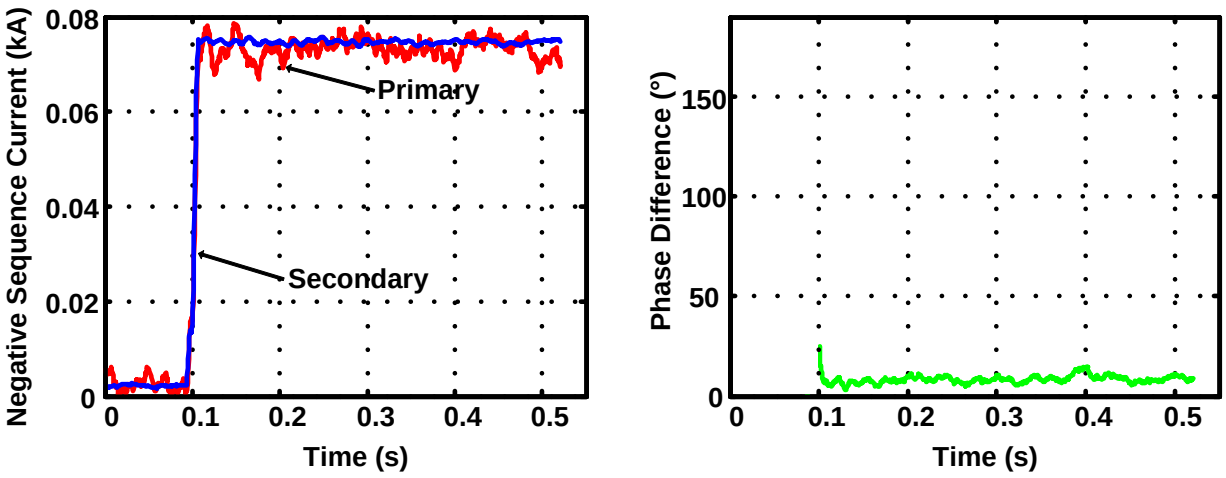

Figure 4.18: Proposed Algorithm: 1% Turn-to-Turn Fault with Δ - Y Transformer, Steady-State

% Turns Faulted	Trip Time (ms)
1	276.04
3	21.88
5	93.23
10	34.90
15	15.10
25	20.31

Table 4.27: Neg. Sequence Algorithm: Δ-Y Transformer, Energization, Fault on Phase C

% Turns Faulted	Trip Time (ms)
1	No Trip
3	361.46
5	385.42
10	119.79
15	78.65
25	16.15

Table 4.28: Differential Algorithm: Δ-Y Transformer, Energization, Fault on Phase C

In comparison the differential algorithm showed significant delays in issuing a trip signal, as shown in Table 4.28, when compared to the proposed algorithm shown in Table 4.27. With the CT ratio on the primary side of the transformer doubled, as shown in Table 3.6, neither of the algorithms tripped during external fault.

The negative sequence algorithm was found to be more vulnerable to CT saturation in the Δ - Y winding configuration than the differential algorithm. When the simulation

was conducted with the CT ratios as given in Table 3.3, the proposed algorithm tripped erroneously for an external fault located on the high-voltage side of Phase C. These CT ratios had been selected for the Y - Y winding configuration. Therefore, care must be exercised in selecting current transformer ratios to suit the winding configuration. As shown in Figure 4.19, CT saturation caused the phase difference to fall below 60° for 29 samples. Erroneous tripping should have been eliminated when the CT ratio on the low voltage side was doubled accounting for the $\sqrt{3}$ increase in current, resulting from the winding configuration changing from Y - Y to Δ - Y. Trip signal time data for this CT configuration is given in Table 4.25.

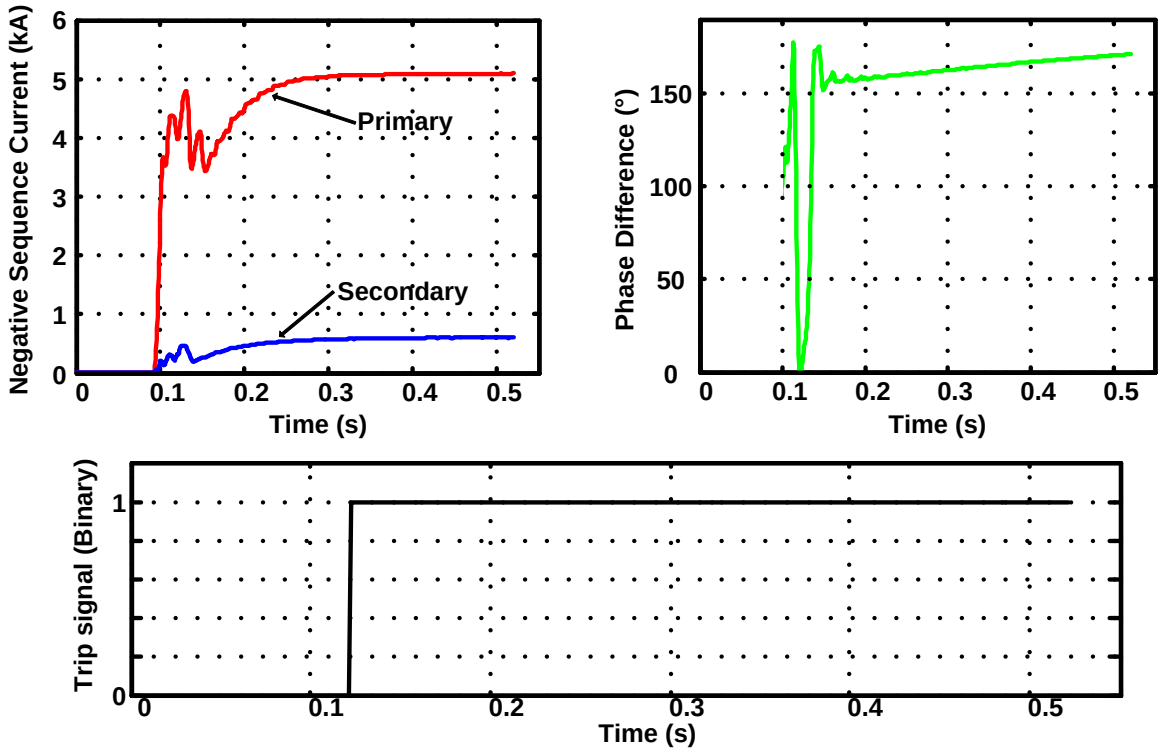

Figure 4.19: Proposed Algorithm: External fault, LV CT ratio 300

A CT ratio of 600 on the primary (Low Voltage) side improved the reliability of the proposed algorithm but it did not prevent tripping for heavy external faults. The CT ratio on the secondary side of the transformer had to be increased from 50 to 100 as well in order to prevent erroneous tripping. This is a deficiency of the proposed negative sequence algorithm since the CT sizing procedure, outlined in Subsection 3.2.4, specifies a secondary CT ratio

of 50. Figure 4.20 shows the worst phase disturbance, for an external line-to-ground fault given a primary CT ratio of 600 and secondary CT ratio of 100, seen during 12 trials, none of which resulted in an erroneous trip.

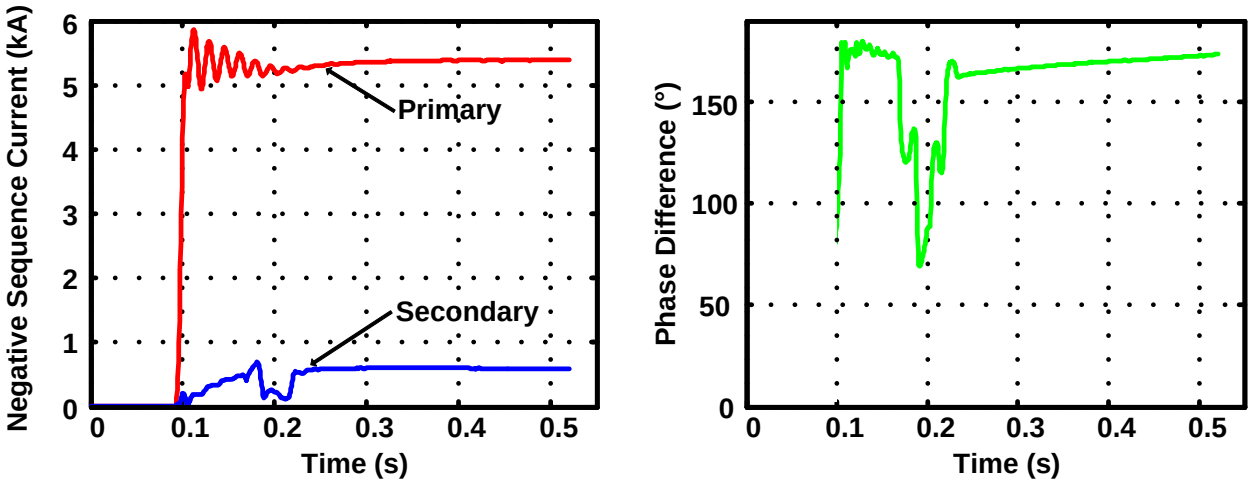

Figure 4.20: Proposed Algorithm: External fault, LV CT ratio 600 and HV CT ratio 100

During energization, protection parameters are derived from the magnitude of negative sequence voltage present on the primary and secondary sides of the transformer. The proposed algorithm was sensitive enough to detect 1% turn-to-turn faults. Trip times for all fault severities tested are given in Table 4.27. Results for a 3% turn-to-turn fault require closer examination. It appears that a 3% fault is detected significantly faster than a 5% turn-to-turn fault. From the negative sequence differential and restraining voltages shown in Figure 4.21, it is clear that the differential voltage briefly rises above the restraining voltage before dipping below the restraining voltage again. The differential voltage rises above the restraining voltage at 150ms. At this time, the trip criteria is definitive as the differential curve remains above the restraining curve.

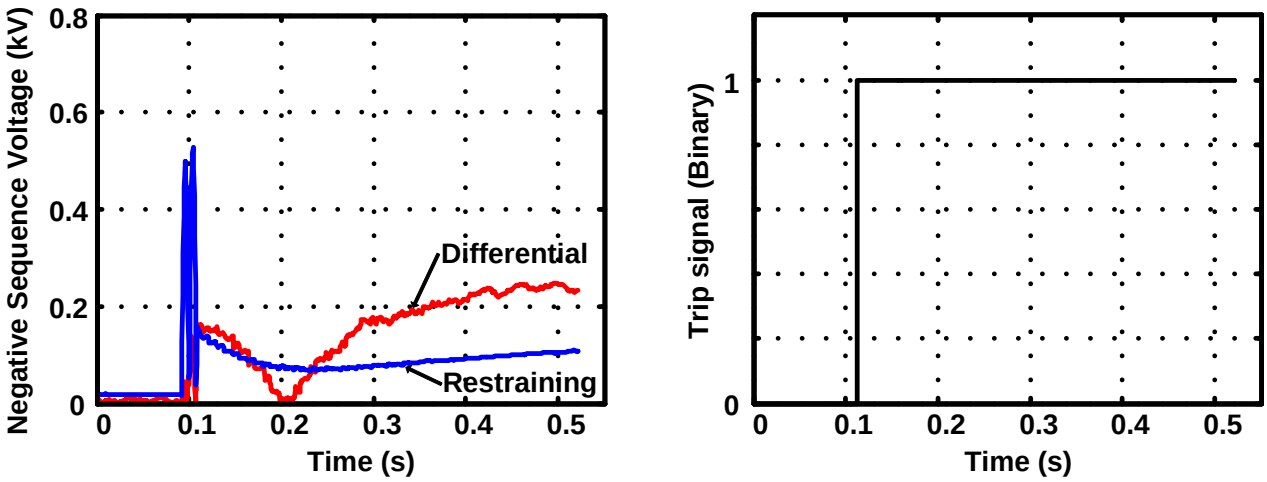

Figure 4.21: Proposed Algorithm: 3% during Energization

4.8.1 Δ - Y Transformer under 115% Over-Excitation

A Δ - Y transformer with 120% over-excitation on the primary side, protected by the proposed algorithm, resulted in an erroneous trip when subjected to an external line-to-ground fault on phase C. After reducing the transformer's excitation to 115% of its rated voltage, no erroneous trips were observed due to external line-to-ground faults. This reduction to 115% over-excitation was acceptable since, as discussed in Section 1.5, a transformer is rated to withstand a continuous 110% over-excitation voltage.

Table 4.29 shows the trip times for a Δ - Y connected transformer with 115% over-excitation on the primary side. These results are very similar to the Y-Y connected transformer. During energization, the proposed algorithm was less sensitive to faults involving 5% of the windings when compared to the Y-Y configured transformer with 120% over-excitation as shown in Table 4.31. The differential algorithm, applied to a transformer configured with 115% over-excitation on the primary side, detected faults involving more than 15% of the windings as shown in Table 4.30. The differential algorithm's response, during energization of the Δ - Y transformer, compares well to the algorithm's response to the Y-Y configured transformer with 120% over-excitation as shown in Table 4.32.

% Turns Faulted	Trip Time (ms)
1	18.75
3	11.46
5	11.46
10	13.02
15	9.90
25	8.85

Table 4.29: Neg. Sequence Algorithm: Δ-Y Transformer: 115% Over-Excitation

% Turns Faulted	Trip Time (ms)
1	No Trip
3	No Trip
5	No Trip
10	No Trip
15	19.27
25	19.79

Table 4.30: Differential Algorithm: Δ-Y Transformer: 115% Over-Excitation

% Turns Faulted	Trip Time (ms)
1	No Trip
3	91.67
5	68.75
10	21.35
15	16.15
25	20.83

Table 4.31: Neg. Sequence Algorithm: Δ-Y Transformer: 115% Over-Excitation and Inrush

% Turns Faulted	Trip Time (ms)
1	333.33
3	401.56
5	381.25
10	295.31
15	18.23
25	53.65

Table 4.32: Differential Algorithm: Δ-Y Transformer: 115% Over-Excitation and Inrush

4.9 Effect of Coupling Capacitor Voltage Transformer (CCVT)

During energization the inrush current creates voltage harmonics due to the source's impedance. The voltage data displayed in Figure 4.22 were observed during the low-voltage side energization of a Δ - Y Transformer. Clearly harmonics are present in this waveform as its

shape is not purely sinusoidal. The effect of these harmonics can be observed by comparing Tables 4.27 and Tables 4.33. The inclusion of the CCVT causes the 1% turn-to-turn fault to go undetected while the trip times for other faults are reduced significantly for most fault severities.

% Turns Faulted	Trip Time (ms)
1	No Trip
3	20.83
5	67.19
10	25.00
15	23.44
25	6.25

Table 4.33: Neg. Sequence Algorithm: Δ-Y Transformer, Energization, Fault on Phase C, with CCVT

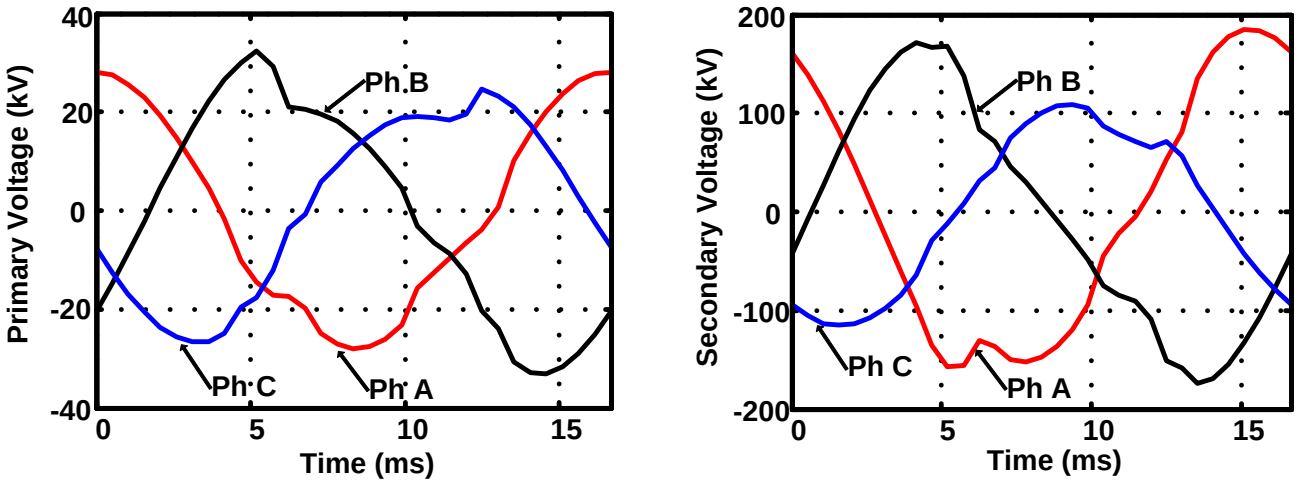

Figure 4.22: Voltages During Energization, Source Imp 1.6Ω

Oscillations in the negative sequence voltage signals are the cause of this change in trip time. The most significant reduction in trip time occurs for a fault involving 25% of the turns on the high voltage side of the phase C transformer as shown in Figure 4.23. This increased sensitivity comes at a price. The risk of false tripping is increased. Figure 4.24

shows the operation of the proposed algorithm during inrush for a healthy transformer. The oscillations bring the negative sequence differential voltage very close to the negative sequence restraining voltage for the first 250ms following energization. These oscillations also occur when the system is subjected to external faults.

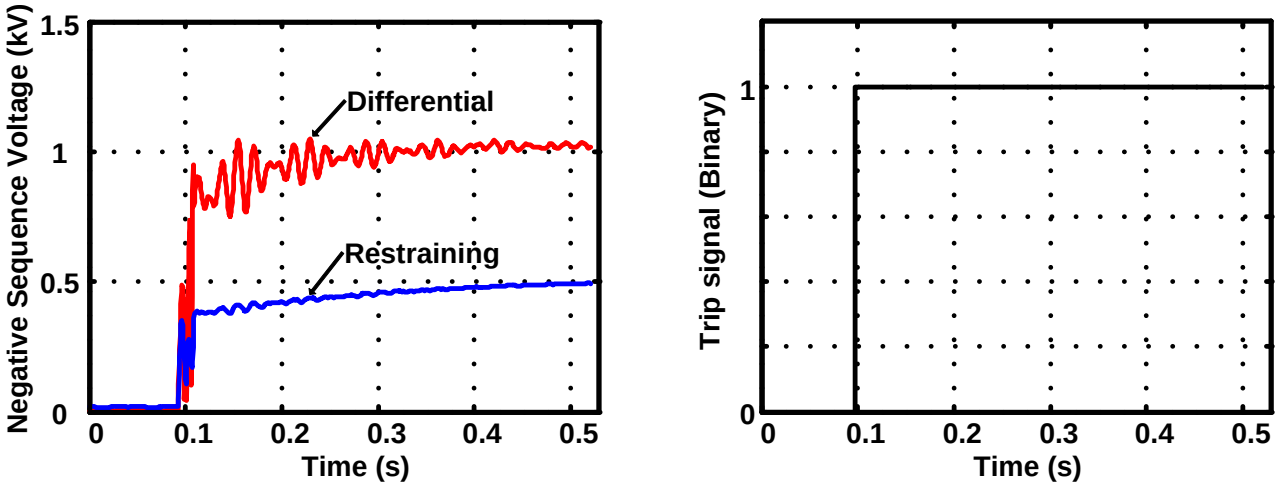

Figure 4.23: Proposed Algorithm: 25% during Energization with CCVT

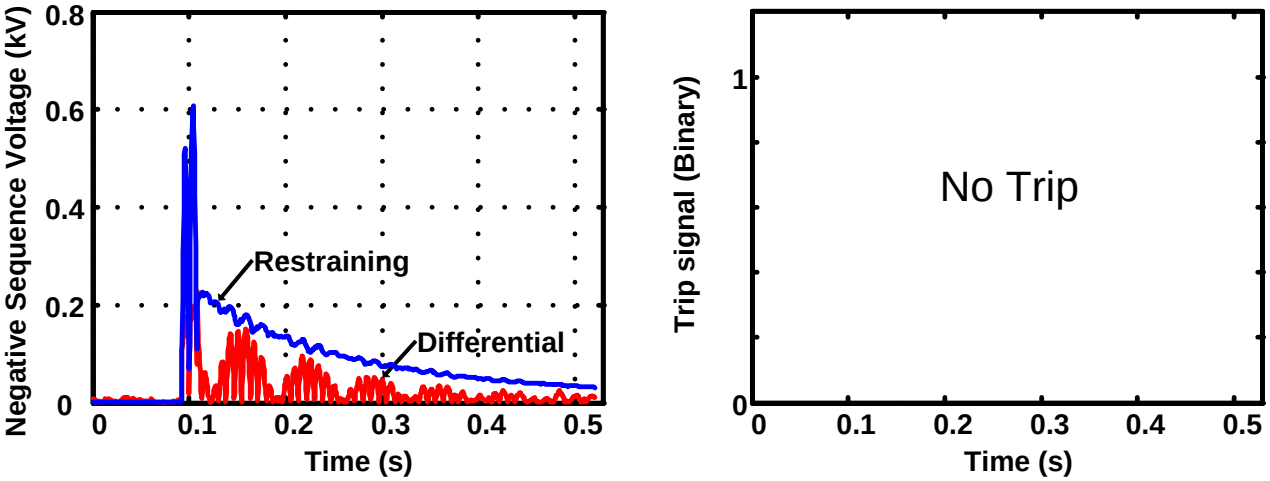

Figure 4.24: Proposed Algorithm: Energization without Fault with CCVT

4.10 Summary

Experimental data was presented in this chapter. First, an accuracy check was performed to ensure the analog-to-digital conversion system was functioning adequately. Turn-to-turn faults were simulated for the following scenarios: steady-state, energization, current transformer saturation, transformer over-excitation, and non-zero fault resistance. The proposed algorithm was also adapted to a Δ-Y Transformer and the effect of a coupling capacitive voltage transformer was examined. Trip time tables were used to compare the proposed algorithm performance to current differential protection with second harmonic restraint.

Chapter 5

Summary and Conclusion

5.1 Summary

This thesis described the development and testing of an algorithm and prototype for turn-to-turn fault detection in power transformers. The turn-to-turn fault is difficult to detect in its early stages since it causes little change in the faulted transformer's terminal currents.

This thesis began with basic transformer equations being presented in order to set the stage for the development of a novel algorithm capable of detecting minor turn-to-turn faults occurring in a transformer during energization and during normal operation. Stresses acting on a transformer's winding and insulation are briefly described to illustrate how turn-to-turn faults develop over time. Transformer inrush current and over-excitation are both discussed and related to the properties of the transformer's core. Various methods of transformer protection were examined in Chapter 1, in the form of a literature review, in order to present state-of-the-art methods of transformer protection. Transformer differential protection is discussed in detail since its sensitivity and speed was compared to the proposed algorithm.

Negative sequence current based turn-to-turn fault protection is discussed in Chapter 2. The algorithm is described in detail and a numerical example is provided in order to clearly illustrate how negative sequence current may be used to detect turn-to-turn faults occurring in a transformer. This example also demonstrates that a non-zero current must be flowing in both the primary and secondary sides of the transformer in order for the negative sequence current algorithm to be sensitive to turn-to-turn faults. The proposed method of detecting

turn-to-turn faults during transformer energization is discussed next. This negative sequence voltage based algorithm is first described using a faulted single phase transformer. Then, a numerical example of the negative sequence voltage based algorithm is presented. This example demonstrated that by using the primary and secondary terminal voltages, a turn-to-turn fault could be detected in a transformer. The hybrid negative sequence algorithm, comprised of the negative sequence current algorithm and the negative sequence voltage algorithm is presented at the end of the chapter.

Chapter 3 described the construction of the relay prototype and the development of a transformer model for use in a real time simulator. The simulation of turn-to-turn faults was discussed and the search for a method of modeling transformer inrush was outlined. A verification of the resulting inrush current waveforms, generated by the completed real-time simulator transformer model, was performed to ensure the model generated realistic inrush current wave shapes. Each component of the simulator model is then described in detail. The construction of the relay prototype is discussed, beginning with the analog-to-digital converter board. It was used to digitize the signals, representing the primary and secondary voltages and currents of a power transformer, to be read by a micro-controller. This micro-controller processed the digitized signals and applied the protection algorithm. Changes to the protection algorithm, required to protect Δ - Y Transformers, are presented at the end of this chapter.

Experimental results, gathered during tests performed with the relay prototype, are discussed in Chapter 4. The data presented in Chapter 4 shows that the hybrid negative sequence based algorithm proposed in this work could consistently detect turn-to-turn faults involving 3% of the windings. The proposed algorithm consistently detected turn-to-turn faults, during energization and normal operation of the transformer, faster than the differential method of transformer protection. The effect of the current transformers and coupling capacitor voltage Transformers (CCVT) were considered in the power system model used to test the proposed algorithm. The proposed algorithm successfully detected 3% turn-to-turn faults in a Δ - Y configured transformer despite oscillations caused by including the CCVTs in the simulation model.

5.2 Conclusion

Currents and voltages were generated using a real time simulator and fed to a relay prototype executing the proposed negative sequence based algorithm. For comparison purposes, a current differential relay prototype was also built and tested in the same manner as the negative sequence based algorithm. The curves used as trip criteria were examined, along with the trip signal, for each algorithm. The negative sequence based algorithm was consistently shown to be more sensitive and faster than the current differential algorithm. This observation is supported by the experimental data. Turn-to-turn faults involving 3% of the transformer's windings were detected by the proposed algorithm. The current differential algorithm with second harmonic restraint was able to detect turn-to-turn faults involving 10% of the transformer's windings under ideal conditions. The sensitivity of the differential current scheme was found to vary with CT saturation, fault resistance, and transformer over-excitation.

5.3 Thesis Contributions

The contributions of this thesis are summarized below:

- A hybrid algorithm, capable of detecting turn-to-turn faults during energization, was developed in this thesis. First, a negative sequence voltage based algorithm was developed in order to detect turn-to-turn faults occurring during energization. This algorithm was combined with a negative sequence current based protection scheme to form a hybrid negative sequence based algorithm. A relay prototype was designed and developed and used to test the sensitivity of the hybrid algorithm proposed in this work.

- The construction and implementation of a real-time transformer model allowed for the testing of the relay prototype. The model allowed for the simulation of non-linear behavior associated with the magnetic properties of the transformer's core such as energization inrush current and over-excitation in addition to turn-to-turn faults.

5.4 Future Work

- As described in Section 4.4.2, the transformer real-time model did not adequately represent the voltages of a transformer suffering a turn-to-turn fault on the same side as energization. The transformer model used to test the proposed algorithm may be improved by implementing a model which models voltage appropriately if the number of turns is reduced due to a turn-to-turn fault. The model proposed in [17] is a good candidate for such an improvement.

- Oscillations appeared in the negative sequence voltage due to the CCVT required to reduce the bus voltage to a voltage acceptable to the relay. These oscillations had the potential to cause a false trip during energization. Additional signal processing of the negative sequence differential and restraining voltages may be applied to negate the effect of the CCVT. Initial CCVT transients are known to have an adverse effect on distance protection algorithms [70]. This effect is prevalent during the initial cycles following a sudden change to the system such as a fault.

- Transformers are never used in isolation. An investigation of the proposed algorithm as part of a protection scheme of a transformer integrated into a wider system would yield data regarding the algorithm's response to complex interactions occurring between power system components. Sympathetic inrush and recovery inrush are examples of such complex interactions.

- The implementation of the proposed algorithm on a commercial relay platform and testing it using power hardware-in-the-loop testing may be done in a future work.

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Appendix A

Settings Tables

Leakage Reactance	**25%**	**15%**	**10%**	**5%**	**3%**	**1%**
X12	62.74	32.97	23.71	17.68	14.82	0.1196
X13	121.82	156.87	178.49	204.85	218.7	232.6
X14	66.4	109.88	141.92	184.82	207.73	230.64
X23	278.49	252.92	243.46	236.47	234.505	232.54
X24	162.34	181.61	194.02	210.83	221.195	231.56
X34	131.9	106.58	92.09	71.13	65.15	59

Table A.1: Single Phase Transformer Leakage Reactances for Turn-to-Turn Faults on High-Voltage Side of Transformer

Leakage Reactance	**25%**	**15%**	**10%**	**3%**	**1%**
X12	71.38	36.97	25.6	16.87	7
X13	128.48	164.42	200.36	219.09	247.69
X14	69.55	113.14	156.73	204.4	234.097
X23	308.2	277.56	246.92	244.63	217.512
X24	178.16	196.4	214.64	222.14	237.056
X34	147.45	113.11	78.77	46.88	22.352

Table A.2: Single Phase Transformer Leakage Reactances for Turn-to-Turn Faults on Low-Voltage Side of Transformer

Setting	Value	Units
R_p	474.0	Ω
L_p	4.46	H
N_p	27800	H
R_s	0.18	Ω
L_s	4.7e-4	H
R_{bp}	2298.0	Ω
R_b	400.9	Ω
L_b	1.84	H

Table A.3: Low Voltage VT Parameters

Setting	Value	Units
V_{HV}	230	kVF
V_{Int}	17	kVF
C_1	1.28962e-2	μF
C_2	2.63974e-1	μF
L_t	20.953	H
A	6.5e-3	m^2
l	0.5	m
R_p	474.0	Ω
L_p	4.46	H
N_p	11000	Ω
R_s	0.18	Ω
L_s	4.7e-4	H
N_s	115	Ω
R_{F1}	1.06	Ω
L_{F1}	0.01	H
C_F	8.0	μF
R_{F2}	4.24	Ω
L_{F2}	0.394	H
R_F	40.0	Ω
R_{bp}	2298.0	Ω
R_b	400.9	Ω
L_b	1.84	H

Table A.4: High Voltage CCVT Parameters