Study of Radiation-Tolerant SRAM Design

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Abstract

Static Random Access Memories (SRAMs) are important storage components and widely used in digital systems. Meanwhile, with the continuous development and progress of aerospace technologies, SRAMs are increasingly used in electronic systems for spacecraft and satellites. Energetic particles in space environments can cause single event upsets normally referred as soft errors in the memories, which can lead to the failure of systems. Nowadays electronics at the ground level also experience this kind of upset mainly due to cosmic neutrons and alpha particles from packaging materials, and the failure rate can be 10 to 100 times higher than the errors from hardware failures. Therefore, it is important to study the single event effects in SRAMs and develop cost-effective techniques to mitigate these errors. The objectives of this thesis are to evaluate the current mitigation techniques of single event effects in SRAMs and develop a radiation-tolerant SRAM based on the developed techniques.

Various radiation sources and the mechanism of their respective effects in Complementary Metal-Oxide Semiconductors(CMOS) devices are reviewed first in the thesis. The radiation effects in the SRAMs, specifically single event effects are studied, and various mitigation techniques are evaluated. Error-correcting codes (ECC) are studied in the thesis since they can detect and correct single bit errors in the cell array, and it is a effective method with low overhead in terms of area, speed, and power. Hamming codes are selected and implemented in the design of the SRAM, to protect the cells from single event upsets in the SRAM. The simulation results show they can prevent the single bit errors in the cell arrays with low area and speed overhead. Another important and vulnerable part of SRAMs in radiation environments is the sense amplifier. It may not generate the correct output during the reading operation if it is hit by an energetic particle. A novel fault-tolerant sense amplifier is introduced and validated with simulations. The results showed that the performance of the new design can be more than ten times better than that of the reference design. When combining the SRAM cell arrays protected with ECC and the radiation-tolerant hardened sense amplifiers, the SRAM can achieve high reliability with low speed and area overhead.

Acknowledgements

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I also gratly appreciate my laboratory colleagues. We worked together to finish the design and testing. Thanks to Dr. Shuting Shi. His instruction on radiation effects and chip testing helped me significantly with the simulation and radiation-hardened design in my project. Thanks also to Mo Chen for the instruction of my SRAM design and circuit function simulation. Although she has graduated, we still meet frequently online or by email. She provided much guidance and many useful technical suggestions. Thanks to Issam Nofal from iRoC on the instruction of TFIT simulation. TFIT is an important simulation tool on the radiation effect in my thesis.

As a Huskies Track and Field athlete at the University of Saskatchewan, I would like to say thank you to all the coaches and teammates I met, especially to the head coach Joanne McTaggart and Jason Reindl who are also the coaches for the sprint team. Thank you not only for the training program and instruction but also for the inspiring talk and cheer up when I was down. You taught me not to give up easily. I will always be proud of being one of the Huskies athletes.

Finally, I would like to thank my parents for supporting me during my further study in abroad. Their support and encouragement helped me to keep focused on my work.

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List of Abbreviations

ATD	Address-Transition Detector
CMRR	Common Mode Rejection Ratio
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CR	Constraint Ratio
CRC	Cyclic Redundancy Check
CVSL	Cascode Voltage Switch Logic
DICE	Dual Interlocked Storage Cell
DRAM	Dynamic Random Access Memory
ECC	Error-Correcting Codes
EDAC	Error Detection and Correction
FDSOI	Fully Depleted Silicon-On-Insulator
FF	Flip-Flop
FinFET	Fin Field-Effect Transistor
FIT	Failure-In-Time
GCR	Galactic Cosmetic Rays
GDS	Graphic Database System
GND	Ground
HDB	Hardening By Design
IBM	International Business Machines
IC	Integrated Circuit
LEAP	Layout Design Through Error-Aware Transistor Positioning
LET	Linear Energy Transfer
LSI	Large-Scale Integration
MCU	Multiple Cells Upset
NMOS	Negative-Channel Metal Oxide Semiconductor
NSREC	Nuclear and Space Radiation Effect Conference
PDSOI	Partially Depleted Silicon on Insulator
PMOS	Positive-Channel Metal Oxide Semiconductor
PR	Pill-Up Ratio
PSRR	Power Supply Rejection Ratio
Quatro	Quad-Node Ten Transistor Cell
RAM	Random Access Memory
RC	Resistor Capacitor Circuit
RHBD	Radiation Hardened By Design
SA	Sense Amplifier
SEC	Single Error Correction
SEE	Single Event Effect
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset

SOI	Silicon-On-Insulator
SRAM	Static Random Access Memory
SPE	Solar Energetic Particle Event
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology Computer Aided Design
TMR	Triple Modular Redundancy
TI	Texas Instrument
TSMC	Taiwan Semiconductor Manufacturing Company
VDD	Voltage Drain Drain
VSS	Voltage Source Source
WL	Work Line
XOR	Exclusive OR

1. Introduction

1.1 Background

Integrated circuits in space face reliability issues due to the radiative surroundings. High-energy particles in space can ionize a semiconductor and induce errors due to single event effects (SEEs). In 1975 Binder *et al.* Reported that anomalies in communication satellite operators had been caused by the unexpected triggering of digital circuits [1]. Until 1978 research did not focus specifically on SEEs as they were not considered to be a major concern or issue for the reliability of spacecraft electronics.

After scientists observed SEEs in space electronics, they discovered the same phenomena in ground integrated circuits [2]. It was reported that when Dynamic Random Access Memory(DRAM) size was changed from 16k to 64k, the soft error rate increased dramatically as soft errors are defined as recoverable errors, where as hard errors are permanent failures. Scientists identified packing materials as the main reason. These materials had been polluted by alpha particles, a problem which was experienced by Intel. The company found that its new Large Scale Integration(LSI) ceramic packaging factory was located close to an abandoned uranium mine. The mine had polluted the water in the area, and that polluted water was used by the Intel factory. The materials contaminated by alpha particles had been packaged into all the chips it had manufactured. After this discovery, low radiation materials were used successfully to prevent single event occurrences.

At the end of 1970, researchers proved that the soft errors happening in the storage of the satellites were induced by space radiation particles. At that time, satellites and integrated circuits were working in low earth orbit. In their study, C.S.Guenzer and his partners used the term Single Event upset(SEU) for the first time [3] to represent this kind of soft error. This term was adopted quickly by others. It was used to describe integrated circuit upset caused by direct and indirect ionization. In 1979, two teams announced that protons and electrons could cause indirect ionization, which in turn can cause SEU in integrated circuits

[4], [3]. In space, because the number of protons is far more greater than the number of other particles, the proton become a major source for SEU. Subsequently, researchers found that not only cosmic radiation but also solar wind and protons captured in the earth's radiation belt can cause SEUs. In 1979, researchers also found Single-Event Latch-up in the integrated circuits for the very first time [5].

In the early 1980s, SEU was a major research topic in the radiation-effect community. The research in this period was focused on DRAMs, SRAMs, latches, and flip-flops. During that decade, a number of methods for mitigating SEU were introduced [6] [7]. Meanwhile, the research on the fundamental formation mechanism of Single Event Effects(SEEs) has increased researchers' understanding of this problem. There were also some studies aimed at problems that might appear in the future, such as Single-Event Transient (SET), which is a transient effect caused by an ion hit in combinational logic circuits. In the late 1980s, some studies were also done of SEEs in complex logic circuits [8], [7], [9].

In the 1990s, two factors motivated researchers to further harden ICs against SEEs. The first was that due to the increasing complexity of ICs more and more circuits had to be protected from radiation effects. The second was that due to the scaling of silicon technology the size of transistor was decreasing. According to Moores Law, the number of transistors in a chip doubles about every 18 months. The speed of the ICs increases, and the size of transistors decrease. This makes ICs more sensitive to SEEs. Ronen *et al.* predicted that the error rate would grow by 40% after every new processing line generated if no mitigation approaches were adopted [10]. By the end of the 1990s, errors caused by SETs were increasingly more significant in digital circuits, since the SET rate in logic circuits increases with the clock frequency, while the SEU in storage cells remains relatively constant.

In the twenty-first century, the soft error rate in memories, sequential circuits, and combinational circuits keep increasing due to the scaling of the device, lower power supply voltage, and higher clock frequency. This imposes a threat not only to the electronics in space applications, but also to commercial products at the ground level. The fault-tolerant function has already become one of the main features used to fulfill the reliability requirements in the IC industry. Various hardening by design(HBD) techniques have been introduced in this field [11] [12]. Some processes, such as Silicon on Insulator which can naturally reduce soft

errors, also have become attractive in the community [13], [14].

1.2 Hamming Code

In order to detect or correct errors, we can adopt Error Correcting Codes (ECCs). Using ECC designs in memory circuits can greatly improve the reliability of the circuit. Hamming code is one of the most representative ECCs. Hamming Code was created in the 1950s [15] and was named after its inventor, Richard Hamming. It has been adapted and widely used for SRAM [16]. Hamming code is a linear error correcting code which can detect two bits and correct one bit of an error. In addition, the redundancy of Hamming code and the delay are also very small. In this thesis, in order to increase the reliability of an SRAM circuit while ensuring small redundancy and small delay, Hamming code is adopted.

1.3 FDSOI

In recent years, transistor feature size has been decreased to below 10nm. The leakage current induced by the short channel effect becomes increasingly significant. In order to address this problem, new technologies has developed such as FinFET(Fin Field-Effect Transistor) or SOI. SOI technology uses an oxide layer under the devices in the substrate, and each transistor is insulated by silicon oxide. IBM was the first to report on SOI technology, and it was used for the Macintosh PowerPC G4 processor. Apart from IBM, Motorola, TI, and NEC also started to research SOI. It is a very attractive technology due to its low power consumption and high speed when compared to conventional bulk technologies.

SOI can be divided into Partially Depleted (PD) and Fully Depleted (FD). A depletion zone without free carriers will be formed in the silicon body. For FDSOI, the silicon body is thin and the bulk charge is fixed. In PDSOI, the silicon body is thick. The bulk voltage varies with the charge in the silicon. The thickness of the FDSOI oxide layer is usually smaller than 800Å. The thickness of the PDSOI oxide layer is usually from 1000Åto 2000Å.

Figure 1.1 is the basic FDSOI wafer structure.

FDSOI is a planar process technology that can reduce the silicon manufacturing process.

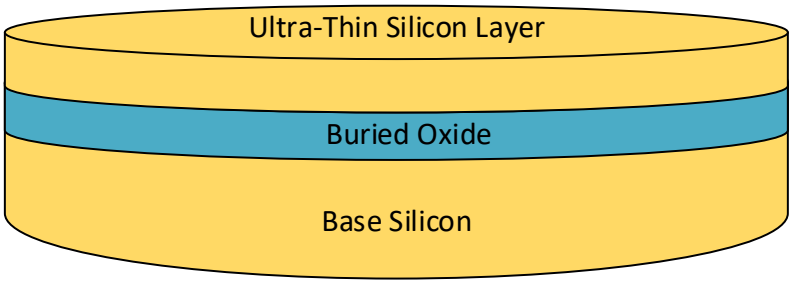

Figure 1.1: FDSOI wafer structure

This process relies on two main steps. First, an ultra-thin layer of the insulator is placed on the basic silicon waver. This insulator is called buried oxide. Then, a very thin silicon layer is placed. This layer which is not doped is used for the transistor channels.

SOI has several advantages compared with bulk silicon.

- It realizes dielectric isolation for transistors instead of using reverse-biased PN junctions;

- It reduces the parasitic capacitances in transistors, and hence increases the speed. SOI can gain a 20 to 30% speed increase compared to bulk silicon technology with the same feature size;

- It consumption less power because the SOI helps reduce the parasitic capacitance and leakage current. The power consumption can be reduced by 35 to 70%;

- It eliminates the latch-up effect, which is important for space applications;

- It is compatible with existing production processes.

FDSOI is widely used in SRAM design because of its excellent properties, especially for the advanced 28nm FDSOI technology. Previous experiments show that FDSOI can significantly reduce the soft error rate in radiation environments [17], [18], [19], [20].

1.4 Motivation

As mentioned previously, 28nm FDSOI technology can effectively reduce the soft error rate in SRAMs. In order to further reduce soft errors, Hamming code is a good candidate to protect cell arrays since its area overhead is small. So far, its overall performance, such as power, speed, and error rates, has not been reported in the community. Since the radiation hardened by design SRAM research is focusing on small size [21], it is necessary to carry out some larger size of SRAM and do the radiation test to see how the hardened method work in it.

Besides the cell arrays, errors may happen in the peripheral circuits during the reading/writing period. Sense amplifiers are vulnerable to SEEs. Therefore, radiation-tolerant sense amplifiers are also necessary. Radiation-hardened sense amplifiers for SRAM have been developed but the area overheads are enormous [22]. Therefore, it is useful to conduct research in order to find cost effective approaches for radiation-hardened SRAM sense amplifiers.

1.5 Objective

The overall objective of this thesis is to enhance SRAM radiation-tolerant performance by developing hardening design techniques in order to reduce soft errors generated by SEEs. The two main approaches adopted in this thesis are:

- Improving the cell array SEE performance. This will be accomplished by using Hamming code redundancy. The Hamming code redundancy can not only detect one-bit error but also correct the affected bit. 1Mx16 bit asynchronous SRAM will be designed and Hamming code will be used to protect the cell arrays. Adding Hamming code to this large, asynchronous SRAM can better measure the performance of the hardening design method;

- Developing a novel sense amplifier to further reduce the soft error rates induced by SEEs. To evaluate the effectiveness of the design, simulations based on the schematic

and layout will be used to verify the results.

The steps below are followed to accomplish the objectives:

- Review the literature on SEEs. The background includes the principle and formation of SEEs and the different radiation sources, including how they impact the SRAM circuits;
- Summarize the existing mitigation solutions for SEEs;
- Design the SRAM and use simulations to validate the functionality;
- Apply the specific single event tests on the primary 6T cell for the SRAM and the Hamming code structure, and evaluate its performance;
- Test the functional simulation, schematic SEU simulation, and the TFIT simulation on the developed sense amplifier. The result will be compared with that of the unhardened sense amplifier to evaluate its performance.

1.6 Thesis Organization

- Chapter 1 is the introduction containing the radiation-hardened design background, Hamming code introduction, FDSOI introduction, and the objective of the thesis.
- Chapter 2 discusses radiation effects and the different radiation sources.
- Chapter 3 contains the current SEE tolerant design review for SRAM. The Hamming code method and several existing sense amplifiers will be discussed. A specialized simulation tool for studying SEEs will also be introduced in this chapter.
- Chapter 4 describes the SRAM designs. This chapter include the introduction of the SRAM operation, Hamming code circuits design, and the radiation-tolerant sense amplifier design.
- Chapter 5 presents the simulation results of the thesis. The results include the 6T SRAM cell, Hamming code circuit, developed sense amplifier, and all the SRAM test results.

- Chapter 6 contains the conclusions and possible future works.

2. Radiation Effects

2.1 Radiation Source

There are several different radiation sources in space. The first, galactic cosmetic rays (GCR) comes out of our solar system and have very high energy. Most of them came from a supernova explosion, neutron star, and pulsar. This radiation contains 98% high-energy particles and 2% electrons. The high-energy particles contain 85% protons, 14% alpha particles and 1% heavier particles.

The second radiation source is solar energetic particle events (SPEs). The sun creates solar wind by emitting particles which contain protons and electrons. The low-energy particles are around 100eV to 3.5keV with a speed of 300 to 800km/s. However, the surface of the sun will release large amounts of soft and hard X-rays with different wavelengths. In some large solar energetic particle events, the maximum instantaneous intensity of a proton can exceed three or four orders of magnitude of an ordinary cosmic ray. This kind of event is dangerous to ICs.

The third radiation source is a radiation belt called the Van Allen Belts near the earth. The particles trapped by these belts have very high energy. The electrons usually have 7 MeV of energy and protons usually have up to 600 MeV of energy. These particles are trapped in a specific position. They travel in a mirror movement along the magnetic field line. In this area, protons play the most critical role.

Linear Energy Transfer(LET) is the value of energy that an energetic particle transfer to the material such as silicon in the track of per unit distance. The radiation effect has an important relation with LET value. In general, the higher the LET value of radiation at the same absorbed dose, the greater the radiation effect is. This is the formula for getting LET

$$LET = -\frac{1}{\rho}\frac{dE}{Dx} \tag{2.1}$$

LET has two different units, MeVcm^2/mg and pC/um. Both of the units are mentioned

in this thesis. The convert of the two unit is shown as,

$$1pC/um = \frac{1 \times 10^{-12}C}{1.6 \times 10^{-19}C/pair} \frac{3.6eV/pair}{\rho \times 10^{6}} 10^{-4}cm^{-1} = 96.608MeVcm^{2}/mg \tag{2.2}$$

2.1.1 Alpha Particle

Alpha particles are helium nuclei moving at high speed. An alpha particle usually represented by He contains two protons and two neutrons. The rest mass is 6.64 x 10^{-27} kg and the electric charge is 3.20 x 10^{-19} coulomb. Intel was the first to report an SEE on earth caused by an alpha particle. The cause was packaging material of ICs, which contained radiation pollution.

2.1.2 Heavy Ions

Heavy ions refer to a mass number larger than four, that is, ions next to He in the periodic table. In space, protons are the most common particles, but heavy ions such as O, C Ni, Si are also very common. However, the particles whose charge number is larger than 30 is very rare. The LET range is from 1 MeVcm^{-2}/mg to 100 MeVcm^{-2}/mg [23]

The first detected soft error in space was caused by heavy ions [24]. It began the study of the effect of these particles and research into radiation-tolerant designs for integrated circuits in space devices. Researchers successfully simulated heavy ion beams on the ground by using heavy ion accelerators. This technique was used to simulate the space environment. Accelerators was various ions and can generate different LET beams. They also can accelerate the beams to a high speed. Using accelerators is relatively inexpensive and gives a means of controlling heavy ion radiation. We can also repeat the radiation-effect experiments and do a better study of radiation-hardened designs.

2.1.3 Neutrons

The concept of the neutron was proposed by the British physicist Ernest Rutherford and was proven in an experiment in 1932. The mass of a neutron is $1.6749286e^{-27}$ kg, a lightly grater than that of a proton. There are two categories of neutrons: thermal neutrons and fast

neutrons. The difference between the two is their energy, with thermal neutrons having lighter energy than fast neutrons. It is worth noting that neutrons cannot produce direct ionization, only indirect ionization. However, only thermal neutrons can react with boron, after which alpha particles are released. The electronic components in the electronic instruments of the near-earth satellite need to be tested by neutron irradiation, because on the surface of the atmosphere where such satellites work, neutrons account for the highest proportion of high-energy particles.

2.1.4 Protons

The British physicist Ernest Rutherford discovered the proton. In 1918 when working in the Cavendish Laboratory, he used alpha particles to strike a nitrogen nucleus and found the evidence of protons. They are particles with a positive charge, and are abundant in space environments. It makes up 87% of galactic cosmic rays. The energy of a proton is around 1GeV, some of them are higher than $10e^{12}$ MeV. The energy of protons in the Van Allen Radiation Belts is also very high. Protons are the primary particles in that area.

Protons can generate direct and indirect ionization when they strike the electric circuits, depending on the sensitivity of the circuit. For example, in 120nm technology, when the proton energy is lower than 10MeV, the proton can generate direct ionization, but the 120nm transistor is not that sensitive the threshold voltage is high. The highest LET of the proton is lower than the transistor's LET; there will be no SEE, and therefore the direct ionization can be ignored. However, as the technology develops, the size of transistors decrease and the circuits the circuits becomes more sensitive. The LET also becomes smaller. When the proton directly ionizes the silicon layer, there might be an SEE. When the energy is high, the direct ionization can be ignored for all technologies. There will be indirect ionization by generating secondary radiation particles to make soft errors occur.

2.2 Single Event Effect

An SEE occurs when a single high-energy particle, for example, a proton or neutron, hits an integrated circuit sensitive area and changes the correct states of the circuit. SEE was first

mentioned by Wallmark and Marcus in 1962 [25]. May and Woods found a soft error in the IC designs for the first on the ground level [2]. The soft error was from the alpha particles which was contained in the packaging materials for integrated circuits. The category of SEEs are Single Event Upset, Single Event Latch-up, Single Event Burnout and Single Event Gate Rupture.

Because high-performance microelectronic devices are widely used in satellite systems as the IC designs developed, the function of satellites become more and more complex. The SEE became the main concern for space satellite design. In 2003, a solar proton event paralyzed one of the satellites in a geostationary orbit. Many scientific satellites in the United States lost data as a result of this phenomena. The single particle effect is another major space environment effect which threatens the safety of a spacecraft. With the increasing complexity of spacecraft systems and device integration, the single particle effect will become more serious. In the actual radiation environment, the probability of being strike by two particles at the same time is far less than the probability of being strike by a single particle. The single event is the main research for the radiation-tolerant design.

2.3 Single Event Transient

The digital logic circuit can be divided into two different kinds: sequential and combinational. They are divided into two different kinds by their logic function. The combinational logic circuit does not have memory. A Single Event Transient(SET) is a specific kind of SEE in which a single energetic particle strikes the reverse-biased PN junctions of combinational logic and cause a voltage transient to occur[3].

When an energetic particle passes through the sensitive area of an IC device, it will deposit a charge on the incident trajectory. The previous research [26], [27] shows that the disturbance caused by a single particle in an integrated circuit can be characterized as a transient pulse with a rapidly rising edge and a stable step part.

Researchers found that heavy ions are the main source particles that induce a SET. A heavy ion which strikes an IC device will have a Coulomb interaction with the electron of an atom. When the energy is large enough, the electron will leave the atom. The atom will have

a positive charge and the electron have a negative charge. This is called direct ionization. Particles generated by direct ionizing can cause other atoms to ionize. This is called secondary ionization. The number of electrons produced by secondary ionization accounts for a large proportion of the total ionization process (60% to 80%). The electron-hole pairs will be gathered by the N or P area and a SET will be generated.

2.4 Single Event Upset

An SEU is a status change caused when energetic particles hit a sequential logic circuit [28]. It is one of the most common SEE caused by space radiation. It usually happened in data storage cells such as memory circuit and microprocessor. The device error caused by SEU is a "soft error". A soft error can be correct by system reboot, repower or rewrite. SEUs were first discovered and reported in some above ground nuclear testing from 1954 to 1957. During that time, a large number of errors were observed in electronic devices in aircraft. Researchers are constantly exploring ways to solve this problem.

As the transistor size of CMOS designs decreased, the problem caused by SEUs became more serious. Researchers found that alpha particles from tiny amounts of radioactive isotopes in packaging materials could also cause SEUs. The energy of an alpha particle is usually around 5 MeV, with a penetration depth of 25 microns. The number of electron-hole pairs generated is 10^6 orders of magnitude. The electron-hole pairs in the sensitive area are gathered by PN junctions. The current generated by this charge movement can cause errors in semiconductor devices. The error rate varies with particle energy. Particles with an energy of around 4 MeV cause the highest error rate. The incident angle of particles will also have different effects. When the angle is 60, the particles can cause the most errors because particles with this angle travel the longest distance in sensitive regions. In memory designs, Figure 2.1 is an example of the SEU sensitive map. In this figure, the node A = 1; node AN = 0. In this status, transistors M3 and M2 are turned off. The two transistors have the reverse-biased PN junction(shown in the red circle). When SEUs happen in those two nodes, the turning off transistors may be turned on. Errors may happen.

SEUs not only occur in cross-coupled inverters, they also occur in WL transistors because

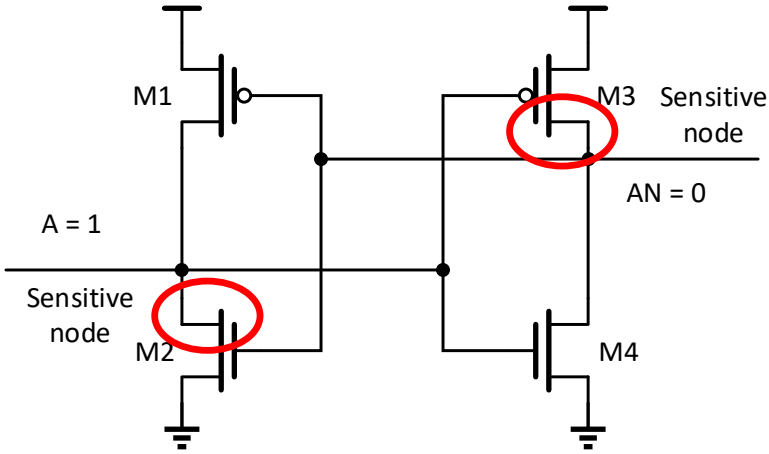

Figure 2.1: Cross-coupled inverters sensitive nodes

the N^+ area can gather electrons and change the status of the WL. This change can cause memory to read or write incorrect data. Researchers found that the sense amplifier(SA) area is also sensitive to SEUs. Most of the SA is a latch-based structure. An SEU can make the latch change from one status to another. Both states have the same probability of switching to the other.

At the transistor level, an energetic particle striking a PN junction can cause a transient current. If the particle striking creates enough charge, the data saved in the junction may be lost. The magnitude and duration of a transient current are related to the type and energy of particles and the type of the transistor technology.

The main method for protecting spacecraft devices against SEUs is to use error-checking and error-correcting codes. Using software or hardware designs, a device can detect an SEU and fix it automatically so that it will not cause further and more serious or even fatal errors.

3. Current SEE Tolerant Designs

3.1 Category of SEE Tolerant Design

When SEEs occur in an electrical circuit, a node hit by particles will normally influence the whole circuit in two ways. If the change in this node affects other nodes and causes a circuit function error, this will be fatal to an electrical circuit. If the node does not affect the level of other nodes, after the energy particles release their energy, the node which was attacked will recover to the previous level. This kind of attack is harmless. Using some specific technology, most of circuit-level designs aim to prevent the attacked node from changing the level of another node.

The technology of radiation-tolerant design can be divided into four approaches. The first is to reduce the number of electrons or holes generated by the energetic particles or reduce the number absorbed. Researchers usually accomplishing by improving the quality of the material used and the manufacturing process. The second is to prevent the node from absorbing the electrons or holes generated by the energetic particles or reduce the number. Researchers usually improve this by improving the layout and circuit structure. The third approach is to increase the amount of characterization logic 1 in the circuit. This allows the node not to flip even if it absorbs the electrons. However, this kind of technology is not matched with the development of modern integrated circuits. Because the size of the transistors is decreasing, the amount of characterization logic 1 is also getting smaller. The fourth approach is to avoid affecting other nodes when a node experiences an SET. Researchers are responding to this situation with new designs on the electrical circuit.

SEE-hardened designs can be achieved in two ways. One is processing and the other is circuit design. This section will introduce the circuits that are radiation-hardened by design.

3.2 Silicon-on-Insulator

In the 1960s, SOI technologies were developed for military use [29], [28]. The Bulk and SOI are two technologies of CMOS. The advantages of the SOI can be demonstrated by comparing the two technologies. An SOI wafer contains a thin layer of oxide called berried oxide between the substrate and top silicon. The oxide gives the SOI structure the ability to solve the latch-up completely. It also has the advantage of small parasitic capacitance, a high level of integration, high speed, and a wide temperature range. SOI also has a high radiation-tolerant performance according to previous studies [28], [30]. Figures 3.1 and Figure 3.2 show the structures of nMOS FDSOI and nMOS Bulk transistor.

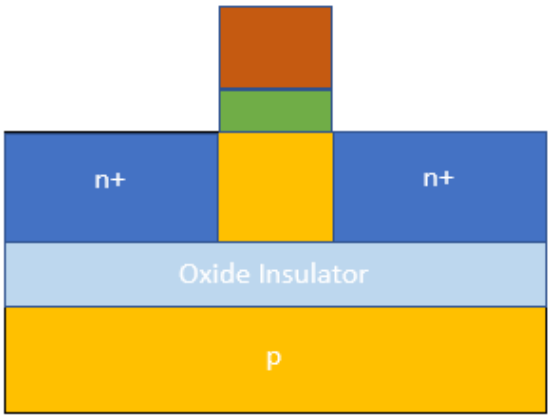

Figure 3.1: nMOS FDSOI transistor

3.3 Redundancy-Based Methods

3.3.1 TMR

Figure 3.3 shows the structure of Triple Modular Redundancy (TMR). The TMR method was first published in 1962 to improve computer reliability [31]. There are three redundant identical logic circuits and a voter logic circuit. The voter logic judges and takes the majority

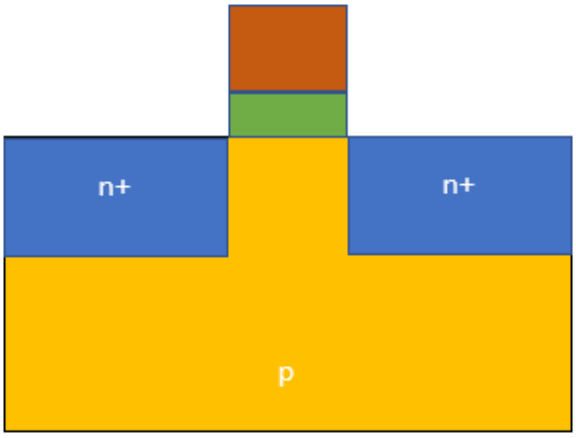

Figure 3.2: nMOS Bulk transistor

of the inputs to be the output value. If one of the logic circuits has an error, the other two are working properly, the output will remain correct. TMR is the most widely used redundant method in radiation fault-tolerant designs. The application of TMR is very convenient because the structure can be designed into the automatic design flow based on standard cells.

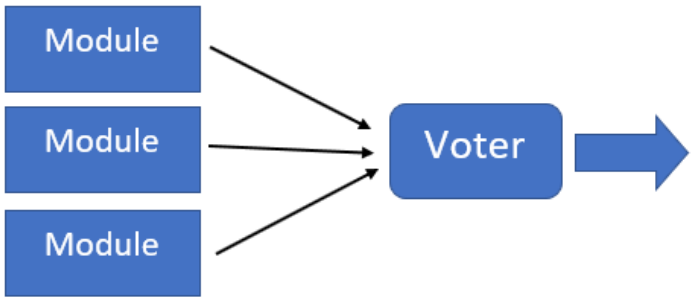

Figure 3.3: TMR working process

In the vast majority of cases where errors are made, the probability of producing a single error at a time is the greatest which means, the TMR can work well. However, with the development of the technology, the transistor size will become smaller. The probability of

multiple errors occurring simultaneously under a single particle attacking. Meanwhile, this design has a lot of redundancy, it's not a good choice.

3.3.2 Guard-Gate

The guard-gate shown in Figure 3.4 is also called the Muller C-element or transition AND gate. It is a form of "delay- judge" circuit. The basic structure of this circuit allows the output to change only if two inputs have the same data. This kind of circuit is usually used in combinational logic. Suppose an energetic particle hit the circuit and changes one of the inputs. The two inputs have different delays, and the pulse is short. If the pulse is shorter than the delay period, the two inputs will be different preventing change to the output [32]. The period of delay must be longer than the worst SET pulse. According to this analysis, the circuit can eliminate the SET. This technique is also referred to as time filtering.

A disadvantage of this circuit is the delay input unit, which cause the delay of the whole circuit to increase. When SEEs were first discovered, researchers tried to use Resistor-Capacitor(RC) filtering technology. Guard-gate technology is usually combined with other techniques.

3.3.3 DICE

Dual Interlocked Storage Cell (DICE) is a form of redundant design which has been used widely since it was reported for the first time in 1996 [33]. Figure 3.5 depicts the basic structure of a DICE cell.

Compared with the two inverters cross-coupled storage cell, a DICE has four storage nodes A, B, C, and D. In these four nodes, A and C have equivalent values, as do nodes B and D. For example, if the nodes A and C are at logic 0, B and C are at logic 1. Then the ON transistors are N1, P2, N3, and P4. The OFF transistors are P1, N2, P3, and N4. The circuit of this state is shown in Figure 3.6.

If node A is hit by a particle, it will have a high-level pulse. Since the transistor N1 is ON, the high level in node A will be driven by this transistor. The two relative transistors P2 and N4 will also be affected. P2 will be turned OFF, and N2 will be turned ON. Since

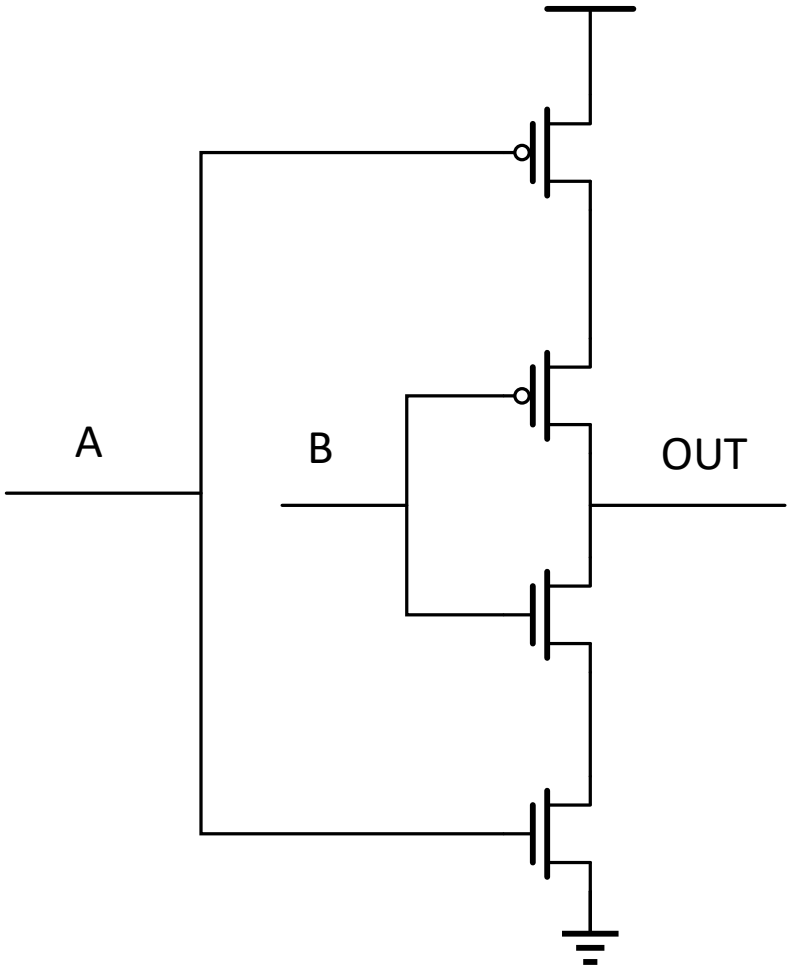

Figure 3.4: Structure of the guard-gate

P2 is turned OFF, N2 is also OFF, and node B will be floating and remain at this status. A critical effect occurs with node D, P4, and N4 will also have a similar effect. The two transistors N4 and P4 are turned ON, and there will be a competition between these two transistors. Node D will also be floating. After the particle strikes and the SET pulse ends, the level of the voltage will recover, and the two floating nodes will recover to their previous voltage value. If there is only one node that is hit, this DICE circuit can prevent an SEU from occurring. Figure 3.7 simulates the situation when one of the nodes is hit.

In order for signals to write data into the DICE circuit, there must be at least two nodes being accessed at the same time. The advantages of the DICE circuit are as follows:

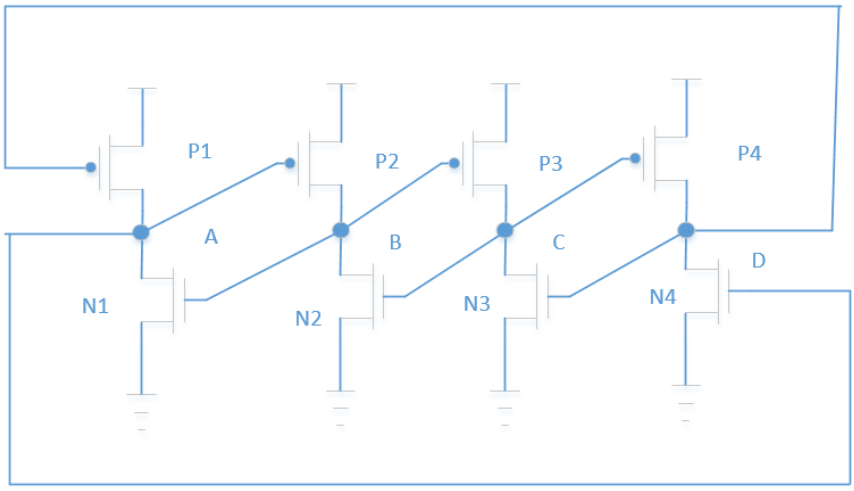

Figure 3.5: DICE structure

- Compared with the TMR structure, the DICE structure has a smaller area and lower power consumption.
- The transistors of the DICE structure does not have a specific size. It is commonly used as an SEU tolerant storage element.

The disadvantage is:

- The DICE can tolerate to a single particle strike, if there two nodes are hit or affected, an SEU will occur. As the size of transistors decreases, the possibility of two nodes been affected at the same time will increase.

3.3.4 Quatro

With the progress of technology, circuits are becoming increasingly sensitive, and thus making the situation more serious for electrical facilities in space [34], [35], [36]. The capacitance and threshold voltages are getting decreasing which makes SRAM more vulnerable to an SEU. Meanwhile, the traditional 6T SRAM cell has several limitations in a radiation environment. An SEU occurring in memory is the main problem for researchers [37]. There are many

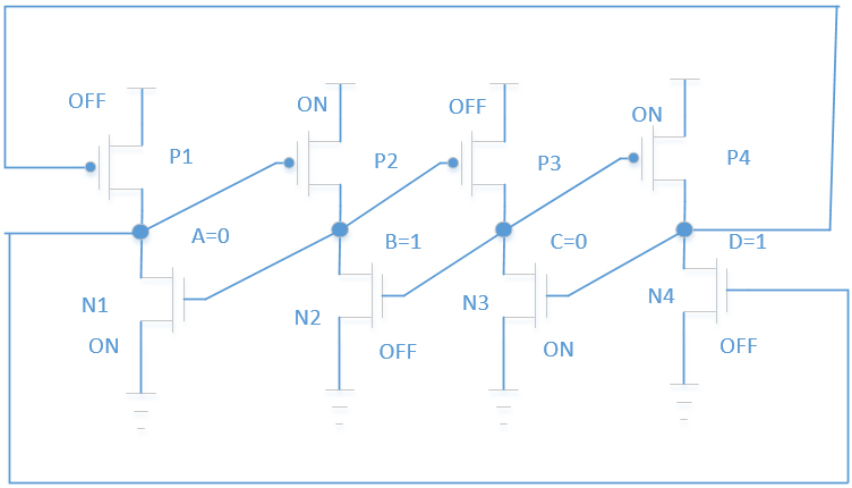

Figure 3.6: DICE node state

new structures being reported. Recently, a Cascode Voltage Switch Logic (CVSL) based Radiation Hardened By Design(RHBD) cell named Quatro been published [38]. In the first design, a 90nm technology structure Quatro was used in an SRAM design. After the Quatro was modified, the behavior was significantly enhanced. The neutron soft error rate was reduced by 98% compared to a regular 6T SRAM cell [39]. It performed very well in SEU tests. Quatro 10T has been used in several SRAMs, Latches, and flip-flops. Figure 3.8 shows the Quatro 10T structure.

3.3.5 LEAP

Layout Design Through Error-Aware Transistor Positioning (LEAP) is a principle for layout designing. LEAP extends traditional layout design, and is a specific way for optimizing a layout in order to enhance the ability to resist SEEs. It is categorized as a redundant method, but LEAP can also be applied in non-redundant design. It can be used in both combinational logic and sequential logic. Among its advantage, this method does not significantly affect timing delay or power consumption. It is used to reduce the possibility of multiple node upsets.

LEAP can utilize charge sharing to reduce overall soft-error sensitivity. For a large area

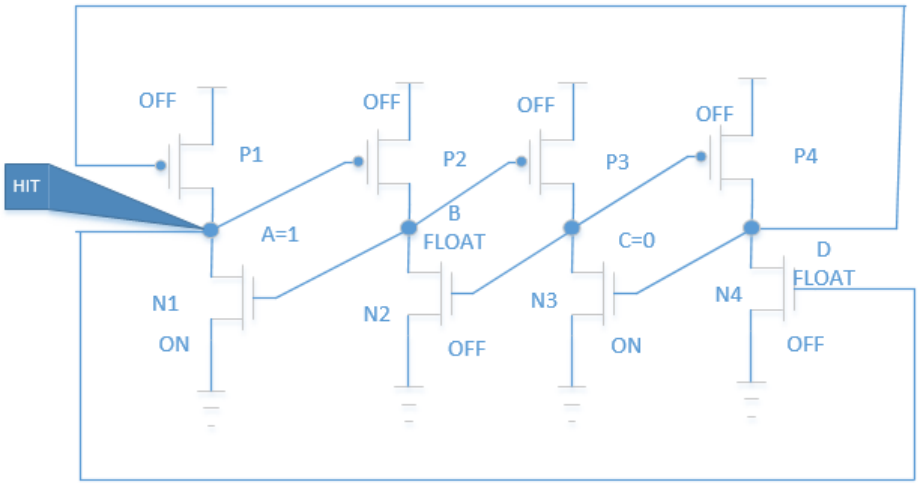

Figure 3.7: Particle hit DICE

layout, such as SRAM arrays, it can be hardened by using error-correcting codes. However, for sequential elements, such as flip-flops and latches, this method does not work. As technology develops, the charge deposited by a particle strike can affect multiple nodes in the same well. This effect has become harder to prevent [38]. LEAP was developed to combine and reduce this effect.

When the energetic particle hits the drain of an nMOS, it will generate a positive pulse and decrease the voltage of this node if the particle hits the drain of a pMOS. It will increase the voltage of this node. If the particle hits these two drains at the same time, the two pulses will combine, and the error in the circuit will be reduced. Take a CMOS inverter as an example. Like Figure 3.9, when the input is 1, the output is 0, the PMOS is off, and NMOS is on. When the energy particle hit the PMOS, it is opened by the pulse, and the output will occur a positive pulse like the red curve. If the particle hit the NMOS, there will be a negative pulse like the green curve. If the particle is large enough and hit the two transistors, the two unexpected pulses will cancel out some of each other, just like the blue curve.

The method of LEAP is to place the drains of the PMOS and NMOS close to each other just like the Figure 3.10. The arrows in the diagram indicate that the bombardment in that

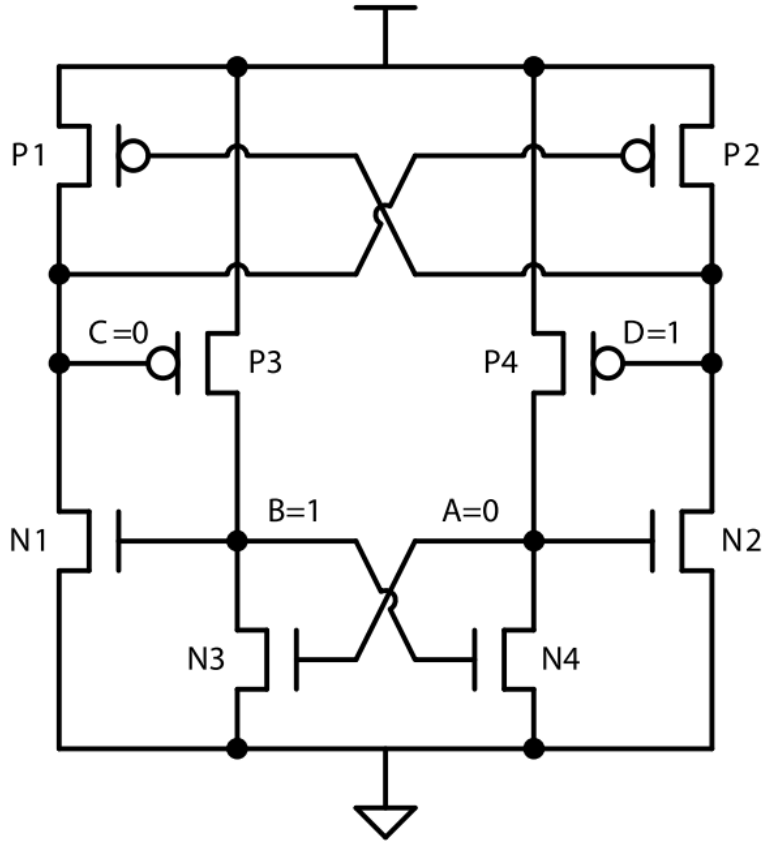

Figure 3.8: Quatro cell in state-0 [39]

direction is immune to this structure. That is the direction in which these two drains are attacked at the same time. Kelin *et al.* used the DICE structure to combine with the LEAP method because the DICE is immune to a single particle attack and vulnerable to multiple particles attack [40]. In his research, the LEAP-DICE improves 2000 times compared to the regular DFF and five times better than the regular DICE. The LEAP-DICE increases area by 40% and power consumption by 54%. According to the assumption of "2X node separation equals to 10X fewer soft errors [41]", the five times better performance is not from the extra 40%area which can only improve by 1.75 times. Lilja *et al.* used the LEAP method in a 28-nm CMOS design on a DICE flip flop cell. The test result of alpha and neutron shown no errors generated. In conclusion, adding LEAP in a 28-nm technology design can get a better result than in a 180-nm design. LEAP layout is more suitable for the advanced technologies.

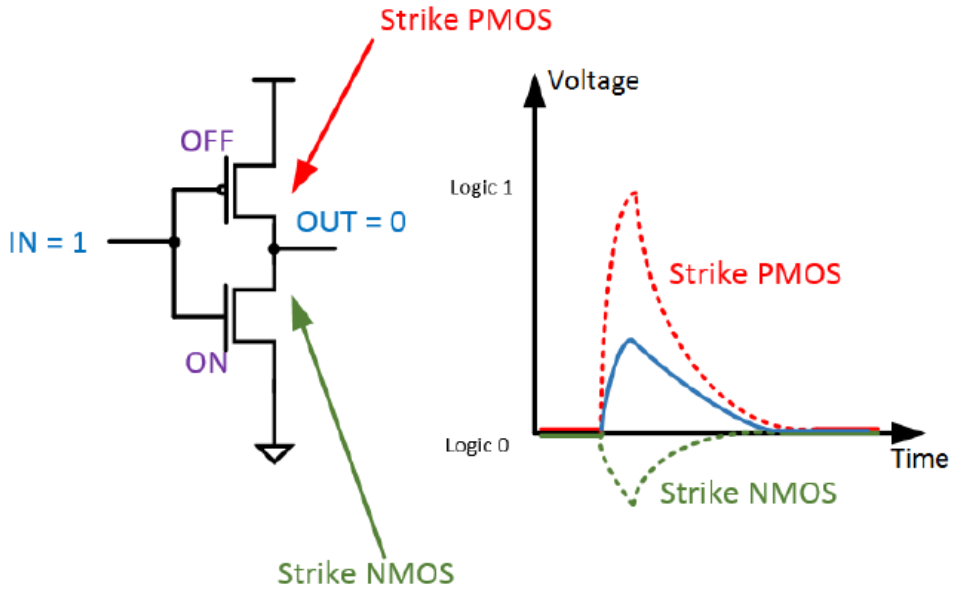

Figure 3.9: The change in current when a particle hit both drains of the PMOS and NMOS in an inverter

3.4 ECC

Transmission of data through an electrical circuit will generate errors. Researchers use several error-detecting methods to solve the electrical error problem, such as parity bits and Cyclic Redundancy Check(CRC) [42], [43], [44], [45]. These methods have been used by scientists to harden IC design. An Error Correcting Code (ECC) can fix the error in the data transport automatically, giving data the ability to add redundant bits and increase reliability. When the receiver or the detection device receives the data, it will judge the data according to the redundant bits. The data in memory is easily attacked by SEEs and code error detection to protect memory circuit has proven to be very useful.

3.4.1 Parity Check

A parity check can be used to detect the correctness of data transmission. The basic technique is to add a parity bit to data. If the number of "1" is odd, the check is called odd check. If it is even, it is called even check. Choosing which check to use is designed in advance.

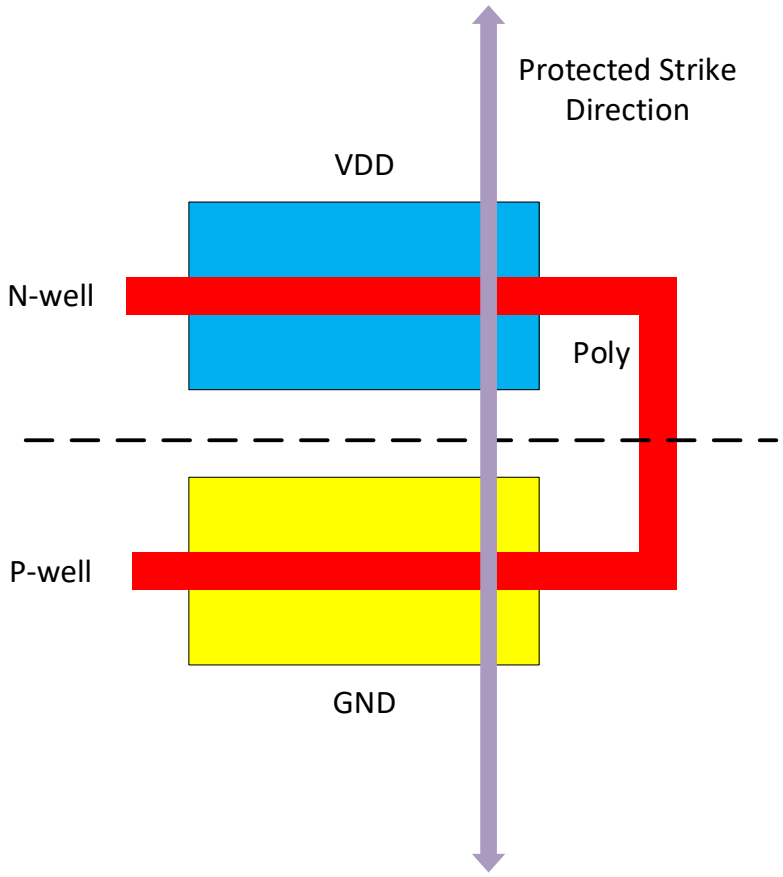

Figure 3.10: Layout for an inverter using LEAP

This error-detecting code for data transmission is also used to detect data errors in storage integrated circuits such as SRAM, which uses multi-bit storage for one word.

A parity check is the easiest way to detect an error because the redundant area is small and there is no obvious delay. To finish this function in the circuit, some Exclusive-OR(XOR) gates are needed. Table3.1 is the truth table for an exclusive OR gate:

However, the parity check is just an error detecting code which means it cannot fix any error and even cannot detect which bit is the error one.

3.4.2 Hamming Code

Invented by Richard Hamming, Hamming code is a linear debug code used in the communication field in 1950 [46]. It is used in computer storage error-detecting and correcting. Before it was created, there were other error-detecting codes. However, unlike them, the Hamming

Table 3.1: Truth table of exclusive OR gate

Inputs		Outputs
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

code uses the familiar concept with parity check. It adds extra bits to detect error and it can also correct errors. The principle of the Hamming code is to insert k bits as a check digit to make n bits of data extend to (m = n + k). The principle for choosing how many bits can be expressed by

$$2^k - 1 \geq m(m = n + k) \tag{3.1}$$

This is called the Hamming inequality. The Hamming code rule puts the code bit into every 2k bits, and put other data in the original order.

This general algorithm can make a single error correction for any of the bits in the data, and can be described as follows:

- Order all the data from left to right: 1, 2, 3, 4, 5;
- Convert all the order numbers into binary: 0, 01, 10, 11, 100;
- The check digit should be ascending powers of two, such as 1, 2, 4, 8. Insert the Hamming code into that place. The rest of the data should be the original data, and the order should not be changed and all data should be present in every two or more Hamming code bits. The Hamming code in each position is determined by the binary number transferred from original data. For example:
  - The first Hamming code digit should present all the original binary data first digit which is 1, such as 11, 101, 111, 1101.

- The second Hamming code should present all the second binary data digit which is one, such as 11, 110, 1011.
- The fourth Hamming code should present all the third binary data digit which is one, such as 101, 110, 1100, 1110, 1101.
- In summary, the Hamming code digit covers all the data. The Hamming code check can be an odd or even check. An even check is easier in the math area, but for actual circuit design, there is no difference.

3.5 Simulation Tools Introduction

In this project, a new tool called TFIT provided by iRoC Technologies company will be used to simulate the radiation environment and get a simulation result, such as a cross section and Failures in Time(FIT) value [47], [48], [28].

TFIT is a high-speed simulation tool, that can be used to predict and improve the Soft Error Rate(SER) and FIT performance of cell designs. It allows reasonably accurate calculation of the electrical effect of particles impact on a transistor, cell, or circuit early in the design flow, and at much faster speeds than traditional 3D Technology Computer Aided Design(TCAD) simulations.

TFIT can do the following tests:

- Calculation of the effects of a single-charged particle on a digital semiconductor structure;
- Calculation of the cross section corresponding to a sensitive area within a circuit and a specific type of incident charged particle;
- Calculation of the critical charge;
- Calculation of the SEU FIT value for an SRAM or memorizing cells such as flip-flops;
- Calculation of the SET FIT value for combinatorial cells;
- Calculation of the Multiple Cells Upsets'(MCU) FIT values for an SRAM;

- Calculation of the alpha particle cross section for combinational and memorizing cells;

TFIT also provide the opportunity to evaluate devices sensitivity in the early design cycle. This allows researchers to reduce time for products, design efforts.

TFIT has three main modes, they are ion, alpha, and neutron. In ion mode, TFIT can simulate the effect of a single particle simulation, calculate the cross section and calculate the critical charge. In alpha mode, accelerated alpha testing can be simulated given the test set-up information. In neutron mode, two sub-models are possible: thermal neutron and fast neutron.

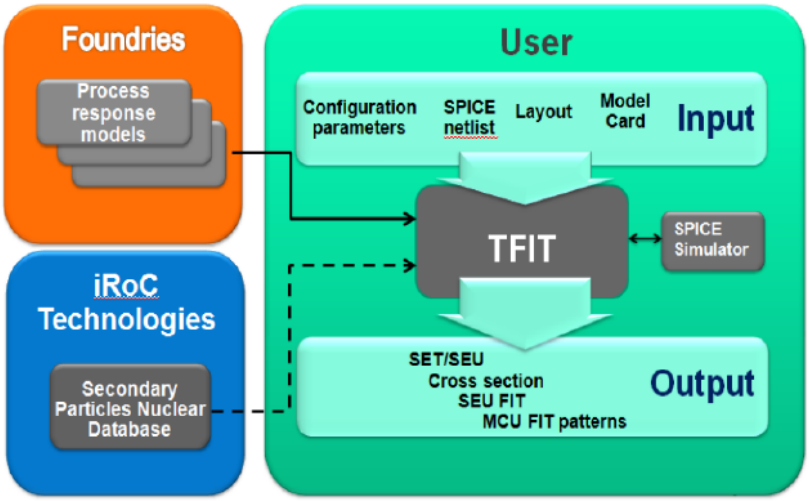

Figure 3.11: TFIT working flow [47]

Figure 3.11 shows the TFIT working flow and what source files are needed. Components are as follows:

- Configuration parameters. This is a script that is used to drive and guide the tool;
- The SPICE netlist. A parasitic should be included in this file for accurate analysis;
- Layout. This is the geometry description of the design. TFIT will use the information in this layout to estimate charge-sharing effects;
- Model card. This is the SPICE library file provided by the foundry;

- Process response models are models contain the devices responses to single-events. These responses are obtained through the TCAD simulations. The models are technology specific, and the accuracy of the estimation results depends heavily on them.

- Secondary particles nuclear database. This database is needed to provide an estimation of secondary particle creation.

It should be noted that TFIT itself cannot complete all the tasks required for the SER analysis. At least one SPICE simulator must to be installed and activated before launching the TFIT simulation. The SPICE simulators supported by TFIT are Synopsys HSPICE and Mentor Eldo.

Table3.2 summarizes all the modes for a TFIT simulation and the description for each mode. In the process of this project, one of the most commonly used modes is the cross-section mode. Proton simulation is very common because protons in the space radiation environment are the most common particles.

Table 3.2: TFIT modes summary

Mode	Description
Inside Drain	Single particle hit
Critical charge	Nodal critical charge simulation
Cross Section	Cross-sections analysis
Impact xy	Simulations of particle hits at user-defined locations
Angular map	Particle-hit locations scanning
Neutron	Neutron radiation simulations
Alpha	Alpha radiation simulations
Proton	Proton radiation simulations

The TFIT simulation can calculate the states for each node. If the configuration file does not mention the input state signals, TFIT simulates all possible states.

The output of TFIT has two components. The first is the log file results. It contains the cross section and FIT value. In angular map mode, there is only the cross section mode. In neutron and proton modes, the result file contains both the FIT value and cross section. The

second output file contains the cross-section layout figure. It shows the layout and sensitive area in different colors. This information is used to detective if the circuit is sensitive and, if so, which part is sensitive.

3.6 Sense Amplifier Design

A sense amplifier (SA) is an important part of SRAM. It connects with the bit line, BL and BLB. It has a significant effect on the performance of the whole memory circuit. When the charging and discharging capability of the memory device are weak, and the capacitance of the connection between the SA and bit lines is large, the weak electrical conductivity of the cell makes the voltage swing of the bit line very small when reading is in progress. Apart from that, it takes a long time to drive the bit lines to the standard circuit level. In the output of the reading circuits, an SA must be placed to increase the speed and driving capability. When reading starts, the chosen cell opens and the storage unit discharges to the bit line. In general, the bit line will be precharged to a certain level, and the reading process is the discharge process of a single bit line. When the bit line voltage rises to a certain level, usually under a few hundred millivolts, the SA will be turned on and raise the small voltage to the logic 1 or 0 immediately, and send the data to the output.

Due to the inherent difference characteristics of SRAM circuits, all the SA should have differential input. The differential input structure has excellent anti-noise performance. This structure can provide an excellent common mode rejection ratio (CMRR) and a power supply rejection ratio (PSRR). The larger these two values, the better the performance of the SA [49]. The anti-jamming capability is also better.

In the overall structure, the SA and operational amplifier are both two-port network circuits. Both amplifiers can amplify the input signals and output amplified signals.

- Compared to a normal amplifier, the gain of sense amplifiers is small. The typical values of an SA are from 10 to 100. The ideal operational amplifier can amplify the signal to infinity because the input signals of the operational amplifier are very small and at a very high frequency. The input of an SA is larger. It varies from dozens to hundreds of millivolts.

- Operational amplifiers have strict output distortion requirements. They require amplified signal protection to hold the original characteristics of the signals. There is a limitation of the distortion.

- Operational amplifiers' output range is small. The output of the signal should hold the original characteristics, and MOS transistors should work in the saturation region. For the SA, the best logic level is 1 or 0. When all the signals of the device are stable, they are all in the cut-off region.

- Operational amplifiers are usually complex. They have some regenerative circuits and compensating circuits. The SA is a regenerative circuit. It can speed up the process of amplification.

- The speed requirement of an operational amplifier is not very high. To achieve the function of the circuit, researchers sometimes even add a delay of the output. For the SA, the speed limit is very high.

Figure 3.12 is the SA operation timing diagram of the SA. The voltage difference between BLB and BL is very small. The output is the red line and blue line.

The SA in SRAM should be a differential amplifier. In this kind of amplifier, the SA can be divided into three different types: an operational amplifier, a cross-coupled amplifier, and a latch type amplifier. Among the three types, the first two: operational and cross-coupled, have a differential amplification structure. The third one, the latch type amplifier does not have a differential amplification structure. It has been widely used in designing high-speed and low-power consumption amplifiers.

3.6.1 Operational Sense Amplifier

The typical operational sense amplifier is shown in Figure 3.13. BL and BLB are the two inputs for the SA. These two lines are the same as the SRAM bit line, BL and BLB. Data a and Data b are the two outputs. One of them is the storage data in the SRAM cell, the other one is the invert data.

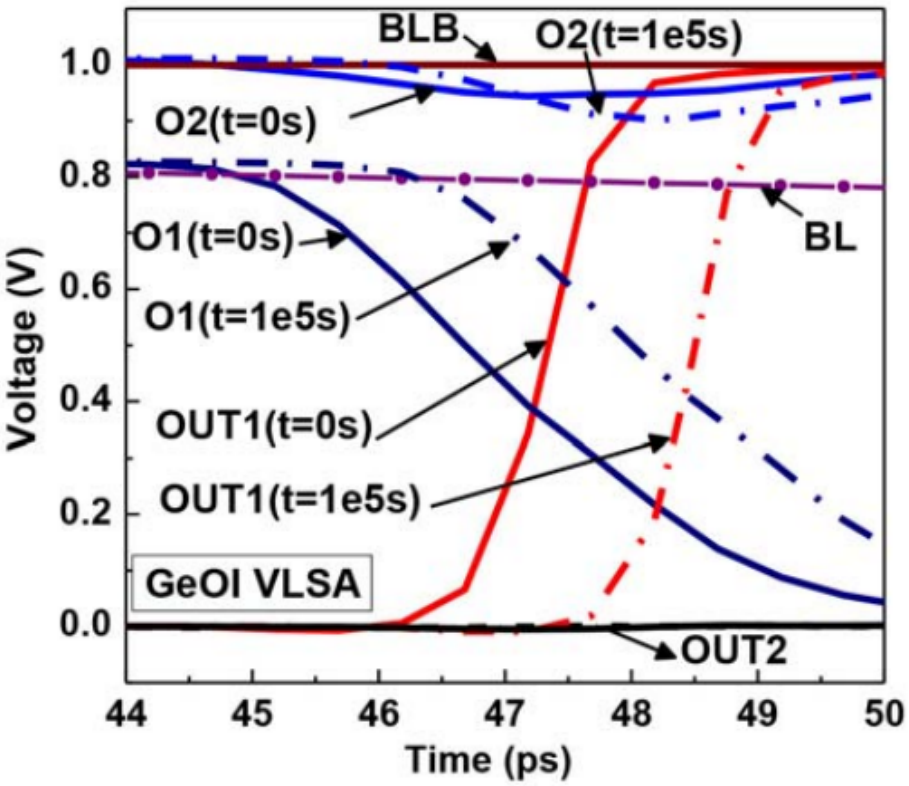

Figure 3.12: Timing of a sense amplifier [50]

In Figure 3.13, the MOS transistors, M1, M2, M3, and M4, and the current source consist the whole operational sense amplifier. M1 and M2 consist of the differential transistors. M3 and M4 are the mirror load. The rest is the biasing circuit which is located on the top of the circuits. The function of the biasing circuit is to provide the static biasing voltage for the whole circuit and set up the quiescent operating point. After the output of this operational sense amplifier, there should be a buffer circuit to increase the driving ability.

The operational sense amplifier structure is source coupled. In order to increase its magnification capacity without increasing the area and power consumption, it uses M3 and M4 as the mirror load and replaces the traditional resistive load. Comparing with the current of M1 and M2 can get the operational sense amplifier gain. The gain of the amplifier can be expressed as.

$$A = \frac{2g_{m2}}{I_{SS}\left(\lambda_2 + \lambda_4\right)} \tag{3.2}$$

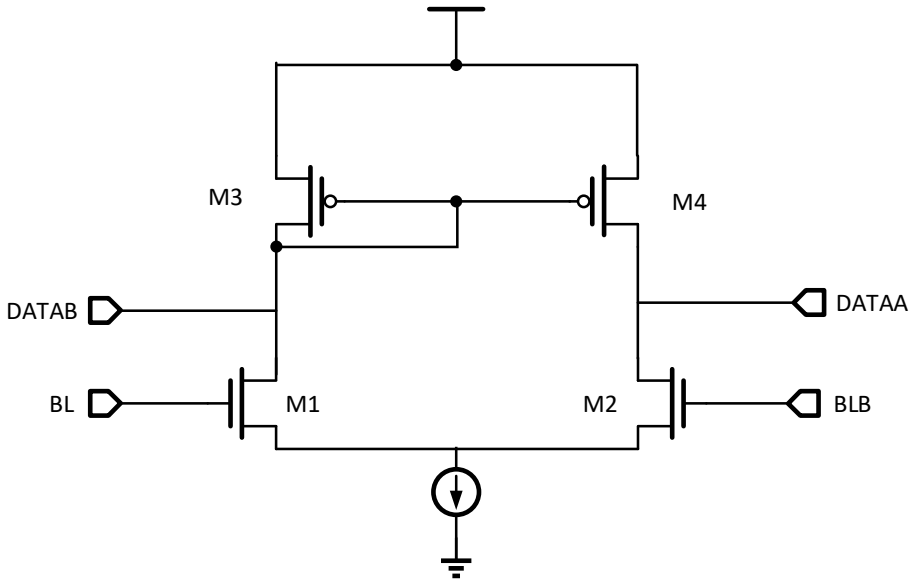

Figure 3.13: Typical operational sense amplifier

In this equation, A is the gain, g is the transconductance of the input transistor M2, and λ is the channel length modulation factor. I is the current from the current source. It is separated into transistor M1 and M2. The features of the amplifier are as follows:

- This amplifier has a big gain, and is also very sensitive. It can amplify and get the logic high and current level low even if the voltage difference is very small

- In an ideal situation, the common-mode gain is 0. It has a very high common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR).

- The operational sense amplifier has two inputs and one input. For those designs which require two outputs, the designer must use two of the same amplifiers. This is a waste of layout area.

- The speed of this amplifier is not as high as the other SAs and the delay of this amplifier is high.

3.6.2 Cross-coupled Type Sensitive Amplifier

The cross-coupled type sense amplifier is the second type of amplifier to be examined because it has a higher reading speed, which is more important in modern memories. For this reason, the operational sense amplifier is not commonly used nowadays. The cross-coupled type sense amplifier can solve this problem. Figure 3.14 shows the structure of the cross-coupled type sense amplifier.

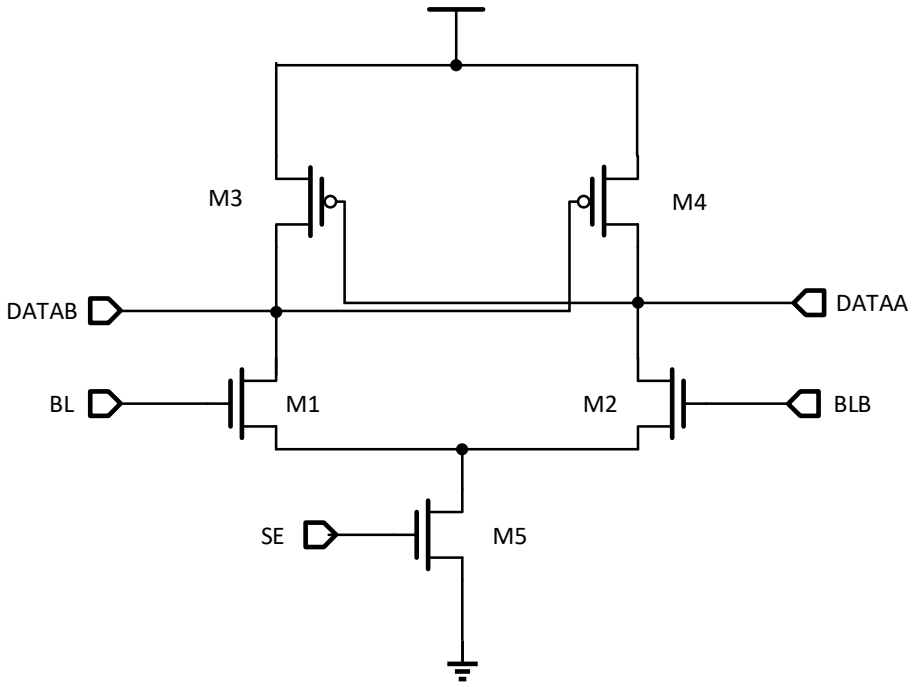

Figure 3.14: Cross-coupled type sensitive amplifier

The high-speed performance for the cross-coupled type sense amplifier is a result of its two pMOSs, M3, and M4 which combine the positive feedback. For example, if the voltage of the BLB decreases, the voltage of the DATA node will increase. The gate voltage of M3 decrease, and the current passing through M3 also decreases. The voltage of the DATAB node will decrease, and the feedback will make the gate voltage of M2 increase. The current of M4 will increase. The voltage of the DATA node will also increase and form positive feedback until it remains stable. The SE signal is used to control the transistor M5. It is the switch of the whole circuit. When the data arrives, the SE signal turns on the circuit. This

makes the SA energy efficient.

- The advantage of this type of amplifier is high-speed performance.
- The disadvantage of this structure is that the noise can cause an error state in the latch structure, and then the SA will not work. The transistor size design and the timing table set up are all difficult problems.
- Another disadvantage is that the gain of the cross-coupled type sense amplifier is small.

3.6.3 Latch Sensitive Amplifier

The third structure to be introduced is called the latch sensitive amplifier. It is widely used because of its outstanding advantages and unique way of amplification.

The basic structure is shown in Figure 3.15. This SA is first used in DRAM design. The core of this structure is the cross-coupled inverters, also called the latch. It is a positive feedback structure, which helps speed up the amplification. BL and BLB can be regarded as the two inputs and the two outputs. The transistor M5 controls the whole circuit. It makes this SA power efficient. When the SA is in high level, M5 turns on, and the circuit starts to work. In the working process, suppose the signal on BL is high. The SA can then push the BL to a strong high level. Through the action of two the inverters, the signal on BLB is pulled down. The signal then travels between BL and BLB. The two sides have only one transistor open. The current from the source does not go to the Ground (GND) directly, so the static power consumption is 0. Figure 3.15 is the schematic for the latch sensitive amplifier.

The final structure is a basic structure called a modified latch sensitive amplifier. It is also called difference latch sensitive amplifier. Figure 3.15 shows that the input and output are the same. As mentioned previously, the number of SRAM cells connected with the one-bit line is very large. The stray capacitance is also very large. In the process of amplifying, if the amplifier pulls the voltage on a bit line, the delay the power consumption is very high. This kind of latch SA is not used very often.

In an SRAM, in order to separate the input and output of the SA, researchers usually use the modified SA shown in Figure 3.16, which has three more transistors compared to Figure

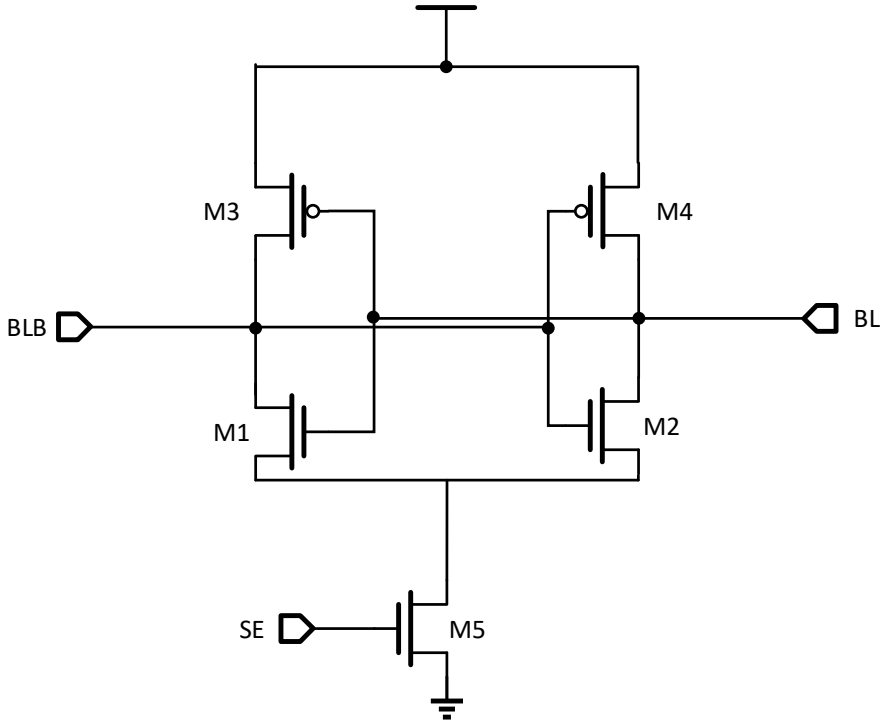

Figure 3.15: Basic SA schematic

3.15. In this circuit, M7 is the balance transistor, M8 and M9 are the different transistors, and EQU is the balance signal. EQU is used to control the output status. When the EQU signal is low, the two output signals are equal to each other. When the SE signal is high, the SA starts to amplify the signals. At that time, M7 cannot be closed immediately. A small difference between the two sides can start the positive feedback. Only when the difference between the two differential input voltages of the amplifier reaches a certain tolerance, can EQU be closed and the SA start working.

When the SE is high and EQU has been closed, BL and BLB will be precharged to Voltage Drain Drain (VDD). The transistors M1, M2, M3, and M4 are all working in the saturation area, according to the differential half circuit equivalent method, in a semi-stable state. This circuit is a negative source feedback common mode amplifier circuit. The M6 is the switch and the resistance can be ignored.

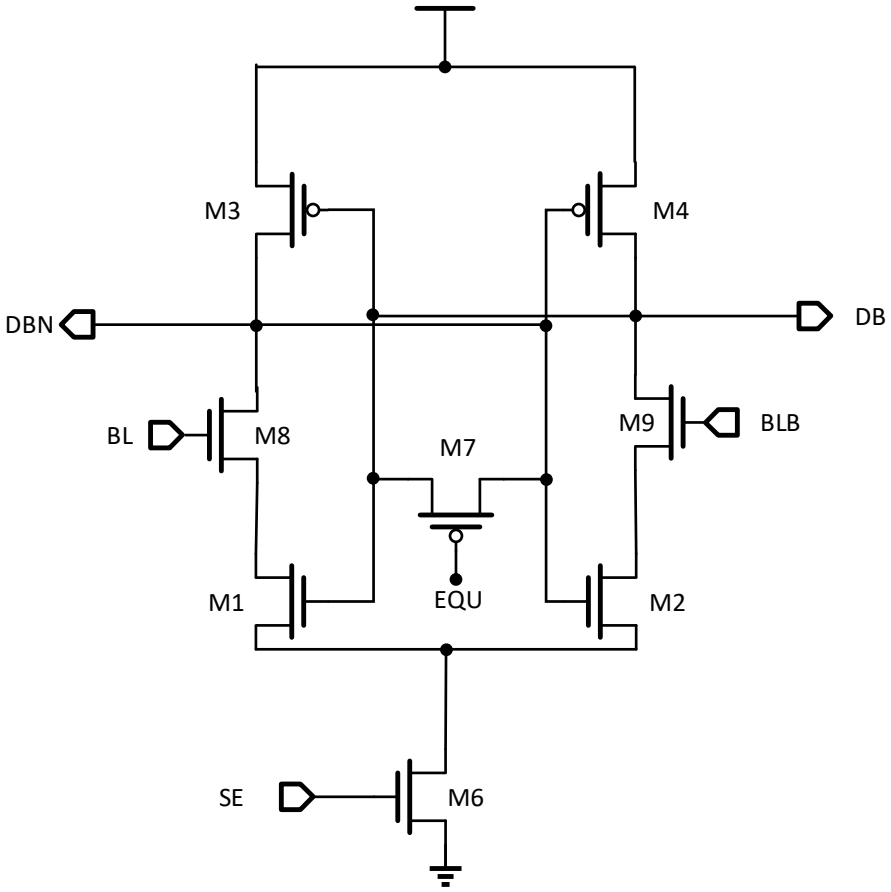

Figure 3.16: Modified SA

4. SRAM Design

This chapter introduces the overview of the proposed Static Random Access Memory(SRAM) structure, and presents each individual block design of the SRAM. Hamming code design embedded in this SRAM is also described. A novel sense amplifier is also developed in the last section of this chapter.

4.1 Memory Design Overview

SRAM is usually used as a level 2 cache. The speed of SRAM is high, but the power consumption is large. It has low integration and a high price. SRAM can also be separated into asynchronous SRAM and synchronous SRAM. The access of asynchronous SRAM is independent of the clock. The input and the output are controlled by the address signal. If the address changes, the output and input receive the signal. Synchronous SRAM works differently. It has a clock to control all the input and output. SRAM is composed of a storage array and a peripheral control circuit. The control circuit consists of a sense amplifier, an address decoder, and a read and write circuit. Although the function behavior is determined by the semiconductor process. However, a better layout array can also increase the function. A good design of the peripheral control circuit also increases the function of the whole circuit.

In SRAM, the address signal needs the decoder to choose the correct cell and read or write the data. The basic storage consists of six transistors. There are two cross-coupled inverters to save the signal. This cross-coupled structure gives the SRAM high reliability and speed. However, it has the disadvantage of not being highly integrated. The back-to-back structure can be either 1 or 0 as decided by the control circuit. By arraying the cells into different rows and columns, an SRAM storage array can be created. This storage array is the main part of the entire SRAM.

Figure 4.1 and Figure 4.2 show the SRAM reading and writing operation timing.

In this thesis, a novel design of an asynchronous SRAM with radiation-tolerant capability

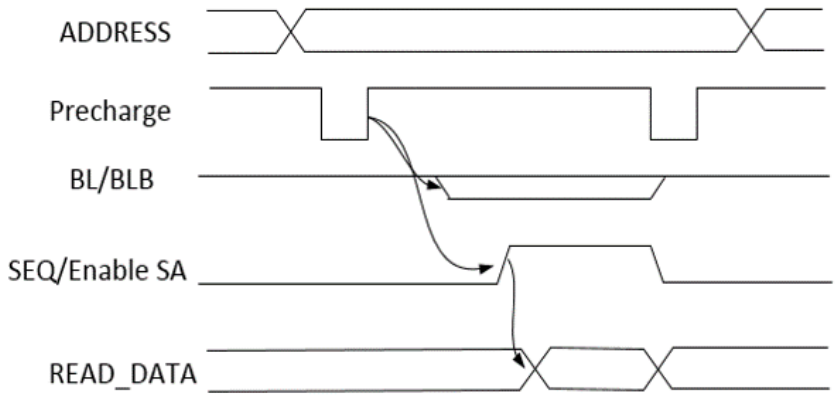

Figure 4.1: SRAM reading operation

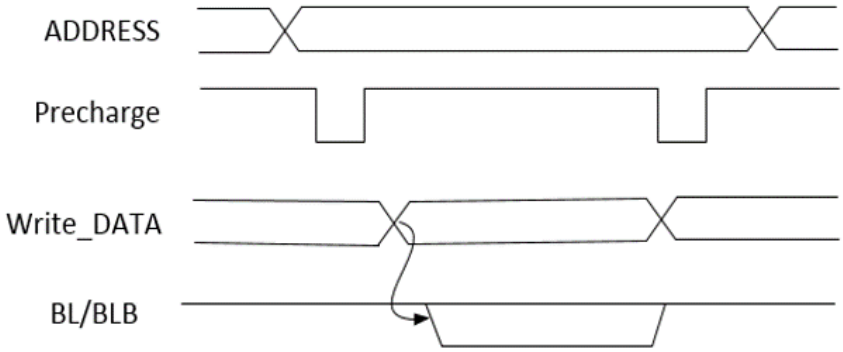

Figure 4.2: SRAM writing operation

is presented. The size of the SRAM is 8 bits x 2M, and there are 32 blocks x 512k. In each block, there are 512k bits cells. The 512k consists of 512 rows x 128 columns x 8 bits.

Figure 4.3 is the whole SRAM design. The page decoder has nine inputs from A0 to A8 and 512 outputs for each cell in each column. The page decoder helps to choose a page from the 32 blocks.

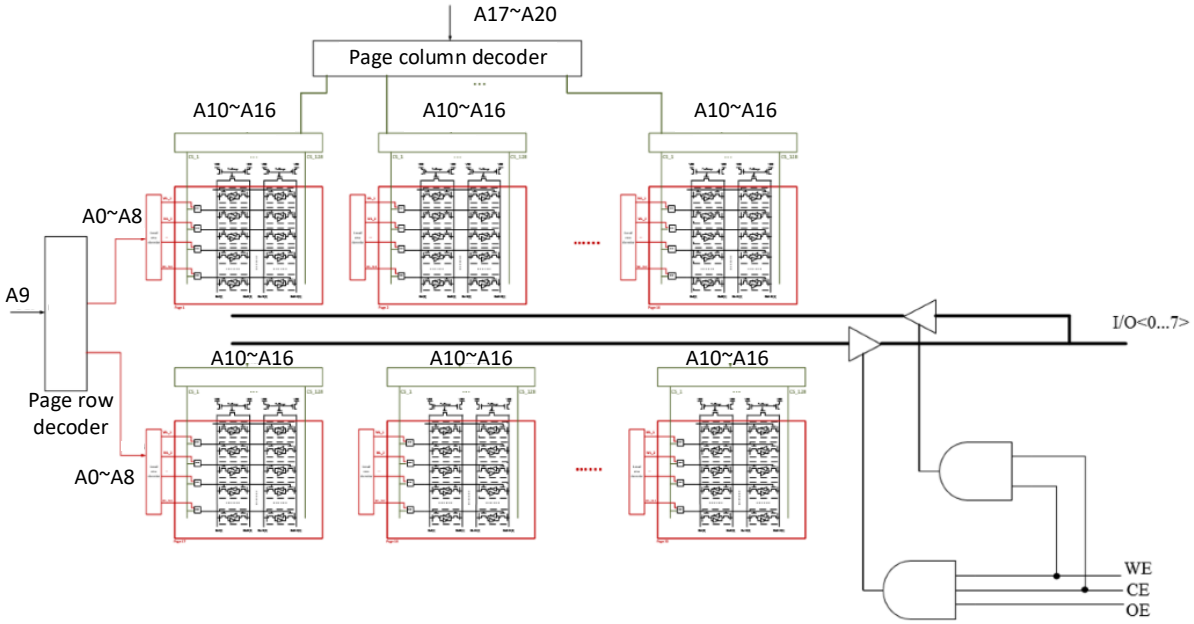

Figure 4.3: Whole SRAM design diagram

Figure 4.4 is the block design detail. The input signal of each cell in each column comes from the local row decoder. The local column decoder and the row decoder combine to choose which 8-bit cells are the ones which have been accessed. Address-Transition Detector (ATD) is the control signal generator. Once the address changes, the ATD will generate the signal to control the reading driver, writing driver, and precharge for the cells. In each block, there are 128 columns which match with the signal from CS1 to CS128 from the column decoder.

On the outside of the SRAM storage array, it is the decoder and external signal interface circuit. The layout of the array is usually a square or rectangle. This reduces the whole area of the circuit and access to the data. The peripheral circuit controls the signal read and write, they can be divided into several parts:

- The address decoding logic completes the row and column selection;
- The changing of the address drives the reading and writing control;
- The reading logic circuit completes the reading of the data and sends the data to I/O;
- The writing logic circuit captures the input data and saves the data into storage;

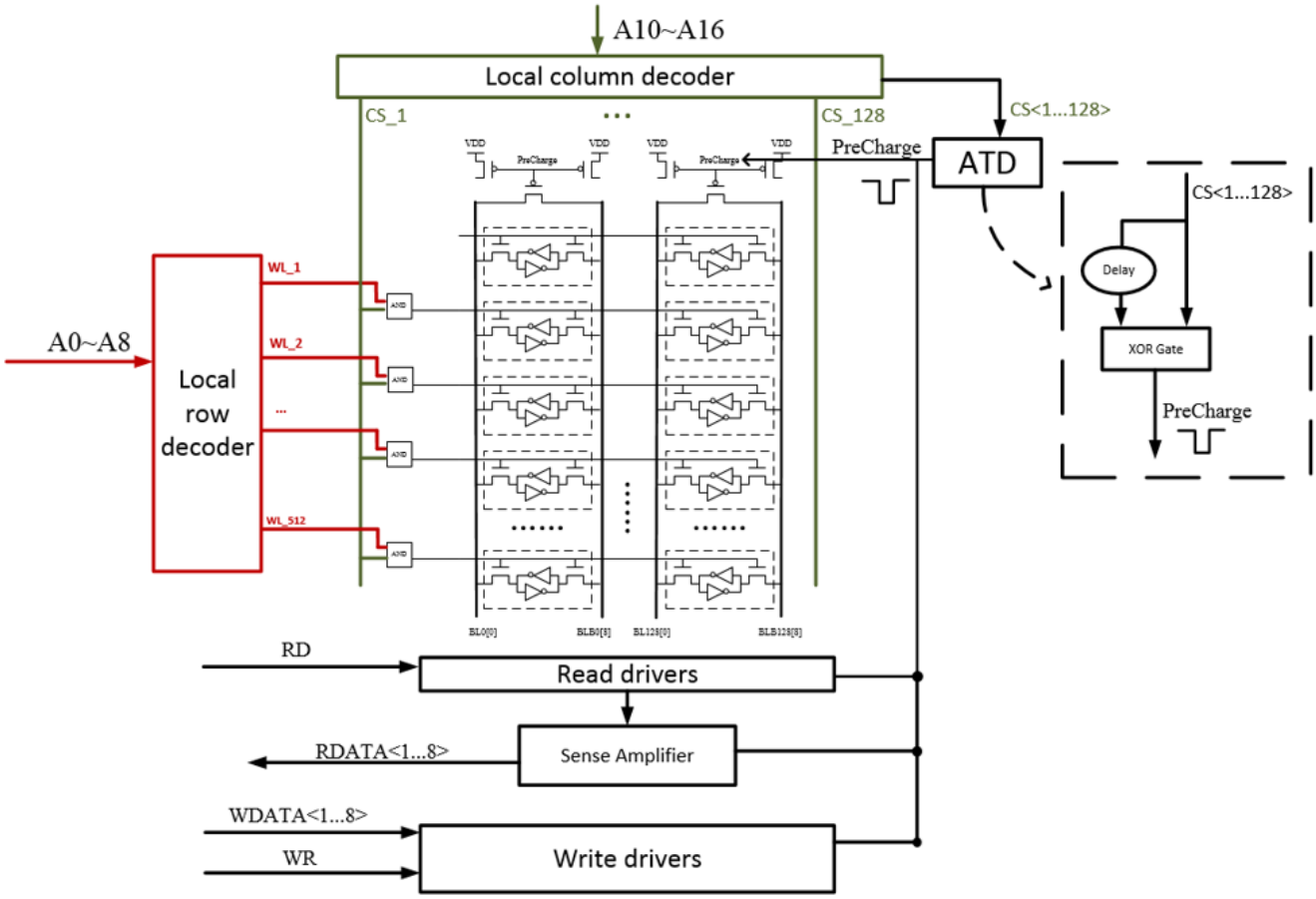

Figure 4.4: SRAM block design

- The sense amplifier can read the data from the small signal and reduce the delay of the circuit.

4.2 Memory Cell and Circuit Design

4.2.1 Memory Cell

The most widely used SRAM cell is combined with six transistors, and is called the 6T SRAM cell. This cell contains two identical inverters that are connected back-to-back. Transistors are labeled P1, N1, and P2, N2. These two inverters are driven by a word line (WL), called N3 and N4. N3 and N4 are also connected to bit lines. Those two lines' function is connected to the nodes Q and QB, and they read and write data to the cell. The P1, N1, P2, and N2s

function is to hold the signal in the cell; N3 and N4 are just like a switch to turn the cell on and off. There are three basic states of a standard SRAM cell: standby, reading operation and writing operation.

The SRAM storage unit size setting should not only be small but also reliable. Therefore, there should be some restrictions between the different transistors in order to avoid destroying the data stored in the cell.

The process of setting the 6T SRAM cell transistor size is as follows:

- Based on current technology, find the smallest transistor size;
- Based on the theory restrictions, find out the size relationship between the different transistors;
- After setting all the transistors' sizes, using simulation software to test the simulation result;
- Adjust the parameter and do the simulation again.

To ensure the correction of this CMOS 6T SRAM cell transistor W/L, there are two basic rules to consider:

- Data read operations should not destroy information stored in storage units.
- The storage unit should be able to allow changes in the stored information during data writing.

Figure 4.5 shows the schematic of the 6T SRAM cell.

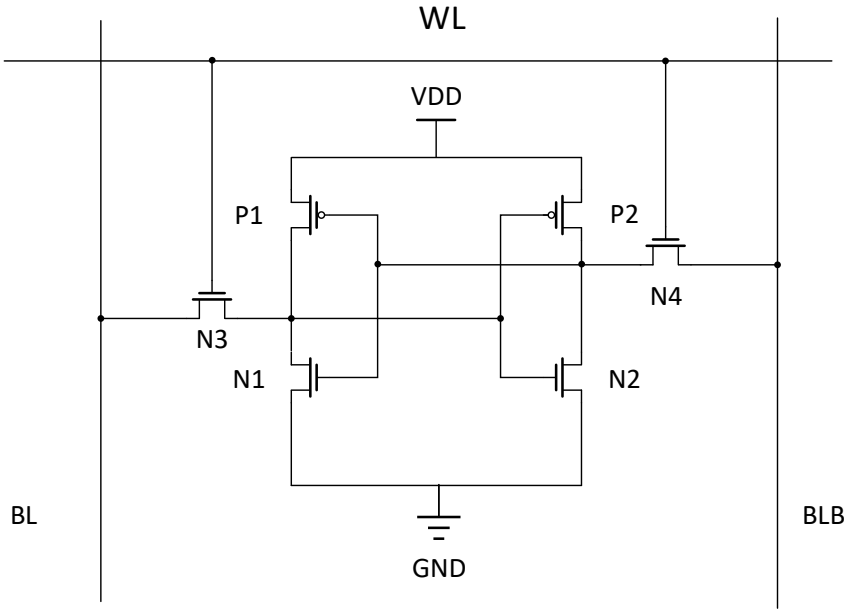

Figure 4.5: A 6T SRAM cell

4.2.2 Address Decoder

The address decoder is a key part in an SRAM circuit. The design of this decoder has a high requirement for speed and power consumption. In the large storage designs, the delay of the decoder consists of up to 50% of the total circuit delay. The address decoder consists of row decoders and a column decoder. The column decoder is used to choose the column. The row decoder is used to choose which single cell to turn on in order to write in or read from data in one column. Before the signal from the row decoder and column decoder go through the 6T cell, there should also be a logic gate to combine the two signals. This logic can be divided into dynamic logic circuit and static logic circuit. In a static circuit, researchers can use a NOR gate or a NAND gate. The NOR gate is much faster than the NAND gate, but needs more layout area and more power consumption. Figure 4.6 shows the schematic of a decoder. In this schematic, A0 and A1 are the two inputs. D0 to D3 are the outputs.

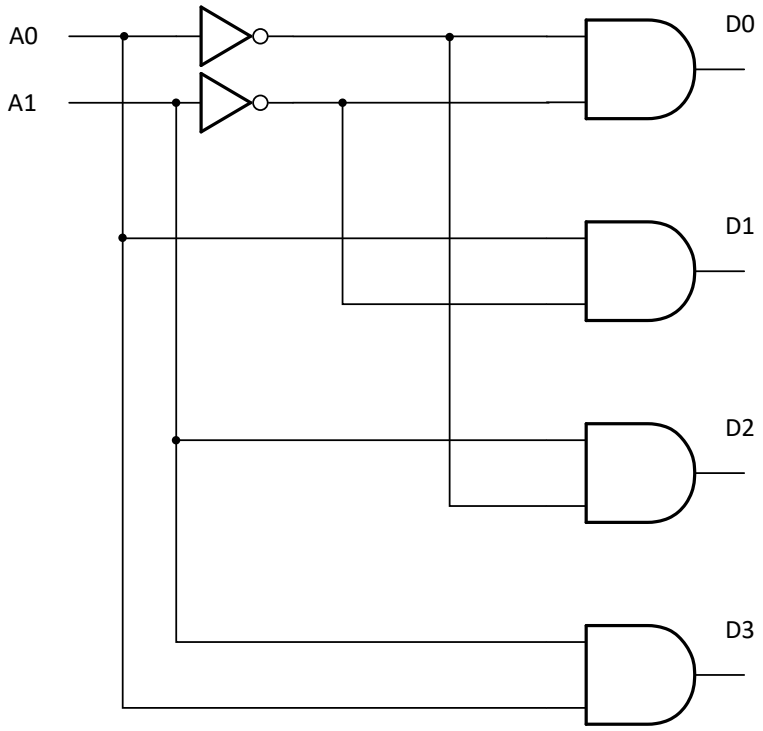

Figure 4.6: 2 To 4 decoder

This SRAM is 2M x 8 bits, can be divided into 32 blocks x 512k. Since there will be four extra bits adding for the Hamming code, the 2M x 8 bits will become 2M x 12 bits. The row decoder for the SRAM column is a 9 to 512 bit decoder.

4.2.3 Precharge

A precharge circuit is designed for SRAM reading progress because there are lots of cells connected with bit lines (BL and BLB). It is not possible to let the data voltage drive the memory cell. The precharge circuit is used to precharge the bit lines (BL and BLB). It helps to pull the two lines to a high voltage before the write operation. Figure 4.7 shows a simple precharge design.

For this design, the precharge circuit has low-level sensitivity, which means that when the precharge does not work, the circuit should be high. When the precharge needs to work for the SRAM writing, the level should be low.

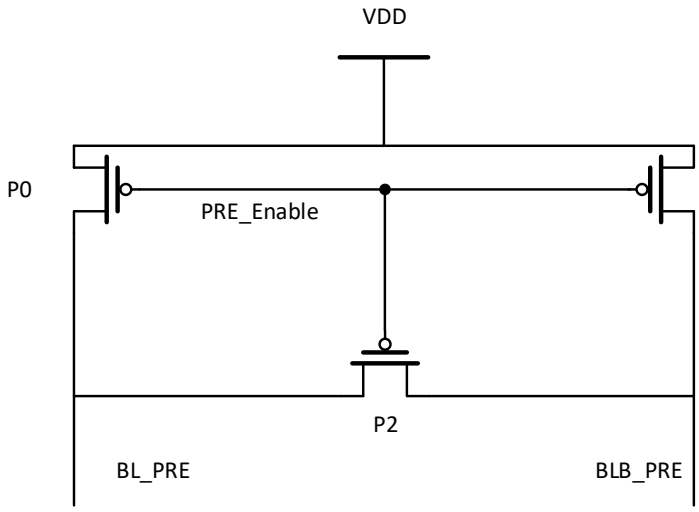

Figure 4.7: Precharge schematic

4.2.4 Address-Transition Detector

An ATD is used for an asynchronous SRAM. Because there is no clock, an asynchronous SRAM needs a signal to drive the circuit. In a synchronous SRAM, a master clock is used working during the reading and writing. In an asynchronous SRAM, the address changing can be captured as a signal by the address transition detector. When the address is changing, the ATD can help to produce a pulse. Usually, an ATD consists of a wide OR gate and a delay. If an address changing signal comes through the ATD, the signal going through the delay will arrive later than the other line. When the first line changes and the line with the delay do not change, the OR gate will recognize the difference and generate a data change. After the signal to pass the delay and the two inputs of the OR gate become the same, the OR gate output will be restored. Figure 4.8 shows an ATD working flow.

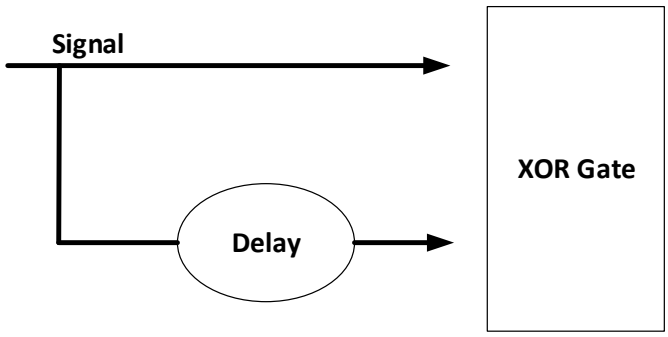

Figure 4.8: ATD working flow

There is also an ATD in this project. For every transition of an address bus, there will be a pulse of the output of the structure. In some large circuit designs, the pulse generated by the ATD is not powerful enough to drive the rest of the circuit so sometimes there is a buffer after the ATD circuit. However, this increases the delay of the signal. Figure 4.9 is the ATD schematic.

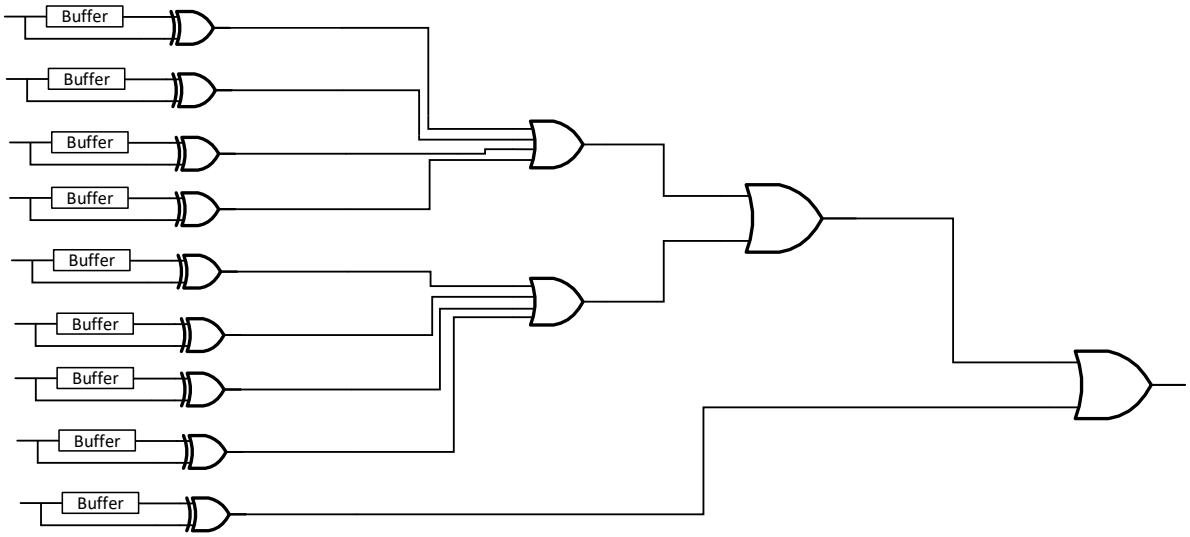

Figure 4.9: ATD schematic

4.3 Standby

Standby means the cell does not have any writing or reading mission and it keeps the states static. If the word lines are all low, N3 and N4 are closed. Then the basic cell and the BL and BLB are separated. The two connected inverters (N1, P1, N2, and P2) keep the current state.

4.4 Write Operation

It can be assumed that the beginning state is Q = 1 when writing 0 into it. BLB should be high, and BL should be low. WL is the control line and should be open. Both N3 and N4 turn on to make the signal access to Q and QB. Q must be low enough to make sure that it is lower than the threshold voltage. When Q is low enough, P1 on and N1 off. When designing the size of the transistors, the N4 should be bigger than P2. That can make the data write into the cell. This is the formula for choosing the correct size. The result of the formula is the pull-up ratio (PR).

$$PR = \frac{W_{P2}/L_{P2}}{W_{N4}/L_{N4}} \tag{4.1}$$

The result of PR must be smaller than 1.8.

Figure 4.10 shows the simplified model of the SRAM cell writing operation.

4.5 Read Operation

Assume that the current storage is 1, which means the Q is in high level. At the beginning of the reading cycle, the two-bit lines BL and BLB are precharged to high. Then, WL goes high. This makes the two transistors mentioned before, N3 and N4, open. In the second step of reading, the 1 stored in Q and this data is sent to BL, which is also the precharge voltage. The charge on BLB goes low, because the transistors N2 and N3 connect this node to the ground. On the other side, BL stays high. Transistors P2 and N4 make VDD connect to BL. If the storage is 0, the different circuit status will make BL 0. The difference between

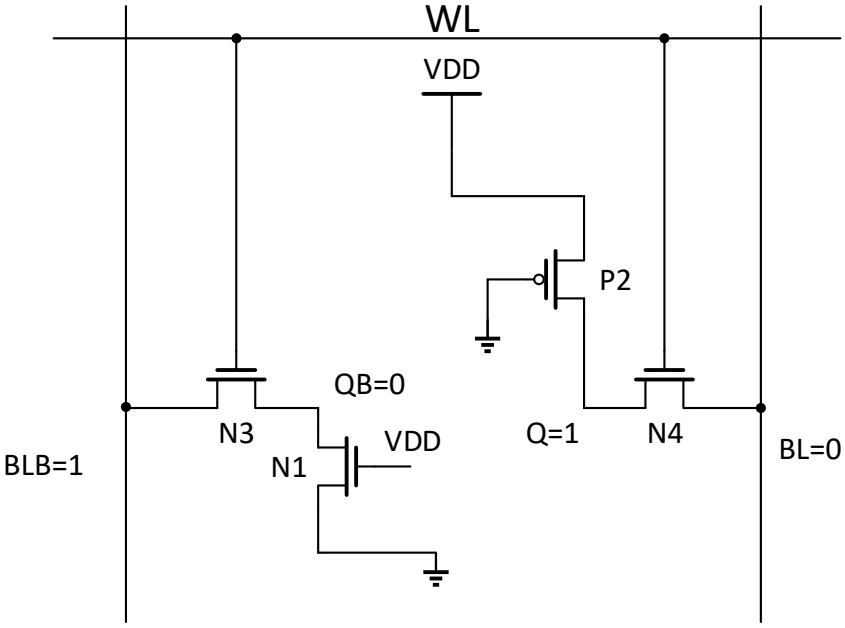

Figure 4.10: Simplified model of 6T cell during write

BL and BLB needs to be very small. The amplifier will recognize them and generate output. There is also a formula for the constraint ratio (CR). The CR must be greater than 1.2.

$$CR = \frac{W_{N1}/L_{N1}}{W_{N3}/L_{N3}} \tag{4.2}$$

Figure 4.11 shows the simplified model of the reading operation.

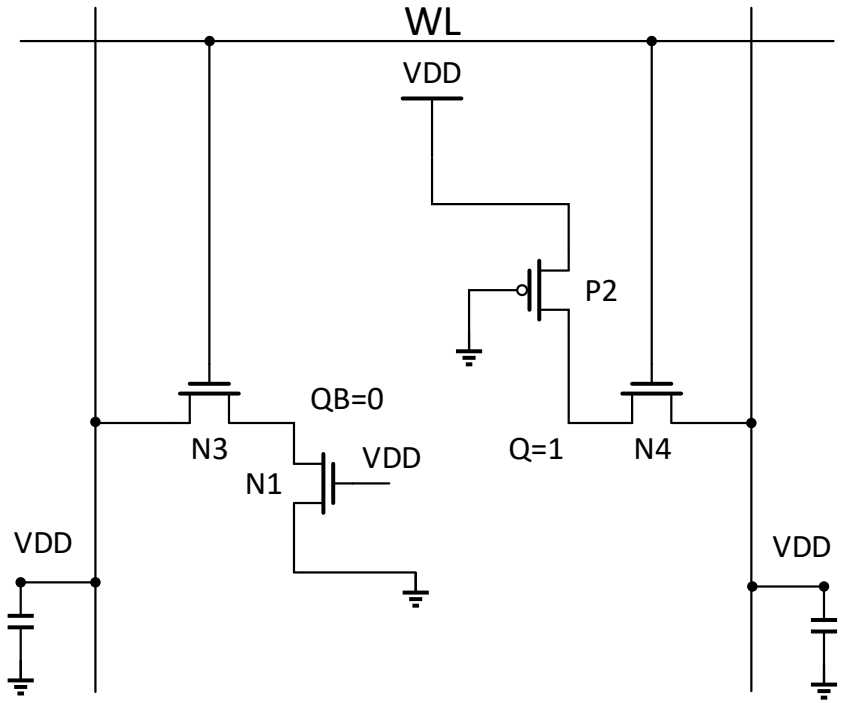

Figure 4.11: Simplified model of 6T cell during read

Figure 4.12 is the schematic of the reading driver. A signal from the precharge goes through an inverter and opens the read driver. The SA starts receiving the signals from BL and BLB. The output of the SA is the data output.

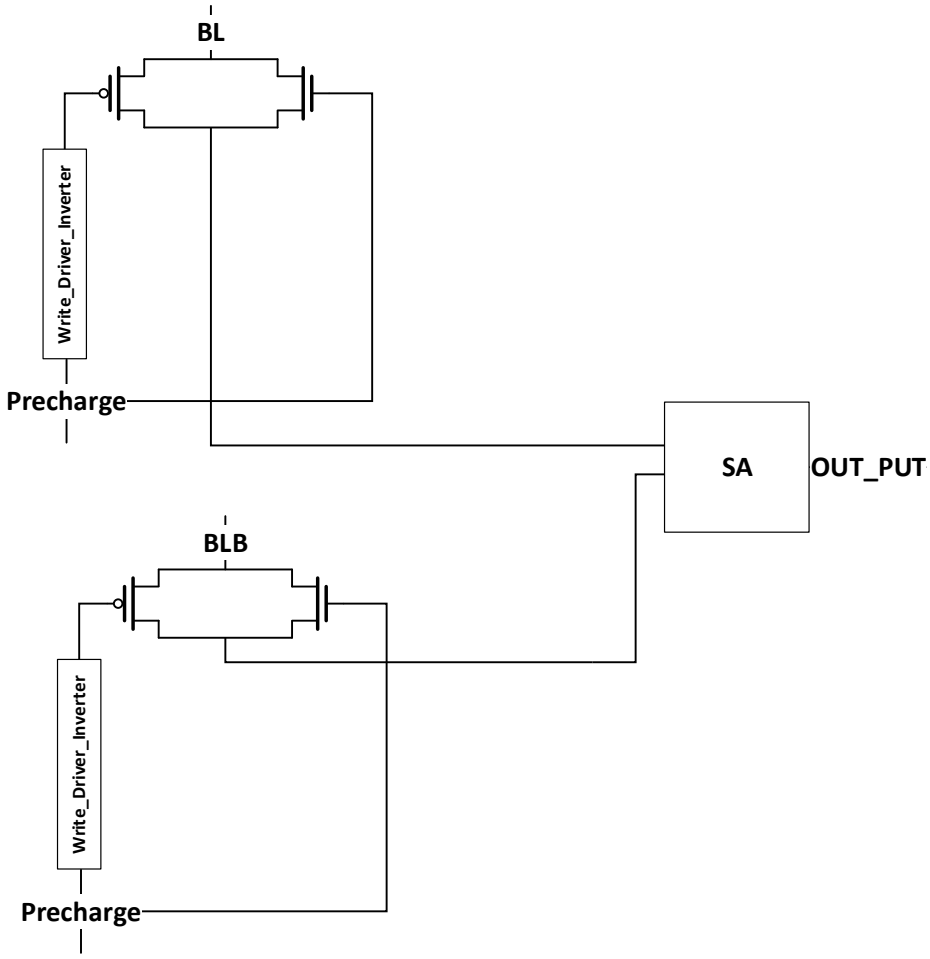

Figure 4.12: Read driver schematic

4.6 Hamming Code Design

This section discusses the operation of a Hamming code circuit. The three different functions of the circuits are finishing the whole encoding, decoding, and error-detecting and correcting operation. The first Hamming code circuit is placed in the input of the SRAM. Before writing the data into the storage cells, the Hamming code circuit finishes the encoding process. The output from the first part of the Hamming code circuit is four extra bits for every 8 bits of data. After the encoding process, the 12 bits of data are written in through the write driver and stored in the 6T SRAM cell. The other two parts are set next to the output of each cell. After the reading cell finishes reading the data, the sense amplifier separates the two signals.

When the data come out of the output node of the SA, it is sent into the second part of the Hamming code logic circuits. The function of this part is to detect the data if there are errors generate. The last part of the Hamming code logic is to fix the error since the data in the digital logic circuit has only two states: 1 and 0. Once detected the error, invert the data, the data will be fixed.

This design is a 2M x 8 bit asynchronous SRAM. There should be a three-bit Hamming code for every 8 bit of data. The following example shows how Hamming code works in SRAM.

Step 1. If the data is set as D, and the Hamming code as X, this is the form for the 8-bit and 4-bit Hamming codes. There are a total of 12 bits in this word. The numbers of the bits in binary are:

0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100.

Four of the binary numbers have only one 1. They are 0001, 0010, 0100, 1000. They are the numbers that are set as the Hamming code. Table 4.1 is the Hamming code data converted into binary.Step 1. If the data is set as D, and the Hamming code as X, this is the form for the 8-bit and 4-bit Hamming codes. There are a total of 12 bits in this word. The numbers of the bits in binary are:

0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100.

Four of the binary numbers have only one 1. They are 0001, 0010, 0100, 1000. They are the numbers that are set as the Hamming code. Table 4.1 is the Hamming code data converted into binary.

Table 4.1: Hamming code table in binary

0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100
0	1	2	3	4	5	6	7	8	9	10	11
X0	X1	D2	X3	D4	D5	D6	X7	D8	D9	D10	D11

Step 2. After the Hamming code is chosen, that equation can set the number of the Hamming code bits. For example, for the Hamming code of 0001, the next step is to exclusive-OR all the data bits containing 1 in the first bit of the binary number. They are 0011, 0101, 0111, 1011, and 1001.

For the other Hamming code use the other equations. Since the algorithm is just XOR, it is not complicated to realize it in the circuit. After using the four-equations, all of the four Hamming code bits should be set in the next equation.

$$X_0 = D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \tag{4.3}$$

$$X_1 = D_2 \oplus D_5 \oplus D_6 \oplus D_9 \oplus D_{10} \tag{4.4}$$

$$X_3 = D_4 \oplus D_5 \oplus D_6 \oplus D_{11} \tag{4.5}$$

$$X_7 = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \tag{4.6}$$

$$r_1 = X_0 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \tag{4.7}$$

$$r_2 = X_1 \oplus D_2 \oplus D_5 \oplus D_6 \oplus D_9 \oplus D_{10} \tag{4.8}$$

$$r_3 = X_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{11} \tag{4.9}$$

$$r_4 = X_7 \oplus D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \tag{4.10}$$

Step 3. After all the Hamming code bits are not, they need to be combined. Since the Hamming codes are coming from XOR gate, the result for these equations should all be 0.

- $r_1 = 0$
- $r_2 = 0$
- $r_3 = 0$
- $r_4 = 0$

Step 4. In the error-detecting process, the R should be XOR all together if the result is 0, which means there is no error.

If one bit is incorrect, the result of the XOR of the R should be 1.

Step 5. If there are some errors and they have been detected, the Hamming code can also help to find which bit is in error and fix it. If the data kept in the memory is 11111111, the form 1 should be like Table 4.2. Table 4.2 is the Hamming code array with data. It is 12 bits in total.

Table 4.2: Hamming code array with data

0	1	2	3	4	5	6	7	8	9	10	11
X0	X1	1	X3	1	1	1	X7	1	1	1	1

When the data is inserted into the second group of the equations, it should be like equations 4.11 and 4.14:

$$1 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.11}$$

$$1 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.12}$$

$$0 = 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.13}$$

$$0 = 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.14}$$

After using this equation, the Hamming codes are 1100

- X0 = 1
- X1 = 1
- X3 = 0
- X7 = 0

Table 4.3: Combining the 4-bit Hamming code and 8-bit data

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	1	1	1	0	1	1	1	1

After the Hamming code is inserted into the 12 bits data, the whole set of data in this form is shown in Table 4.3

Then according to the third equation, after all the data is inserted in this word. r1, r2, r3, and r4 should all equal 0.

$$r_1 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.15}$$

$$r_2 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.16}$$

$$r_3 = 0 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.17}$$

$$r_4 = 0 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \tag{4.18}$$

The results of the equations will be:

$$r_1 \oplus r_2 \oplus r_3 \oplus r_4 = 0 \tag{4.19}$$

If the last equation is still 0, then no errors have occurred.

For example, if one of the bit cells is hit by particles and has a soft error, such as if D2 changes from 1 to 0, the 12 bits word will be shown in Table 4.5

Table 4.4: 4-bit Hamming code and 8-bits data with an error

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	0	1	1	1	0	1	1	1	1

After all the bit data is inserted into the third equation, and calculated the results are:

$$1 \oplus 0 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 0 \tag{4.20}$$

$$1 \oplus 0 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 0 \tag{4.21}$$

$$1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 0 \tag{4.22}$$

$$1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 0 \tag{4.23}$$

When the value is returned to r, the results are:

- $r_1 = 0$
- $r_2 = 0$
- $r_3 = 1$
- $r_4 = 1$

Combining all the values of r, the number of the results will be the number of the error bit. The result is in this equation

$$r_1 r_2 r_3 r_4 = 0011 \tag{4.24}$$

The binary number is 0011. After converting it to decimal, the number is 3. The third bit, which is D2, has been changed. The next step is using an XOR gate to fix this error. The data will be recovered. This is the whole process of the Hamming code error-detecting and correcting.

This is the first part of the Hamming code logic. The function of this circuit logic is to encode the 8-bit data. The 8 bits data should have four redundant bits of Hamming code data to set. The algorithm for this logic function was shown in the last section. Figure 4.13 is the schematic for this part. The input data needs to be XOR in the order of the equations from the last section. The output of this part is the four data for the redundant Hamming codes. There are four groups of eight different XOR gates in this circuit logic. It has 8-bit input and 8-bit output.

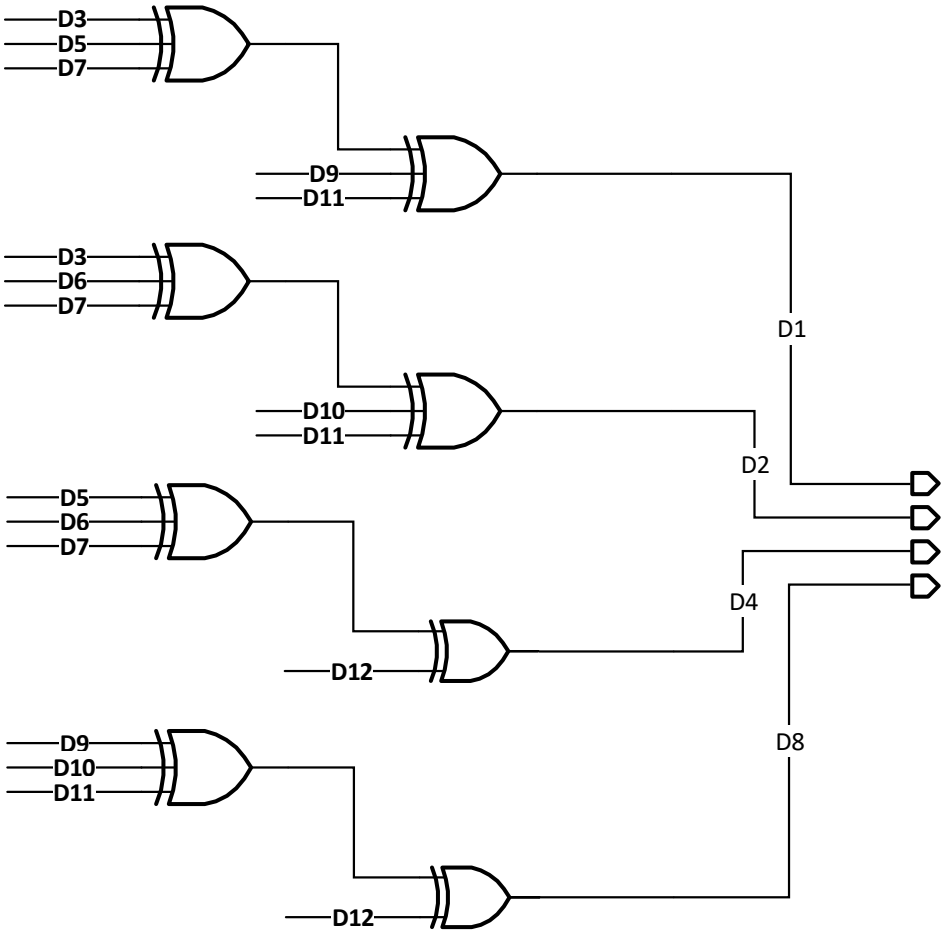

Figure 4.13: Schematic for Hamming code encoding

This is the second Hamming code logic part. The main function of this part is to decode the data. Figure 4.14 is the schematic for the logic. XOR the data to get four Hamming code mark bits. There are four groups of 10 different XOR gates.

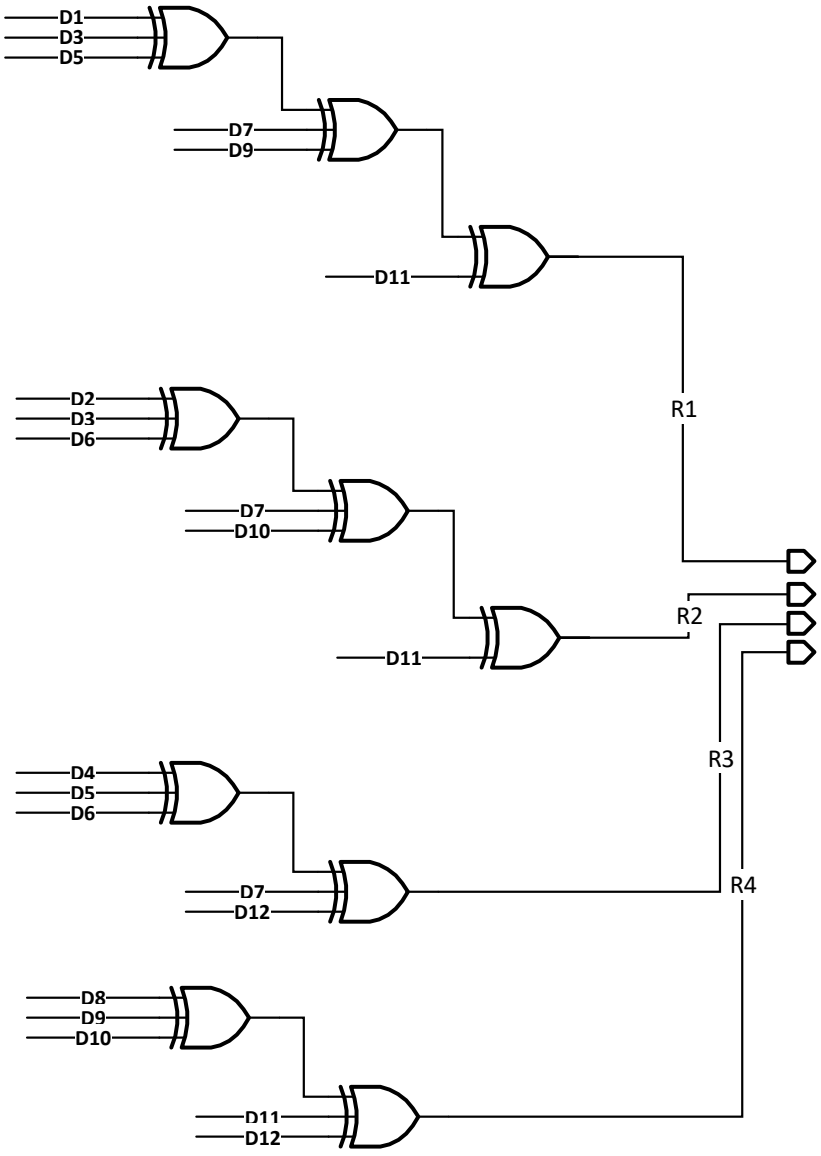

Figure 4.14: Hamming code encoding for array R

Table 4.5: Truth table of an XOR gate

INPUT		OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

This 4-bit output is different from the 4-bit output from the first logic circuit. This 4-bit data is not the Hamming code data, and it will not be stored in any 6T cell. The input for this part is also different from the last part. It has 12-bit input and 4-bit output.

The third part is the last part of the Hamming code of the Hamming code circuit logic. The function of this circuit is to detect the error and correct the error. After the second logic circuit decodes the four bits data. A 4 to 16 decoder will decode the code and restore it into the 12 bits data. The decoder has 16 bits output, but only the first 12 bits are needed. During the error-correcting 12 bits come form the decoder with the data stored in the SRAM. The bits which are correct from the decoder should be 0. Only the wrong data bit from the decoder should be 1. Whether the previous data is 0 or 1, the XOR gate can detect the difference and correct it, because if one of the inputs of XOR gate is 1, the other bit of input will change. The wrong data will be corrected. Table 4.5 shows the truth table for an XOR gate.

4.7 DICE Sense Amplifier

Inspired by the radiation-hardened design of SRAM cells, such as DICE and Quatro, researchers began to use a radiation-tolerant design to modify the SA. The latch sense amplifier has a similar cross-coupled inverter. cross-coupled inverters can store data. In this structure, it contains two nMOS transistors and two pMOS transistors which have eight reverse-biased PN junctions when the enable signal is high. The reverse-biased PN junctions of nMOS are very sensitive to an SEE. If it is hit by high energy particles when it is amplifying the signals from BL and BLB, there may be some errors. If the cross-coupled inverters are modified in an SA, the radiation-tolerant behavior can be increased.

DICE is a redundant radiation-tolerant design. The advantage is that when the sensitive node is hit by a single particle, the storage data in the circuit cannot be overwritten. When the sensitive node is hit and changed, the other two nodes connected with this node will be pulled to floating since the pulse opens the two connected transistors. After the particle energy is released, the two floating and the hit node will recover to their previous status. In the figure of the DICE SA, the transistors, M5, and M11 are connected to the BL signal, The M6, and M12 are connected to the BLB signal. Transistors M13, and M14 are controlled by the sense-enable signal. When the signal is at a high level, the SA will be turned on and start amplifying the signal from BL and BLB. DB is the output of the SA, DBN is the output data reverse. In some designs, the circuit can only use one signal output, DBN and connect an inverter to get the right result.

The price paid for this is to add two more redundant inverters which contain two nMOS transistors and two pMOS transistors. It adds more area cost. However, in a real SRAM design, the number of sense amplifiers is far less than the 6T SRAM cell. The price for adding redundant transistors to an SA is not significant. As in this design, each column has one sense amplifier. The BL and BLB connect all the cells in one column, in the end part of a column, an SA is connected. During the reading operation, the enable signal is at a high level, which is the sensitive period for an SA. The result section containing the SEE simulation result. When the signal of SE is 1, the MOS transistors in the cross-coupled structure become sensitive. In the result, there will be comparing of how the DICE design

did in the SA radiation sophisticated design.

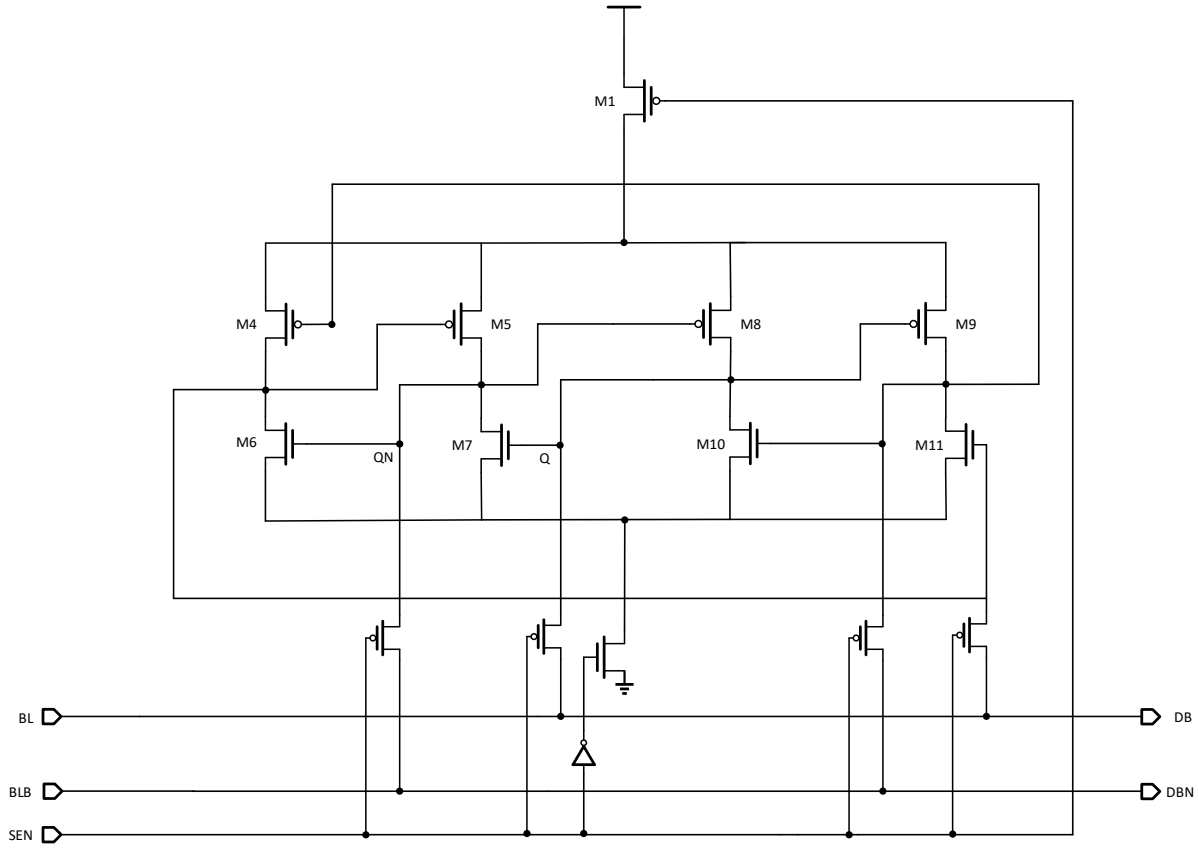

Figure 4.15: DICE sense amplifier schematic

The DICE structure needs dual input to write in the data which means there are two BLs and two BLBs in the circuit. In Figure 4.15 for example, the two inputs of BL are connected together, when the particle hits node Q. The transistors M7 and M9 will be floating, which prevents the data change. But Q is connected to the node between the transistors M4 and M6. Once the energy particle is powerful enough to drive the two nodes and change the transistors connected to the two nodes, the data will be changed, and cannot be recovered by itself, just like in the writing operation. This is the original DICE structure. To solve this problem, separating the two nodes connected in the same input line, such as BL is the main idea. In this project, there will be two separated BL (BL1, BL2) and two separated BLB (BLB1, BLB2). The two BL signals are the same and the two BLB signals are the same. The modified DICE SA is shown in Figure 4.16. Due to the separation, if the node Q is in the

reverse state and has been attacked by an energetic particle, the charge will generate a pulse in node Q and be fixed by the two connected transistors. The charge will not be diffused through the BL wire. Therefore, the DICE structure can work during the SA operation. This modification does not add any extra area or delay.

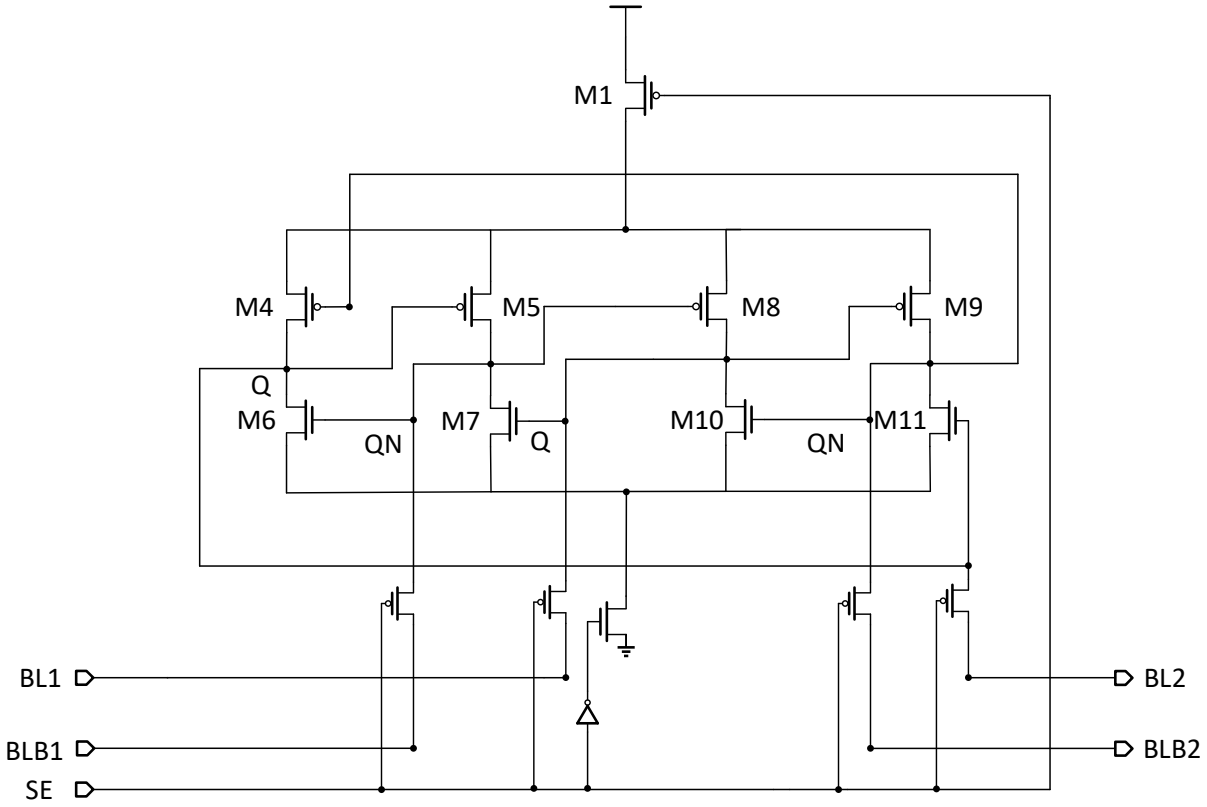

Figure 4.16: Modified DICE sense amplifier schematic

5. Simulation Results

The simulation results consist of four different parts. The first is the 6T SRAM cell simulation. The 6T SRAM cell is the primary cell in the SRAM design. It is vital to make sure the primary cell works correctly evaluate how the radiation-tolerant behavior.

The second part is the Hamming code circuit combined with the SRAM reading and writing circuit simulation. Hamming code is key this radiation-tolerant method in this project. To get the Hamming code circuit features and how it works is also necessary.

The third part is the sense amplifier hardened by DICE simulation results. In this part, there will be a comparison between a standard dynamic sense amplifier and a hardened by design dynamic sense amplifier. The first part of this comparison is in the schematic testing. After the amplifier is shown to work correctly, the radiation-tolerant test can be done. The radiation-tolerant test includes using a pulse to simulate the energetic particle hit, and the cross-section calculation. Cross-section is also called sensitive area.

The last part is the whole SRAM function testing. The test result will show the SRAM reading and writing.

5.1 6T Cell Simulation Results

The 6T SRAM cell is the basic structure of SRAM. The behavior of radiation-tolerant is related to the 6T cell radiation-tolerant behavior. Therefore, it is necessary to do a 6T cell simulation. The WL signal controls the 6T cell. When the WL signal is high, the cell will start working. It is also a sensitive time for the cell.

In Figure 5.1 TFIT analyzes the state for each node. This 6T SRAM cell layout is based on 28nm FDSOI. The input signals and node states can all be set before the simulation. To make the result easy to understand, just setting one of the most sensitive status. When the PN junction is in the reverse state, the junction is very sensitive. For example, when the gate voltage of pMOS is high, the MOS is shut down, and the drain generates the reverse-biased

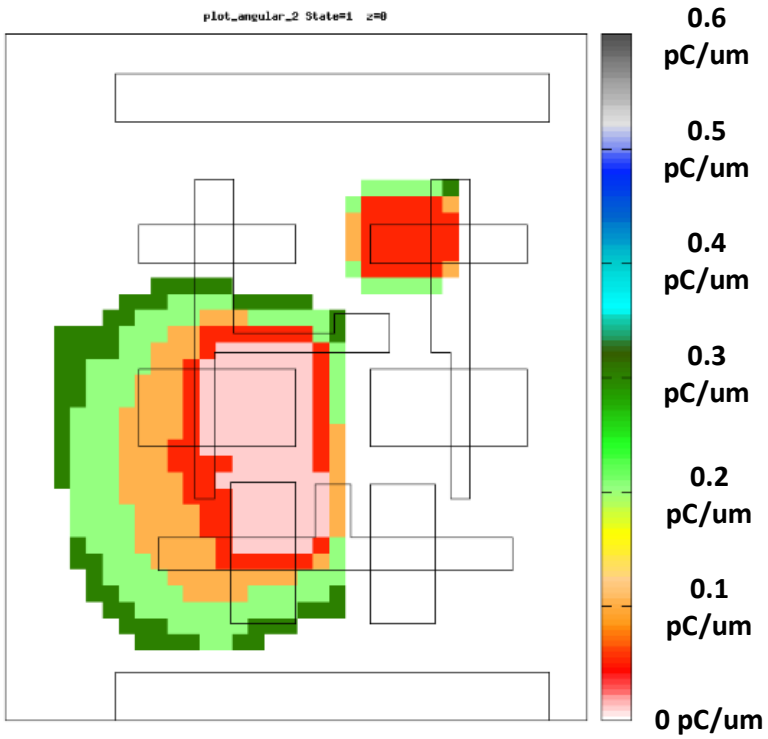

Figure 5.1: 6T SRAM cell TFIT result

PN junction to the substrate which is sensitive to an SEU. In this simulation, the input signals are WL = 0, BL = 1, and BLB = 1. The state nodes are Q = 1, and QN = 0. There will be two sensitive transistors in cross-coupled inverters, the two nMOS connected to WL which are also sensitive. The result and cross-section layout coincide with the theory.

This Figure 5.2 shows the TFIT result. It contains the LET (pC/um), tilt angle, rot angle, and the cross section (cm^2). The LET is 0.3 pC/um and the cross section is 1.02E-08cm^2. In the layout, the TFIT marked all the sensitive area. For each different cross-section, the area is marked in different color. In this figure, the pink and red area means more sensitive compared to the green area. Because the green area needs high energy particle to make it sensitive.

```
================================================================================
============================  TFIT Results ============================
================================================================================


- State 1:
===========
.QN = 0,    .BLB = 1,    .WL = 0,    .BL = 1,    .Q = 1,


Effects are observed on node .Q
Results obtained for "SEU" events
+-----------------------------------------------------------+
| LET(pC/um) | Tilt Angle | Rot. Angle | Cross-section(cm2) |
+-----------------------------------------------------------+
| 0.003      | 0.0        | 0.0        | 0.00e+00           |
| 0.010      | 0.0        | 0.0        | 2.08e-09           |
| 0.050      | 0.0        | 0.0        | 3.88e-09           |
| 0.100      | 0.0        | 0.0        | 5.88e-09           |
| 0.200      | 0.0        | 0.0        | 8.70e-09           |
| 0.300      | 0.0        | 0.0        | 1.02e-08           |
+-----------------------------------------------------------+
```

Figure 5.2: 6T SRAM cell TFIT report

5.2 Hamming Code Decoding Results

The Hamming code is the main component of the radiation-tolerant design. In this simulation, the input signal line will be connected to the input source rather than the SRAM cell. This modification makes the testbench easier to debug once an incorrect result is found, as in the example mentioned before. The input data are all 1: 11111111. The Hamming code of this data group is 1100. The combination of the 12-bit data will be 111011101111. If there is an error and the third bit status has changed to 0 (the error can be any bit of the data, so to make the test result easy to understand, an error in the third bitis used), the data with an error will be 110011101111. In the testbench circuit, the 12-bit input of the Hamming code decoding and error-detecting are the same. The output of the Hamming encoding is the mark bit of the error. The output is 0011 which is sent to the 4 to 16 decoder, and the output will be the mark of the error bit. The Hamming code error-detecting component

combines the data of the output and data come from the decoder, using an XOR gate can change the bit from the output when the decoder output is 1. The output of the Hamming code error detecting component is the correct data with the Hamming code.

Figure 5.3 is the signals of the Hamming code encoding output. There are some 1 ns pulses from the source used as the signal 1. The signals r3, r2, r1, and r0 are the output of this part. r3 and r2 are 0. r1 and r0 are 1. The delay of the signal is about 0.064ns. This delay does not significantly affect circuit function

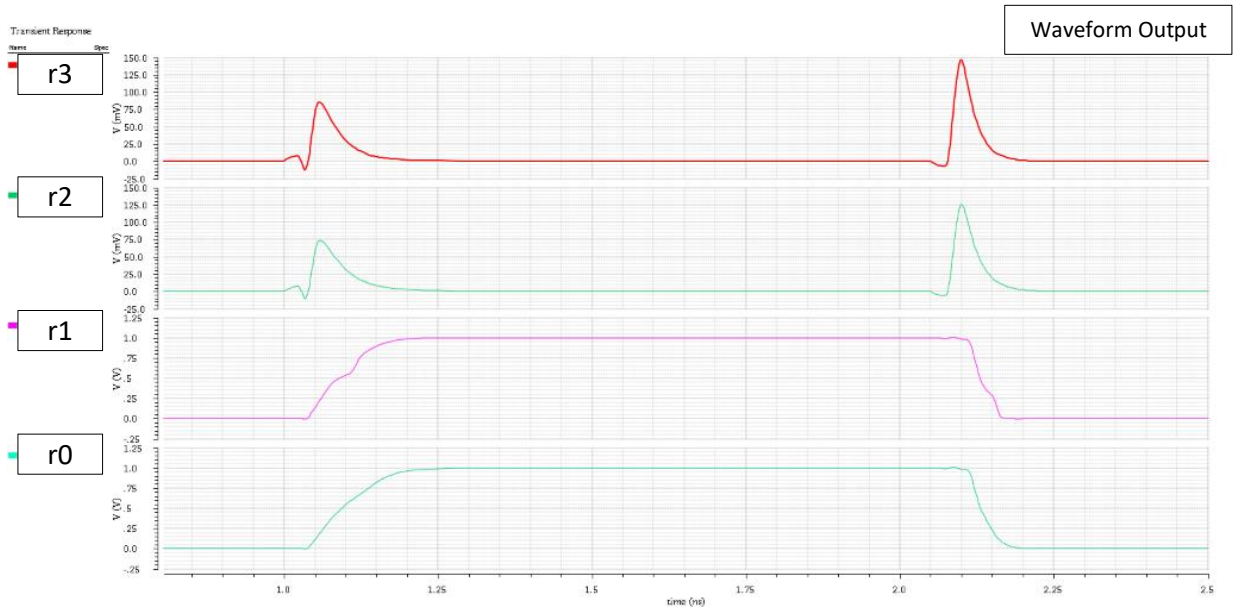

Figure 5.3: Hamming code four-bit data

Figure 5.4 shows the signals of the Hamming code error-detecting and correcting. It has 24 inputs, 12 from the cell containing error. 12 from the decoder containing the error bit information. The schematic does not cover the 12 signals from the decoder, but the signals from the decoder are 001000000000. The other 12 signals in the figure are the output of the entire Hamming code. The fixed data has no error. The fixed signal in this figure is the error bit but it is fixed by Hamming code. This signal has a 0.114 ns delay. The other correct signals are all the same. To make the timing figure clear and to show the detail, those signals outputting one and zero have been combined into two signals. The first normal signal is when the output=1. The third signal whose name is also called the normal signal is when the output = 0.

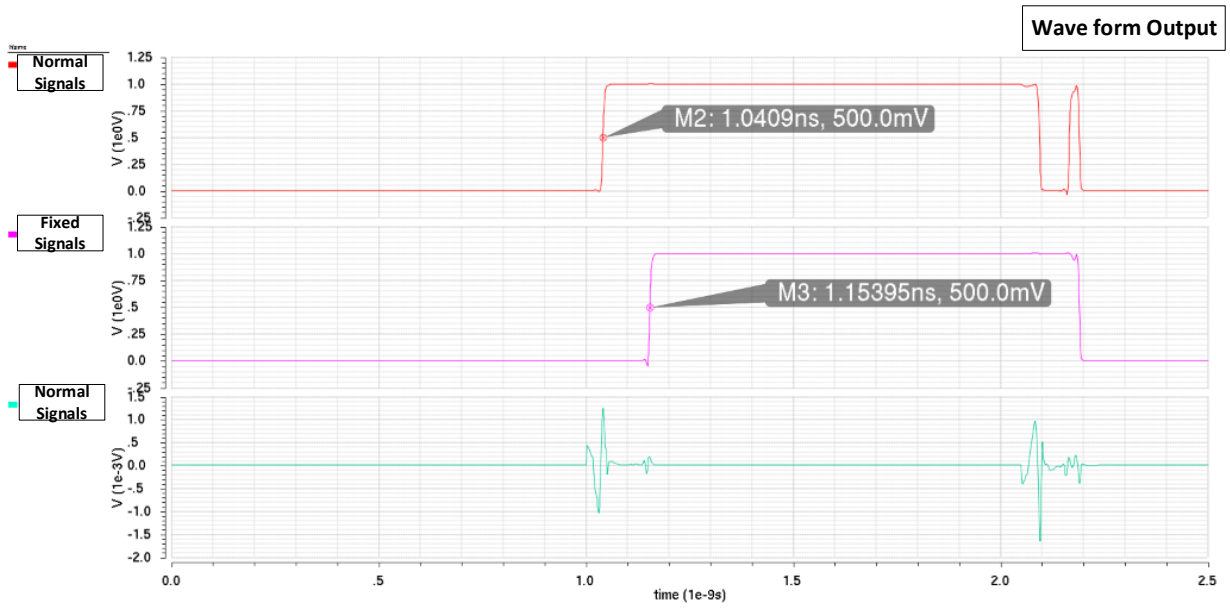

Figure 5.4: Hamming code output waveform

This simulation shows that the function of the Hamming code circuit is working correctly. There are some delays when the error data is fixed. However, the delay is around 0.1 ns which will not significantly affect the circuit. The total delay of the Hamming code encoding, and error-correcting is around 2ns. The circuit performs well in terms of delay. Compared with traditional redundancy-based hardened design, this Hamming code adds 50% to the extra cell area which is much smaller than, for example, TMR which has 200% more extra area.

5.3 Sense Amplifier Radiation Simulation Results

5.3.1 Schematic Function Simulation Results

This section presents the sense amplifier radiation simulation results. Both of the SA layouts are designed in 65nm process, which contains two different sense amplifiers result simulations. In the first part of the test results, there are the DICE sense amplifier timing results which prove that the new by designed SA works correctly. Before the radiation simulation, the function of the newly designed circuit should be proven. In this design, SEN controls the whole circuit. When the high-level signal arrives, the two pMOSs in the BL and BLB lines will shut down the BL and BLB signal, and the SA starts amplifying. Before the BL and

BLB go to the same level, the SEN signal is turned on. The BL and BLB will open again and get the result output. Figure 5.5 shows the designed timing for the schematic testing.

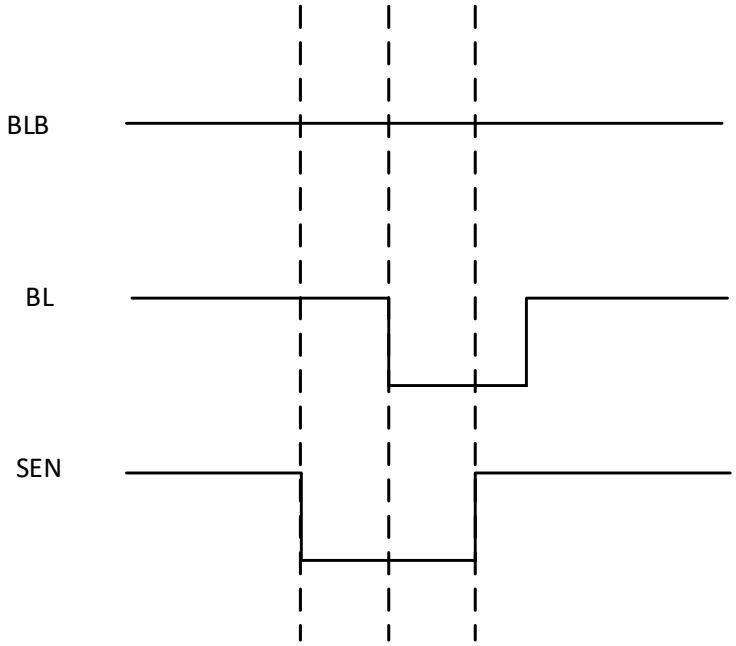

Figure 5.5: Sense amplifier timing design

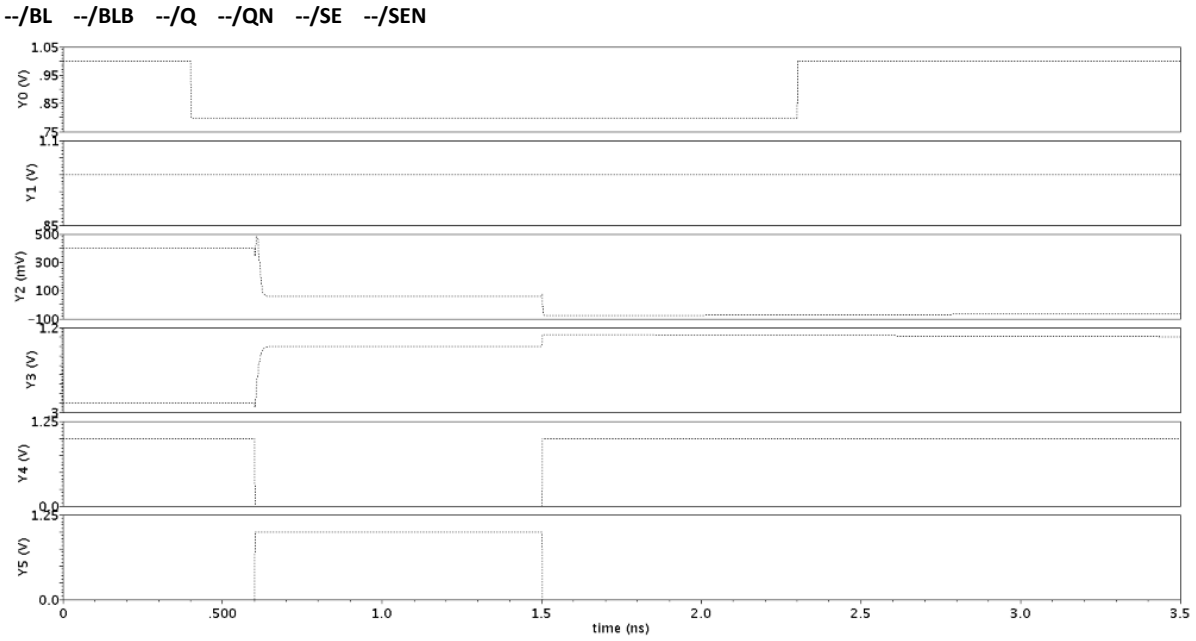

Figure 5.6: Sense amplifier timing when output = 0

The corresponding circuit design is a conventional sense amplifier. This SA does not contain any radiation-hardened design. For comparison, the result of this SA has been provided. Figure 5.6 shows the timing for this SA. The timing design is similar to the DICE SA. The result in Figure 5.6 is 0V.

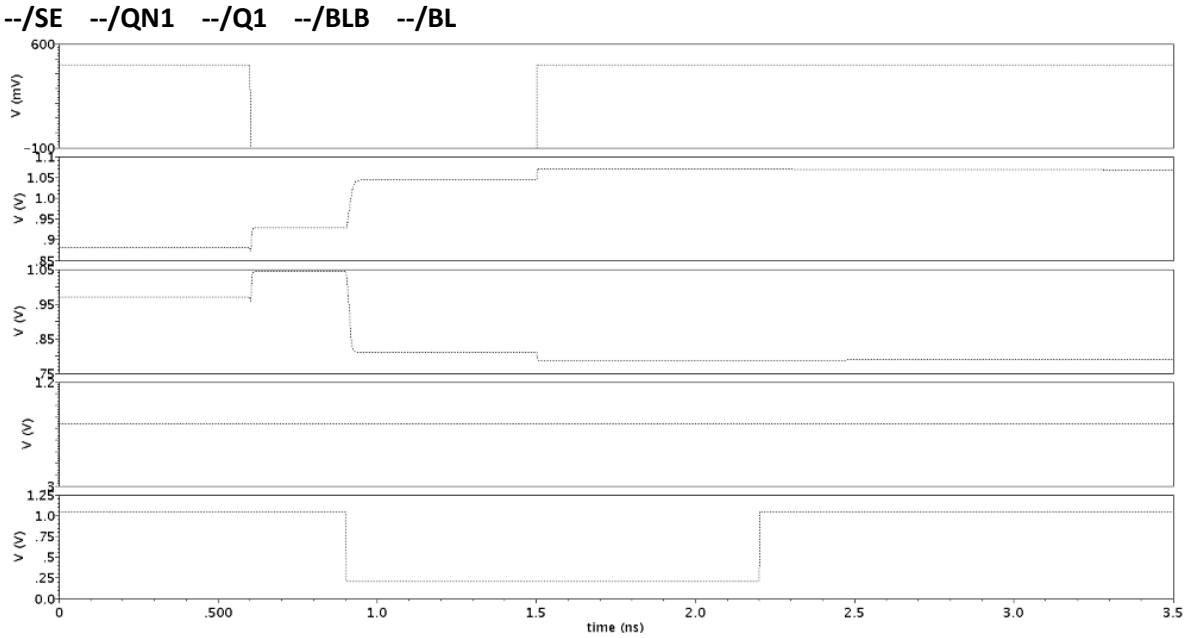

Figure 5.7: DICE sense amplifier timing when output = 0

Figure 5.7 shows the DICE SA test result. Q and QN are the two nodes in the cross-coupled inverter. Q can be regarded as the output, and QN is the opposite output value in the other inverter. The SE signal starts a change in the 0.6 ns, and the BL starts changing from 0.9 ns. From 0.9 ns to 2.2 ns, the BL and BLB maintained the difference which is the BL at 0.8V, and the BLB at 1.0V. The BL is set at 0.8V rather than 0V in order to make the experiment closer to the actual situation. SE is turned off again in 1.5 ns. Then, the result of the SA can be detected in the output node, and the DICE SA finishes the amplifying process. In the timing result, the output is 0.02V, and the output bar is 1.239V, which means the result is 0V.

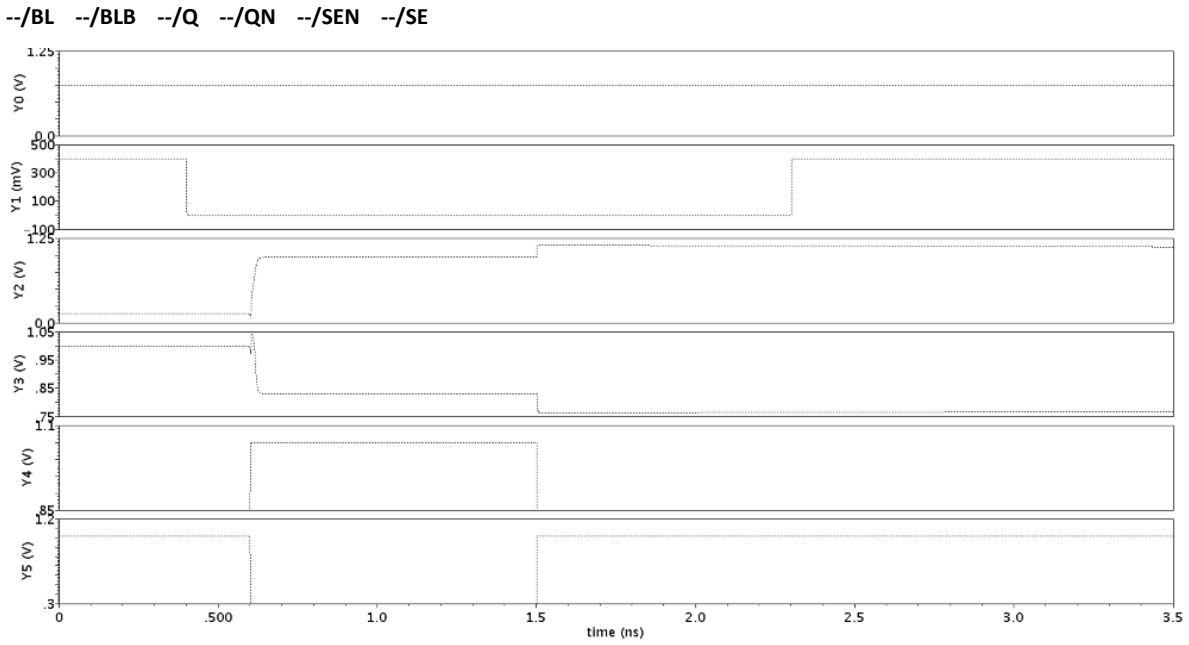

Figure 5.8: Sense amplifier timing when output = 1

The conclusion drawn from this set of comparative experiments is that both of the SAs work correctly. The amplify range is from 0.2V to 1V. Due to the back-to-back structure, the delay of the SA is also very small. The results of the experiment matched with the design expectation. These two timing results amplify the 0V. To present the completed results, the next two figures show the result of amplifying 1, which means that BL is 0.8V and BLB is 1.0V.

Figure 5.8 shows the result of SA output = 1.

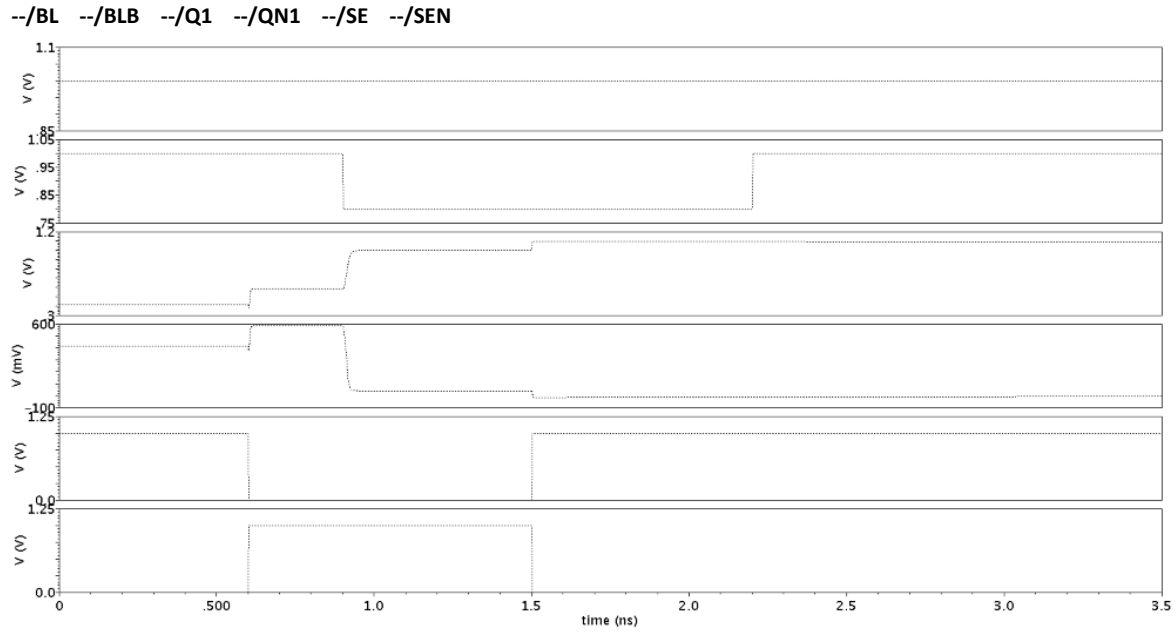

Figure 5.9: DICE sense amplifier timing when output = 1

Figure 5.9 shows the result of DICE SA output = 1.

According to the above results, the function for the newly designed DICE SA has been proven. Also, for the area efficiency, the DICE structure only adds four more transistors as redundancy, and it is much smaller than the previous hardened SA (triple area redundancy) [22].

5.3.2 Schematic Single Event Upset Simulation Results

Following the verification of the basic function of the two different sense amplifiers, this section is the Cadence SEU tolerant design test. Figure 5.10 shows the testbench for the DICE SA SEU simulation test. Adding a capacitance with a switch is the key feature. By indirectly switching capacitance at QN and ground, the initial voltage of capacitance is opposite to that at point QN. When the switch is turned off, the voltage difference between the two will generate instantaneous current to simulate the single-particle effect. The capacitance C was used to compare the irradiation resistance of each SA.

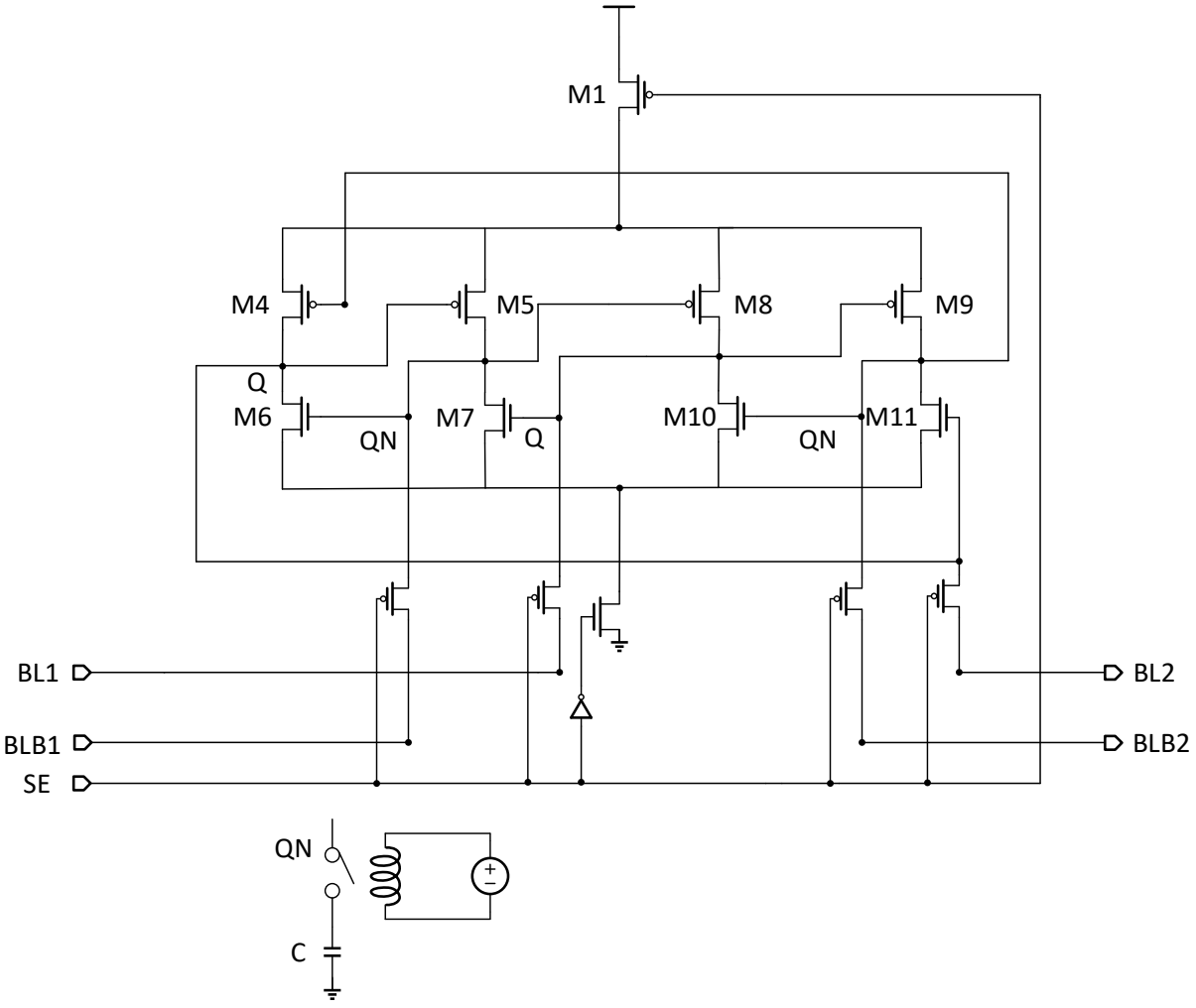

Figure 5.10: DICE sense amplifier testbench

The testbench for SA is similar to the DICE SA's. The connected node of the SA is QN which is connected to BLB in the circuit. The initial state is 1. Figure 5.11 shows the result in the SA, the critical value of the normal SA is between 17 fF and 18.2 fF. The signal changed and could not recover to its previous status when the capacitance was larger than 17.3 fF. The radiation-tolerant performance of the DICE SA is more than ten times better than the normal SA.

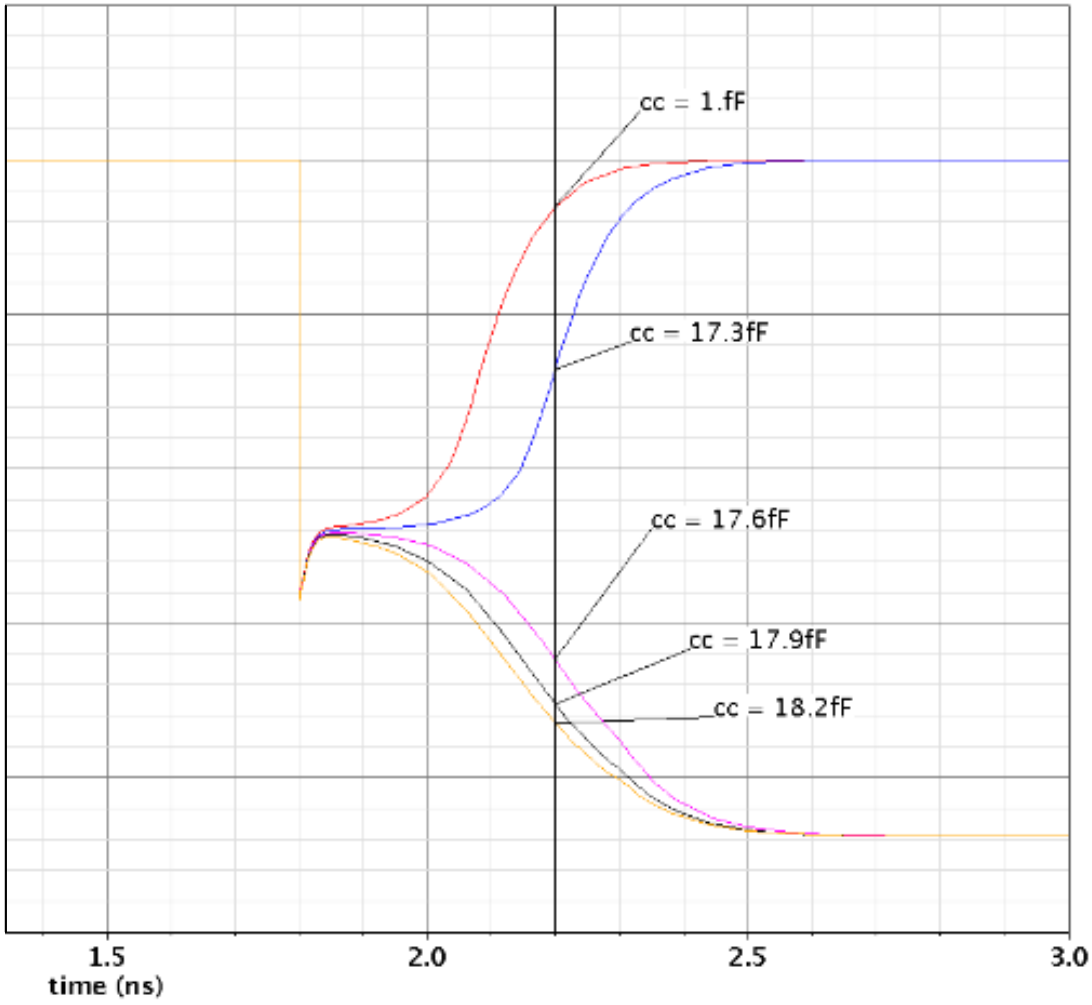

Figure 5.11: SA schematic pulse test

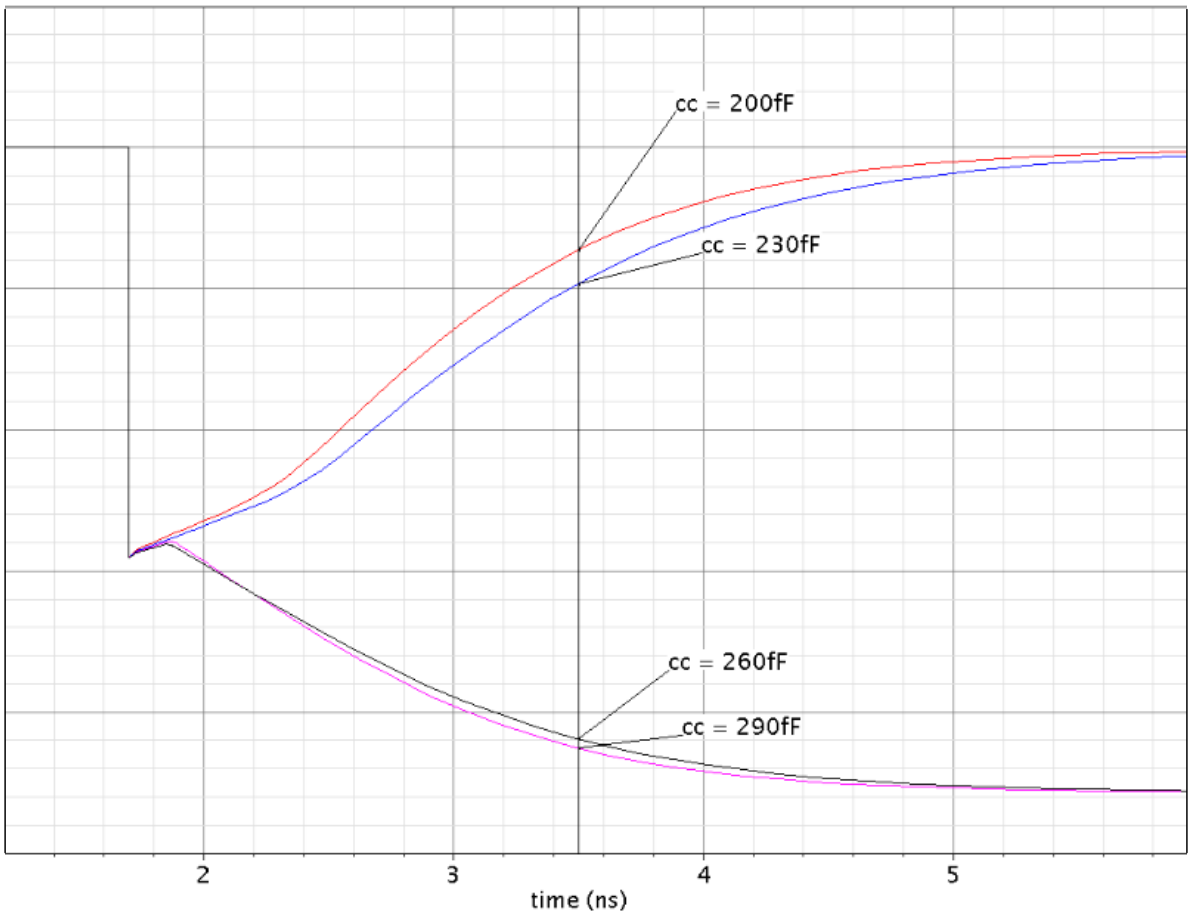

Figure 5.12: DICE SA schematic pulse test

Figure 5.12 shows the result of the SEU simulation for the DICE SA. The initial state of QN is 1, and the initial capacitance is not charged. In the 1.7 ns, the switch of capacitance opens, and the capacitance connects to the circuit and generates a pulse. In the DICE SA test, the critical value of the circuit is between 1 fF and 290 fF. The signal stored in the SA did not reverse until the capacitance was larger than 230fF.

The simulation results show that the enhanced sensitive amplifier has better performance. According to the capacitance of the two groups of experiments, the capacitance in the DICE SA group is much larger than the normal SA group. The performance of the newly designed circuit has been improved more than ten times. But this set of experiments can only give a rough idea of how circuits behave in SEU tolerance. To get a more accurate cross-section result, the TFIT result should be involved.

5.3.3 Layout TFIT Simulation Results

This section contains the last part of the two SA test results. The simulation tool is TFIT, and the particles used for the test are heavy ions. The energy for each sense amplifier is the same so that it can make a clear comparison.

These two layouts cross-sections are the TFIT results. Figure 5.13 is the basic latch sense amplifier. Figure 5.14 is the DICE hardened sense amplifier. The LET is from 0.1 to 60 MeVcm^2/mg (0.1, 1, 20, 30, 40, 50, 60). The status is the same for the two circuits test. SE = 0, SEN = 1, Q = 0, QN = 1, BLB1 = 1, BL1 = 0, BLB2 = 1, BL2 = 0. SE is the switch signal. When SE = 0, the circuit connection between BL and Q has been cut off. One of the nodes in Q and QN should be sensitive. This is an ideal testing status for radiation-hardened performance. The observed node is QN which is the signal output node.

Figure 5.13 is the normal SA sensitive area. The two pMOSs in the cross-coupled inverters are very sensitive. The input signals and node states are SE = 0, SEN = 1, Q = 0, QN = 1, BLB = 1 and BL = 0. When SE is 0, the transistor connected to the inverters has been shut down. This transistor is also sensitive. The diagonal transistors in the cross-coupled inverter which contain the reverse-biased PN junction are also sensitive. The range of the LET is from 0 to 60 MeVcm^2/mg in this figure. The area marked by blue and yellow which means a higher LET, is less sensitive. Because those area means only with high LET, it would be sensitive to SEE. In the three drains of the transistors which is marked as yellow is the most sensitive area.

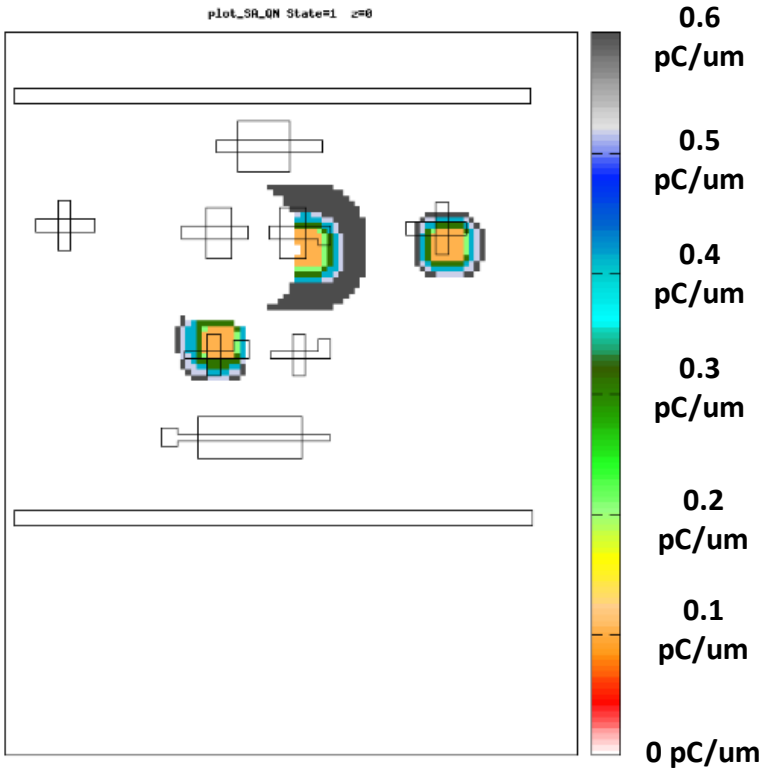

Figure 5.13: SA layout cross-section

However, in the TFIT result, there are no sensitive transistors detected in the new DICE SA. The DICE structure is immune to the single-particle attack. The technology for the SA design is 65nm, and the multiple node errors are not very significant. For these reasons, there are no sensitive transistors detected.

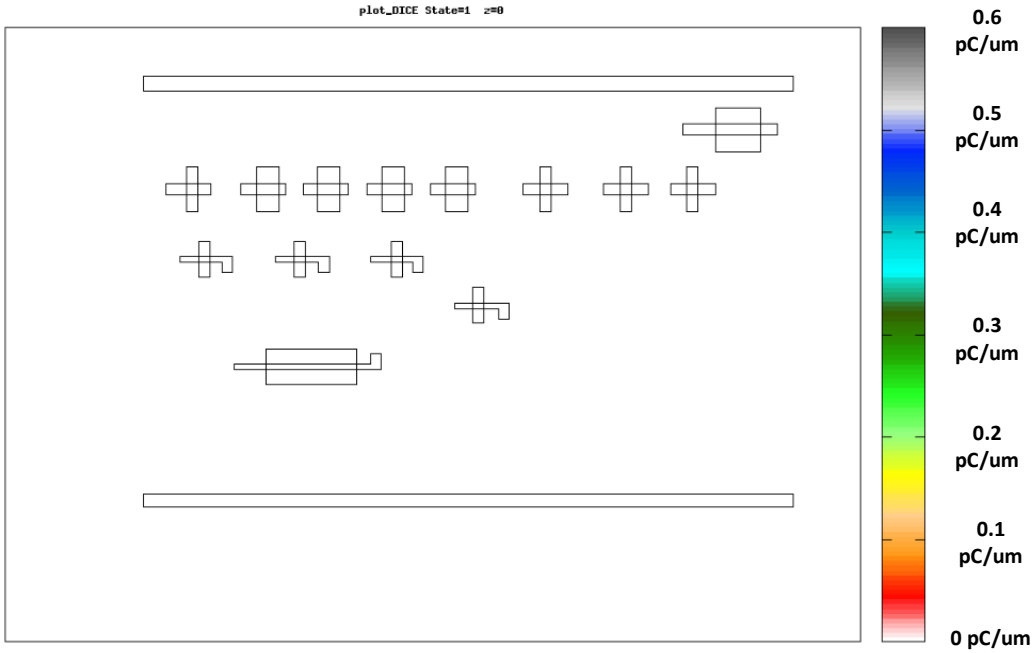

Figure 5.14: DICE SA layout cross-section

Table 5.1 contains the result summary of the cross-section to the two sense amplifiers. The normal sense amplifier still has a sensitive area when the LET varies from 10 MeVcm^2/mg to 60 MeVcm^2/mg. When the LET is 60 MeVcm^2/mg, which is the highest LET in the set of the simulation, the SA has the largest cross-section. To summarize the contents of this table, the following points can be found. The cross-section of the normal sense amplifier increases with the LET. For the hardened SA, no matter what happens to the LET, the cross-section does not change. In conclusion, according to the simulation of layouts, it is found that the newly designed hardened SA shows good performance.

Table 5.1: SA cross section results

LET(MeV)	0.1	1	10	20	30	40	50	60
Cross section(cm2) SA	0	0	2.53E-09	3.10E-09	4.70E-09	6.68E-09	8.18E-09	1.40E-08
Cross section(cm2) DICE	0	0	0	0	0	0	0	0

5.4 Simulation of SRAM with Hamming Code

This section will verify that the SRAM works properly. Since the size of the SRAM is very large and most of the cell arrays are the same, it is not necessary to verify every address for both the read and write operation. In this simulation, a data array, 11111111 with its Hamming code 1100, will be simulated. The whole data array is 111011101111. Figure 5.15 the result of the simulation. It contains writing and reading of the signal HWDATA 3 which is the third cell of the array. From 0.4 ns to 2 ns, the WL is turned on, and the writing operation starts. The data 1 has been written into the cell. Before 4 ns, the signal on BL2 and BLB2 has been precharged into VDD at the same time. The VDD is 1V. At 4 ns, the WL turns one again, BL and BLB start to show the difference, and the SA enable is turned on. The signals on the BL and BLB have been sent into the read driver. At 5.5 ns, the data come from the read driver has been sent into the Hamming code error detecting and correcting circuit. Around 6 ns, the output of the Hamming code error detecting send the data out. The data that has been written and read is 1.

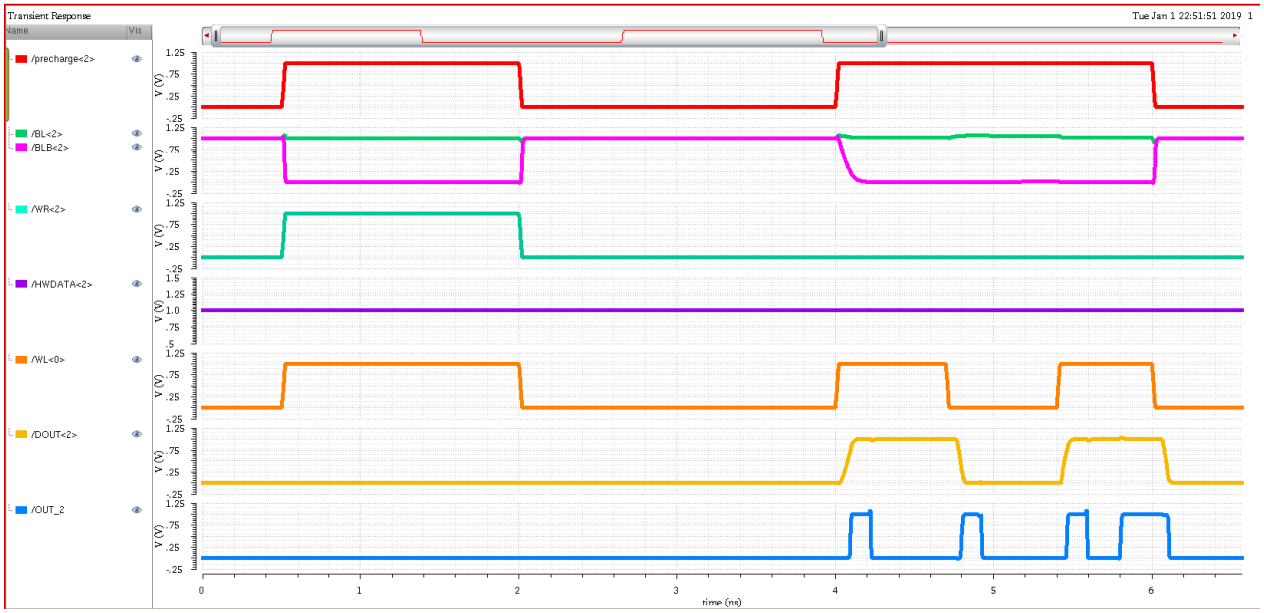

Figure 5.15: SRAM simulation result with one signal

The second simulation for the SRAM simulation combines three different signals writing and reading. Figure 5.16 shows the timing for this simulation. The three bits of data are cell

0, cell 2, and cell 3. Cell 0 is the first Hamming code bit. The data in the cell is 1. Cell 2 is the first SRAM bit. The data in cell 2 is 1. Cell 3 is the third cell of the Hamming code. The data in the cell is 0. The difference between cell 0 and cell 2 is that the input signals are different. The Hamming code input is generated in the SRAM. Cell 3 has the different data compared with the other two cells. These three data are the most representative. In the final output around 6 ns, the data outputs are correct.

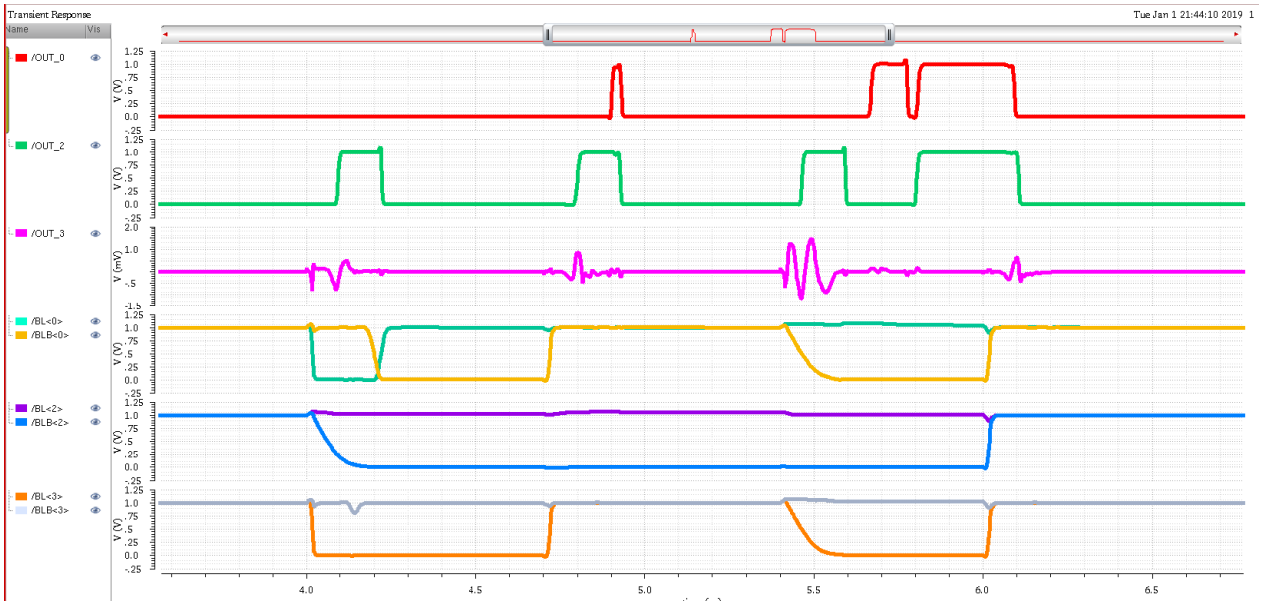

Figure 5.16: Three signals of the SRAM write and read simulation

6. Conclusion and Future Work

6.1 Conclusion of the Thesis

With the scaling of silicon technologies, modern ICs contain more transistors with lower power supply voltage and higher speed. These features have made them more vulnerable to SEEs and make it more challenging to maintain reliable operations when working in radiation environments. This thesis aims to develop a radiation-tolerant SRAM for space applications. The main research content and work summary of this paper are concluded as follows:

In Chapter 2, different radiation sources such as alpha particles, heavy ions, neutrons, and protons were introduced, followed by a discussion of the radiation effects and the mechanism of radiation effects.

In Chapter 3, a literature review of the current radiation-tolerant designs was carried out based on the redundancy methods. Commonly used design techniques such as TMR, Guard-gate, DICE, Quatro, and LEAP were introduced. For the ECC techniques, the parity check was introduced first, which is the base of the Hamming code algorithm. Then, the Hamming code was introduced in detail since it is adopted as one of the major techniques in designing the SRAM for this thesis.

In Chapter 4, an SRAM design specification was introduced and followed by the design approaches to mitigate the SEEs for each section. A 6T SRAM cell was developed first since it is the basic component for the SRAM. Hamming code implementation was realized to protect the cell arrays since it can effectively detect and correct single bit errors. Different sense amplifier structures were introduced, and a novel sense amplifier was also developed based on the DICE structure.

In Chapter 5, simulations were carried out for the SRAM designs to validate the functionality and the radiation-tolerant performance. The function of a 6T cell was validated first and followed by the sensitive map analysis with the TFIT CAD tool. It shows that the cross-coupled inverters are the sensitive components in the cell. The functionality of the

cell arrays with Hamming code protection was also validated with schematic simulations. It shows that the Hamming code can effectively protect single-bit errors in cell arrays. The performance of reference and novel sensitive amplifiers was also simulated with the Cadence and TFIT tools. The results indicated that the cross-section of the DICE amplifier was three times smaller than the normal sense amplifier even in the worst case.

The major contributions of the thesis include the design of the overall SRAM structure, the implementing of the Hamming code for the cell arrays and the novel design of the sense amplifier based on the DICE structure. The simulations based on the schematic and layout have demonstrated the effectiveness of the designs.

6.2 Future work

For the DICE sense amplifier, there are already many functional and radiation simulation results. However, there are still rooms to modify the design in order to enhance the functions such as increasing the speed and decreasing the circuit delay. In the future, combining the idea of DICE and LEAP layout techniques will also benefit the radiation-tolerant performance of the developed sense amplifier.

In the future, it is beneficial to fabricate the radiation hardened SRAM design with 28nm FDSOI technology, and test it in the radiation environment to further evaluate the overall performance of the SRAM.

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