LINT MODULATOR

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ABSTRACT

As the radio spectrum in the lower microwave frequency bands is becoming more crowded, it is almost impossible to support new broadband systems, which use larger portions of the radio spectrum. Thus, new and emerging wireless systems available for broadband services turn towards the high microwave and millimeter-wave spectrum range. Linear modulation schemes like Quadrature Amplitude Modulation (QAM) are preferred in broadband wireless communication systems due to their high spectrum efficiency, which makes them utilize the limited channel bandwidth more efficiently. The problem is that the non-constant envelope of linear modulation schemes requires linear amplification. Linear amplification can be obtained with a Class A amplifier solution, which suffers from very low power efficiency. Poor power efficiency is not suitable for highly integrated or portable equipment, because large batteries are needed to supply extra power, and large transistors and heat sinks are required to dissipate this power. Therefore, a linear modulator architecture that can achieve high power efficiency and implementation at upper microwave and millimeter-wave frequencies is very attractive.

The novel LInear modulation with Nonlinear Translation (LINT) modulator architecture proposed in this thesis is based on the direct modulation method and the LInear amplification with Nonlinear Components (LINC) technique. It involves decomposing arbitrary baseband signals into two constant envelope signals. Then each constant envelope signal is modulated at a subharmonic carrier using vector modulation followed by xN frequency multiplication to achieve frequency translation to the desired output frequency. Highly efficient power amplifiers can be employed to prepare the signal for transmission at a required power level. Finally, two amplified signals are passively combined to produce a high frequency and amplified replica of the input signal. Although frequency multiplication and power amplification are nonlinear processes, the overall input to output transfer function of the LINT modulator is linear. As opposed to the more convensional method of modulation at an IF and upconversion to the desired transmit frequency, the direct modulation method removes the requirement for IF, upconversion, and filtering circuitry, resulting in cost and complexity reduction of the hardware implementation.

The main part of the modulator is a x12 two-stage microwave frequency/phase multiplier chain. The multiplier chain consists of x3 and x4 multipliers connected in cascade, and translates a modulated subharmonic carrier at 2.33 GHz to 28 GHz. The circuitry is simulated assuming soft substrate implementation, which simplifies the fabrication process. The multiplier chain itself shows good performance, and can be used to generate stable source signals at high microwave frequencies.

Performance of the LINT modulator is investigated using realistic multiplier chains. The effect of amplitude imbalance and phase noise on the 16-QAM modulated signal is simulated.

The result of this research presents a generic modulator architecture that is very attractive for broadband wireless applications at upper microwave and millimeter-wave frequencies.

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DEDICATION

To my parents, Zhanjing Ma and Fengrong Wang, and my sister, Liguang Ma.

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LIST OF ABBREVIATIONS

ACI	adjacent channel interference
ADS	Advanced Design System
ASK	Amplitude Shift Keying
ATC	American Technical Ceramics
ATM	asynchronous transfer mode
b/s	bits per second
BPF	bandpass filter
bps/Hz	bit per second per Hertz
CW	continuous wave
dB	decibel
dBc	decibels relative to carrier
dBc/Hz	decibels relative to carrier per Hertz
dBm	decibels relative to 1 milliwatt
DC	direct current
DSP	digital signal processing
FET	field effect transistor
FPGA	field programmable gate array
FSK	Frequency Shift Keying
GHz	gigahertz
GMSK	Gaussian Minimum Shift Keying
Hz	hertz
I	in-phase
IEEE	Institute of Electrical and Electronics Engineers, Inc.
IF	intermediate frequency
IMD	intermodulation distortion

ISI	intersymbol interference
KCL	Kirchoff's Current Law
kHz	kilohertz
LINC	LInear amplification with Nonlinear Components
LINT	LInear modulation with Nonlinear Translation
LMDS	local multipoint distribution service
mA	milliamp
Mbits/s	mega bits per second
MIC	microwave integrated circuit
mil.	0.001 inches
MMDS	multichannel multipoint distribution service
MMIC	monolithic microwave integrated circuit
mS	millisiemens
MSK	Minimum Shift Keying
Ω	Ohms
OFDM	orthogonal frequency division multiplexing
pF	picofarads
PSK	Phase Shift Keying
PTFE	polytetrafluorethylene
Q	quadrature
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RC	raised cosine
RF	radio frequency
rms	root mean square
SCS	signal component separator
SRD	step recovery diode
SRRC	square root raised cosine
SSB	Single Sideband
sym/s	symbols per second

μ s	microseconds
V	volt
WLAN	wireless local area network

Chapter 1

INTRODUCTION

1.1 Background

Wireless communication grew enormously in the last decade, and it shows little sign of slowing. It was predicted that wireless would surpass wireline as the dominant method of telecommunications worldwide by 2008 [1]. In additional to expanded voice services, the driver for wireless growth will be the demand for high-speed data and video services, using high speed transport techniques like asynchronous transfer mode (ATM) at rates of 155 and 622 Mbits/s [2]. As high-speed data transportation occupies a large bandwidth, the demand for broadband wireless (communication techniques that use larger, or broader portions of radio frequency spectrum) will increase substantially.

However, the radio spectrum in the lower frequency bands is becoming more and more crowded, which makes it almost impossible to support new broadband systems. Thus new and emerging wireless systems available for broadband services are moving towards high microwave and millimeter-wave frequency bands.

Wireless local area networks (WLANs) are examples of broadband technology, which provides high bandwidth to users in a limited geographical area like factories, warehouses and offices. The IEEE 802.11 standard [3] developed within the Institute of Electrical and Electronics Engineers, Inc. (IEEE) is a popular and successful standard for WLAN. In the 1999 edition of IEEE 802.11 standard, a maximum data rate of 2 Mbits/s in the 2.4 GHz band is supported. In IEEE 802.11b, which is one of the two additional amendments for 802.11, much higher data rates up to 11 Mbits/s are provided at the same frequency band. In the 802.11a amendment, data

rates up to 54 Mbits/s are provided using orthogonal frequency division multiplexing (OFDM) technique in the 5-6 GHz bands.

In order to provide higher bit rates, an ATM-based millimeter-wave WLAN for application in the 60 GHz frequency band was developed [4]. This ATM-based WLAN has a target data rate of 155 Mbits/s due to the greater bandwidth available in millimeter-wave frequency band. It is expected to be commercially available in the near future. Another system that can provide broadband services is called multichannel multipoint distribution service (MMDS). MMDS is a bi-directional, high-speed fixed broadband wireless networking service operating in the 2 to 3 GHz range. It supports data rates up to 37 Mbits/s. Unfortunately, due to the lack of frequencies in lower microwave portion of spectrum, MMDS is viable only in a limited number of countries [5]. Another emerging broadband wireless technology that has much stronger market potential than MMDS is local multipoint distribution service (LMDS). LMDS, like MMDS, is a high-speed bi-directional wireless networking service, but operates at much higher frequencies - typically in the 28, 38 or 40 GHz bands [5] [6]. There is high bandwidth available for LMDS in most, if not all, countries. This allows data delivery at speeds up to 155 Mbits/s - over four times that of MMDS systems.

Although it is becoming increasingly apparent that millimeter-wave spectrum range must be utilized in order to provide wireless communications with high bit rates, the technology of transceiver design in such frequency is not quite mature. Simple, high performance and cost-effective transmitter operating at millimeter-wave frequency bands is very attractive for the future development of wireless broadband communications.

As these emerging systems are commercialized, high performance modulator architectures which result in cost-effective hardware realizations will become increasingly attractive.

1.2 Direct Modulation

Modulation is a signal processing technique in which one signal (the modulating signal) modifies a property of another signal (the carrier signal) so that a composite signal (the modulated signal) is formed. In digital communication systems, the modulating signal is a sequence of discrete messages. This signal is used to modify the amplitude, phase or frequency of a sinusoidal carrier signal. The conventional method of digital modulation is performed at an intermediate frequency (IF), then the signal is upconverted to the desired transmitting frequency using several mixers, oscillators, and bandpass filters (BPF) as shown in Figure 1.1. While this method yields good performance, it is expensive since it results in substantial hardware.

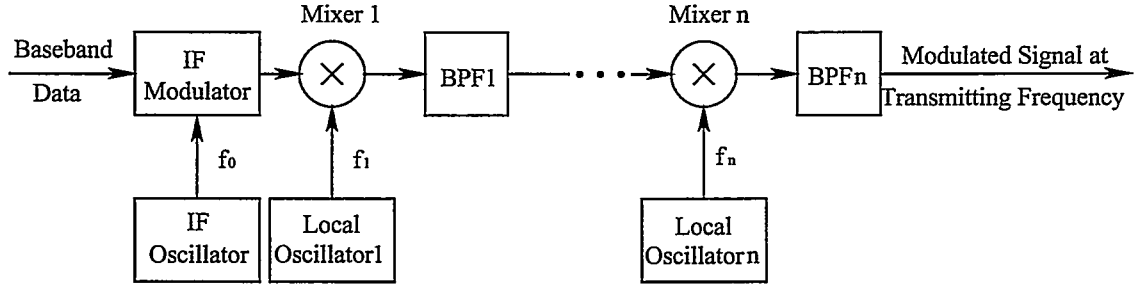


Figure 1.1 Block diagram of conventional method of digital modulation.

As an alternative, direct modulation is an attractive option for reducing the cost and complexity of the transmitter. With this method, the amplitude, phase, or frequency of a sinusoidal carrier is modulated at the transmitting frequency directly by the baseband information sequence. Direct modulation removes the requirement for multiple stages of IF, upconversion and filtering circuitry. If the carrier produced by a single microwave power oscillator is directly modulated at the desired transmitting power level, the requirement for a high power amplifier as the final stage in the transmitter is also removed. The result is a significant reduction in the hardware required in the transmitter.

1.3 Linear Modulation

Most wireless communication systems use digital modulation techniques to transmit data on a carrier signal. There are three characteristics that can be changed with time: amplitude, phase and frequency. The result forms three major categories of modulation techniques currently employed in modern communication systems: Amplitude Shift Keying (ASK), Phase Shift Keying (PSK), and Frequency Shift Keying (FSK). Among them, the amplitude modulation technique, in which the amplitude of the modulation envelope is directly proportional to the amplitude of the data signal at all modulation frequencies, is sometimes called linear modulation. Constant envelope modulation schemes, such as frequency and phase modulations, are examples of nonlinear modulation.

The goal of modulation is not only to effectively transport the message signal through a radio channel, but also to achieve this with desirable qualities, such as high power efficiency and high bandwidth efficiency or spectral efficiency.

The massive growth in wireless has put great strain on scarce spectral resources, resulting in overcrowded communication channels. In this regard, it is very important that each communication uses as little bandwidth as possible. Thus, the modulation technique that enables more information to be carried over a limited channel bandwidth is preferred. Bandwidth efficiency is the term that describes how efficiently the allocated bandwidth is utilized by a modulation scheme. Bandwidth efficiency, η, is defined as the transmitted bit rate divided by the bandwidth of the signal, which can be expressed mathematically as [7]

$$\eta = \frac{R_b}{W}, \tag{1.1}$$

where W is the bandwidth of modulated signal in Hz, and R_b is the bit rate in b/s.

Bandwidth efficiency improves as more information bits are sent with each modulating "symbol". The symbol rate, R_s, is the bit rate divided by the number of bits that can be transmitted with each symbol. Theoretically, the minimum occupied bandwidth of the modulated signal is equal to the symbol rate. Substituting

for bandwidth, W, in Equation 1.1 with the symbol rate, the theoretical maximum bandwidth efficiency is equal to the number of bits transmitted with each symbol.

Nonlinear modulation formats like FSK and Minimum Shift Keying (MSK) have low bandwidth efficiency on the order of 1 bps/Hz. Linear modulation formats can achieve much higher bandwidth efficiency, thus make more efficient use of the spectrum. For example, the theoretical bandwidth efficiency of Quadrature Phase Shift Keying (QPSK) modulation format is 2 bps/Hz, and 16-QAM is 4 bps/Hz. The superior spectral efficiency characteristic of high order linear modulation schemes makes them desirable in wireless communication applications. In the proposal for the IEEE 802.16 standard on broadband wireless access, QAM is recommended as the modulation format due to the high spectral efficiency [8].

Although highly spectrally efficient, high order linear modulations have poor power efficiency. With the varying envelope, linear modulation schemes are especially sensitive to nonlinear amplification and require highly linear, low efficient amplifiers, which reduces the desirability of implementing such modulation formats in many applications. This is the reason that the less bandwidth efficient constant amplitude modulation formats like MSK are still popular in mobile communication systems, where power efficiency is extremely important. A simple architecture for power efficient linear modulation at high frequencies would be very attractive for emerging applications.

1.4 Literature Review

As discussed in Section 1.3, linear modulation methods are desirable in wireless communication system because with these methods, limited spectral resources can be effectively utilized. However, the amplitude variations of the carrier signals require linear amplification, which suffers from very low power efficiency. Therefore, it is attractive to develop a method, with which both high spectral efficiency and high power efficiency can be obtained.

1.4.1 Phase Modulation Using Nonlinear Circuits

A simple Gaussian Minimum Shift Keying (GMSK) modulator architecture operating at upper microwave frequency band has been reported [9]. This modulator employs direct modulation, resulting in reduction of the cost and complexity of the hardware architecture. The modulator is based on achieving continuous linear phase modulation of a carrier signal over the full 360° range. The 360° phase shifter is realized by using a highly linear fractional-range phase shifter and a frequency/phase multiplier. The xN frequency/phase multiplier expands the fractional phase shift range by a factor xN to full 360°, and upconverts a subharmonic input frequency by xN to 18 GHz. High power efficiency can be obtained by using an efficient Class C amplifier at the output, as GMSK is a constant envelope modulation format. The transmitted frequency can be easily extended to higher frequency range just by increasing the multiplication factor of the frequency/phase multiplier.

Although this modulator architecture is simple, and works well for generating constant envelope continuous phase modulations with high power efficiency, it can not reliably produce linear amplitude modulation and is not applicable to spectrally efficient linear modulation schemes.

1.4.2 LINC Technology

LINC technique is one of the most promising methods for obtaining linear amplification with high power efficiency. The concept is derived from the outphasing modulation technique developed in the 1930s [10]. In 1974, it was introduced as the LINC technique [11]. The concept involves decomposing any input signal into two phase modulated, but constant envelope, signals. Then the constant envelope signals are amplified through power efficient but nonlinear amplifiers separately, and finally passively combined to produce an amplified replica of the input signal. Although nonlinear components are contained in the LINC amplifier, the overall input to output transfer function of the LINC amplifier is linear [11].

The LINC concept has been developed further in various papers since it was introduced. Component signal separation and recombination was examined in [12];

a practical prototype LINC transmitter operating at 170 MHz was constructed and tested in [13]; the effect of imbalances and modulation schemes on performance of LINC transmitters was presented in [14], [15] and [16]; the effect of quantization for LINC transmitters was analyzed in [17]; a signal combiner implementation to achieve high efficiency was described in [18]; techniques for correcting the imbalances in LINC transmitter is studied in [19], [20], [21] and [22].

With the LINC architecture, both high power efficiency and spectral efficiency can be obtained. One disadvantage of this technique is that it is not suitable for implementation at upper microwave and millimeter-wave frequency bands, as it is difficult to accomplish a stable reference signal and precise vector modulation at such high frequencies.

From the literature review, it is apparent that little research has been reported on extending the direct modulation and LINC concept to linear modulation methods suitable for implementation at upper microwave and millimeter-wave frequencies. A modulator that combines direct modulation with LINC technique has advantages of simple structure, power and spectral efficiency and suitability for linear modulation schemes. If nonlinear concepts for providing frequency translation similar to those described in Section 1.4.1 were also exploited, the hardware complexity could be substantially reduced and the result would be a very attractive architecture for applications at upper microwave and millimeter-wave frequencies.

1.5 Research Objectives

This thesis focuses on developing a simple, generic linear modulator suitable for a wide range of transceiver functions required in emerging wireless communication systems operating at upper microwave and millimeter-wave frequencies. The new modulator is named LINT, an acronym for LInear modulation with Nonlinear Translation, which attempts to incorporate the desirable features of frequency translation and power efficiency into linear modulation at high frequencies. The main objectives of the research are summarized as follows:

1. Propose a new modulator architecture (LINT), which is suitable for linear

modulation schemes at microwave and millimeter-wave frequencies with high power efficiency and frequency translation.

2. Investigate the validity of LINT signal component separation and phase scale algorithm.

3. Design and simulate realistic microwave circuits for evaluation of the LINT technique.

4. Investigate the performance of the LINT technique with typical modulator impairments such as amplitude imbalance and phase noise.

1.6 Thesis Organization

This thesis is organized into seven chapters. In Chapter 2, the direct LINT modulation method is presented. The architecture of the LINT modulator is described in detail.

In Chapter 3, LINT modulating signal design and imperfections in the LINT technique that will affect the overall performance of LINT modulator is discussed. Simulation results using MATLAB for the modulating signal design are presented.

In Chapter 4, theoretical and practical considerations in FET frequency/phase multiplier design at microwave frequencies are described.

In Chapter 5, considerations for microwave circuit realization are discussed. The design procedures for simplified microwave circuits and complete microwave circuits suitable for MIC fabrication are presented.

In Chapter 6, simulation results for the simplified and complete circuits designed in Chapter 5 are presented. Two imperfections that will degrade the overall performance of LINT modulator are also simulated in this chapter.

In Chapter 7, conclusions of this research are presented and future research directives are suggested.

Chapter 2

DIRECT LINT MODULATION METHOD

2.1 Direct LINT Operation

The principle of the LINT modulator is to decompose arbitrary baseband non-constant envelope source signals into alternative baseband modulating signals used to produce two constant amplitude phase modulated signals. These two signals are then frequency translated to the desired transmitting frequency separately with two identical paths of frequency/phase multiplier chains. An efficient power amplifier operating at this high transmitting frequency in each path delivers two branches of signals at the desired transmitting power level. Finally these two high frequency and high power signals are passively recombined with a hybrid combiner. Although frequency/phase multiplier chains and power amplifiers are highly nonlinear circuits, no intermodulation distortion (IMD) will be introduced due to the constant envelope property of the input signals. In this respect, the overall direct LINT modulator is insensitive to the nonlinear characteristic of the circuits in its structure. Thus, the output signal from the modulator is a frequency translated and amplified replica of the source signal. Also high power efficiency can be obtained from this modulator since highly efficient power amplifiers are employed. The linear property of this direct LINT modulator makes it suitable for a variety of linear modulation schemes like QAM, which have a higher bandwidth efficiency than constant envelope frequency modulations. The direct LINT modulator architecture is presented in the next section.

2.2 Direct LINT Modulation Architecture

In this section the block diagram of direct LINT modulator is presented. The theoretical principle of each functional block for the modulator is described in depth.

2.2.1 Block Diagram of Direct LINT Modulator

The block diagram of the direct LINT modulator is shown in Figure 2.1. The basic principle is that the baseband source signal, $s(t)$, is separated into two constant amplitude but phase modulated signals in what is called the signal component separator (SCS) and phase scaler. The baseband constant amplitude signals are then further decomposed into in-phase (I) and quadrature (Q) components, which drive vector modulators to modulate subharmonic carrier signals. Then the two modulated signals at the subharmonic are frequency translated to the desired transmitting frequency in two identical xN frequency/phase multiplier chains. After frequency translation, the two path signals are amplified through power amplifiers and then passively recombined to produce a bandpass replica of the original input source signal. More details of the direct LINT modulator architecture are described next.

2.2.2 SCS and Phase Scaler

The principle of the SCS is similar to the signal separation method of the LINC transmitter [14], but also requires a phase scaler.

A general baseband representation of the bandlimited modulating signal can be written as

$$s(t) = r(t)e^{j\phi(t)};\ 0 < r(t) < r_{max} \tag{2.1}$$

where $r(t)$ is the amplitude of the baseband signal, and $\phi(t)$ is the phase of the baseband signal, and represents the desired amplitude and phase modulation of the carrier signal. This signal can be split into two signals, $s_{i1}(t)$ and $s_{i2}(t)$, by adding and subtracting a perpendicular vector from $s(t)$ as shown in Figure 2.2. Hence

$$s_{i1}(t) = s(t) + e(t), \tag{2.2}$$

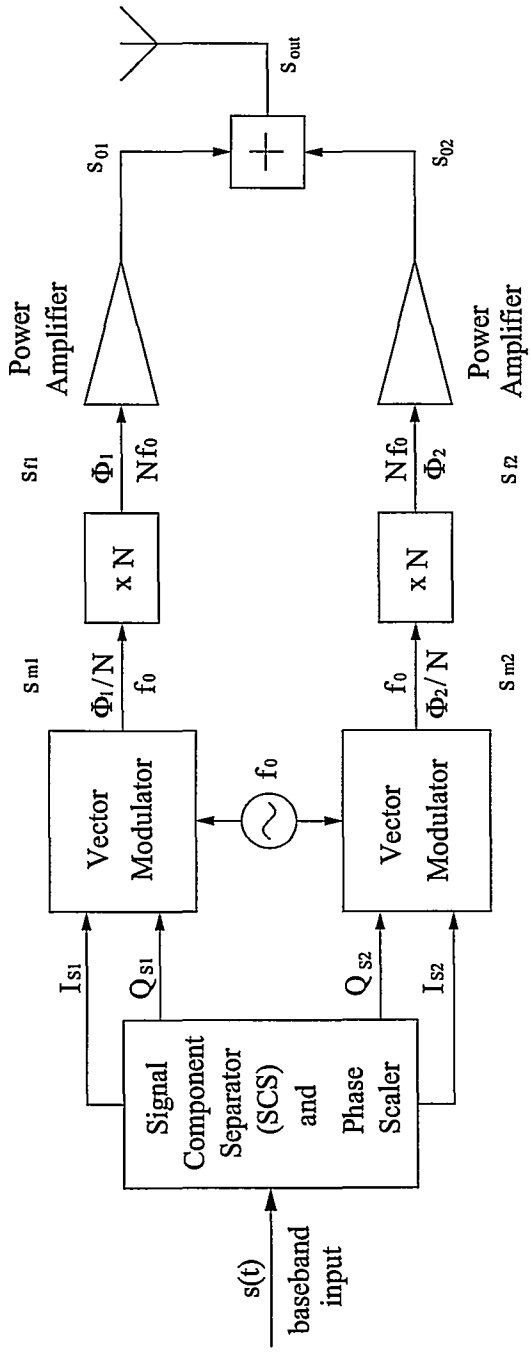


Figure 2.1 Block diagram of direct LINT modulator .

$$s_{i2}(t) = s(t) - e(t), \tag{2.3}$$

where $e(t)$ is a signal that is in quadrature with the source signal $s(t)$, and can be calculated by [14]

$$\begin{aligned} e(t) &= js(t)\sqrt{\frac{r_{max}^2}{\mid s(t) \mid^2} - 1} \\ &= \sqrt{r_{max}^2 - \mid s(t) \mid^2} e^{j[\phi(t)+\frac{\pi}{2}]}; \mid e\ (t)\ \mid \leq r_{max}. \end{aligned} \tag{2.4}$$

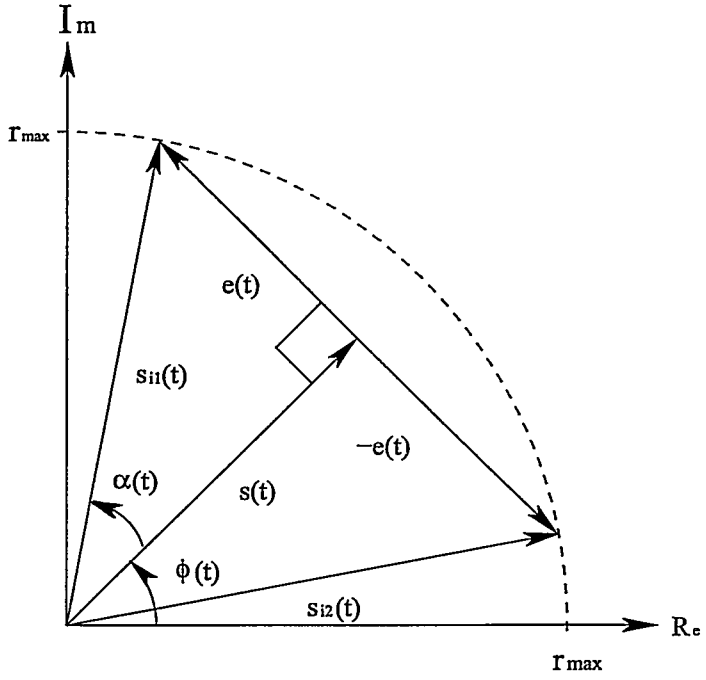


Figure 2.2 Signal component separation.

The two decomposed signals, $s_{i1}(t)$ and $s_{i2}(t)$, have constant amplitudes such that

$$2s(t) = s_{i1}(t) + s_{i2}(t),\ \mid s_{i1}(t) \mid = \mid s_{i2}(t) \mid = r_{max}, \tag{2.5}$$

where

$$s_{i1}(t) = r_{max} e^{j[\phi(t)+\alpha(t)]}, \tag{2.6}$$

$$s_{i2}(t) = r_{max} e^{j[\phi(t)-\alpha(t)]}, \tag{2.7}$$

$$\alpha(t) = \arccos[\frac{r(t)}{r_{max}}]. \tag{2.8}$$

In LINC transmitter, the I and Q components of the decomposed constant amplitude signals are directly fed into vector modulators and then power amplified. But for the proposed direct LINT modulator, the separated signals need to be treated further. The phases of the two constant envelope signals, $s_{i1}(t)$ and $s_{i2}(t)$, are divided by an integer N to account for the later phase multiplication by N, while the amplitude is maintained constant. Hence, through SCS and phase scaler the input source signal $s(t)$ is eventually separated into two constant envelope but phase modulated components, which can be written as

$$s_1(t) = r_{max} e^{j[\phi(t)/N + \alpha(t)/N]}, \tag{2.9}$$

$$s_2(t) = r_{max} e^{j[\phi(t)/N - \alpha(t)/N]}. \tag{2.10}$$

2.2.3 Vector Modulator

Two methods can be used to phase modulate the subharmonic carrier; vector modulator or phase shifting. A linear phase shifter to accomplish continuous 360° linear phase modulation employing a fractional phase shifter followed by frequency/phase multiplication is presented in [23]. An undesired characteristic of the phase modulation is the phase wrapping problem at the $\pm\pi$ phase point in the carrier phase [24], which is caused by a voltage discontinuity from maximum to minimum value at the voltage control port. The effect of voltage discontinuity is a collapse in the modulation vector diagram around the $\pm\pi$ phase point and distortion in the eye diagram. In a vector modulator, 360° phase modulation is produced by summing two continuous sinusoidal waves with appropriate amplitudes in quadrature. Therefore, phase modulation using a vector modulator avoids the phase wrapping problem, and is a more suitable choice. The function of a vector modulator is to translate I and Q components in the input signal by a carrier frequency components (also represented by I and Q components). The block diagram of a vector modulator is shown in Figure 2.3. It is composed of a local oscillator,

mixers, and a combiner. First, I and Q input signals are multiplied by the I and Q components from a subharmonic carrier frequency (provided by a local oscillator). Then the two signals are summed together to form a modulated signal. The resulting modulated signal, $s_m(t)$, can be expressed as

$$s_m(t) = I(t)\cos(2\pi f_0 t) - Q(t)\sin(2\pi f_0 t), \tag{2.11}$$

where f_0 is the subharmonic carrier frequency.

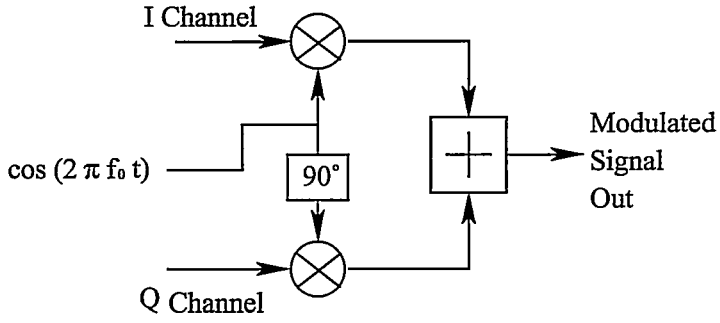


Figure 2.3 Block diagram of vector modulator.

Derived from Equation 2.9, the I and Q components of $s_1(t)$ are given by

$$I_{s1}(t) = r_{max}\cos[\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}], \tag{2.12}$$

$$Q_{s1}(t) = r_{max}\sin[\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]. \tag{2.13}$$

And the I and Q components for $s_2(t)$ are given by

$$I_{s2}(t) = r_{max}\cos[\frac{\phi(t)}{N} - \frac{\alpha(t)}{N}], \tag{2.14}$$

$$Q_{s2}(t) = r_{max}\sin[\frac{\phi(t)}{N} - \frac{\alpha(t)}{N}]. \tag{2.15}$$

According to Equation 2.11 the modulated signal at the subharmonic carrier frequency for the upper path of the direct LINT modulator can be expressed as

$$s_{m1}(t) = r_{max}\cos[2\pi f_0 t + \frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]. \tag{2.16}$$

Similarly the modulated signal at subharmonic carrier frequency for the lower path is given by

$$s_{m2}(t) = r_{max}\cos[2\pi f_0 t + \frac{\phi(t)}{N} - \frac{\alpha(t)}{N}]. \tag{2.17}$$

For an ideal vector modulator, the I and Q components of the subharmonic carrier signal are exactly 90° difference in phase. But for a real vector modulator, the I and Q components are not perfectly in quadrature, and there is a small phase error between the quadrature inputs of the carrier signal. As the result of this small phase error, the sum output of the vector modulator will have amplitude error as well as phase error, which will consequently degrade the performance of the direct LINT modulator. Effect of imbalance in the vector modulator on the LINT modulator is discussed in Chapter 3.

2.2.4 Frequency/phase Multiplier Chain

Frequency/phase multipliers provide a convenient means for converting a frequency stable, low frequency oscillator signal to higher frequencies. The principle is to employ a nonlinear device to generate harmonics of a fundamental frequency continuous wave (CW) input signal. The desired Nth harmonic output is selected, while the fundamental frequency and all other harmonic signals are rejected, usually by a resonator tuned to the Nth harmonic of the input frequency.

Since frequency and phase are related (frequency is the time derivative of phase), the process of frequency multiplication is also a process of instantaneous phase multiplication by a multiplication factor N. If higher order of harmonic frequency is required, several stages of frequency multipliers can be connected in cascade to provide a total multiplication factor that is the product of the multiplication factor of each stage. Thus, a CW input signal through a xN multiplier chain results in an output signal with carrier frequency and instantaneous phase multiplied by N. For the proposed LINT modulator, the frequency translated output signals derived from the subharmonic carrier modulated signals (see Equations 2.16 and 2.17) through the upper path and lower path xN frequency/phase multiplier chains can

be expressed as

$$s_{f1}(t) = r_{max} G_M \cos[2\pi N f_0 t + \phi(t) + \alpha(t)], \tag{2.18}$$

$$s_{f2}(t) = r_{max} G_M \cos[2\pi N f_0 t + \phi(t) - \alpha(t)], \tag{2.19}$$

where G_M denotes the gain of multiplier chain. It can be seen that after frequency/phase multiplication, the signal carrier frequency is translated up to N times of the subharmonic carrier frequency f_0, and the phase is restored to ϕ - the phase of baseband signal after SCS and before phase scaling (see section 2.2.2).

2.2.5 Power Stage

Amplifiers are one of the most frequently used circuits involving active microwave components. Power amplifiers are usually required to increase the output power level to a sufficient level for a transmitter. There are three basic modes of operation for power amplifiers: Class A, Class B and Class C. The classification is based on different output current conduction characteristics during the input signal cycle. When the output current flows for the full period of the input voltage cycle, the amplifier is operated in the Class A mode. If the output current flows for half the period of the input cycle, the amplifier is designated as a Class B amplifier. If the output current flows for less than half the period of the input voltage cycle, the amplifier is called a Class C amplifier. The Class A amplifier is referred to as linear amplifier, for which the output power increases linearly with the input power. The input signal, whether constant envelope or non-constant envelope, can be linearly amplified without distortion. Class B and Class C amplifiers have a nonlinear characteristic, and the output power is not in proportional to the input power. Thus, if the input signal has varying amplitude, the nonlinear behavior in Class B and C amplifiers introduces distortion in the amplified signal.

The Class A amplifier suffers from very low DC (direct current) to RF (radio frequency) power efficiency, which is defined as

$$\eta = \frac{P_{out}}{P_{dc}}, \tag{2.20}$$

where P_{out} is the output signal power and P_{dc} is DC power supplied. Low efficiency is not suitable for highly integrated or portable equipment, because large batteries are required to supply excess power, and large transistors and heat sinks are required to dissipate this power. For the LINT modulator, an arbitrary baseband input signal is separated and translated into two constant envelope signals, thus, high efficiency Class B or Class C amplifiers can be employed. With $s_{f1}(t)$ and $s_{f2}(t)$ as input signals for the upper and lower paths, the power amplifier output signals can be expressed as

$$s_{o1}(t) = G_A G_M r_{max} \cos[2\pi N f_0 t + \phi(t) + \alpha(t)], \tag{2.21}$$

$$s_{o2}(t) = G_A G_M r_{max} \cos[2\pi N f_0 t + \phi(t) - \alpha(t)], \tag{2.22}$$

where $s_{o1}(t)$ is the amplified signal for the upper path of the modulator, $s_{o2}(t)$ is the amplified signal for the lower path of the modulator, and G_A is the amplifier gain. Here, the phase delay of the two power amplifiers is assumed to be identical and not included in the phase of the modulated signals; but would produce error if the amplifiers are not well matched.

2.2.6 Hybrid Combiner

Hybrid combiners are passive microwave components used for signal combining. Although a hybrid combiner can be represented as a multiport network, a simple three-port (T junction) or a four-port structure with the fourth port terminated is applicable for the LINT modulator. Among these ports, two of them are used to receive input signals, which are added at the output port to form a combined signal. Some forms of hybrid combiners may have either a 90° or a 180^0 phase shift between the input ports [25]. That means one path of the input signal has to be shifted 90° or 180° in order to have the two input signals properly summed in phase. The phase shift at one path of the input signal can be easily performed at the baseband after SCS and phase scaler. For example, a phase shift of $90°/N$ can be added to the phase of baseband modulating signal at upper branch, $s_1(t)$, resulting in a phase shift of 90° after frequency/phase multiplication. The 3 dB combiner

is the most frequently used hybrid combiner in active or passive circuit design. With the assumption that the phase shift through the combiner is compensated, the combined output signal related to $s_{o1}(t)$ and $s_{o2}(t)$ can be expressed as (see Figure 2.2)

$$s_o(t) = \frac{1}{\sqrt{2}} G_A G_m r(t) \cos\left[2\pi N f_0 t + \phi(t)\right], \tag{2.23}$$

where the $\frac{1}{\sqrt{2}}$ reduction in amplitude is introduced by an ideal 3 dB hybrid combiner.

Compared with input source signal $s(t)$ (see Equation 2.1), the combined bandpass signal $s_o(t)$ is amplified and modulated at a carrier frequency Nf_0, and the instantaneous phase of the combined signal is exactly the same as the input source signal. That means that the modulator performs an amplification and frequency translation process of the input signal without distortion.

2.3 Summary

The direct LINT modulator consists of a SCS and phase scaler, and two identical branches of vector modulators, frequency/phase multiplier chains, power amplifiers, and a hybrid combiner. The SCS and phase scaler performs the baseband signal processing, decomposing the input source signal into two constant envelope signals. The vector modulator is used to phase modulate the subharmonic carrier signals with the constant envelope signals. The constant amplitude nature of the phase modulated signals allows them to be processed further in nonlinear circuits. In the frequency/phase multiplier chain, the subharmonic carrier signal is translated to a signal at a higher microwave frequency. In theory, the carrier frequency could be made extremely high by increasing the multiplication factor of the chain. Highly efficient power amplifiers are employed to prepare the signal for transmission at a required power level. Finally, the two amplified signals are combined to produce a high frequency and amplified version of the input source signal. Because any input source signal can be decomposed into constant amplitude signals, the direct LINT modulator is suitable for transmission of amplitude modulated signals like QAM. Also, high power efficiency is possible with this modulator since highly efficient amplifiers are employed as power stage. Traditional QAM transmitters typically

have poor power efficiency since linear power amplifiers are required to amplify the non-constant envelope signals without distortion.

Chapter 3

16-QAM MODULATION USING LINT

3.1 16-QAM Modulation Scheme

Modulation is the process by which some property of a carrier signal, namely, the amplitude, frequency or phase is varied in accordance with a modulating wave [26]. Essentially, there are two main categories of modulation: analog modulation and digital modulation. In analog modulation, the carrier property is varied continuously in proportion to the analog signal. However, digital modulation has data chosen from a discrete signal set with the carrier varied in accordance with the discrete message.

Digital modulation schemes transform digital signals into waveforms that are compatible with the nature of the communications channel. There are two major categories of digital modulation. One category uses a constant amplitude carrier and carries the information in phase or frequency variations. Examples include FSK and PSK. The other category conveys the information in carrier amplitude variations and is known as ASK. QAM is a quadrature ASK modulation scheme, in which two quadrature carriers are separately amplitude modulated and then combined to form the amplitude and phase modulated resultant.

Digital modulation involves mapping a binary information sequence into a set of symbols. The length of each symbol is a k-bit block obtained from $k = \log_2 M$, where M is the number of symbols in the modulation scheme. The encoded symbols transmit at a rate of $R_s = R_b/k$ symbols per second (sym/s), where R_b is the bit rate of binary information sequence in unit of bits per second (b/s). 16-QAM is a modulation scheme that maps a binary data sequence to 16 symbols ($M = 16$).

Thus each symbol is represented by 4 bits ($k = 4$) of binary data. The signal space constellation of in-phase and quadrature components for 16-QAM is shown in Figure 3.1 and Figure 3.2. Each of the quadrature components has four amplitude levels, which gives 16 possible symbols at the transmit output. The various possible combinations of I and Q for 16-QAM is shown in Figure 3.3, which is referred to as a constellation diagram. On this plot, 16-QAM symbols are equally spaced in a rectangular area, and each is represented by a unique amplitude and phase.

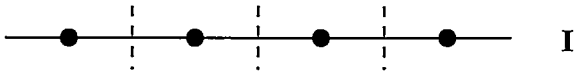


Figure 3.1 In-phase constellation diagram for 16-QAM.

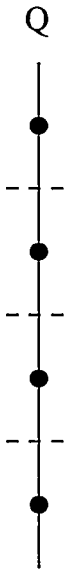


Figure 3.2 Quadrature constellation diagram for 16-QAM.

The spectrum of a flat top pulse is infinite, while the bandwidth capacity of the channel is limited. A pulse shaping function is usually added to restrict the spectrum of symbols to a limited bandwidth. Pulse shaping is usually performed by a pre-filter. QAM is a digital modulation scheme which is accomplished by separating the binary information sequence into I and Q components, pre-filtering, and impressing them on the two quadrature carriers. This is explained further in Section 3.2.

The time waveforms for each QAM modulated symbol can be expressed as [7]

$$\begin{aligned} s_m(t) &= Re[(A_{mI} + jA_{mQ})g(t)e^{j2\pi f_c t}] \\ &= A_{mI}(t)g(t)\cos(2\pi f_c t) - A_{mQ}(t)g(t)\sin(2\pi f_c t);\ m = 1, 2, ..., M \quad (3.1) \end{aligned}$$

where A_{mI} and A_{mQ} are amplitudes of the quadrature carriers corresponding to the mth symbol in the set, $g(t)$ is the pulse shaping function and M is the number of symbols in the symbol set.

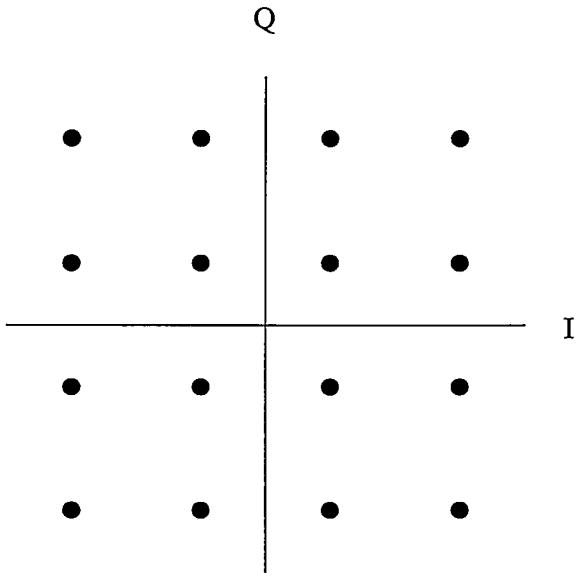


Figure 3.3 Constellation diagram for 16-QAM.

The lowpass equivalent waveform for QAM signal is complex-valued and can be expressed in terms of quadrature components as

$$u(t) = u_I(t) + ju_Q(t), \quad (3.2)$$

where

$$u_I(t) = A_{mI}g(t), \quad (3.3)$$

$$u_Q(t) = A_{mQ}g(t), \quad (3.4)$$

and $u_I(t)$ is the I component and $u_Q(t)$ is the Q component of $u(t)$. The lowpass equivalent can also be represented in polar form as

$$u(t) = u_m e^{j\theta_m} g(t), \tag{3.5}$$

where

$$u_m = \sqrt{A_{mI}^2 + A_{mQ}^2}\ , \tag{3.6}$$

$$\theta_m = \arctan(\frac{A_{mQ}}{A_{mI}}), \tag{3.7}$$

and u_m denotes the amplitude of the modulated signal, and θ_m denotes the phase of the modulated signal at the mth symbol.

From this expression, it is apparent that QAM is a combined amplitude and phase modulation method.

3.2 Modulating Signal Design

As described in the previous section, the 16-QAM modulated signal has a large amplitude variation with time. As such, it is a suitable modulation for evaluation of the LINT modulator. The block diagram for the LINT source signal generation is shown in Figure 3.4.

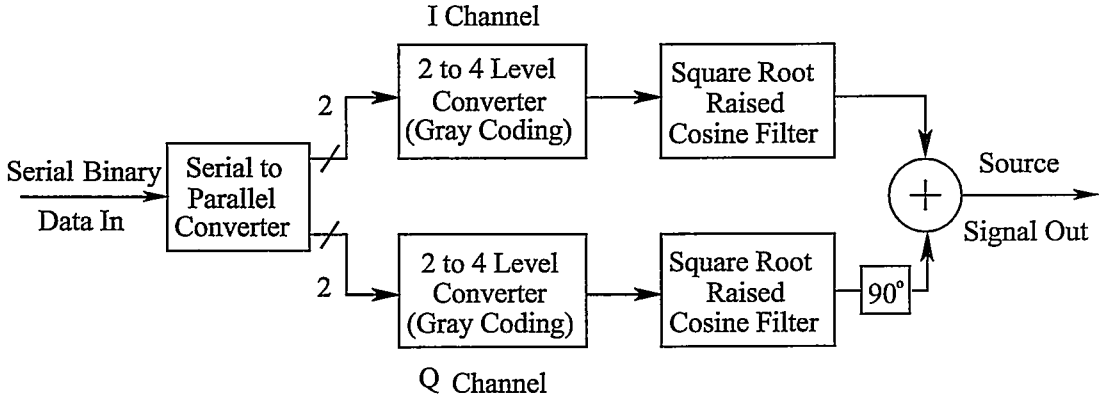


Figure 3.4 Block diagram for LINT source signal generation .

The binary information sequence is converted into two parallel channels, the I channel and Q channel. Gray coding is used for signal mapping. The four amplitude

levels for each channel in accordance with Gray code are shown in Table 3.1. For 16-QAM, such a mapping allows only one bit error between adjacent symbols (see Figure 3.5).

Table 3.1 Relationship between amplitude level and Gray code.

level	Gray code
-3	00
-1	01
+1	11
+3	10

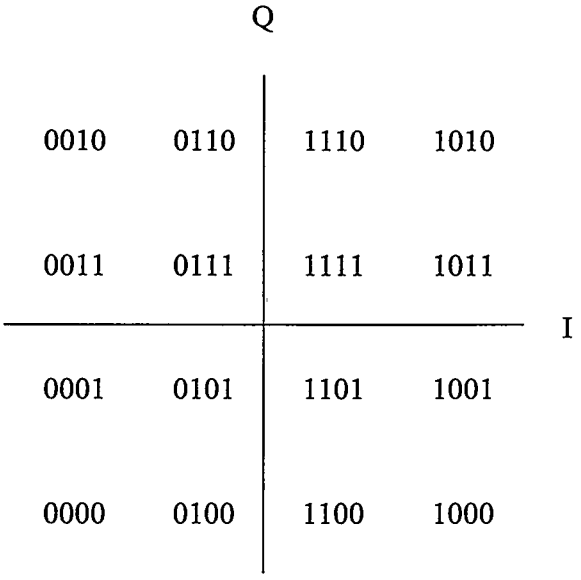


Figure 3.5 Gray encoded constellation diagram for 16-QAM.

Pre-filtering is done at baseband to limit the spectrum of symbols to a finite bandwidth. Filtering causes symbols to spread in time. For consecutive symbols, this spreading causes the symbol time waveforms to overlap, which is called intersymbol interference (ISI). ISI can be eliminated by carefully chosen transfer functions of the filter. Raised cosine (RC) filter is the type of commonly used filter

for such a purpose. Its transfer function $H_{RC}(f)$ is given by [7]

$$H_{RC}(f) = \begin{cases} 1 & 0 \leq |f| \leq \frac{(1-\alpha)}{2T_s} \\ \frac{1}{2}\{1+\cos[\frac{\pi}{\alpha}(|f| - \frac{1-\alpha}{2})]\} & \frac{(1-\alpha)}{2T_s} \leq |f| \leq \frac{(1+\alpha)}{2T_s} \\ 0 & |f| \geq \frac{(1+\alpha)}{2T_s} \end{cases}, \tag{3.8}$$

where α is the filter roll-off factor and T_s is the symbol period. Figure 3.6 shows the frequency response of raised cosine filter with three different values of α. The frequency axis is normalized to the symbol rate $(1/T_s)$. It can be seen from this plot that the sharpness of the filter is controlled by roll-off factor α, and $\alpha = 0$ corresponds to an ideal brick-wall filter. The bandwidth B of the filter is defined by $B = \frac{(1+\alpha)}{2T_s}$.

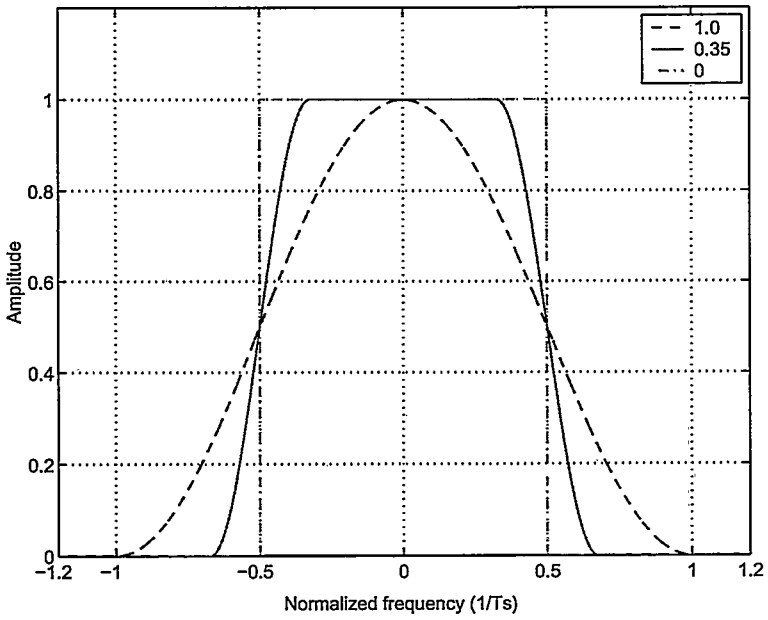


Figure 3.6 Frequency response of raised cosine filter.

The impulse response of a RC filter can be expressed mathematically as [7]

$$h_{RC}(t) = \frac{sinc(\pi\frac{t}{T_s})\cos(\pi\alpha\frac{t}{T_s})}{1-(\frac{2\alpha t}{T_s})^2}, \tag{3.9}$$

and is plotted in Figure 3.7. Although the impulse response is infinite in time, zeros occur at integer multiples of symbol periods. ISI can be avoided by sampling the

symbol stream exactly where the impulse response goes through zero.

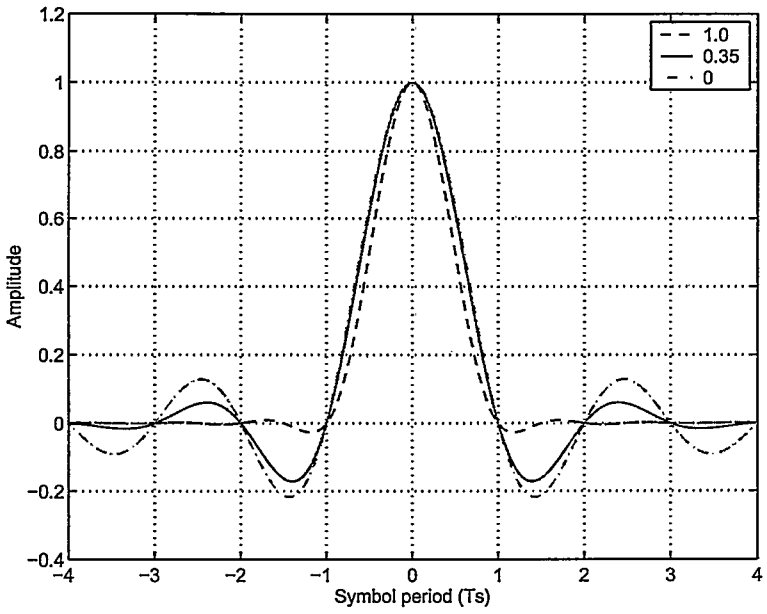


Figure 3.7 Impulse response of raised cosine filter.

The overlapping plot of I channel and Q channel samples through the RC filter at one or multiple symbol periods is called eye diagram. An eye diagram is shown in Figure 3.8 with $\alpha = 0.35$. An Eye diagram is used to diagnose problems of ISI in transmission system [27]. The trajectory of a 16-QAM vector diagram, which is the combination of RC filtered I and Q channels is shown in Figure 3.9.

To obtain zero ISI performance, the RC filter must apply to the whole transmission path, including transmitter and receiver. The transfer function of a RC filter is commonly split to two equal functions: one is for transmitter and the other for receiver. The new filter is called square root raised cosine (SRRC) filter because it has a transfer function that is a square root of the transfer function of a RC filter. The frequency response $H_{SRRC}(f)$ of a SRRC filter is given by [28]

$$H_{SRRC}(f) = \begin{cases} 1 & 0 \le |f| \le \frac{(1-\alpha)}{2T_s} \\ \sqrt{\frac{1}{2}\{1+\cos[\frac{\pi}{\alpha}(|f| - \frac{1-\alpha}{2})]\}} & \frac{(1-\alpha)}{2T_s} \le |f| \le \frac{(1+\alpha)}{2T_s} \\ 0 & |f| \ge \frac{(1+\alpha)}{2T_s} \end{cases}, \qquad (3.10)$$

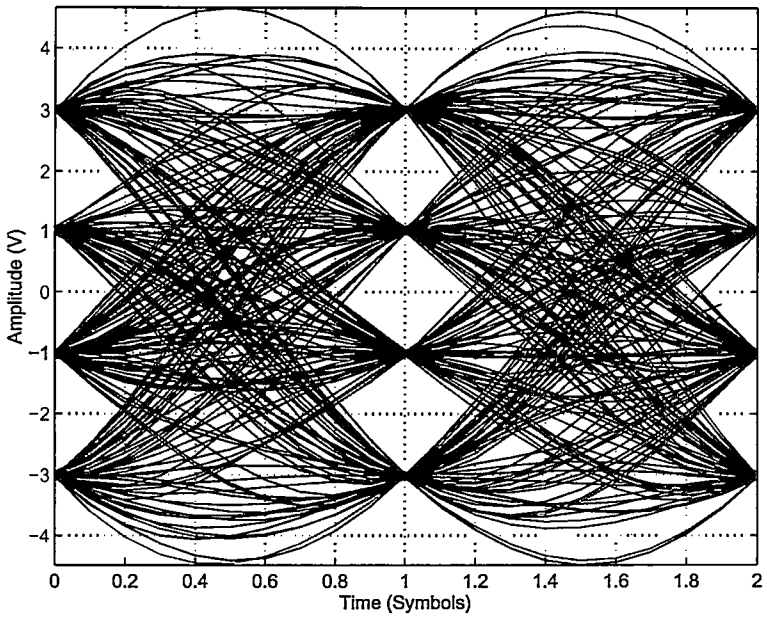


Figure 3.8 Eye diagram for 16-QAM with $\alpha = 0.35$.

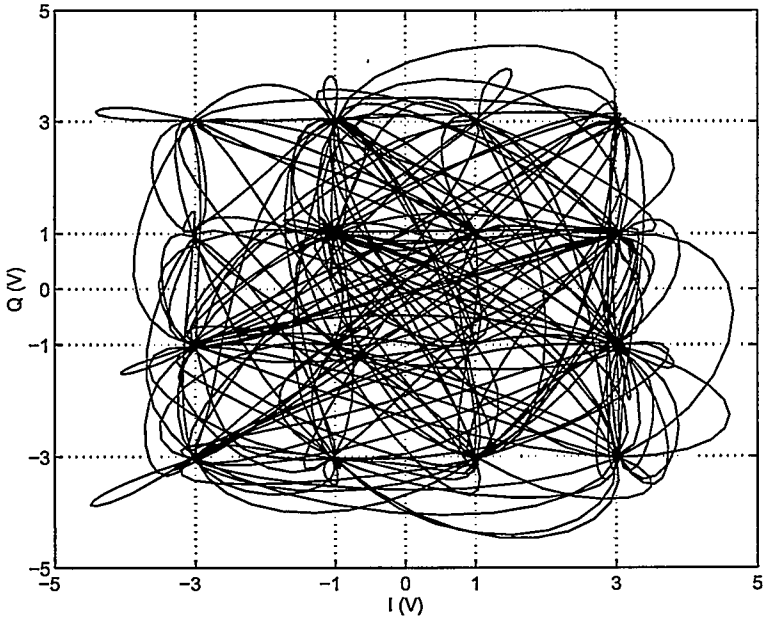


Figure 3.9 RC filtered vector diagram for 16-QAM .

and the corresponding impulse response of the SRRC filter can be expressed as [28]

$$h_{SRRC}(t) = \frac{4\alpha}{\pi\sqrt{T_s}} \frac{\cos[\frac{(1+\alpha)\pi t}{Ts}] + \frac{T_s}{4\alpha t}\sin[\frac{(1-\alpha)\pi t}{T_s}]}{1-(\frac{4\alpha t}{T_s})^2}. \tag{3.11}$$

The SRRC filtered trajectory of a 16-QAM vector diagram with $\alpha = 0.35$ is shown in Figure 3.10.

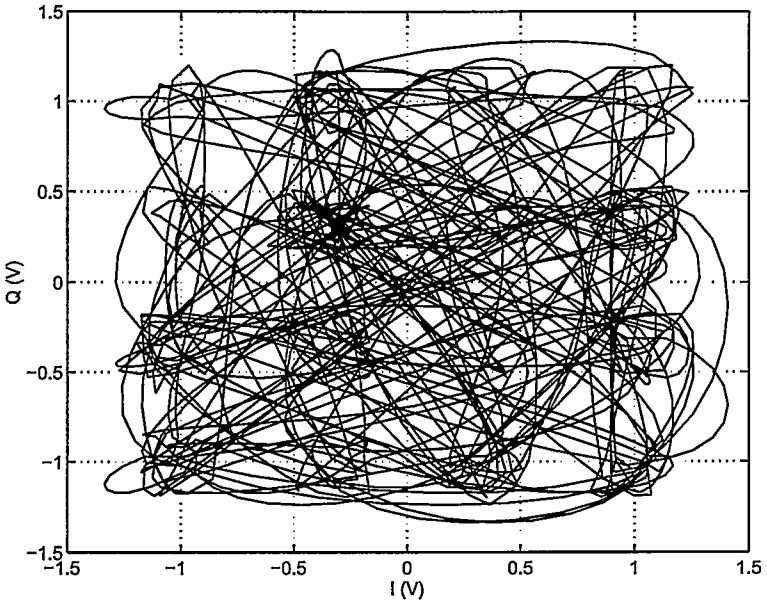
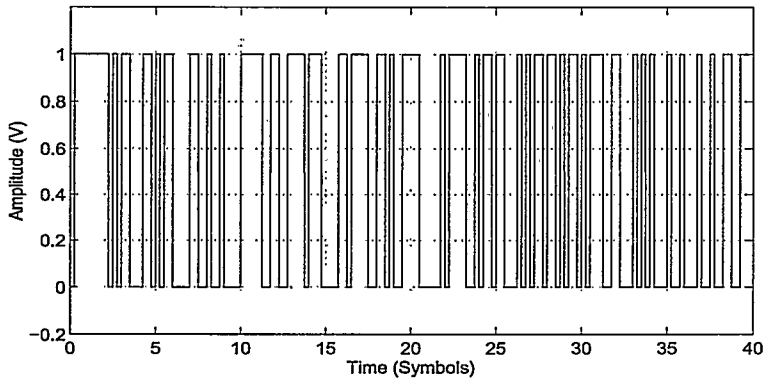


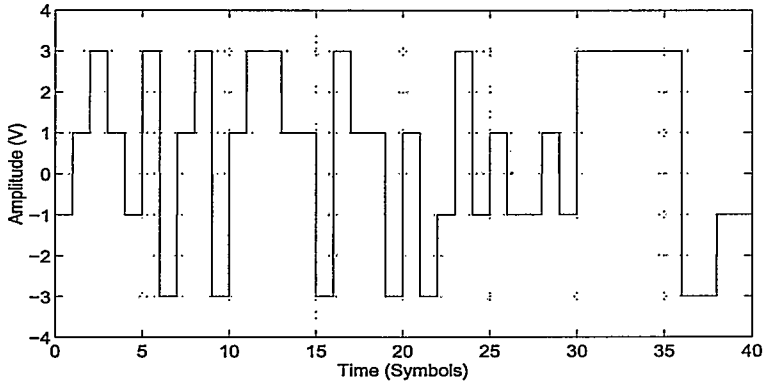
Figure 3.10 SRRC filtered vector diagram for 16-QAM .

The time waveforms that show the evolution from a binary data sequence to a LINT source signal for the I channel are presented in Figure 3.11. The time waveform of the binary input signal is shown in Figure 3.11(a), the Gray encoded signal is shown in Figure 3.11(b), and the SRRC filtered signal with $\alpha = 0.35$ is shown in Figure 3.11(c). The SRRC filter has a time delay, which results in the SRRC filtered signal lagging behind the input Gray encoded signal. To show all the waveforms started from the same time (zero), the time axis of Figure 3.11(c) is shifted.

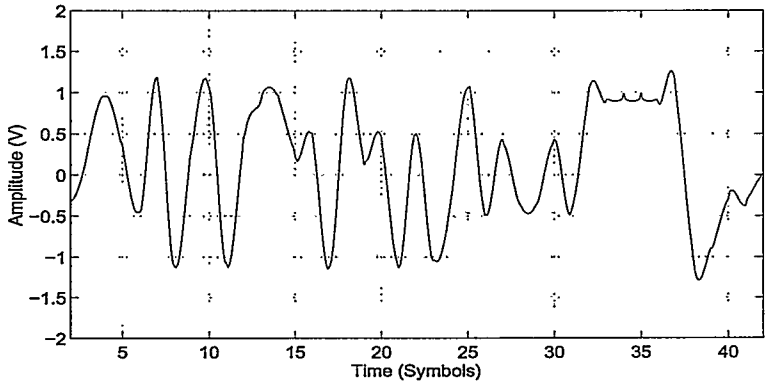
The input source signal for the LINT modulator is formed by summing the filtered I channel and Q channel signals in quadrature. The input source signal can



(a) Time waveform of binary input signal.



(b) Time waveform of Gray encoded signal.



(c) Time waveform of SRRC filtered signal.

Figure 3.11 Time domain representations of inphase signal at various stages.

be written as

$$s(t) = I(t) + jQ(t). \tag{3.12}$$

The baseband signal processing through the SCS and phase scaler is simulated using MATLAB software. In the LINT modulator, the input source signal is decomposed in the SCS into two constant envelope signals with phase range from 0° to 360° (see Equations 2.6 to 2.8). The trajectory of the constant envelope signal for the upper branch is shown in Figure 3.12, where $r_{max} = 5$ is assumed. It can be seen from this figure that the amplitude of the signal is constant, since the trajectory is a circle. The phase of the constant envelope signal between symbol intervals for the upper branch is shown in Figure 3.13. The modulating signal for the LINT modulator is formed by scaling the phases of the constant envelope signals after SCS by an integer N. The mathematical expressions of modulating signals for the upper path and lower path can be found in Equations 2.9 and 2.10 respectively. The trajectory of the modulating signal for the upper branch is shown in Figure 3.14. The phase of the modulating signal for the upper branch is shown in Figure 3.15. Here $N = 12$ is assumed (see Section 2.2.2). The modulating signal keeps constant envelope property, but the phase is constrained within 30°.

3.3 Effect of Imperfections

In this section, some practical considerations that may degrade the overall performance of LINT modulator are discussed. The effects of these on LINT performance are presented in Sections 6.2 and 6.3.

3.3.1 Amplitude and Phase Imbalance

The linearity of the LINT architecture is based on the condition that the two paths of multiplier chains and power amplifiers are well balanced in terms of amplitude and phase errors. The tight requirement on the matching of the two paths is a potential limitation of the LINT technique because in practice, the condition is difficult to achieve. Due to the differences in electrical lengths, thermal drift, and component differences and aging, the gains and phase delays between the two

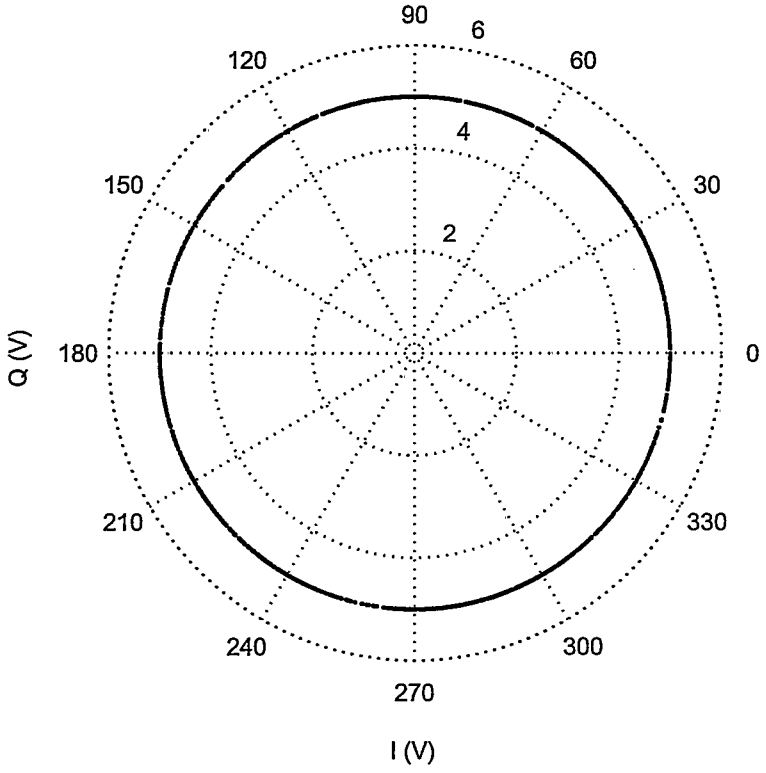


Figure 3.12 Trajectory of constant envelope signal after SCS for upper branch.

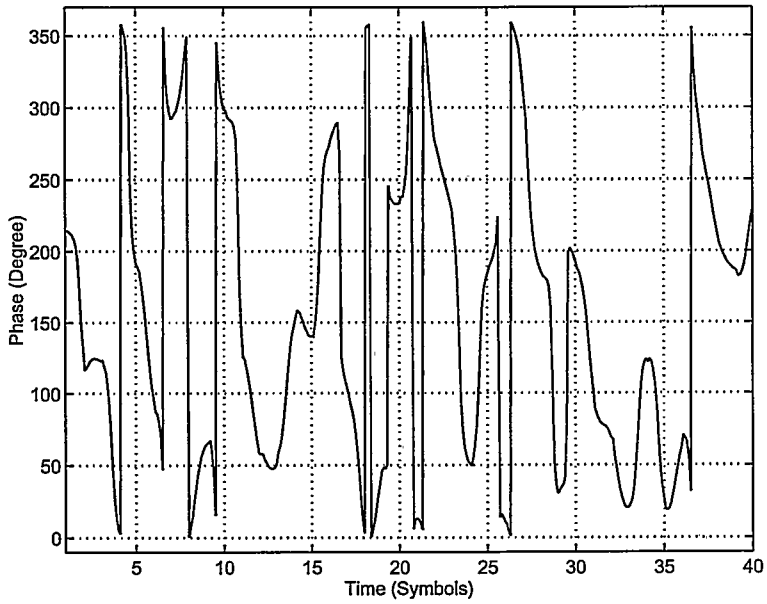


Figure 3.13 Phase of constant envelope signal after SCS for upper branch.

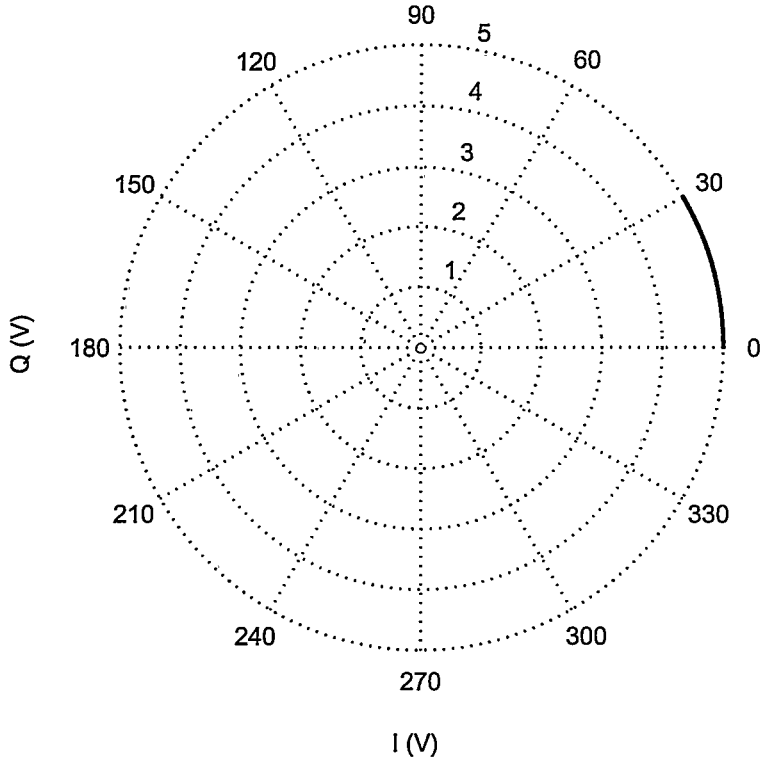


Figure 3.14 Trajectory of modulating signal for upper branch.

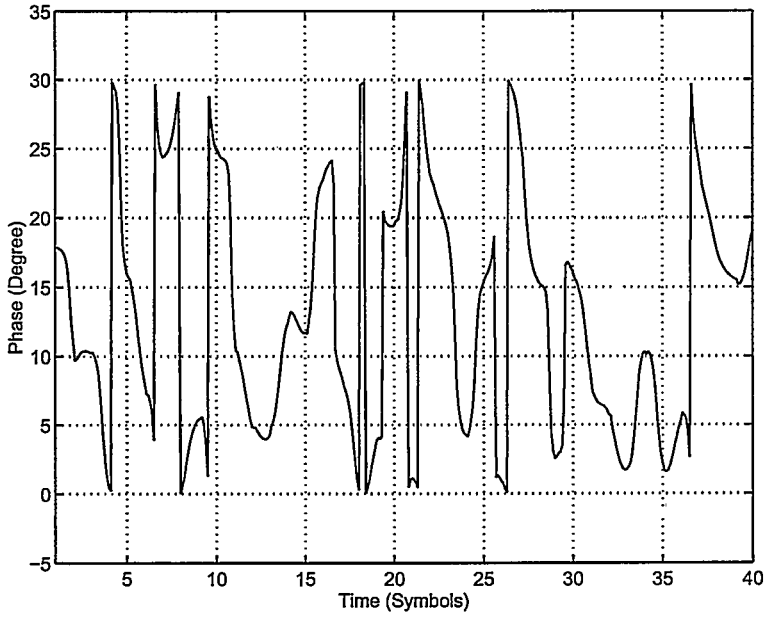


Figure 3.15 Phase of modulating signal for upper branch.

paths are not exactly the same. The imbalance between the two branches results in incomplete cancellation of the quadrature signal e(t) (see Section 2.2.2) at the input of the hybrid combiner, which consequently causes distortion and power spectrum spreading [19]. LINT performance is degraded by the imbalance characteristic since the out of band spectrum may leak into adjacent channels, introducing adjacent channel interference (ACI), and the distortion causes ISI.

Several methods are proposed to solve this problem for the LINC transmitter [19] [20] [21] [22]. Reference [21] presented a calibration technique for iterative correction of the gain and phase errors of the LINC transmitter. With the proposed method, the LINC output is translated to baseband by use of a downconversion mixer and allows a correction algorithm to operate at the baseband frequency. With the correction algorithm in [21], the gain and phase imbalance are measured and compensated iteratively, and with several iterations, the gain and phase error are able to converge to an arbitrarily low level. Although a constant power gain for the amplifiers is assumed, the algorithm will not lose generality for a nonlinear power amplifier since the algorithm is iterative [21]. Similar methods of error correction could be applied to the LINT modulator, but this is beyond the scope of the present research.

Another source of imbalance occurs at the input of the multiplier chains. With the development of modern digital signal processing (DSP) technology, the SCS in the LINC transmitter can be implemented with software using a DSP device [13]. Signals are represented in a finite word length in a DSP device. An amplitude error as well as a phase error between the two paths of constant envelope signals $s_{i1}(t)$ and $s_{i2}(t)$ are introduced due to the quantization error of the quadrature signal $e(t)$. The detailed analysis of quantization errors in SCS can be found in [17]. The similar errors exist in the LINT modulator since the same vector decomposition algorithm is employed in the LINT modulator as that in the LINC transmitter. After the vector modulators, the two path signals presented at the input of the multiplier chains will have amplitude and phase imbalance at the subharmonic carrier frequency.

As mentioned in Section 2.2.3, a practical vector modulator is not perfectly

balanced. Assuming that there is a small phase error between the quadrature inputs of the carrier signal, the resultant I and Q components of the carrier signal are

$$I_o(t) = \cos(2\pi f_o t), \tag{3.13}$$

$$Q_o(t) = \sin(2\pi f_o t + \sigma), \tag{3.14}$$

where σ is the phase error.

The output of the vector modulator in the upper branch then becomes

$$\begin{aligned} s'_{m1}(t) &= I_{s1}(t)I_o(t) - Q_{s1}(t)Q_o(t) \\ &= r_{max}\cos[\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]\cos(2\pi f_o t) - \\ &\quad r_{max}\sin[\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]\sin(2\pi f_o t + \sigma) \\ &= (\frac{1}{2} + \frac{1}{2}\cos\sigma)r_{max}\cos\{2\pi f_o t + [\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]\} + \\ &\quad (\frac{1}{2} - \frac{1}{2}\cos\sigma)r_{max}\cos\{2\pi f_o t - [\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]\} - \\ &\quad \frac{1}{2}\sin\sigma r_{max}\sin\{2\pi f_o t + [\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]\} + \\ &\quad \frac{1}{2}\sin\sigma r_{max}\sin\{2\pi f_o t - [\frac{\phi(t)}{N} + \frac{\alpha(t)}{N}]\}, \end{aligned} \tag{3.15}$$

where I_{s1} and Q_{s1} are the I and Q components of the output signal from the SCS and phase scaler in the upper branch (see Equations 2.12 and 2.13). Comparing Equation 3.15 with the output signal of an ideal vector modulator (see Equation 2.16), the above equation demonstrates that distortion is introduced due to the imbalance between I and Q branches of the vector modulator.

In theory, the phase error in the vector modulator can also be compensated by adjusting the I and Q components of input baseband signal. For example, the I and Q components of the signal after SCS and phase scaler in the upper branch are adjusted such that

$$\hat{I}_{s1}(t) = I_{s1}(t) + Q_{s1}(t)\frac{\sin\sigma}{\cos\sigma}, \tag{3.16}$$

$$\hat{Q}_{s1}(t) = \frac{Q_{s1}(t)}{\cos\sigma}, \tag{3.17}$$

where $I_{s1}(t)$ and $Q_{s1}(t)$ are the I and Q components of $s_1(t)$, as shown in Equations 2.12 and 2.13, σ is the small phase error between the quadrature inputs of the carrier signal.

Modulated through the vector modulator with phase error σ, the modulating signal for the upper branch can be written as

$$\hat{s}_{m1}(t) = \hat{I}_{s1}(t)I_0(t) - \hat{Q}_{s1}(t)Q_0(t). \tag{3.18}$$

Substituting $I_0(t)$ and $Q_0(t)$ in Equations 3.13 and 3.14, $\hat{I}_{s1}(t)$ and $\hat{Q}_{s1}(t)$ in Equations 3.16 and 3.17, and $I_{s1}(t)$ and $Q_{s1}(t)$ in Equations 2.12 and 2.13, the corrected modulating signal for the upper branch can be obtained as

$$\begin{aligned}
\hat{s}_{m1}(t) &= [I_{s1}(t) + Q_{s1}(t)\frac{\sin\sigma}{\cos\sigma}]\cos(2\pi f_0 t) - \frac{Q_{s1}(t)}{\cos\sigma}\sin(2\pi f_0 t + \sigma) \\
&= I_{s1}(t)\cos(2\pi f_0 t) - Q_{s1}(t)\sin(2\pi f_0 t) \\
&= r_{max}\cos[2\pi f_0 t + \frac{\phi(t)}{N} + \frac{\alpha(t)}{N}],
\end{aligned} \tag{3.19}$$

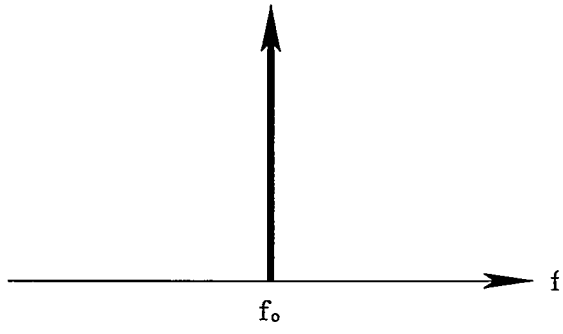
which is the same as the ideal signal at the subharmonic carrier frequency for the upper path of the LINT modulator shown in Equation 2.16.

The phase error of the vector modulator in the lower path of the LINT modulator can be compensated with the same mathematical method.

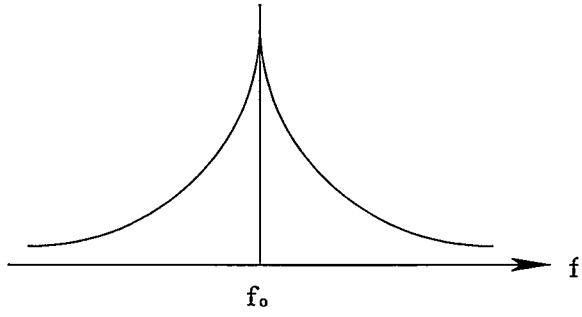
The effect of amplitude imbalance on the combined signal constellation is checked in Chapter 6.

3.3.2 Phase Noise

In the LINT modulator, oscillators are used to generate stable carriers for the vector modulators. For an ideal oscillator operating at f_o, the spectrum is an infinitely narrow line (delta function) as shown in Figure 3.16(a). For an actual oscillator, the spectrum expands around the center frequency f_o as shown in Figure 3.16(b). This is caused by random phase fluctuations in the output signal, which is referred to as phase noise.



(a) Spectrum of ideal oscillator.



(b) Spectrum of actual oscillator.

Figure 3.16 Spectrum of an oscillator.

The source of phase noise in an oscillator is due to thermal and flicker or $1/f$ noise [29]. Many methods are used to measure phase noise [30]. One of the most common fundamental descriptions of phase noise is Single Sideband (SSB) phase noise. Phase noise is usually characterized in the frequency domain. The SSB phase noise is defined as the ratio of power in one phase modulation sideband per Hertz

bandwidth, at an offset Δf Hertz away from the carrier, to the signal power [30], which can be illustrated mathematically as

$$L(\Delta f) = \frac{P_{ssb}}{P_c}, \tag{3.20}$$

where P_c is the carrier power and P_{ssb} is the sideband power in a one Hz bandwidth at an offset frequency of Δf from the center frequency. Figure 3.17 graphically shows the frequency domain representation of SSB phase noise.

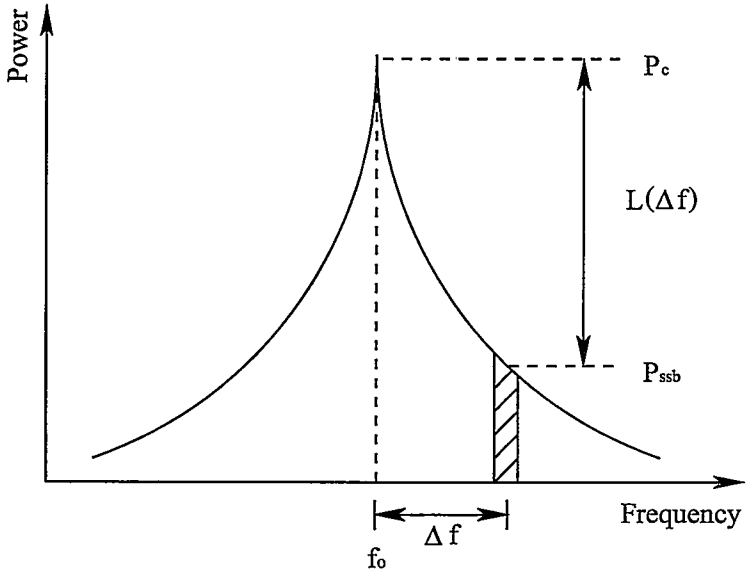


Figure 3.17 SSB phase noise representation.

The SSB phase noise is more useful when expressed in logarithmic form as

$$\begin{aligned} L(\Delta f)\ in\ dB &= 10\ log\frac{P_{ssb}}{P_c} \\ &= 10\ log(P_{ssb}) - 10\ log(P_c). \end{aligned} \tag{3.21}$$

If a carrier with phase noise is modulated by a baseband information sequence, the error rates of digital communication systems will increase [31]. Also phase noise in an oscillator can lead to contamination of adjacent frequency channels.

3.4 Summary

This chapter deals with the LINT modulating signal design and describes some imperfections in the LINT architecture. In this study, 16-QAM modulation is employed for the LINT modulator. This is a digital modulation method, which has higher bandwidth efficiency than other modulation schemes like FSK. In 16-QAM, two bits I and Q components are combined by vector sum to realize 16 unique states in each symbol, allowing transmission of 4 bits per symbol. 16-QAM is a combination of amplitude modulation and phase modulation. For baseband signal generation, the binary data sequence is split into I and Q channels. Then the I and Q binary data are converted to four amplitude levels using Gray coding, and filtered by SRRC filters to eliminate out of band spectrum. Finally, I channel and Q channel data are summed to form the filtered 16-QAM signal, which is employed as the input source signal to the LINT modulator. The validity of the LINT signal separation and scaling algorithm is also tested using MATLAB. Simulation results show that the varying envelope of the 16-QAM signal is decomposed in accordance with the theory described in Section 2.2.2.

The performance of the direct LINT modulator may be degraded by some imperfections. One is the gain and phase imbalance between two paths of multiplier chains and power amplifiers. The second source of imperfections is the quantization errors occurring in the SCS and phase scaler when using a DSP device. The third is the phase error between quadrature components of the vector modulators. The first two problems can be detected and then compensated by varying amplitude and phase delay of input source signal at baseband using a certain algorithm. In theory, the last one can also be solved by adjusting the I and Q components of the baseband source signal .

Chapter 4

MICROWAVE CIRCUIT DESIGN

4.1 Frequency/phase Multiplier

4.1.1 Nonlinear Device

Nonlinear devices are used to achieve the function of frequency/phase multiplication. An input sinusoidal CW signal is distorted using nonlinear devices, resulting in an output signal rich in harmonic frequencies other than the fundamental frequency.

Two terminal passive nonlinear components such as resistive diodes, varactor diodes, and step recovery diodes (SRDs) have been employed as multiplication devices in microwave and millimeter wave multiplier design for some time [32]. Multipliers using such devices have the advantages of high order multiplication and broad bandwidth. The benefits of low noise and operation at millimeter wavelengths are especially attractive in some applications.

Another alternative for multiplication devices is the use of active components such as field effect transistors (FETs). Although active multipliers have a poorer noise performance, their high efficiency offers an advantage over diode multipliers [33]. Because diodes are passive elements, diode frequency multipliers are lossy. In practice, varactor diode multipliers can achieve a conversion efficiency of $1/n$ [32], where n is the harmonic number. For resistive multipliers the situation is even worse. The conversion efficiency for generating the nth harmonic is fundamentally limited to $1/n^2$ [34] [35]. Active multipliers, on the other hand, can provide conversion gain and require small input powers. This characteristic can simplify multiplier chain design significantly. The multiplier chain using passive multiplier

stages needs amplifiers between two adjacent stages to overcome the power losses and supply enough input drive level for the next stage. This results in complex circuitry and extra loss of power. Low order active multipliers can have conversion gain in each stage, so additional amplification is often not required.

With the development of solid state devices, packaged and unpackaged transistors operating at millimeter wave frequencies are commercially available. This makes active frequency multipliers more and more popular in microwave circuit design. Due to the advantages of active multipliers over passive multipliers, a FET multiplier architecture is chosen to provide frequency translation. The theory of FET multiplier design is discussed in the next section.

4.1.2 FET Frequency Multiplier

A simple frequency multiplier can be designed using a single nonlinear FET device to generate harmonics by rectifying the sinusoidal input signal. There are two different bias conditions that support harmonic generation [36]. One is called Class A rectification. It is accomplished by operating the FET in the vicinity of forward conduction threshold so that the gate voltage exceeds the forward conduction and the drain current is clipped. The other is called Class B rectification. This method is accomplished by biasing the FET in the vicinity of or below the pinch-off voltage V_t so that the gate voltage swings below V_t and the drain current is clipped. When biased below V_t, the FET is actually biased at a Class C power amplifier bias point.

The resulting rectified drain current waveform in either case is rich in harmonic components. However, the two types of multipliers have different advantages and disadvantages. Class A type FET multipliers, similar to Class A power amplifiers, can provide good gain performance but poor output power. While Class B type FET multipliers, similar to Class B and Class C power amplifiers, can achieve high output power but poor multiplication gain performance [36]. It is suggested that compared with Class B operation, Class A operation involves higher DC drain current (and thus lower DC to RF efficiencies) as well as a high risk of device failure due to elevated gate current spikes [37]. To achieve maximum reliability, a Class C

bias condition is selected for FET multiplier design.

A simplified circuit of FET frequency multiplier is shown in Figure 4.1 [38]. The circuit contains a FET, an excitation source $V_s(t)$, two bias sources, a tuned circuit and a load impedance R_L . The gate bias voltage V_{gg} is adjusted below pinch-off voltage V_t. The drain bias voltage is V_{dd}. The output resonator is tuned to the nth harmonic of the fundamental excitation frequency f_0, and short circuits the drain at all unwanted harmonics and also the fundamental frequency.

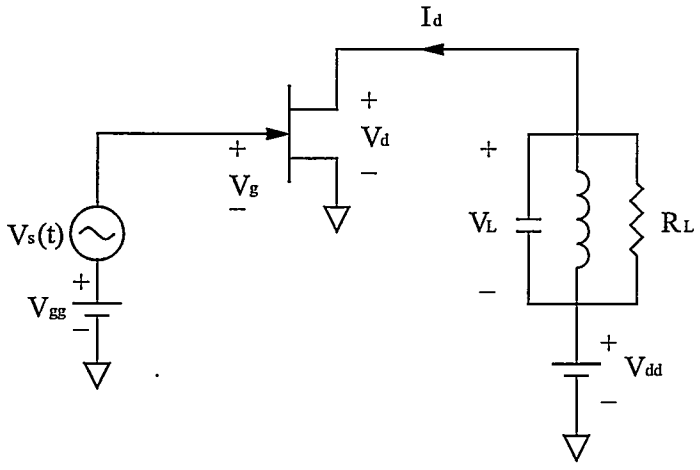


Figure 4.1 Simplified circuit of FET frequency multiplier.

Biased near or below pinch-off voltage V_t, the FET drain conducts only when the gate voltage swings above V_t. Therefore, the drain current only conducts over a part of the excitation cycle. The drain current is a pulse train, which approximates a half-wave rectified cosine wave. The voltage and current waveforms in an ideal x2 FET frequency multiplier are shown in Figure 4.2 [32]. $V_g(t)$ is the waveform of the gate voltage with a maximum voltage of $V_{g,max}$. $I_d(t)$ is the waveform of the drain current with maximum value I_{max} corresponding to the maximum gate voltage $V_{g,max}$. $V_d(t)$ is the drain voltage assuming that the 2nd harmonic is selected. Since the output resonator short circuits all other harmonic and fundamental components, $V_d(t)$ is a sinusoidal waveform having frequency of $2f_0$.

The rectified cosine shape drain current is rich in harmonic frequencies, which can be exhibited by its Fourier series representation [38]

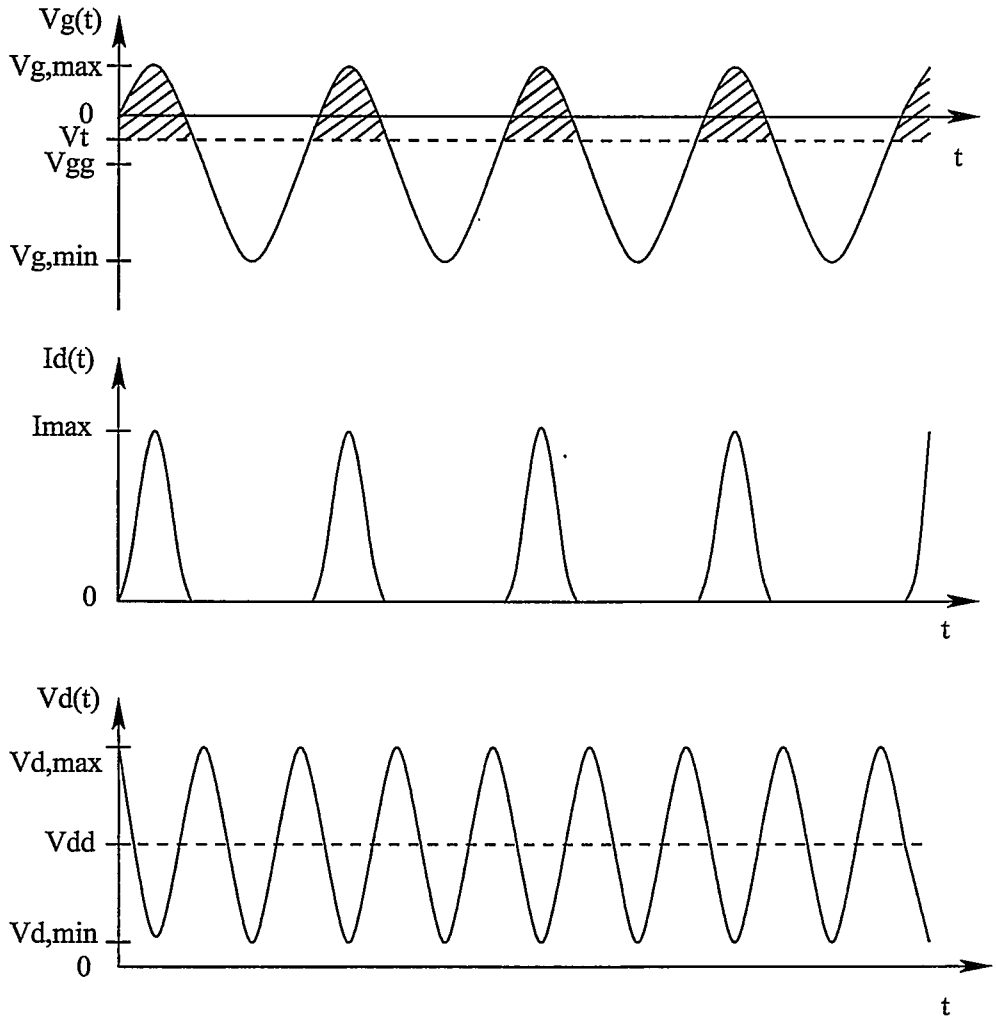


Figure 4.2 Voltage and current waveforms for an ideal x2 FET multiplier .

$$I_d(t) = I_{dc} + \sum I_n \cos(n2\pi f_0 t), \tag{4.1}$$

where I_{dc} is DC drain current, I_n is the drain current for the nth harmonic. The coefficients can be calculated by [38]

$$I_{dc} = I_{max}\frac{2t_0}{\pi T}, \tag{4.2}$$

$$I_n = I_{max}\frac{4t_0}{\pi T}\left|\frac{\cos(n\pi t_0/T)}{1-(2nt_0/T)^2}\right|, \tag{4.3}$$

where T is the period of the fundamental excitation, t_0 is the length of the drain current pulse, and t_0/T is the duty cycle, which is the conduction fraction of the input period. The duty cycle represented in phase, $2\pi\frac{t_0}{T}$, is called the conduction angle. A plot that relates the ratio of harmonic drain current I_n and maximum drain current I_{max} as a function of duty cycle t_0/T from the 2nd harmonic to the 6th harmonic is shown in Figure 4.3.

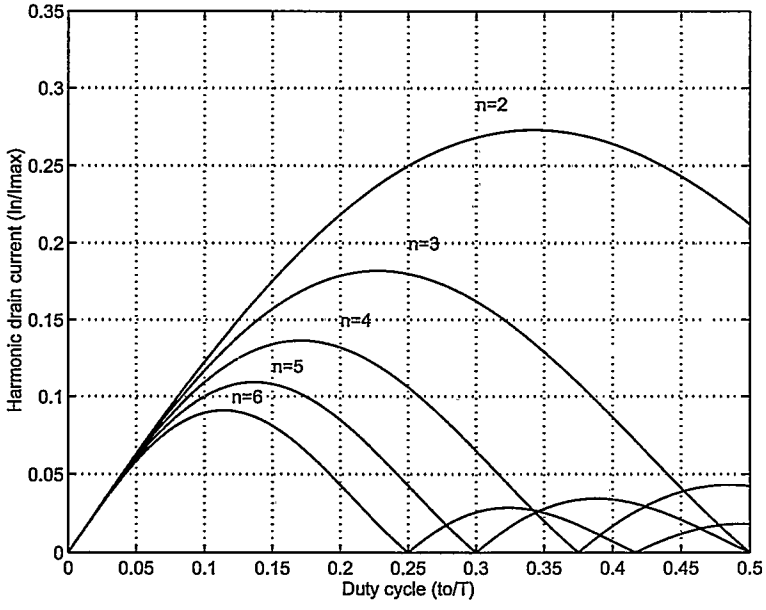


Figure 4.3 Ideal harmonic drain current components of $I_d(t)$ as a function of duty cycle.

In order to get the maximum output power at the desired nth harmonic, I_n must be maximized. Equation 4.3 shows that, to maximize I_n, the maximum drain

current must be kept as high as possible. That requires that the corresponding maximum gate voltage must also be as high as possible. So the only remaining degree of freedom to maximize I_n is to change the duty cycle t_0/T to its optimum value. Figure 4.3 shows that each order of harmonic current corresponds to an unique duty cycle, and as the order of harmonic increases, the value of optimum duty cycle decreases. The small duty cycle can be achieved by decreasing the DC gate bias voltage V_{gg}. As the gate bias is lowered, the level of input excitation must be increased to maintain the maximum drain current at I_{max}. As the duty cycle continues to decrease in this manner, the negative peak of the gate voltage will exceed the gate breakdown voltage of the FET, and can also cause instability [23]. This is the reason that a non-optimal conduction angle is often chosen for higher order FET frequency multiplier design.

Assuming that a perfect output resonator is included in the multiplier circuit (see Figure 4.1), the voltage across the load resistance R_L can be expressed as [38]

$$|V_L(t)| = I_n R_L = \frac{(V_{d,max} - V_{d,min})}{2}, \tag{4.4}$$

where I_n is the nth harmonic current in the load resistance R_L and is given by Equation 4.3. $V_{d,max}$ and $V_{d,min}$ are the maximum and minimum drain voltages shown in Figure 4.2. To maximize the power delivered to R_L, the drain voltage is required to have its maximum variation. To meet this requirement, the minimum drain voltage should equal to the lowest value permitted by the FET I-V curve, which corresponds to the I-V "knee" voltage.

From Equation 4.4, the optimal load resistance can be calculated by

$$R_L = \frac{(V_{d,max} - V_{d,min})}{2I_n}. \tag{4.5}$$

For high order frequency multipliers, the drain harmonic current is small. Therefore, quite a large load resistance is required by Equation 4.5 to provide the maximum load voltage excursion. This load resistance could be impractically large for

impedance matching in microwave circuit design.

An active frequency multiplier consists of an active nonlinear device (FET), input and output termination circuitry as shown in Figure 4.4. The gate bias voltage and the input signal level are selected to obtain a conduction angle, with which maximum output level at the desired harmonic can be provided. The input termination circuitry translates the generator impedance Z_1 (usually 50 Ω) to the conjugate of the impedance looking towards the FET gate at the fundamental frequency. The output termination circuitry transforms the impedance Z_2 (usually 50 Ω) to the optimum load impedance Z_L at the drain at the desired harmonic frequency. A narrow bandwidth bandpass filter is included in the output matching circuitry to perform the function of harmonic selection as well as impedance matching. It passes the desired harmonic component while rejecting the fundamental and all unwanted harmonic components.

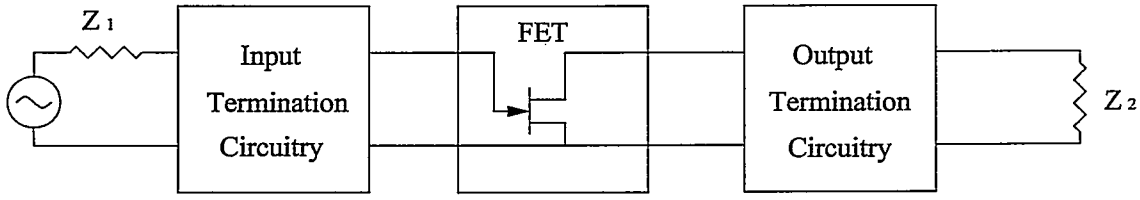


Figure 4.4 Functional block diagram of a frequency/phase multiplier.

The highest multiplication factor of a one-stage active frequency multiplier using a single active nonlinear device reported so far is 7 [33]. When higher multiplication factors are needed, a multiplier chain consisting of two or more stages can be used. It is best to avoid the use of high harmonic stages in frequency multiplier chains because the output levels of high harmonic multipliers may not be high enough to drive the next stage and so amplification may be needed.

4.2 Harmonic Balance Analysis

The input power levels for nonlinear circuits such as power amplifiers or frequency multipliers are generally large enough to violate the small signal approximations of a nonlinear device. Therefore, accurate analysis of a nonlinear circuit

requires a numerical solution of the nonlinear device model equations. Harmonic Balance analysis is one of the most important techniques for analyzing nonlinear circuits, and is used as the nonlinear simulation method by many RF and microwave design software systems such as Advanced Design System (ADS) and Series IV [39]. Harmonic Balance analysis is applicable for circuits containing both linear and nonlinear elements excited by large signal periodic sources [39]. It is most useful for strongly nonlinear circuits that have single-tone excitation [38], such as the multipliers presented in this thesis.

The Harmonic Balance method is based on the assumption that for a given sinusoidal excitation there exists a steady-state solution that can be approximated to satisfactory accuracy by means of a finite Fourier series. Because the transistors are nonlinear, they are best described by lumped element models in the time domain. On the other hand, all the linear coupling, filtering and matching networks necessary in the nonlinear circuits are best described in the frequency domain. So elements in a general nonlinear two-port microwave circuit can be grouped to a linear subcircuit and a nonlinear subcircuit containing a number of nonlinear elements. The circuit port voltages can be represented by a set of amplitudes and phases for all frequency components. If the frequency domain port voltages are known, the currents flowing from the ports into the linear subcircuit can be found by a frequency domain linear analysis using Y-parameters, S-parameters or some other matrix. Inverse-Fourier transforming the port voltages in the frequency domain gives the time domain voltage waveform at each port, because the frequency components and time waveforms are related to each other by the Fourier transform. The time domain currents from the ports into the nonlinear subcircuit can be determined using the port voltages in the time domain and the nonlinear I-V model relationships. According to Kirchoff's Current Law (KCL), I_k, which represents the phasor quantity of the kth harmonic component of the current calculated via the port voltages and the Y-parameters of the linear subcircuit, and $\hat{I}_k$, which is the current component calculated via the same port voltages and the nonlinear elements, should sum to zero at all ports. The idea of Harmonic Balance is to find

such a set of port voltage waveforms, or the harmonic voltage components, that give the currents with the same value but in opposite direction in both the linear network equations and the nonlinear network equations. When this set is found, it must be the steady state solution.

Because of the nonlinear elements in the circuit, the port voltages and currents must have frequency components at harmonics of the excitation. Although in theory an infinite number of harmonics exists at each port, it is desirable to select a moderate number of harmonics and ignore all higher order of harmonics, because the number of harmonic frequencies applied to a network considerably affects the required memory and simulation time. The steady state solution is obtained by comparing the currents into the linear subcircuit I_k with the currents into the nonlinear subcircuit $\hat{I}_k$ at each port for all selected number of harmonics. An error function is formulated by calculating the sum of currents at all ports. This error function is a measure of the amount by which KCL is violated. If the error is within tolerance, then convergence is achieved and the resulting amplitudes and phases approximate the steady state solution. If not, a set of new voltages is determined based on the previous values to reduce the error function. The Harmonic Balance analysis is run iteratively and the port voltage amplitudes and phases are adjusted until convergence to a solution is obtained for all harmonic frequencies.

4.3 Summary

This chapter describes theoretical and practical considerations in FET frequency multiplier design. A frequency multiplier translates the input signal at the fundamental frequency to an output signal at the nth harmonic of the fundamental frequency. The FET multiplier is biased in Class C mode to obtain an appropriate conduction angle conducive to high nth harmonic output. The input termination circuitry transforms the 50 Ω generator resistance to the conjugate of the impedance looking towards the FET gate at the fundamental frequency. The output termination circuitry transforms the 50 Ω resistance to the optimum load impedance at the drain at the desired harmonic frequency. A BPF is included in the output termi-

nation circuitry to suppress the unwanted harmonic and fundamental frequencies while allowing the selected nth harmonic component to circulate in the load. A simulation technique for nonlinear circuits such as frequency multipliers and power amplifiers known as Harmonic Balance analysis is also presented in this chapter. With this method, the circuit is divided into linear and nonlinear subcircuit multiport networks. Each element in the nonlinear subcircuit is connected to a port in the linear subcircuit. The linear subcircuit is analyzed in frequency domain while the nonlinear subcircuit is analyzed in time domain. The solutions in time domain and frequency domain are related by the Fourier transform. If a set of port voltages at the harmonics designated by the simulator gives the same solution in frequency domain as that in time domain within acceptable error, then these voltages approximate the steady state solution.

The realization of FET frequency multipliers as the extension on these design equations is presented in the next chapter.

Chapter 5

CIRCUIT REALIZATION

5.1 Fabrication Technology

5.1.1 Microwave Integrated Circuits

Hybrid microwave integrated circuits (MICs) were first developed in the 1960s [25]. With MICs, all the circuit components are connected to each other and manufactured in a planar form, as opposed to fabricating the circuits separately and connecting them together using coaxial lines or waveguides [40]. The MIC technology results in considerable reduction in size, weight, and cost of the functional circuits. The technology offers the advantage of combining multicircuit functions without interconnecting wires, thus permitting compact integrated modules with highly reliable performance. Hybrid MICs typically have one layer of metallization for transmission lines, which have the general name of planar lines. "Microstrip" transmission line is a widely used planar type in hybrid MIC design. The microstrip line consists of a strip conductor on a flat dielectric substrate, the reverse side of which is metallized to provide a ground plane. Discrete components such as capacitors and transistors can be connected to the transmission lines by means of soldering, gluing, or wire bonding.

Monolithic microwave integrated circuits (MMICs) have a much higher degree of miniaturization and integration. In MMICs, all passive and active circuit elements and all connections between them are constructed on a semiconductor substrate. MMICs contain no hybrid elements and no connections such as bonding wires, soldering, or gluing. The circuit tuning after fabrication is difficult, if not impossible. The MMICs can be made at low cost when manufactured in large quantities, but

the fabrication process is very expensive when the circuits are made in small quantities. The microwave circuits presented in this thesis are designed using hybrid MIC technology, but it is expected that similar results could be obtained using MMIC technique.

5.1.2 Substrate

Substrates are the supporting material upon which the conductors and the hybrid elements are built to produce the required circuit. In choosing substrates, general characteristics such as relative permittivity, loss factor, substrate surface roughness, thermal conductivity, and cost are important considerations. Two basic types of substrate are used for hybrid MICs - "hard" substrates and "soft" substrates.

In the hard substrates category, aluminum-oxide ceramic (Al_2O_3), which is also called "alumina", is common in microwave technology. It is a moderately expensive substrate but still the least expensive of the hard substrates. Alumina has a high relative permittivity, usually 9 to 10, which results in a smaller circuit size and higher levels of circuit integration. Alumina also has low loss factor and surface roughness, which decreases the dielectric losses and conductor losses of the MICs. The thermal conductivity of alumina is relatively high, which allows larger heat dissipation from components (e.g., power transistors). The disadvantage of using alumina is the high cost in circuit fabrication. The conductors on the substrate are produced using expensive thin-film technology. This technology requires a great investment in complex production equipment. Alumina is also very hard and brittle, and is difficult to machine. Cuts can be made with a diamond saw or a laser; holes can be drilled with a laser or a carbide tool.

Soft substrates are available in a wide range of relative permittivities depending on material. The substrate materials can be pure plastics or plastics loaded with glass fibers or ceramic powder. Soft substrates usually use copper for their conductors. The laminates are copper-coated on both sides. The copper layer is usually fabricated either by rolling or electro-chemical deposition. Soft substrates provide

the simplest method of producing MICs. All that is required is a high resolution photoetching system to permit structure fabrication on the copper-clad laminates. Soft substrates are also easy to machine. Except for relative permittivity, which can be made as high as that of alumina, other charateristics such as loss factor, the substrate surface roughness and thermal conductivity are worse than those of alumina, but still acceptable for many applications. The advantage of using soft substrates is that the cost for MIC fabrication is very low, because the circuits can be made in the laboratory without the need for complex technological equipment.

Despite its inferior properties at high microwave frequencies, soft substrate is chosen as the material for circuit implementation due to its simple form and low cost for fabrication. The selected substrate is RT/duroid^{TM} 6010, which is a ceramic powder-filled polytetrafluorethylene (PTFE) composite with a high relative permittivity $\epsilon_r = 10.8$, substrate thickness of 25 mil, and copper conductor thickness of 0.7 mil. The various microstrip transmission line parameters corresponding to the physical parameters of the substrate can be calculated using the Series IV LineCalc program [39]. The width of a 50 Ω microstrip line is 28 mil. The length of a $\lambda/4$ transmission line ($\pi/2$ radian electrical length) is 478 mil at frequency of 2.33 GHz, 157 mil at 7 GHz, and 36 mil at 28 GHz.

5.2 Transistor Selection

The first step in circuit design is to select a transistor device suitable for multiplier implementation. The transistor must have high frequency performance in excess of 28 GHz, because that is the output frequency of the second stage multiplier. The multipliers are in "strong" Class C operation. To get a conduction angle less than 180°, a large gate voltage excursion is required, as described in Section 4.1.2. The reverse magnitude of the gate voltage could be very large. It is desirable that the selected transistor has a high gate breakdown voltage to withstand the large gate voltage. In order to obtain a high output power for the desired harmonic frequency of a multiplier, the peak drain current must be quite large. Therefore, a transistor with a high saturated drain-source current is required.

Small signal FETs are usually designed for applications requiring small signal excitation. Therefore, small signal devices have relatively low gate breakdown voltage and small saturated drain current. For this reason, small signal FETs are not suitable for multiplier applications. Power FETs, however, are designed to withstand higher gate voltage and drain current, and therefore, are suitable for multiplier applications. The NE1280400 medium power FET chip manufactured by NEC is selected for multiplier implementation. It has an operating frequency up to 40 GHz, which is larger than the operating frequency of 28 GHz required by the multipliers presented in this thesis. The maximum gate to source breakdown voltage rating is $-5\ V$. The typical saturated drain current is as high as 700 mA at $V_{ds} = 1.5\ V$ and $V_{gs} = 0\ V$. The detailed characteristics of the device can be found in Appendix A. The NE1280400 is an "unpackaged" chip device. Therefore, there is no parasitic capacitance and inductance related to the package, which makes the chip device easier to match at the drain for high performance operation. The only parasitic reactance is the inductance of the bond wires required to connect the chip to the circuit.

5.3 x4 Multiplier Design

In this section, design procedures for x4 multipliers are presented. Initially, simplified multiplier circuits with ideal capacitors and simplified chokes are investigated to simplify the design process. Then, the complete multiplier circuitry suitable for practical implementation is designed. The complete design employs the critical performance parameters derived from the simplified design, and is performed by replacing the ideal components with practical ones, which makes the design procedure simpler. The performance results for the simplified and complete circuits are presented in Chapter 6.

5.3.1 Basic Design

The simplified circuitry employs ideal capacitors and simplified chokes. Ideal capacitors do not have unwanted inductance, resistance, and dielectric absorption. The impedance of an ideal capacitor decreases linearly with increasing frequency.

There is no power loss in an ideal capacitor. The simplified chokes provide harmonic termination and DC passage without practical consideration.

Biasing

The conduction angle to achieve the maximum 4th harmonic drain current is 61.2° (see Figure 4.3). However, this optimal conduction angle is too small to be obtained due to the considerations of gate-source breakdown voltage and circuit stability, as described in Section 4.1.2. Therefore, a conduction angle bigger than the optimal one has to be chosen. A reasonable conduction angle in the vicinity of 110° is selected for x4 multiplier design. The 5th harmonic drain current at this conduction angle is zero.

The desired conduction angle is provided by carefully selecting the gate signal level and bias voltage. For an ideal sinusoidal drain current pulse, the conduction angle can be calculated by [38]

$$\theta_t = 2\arccos\left(\frac{2V_t - V_{g,max} - V_{g,min}}{V_{g,max} - V_{g,min}}\right). \tag{5.1}$$

For the NE1280400, the pinch-off voltage, V_t, is $-1.6\ V$, and maximum gate breakdown voltage is $-5\ V$. From Equation 5.1, a conduction angle of 113° is obtained with $V_{g,max} = -0.6\ V$ and $V_{g,min}$ reaches the gate breakdown voltage of $-5\ V$. The resultant gate bias voltage is $V_{gg} = \frac{V_{g,max}+V_{g,min}}{2} = -2.8\ V$. A drain bias voltage of $V_{dd} = 4\ V$ is chosen. Assuming that the drain is forced to saturation at "knee" voltage of $1\ V$, this bias point provides a maximum drain voltage of $V_{d,max} = 7\ V$.

Output Circuitry

The output circuitry of a x4 multiplier is designed to provide maximum 4th harmonic output power to the load impedance. The fundamental frequency component and all other harmonics are rejected. This is accomplished by terminating the drain at the 4th harmonic frequency with an appropriate impedance, while short circuiting the drain at the fundamental and all other harmonics. Only the 4th harmonic voltage exists at the drain, and the voltage at the fundamental frequency and un-

wanted harmonics is zero. Thus, only the 4th harmonic voltage contributes to the output power.

It is assumed previously that the optimal drain termination of FETs is short circuits at the fundamental frequency and unwanted harmonics. A comparison was made using short circuit and open circuit drain terminations at the fundamental excitation frequency for a 20 - 40 GHz doubler [36]. It is suggested that multipliers having an open circuit drain termination at the fundamental frequency provide high gain and moderate power, whereas multipliers having a short circuit drain termination at fundamental frequency provide lower gain but better output power. With open circuit terminations at the drain, the fundamental drain current is zero, but the fundamental drain voltage might be large. With the high reverse peak gate voltage, the drain-gate voltage swing could be very big, and exceed the drain-gate avalanche voltage of the FET. The increase in gain for multipliers with open circuit drain terminations is usually the result of internal feedback [38]. Feedback is likely to have a deleterious effect on the multiplier's stability. Due to this disadvantage of open circuit drain terminations, short circuit terminations are selected for multiplier realization.

Series IV Harmonic Balance analysis has a powerful function of terminating each of the output harmonics with a desired load impedance independently without interfering with one another. Therefore, each harmonic can be ideally terminated with a reflection coefficient of any desired value. For the multiplier in this thesis, the drain of the NE1280400 is first short circuited at the fundamental frequency and all harmonics in order to select an appropriate input level to provide the desired conduction angle. The FET is terminated with a voltage reflection coefficient of $\Gamma_n = 1\angle 180°$, which corresponds to ideal short circuit termination, at all harmonics. No input matching and output matching circuitry is initially employed. The input power level is increased while keeping the gate voltage excursion within the gate-source breakdown voltage of $-5\ V$.

The time waveform of gate voltage is shown in Figure 5.1. It can be seen from this figure the conduction angle is approximately 96° instead of the desired

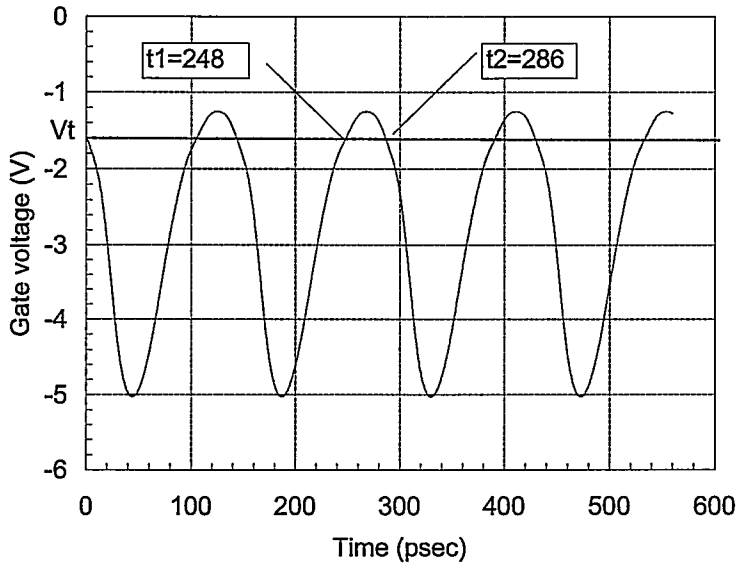


Figure 5.1 Time waveform of the NE1280400 gate voltage with ideal short circuit drain termination for x4 multiplier.

conduction angle of 113° as calculated using Equation 5.1, and the peak gate voltage does not reach the value of $-0.6\ V$ as expected. Some difference between the theoretical analysis results and simulation results lies in the fact that for a real FET there exists internal feedback. In the theoretical analysis, the FET is treated as an ideal component without feedback effects and parasitic components. In a real circuit, the gate voltage is not a pure sinusoidal waveform due to the feedback.

Table 5.1 shows the ratio of harmonic drain current components to the peak drain current at harmonics from fundamental frequency up to the 5th harmonic using Harmonic Balance analysis. Table 5.1 also shows the ideal harmonic drain current components relative to the peak drain current at a conduction angle of 96°, as calculated with Equation 4.3 using an ideal sinusoidal drain pulse. The simulated magnitudes of drain current components for NE1280400 with ideal short circuit terminations are close to the calculated results using ideal sinusoidal drain pulse with a conduction angle of 96°. This confirms that the drain bias voltage and the input power level were selected to provide a conduction angle of approximate 96°.

Table 5.1 Harmonic drain current components for NE1280400 with ideal short circuit drain terminations for x4 multiplier.

Number of harmonics (n)	Frequency (GHz)	Calculation result	Simulation result
		$\frac{I_n}{I_{d,max}}$	$\frac{I_n}{I_{d,max}}$
1	7	0.32	0.31
2	14	0.26	0.22
3	21	0.17	0.16
4	28	0.09	0.09
5	35	0.02	0.02

The next step is to find the optimal load impedance, with which the maximum output power can be obtained. In order to maximize the 4th harmonic output power at 28 GHz, the drain termination should be designed to resonate the FET drain capacitance at the 4th harmonic frequency and provide a real load impedance to the drain. Therefore, an inductive susceptance equal to the drain capacitive susceptance is required to be connected in parallel with the drain. This inductive reactance and the load resistance connected in parallel provide the ideal load impedance for the output circuitry. With the conduction angle of 96°, the 4th harmonic current is 9% of the peak drain current, which is 205 mA under the gate voltage excitation shown in Figure 5.1. The optimal 4th harmonic load resistance calculated using Equation 4.5 is 162 Ω. Assuming that the drain capacitance is 0.5 pF, the estimated load impedance at 28 GHz is Z_L (28 GHz) = $(0.8 + j11.3)$ Ω. The corresponding voltage reflection coefficient is Γ_L (28 GHz) = $0.97\angle 154°$. This estimated value is used as a starting point for Harmonic Balance analysis. The drain is terminated with this reflection coefficient at the 4th harmonic, while the other harmonics remain short circuit terminated with $\Gamma_n = 1\angle 180°$. The Harmonic Balance analysis is run with the optimization goal set to maximize the 4th harmonic output power level at 28 GHz. The optimized reflection coefficient for 4th harmonic is $\Gamma_4 = 0.81\angle 164°$, which gives a load impedance of 11 Ω inductive reactance in parallel with 15 Ω resistance. The optimized load resistance of 15 Ω is much smaller than the expected

value of 162 Ω. The possible reason for the inconsistency betweeb the optimized and theoretical results are discussed in Chapter 7.

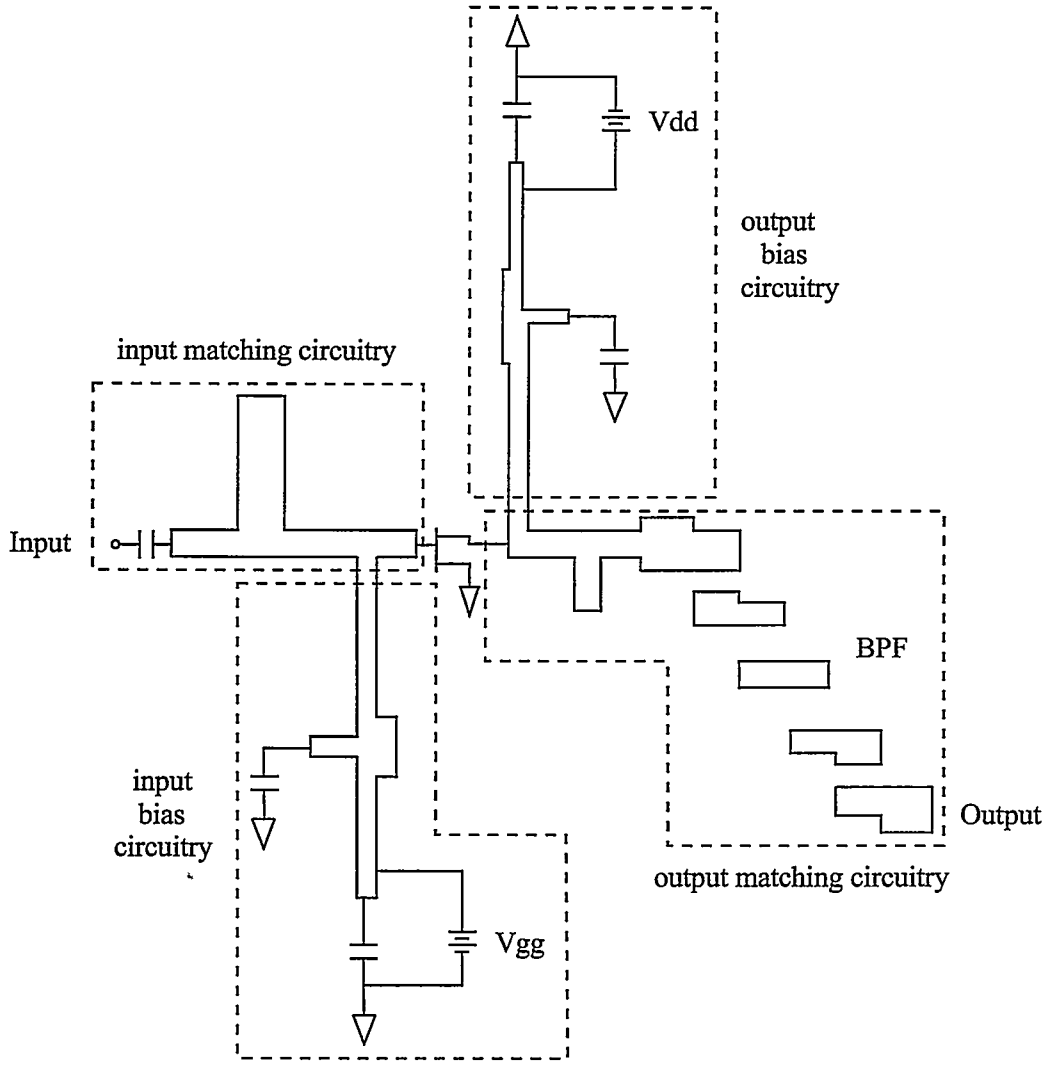


Figure 5.2 Layout for simplified x4 multiplier.

Next the output matching circuitry and output bias circuitry are designed to transform the 50 Ω load to the optimized 4th harmonic load impedance, while terminating the fundamental frequency and other harmonics in short circuits at the drain. Providing good short circuit drain terminations at the fundamental frequency and the 2nd harmonic is more important than the 3rd harmonic, because the drain currents at these two frequencies are very high. The structure of the output matching circuitry and bias circuitry is shown in Figure 5.2, which is the

layout for the x4 multiplier. A coupled line BPF is included in the output circuitry to suppress unwanted harmonic output. A coupled line filter at the output can also provide DC blocking from the drain bias, so no DC blocking capacitor, which is difficult to obtain at frequency as high as 28 GHz, is needed. A simple 3rd order coupled line filter can provide adequate rejection at unwanted harmonics. The filter is designed using the 3rd order Butterworth low pass filter prototype. For a filter with order of $N = 3$, the element values are $g_1 = g_3 = g_4 = 1$ and $g_2 = 2$ [25]. The design equations for the filter with four sections of $\lambda/4$ coupled lines are [25]

$$Z_0 J_1 = \sqrt{\frac{\pi\Delta}{2g_1}}, \tag{5.2}$$

$$Z_0 J_n = \frac{\pi\Delta}{2\sqrt{g_{n-1}g_n}}, \quad n = 2, 3, \ldots, N, \tag{5.3}$$

$$Z_0 J_{N+1} = \sqrt{\frac{\pi\Delta}{2g_N g_{N+1}}}, \tag{5.4}$$

where Δ is the fractional bandwidth relative to the center frequency of the filter.

The even and odd mode line impedances for the nth coupled line are

$$Z_{0e} = Z_0[1 + J_n Z_0 + (J_n Z_0)^2], \tag{5.5}$$

$$Z_{0o} = Z_0[1 - J_n Z_0 + (J_n Z_0)^2]. \tag{5.6}$$

Using Equations 5.2 to 5.6, the even and odd mode characteristic impedances can be calculated for a 3rd order coupled line filter with 10% bandwidth. The results are summarized in Table 5.2.

Table 5.2 Calculation results for 3rd order Butterworth coupled line filter.

n	g_n	$J_n Z_0$	$Z_{0e}(\Omega)$	$Z_{0o}(\Omega)$
1	1	0.3962	77.66	38.04
2	2	0.1110	56.17	45.07
3	1	0.1110	56.17	45.07
4	1	0.3962	76.66	38.04

The dimensions of the four sections of coupled lines can be obtained using Series

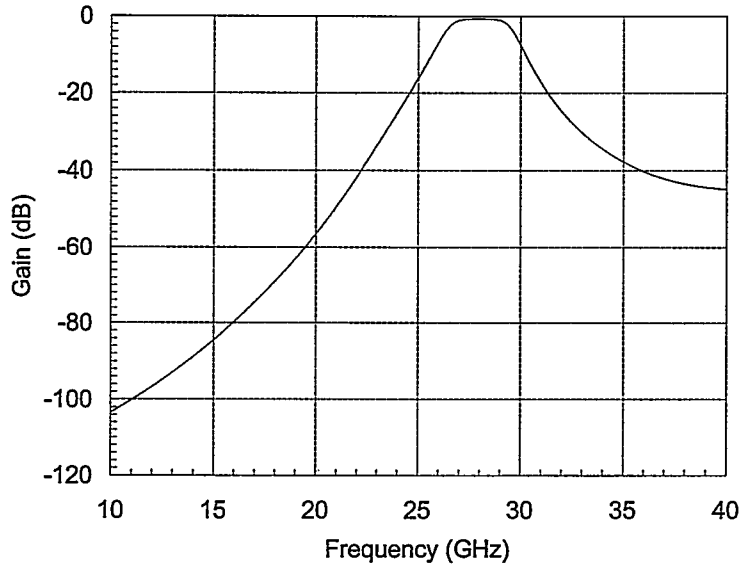


Figure 5.3 Amplitude response of 28 GHz 3rd order coupled line bandpass filter.

IV LineCalc program based on the calculated even mode and odd mode impedances. These coupled line dimensions are used as a starting point for optimization of the filter. The simulated filter amplitude response as a function of frequency is shown in Figure 5.3. The return loss of the filter, which is defined (in dB) as

$$RL = -20 \log |\Gamma| \text{ dB}, \tag{5.7}$$

is shown in Figure 5.4. From these two figures, it is apparent that the filter is matched well at 28 GHz, as the return loss at this frequency is high and the amplitude is approximate unity. The filter also shows a good performance of rejection at the fundamental and harmonic frequencies, with 89 dB amplitude attenuation at 14 GHz, and 49 dB amplitude attenuation at 21 GHz.

From Figure 5.4, the magnitude of voltage reflection coefficients for harmonics other than the 4th harmonic of 28 GHz is near 1, as the return loss at those harmonics is almost 0 dB. The input impedance of the filter at these harmonics is reactive. On the other hand, the impedance at the 4th harmonic of the fundamental frequency is near 50 Ω, since the voltage reflection coefficient is almost zero at this

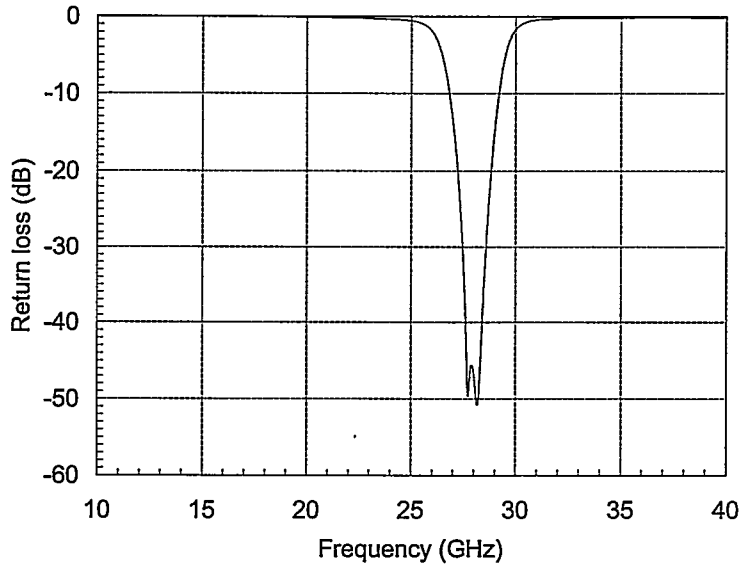


Figure 5.4 Return loss of 28 GHz 3rd order coupled line band-pass filter.

frequency. Therefore, a section of 50 Ω transmission line can effectively transform the reactive impedance at the 2nd harmonic frequency to a short circuit at the drain, while maintaining the 50 Ω impedance at 28 GHz.

The short circuits for the fundamental and 3rd harmonic frequencies at the drain are provided by the output bias circuitry shown in Figure 5.2. It consists of transmission lines, an open circuit stub, and a short circuit stub, which is realized by connecting the transmission line to the ground through a 10 pF capacitor. The DC drain bias voltage is supplied through a 5 pF capacitor. The whole output bias circuitry is designed to provide short circuits at the fundamental and 3rd harmonic frequencies, and open circuits at the 2nd and 4th harmonic frequencies. The voltage reflection coefficients of the output bias circuitry and the output matching circuitry at the drain for the first four harmonic frequencies are shown in Table 5.3. From Table 5.3, it is apparent that the output bias circuitry provides good short circuits at odd harmonics and open circuits at even harmonics.

The short circuit at the 2nd harmonic frequency and transformation of the 50 Ω load impedance to the optimal voltage reflection coefficient of $\Gamma_4 = 0.81\angle 164°$ at the 4th harmonic frequency is accomplished by the output matching circuitry. Af-

Table 5.3 Voltage reflection coefficients of the output bias circuitry and output termination circuitry for simplified x4 multiplier.

Number of harmonics (n)	Frequency GHz	Γ_{bias}	Γ_{output}
1	7	$0.99\angle 166°$	$0.99\angle 175°$
2	14	$0.95\angle -0.8°$	$0.98\angle -177°$
3	21	$0.99\angle 173°$	$0.95\angle 177°$
4	28	$0.90\angle 0.51°$	$0.81\angle 164°$

ter optimization, the voltage reflection coefficient is approximately short circuits at harmonics lower than the 4th harmonic, and is the desired value of $\Gamma_4 = 0.81\angle 164°$ at the 4th harmonic frequency, as shown in Table 5.3. Table 5.4 shows the harmonic current components at the drain for the NE1280400 with output termination circuitry, which are comparable to those with ideal short circuit terminations shown in Table 5.1. Table 5.4 also shows the root mean square (rms) values of harmonic voltage components at the NE1280400 drain with output termination circuitry. The harmonic voltage levels at the drain are smaller than the voltage at the 4th harmonic, which indicates that the output termination circuitry short circuits the drain at unwanted harmonics.

Table 5.4 Harmonic drain current and voltage components for NE1280400 with output termination circuitry for simplified x4 multiplier.

Number of harmonics (n)	Frequency GHz	$\frac{I_n}{I_{d,max}}$	$\lvert V_{ds,n}\rvert(V_{rms})$
1	7	0.31	0.06
2	14	0.22	0.04
3	21	0.15	0.02
4	28	0.08	0.10

The next step is to design the multiplier input circuitry, which will be discussed next.

Input Circuitry

After the output termination circuitry is optimized, the next step is to find the optimal source impedance for the terminated FET, which is the conjugate match of the gate impedance at the fundamental frequency of 7 GHz. The large signal S-parameters of the FET with the output termination circuitry can be extracted using the Harmonic Balance method in Series IV. The input level is set to provide the desired peak gate voltage as shown in Figure 5.1 with output termination circuitry. This ensures that the right conduction angle of 96° is obtained. It is very important to set the input power to the level with which the peak gate voltage can be obtained in the measurement of large signal S-parameters, because the input impedance is the function of input level. With this method, the measured large signal input impedance of the terminated FET at the fundamental excitation frequency of 7 GHz is $Z_{in} = (13.3 - j61.1)\ \Omega$. Thus, the optimal source impedance is $Z_s = (13.3 + j61.1)\ \Omega$, which is a conjugate match of the gate input impedance.

The 50 Ω source impedance is transformed to the conjugate matched source impedance, Z_s, using microstrip transmission lines. The input circuitry is designed to perform this task and includes the input matching circuitry and input bias circuitry, as shown in Figure 5.2. The input matching circuitry transforms the input impedance of $Z_{in} = (13.3 - j61.1)\ \Omega$ to the 50 Ω source impedance at 7 GHz. A 2.2 pF capacitor is included to provide DC blocking at the gate. The input bias circuitry is similar to the output biasing circuitry. It provides high impedance at the fundamental frequency and odd harmonics and low impedance at even harmonics of the fundamental input frequency. The input matching circuitry is optimized to provide good input match at 7 GHz, while maintaining maximum power to the 50 Ω load. The input power to the x4 multiplier is selected to provide the desired peak gate voltage, and is 5 dBm when the whole circuit is optimized.

The last step is to check stability. The multiplier with input and output circuitry can be treated as a two-port network. The large signal S-parameters can be extracted using Series IV. The two-port network is said to be unconditionally stable if it is stable for all passive load and source impedances. The necessary and

sufficient conditions for unconditional stability are that $K > 1$ and $B_1 > 0$ [41], where K and B_1 are the stability factors and are functions of the S-parameters of the two-port network. The stability analysis is performed at the fundamental input frequency and all major harmonic frequencies, and the conditions for unconditional stability are met at these frequencies.

5.3.2 Practical Implementation Considerations

In theory, the impedance of an ideal capacitor is purely reactive. However, a real capacitor will exhibit some resistance due to its parasitic elements, and thus is a lossy component. A capacitor's power dissipation is inversely proportional to its quality factor. The lower the capacitor's quality factor, the greater its loss. Therefore, low loss high quality factor capacitors are desirable in such applications as bypass, DC blocking and circuit matching. The size of capacitors is another major consideration in their selection. In microwave circuits design, all lumped elements are required to have a length much smaller than the wavelength at the operating frequency. The "600s Series" chip capacitors manufactured by American Technical Ceramics (ATC) satisfy the requirements mentioned above, and are selected for practical circuit realization.

The layout of the x4 multiplier is shown in Figure 5.5, and also drawn to scale in Appendix Figure B.1. The bandpass filter in the output matching circuitry is a 2nd order coupled line filter, instead of a 3rd order filter in the simplified x4 multiplier presented in Section 5.3.1. Since the simplified x4 multiplier with 3rd order filter exhibits very good performance on harmonic rejection with the levels of unwanted harmonic components below 55 dBc as shown in Figure 6.2, a 2nd order filter will be enough for harmonic suppression purpose.

The 2nd order coupled line filter still employs Butterworth low pass filter prototype with element values $g_3 = 1$ and $g_1 = g_2 = \sqrt{2}$ [25]. The bandwidth of the filter is $\Delta = 10\%$. The filter parameters can be calculated using Equations 5.2 to 5.6. The results are summarized in Table 5.5.

The dimensions of the three coupled line sections obtained using Series IV

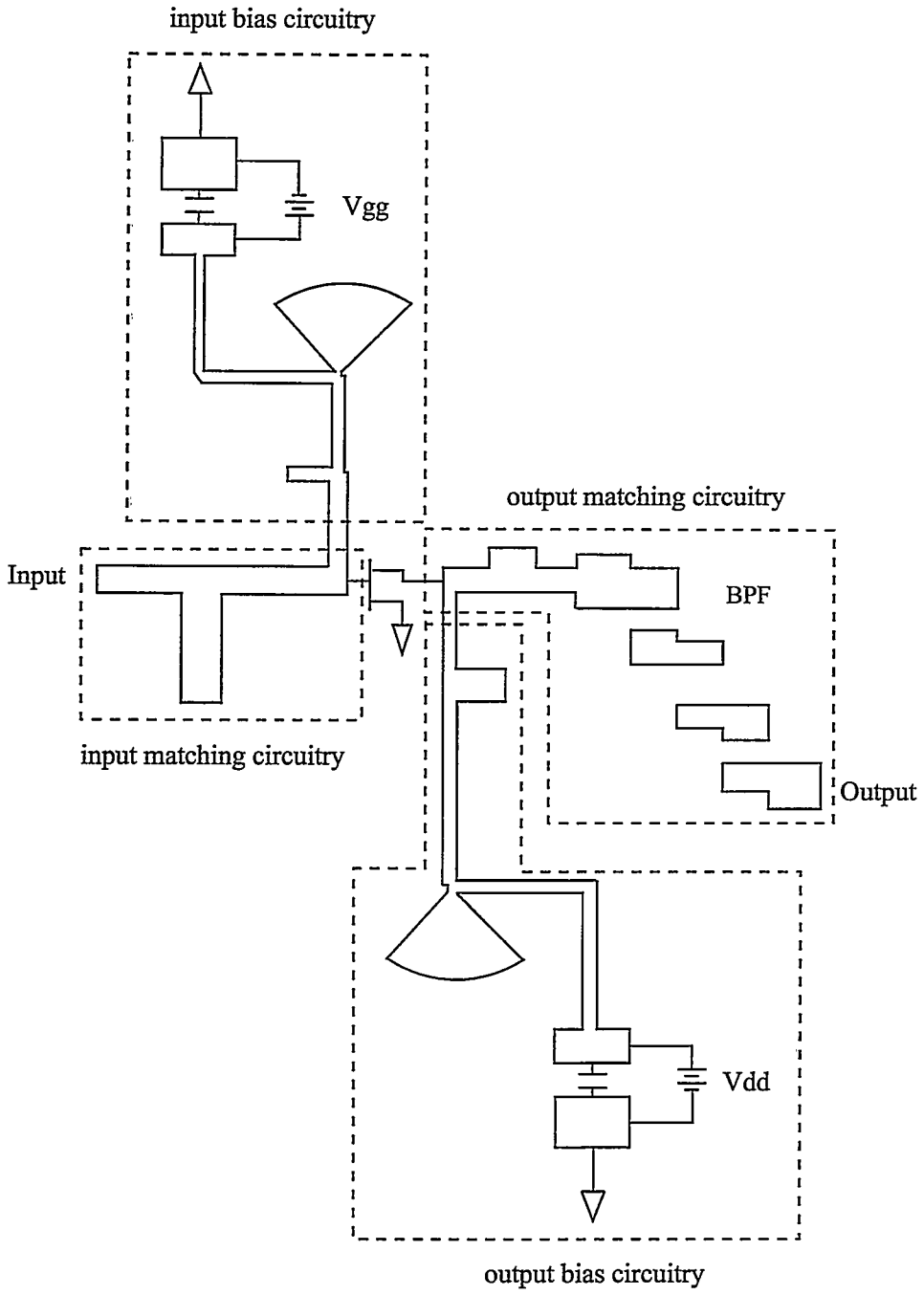


Figure 5.5 Layout for complete x4 multiplier.

Table 5.5 Calculation results for 2nd order Butterworth coupled line filter.

n	g_n	J_nZ_0	$Z_{0e}(\Omega)$	$Z_{0o}(\Omega)$
1	$\sqrt{2}$	0.3332	72.21	38.89
2	$\sqrt{2}$	0.1110	56.17	45.07
3	1	0.3332	72.21	38.89

LineCalc program based on the calculation results in Table 5.5 are used as a starting point for filter optimization. The amplitude response of the 28 GHz filter versus frequency is shown in Figure 5.6. The return loss of the filter is shown in Figure 5.7. The filter presents a small attenuation of 0.5 dB at the multiplier output frequency of 28 GHz, and an attenuation of 31.9 dB at the 3rd harmonic of 21 GHz.

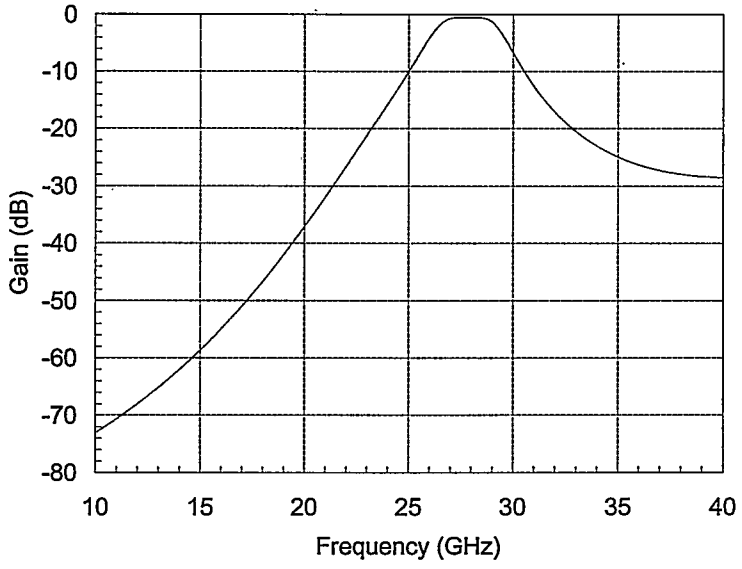


Figure 5.6 Amplitude response of 28 GHz 2nd order coupled line bandpass filter.

The output matching circuitry shown in Figure 5.5 transforms 50 Ω load to the desired load impedance at the 4th harmonic of 28 GHz, while providing a short circuit at the 2nd harmonic of 14 GHz. The output bias circuitry consists of a high impedance feed line and a combination of radial and tuning stubs optimized to provide good short circuits at the fundamental and the 3rd harmonic frequencies. The radial stub provides a short circuit at 28 GHz at the input end (narrow end), so that any variation in the DC voltage source does not affect the circuit performance at 28 GHz. The DC drain bias is applied at the narrow end of the radial stub through a transmission line of high characteristic impedance. Alternative short circuits can be implemented using low impedance open-circuited quarter-wavelength microwave stub. But radial stubs are proved to have larger bandwidth and smaller area than quarter-wavelength open stub of the similar resonance frequency [42]. A

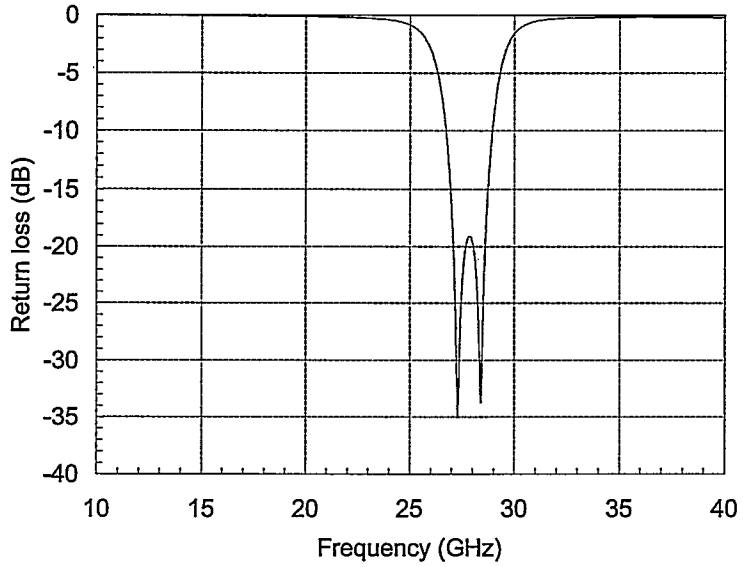


Figure 5.7 Return loss of 28 GHz 2nd order coupled line band-pass filter.

shunt chip capacitor of 5.6 pF decouples the high frequency energy from the V_{dd} supply line to ground. The drain voltage reflection coefficients of the output bias circuitry and the output termination circuitry for the first four harmonic frequencies are shown in Table 5.6. From this table, it is apparent that the output termination circuitry provides a good match at 28 GHz and good short circuits at other harmonic frequencies.

Table 5.6 Voltage reflection coefficients of the output bias circuitry and output termination circuitry for complete x4 multiplier.

Number of harmonics (n)	Frequency GHz	Γ_{bias}	Γ_{output}
1	7	$0.98\angle -172°$	$0.97\angle -178°$
2	14	$0.99\angle 0.001°$	$0.99\angle 179°$
3	21	$0.92\angle 177°$	$0.94\angle -172°$
4	28	$0.94\angle 0°$	$0.81\angle 164°$

The input matching circuitry transforms 50 Ω to the desired source impedance at the excitation frequency of 7 GHz. No DC blocking capacitor is included in

the input matching circuitry, because the x4 multiplier is designed to follow the x3 multiplier, where a coupled line filter is included in the output circuitry and inherently blocks the DC components. A radial stub short circuits the microwave signal at frequency of 7 GHz. The gate voltage is applied through a high impedance transmission line. A bypass chip capacitor with the value of 5.6 pF is adequate to decouple the high frequency signal from the drain bias voltage to ground.

Like the simplified x4 multiplier, the complete x4 multiplier is unconditionally stable at fundamental frequency and all major harmonic frequencies.

5.4 x3 Multiplier Design

Similar to the x4 multiplier design presented in Section 5.3, simplified x3 multiplier is investigated first, and then more practical microwave circuitry is added to complete the design.

5.4.1 Basic Design

Biasing

The x3 multiplier is the first stage of the two-stage multiplier chain. It is followed by the x4 multiplier designed in Section 5.3. Hence, the bias voltage and the input level of the x3 multiplier should be selected to provide an output level that is the optimal input level for the x4 multiplier. Also, it is desirable that these parameters are chosen to provide the conduction angle with which high 3rd harmonic drain current can be obtained.

The optimal conduction angle for the 3rd harmonic drain current is 83.5°, as shown in Figure 4.3. With $V_{g,max} = -1.1\ V$, $V_{g,min} = -4.3\ V$ and the pinch-off voltage $V_t = -1.6\ V$, an estimated conduction angle of 93° is obtained using Equation 5.1. The corresponding gate bias voltage is $V_{gg} = -2.7\ V$. A drain bias voltage of $V_{dd} = 4\ V$, which is the same value as that of the x4 multiplier designed in Section 5.3.1, is chosen.

Output Circuitry

The conduction angle is verified using a similar procedure described in Section 5.3.1 and found to be approximate 93° as estimated according to the time

waveform of the gate voltage shown in Figure 5.8.

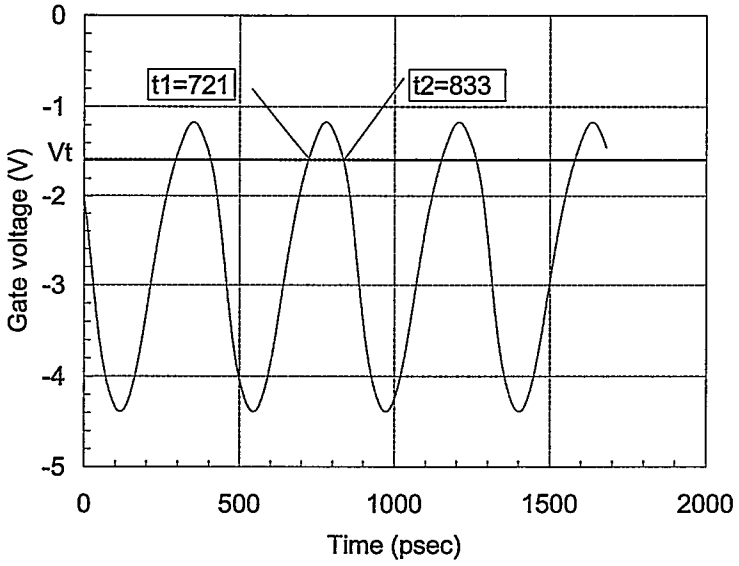


Figure 5.8 Time waveform of gate voltage of the NE1280400 with ideal short circuit drain terminations for x3 multiplier.

A comparison between the simulated magnitudes of drain current components for NE1280400 with ideal short circuit terminations and the calculated results using ideal sinusoidal drain pulse is made in Table 5.7. The simulated results and the calculated results are close. This confirms that the gate bias voltage and the input level were selected to provide a conduction angle of approximate 93°.

Table 5.7 Harmonic drain current components for NE1280400 with ideal short circuit drain terminations for x3 multiplier.

Number of harmonics (n)	Frequency (GHz)	Calculation result	Simulation result
		$\frac{I_n}{I_{d,max}}$	$\frac{I_n}{I_{d,max}}$
1	2.33	0.31	0.28
2	4.67	0.25	0.22
3	7	0.18	0.16
4	9.33	0.10	0.09

The load impedance is selected to achieve the maximum 3rd harmonic output

power. With the conduction angle of 93°, the 3rd harmonic current is 18% of the peak drain current, which is 212 mA under the gate voltage excitation shown in Figure 5.8. Assuming that the drain voltage swing is $V_{d,max} - V_{d,min} = 6\ V$, an estimated load resistance of $R_L = 79\ \Omega$ is obtained using Equation 4.5. Assuming that the drain-source capacitance is 0.5 pF, an inductive susceptance with the value of -21.98 mS is required in parallel with the load resistance R_L. With the susceptance and resistance as calculated above, the estimated load impedance at 7 GHz is Z_L (7 GHz) = $(19.68 + j34.16)\ \Omega$. The corresponding load voltage reflection coefficient at the drain is Γ_L (7 GHz) = $0.59\angle 105°$. It is used as a starting point for Harmonic Balance analysis to find out the optimal load impedance. The Harmonic Balance analysis is run with the drain terminated with the estimated voltage reflection coefficient of Γ_L (7 GHz) = $0.59\angle 105°$ and ideal short circuits with $\Gamma_n = 1\angle 180°$ at other harmonics. The optimization result gives a voltage reflection coefficient of Γ_L (7 GHz) = $0.57\angle 147°$, which corresponds to a load impedance of 27 Ω resistance in parallel with 27 Ω inductive reactance. Again, the optimized load resistance is smaller than the rough calculation.

The 50 Ω load impedance is transformed to the optimized 3rd harmonic load impedance by output termination circuitry shown in Figure 5.9. The output termination circuitry is designed to enhance the 3rd harmonic while maintaining rejection of unwanted harmonics. It presents short circuits at the drain for the fundamental, the 2nd, and the 4th harmonic frequencies. A simple 3rd order coupled line BPF is included in the output circuitry to provide the desired rejection at the fundamental and spurious harmonics, and is also used for impedance matching for maximum output level. No DC blocking capacitor is needed at the output circuitry due to the inherent DC blocking property of the coupled line filter. The design parameters of the 7 GHz filter calculated using Equations 5.2 to 5.6 are the same as those shown in Table 5.2, since the design of these two filters is based on the same 3rd order Butterworth low pass filter prototype and the two filters have the same fractional bandwidth of 10%. The dimensions of the four sections of coupled lines are obtained using Series IV LineCalc program based on the calculated parameters and are used

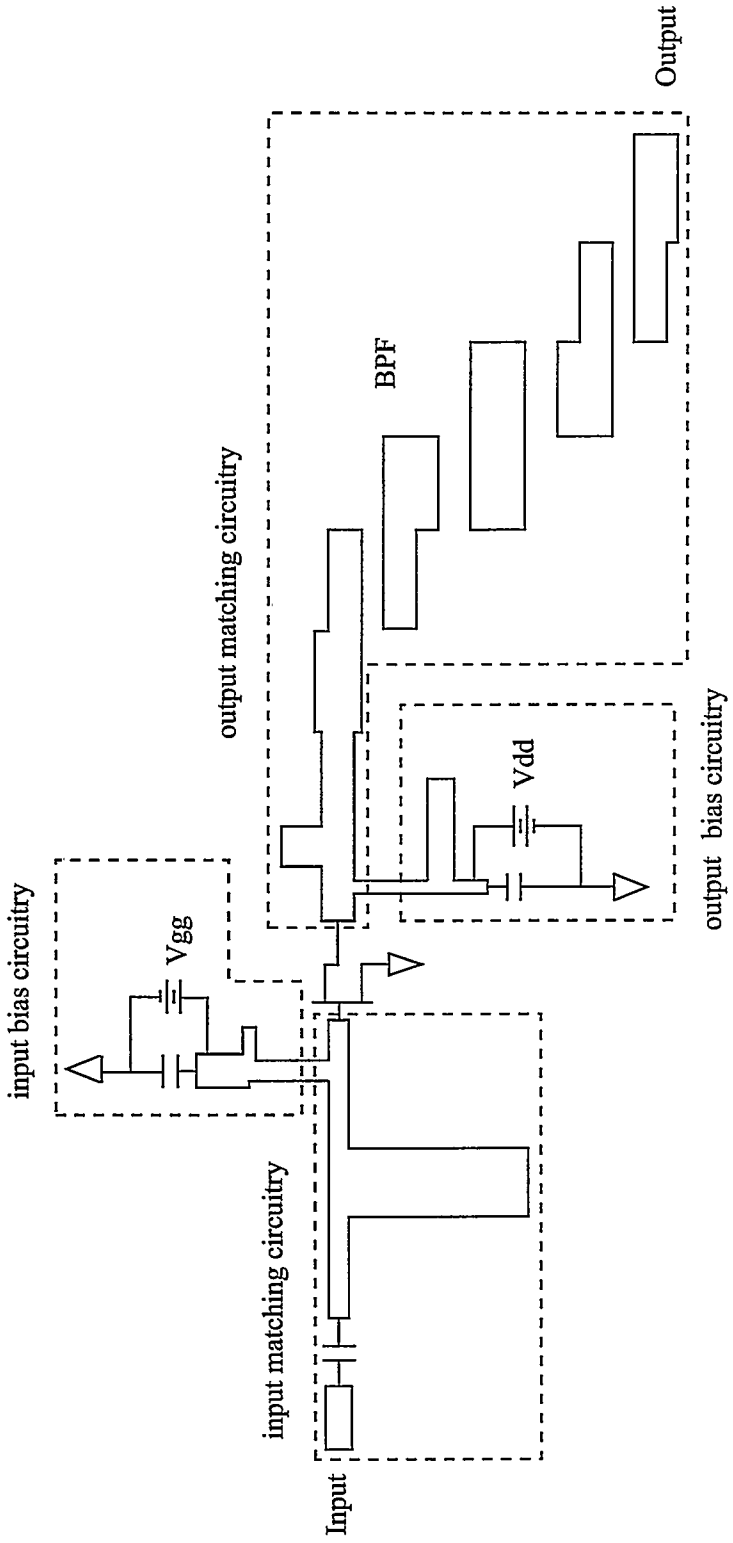


Figure 5.9 Layout for simplified x3 multiplier.

as a starting point for the simulation of the filter circuit. The simulated filter amplitude response is shown in Figure 5.10. The input return loss of the filter is shown in Figure 5.11. The filter is well matched to 50 Ω at 7 GHz, since the return loss at 7 GHz is as low as -37.5 dB. The filter also presents a good performance on harmonic rejection, since the attenuation at the fundamental and unwanted harmonic frequencies are below 39 dB. The loss at pass band is very low, about 0.8 dB.

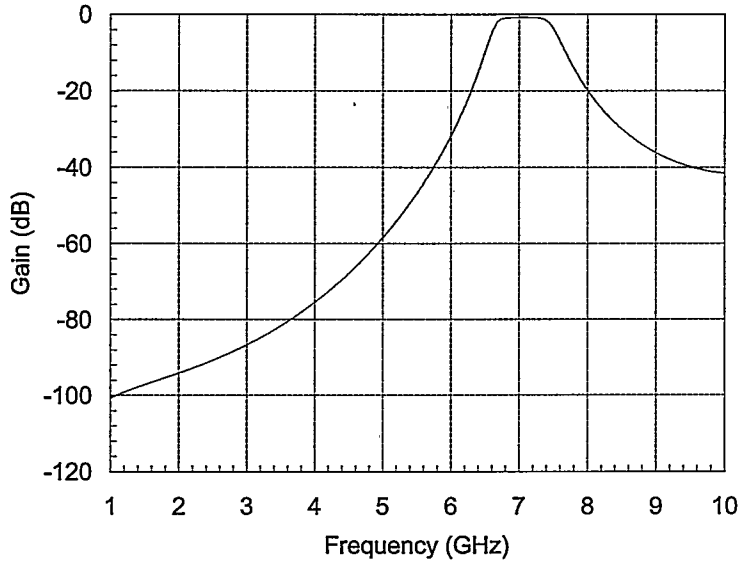


Figure 5.10 Amplitude response of 7 GHz 3rd order coupled line bandpass filter.

The short circuit drain termination at the fundamental frequency and the transformation of the optimal drain load impedance from 50 Ω at the 3rd harmonic is accomplished by the output matching circuitry. The short circuits of the 2nd and the 4th harmonics are provided by the bias circuitry, which presents a high impedance at the fundamental and the 3rd harmonic frequencies, and does not affect the drain terminations at these two frequencies. The voltage reflection coefficients of the drain termination circuitry for the first four harmonic frequencies are shown in Table 5.8.

The harmonic current components at the drain for the NE1280400 with output termination circuitry is shown in Table 5.9. The ratio of the harmonic currents to the peak drain current is close to that for the NE1280400 with ideal short circuit terminations shown in Table 5.7.

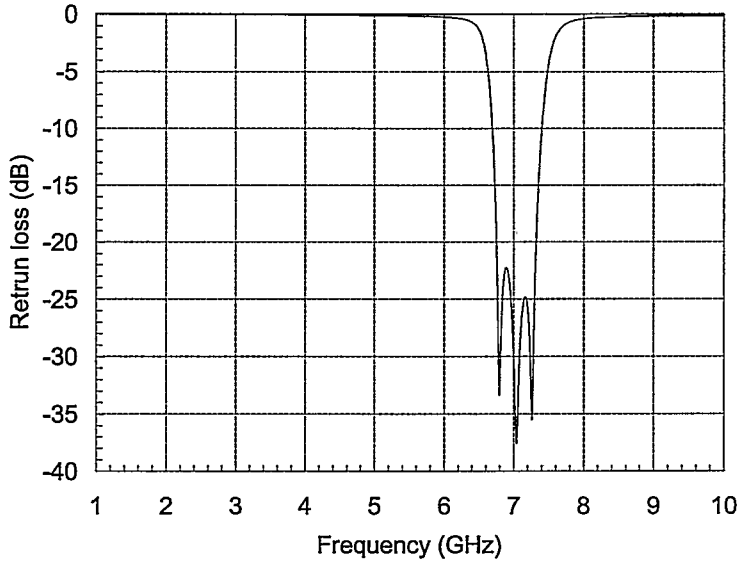


Figure 5.11 Return loss of 7 GHz 3rd order coupled line band-pass filter.

Table 5.8 Voltage reflection coefficients of the output drain termination circuitry for simplified x3 multiplier.

Number of harmonics (n)	**Frequency GHz**	Γ_{output}
1	2.33	$0.99\angle 180°$
2	4.66	$0.96\angle 179°$
3	7	$0.57\angle 147°$
4	9.33	$0.96\angle -176°$

Table 5.9 also shows the drain voltages at harmonic frequencies for the NE1280400 with drain termination circuitry. The small voltage levels at unwanted harmonics relative to the voltage level at the 3rd harmonic indicate that the output termination circuitry is effectively resonated at the 3rd harmonic and provides good short circuits at unwanted harmonics.

Table 5.9 Harmonic drain current and voltage components for NE1280400 with output termination circuitry for simplified x3 multiplier.

Number of harmonics (n)	Frequency GHz	$\frac{I_n}{I_{d,max}}$	$\lvert V_{ds,n}\rvert(V_{rms})$
1	2.33	0.28	0.01
2	4.66	0.22	0.02
3	7	0.14	0.31
4	9.33	0.09	0.02

Input Circuitry

Using a similar method for the x4 multiplier design presented in Section 5.3.1, the input impedance of the terminated FET at 2.33 GHz is measured and found to be $Z_{in} = (20.6 - j193.1)\ \Omega$. The estimated source impedance is $Z_s = (20.6 + j193.1)\ \Omega$, since it is a conjugate match of the input impedance.

The estimated source impedance is transformed from 50 Ω by input circuitry. It consists of input matching circuitry and bias circuitry, as shown in Figure 5.9. A 2.2 pF capacitor is included in the circuitry to provide DC blocking at the gate. The input circuitry is optimized to provide maximum power to the 50 Ω load, while maintaining a good match between the input circuitry and the 50 Ω source impedance. The input level to the x3 multiplier is adjusted to provide the desired gate voltage.

The simplified x3 multiplier is confirmed to be unconditionally stable after the stability check.

5.4.2 Practical Implementation Considerations

The complete x3 multiplier designed in this section is based on the design of the simplified x3 multiplier described in Section 5.4.1. The input and output circuitry is redesigned for the complete x3 multiplier to make it practical for real circuit implementation.

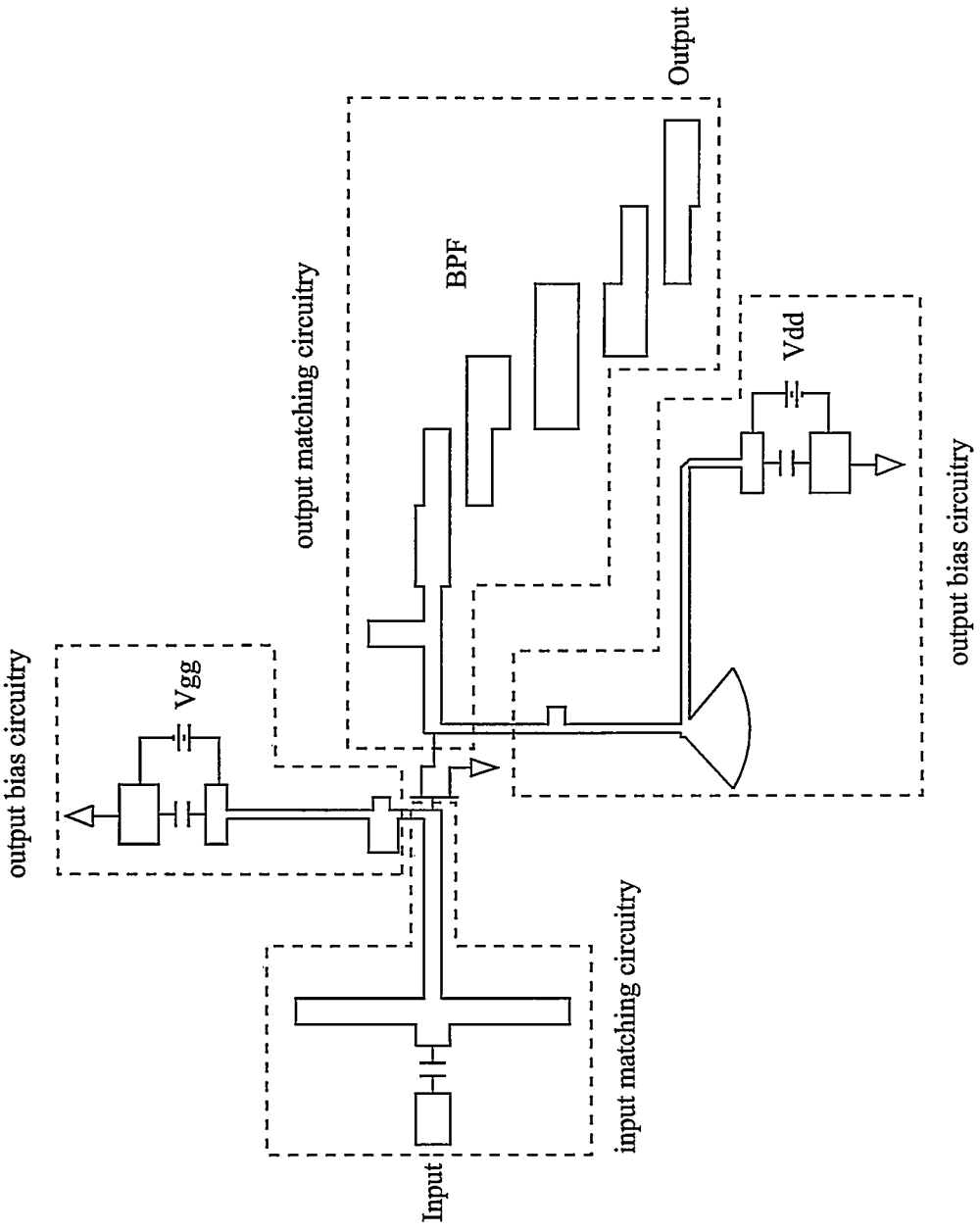


Figure 5.12 Layout for complete x3 multiplier.

The layout of the complete x3 multiplier is shown in Figure 5.12, and also drawn

to scale in Appendix Figure B.2. The 7 GHz 3rd order coupled line bandpass filter described in Section 5.4.1 is employed in the output matching circuitry to perform harmonic rejection function. The output matching circuitry transforms 50 Ω load to the desired load impedance at the 3rd harmonic frequency of 7 GHz, and provides a short circuit at the fundamental frequency of 2.33 GHz. The bias circuitry is similar to that in the complete x4 multiplier presented in Section 5.3.2, and provides short circuit at the 2nd harmonic frequency. The output termination circuitry, which is the combination of the output matching and bias circuitry, provides a good impedance match at the 3rd harmonic frequency and short circuits at the fundamental and 2nd harmonic frequencies. The voltage reflection coefficients of the drain termination circuitry for the first four harmonic frequencies are shown in Table 5.10.

Table 5.10 Voltage reflection coefficients of the output drain termination circuitry for complete x3 multiplier.

Number of harmonics (n)	**Frequency GHz**	Γ_{output}
1	2.33	$0.99\angle -179°$
2	4.66	$0.97\angle -177°$
3	7	$0.57\angle 147°$
4	9.33	$0.89\angle 87°$

The input matching circuitry transforms the 50 Ω source impedance to the optimal source impedance at the fundamental frequency of 2.33 GHz. A 5.6 pF chip capacitor is employed to block the DC components from the gate bias supply. The DC gate voltage is applied by input bias circuitry. As the dimension of the radial stub to short circuit 2.33 GHz frequency component is too large, and becomes impractical for circuit fabrication, the microwave signal is simply bypassed to ground by a 100 pF capacitor.

The complete x3 multiplier is unconditionally stable at the fundamental frequency and all major harmonics.

5.5 Summary

In this chapter, considerations for microwave circuit realization, such as fabrication technology and substrate and transistor selection, are discussed. The detailed design procedures for simplified microwave circuits and complete microwave circuits suitable for MIC fabrication are also presented.

The x3 and x4 multipliers are designed based on the multiplier design theory described in Chapter 4. The x4 multiplier is designed first. The x3 multiplier, which is followed by the x4 multiplier in the two-stage multiplier chain, is designed to provide the desired drive level for the next stage. The x3 and x4 multipliers are designed separately. The simplified microwave circuitry using ideal capacitors and simplified chokes are initially simulated to simplify the design procedure. Then practical circuits required to realize microstrip circuitry at microwave frequencies are added to complete the design.

The simulation results for the multipliers designed in this Chapter are presented in Chapter 6.

Chapter 6

SIMULATION RESULTS

6.1 Microwave Circuits

The performance of the microwave circuits designed in Chapter 5 is presented in this section. All the results in this section are given by simulating the circuits using Series IV with the Harmonic Balance analysis method. The number of harmonics used for the simulation of multipliers and multiplier chains is 24. The harmonic components higher than 24 are very small compared with the harmonic components at the operating frequency of the multipliers and multiplier chains, and can be neglected without affecting the precision of the simulation results.

6.1.1 x4 Multiplier

The simulation results of the x4 multipliers designed in Section 5.3 are presented. The performance of the simplified x4 multiplier designed in Section 5.3.1 and complete x4 multiplier designed in Section 5.3.2 are shown graphically.

The fundamental excitation frequency of the x4 multipliers is 7 GHz. The output frequency is 28 GHz. The gate bias voltage, V_{gg}, for the multipliers is $-2.8\ V$, and the drain bias voltage, V_{dd}, is $4\ V$.

Basic Circuit

The input level for the x4 multiplier is +5 dBm. The output power of the simplified x4 multiplier as a function of output frequency is shown in Figure 6.1. It provides +1.6 dBm output power at 28 GHz. The input return loss at 7 GHz is -19 dB, which confirms that input of the multiplier is well matched to 50 Ω.

The performance of the multiplier circuitry in removing undesired harmonic

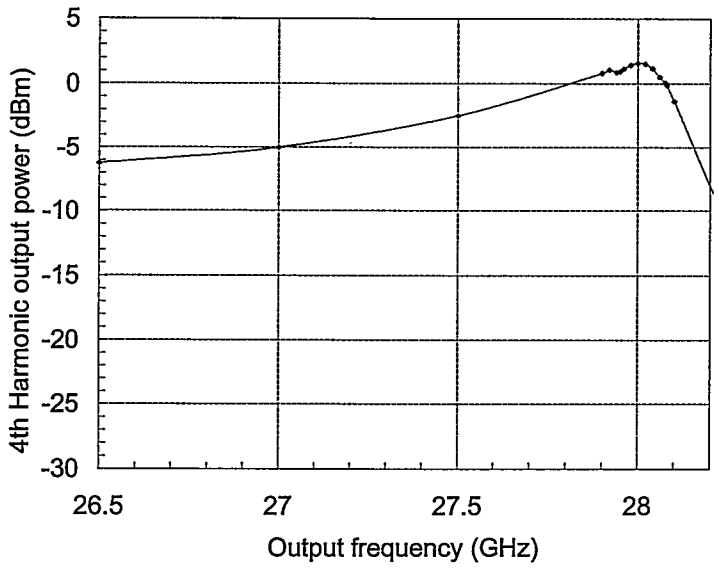


Figure 6.1 Output power of simplified x4 multiplier.

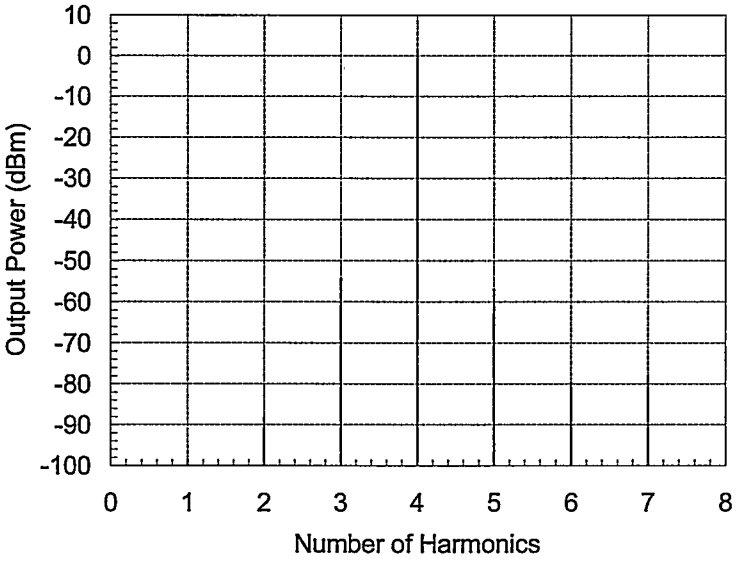


Figure 6.2 Harmonic components of simplified x4 multiplier.

components is shown in Figure 6.2. Figure 6.2 shows that the circuitry provides very good selectivity of the 4th harmonic component at 28 GHz, as the levels of unwanted harmonic components are below 55 dBc.

Practical Circuit

The input power level for the complete multiplier is also +5 dBm. The output power of the x4 multiplier as a function of output frequency is shown in Figure 6.3. It provides +0.6 dBm output power at 28 GHz. The peak output level occurs at 27.95 GHz with the value of +0.9 dBm. Compared with the result of the simplified x4 multiplier, the output level of the practical circuit is a bit lower due to the losses in the capacitors and chokes.

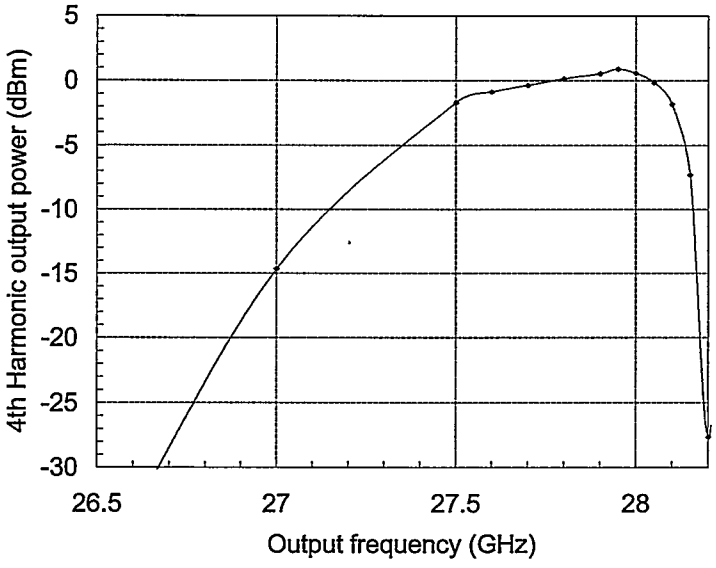


Figure 6.3 Output power of complete x4 multiplier.

The performance of the multiplier circuitry in removing undesired harmonic components is shown in Figure 6.4. Figure 6.4 shows that the circuitry provides very good selectivity of the 4th harmonic component at 28 GHz, as the levels of unwanted harmonic components are below 32 dBc. The harmonic rejection performance of the complete x4 multiplier is not as excellent as that of the simplified x4 multiplier, which provides more than 55 dBc harmonic rejection at unwanted harmonics. This result is within expectation since a 2nd order filter is used instead of a 3rd order

filter.

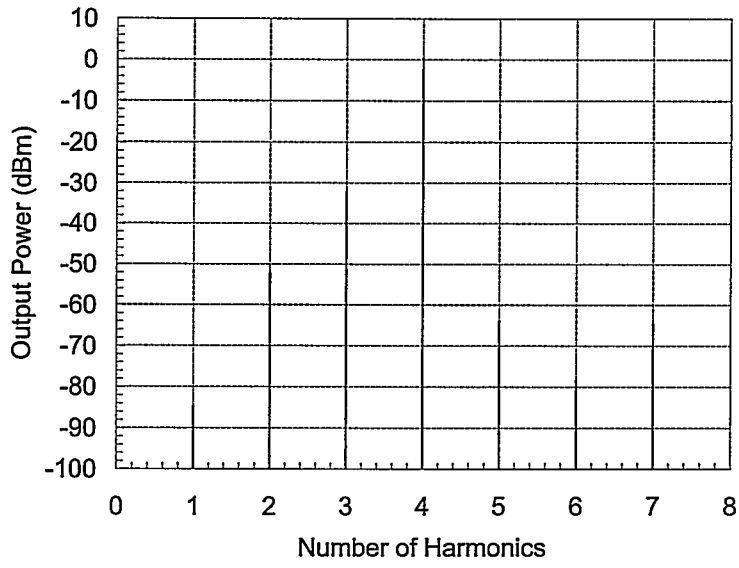


Figure 6.4 Harmonic components of complete x4 multiplier.

6.1.2 x3 Multiplier

The simulation results of the x3 multipliers designed in Section 5.4 are presented in this section. The performance of the simplified x3 multiplier designed in Section 5.4.1 and complete x3 multiplier designed in Section 5.4.2 are shown graphically.

The fundamental excitation frequency of the x3 multipliers is 2.33 GHz. The output frequency is 7 GHz, which is the input frequency of the x4 multipliers. The gate bias voltage, V_{gg}, for the multipliers is $-2.7\ V$, and the drain bias voltage, V_{dd}, is $4\ V$.

Basic Circuits

The input power for the simplified x3 multiplier is -4.9 dBm. The output power of the x3 multiplier is shown in Figure 6.5. It provides $+5$ dBm output power at 7 GHz, which is the required drive level for the next stage, the x4 multiplier. The power gain at 7 GHz is 9.9 dB. The input return loss at 2.33 GHz is -20 dB, which confirms that the input circuitry is well designed to match the input impedance Z_{in} to the 50 Ω source resistance.

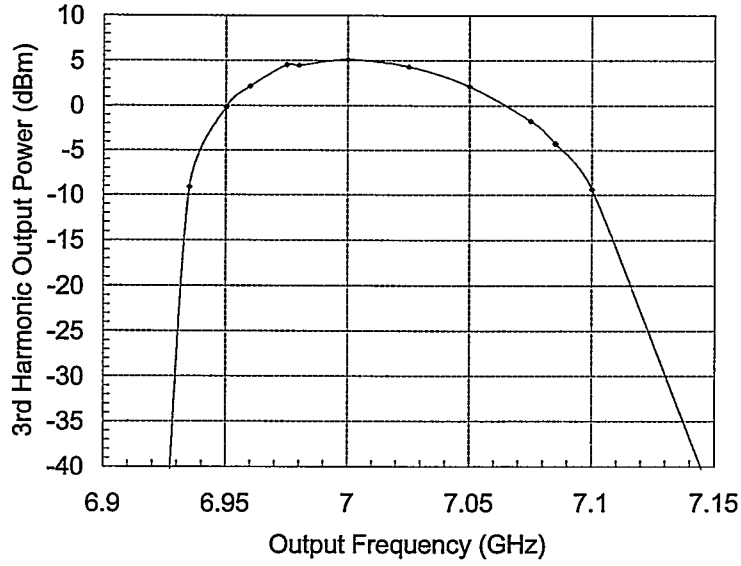


Figure 6.5 Output power of simplified x3 multiplier.

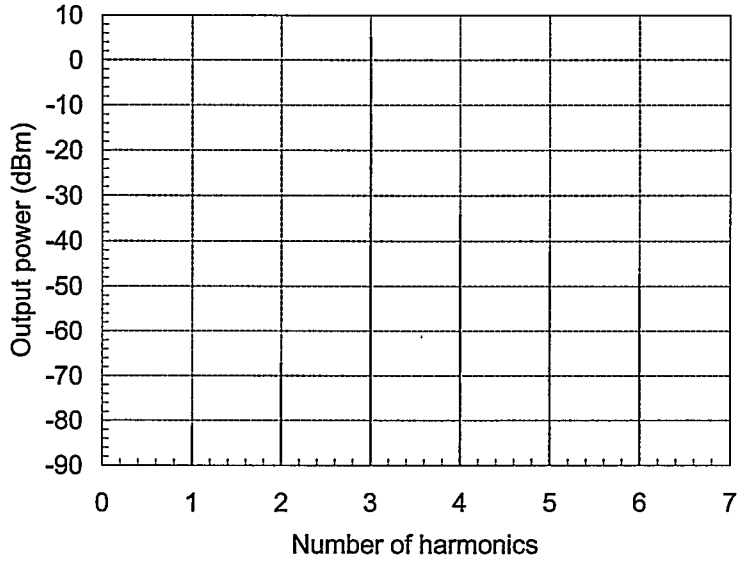


Figure 6.6 Harmonic components of simplified x3 multiplier.

The performance of the multiplier circuitry in removing undesired harmonic components is shown in Figure 6.6. Figure 6.6 shows that the circuitry provides very good selectivity of the 3rd harmonic component at 7 GHz, as the levels of unwanted harmonic components are below 39 dBc.

Practical Circuits

The input source level for the complete x3 multiplier is −3.7 dBm. The output power of the x3 multiplier is shown in Figure 6.7. The output power at 7 GHz is +4.3 dBm, which is the maximum value of the multiplier. The power gain at 7 GHz is 8 dB, which is 2 dB less than the simplified circuit. This could be the result of different drain termination condition. In the simplified x3 multiplier design, the 4th harmonic is short circuited at the drain as shown in Table 5.3. While in the complete multiplier design, the 4th harmonic component is not short circuited, because it is hard to obtain short circuit 4th harmonic termination with practical microwave components.

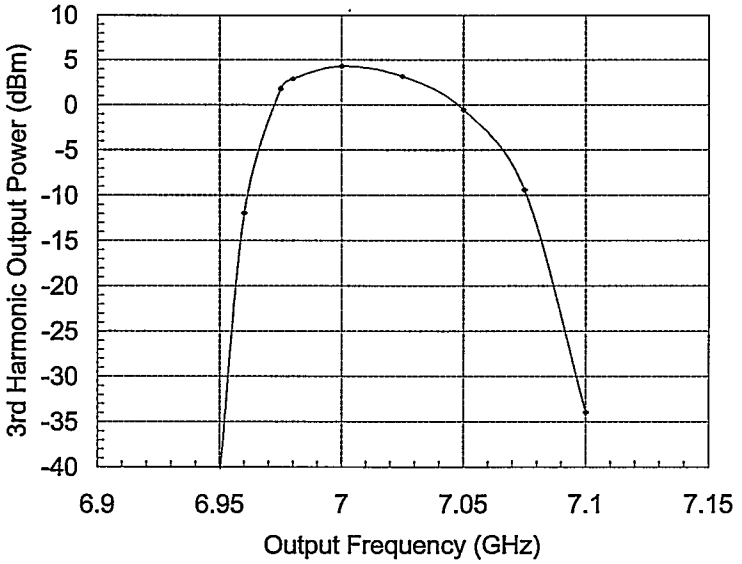


Figure 6.7 Output power of complete x3 multiplier.

Figure 6.8 shows the multiplier's performance on harmonic rejection. The depression of unwanted harmonics is under 28 dBc.

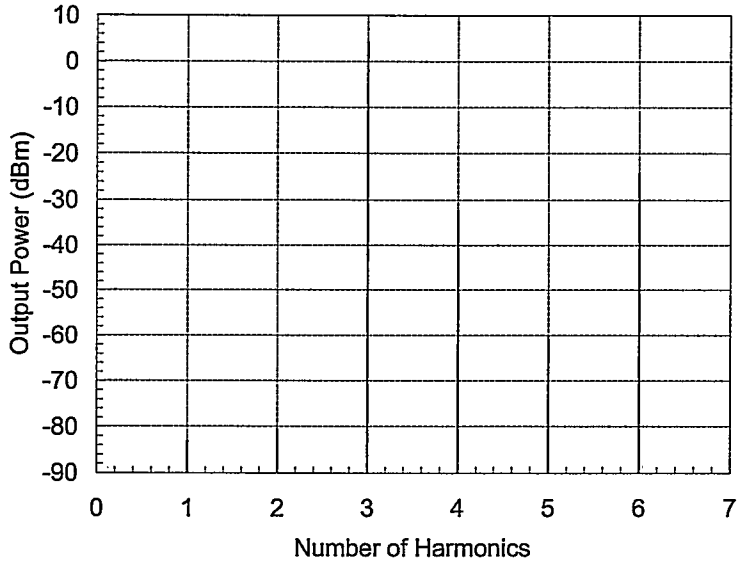


Figure 6.8 Harmonic components of complete x3 multiplier.

6.1.3 Multiplier Chain

The multiplier chain contains the x3 and x4 multipliers designed in Sections 5.4 and 5.3 connected in cascade. The resultant overall multiplication factor is x12. The subharmonic input frequency is 2.33 GHz, which is the fundamental frequency of the x3 multiplier. The 12th harmonic output frequency is 28 GHz, which is the 4th harmonic output frequency of the x4 multiplier.

Basic Circuit

The simplified multiplier chain contains the simplified x3 and x4 multipliers designed in Sections 5.4.1 and 5.3.1 connected in cascade. The input power of the multiplier chain is -4.9 dBm, the same as that of the simplified x3 multiplier.

The output power of the multiplier chain is shown in Figure 6.9. It provides $+3.9$ dBm output power at 28 GHz. The conversion gain at 28 GHz is 8.8 dB. Since the peak output power of the simplified x3 and x4 multipliers occurs exactly at the center frequencies of 7 GHz and 28 GHz respectively (see Figure 6.5 and 6.1), the maximum output power for the multiplier chain is expected to appear at 28 GHz. Figure 6.9 shows that the peak output power occurs at the output frequency of 27.95 GHz with the value of $+4.3$ dBm. In the simulation of x3 and x4 multipli-

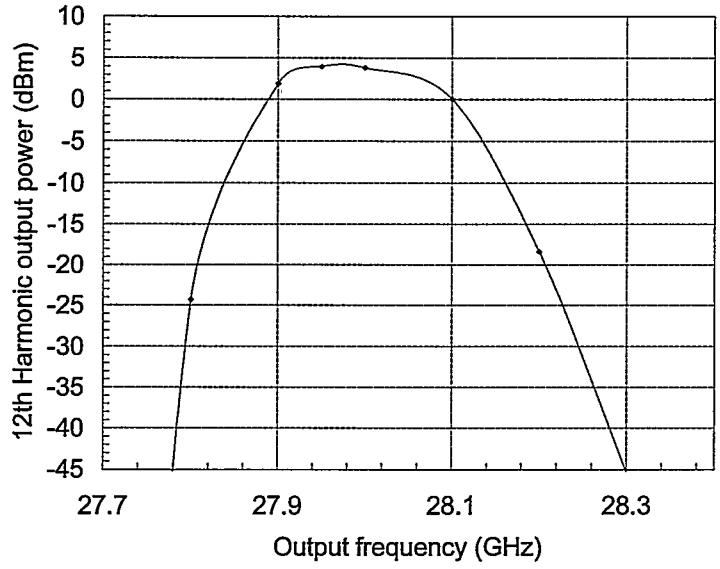


Figure 6.9 Output power of simplified x12 multiplier chain.

ers separately, the source and load impedances connected to the input and output ports of the multipliers are ideal wideband 50 Ω. However, the input impedance for the x4 multiplier is approximately 50 Ω only within a narrow frequency band around 7 GHz. That means that in the multiplier chain, the output port of the x3 multiplier is connected with a narrowband 50 Ω load instead of a broadband 50 Ω load as in the simulation of separate x3 multiplier. The output impedance for the x3 multiplier is probably not 50 Ω even within a narrow band. Therefore, the similar problem exists at the input port of the x4 multiplier in the multiplier chain simulation. As a result, the load impedances of the x3 multiplier at fundamental frequency and harmonics may not be the desired ones since they are transformed from a narrowband 50 Ω load. Similarly, the source impedances of the x4 multiplier may not be the required values, either. The changes of the source and load impedances will consequently affect the main parameters of multipliers, such as gate voltage level and conduction angle. The above differences between the separate multipliers and the multipliers connected in cascade result in the difficulty of predicting the multiplier chain behavior from the behaviors of separate multipliers. The corresponding conversion gain at 27.95 GHz is 9.2 dB, which is the minimal

value obtained with the multiplier chain.

The performance of the multiplier chain circuitry in removing undesired harmonic components is shown in Figure 6.10. Figure 6.10 demonstrates that the circuitry provides very good selectivity of the 12th harmonic component at 28 GHz, as the levels of unwanted harmonic components are below 50 dBc.

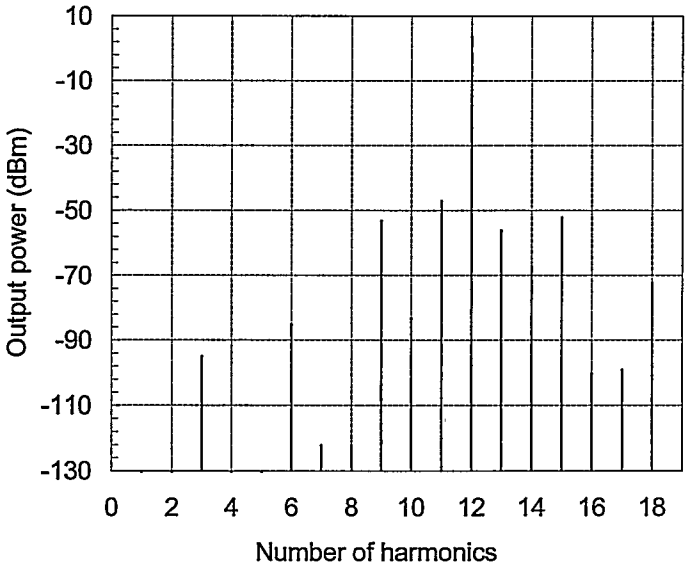


Figure 6.10 Harmonic components of simplified x12 multiplier chain.

Practical Circuit

The complete multiplier chain contains the complete x3 and x4 multipliers designed in Sections 5.4.2 and 5.3.2 connected in cascade. The input power of the multiplier chain is -3.7 dBm, the same as that of the complete x3 multiplier.

The output power of the complete multiplier chain is shown in Figure 6.11. It provides $+3.1$ dBm output power at 28 GHz. The conversion gain at 28 GHz is 6.8 dB. The peak output power occurs at the frequency of 27.98 GHz with the value of $+3.4$ dBm. The corresponding maximum gain is 7.1 dB.

Figure 6.12 shows the output power levels at frequencies from 6th to 18th harmonics of the fundamental excitation frequency. The multiplier exhibits good performance on harmonic rejection, with the level of unwanted harmonics below 33

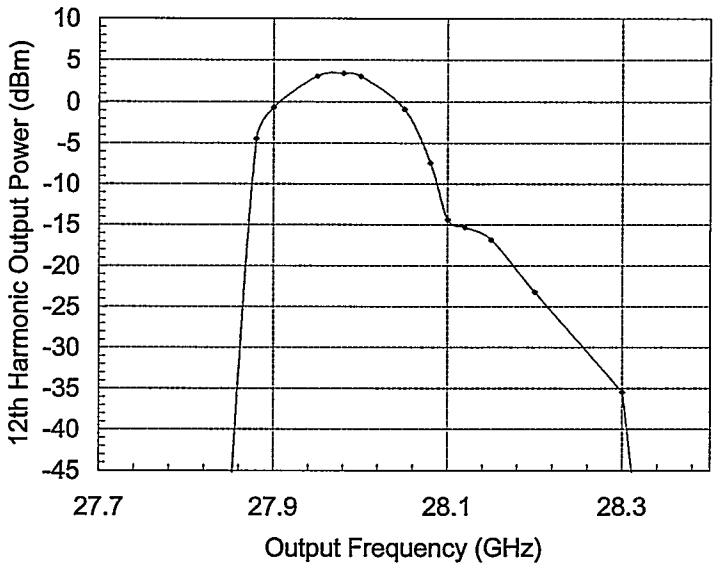


Figure 6.11 Output power of complete x12 multiplier chain.

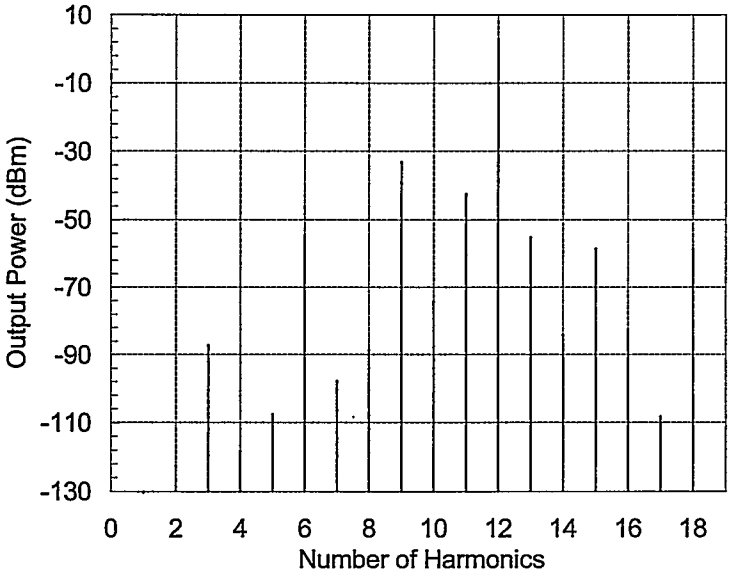


Figure 6.12 Harmonic components of complete x12 multiplier chain.

dBc.

6.2 Amplitude Imbalance

As discussed in Section 3.3.1, imbalance at the input of the two multiplier chains will be introduced due to the quantization errors in SCS and the phase error of the quadrature components in vector modulator. In this Section, the effect of the amplitude imbalance at the input of the two branches of the realistic multiplier chains designed in Chapter 5 will be presented. It is assumed that no power stage is present and the hybrid combiner used for power combination is an ideal component.

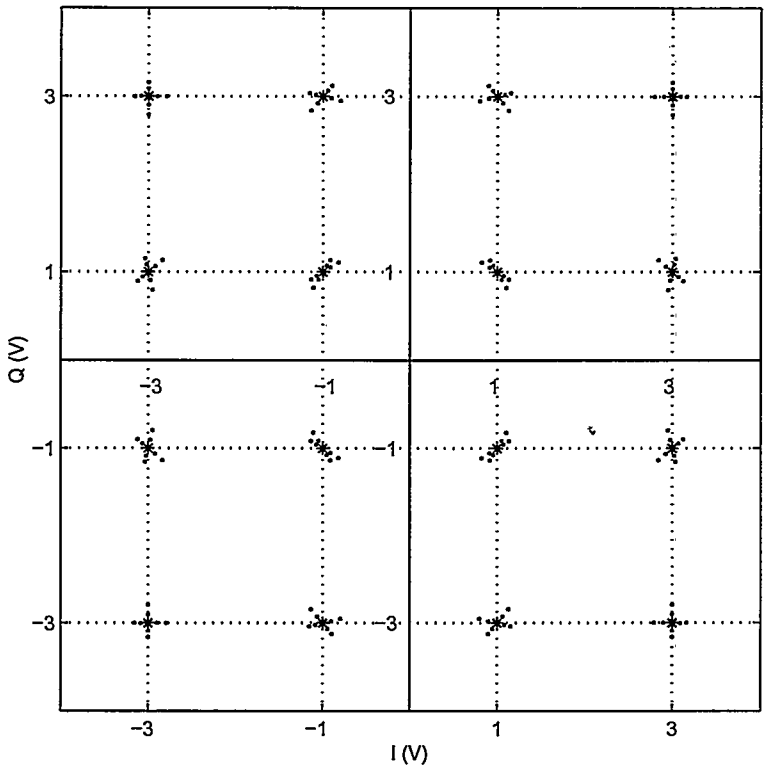


Figure 6.13 Combined constellation diagram for 16-QAM with ±0.1 dB (inside four points) and ±0.2 dB (outside four points) input imbalance using simplified multiplier chains.

Figure 6.13 shows the effect of amplitude imbalance at the input of the two multiplier chains on the combined 16-QAM constellation. The simplified multiplier chains consisting of simplified x3 and x4 multipliers designed in Sections 5.4.1 and 5.3.1 respectively are used for this simulation. The input imbalance between the

two multiplier chains is ±0.1 and ±0.2 dB, which is simulated by keeping one path with no input error, while adjusting the input level of the other path by ±0.1 and ±0.2 dBm. It is assumed that there is no phase imbalance between the input signals at both paths. Figure 6.13 shows that the input amplitude imbalance between the upper branch and lower branch of simplified multiplier chains leads to amplitude and phase error and dispersion in the combined signal constellation points.

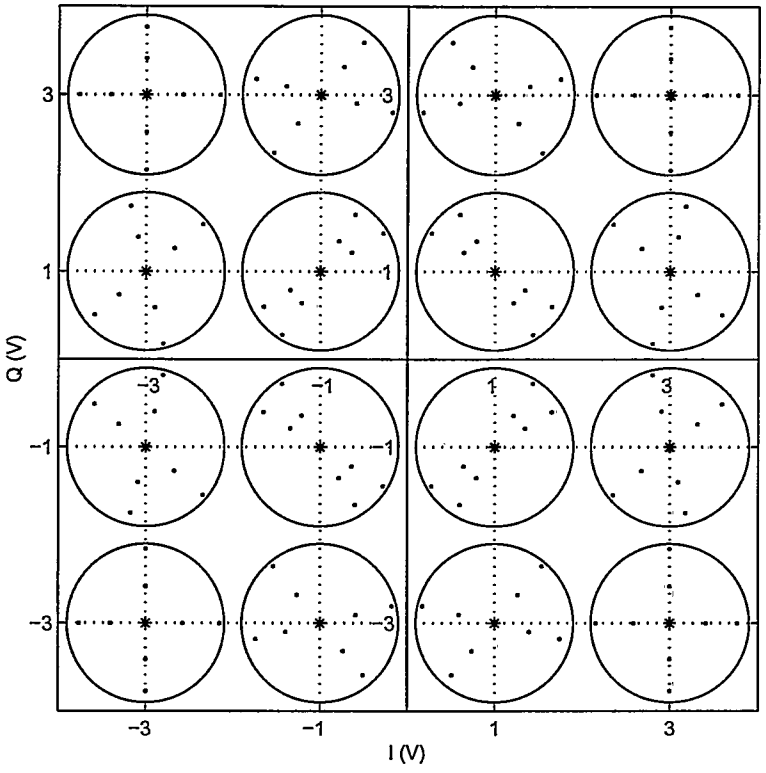


Figure 6.14 Combined constellation diagram for 16-QAM with ±0.1 dB (inside four points) and ±0.2 dB (outside four points) input imbalance using complete multiplier chains.

Figure 6.14 shows the effect of amplitude imbalance on the combined signal constellation using complete multiplier chains, which comprise complete x3 and x4 multipliers designed in Sections 5.4.2 and 5.3.2 and connected in cascade. Similar to the result shown in Figure 6.13 using the simplified multiplier chains, the amplitude imbalance results in both amplitude and phase error in the combined signals and dispersion in the constellation points. Compared with the simplified multiplier

chain, the complete multiplier chain is more sensitive to the amplitude variation of the input signal. This phenomenon can be explained by examining the input to output relationship of the simplified and complete multiplier chains as shown in Figure 6.15 and Figure 6.16 respectively. In these two figures, the horizonal axis denotes the input imbalance, which is the input power relative to the zero error input level. The vertical axis is the output imbalance, which is the output power relative to the zero error output power. It can be seen that for the complete multiplier chain, the output level variation with input level variation is much higher than a linear input to output relationship and also significantly higher than for the simplified multiplier. This results in larger point dispersion in combined signal constellation as demonstrated in Figure 6.14.

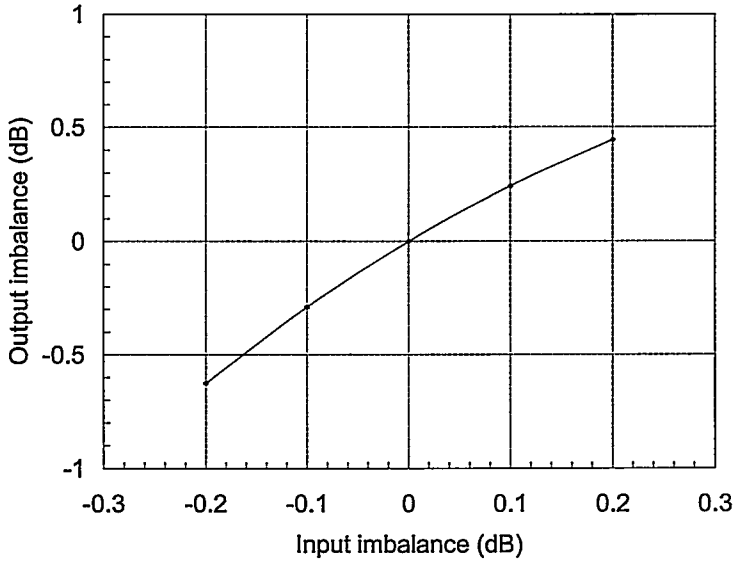


Figure 6.15 Input output relationship for simplified multiplier chain.

Multiplier output level is very sensitive to changes in conduction angle as a result of changing input level. Operating the multiplier in gain saturation might help improve the combined signal constellation. When operated in saturation, the multiplier's output power may vary slightly with variations of input power. Therefore, the amplitude and phase error of combined signal due to the amplitude imbalance between the inputs of both paths will consequently become smaller. Gain satura-

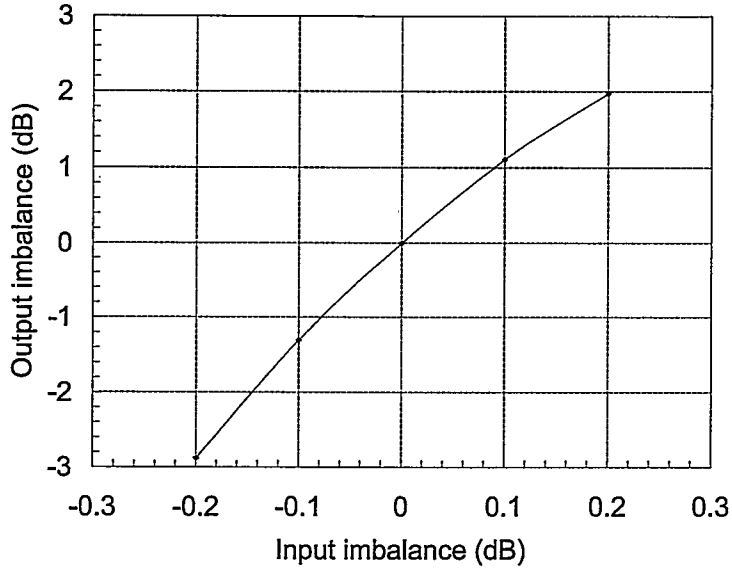


Figure 6.16 Input output relationship for complete multiplier chain.

tion requires that the load resistance, R_L, is large enough so that the maximum load voltage variation permitted by the I-V curve can be obtained with the generated harmonic current [38]. However, the harmonic drain current is small for high order multipliers. The load resistance according to Equation 4.5 is required to be very large to meet the saturation condition. This impractically large load resistance makes the load matching and gain saturation difficult.

6.3 Phase Noise

As mentioned in Section 3.3.2, phase noise causes spectral expansion around the center frequency of the carrier generated by an actual oscillator. In this section, the effect of phase noise on the combined signal constellation is examined.

The precise simulation of real oscillator phase noise can be very complicated. To simulate using the Harmonic Balance simulator for the LINT architecture, a simple approximation of phase noise representative of a real oscillator phase noise process is required. The output of an oscillator can be represented as [43]

$$s(t) = A\cos\left[2\pi f_0 t + u(t)\right], \tag{6.1}$$

where A is the amplitude of the signal, f_0 is the oscillator's operating frequency, and $u(t)$ represents the phase noise.

One possible method to approximate the phase noise, $u(t)$, is to pass discrete white noise through a digital filter [43], the frequency response of which has the correct shape so that the filtered signal has the specific power spectral density similar to that of the required phase noise signal.

An alternative and relatively direct method to generate phase noise is to simulate the noise as a sum of sine waves with random phase [29]. This simulation method is adopted in this thesis. The simulation of the phase noise effect on the combined signal using simplified circuitry and complete circuitry is presented in the next two sections separately. The hybrid combiner is assumed an ideal component for all simulations.

6.3.1 Basic Circuit

A sinusoidal voltage signal can be expressed as

$$V(i) = V_{amp}(i) \sin [2\pi f(i)t + \theta(i)], \tag{6.2}$$

where i is the frequency index, which changes from 1 to the end of the frequency range used in the simulation, f is the frequency, V_{amp} is the amplitude of the sine wave, and $\theta(i)$ represents the random phase of the sinusoidal signal.

The random phase $\theta(i)$ is generated by function "rand" in MATLAB, which produces pseudo-random numbers. The phase noise signal is created by summing together all the individual voltage components $V(i)$, and can be mathematically expressed as

$$u(t) = \Sigma V_{amp}(i) \sin [2\pi f(i)t + \theta(i)], \tag{6.3}$$

with i ranges from 1 to the end of the simulation frequency.

By substituting the noise signal $u(t)$ from Equation 6.3 into 6.1, the simulated output voltage of an oscillator with phase noise is obtained. The amplitude, V_{amp},

of the noise signal with different frequencies should be carefully selected to provide an oscillator signal, which approximates a desired phase noise characteristic.

The phase noise of an oscillator signal is simulated using MATLAB software. The operating frequency, f_0, is 2.33 GHz, which is the subharmonic input frequency of the x12 multiplier chain. The amplitude, A, of the subharmonic sine wave is the voltage from the power source with available power of -4.9 dBm, which is the input level to the simplified x12 multiplier chain. The amplitude, V_{amp}, of the noise signal is varied until a desired SSB phase noise is obtained.

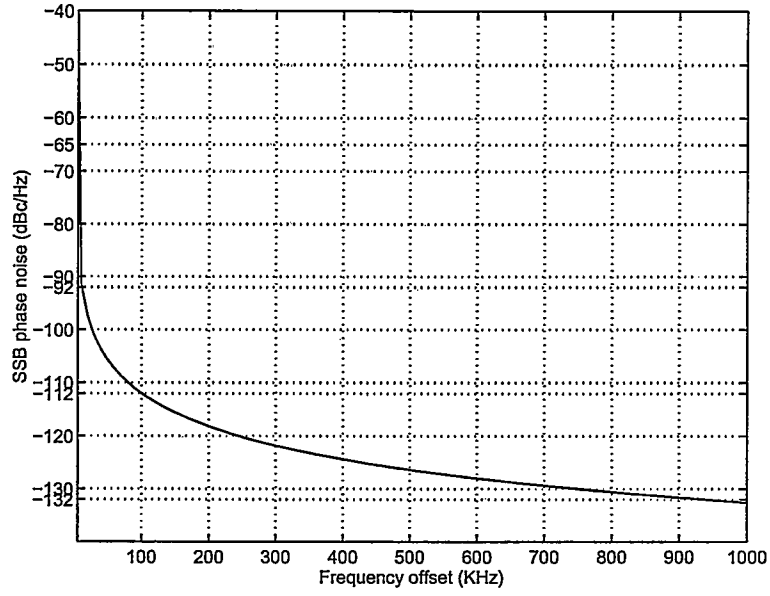


Figure 6.17 SSB phase noise of simulated 2.33 GHz oscillator for circuitry using simplified multiplier chains.

The SSB phase noise of the simulated 2.33 GHz oscillator is shown in Figure 6.17. The specific values of the phase noise at offset frequencies of 10 kHz, 100 kHz and 1000 kHz are very close to those of a typical oscillator [44] operating at the same frequencies as shown in Table 6.1. This demonstrates that the phase noise of the simulated oscillator is reasonable.

From Equations 6.1 and 6.3, it can be seen that phase noise can be simulated as the sum of phase deviation from the center frequency of a source signal in time domain. Therefore, it is reasonable to evaluate the phase noise effect on combined signal constellation by applying a source signal with certain phase deviation instead

Table 6.1 SSB phase noise of a typical oscillator.

SSB phase noise dBc/Hz offset frequencies		
10 kHz	100 kHz	1000 kHz
-92	-112	-132

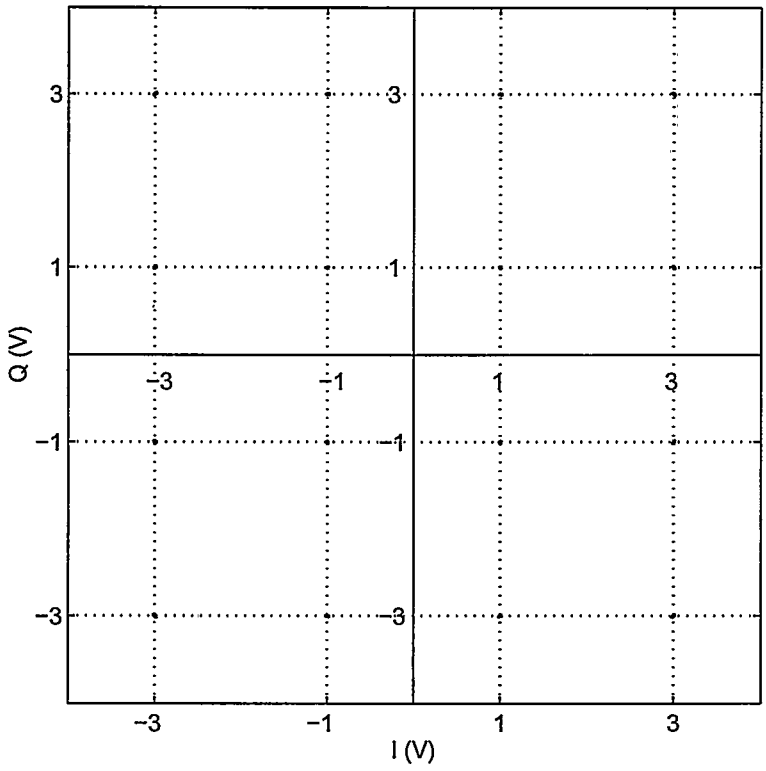


Figure 6.18 Effect of phase noise on combined 16-QAM signal using simplified multiplier chains.

of applying the complete noisy source signal to the circuit. The possible maximum phase deviation is the sum of the peak amplitudes, $V_{amp}(i)$, of the sinusoidal signals at all frequencies. The effect of phase noise on the combined signal constellation using the simplified multiplier chains is shown in Figure 6.18. It is obtained by applying a source signal with discrete phase deviation, which is kept within the possible maximum value, to the circuit under simulation. Like the effect of amplitude imbalance, phase noise on a source oscillator also results in dispersion of the combined 16-QAM constellation points, but this is minimal assuming the phase noise characteristic of a typical subharmonic reference signal.

6.3.2 Practical Circuit

The amplitude, V_{amp}, of noise signal, $u(t)$, in Equation 6.3 should be adjusted for the circuitry under test using complete multiplier chains, since the input level to the complete multiplier chain is -3.7 dBm, instead of -4.9 dBm to the simplified multiplier chain. The amplitude, A, of the noisy source signal in Equation 6.1 is set with a new value, which is the voltage from a -3.7 dBm power source followed by a complete x12 multiplier chain. Then the amplitude of noise signal, $u(t)$, at different frequencies is adjusted until a SSB phase noise close to that of the typical oscillator shown in Table 6.1 is obtained. Figure 6.19 shows the SSB phase noise of the simulated oscillator for circuitry using complete multiplier chains.

The effect of phase noise on the combined signal constellation using complete multipliers is shown in Figure 6.20, which is obtained using the same method described in Section 6.3.1. From Figures 6.18 and 6.20, it can be seen that the phase noise in an oscillator has similar effect on combined signal constellation, no matter simplified or complete multiplier chains are used.

6.4 Summary

In this chapter, simulation results for the simplified and complete circuits designed in Chapter 5 are presented.

The x3 and x4 multipliers show good performance separately. The simplified and complete x12 multiplier chains both exhibit good performance as well. The

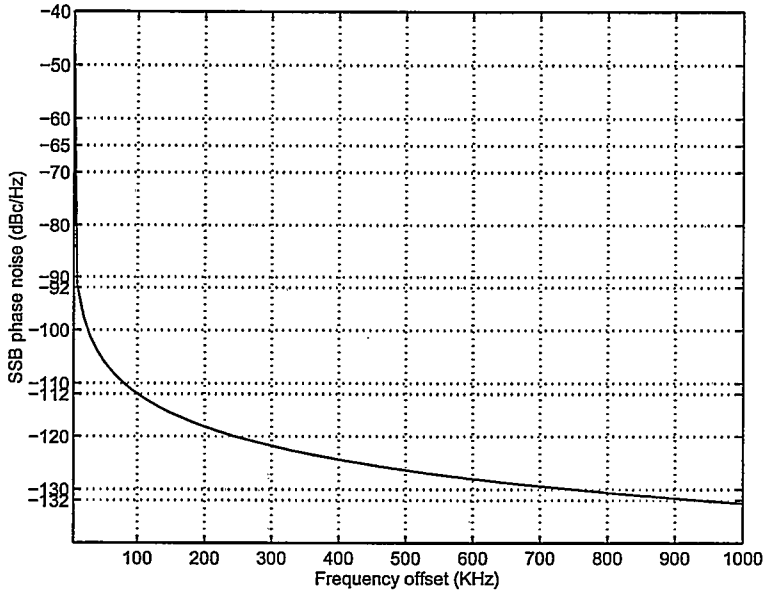


Figure 6.19 SSB phase noise of simulated 2.33 GHz oscillator for circuitry using complete multiplier chains.

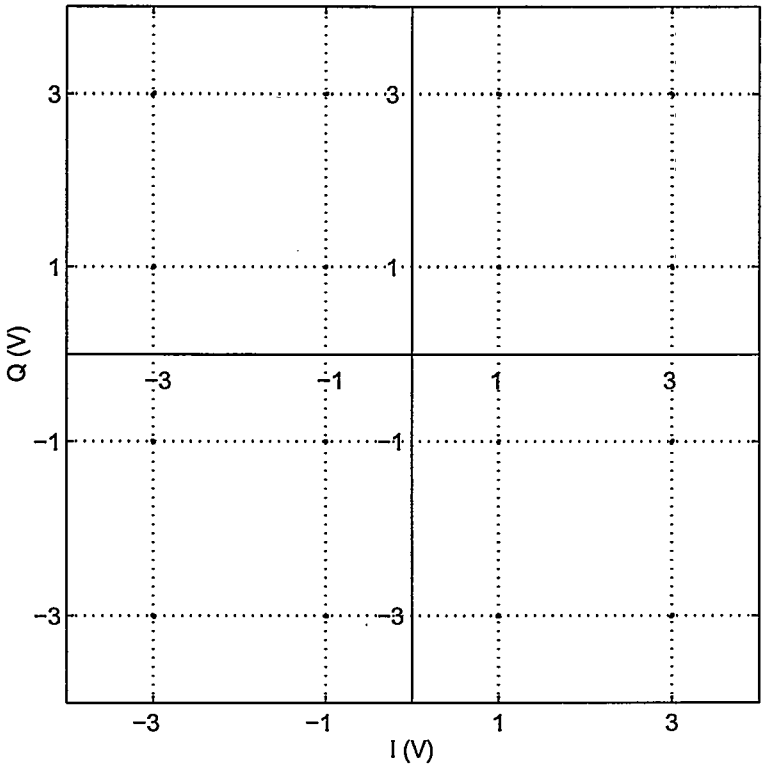


Figure 6.20 Effect of phase noise on combined 16-QAM signal using complete multiplier chains.

simplified multiplier chain provides a conversion gain of 8.8 dB and output level of +3.9 dBm at 28 GHz, and unwanted harmonic suppression below 50 dBc. Due to the loss of capacitors and the use of a 2nd order filter in x4 multiplier, the complete x12 multiplier chain has lower conversion gain of 7 dB and output level of +3.1 dBm at 28 GHz, and higher levels of unwanted harmonic components < 33 dBc.

Two imperfections that will degrade the overall performance of the LINT modulator are also simulated in this chapter. One is the effect of amplitude imbalance at the input of both multiplier chains on the combined 16-QAM constellation. The amplitude imbalance causes dispersion of the combined signal vectors. The other is the effect of phase noise of the input power sources on the combined signals. The phase noise of an oscillator is simulated as the sum of sine waves at offset frequencies ranging from 10 kHz to 1000 kHz by using MATLAB. The SSB phase noise of the 2.33 GHz oscillator is simulated based on the phase noise of a commercially available oscillator operating at the same frequency. Like the effect of amplitude imbalance, the phase noise also causes vector splatter of the combined signals. The complete multiplier chain is more sensitive to amplitude variation of the input source signal, and thus the amplitude imbalance introduces severe distortion on the combined signal. Operating the multipliers in gain saturation is an effective method to improve the performance. The simplified and complete multiplier chains both show good performance on phase noise effect with similar simulation results.

Chapter 7

CONCLUSIONS

7.1 Summary

The ever increasing demand for high speed data services is forcing new and emerging broadband communications towards the high microwave and millimeter-wave frequency bands. Simple and cost-effective transmitters operating at such frequencies are very attractive. The radio spectrum is a limited resource, and therefore, modulation techniques that enable more information to be carried over a finite channel bandwidth are preferred. Power efficiency is another desired quality of transmitters. Poor power efficiency is not suitable for many applications, where large batteries are needed to supply excess power, and large heat sinks are required. The high spectral efficiency property of linear modulation schemes satisfies the bandwidth requirement of modern communication systems.

Compared with the traditional method of IF modulation and upconversion to the desired transmitting frequency, direct modulation at the transmitting frequency is an attractive option for reducing the cost and complexity of the transmitter. The LINC technique is a promising linearization method to obtain both high power efficiency and high spectral efficiency. The new LINT modulator described in this thesis expands the direct modulation and LINC concepts to include frequency translation and is suitable for implementation at upper microwave and millimeter-wave frequencies, and results in simple modulator hardware architecture.

The development history of wireless communication are described briefly in Chapter 1. Concepts of direct digital modulation, linear modulation and LINC technique are introduced.

Basic theory of the direct LINT modulation method is presented in Chapter 2. The block diagram of LINT modulator is given and functions of each block are described in detail. The validity of LINT theory is proved mathematically.

In Chapter 3, principles of the 16-QAM scheme are presented. Baseband LINT modulation employing the 16-QAM format is simulated using MATLAB software. Imperfections that will degrade the overall performance of LINT modulator are discussed.

Theories and practical considerations for microwave frequency/phase multiplier design are presented in Chapter 4. Detailed design procedures for simplified and complete x3 and x4 multipliers based on the theories described in Chapter 4 are presented in Chapter 5.

Performance of the microwave circuits designed in Chapter 5 is shown graphically in Chapter 6. Effects of the imperfections discussed in Chapter 3 on the combined signal constellation using microwave circuits designed in Chapter 5 are also simulated.

7.2 Conclusions

The objectives of this research as defined in Chapter 1 are as follows:

1. Propose a new modulator architecture (LINT), which is suitable for linear modulation schemes at microwave and millimeter-wave frequencies with high power efficiency and frequency translation.

2. Investigate the validity of LINT signal component separation and phase scale algorithm.

3. Design and simulate realistic microwave circuits for evaluation of the LINT technique.

4. Investigate the performance of the LINT technique with typical modulator impairments such as amplitude imbalance and phase noise.

The first objective is fulfilled after investigating some published papers on direct digital modulation and LINC techniques. The new LINT modulator proposed in this thesis is an extension of direct modulation principle and the LINC concept.

The LINT modulator employs the method of direct modulation of a subharmonic carrier signal using vector modulation followed by frequency/phase multiplier chains to achieve the desired modulated output signal characteristics at the desired output frequency. With this method, a single oscillator is present in the transmitter, rather than multiple stages of upconversion and filtering that are typical in more conventional transmitter. A simple and cost-effective hardware solution can be obtained with this method. It is also easy to extend the modulator to higher frequencies, simply by increasing the multiplication factor. This modulator is suitable for more spectrally efficient linear modulation schemes like QAM. Also high power efficiency can be expected due to the use of a Class C power amplifier. The result of this research is a simple, generic linear modulator suitable for a wide range of transceiver functions required in emerging radio systems operating at upper microwave and millimeter-wave frequencies.

The theory of LINT technique is shown mathematically by equations. The baseband signal separation and phase scale is simulated using MATLAB software employing 16-QAM format. The simulation results prove further the validity of the LINT principle.

The two-stage microwave frequency/phase multiplier chain is an important part of the modulator and is considered in detail. It includes x3 and x4 multipliers connected in cascade. The nonlinear microwave circuitry is simulated using HP-EEsof Series IV [39] microwave design software with Harmonic Balance analysis. In the separate x3 and x4 multiplier design, the optimized load resistance, R_L, is much smaller than expected (see Sections 5.3.1 and 5.4.1). This results in a smaller drain voltage swing. One possible explanation is that when the drain voltage excursion decreases, the gate voltage increases due to the feedback effect and this changes the input impedance at the FET gate. Therefore, the drain current gets higher, and consequently the output power level gets higher, too. This phenomenon may confuse the simulator optimization, and drive the simulator to optimize based on a different nonlinear effect. Keeping the peak gate voltage fixed when performing optimization might help solve the problem. Despite the above imperfection in the multiplier

design, the multiplier chain exhibits excellent performance with output level of +3.1 dBm and harmonic rejection below 33 dBc as shown in Section 6.1.3. The two-stage multiplier chain has a multiplication factor as high as 12, and effectively translates an input CW signal at subharmonic of 2.33 GHz to an output signal at upper microwave frequency of 28 GHz. Each multiplier stage is designed using a single FET chip, resulting in a simple hardware solution. Typically, microwave circuits operating at upper microwave bands are designed on hard substrate, and complex technique and equipment is required for circuit fabrication. The multiplier chain presented in this thesis is designed on soft substrate, which makes it cost-effective and easy for laboratory fabrication.

The performance of the LINT modulator is investigated using the x12 multiplier chain and an ideal hybrid combiner. The gains and phase delays between the two multiplier chain paths cannot be exactly the same due to fabrication and device differences. This results in amplitude and phase error at the input of the hybrid combiner, and limitation of the LINT performance. Another source of imperfection occurs at the input of multiplier chains, which includes the quantization error when using a DSP device to accomplish SCS and phase scaler and small phase error between the quadrature inputs of vector modulators. The effect of amplitude imbalance at the input of the two branch multiplier chains on combined 16-QAM signal constellation is simulated using MATLAB software. Simulation results show that the LINT modulator is very sensitive to the amplitude imbalance. Operating the multipliers at gain saturation may decrease the degree of the sensitivity of the circuits to input amplitude variation. Another way to improve the LINT performance is to detect the gain and phase error in the LINT output signal and then compensate it by introducing a correction at the baseband, which is similar to the algorithm employed by the LINC modulator [19] [20] [21] [22]. In order to investigate the phase noise effect on the LINT modulator using Harmonic Balance simulator, a simple approximation of a real oscillator phase noise process is made. With this method, the phase noise is simulated as a sum of sinusoidal waves with random phase. Simulation results show that the phase noise in an oscillator at the

subharmonic frequency has little effect on the combined 16-QAM constellation.

7.3 Future Work

Future research is suggested as follows:

1. The multipliers can be designed in gain saturation to mitigate the amplitude imbalance effect on the LINT modulator.

2. The x12 multiplier chain can be fabricated using MIC or MMIC technology described in Section 5.1.1 and the performance can be tested using vector network analyzer.

3. A power combiner or divider operated at 28 GHz can be designed.

4. The baseband digital circuitry can be implemented using FPGAs (field programmable gate arrays) and look-up tables. An alternative is to implement the baseband signal process in software by using DSP device.

5. The usefulness of the modulator for realizing other microwave and millimeter-wave modulation and multicarrier modulation schemes like OFDM [45] [46] can be investigated.

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