RELIABILITY EVALUATION OF MICROELECTRONIC DEVICES

A thesis

Submitted to the Faculty of Graduate Studies and Research

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in the

Department of Electrical Engineering

University of Saskatchewan

by

Kunche Satyanarayana

Saskatoon, Saskatchewan

June 1981

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Saskatoon, Saskatchewan, Canada

ACKNOWLEDGEMENTS

The author would like to express his gratitude and thanks to Dr. Roy Billinton and Dr. S. K. Dey for their assistance, guidance, and encouragement during the course of this project. He also wishes to thank Professor A. E. Krause for his assistance in the use of the RSX-11M (version 3.2.) system on the department's DEC PDP-11/60 computer for the editing and text formatting of this thesis.

He also wishes to thank RCA, Bell Laboratories, Intel, Bell Nothern Research, Tektronix, SED etc., organizations for their valuable assistance in the preparation of this thesis.

Financial assistance, in the form of National Overseas Scholarships was provided by the Government of India, Ministry of Home Affairs. Special study leave was provided by the Government of India, Ministry of Industry (Small Industry Development Organization). Their support is gratefully acknowledged.

UNIVERSITY OF SASKATCHEWAN

Electrical Engineering Abstract 81A210

RELIABILITY EVALUATION OF MICROELECTRONIC DEVICES

Student: K. Satyanarayana Supervisors: Dr. Roy Billinton
Dr. S. K. Dey

M.Sc. Thesis presented to the College of Graduate Studies

June 1981

ABSTRACT

The semiconductor device industry is approximately 30 years old. Since its inception, reliability, speed of operation and production yields have steadily improved while cost, power consumption and size have been reduced drastically. This is particularly true for both bipolar transistors and metal oxide semiconductor field effect transistors (MOSFETs). There is very little standardization in the integrated circuit (IC) industry regarding materials and technologies used due to a continuing emphasis on the device reliability, complexity and miniaturization.

The activity in regard to the reliability of semiconductor discrete devices has largely saturated while the activity in the area of microelectronic devices is continuing to accelerate due to the dynamic nature of microelectronic device technology. Microelectronic devices are usually extremely complicated and therefore their evaluation should be considered as a separate area which warrants a sophisticated reliability evaluation program. The most important aspects to be considered are the failure modes and failure mechanisms, burn-in and accelerated life testing, failure distributions, activation energy and acceleration factors and their applications in failure rate prediction and sample size estimation and failure analysis techniques.

This thesis presents (1) the basic theory and techniques for reliability evaluation of microelectronic devices and an examination of the practical work done by industries like RCA, Intel, Harris, Bell-Laboratories, Bell Telephone Laboratories, Texas instruments etc., and based on these findings, (2) a total reliability evaluation program for 4K CMOS static memory devices and (3) a cost analysis and reliability facility plan.

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LIST OF ABBREVIATIONS

Access time : The time required to communicate with the memory.

AES : Auger electron spectroscopy.

ASTM : American society for testing and materials.

AQL : Acceptable quality level.

BV_{EBO} : Breakdown voltage of emitter-base junction of a bipolar transistor.

BTL : Bell telephone laboratories.

BPO : British post office.

CCD : Charge coupled device.

CERDIP : Ceramic dual-in-line package.

C.L : Characteristic life as per weibull distribution.

CMOS : Complementary metal oxide semiconductor.

CS : Chip select.

DH : Device-hours.

DIP : Dual-in-line package.

dt : time interval.

DT or dT : Temperature interval.

DTL : Diode transistor logic.

DUT : Device under test.

EBIC : Electron beam induced current.

ECOM : Electronics technology and device laboratory.

EDH : Estimated device-hours.

EPROM : Erasable programmable read only memory.

ERL : Estimated reliability level.

ESCA : X-ray photoelectron spectroscopy.

F : Acceleration factor.

FAMOS : Floating-gate avalanche-injection metal oxide semiconductor.

FIT : one failure per 10^9 device-hours.

GALPAT : Gallaping 1's and 0's.

HMOS : High performance metal oxide semiconductor devices.

IC : Integrated circuit.

Idd : Current drawn from Vdd power supply.

IGFET : Insulated gate field-effect transistor.

IIL(H) : Input low (high) current - current when the output is at logic 0(1) level.

IL(H)Z : High impedance, low (high) leakage current - leakage current measured at logic 0(1) level when output is in high impedance state.

IMMA : Ion microprobe mass analyzer.

IOL(H) : Output low (high) current - current when the output is at logic 0(1) level.

K : Boltzman's constant, 8.63×10^{-5} e.v./^{0} K.

K-S : Kolmogorov-Smirnov.

LCD : Liquid crystal display.

LSI : Large scale integration.

LSO : Least square.

LSTTL : Large scale transistor-transistor logic.

LTPD : Lot tolerance percent defective.

MARCH	:	Marching 1's and 0's.
MASEST	:	Multiple address selection exercise test.
MIL	:	U.S military specification.
M.L	:	Median life.
MLH	:	Maximum likelihood.
MOS	:	Metal oxide semiconductor.
MSI	:	Medium scale integration.
MUT	:	Memory under test.
n	:	Sample size.
NCR	:	NCR Corporation.
NMOS	:	N-Channel MOS.
nv	:	nano-volt.
PC/MS	:	Plasma chromography mass spectroscopy.
PIND	:	Particle impact noise detection.
PMOS	:	P-Channel MOS.
PRAM	:	Pattern random access memory.
PROM	:	Programmable read only memory.
PSG	:	Phosphosilicate glass.
pv	:	Pico-volt.
RAM	:	Random access memory.
RAID	:	Rewritable avalanche injection device.
RCA	:	Radio corporation of America.
Refresh time	:	The time required for an operation performed periodically on dynamic memory devices to preserve the stored data.
R.F	:	Radio frequency.
RH	:	Relative humidity in % .

SEM	: Scanning electron microscopy.
SIM	: Scanning ion mass spectroscopy.
SOS	: Silicon-on-Sapphire.
SSI	: Small scale integration.
SVC	: Selective voltage contrast in SEM.
TAA	: Address access time - measured from address change to output valid data.
TB	: Temperature bias.
TBF	: Time between failures.
THB	: Temperature humidity and bias.
UV	: Ultra-violet.
Vcs	: CS voltage.
Vd	: Drain voltage of FET.
Vdd	: Drain voltage of MOS IC.
Vdsat	: Drain saturation voltage of FET.
VIL(H)	: Low (high) level input voltage - input voltage when set for a logic 0(1) level.
VLSI	: Very large scale integration.
VMOS	: V-grooved MOS.
VOL(H)	: Low (high) level output voltage - output voltage when set for a logic 0(1) level.
Vss	: Source voltage of MOS IC.
VWE	: WE voltage.
WE	: Write enable.
XPS	: X-ray photoelectron spectroscopy.

1. INTRODUCTION

The semiconductor device industry is approximately 30 years old. Integrated circuit (IC) manufacturing was started about 20 years ago and by 1961 ICs were made available commercially. Since then, reliability, speed of operation and production yields have steadily improved while cost, power consumption and size have been reduced drastically in particular for both bipolar transistors and metal oxide semiconductor field effect transistors (MOSFETs). The term "MICROELECTRONICS" was introduced to designate the high density IC devices. The discrete transistor was introduced in 1951, small scale integrated (SSI) circuits (less than 100 components per chip), medium scale integrated (MSI) circuits (more than 100 and less than 1000 components per chip), large scale integrated (LSI) circuits (more than 1000 and less than 10,000 components per chip) and very large scale integrated (VLSI) circuits (more than 10,000 components per chip) were introduced in 1960, 1966, 1969 and 1975 respectively [1]. In order to appreciate the concepts used in this thesis, it is necessary to consider the basic elements of a microelectronic device.

A cross sectional view of a device in a dual-in-line (DIP) hermetically sealed package and a DIP plastic encapsulated package is shown in figures 1.1 and 1.2

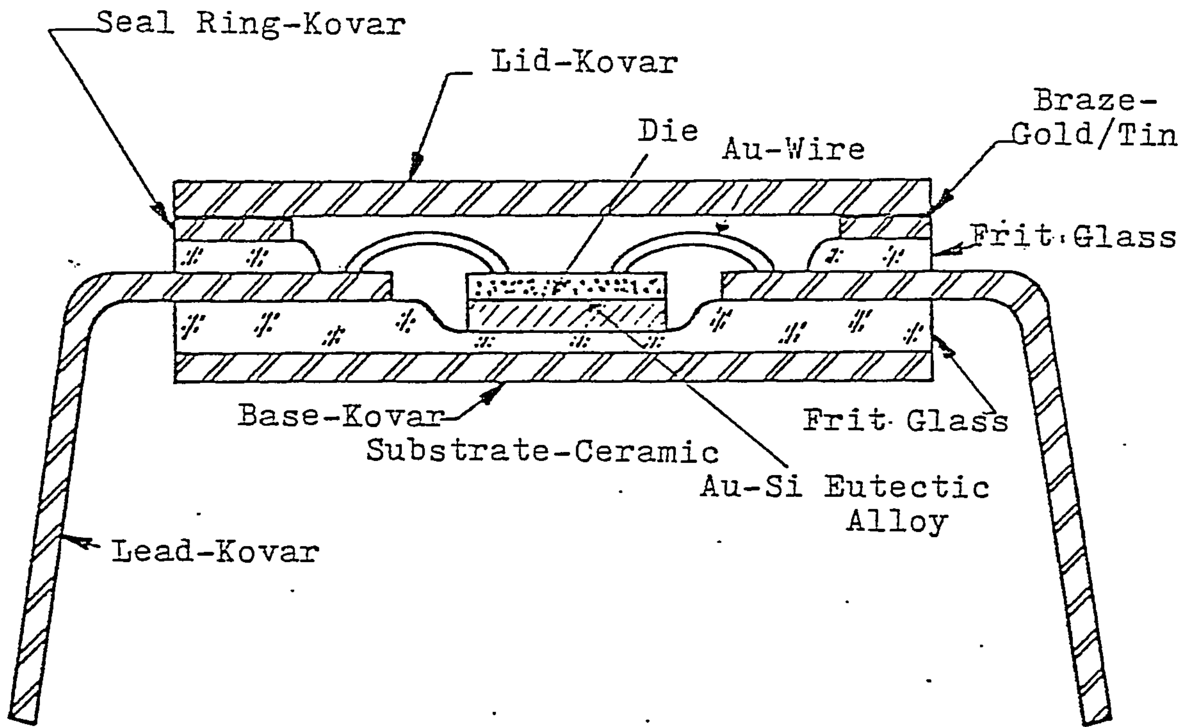


Figure 1.1 Cross section of hermetically sealed device.

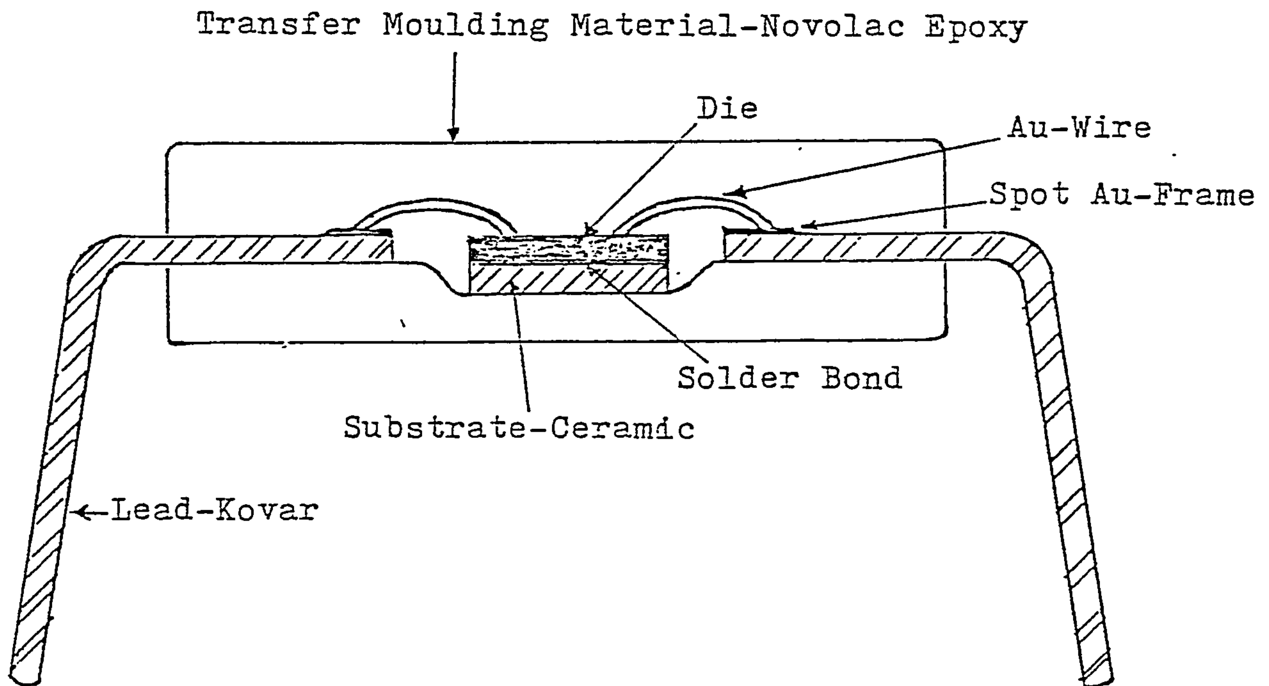


Figure 1.2 Cross section of plastic encapsulated device.

respectively. The basic device consists of the following parts.

(1) Leads.

(2) Lead frames.

(3) Encapsulation or package.

(4) Passivation.

(5) Bonding wire.

(6) Die, consisting of

  (a) Metallization.

  (b) Dielectric layer (in case of MOS devices).

  (c) Silicon base.

(7) Substrate.

The device may have flat, axial or dual-in-line (DIP) type of leads. The number of leads and the materials used for leads and plating vary from device to device depending on the use environment and device complexity (component density and function).

The device package may be either plastic or hermetically sealed. A variety of device package materials are available in the market. In plastic package types, silicone, silicone epoxy, epoxy novalac, epoxy anhydride etc., are available. Hermetically sealed packages may be available in many combinations of alloys and metals as can

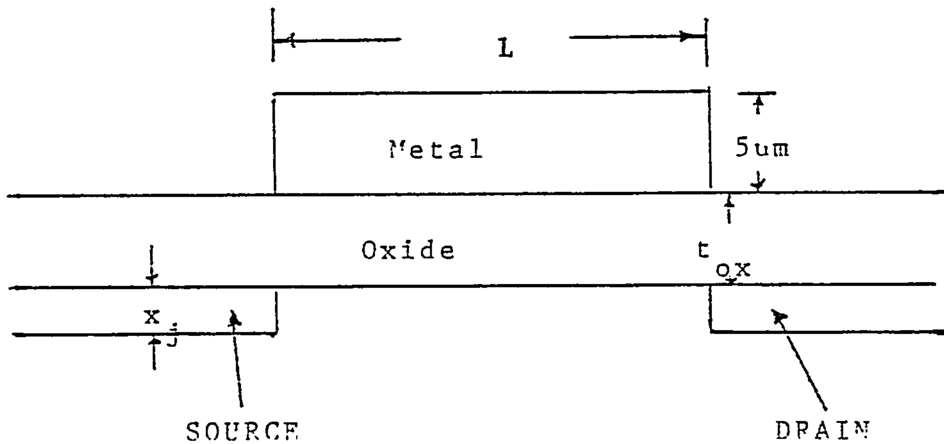
be seen in figure 1.1. Silicon dioxide, silicon dioxide + phosphorous, silicon nitride or polymide can be used for passivation to protect the top layer of the chip.

The bond wire to connect the lead frames to the die can be either Al, Au or even cu. Metallization can be either Al or a bimetal (a combination of two metal layers) or a trimetal (a combination of three metal layers). The dielectric layer can be silicon dioxide, silicon dioxide + phosphosilicate glass (PSG), silicon dioxide + Cl, silicon dioxide-silicon nitride or silicon dioxide-aluminum trioxide. The substrate can be ceramic or in some cases a metal. In the case of SOS (silicon-on-sapphire) process, silicon is deposited over sapphire substrate. In addition the device has interconnection (lead frame to bond wire, bond wire to die) bonds and an interlayer (silicon-substrate) bond.

There is very little standardization in the IC industry regarding the components produced. Different manufacturers are using different materials and technologies. The most popular is the planar technology and the SOS is the most recent development. The epitaxial growth process has been almost replaced by vapour deposition and/or ion implantation techniques because of their added advantages over the epitaxial growth process. Masking and etching techniques also vary from manufacturer to manufacturer. This variation

is the outcome of the continuing emphasis on the device reliability and miniaturization. Figure 1.3 shows the typical dimensions of N-channel metal oxode semiconductor (NMOS) and high performance metal oxide semiconductor (HMOS) devices [3].

Reliability engineering has become a distinct branch of technology with its own methods, literature and schools. The inputs to the present approaches commenced about 1949 or 1950. The activity in regard to semiconductor discrete devices has largely saturated while activity in the area of microelectronic devices is continuing to accelerate due to the dynamic nature of microelectronic device technology.



	NMOS	HMOS
L	6.0µm	3.0 µm
t_{ox}	1100 Å	700 Å
x_j	1.7 µm	1.0µm
Voltage	+5.0V	+5.0V
Metal line width	5 µm	5 µm

Figure 1.3 Typical dimensions of NMOS and HMOS Devices.

Reliability engineering is the technology of prediction, control, measurement, reporting and analysis of failure phenomenon and failure rates [2]. Obviously such a broad definition includes much that has been traditional in engineering design, manufacturing, quality control and service report. The basic approach used to achieve adequate reliability varies from discipline to discipline. This thesis is concentrated on electronic devices and particularly those designated as microelectronic components.

Reliability evaluation of electronic devices is related to the analysis of the actual materials used for device fabrication. Reliability evaluation of electronic equipment is related to the analysis of the actual components used in the manufacture of the equipment. Electronics can be generally described as the science and technology of the passage of charged particles in a gas, in a vacuum or in a semiconductor and electrical engineering is the field which deals with devices that depend solely on the motion of electrons in metals [1]. Electronics is normally associated with small components, small currents and voltages and reliability techniques have been developed to consider these aspects in the evaluation. Microelectronic devices are usually extremely complicated and therefore their evaluation should be considered as a separate area which warrants a sophisticated reliability evaluation program.

The basic theory of the reliability evaluation of microelectronic devices and practical work done by industries like RCA, Intel, Harris, Bell-Laboratories, Bell-Telephone laboratories, Texas instruments etc., in this area are presented in Chapters 2 to 7. A total reliability evaluation program for 4K complementary metal oxide semiconductor (CMOS) memory devices is given in Chapter 8. A cost analysis and reliability test facility plan is presented in Chapter 9 to aid research organizations and particularly universities which are interested in setting up such facilities.

2. FAILURE MODES AND FAILURE MECHANISMS OF MICROELECTRONIC DEVICES

The eventual failure of a device is inevitable. It is, however, possible to minimize the susceptibility to failure of a device. The likelihood of failure depends on the design, fabrication, circuit manufacture, degree of testing and screening, and on the actual application. Device failures can be categorized as catastrophic, degradation or soft.

A catastrophic failure is defined as the non-recoverable failure of a device in such a manner as to place one or more of its vital parameters more than 100% outside the minimum or maximum specified values. "Opens", "shorts" and "non-operation" of a device are examples of catastrophic failures.

A degradation failure is defined as the non-recoverable failure of a device in such a manner as to place one or more of its vital parameters outside the minimum or maximum specified values due to time degradation of the device.

A soft failure is defined as the recoverable failure of a device in such a manner as to place one or more of its vital parameters outside the minimum or maximum specified values due to random non-recurring defects.

Two most important terms associated with failure of a device are, (a) failure mechanism and (b) failure mode.

The failure mechanism is defined as the process of degradation or the chain of events which results in a particular failure mode. The failure mechanism is the fundamental physical or chemical or physio-chemical process responsible for a particular failure mode.

Similarly, the failure mode is defined as the abnormality of a device performance which causes the device to be classified as failed. The failure mode is an electrical or mechanical manifestation of a failure.

Many of the processing steps, materials, and construction features are common to both metal oxide semiconductor (MOS) and Bipolar IC's and therefore many of the possible failure mechanisms that have been reported so far apply to both types of devices. In order to better understand the failure modes and failure mechanisms of microelectronic devices, some important failure modes and associated mechanisms are discussed here. Soft failure mode is described in Section 2.1 and catastrophic and degradation failure modes are described in Sections 2.2 to 2.11.

2.1 Soft failure mode

Soft failures are random and non-recurring and are significant in random access memory (RAM) devices. The major findings are that soft failures in terms of change of state of a memory cell usually occur to a specific bit of a given RAM chip and that the location of the bit varies randomly from chip to chip [4]. In the case of a dynamic RAM , soft failure can only occur to a memory cell storing '1' or charged as shown in Figure 2.1 [93], while in the case of a static RAM, the soft failure can occur to a memory cell storing '1' or '0' because of the change in voltage levels. The magnitude of the problem in a static RAM is about an order lower than that in a dynamic RAM [4].

Soft failures are initiated mostly by Alph-radiation emitted by uranium and thorium within the package of the device because of its high radiation energy (3.95 Mev to 9.0 Mev). Plastic and metal lidded ceramic packages have Alpha-fluxes at the 0.1 $/cm^2$-hr level or below and Cerdip packages have at the 0.1 to 1.0 $/cm^2$-hr level. Hermetic packages induce more soft failures than plastic packages [5]. Even though a cosmic radiation effect is not completely dismissed, beta and gamma sources are not expected to produce soft failures because of low energy exposure rates in silicon.

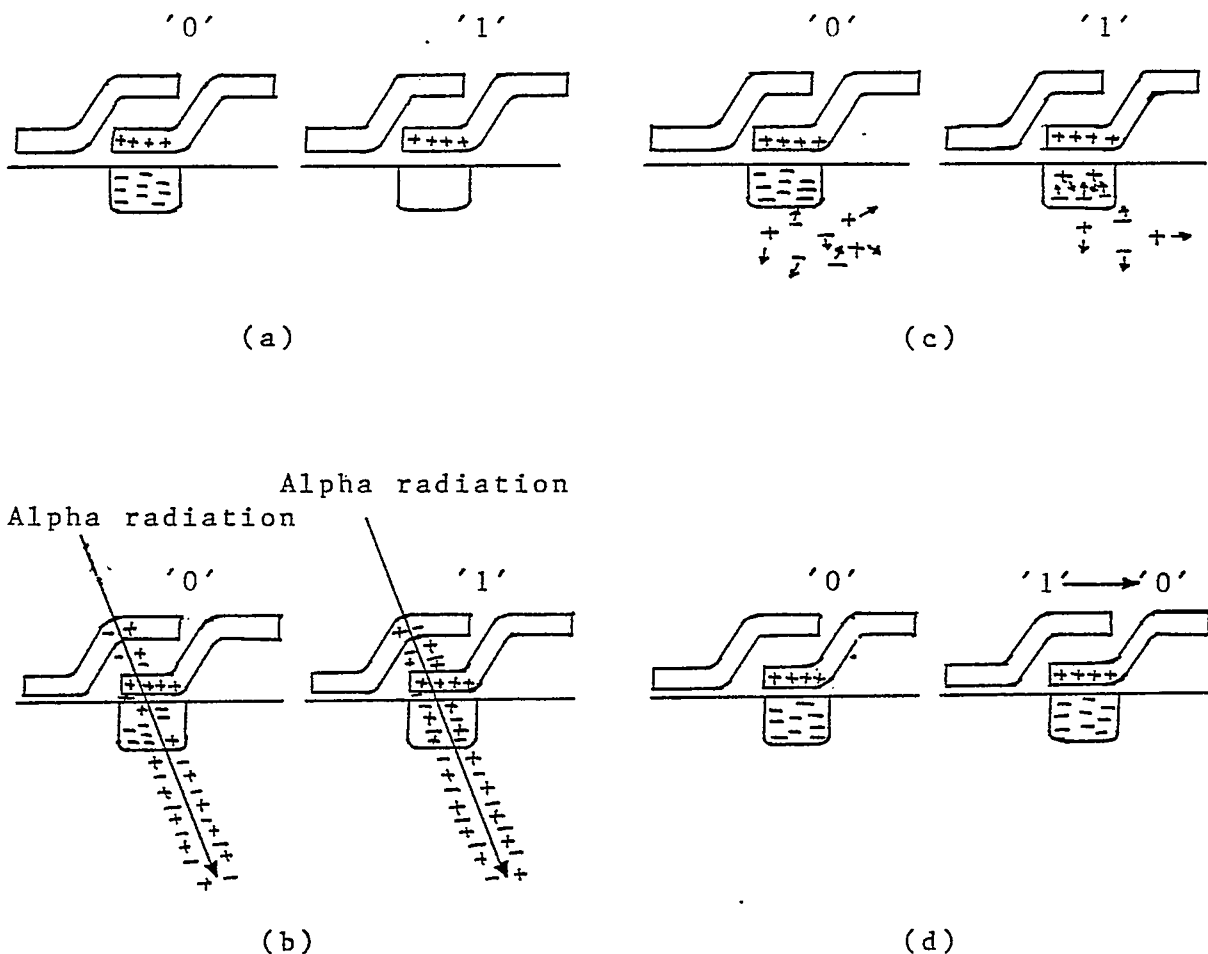


Figure 2.1 Stages of soft failure creation by alpha particles in dynamic memory devices. (a) '0' cell - potential well filled with electrons (P-type silicon in inversion) and '1' cell - potential well empty (P-type silicon in deep depletion). (b) Generation of electron-hole pairs in both the cells due to alpha radiation. (c) Electron-hole pairs generated diffuse, electrons reaching depletion region are swept by electric field into the well and holes are repelled. (d) '0' cell - potential well remains filled (no appreciable collection) and '1' cell - potential well now filled with electrons.

An alpha particle with 3.6 e.v is sufficient to create an electron-hole pair in most of the semiconductor devices. Up to 2.5×10^6 electron-hole pairs can be generated in a period of several picoseconds by the passage of the naturally occuring Alpha-particle. It is interesting to note that even a relatively low Alph flux such as 0.01 $/cm^2$ -hr could be enough to produce soft failures. The actual soft failure rate of a particular test structure or actual device depends on the flux and energy of ionizing radiation, target area, critical charge, collection efficiency, cell geometry etc. Soft failure rate also increases with increase of oxide thickness. Soft failure rate is more at low voltage difference between the states (static RAM) or at low critical charge (dynamic RAM, charge coupled device (CCD) etc.) than at high voltage difference between the states or high critical charge. If the device has a critical charge more than 2.5×10^6 electrons, no soft errors are expected. If the voltage difference between the low level of the high state and high level of the low state is sufficiently large, no soft failures in static RAMs are expected. Certain static NMOS RAMs suffer due to soft failures particularly when operated in a low supply voltage battery backing retention mode.

The refresh time for dynamic RAMs and the critical operational supply voltage at which the memory cell of a static RAM flips from '1' to '0' and vice versa may be used

to screen soft failures. 16K RAMs with soft failure rates greater than $10{,}000 \times 10^{-8}$ failures/hr are reported to have been sold in the market [6]. Since it is difficult to purify the package material used, the most promising area for reducing the soft failure rate is to reduce the device sensitivity to Alph-radiation through change in design and technology.

2.2 Charge loss/gain

Charge storing devices such as dynamic RAM, CCD, erasable programmable read only memory (EPROM) and rewritable avalanche injection device (RAID) are susceptible to this mode. Charge loss or gain in these devices is accelerated by electric field and temperature. Among the above devices EPROM and RAID are observed to fail in the long run due to charge loss/gain.

EPROM or RAID devices use essentially the floating-gate avalanche-injection metal oxide semiconductor (FAMOS) technology. The memory cells are programmed either by storing charge or no charge. The charge stored on the floating gate tends to flow towards the access gate or substrate leading the floating gate to lose charge, because of the increase in electric field towards the access gate and substrate. However, in case of another cell storing no charge, its floating gate slowly acquires charge from the substrate making the cell ultimately turn on.

Threshold voltage and conductivity between drain and source measurements in single devices like FAMOS reveal this failure mode. However, in case of LSI devices (EPROM and RAID) leakage current and functional tests reveal this failure mode. The failed devices due to charge loss or gain are recoverable once the devices are recharged or programmed after erasure.

2.3 Breakdown due to electrostatic discharge

Two sources of static electricity have been identified as the primary cause of dielectric breakdown of MOS devices and localized thermal run-away (second breakdown) leading to silicon melting of bipolar devices. First, the charge stored on the operators body is discharged through the device to the ground and second, the charge on the device itself is discharged to ground through one of the terminals.

The electrostatic discharge from a person's body results in a rapidly decaying current pulse with a peak value of current dependent on the initial voltage and effective resistances. The rate of pulse decay depends on the resistance and capacitance values of the human body. Electrostatic voltages measured in 15% to 36% RH under different conditions of laboratory operations ranged from 500 volts to 39,000 volts and 88% of the laboratory workers examined had charge accumulation of up to 1500 volts [7].

The human body capacitance was found to vary from 80 pF to 1000 pF [8, 9] and human body resistance to be a strong function of the potential used to measure it. For experimental purposes, different investigators have used capacitances between 60 pF to 300 pF and resistances between 1K ohm to 2k ohm and typical human body discharge voltages selected varied from 500 volts to 5000 volts.

For MOS devices the gate input is equivalent to a small, low leakage capacitor (5 pF typical, in parallel with a very high resistance (10^{12}ohms typical) and the field required for gate oxide breakdown to occur varies from $2x10^6$ volts /cm to 10^7volts/cm depending on oxide defects [9]. For an oxide thickness of 1000 ^oA, the static discharge voltage above 20 volts is harmful. In view of this, particularly in the case of HMOS devices, the oxide thickness scaling can not be continued below 700^oA because the oxide defects like pin holes and cracks play a significant role to cause dielectric breakdown to occur at normal supply voltages or electrostatic voltages. The failure is mostly an oxide short.

In the case of bipolar devices the emitter-base junction is more susceptible to damage by electrostatic discharge particularly when the base is negatively biased and the emitter either positively biased or left open. If the voltage drop across emitter-base junction exceeds

BV_{EBO} (about 8 volts) breakdown occurs due to thermal runaway leading to silicon melting. Low current gain (h_{FE})is sensitive to emitter junction damage. The failure is mostly parameter degradation.

The damage of bipolar and MOS devices due to electrostatic discharge is avoided through design modifications using protection networks employing, (a) Diodes, (b) Transistors, (c) Spark gaps, and (d) V-grooved metal oxide semiconductor (VMOS) devices [10] or (e) a combination of these devices. An ideal protection network should respond to fast and very slow rise time pulses and effectively clamp the gate voltages (MOS) or emitter-base (bipolar) voltages to ground before damage to the device can occur. The protection network should not degrade normal operation of the device and should be compatible with conventional processing parameters and design constraints. The breakdown voltages of the devices used in protection networks should be few orders less than the breakdown voltage of the actual device.

On the other hand, the breakdown voltages of the device can be improved by tight screening and process improvements. 5% HCl during oxidation for MOS devices is reported to have increased the oxide yield and breakdown stress. The improvements are likely due to a reduced generation rate of oxide defects under a high field stress condition.

2.4 Corrosion

Die metallization, bond pads, leads and bond wires are susceptible to corrosion. Moisture and contamination constitute the electrolyte and bias acts as the driving force to initiate corrosion. The moisture and contamination for corrosion of internal metal parts of ICs enter either during device processing or penetrate through the package and passivation materials with time. It has been observed that moisture can penetrate the device with leak rates as low as 10^{-8} atm cc/sec [90] through the lead frame or through the package material from the surface. The encapsulating material itself is the source of contamination. Residual impurities during wafer processing, passivation and other device processing steps aid corrosion. Na^+, K, Hg, Cl and I are the most common contaminants that aid corrosion.

Corrosion can occur either in acidic or basic solutions. The phosphosilicate glass which is used to improve mechanical protection and electrical stability by reducing stresses and gettering alkaline ions respectively, acts to increase corrosion. The amount of water absorbed increases with the increase in phosphorus. Phosphorus oxide when reacted with water forms strong acids and hence increased hydrogen ions. The freed Na^+ ions from the PSG via ion exchange migrate to the cathode to cause corrosion [11, 12, 13]. Phosphorus content in the glass above 2% by weight