THE CADMIUM SELENIDE THIN-FILM TRANSISTOR

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David Henry Treleaven

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"THE CADMIUM SELENIDE THIN-FILM TRANSISTOR"

Student: D.H. Treleaven Supervisor: Professor A.C. Tickle

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ABSTRACT

A study of the properties of polycrystalline cadmium selenide semiconductor films has been undertaken as a part of the overall thin-film transistor research program in effect in the Department of Electrical Engineering at the University of Saskatchewan. The semiconductor has been considered throughout as a thin-film transistor component rather than a separate entity.

The properties of polycrystalline semiconductors in general are discussed utilizing comparison with the more familiar properties of single-crystal semiconductors. Specific properties of cadmium selenide are presented in detail. The most important characteristics of the silicon monoxide thin-film transistor insulator are mentioned. The conduction process in thin-film transistors is described including analysis of an incremental thin-film transistor section and of the entire device. Two small-signal equivalent circuits are included. The results of an investigation of the structure of polycrystalline cadmium selenide films by X-ray techniques are described. Important parameters of polycrystalline cadmium selenide films are determined from experimental results. Parameters for which a value is obtained are bulk semiconductor conductivity, bulk free electron concentration, effective electron mobility, surface density of interface traps, conduction channel thickness, and Fermi energy. Assumptions made, sources of error, and accuracy of values obtained are discussed.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF PRINCIPAL SYMBOLS

C_o = insulator capacitance per unit area

C_T = total insulator capacitance

E = electric field

E_i = electric field in insulator

E_s = electric field in semiconductor at semiconductor-insulator interface

E_A = acceptor energy level

E_c = conduction-band edge energy

E_D = donor energy level

E_F = Fermi energy level

E_G = forbidden band gap energy

E_I = ionization energy

E_v = valence-band edge energy

$f(E)$ = probability of occupancy of states at energy E

$G(V_g)$ = total channel conductance for $V_g = 0$

g = $(\text{resistance per unit length})^{-1}$

h = Planck's constant

I_d = drain current

K_i = dielectric constant of insulator

K_s = dielectric constant of semiconductor

k = Boltzmann's constant

L = source to drain length

L_c = effective conduction channel thickness

m_e = electron effective mass

m_h = hole effective mass

$N(E)$ = density of states per unit energy at energy E

N_c = effective density of states at bottom of conduction band

N_v = effective density of states at top of valence band

N_{ST} = surface density of charged traps

n = free electron density

n_o = free electron density in bulk semiconductor

$n(E)$ = electron density per unit energy at energy E

n_F = free carrier density

n_T = density of trapped carriers

n_{ca} = number of conduction electrons per unit area

n_{in} = number of field-induced electrons per unit area

n_{tot} = total number of electrons per unit area

p = hole density

q = charge on an electron

Q_s = surface density of negative charge

T = absolute temperature

t_i = insulator thickness

t_s = semiconductor film thickness

V = electrostatic potential

V_d = drain voltage with respect to source

V_g = gate voltage with respect to source

V_s = potential at semiconductor-insulator interface

V_T = threshold gate voltage necessary for the onset of conduction

V_∞ = potential at $z = \infty$

v_e = average drift velocity of electrons

v_h = average drift velocity of holes

$W(x)$ = voltage drop across insulator at a given x.

Z = semiconductor film width

ϵ_o = permittivity of free space

μ = effective electron mobility

μ_D = true drift mobility

μ_d = effective drift mobility

μ_e = drift mobility of electrons

μ_h = drift mobility of holes

I_{d1} = change in I_d due to change in t_s

I_{d2} = change in I_d due to change in V_g

1. INTRODUCTION

One of the major new technological concepts of the past decade was that on the integrated microelectronic circuit. The impact of integrated circuitry has been felt throughout the entire electronics industry. Prior to the advent of integrated circuits all electronic systems were made of discrete electronic components manually assembled with wire and solder. The integrated circuit has combined electronic components performing a definite function in a single unit, thereby reducing the number of packages that must be used to construct any given system by an order of magnitude. The inherent advantages in the integrated approach to system fabrication are smaller size, lower cost, and higher reliability. In a large number of applications the anticipated economic advantages of integrated circuitry have been realized.

Historically, the first type of integrated circuit to be employed commercially was the hybrid circuit. These circuits consisted of arrays of passive components, principally resistors and capacitors, on a single substrate, with transistors and diodes soldered in place by hand. Hybrid circuits utilized to a degree the advantages of the integrated approach and are in widespread use at the present time.

A major advance in integrated circuitry was the advent of the monolithic integrated circuit in which all components, active and passive, were confined to one substrate. The substrate used almost exclusively for commercial circuits was single crystal silicon. The technology employed was the well-established technology used in the fabrication of silicon transistors, employing such powerful and versatile tools as photolithography, solid-state diffusion, and epitaxial growth.

Complete circuits composed of resistors, capacitors, transistors and diodes could now be placed on a single substrate. The monolithic integrated circuit exhibited a number of distinct advantages over the hybrid. Because the operation of soldering of discrete components to the main substrate was omitted the labor cost associated with the monolithic curcuit as compared to the hybrid circuit was much lower. Reliability was substantially increased. Monolithic circuits of appreciable complexity could be constructed on very small silicon substrates. A packaged monolithic circuit was therefore much more compact than its hybrid equivalent. At the present time many commercial electronic systems have been fully converted to monolithic integrated circuits and many more are in the process of being adapted or redesigned so as to utilize the advantages of this powerful new technology.

The monolithic integrated circuit, like any other technological product, has its distinct limitations. These limitations arise from parasitic resistance and capacitance inherent in the circuit structure. The single-crystal silicon substrate is common to all transistors and diodes and introduces a conduction path between them. Because the resistance of the semiconductor is necessarily of moderate value, some method of isolating components operated at different potentials must be employed. The high resistance of reverse biased p - n junctions is usually used for isolation. These p - n junctions, however, do pass leakage currents that can be significant and also introduce parasitic junction capacitance to the circuit. Good isolation can be obtained by separating regions at different potentials with silicon dioxide

layers but the complicated fabrication procedures essential to this approach make it impractical for all but the most sophisticated circuits. Monolithic integrated circuits must always be designed within the limitations imposed by the isolation technique.

The ideal solution to the isolation problem is to construct circuits on an insulating substrate, thereby providing perfect isolation between circuit components. A promising approach in this direction at the present time is the formation of microelectronic circuits on an insulating substrate solely by vacuum deposition. Circuits of this type are known as thin-film integrated circuits. Techniques for fabricating resistors and capacitors by vacuum deposition are well established, being identical to the techniques used for fabricating the resistor and capacitor arrays used in hybrid integrated circuits. In the past few years techniques have been found that make it possible to fabricate field-effect transistors by vacuum deposition of thin layers of specific materials. These transistors are called thin-film transistors. Since thin-film rectifiers can be obtained by suitable biasing of thin-film transistors it can be seen that thin-film integrated circuits can be fabricated with as great a variety of components as monolithic integrated circuits.

Thin-film integrated circuits possess a number of attractive features in addition to the fact that they are constructed on insulating substrates. Except for packaging, the entire fabrication process takes place in one pump-down of a single vacuum system in a time of perhaps four hours. Both capital equipment and labor costs are therefore low. Circuit geometry is defined by evaporation through masks registered by

mechanical means from outside the system. Tolerances attained are within a factor of two of photolithographic tolerances used in commercial integrated circuits. The registration of masks as well as all other fabrication steps is well suited to automation. Because of these factors it can be seen that the thin-film approach to integrated circuitry possesses the potential of producing integrated circuits in extremely large quantities at extremely low cost.

The field-effect transistor fabricated solely by vacuum deposition, the thin-film transistor, is a relatively new semiconductor device, having first been reported in 1962. The characteristics of the thin-film transistor are similar to those of a small pentode vacuum tube, exhibiting characteristic high input impedance and high output impedance. The ratio of on to off conductance of the thin-film transistor is as large as 10^7, suggesting profitable application of thin-film transistors in switching circuitry. At the present time the theory of operation of the thin-film transistor is not nearly as well understood and generally accepted as that of the junction transistor. Fabrication techniques have not been standardized. Before thin-film transistors can be utilized in commercial applications the operation of these devices must be clearly understood.

This thesis will be concerned with the properties of polycrystalline cadmium selenide, a semiconductor widely used in thin-film transistor fabrication. Polycrystalline semiconductors are composed of a large number of discrete crystallites amassed in random orientation, as compared with single-crystal semiconductors in which nearly all the atoms are arrayed in a perfect, periodic crystal lattice. Single-crystal semiconductors are used for all transistors

and monolithic integrated circuits in present commercial use. The imperfect nature of the polycrystalline semiconductor must be accounted for in any complete theory of operation of the thin-film transistor.

To date the published work in the field of thin-film transistors has emphasized several distinct approaches. Theoretical papers on the operation of thin-film transistors have been published with little consideration of the properties of the materials comprising the device. Papers have also been published detailing observed experimental effects with insufficient theoretical explanation of those effects. Cadmium sulphide thin-film transistors have been reported more extensively than those employing cadmium selenide. Most of the fundamental work on cadmium selenide has been concerned with the properties of that material as related to the field of photoconductivity. A coordination of information pertaining to the properties of polycrystalline cadmium selenide as applied to thin-film transistors is desireable and is undertaken in part in this thesis. The main work reported here is the experimental determination of properties of the cadmium selenide films of the TFTs used by the author. This information is essential for an understanding of the operation of these devices, as well as being applicable to cadmium selenide thin-film transistors in general. It is hoped this thesis will make a worthwhile contribution to the understanding of the properties and operation of the thin-film transistor.

2. CHARACTERISTICS OF TFT'S

2.1 Introduction

Before embarking on a detailed development of specific topics concerning TFTs it is necessary to survey the essentials of TFT operation and construction. This approach, which will allow the following chapters to be placed in proper perspective, is particularly advisable in view of the specialized nature of the topic.

This chapter treats two topics. The first topic is a qualitative description of TFT operation. The general shapes of TFT characteristic curves are explained and transistor terminal symbols are defined. The second topic is a brief discussion of the technology employed in fabrication of TFTs in the thin-film laboratory in the Department of Electrical Engineering at the University of Saskatchewan, hereafter referred to as the thin-film laboratory. The materials used to form TFTs are listed and the techniques for their deposition under vacuum are summarized. The systems used for masking selected areas of substrate during deposition to form desired device geometries and for monitoring film thickness during evaporation are mentioned.

The purpose of this chapter, once again, is to provide a survey of the thesis subject so that the applicability and significance of the following, more detailed, chapters may be easily comprehended.

2.2 A Qualitative Description of TFT Operation

The TFT can be represented symbolically as shown in Figure 2.1 . The basic elements are an insulating substrate, a semiconductor layer, an insulator layer, and three electrodes. The insulating substrate

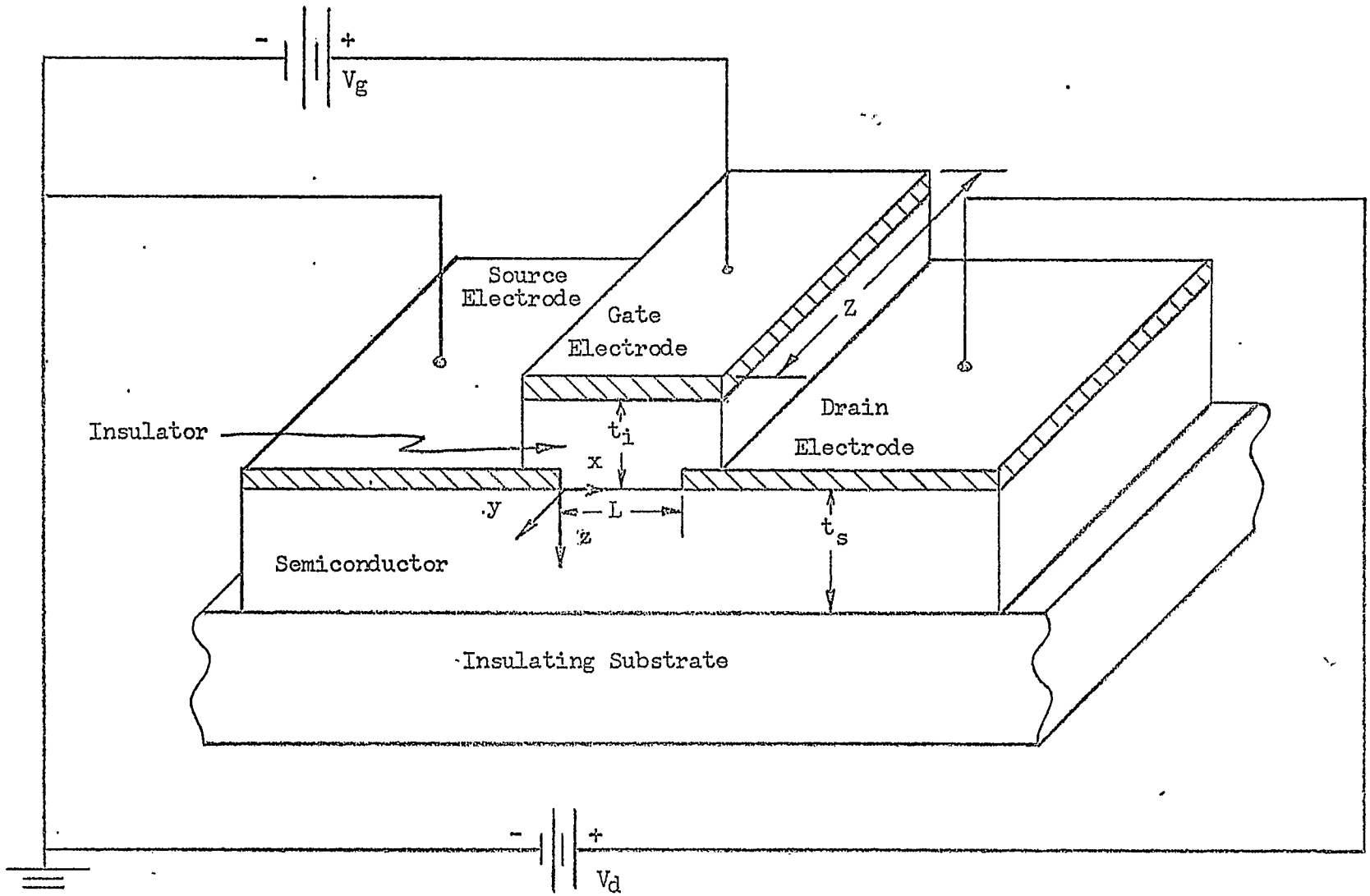


Figure 2.1 Symbolic Representation of TFT

provides excellent isolation between adjacent units and is one of the main advantages of this type of device. The semiconductor is chosen for suitable forbidden energy band gap and mobility, low surface state density, and ease of evaporation. The insulator must also be easily evaporated and a thin layer of this material must effectively isolate the top electrode from the semiconductor. The top electrode is termed the control gate or simply gate and the two lower electrodes are termed the source and the drain. The source electrode is conventionally considered to be at reference potential.

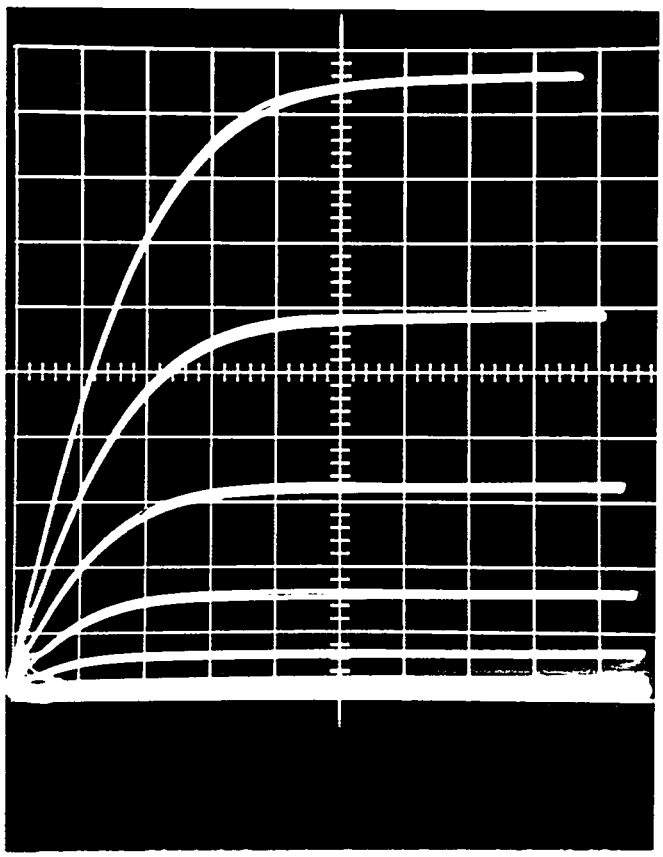
TFT operation may be qualitatively described with the aid of Figure 2.1 . Assume a small positive voltage, V_d, has been placed on the drain electrode. A current, I_d, will flow through the semiconductor from drain to source. Since the semiconductor is bounded by insulating layers this current will be constant across all cross-sectional areas between source and drain taken through the semiconductor perpendicular to the current flow. Assume, now, that a positive gate voltage, V_g, greater than V_d is placed on the gate electrode. The semiconductor will act like the plate of a capacitor with the insulator comprising the dielectric and the gate electrode the other plate. Electrons will be induced in the semiconductor by capacitive action and will accumulate close to the semiconductor-insulator interface forming a highly conductive channel between source and drain. As the number of induced electrons is a function of gate voltage, the resistance of the channel and therefore the channel current, I_d, may now be modulated by means of the gate voltage. An active electronic device has therefore been formed. Since, in this case, the application of V_g increased I_d

above its value at $V_g = 0$, the TFT is said to be in the enhancement mode of operation.

Conversely, if a negative voltage, V_g, is impressed on the gate, conduction electrons existing in the bulk semiconductor will be drawn from the semiconductor resulting in decreased semiconductor conductance and decreased I_d. I_d still may be modulated by means of V_g. Since the application of V_g has reduced the value of I_d below its value at $V_g = 0$, the TFT is now said to be in the depletion mode of operation.

Consider, now, the situation if a TFT is biased such that V_d is greater than V_g, both voltages being positive. Note that the polarity of the value $(V_g - V_d)$ is different at the source and drain electrodes. An accumulation layer of electrons will exist in that portion of the semiconductor from the grounded source electrode to the point where the electron-inducing electric field perpendicular to the semiconductor-insulator interface falls to zero and reverses. Between this field-reversal point and the drain electrode exists a high resistance section of semiconductor. Under these conditions the conduction channel is said to be pinched off. I_d is virtually independent of V_d when the conduction channel is pinched off and I_d is thus said to be saturated in the pinch-off region of operation.

The foregoing arguments explain qualitatively the shapes of the observed TFT characteristic curves shown in Figure 2.2 . The modulation of I_d by V_g and the onset of saturation are clearly visible. The TFT used to obtain the characteristic curve of Figure 2.2 was one of a standard fabrication lot produced in the thin-film laboratory. The photograph was taken on a Tektronix 575 Curve Tracer.



I_d 0.1 ma/division

V_d 1 volt/division

V_g + 1 volt/step, 9 steps

V_T + 4 volts

Fabrication lot 100

Unit 41

Figure 2.2 Photograph of TFT Characteristic Curves

2.3 Device Fabrication Techniques

The TFTs fabricated in the thin-film laboratory are vacuum deposited in the Varian VI - 4B High Vacuum Evaporator shown in Figure 2.3 . Standard vacuum deposition techniques are used (Holland, 1961). A standard fabrication lot consists of a series of 45 TFTs deposited onto a glass substrate as pictured in Figure 2.4 . Aluminum is used for all electrodes because of high conductivity, ease of evaporation, and because it readily forms an ohmic contact with the semiconductor (Holland, 1965). Cadmium selenide comprises the semiconductor and its properties are treated in detail in Chapter 3. The insulator material, silicon monoxide, is further discussed in Chapter 4.

A simple and versatile masking system is used to control TFT geometry (Tickle, 1966). This system permits control of multiple variables during one deposition run thereby providing substantial freedom in the design of experiments. Film thicknesses are monitored electronically during deposition by means of a Sloan Instruments DTM - 2a Deposit Thickness Monitor. This instrument measures the characteristic frequency shift of a quartz crystal as the deposited film alters the mass of the crystal, making possible indicated film thickness control to within 10 angstroms. An interference microscope was used to calibrate the film thickness monitor. The temperature of the substrate during deposition is controlled by means of resistance heaters located along the back side of the substrate. Five thermocouples for sensing substrate temperature are placed in contact with the substrate at regular intervals along the back of the substrate. The maximum difference between any two thermocouple readings is held within 20°C for aluminium and silicon monoxide deposition and within 10°C for cadmium selenide.

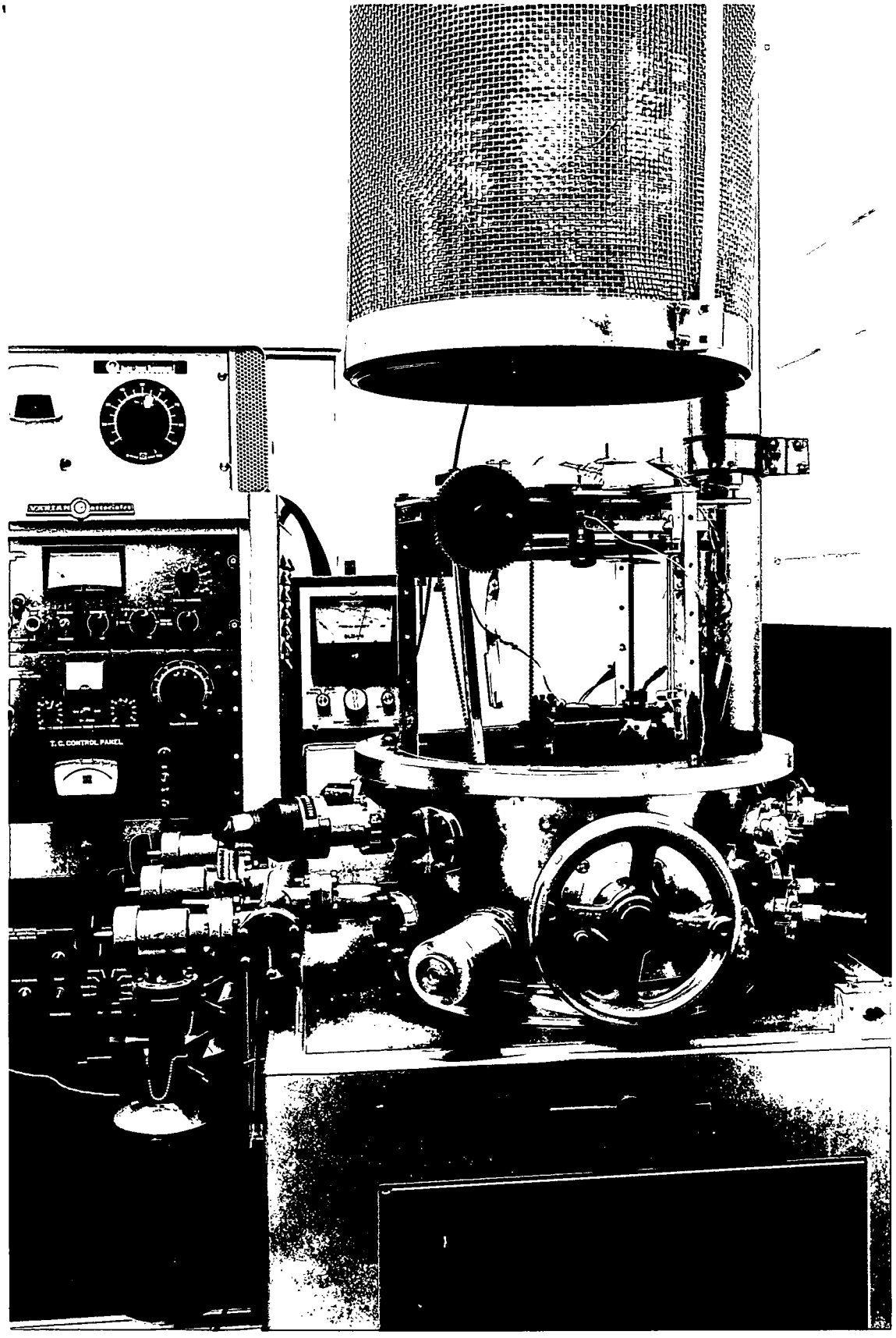


Figure 2.3 Photograph of Vacuum Deposition System and Control Panel

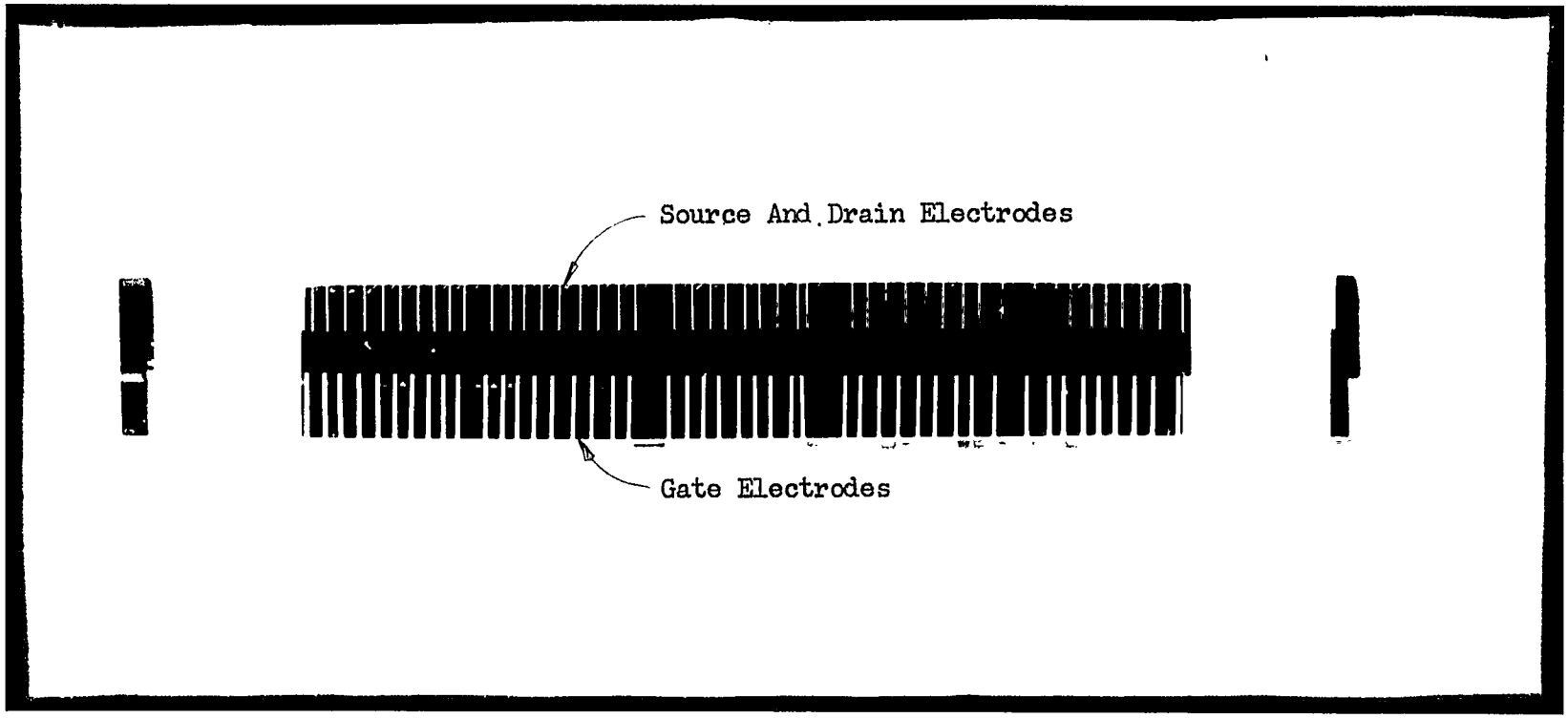


Figure 2.4 Photograph of Fabrication Lot of TFTs

The vacuum deposition techniques and parameters used in the thin-film laboratory are summarized in Table 2.1 . The success of these techniques is clearly demonstrated by the quality of the TFT characteristic curves of Figure 2.2 .

Parameter	Al	Cd Se	SiO
Deposition Rate	200 Å / min.	10 Å / min.	30 Å / min.
Type of Source	Resistance Heated Tungsten Boat	Baffled Box	Drumheller
Pressure	$< 10^{-5}$ torr	$< 5 \times 10^{-6}$ torr	10^{-4} torr
[a] Substrate Temperature	$100 \pm 10\ ^{\circ}C$	$100 \pm 5\ ^{\circ}C$	$100 \pm 10\ ^{\circ}C$
Typical Thickness	200 Å	240 Å	450 Å

a Denotes indicated temperature

Table 2.1 Vacuum Deposition Parameters

3. THE SEMICONDUCTOR

3.1 Introduction

The semiconductor used in TFT fabrication in the present work is polycrystalline cadmium selenide. Polycrystalline semiconductors in general are composed of numerous individual crystallites amassed with limited or negligible order. The random nature of such a solid material is in direct contrast to the structural perfection of single semiconductor crystals in which nearly all of the atoms are arranged in perfect, repeating, geometrical order. In this chapter, single crystal semiconductors will first be described. This description will then be expanded to include polycrystalline semiconductors and finally the specific properties of polycrystalline CdSe will be discussed. The above approach is a logical one for a number of reasons. The theory of single semiconductor crystals is well-established and comparatively simple and is a natural starting point. Polycrystalline semiconductors in general can most easily be described by comparison to single crystal semiconductors. The specific properties of polycrystalline CdSe, which apply directly to the TFTs under consideration, can then be presented in detail. A special effort has been made to include in this chapter only general material essential to the development of the subject. Emphasis has been placed on specific topics that contribute significantly to an understanding of the operation of the TFT.

3.2 Single Crystal Semiconductor

A solution of the problem of wave propagation or particle motion

in certain types of periodic structures, including semiconductors, yields a solution consisting of allowed bands of energy separated by unallowed bands. This result leads to the widely used energy band concept of semiconductors, the essential results of which are stated here.

The energy band model of a semiconductor is represented for a pure crystal in Figure 3.1 by a series of closely spaced energy levels which at a temperature of absolute zero are filled to an energy E_V, called the valence-band edge. Above the energy E_V, lies the forbidden gap, a region of energy width E_G in which, for perfect crystal, there are no allowed energy levels. Heat energy in the form of lattice vibrations or light of proper wavelength can break interatomic bonds in the crystal and thus excite electrons from the valence band, below the energy E_V, into the conduction band, above the energy E_C. This situation is illustrated in Figure 3.1 by circles representing holes in the valence band and solid circles representing electrons in the conduction band. In diagrams such as Figure 3.1 increasing energy for electrons is upwards, for holes downwards. In actual single semiconductor crystals the ideal situation of Figure 3.1 is not realized and a few energy states may exist in the forbidden gap. These energy states arise because of crystal imperfections and their origin and role in the conduction process will be considered in detail later.

In order to utilize the energy band picture in analysis it is necessary to know the distribution in energy of states where an electron may possibly reside and the probability of occupancy of those states.

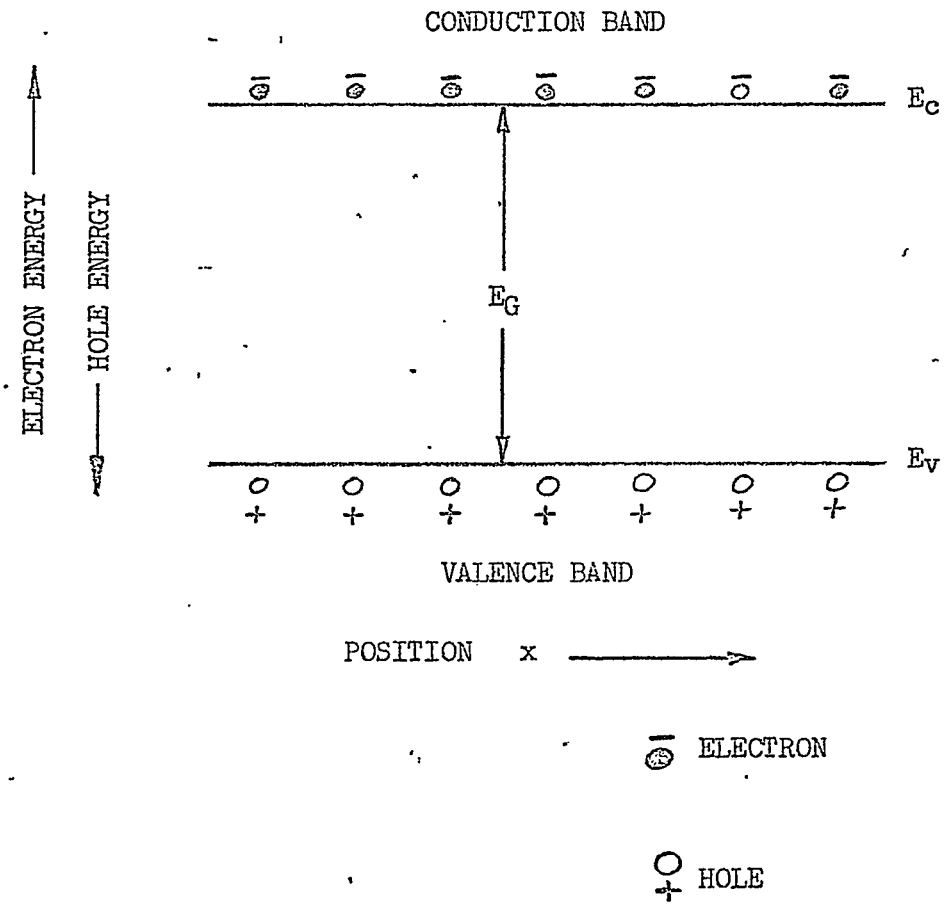


Figure 3.1 Energy Level Diagram of Perfect Crystal, $T > 0\,^{\circ}K$

Mathematically,

$$n(E) = N(E)\, f(E) \tag{3.1}$$

where $n(E)$ = electron density at energy E in number per unit volume per unit energy

$N(E)$ = density of states at energy E in number per unit volume per unit energy

$f(E)$ = probability of occupancy of states at energy E.

$f(E)$ is given by the Fermi-Dirac distribution function,

$$f(E) = \frac{1}{1 + \exp\left[\dfrac{E-E_F}{kT}\right]} \tag{3.2}$$

where E_F = Fermi energy level

k = Boltzmann's constant

T = absolute temperature.

The properties of $f(E)$ are easily summarized:

(1) for $E - E_F \ll -kT$, $f(E) \simeq 1$, signifying that nearly all such states are filled;

(2) for $E = E_F$, $f(E) = \frac{1}{2}$, showing that the location of the Fermi level marks the level where the occupation probability is $\frac{1}{2}$;

(3) for $E - E_F \gg kT$, the Fermi-Dirac distribution reduces to the classical Boltzmann distribution,

$$f(E) = \exp - \left[\frac{E - E_F}{kT}\right] . \tag{3.3}$$

It can be shown (e.g. Adler, et al, 1964) that if the Fermi level is a few $\dfrac{kT}{q}$ below E_c, which will almost always be the case in practice, the total number of electrons per unit volume in the

conduction band is given by the equation

$$n = N_c \exp - \left[\frac{E_c - E_F}{kT}\right] \tag{3.4}$$

where $N_c = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{3/2}$

m_e = effective mass of an electron

h = Planck's constant.

A similar expression can be derived for the total number of holes in the valence band.

$$p = N_v \exp - \left[\frac{E_F - E_v}{kT}\right] \tag{3.5}$$

where $N_v = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{3/2}$

m_h = effective mass of holes.

The additional energy levels, mentioned earlier, which may exist in the forbidden band gap are associated with the presence of structural defects in a crystal such as vacancies, interstitials, and dislocations. Vacancies are unoccupied lattice sites, interstitials are atoms localized between lattice sites, and dislocations are line defects arising from imperfect matching of adjacent crystal planes. Wherever the perfect periodicity of the crystalline structure is disturbed, it is possible for electrons to take on energies which are forbidden in the perfect crystal. The presence of a defect can introduce one or more energy levels in the forbidden gap (Bube, 1960). Unlike the bands themselves, which extend throughout the crystal, the additional levels are localized at the crystal defect. Interfaces between different materials can be considered as extended crystal defects. Structural defects of all kinds often act as traps or recom-

bination centers in semiconductor crystals (Bube, 1960).

The subject of trapping and the effect of traps is extremely important in considering any semiconductor device. Trapping is a fundamental process in almost all electrically active solids and involves the spatial localization of an activated electron or hole, in such a way that the electron or hole is prohibited from moving freely through the crystal unless supplied with thermal or optical energy. When the trapped electron or hole is released, it is free to move until recaptured by another trap. Those regions of the crystal which are able to capture electrons and holes, and detain them in a restricted volume, are called traps.

The difference between traps and recombination centers must be made clear. It has become common practice in semiconductor technology to refer to any center capable of capturing an electron or hole as a trap. In this thesis a capturing center will be denoted as a trapping center if the captured carrier has a greater probability of being thermally re-excited to the free state than of recombining with a carrier of opposite sign at the imperfection, and a recombination center if the probability of recombination with a carrier of opposite sign is greater than the probability of being thermally re-excited to the free state. Because of this definition there is an inherent vagueness in determining what type of centers are traps. A center can be a trap under one set of conditions and a recombination center under another set of conditions. As this chapter becomes specific it will be seen that this problem is not a serious one and that the role of traps dominates over the role of recombination centers for CdSe, the semi-

conductor of special interest here.

The concept of carrier mobility is essential to an understanding of the conduction process in any semiconductor. The mobility of holes may be defined as follows:

$$\overline{v_h} = \mu_h \overline{E} \tag{3.6}$$

where $\overline{v_h}$ = average drift velocity of holes

$\overline{E}$ = electric field

μ_h = drift mobility of holes.

The mobility of electrons may be defined in a similar manner.

$$\overline{v_e} = -\mu_e \overline{E} \tag{3.7}$$

where $\overline{v_e}$ = average drift velocity of electrons

μ_e = drift mobility of electrons.

The minus sign appears in equation (3.7) to account for the negative charge on electrons. Mobility is a measure of the ease of movement of carriers through the semiconductor under consideration. This ease of movement is decreased by scattering, the deviation of carriers from straight-line motion. There are two important scattering mechanisms, lattice scattering and ion scattering.

Lattice scattering arises from interaction between carriers and the atoms of the crystal lattice. These interactions may be loosely thought of as collisions. As the temperature rises the amplitude of vibration of the lattice atoms increases due to increased thermal energy, resulting in increased lattice scattering and decreased mobility.

Ion scattering arises from coulombic interactions between carriers and any immobile electric charges that may exist in the crystal.

Charged traps are a common source of ion scattering. As the temperature rises the mean velocity of the carriers increases, decreasing the deflecting effectiveness of immobile ions. Mobility increases with temperature due to this effect. The question of which scattering mechanism, lattice or ion, dominates carrier mobility in a crystal at any given temperature must be solved for the individual case.

In a semiconductor containing a significant number of traps, the concept of effective mobility is frequently employed (Weimer, 1962).

$$\mu_d = \mu_D \frac{n_F}{n_F + n_T} \tag{3.8}$$

where μ_d = effective drift mobility in presence of traps

μ_D = true drift mobility (mobility in perfect crystal)

n_F = free carrier density

n_T = density of trapped carriers.

Effective mobility is a convenient device to take into account carriers held immobile in traps. The concept of effective mobility is especially important to the consideration of polycrystalline semiconductors in which densities of imperfections are high.

3.3 Polycrystalline Semiconductor

A polycrystalline material consists of a large number of small crystals, or crystallites, assembled together to form a stable solid. The atomic structure within each of these crystallites is single crystal but the orientation of the lattices of the crystallites may vary considerably throughout the material. The interfaces between crystallites or grains are called grain boundaries.

The state-of-the art of the theory describing polycrystalline semiconductors has not yet approached the level of sophistication of the accepted body of theory describing single-crystal semiconductors.

An analysis of electron mobility in polycrystalline CdS films has been performed (Waxman, 1964) utilizing the polycrystalline semiconductor film model shown in Figure 3.2 . The main feature of this model is the presence of regions of different conductivity existing throughout the semiconductor. The energy band variations shown in Figure 3.2 illustrate the variations in free electron concentration and associated energy barriers between the regions of different conductivity proposed in the model. The regions of different conductivity could conceiveably arise because of variations in stoichiometry, adsorbed surface species, grain boundaries, or internal stress effects. For example, stress effects can cause variations in bandgap (Waxman, 1964) and grain boundaries provide preferred locations for traps (Bube, 1960) resulting in low effective mobility of carriers and a corresponding reduction in conductivity. The concept of a polycrystalline semiconductor pictured in Figure 3.2 is at best a first approximation but is useful as a descriptive model, particularly when used in conjunction with knowledge obtained from empirical results.

For the purpose of this thesis, the polycrystalline semiconductor of main interest has the geometric form of a thin evaporated film. The formation of such films has been carefully observed by electron microscope techniques and fully documented (e.g. Pashley and Stowell, 1966). The general system to be considered consists of a source of semiconductor atoms or molecules and a substrate upon which the film is to grow.

Of the first atoms to reach the substrate, some will adhere to the substrate and some will re-evaporate. Those atoms that adhere to

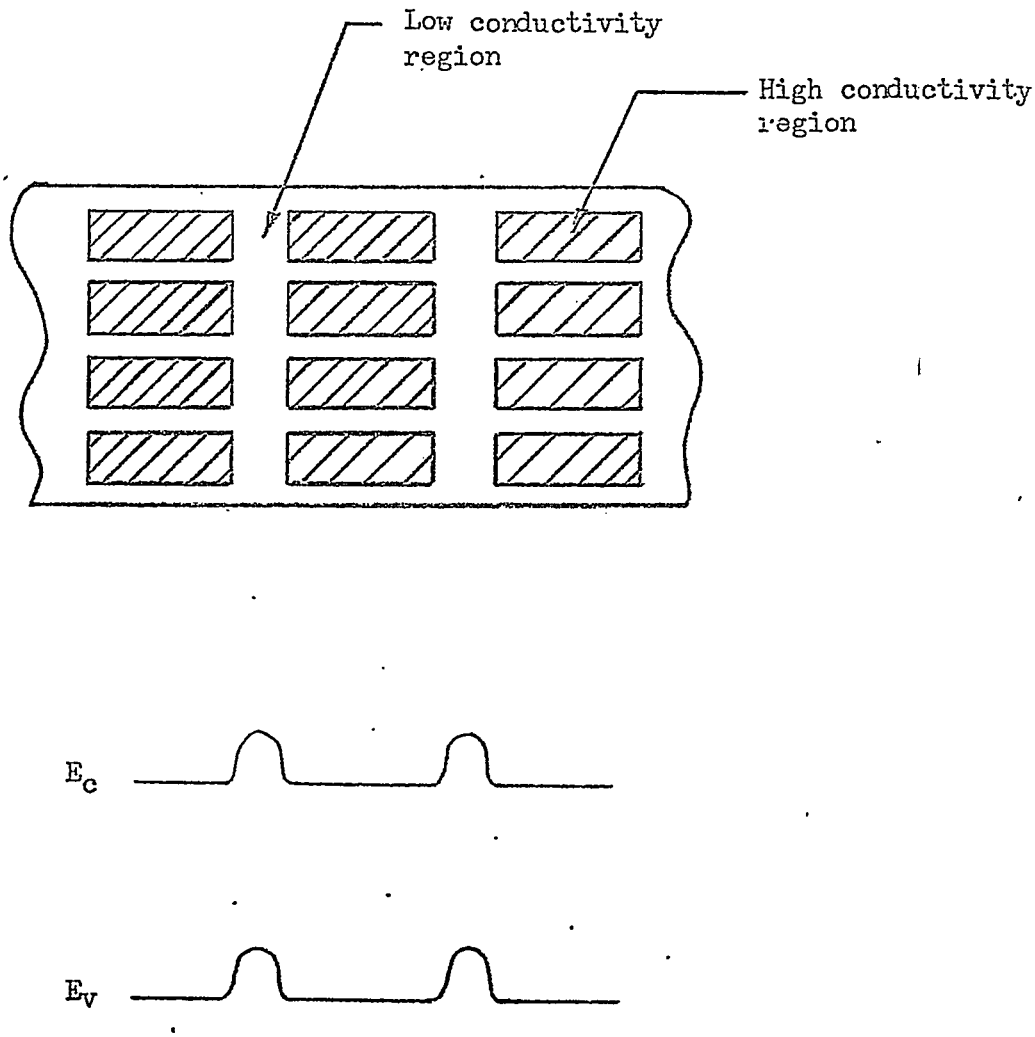


Figure 3.2 Polycrystalline Semiconductor Film Model.

(After Waxman, 1964)

the substrate will have a limited freedom of motion on the substrate and as this freedom of motion is exercised each atom may come in contact with other atoms. Such encounters will result in the formation of atomic bonds between atoms. These bonds may be covalent, ionic, or a combination of the two depending on the semiconductor under consideration. Groups of atoms that are formed in this manner will grow into discrete crystallites. These initial crystallites are known as nucleons and the process by which they are formed as nucleation.

Subsequent atoms reaching the substrate will re-evaporate or adhere to the substrate in proportions determined by the deposition conditions. An atom adhering to the substrate will have the ability to move on the substrate. If a crystallite is encountered during this motion the atom will have a large probability of fitting into the crystal lattice of the crystallite, thereby attaining a local energy minimum. The initial crystallites formed on the substrate thus grow in size until they spread into a continuous thin film. As the evaporation continues and more atoms reach the substrate, the semiconductor film continues to grow in a similar manner.

The average crystallite size in a polycrystalline film has been related to two important deposition parameters, substrate temperature and deposition rate (Holland, 1965). A relatively high temperature substrate imparts substantial kinetic energy to incoming atoms resulting in large freedom of atomic movement on the surface of the substrate. This freedom of movement allows atoms to find and join nucleons already formed, resulting in a small number of relatively large nucleons.

When these nucleons grow large enough to touch, a continuous film is formed composed of relatively large crystallites. Crystallite size is also influenced by the rate of deposition of evaporant atoms onto the substrate in that the greater the deposition rate, the greater the probability of initial interactions between atoms, and the greater the number of initial nucleons that will form. When these nucleons grow large enough to touch, a continuous film will be formed composed of a large number of relatively small crystallites. Thus it can be seen that in general high substrate temperatures and low deposition rates tend to produce large crystallites. High substrate temperatures and low deposition rates also tend to produce low conductivity semiconductor films (Wilson and Gutierrez, 1965), probably due to the complex interaction of many variables influenced by substrate temperature and deposition rate.

Table 3.1 lists all semiconductors used to date in polycrystalline form for the fabrication of TFTs, along with their most important parameters.

3.4 Cadmium Selenide

The semiconductor selected to be used in the fabrication of TFTs in the thin-film laboratory was CdSe. There were a number of reasons for this choice. Both the forbidden energy band gap and electron mobility of CdSe were suitable for TFT application. It had been reported (Wilson and Gutierrez, 1965) that devices utilizing CdSe were easily fabricated and reproducible. This was thought to be mainly due to the relative closeness of the vapour pressure curves of Cd and Se as shown in Figure 3.3 . When a compound is evaporated, fractional

Semiconductor	E_G (ev)	Conductivity Type	μ_e (cm^2/volt-sec)	μ_p (cm^2/volt-sec)
Cd Se [a,f,]	1.7	N	500	< 50
Cd S [a,f]	2.4	N	200	< 50
Cd Te [a,f]	1.5	N	800	100
Pb S [b]	.37	N or P	600	~ 600
Te [c]	.34	P	910	570
In As [d,f,g]	.33	N	20,000	100
In Sb [e,f]	.18	N or P	65,000	700

a Wilson and Gutierrez, 1965
b Pennebaker, 1965
c Weimer, 1964
d Electronics, 1966
e Frantz, 1965
f Bube, 1960
g Properties of Elemental and Compound Semiconductors, 1959

Table 3.1 Semiconductors Used in TFT Fabrication

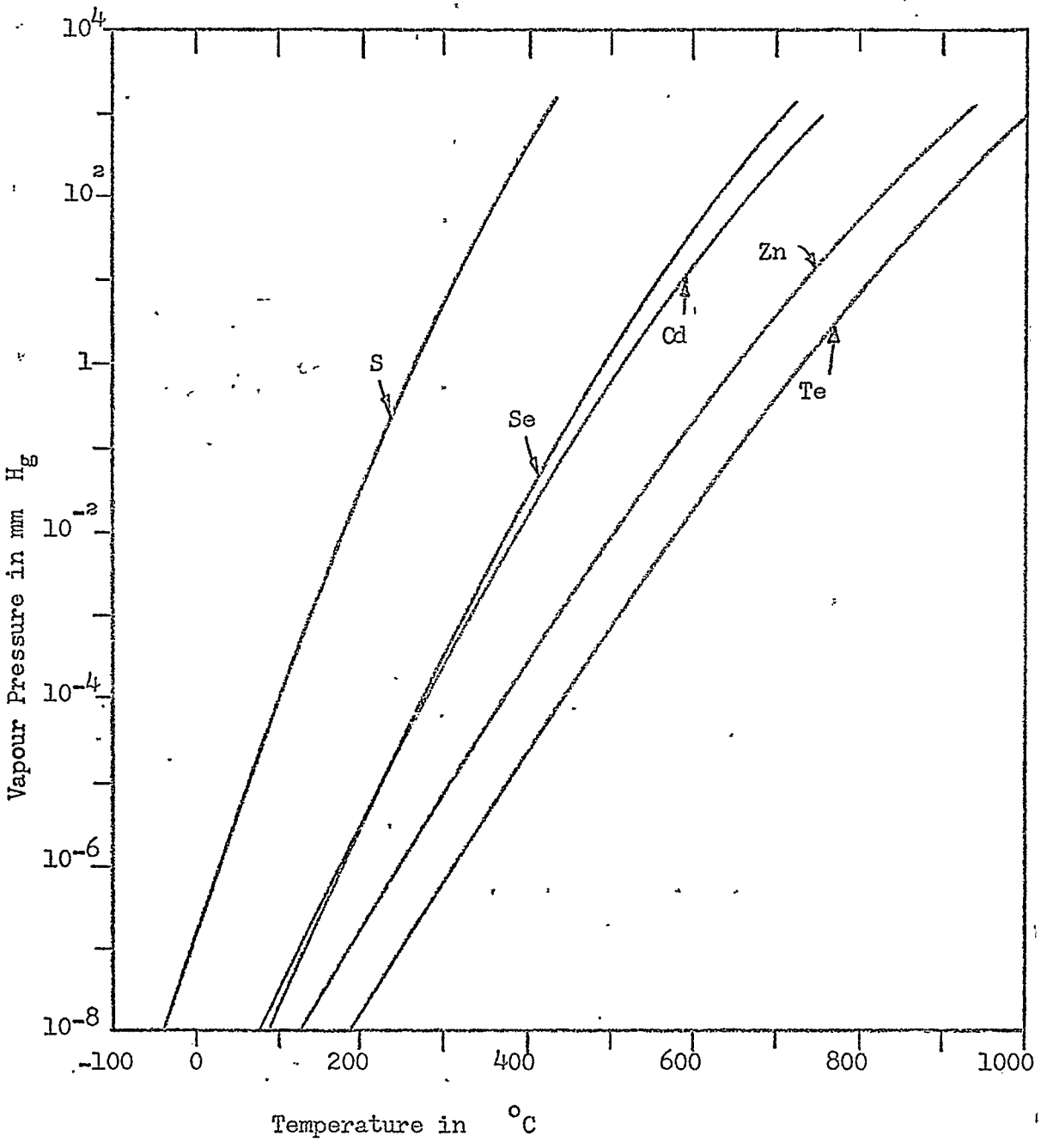


Figure 3.3 Vapour Pressure of Group II - VI Elements

(After Honig, 1962).

distillation occurs in the source material with the result that the initial evaporant is rich in the higher vapour pressure component. As the evaporation proceeds, the composition of the evaporant changes and may lead to a significant gradient across the film thickness. This difficulty is avoided using CdSe. The similarity of the vapour pressure curves of Cd and Se yield a congruent film of close to stoichiometric composition. It was also reported (Wilson and Gutierrez, 1965) that the characteristics of CdSe TFTs were relatively stable with time as compared to similar units made with CdS and CdTe. All these factors contributed to the decision to use CdSe for TFT fabrication and this decision has since been firmly supported by a general trend towards CdSe by the majority of workers in the field.

Table 3.2 lists the most important characteristics of CdSe. It will be noted that the atomic bonding of CdSe is 19% ionic, thereby implying 81% covalent. Because of the dual character to the atomic bonding of CdSe it is necessary to consider in detail the differences the type of bonding makes in the way in which the electronic properties of the material are considered. The structure of CdSe will be discussed from the points of view of ionic and covalent bonding.

For completely ionic bonding (Fig. 3.4(a)), each Cd (Group II) atom will give up two electrons completely to become a Cd^{+2} ion. Each Se (Group VI) atom will take on two electrons completely to become a Se^{-2} ion. The transferred electrons will be localized on the Se^{-2} ion resulting in negligible charge density between ions. For completely covalent bonding (Fig. 3.4(b)), each Cd and each Se will make four bonds, each bond being composed effectively of one-half electron from

Molecular Weight	a	191.4	
Density	a	5.8	grams/cm^3
Melting Point	a	$>$ 1258	^{o}C
Dielectric Constant	a	$\sim$ 4	
E_G	b	1.73	ev
μn	b	500	cm^2/volt-sec.
μp	b	$<$ 50	cm^2/volt-sec.
Type of Bonding	b	19% ionic	

a Handbook of Chemistry and Physics

b Bube, 1960

Table 3.2 Properties of Single-Crystal CdSe

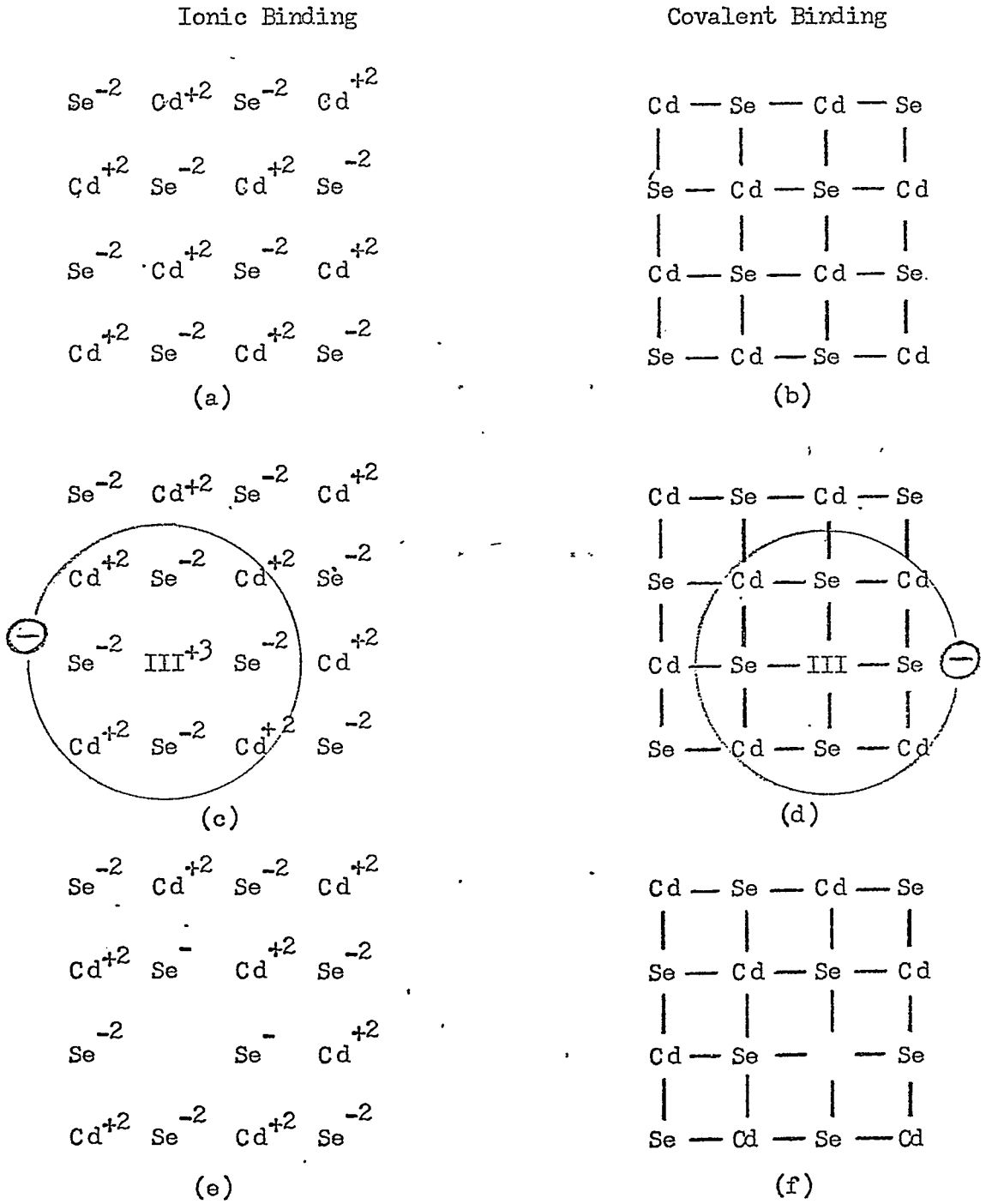


Figure 3.4 Schematic Comparison of Ionic and Covalent Binding,
(a) and (b), Perfect CdSe;
(c) and (d), A Group III Atom Substituted for a Cd atom;
(e) and (f), A Cd Vacancy
(After Bube, 1960).

a Cd and one and one-half electrons from a Se. The charge density will be concentrated in the interatomic spaces.

Consider the result of removing a Cd atom and replacing it with a Group III atom. From the ionic point of view (Fig. 3.4(c)), the removal of a Cd atom leaves behind it two positive charges. The Group III atom will take up these two positive charges but also requires a third positive charge to satisfy it's valence requirements. It therefore gives up an electron which may be bound in the vicinity of the Group III atom at low temperatures but will be freed at higher temperatures, to move through the crystal lattice. From the covalent point of view (Fig. 3.4(d)), the removal of a Cd atom breaks four bonds and leaves a deficiency of two electrons. The substitution of a Group III atom for a Cd is accomplished by having the Group III atom contribute two of its electrons to satisfy the bond requirements, and then being able to donate the extra electron to be free at sufficiently high temperature. Thus the Group III atom acts as a donor when substituted for a Cd atom and the choice of ionic or covalent bonding does not affect the ultimate conclusions.

Arguments similar to the above lead to the results that a Group I atom acts as an acceptor when substituted for a Cd atom, a Group VII atom acts as a donor when substituted for a Se atom, and a Group V atom acts as an acceptor when substituted for a Se atom. The same conclusions are reached for both ionic and covalent bonding.

Consider now the situation if a Cd atom is simply removed from the crystal lattice. From the ionic point of view (Fig. 3.4(e)), the vacancy will have bound to it two positive holes in order to maintain

charge neutrality. In other words, one electron will be missing from each of two adjacent Se atoms. If one or two electrons are captured by the vacancy it becomes negatively charged either once or twice with respect to the rest of the crystal. From the covalent point of view, a vacancy resulting from the removal of a Cd atom is a localized region in the crystal where two electrons are required to complete the bond requirements. Thus it can be seen that a Cd vacancy acts as an acceptor for electrons. Similar reasoning leads to the conclusion that Se vacancies act as donors in the crystal lattice.

Oxygen has varied and in many cases as yet unrecognized effects on the properties of semiconductors in general. Oxygen usually acts like an acceptor in CdSe, (Bube, 1960), particularly on evaporated layers of that material. It is believed that oxygen diffuses into Se vacancies, thereby compensating these vacancies that would otherwise act as donors. This process explains the experimental result that a post-fabrication air bake reduces the conductivity of the semiconductor layer in CdSe TFTs (Wilson and Gutierrez, 1965).

Table 3.3 and Figure 3.5 summarize the energy levels associated with imperfections in CdSe. It will be noted that vacancies in CdSe give rise to double energy levels in the forbidden energy gap and that the ionization energies of donors ($E_C - E_D$), where E_D is donor energy level, are in general much smaller than the ionization energies of acceptors ($E_A - E_V$), where E_A is acceptor energy level.

The topic of donors and acceptors in CdSe is important since in a semiconductor with a forbidden band gap such as that of CdSe (1.7 ev), the number of carriers available for conduction at room temperature is

Imperfection	Group	Substitutes For	Donor or Acceptor	Ionization Energy (ev) $E_c - E_D$	Ionization Energy (ev) $E_A - E_v$
Cl, Br, I	VII	Se	D	0.03	
Cu	I	Cd	A		0.64
Se Vacancy			D	0.14	
			D	~0.6	
Cd Vacancy			A		0.6
			A		1.0

Table 3.3 Ionization Energies of Imperfections In CdSe (After Bube, 1960).

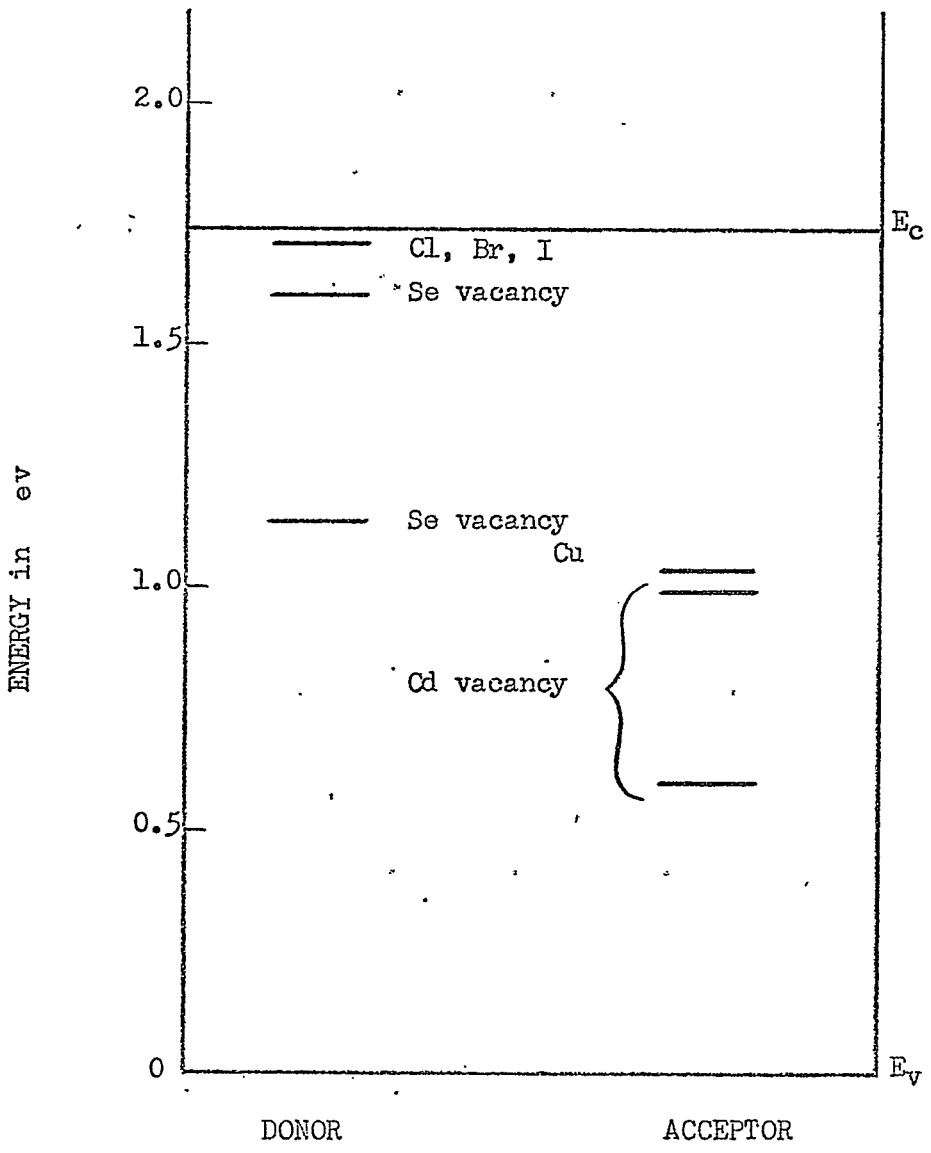


Figure 3.5 Imperfection Levels in CdSe

(After Bube, 1960).

determined by donor and acceptor concentrations. The number of ionized donors is very nearly equal to the number of conduction electrons and the number of ionized acceptors is very nearly equal to the number of holes available for conduction. If Boltzmann statistics are assumed to be valid, the percentage of donors and acceptors that are ionized is directly proportional to the Boltzmann factor, $\exp\left(-\frac{E_I}{kT}\right)$, where E_I is ionization energy. For comparable numbers of acceptors and donors in CdSe, since E_I is much larger for acceptors than for donors, there will be many more electrons available for conduction than holes. This result, compounded by the fact that hole mobility in general is lower than electron mobility, indicates that CdSe is a one-carrier semiconductor with conduction by electrons strongly dominating over conduction by holes. Figure 3.6 shows conductivity per unit mobility plotted against minority carrier concentration for typical values of majority carrier concentration and ionization energy. Conductivity per unit mobility is used as hole mobility in CdSe is very small and not accurately known. Figure 3.6 shows graphically the great assymmetry in conductivity of CdSe that is doped with comparable numbers of donors or acceptors.

The one-carrier nature of CdSe greatly simplifies the problem mentioned in section 3.2 of imperfection centers in a semiconductor that may act as either traps or recombination centers or both. In CdSe, since conduction occurs almost entirely by electron flow, roles played by both recombination centers and hole traps are very minor. The effect of imperfection centers is important only in their ability to act as electron traps.

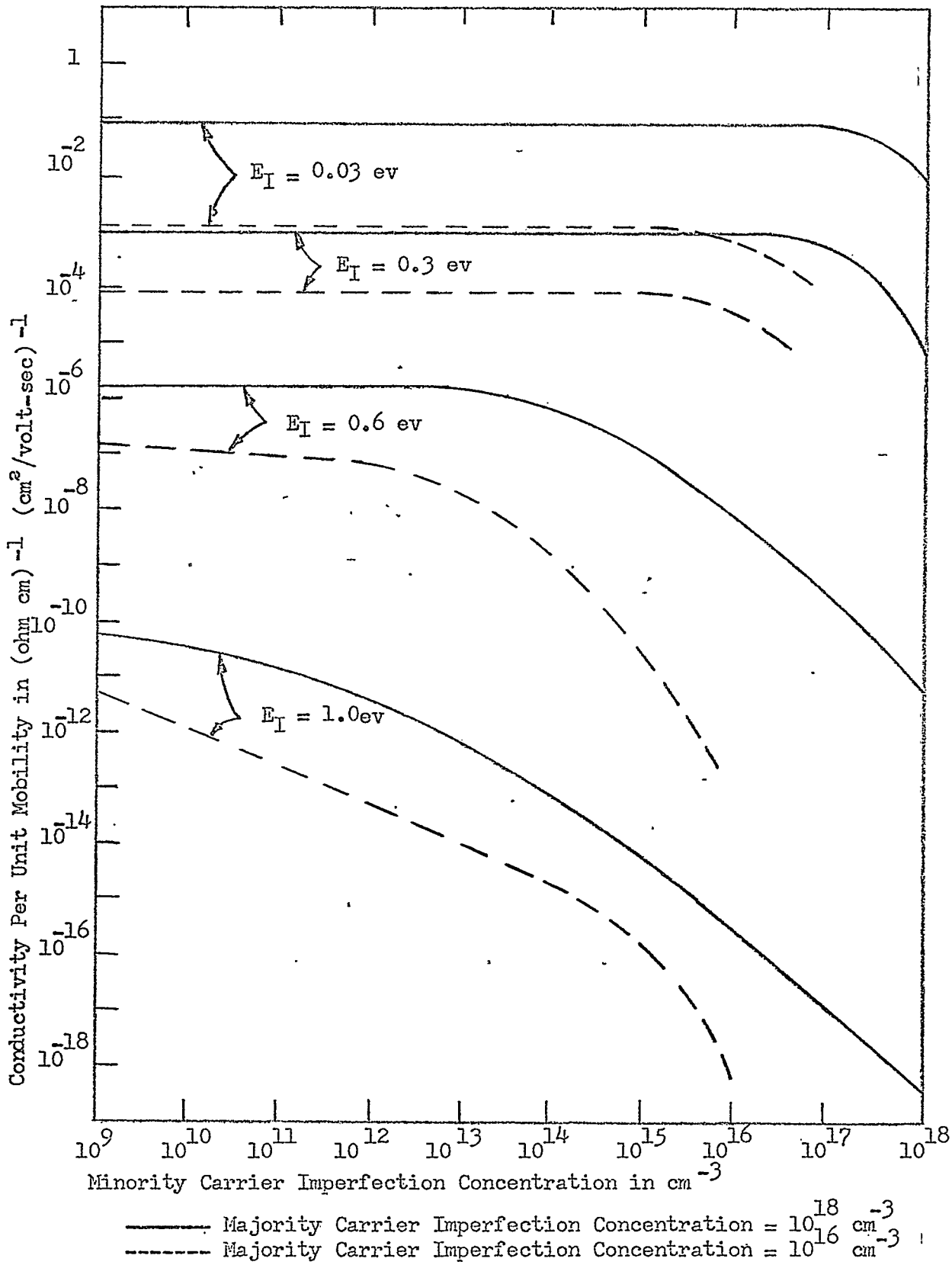


Figure 3.6 Conductivity of Cd Se Versus Imperfection Center Concentrations (After Bube, 1960).

The most important characteristics of single-crystal semiconductors, polycrystalline semiconductors, and CdSe have been presented. The properties described in all three of the above sections are combined in polycrystalline CdSe, the semiconductor of interest in this thesis.

4. THE INSULATOR

4.1 Introduction

Since TFT characteristics are substantially affected by the material properties of the insulating layer, a discussion of these properties is indicated. While the subject matter of this chapter is not intended to be a complete review of the topic, an effort has been made to discuss qualitatively those insulator properties that substantially influence TFT operation.

In order to treat the properties of the insulating layer in a logical fashion, this chapter has been divided into two sections. The first section discusses the necessary attributes of a TFT insulator. Insulating materials that have been successfully employed in TFT fabrication are noted. The specific properties of the insulator used in TFT fabrication in the thin-film laboratory are tabulated and discussed. The second section treats the subject of ion drift in the insulator and the effects of this important physical process on TFT characteristics.

This chapter is not intended to be an isolated discussion of the properties of insulating materials. The properties of the insulators discussed here are considered as important only due to their influence on TFT characteristics. The content of this chapter is qualitative in nature and therefore limited in scope but is included in this thesis because of its very definite importance and also for the sake of completeness.

4.2 Characteristics of TFT Insulators

In order for a material to be suitable for use as a TFT insulator, it must possess certain definite characteristics. Foremost among these

requirements are ease of evaporation by standard vacuum techniques, very low bulk conductivity, and suitable dielectric constant. Many materials possessing these attributes may be rejected because of decomposition during evaporation, lack of reproducibility, absorption of moisture, low breakdown voltage, or frequency dependence of the dielectric constant. The nature of the interface between the insulator and adjacent materials must be considered, including the degree of mechanical stress that will arise at the interface.

The materials that have been used most successfully to date as TFT insulators are silicon monoxide (e.g. Borkan and Weimer, 1963), calcium fluoride (Borkan and Weimer, 1963), and aluminum oxide (Fabula, et al, 1966). Of these, the most common is silicon monoxide. Ease of evaporation and favourable physical constants, listed in Table 4.1, contribute substantially to the popularity of silicon monoxide as a TFT insulator.

In order to vacuum deposit the insulating layer of the TFTs used by the author, silicon monoxide in either powder or lump form may be evaporated in an oxidizing atmosphere at 10^{-4} torr. During the evaporation the silicon monoxide partially oxidizes to form silicon dioxide, resulting in an amorphous glass composed of grains of both silicon monoxide and silicon dioxide (Glang, 1966). The pressure of 10^{-4} torr is held constant from deposition to deposition to encourage reproducibility. No serious problems have arisen in the deposition procedure and the insulating films have been satisfactory to date.

	Parameter	Value	Units
a	Dielectric Constant	6	
a	Dielectric Breakdown Strength	$(1 - 3)\ 10^6$	Volts/cm
b	Density	2.2	grams/cm^3
b	Molecular Weight	44.1	

a Glang, 1966

b Handbook of Chemistry and Physics

Table 4.1 Properties of Silicon Monoxide

4.3 Ion Drift in the Insulator

The existence of mechanisms for migration of ions in silica glass insulating films is well established (Snow, et al, 1965). Substantial experimental evidence exists that the process of ion drift in the insulator plays an important role in the operation of the TFTs fabricated in the thin-film laboratory. The two types of mobile ions that are most likely to exist in vacuum deposited silicon monoxide films are alkali ions and hydrogen ions. The existence and behavior of significant numbers of alkali ions in thermally grown silicon dioxide has been well documated (Snow, et al, 1965 and Hofstein, 1966). A probable mechanism exists by which alkali ions might be present in evaporated silicon monoxide films. Suppose that at the gate-insulator interface an aluminium atom substitutes for a silicon atom. The resulting insulator film will have a single net negative charge unless an ion with a single net positive charge is drawn into the insulator to maintain overall charge neutrality. Since alkali ions are present in most commercial glass, and in particular in the soda glass of the substrate, it is probable that alkali metal ions comprise a significant fraction of the mobile ions in the TFT insulator. High mobility hydrogen ions have also been identified in thermally grown silicon dioxide films (Hofstein, 1966) and may quite possibly arise in vacuum deposited silicon monoxide films due to hydrolysis of adsorbed water at the oxide-metal interface.

The effect of ion drift on TFT characteristics can be explained with the aid of Figure 4.1 . Consider an insulating layer in which there are both positive and negative mobile ions. Overall charge neutrality is, of course, maintained. If a potential difference is

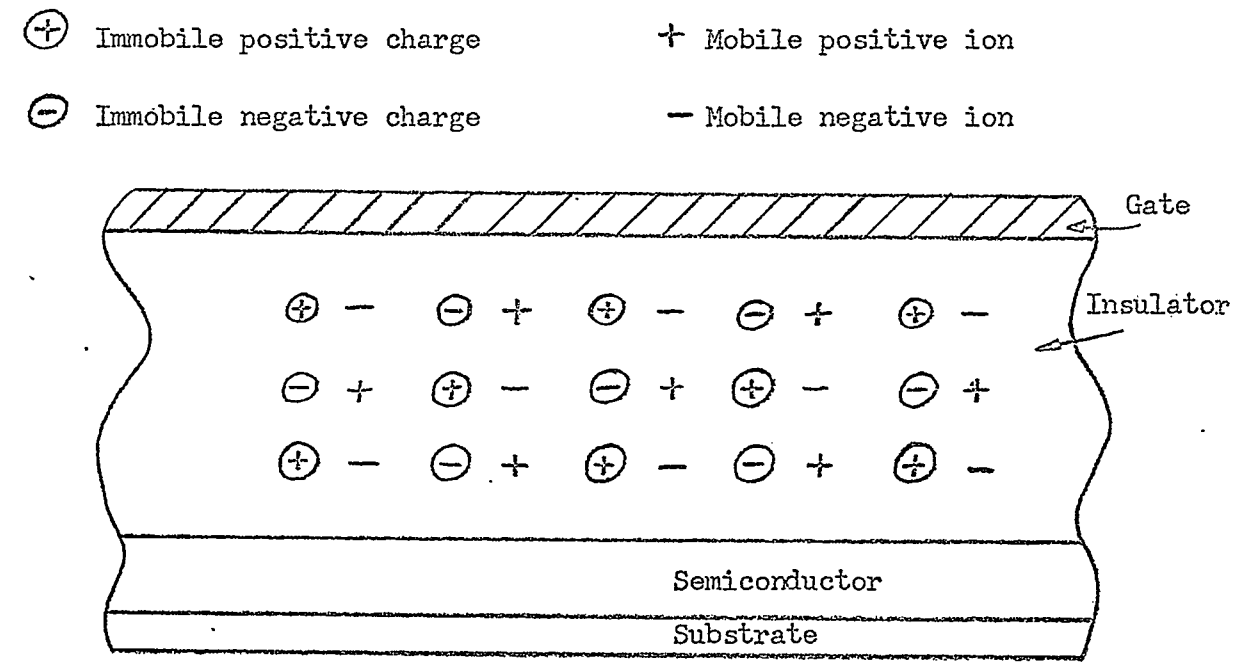


Figure 4.1(a) Insulator with Ions. No Bias Applied

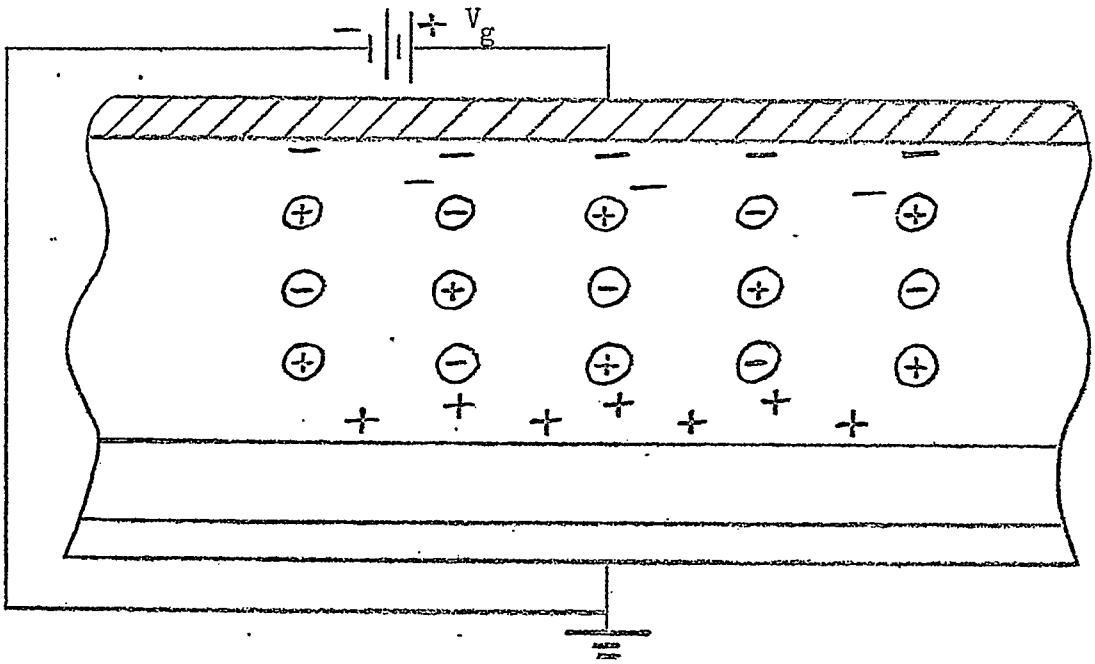


Figure 4.1(b) Insulator with Ions. Bias Voltage Applied

Figure 4.1 The Effect of Ion Drift in the Insulator

applied across the insulating layer, an electric field will be established throughout the insulator. Under the influence of this electric field the mobile ions will tend to drift towards the boundaries of the film. This migration may take minutes, days, or even months depending on the properties of the insulator and the ions. When the potential difference and associated electric field are removed from the insulator the ions will both diffuse and drift towards a more uniform distribution throughout the insulator with a time constant that may be different from that of their initial drift. These changes in the distribution of ions alter the dipole moment and consequently the effective dielectric constant of the insulator. The gate-semiconductor capacitance is thus varied. Because of the ion drift phenomena it can be seen that in a mathematically rigourous TFT analysis, gate-semiconductor capacitance must be considered to be a function of both gate voltage and time.

5. THE CONDUCTION PROCESS IN TFT'S

5.1 Introduction

The material of this chapter will be concerned with the process of current conduction in TFTs, and with the TFT as an active electronic device. Since all insulated-gate transistors operate by similar physical mechanisms, most of the subject matter presented here is as applicable to the metal-oxide semiconductor field-effect transistor as it is to the TFT. Parts of this chapter, in fact, were first derived specifically for the MOS transistor, but can also be applied to the TFT.

The first subject to be treated will be an estimate of the depth of the conduction channel below the semiconductor-insulator interface. In order to solve this problem, a semi-infinite TFT section will be assumed. The derivation, which will be general to the extent of being applicable for any arbitrary value of x, as defined in Figure 2.1, will be carried out for two models. The first model contains a perfectly trap-free semiconductor, while the second model assumes a sheet of trapped electrons existing at the semiconductor-insulator interface, all other areas being trap-free. From this analysis, estimates of the profiles of potential, electric field, and free electron concentration from the gate electrode to the substrate will be obtained.

The second topic of this chapter will be a derivation of an equation predicting steady state TFT characteristic curves. This analysis is based on field effect considerations and is at present the generally accepted model used to describe insulated-gate field-effect transistor operation. The assumptions and limitations of the analysis

will be clearly indicated and are considered to be an important part of the physical interpretation of the model.

The third, and final, section is a brief presentation of two equivalent circuits describing TFT small signal response.

5.2 Calculation of Channel Thickness

The common method used to analyze the conduction process in insulated-gate field-effect transistors, such as TFTs, is to write Ohm's law for an arbitrary incremental section taken normal to the channel current density and then integrate the resulting expression over the entire channel length. Before proceeding in this manner, it is instructive to consider the arbitrary incremental section in some detail. If the assumption is made that the semiconductor layer is infinitely thick, descriptive solutions can be obtained for the conduction channel thickness, potential and electric field variation from gate to substrate, and free electron concentration profile in the semiconductor. Two cases are considered here, the case of no surface states at the semiconductor-insulator interface and the case of a sheet of trapped electrons at the interface. Although the solutions obtained are for the limiting case of an infinitely thick semiconductor, they will also constitute a good approximation for the practical situation in which the semiconductor layer thickness is much thicker than the conduction channel thickness, and are important for this reason.

Consider the semi-infinite incremental TFT section shown in Figure 5.1, taken at some arbitrary value of x as defined in Figure 2.1. A voltage V_g has been applied between the gate electrode and the bottom of the semiconductor. Electrons will be drawn from the gate electrode

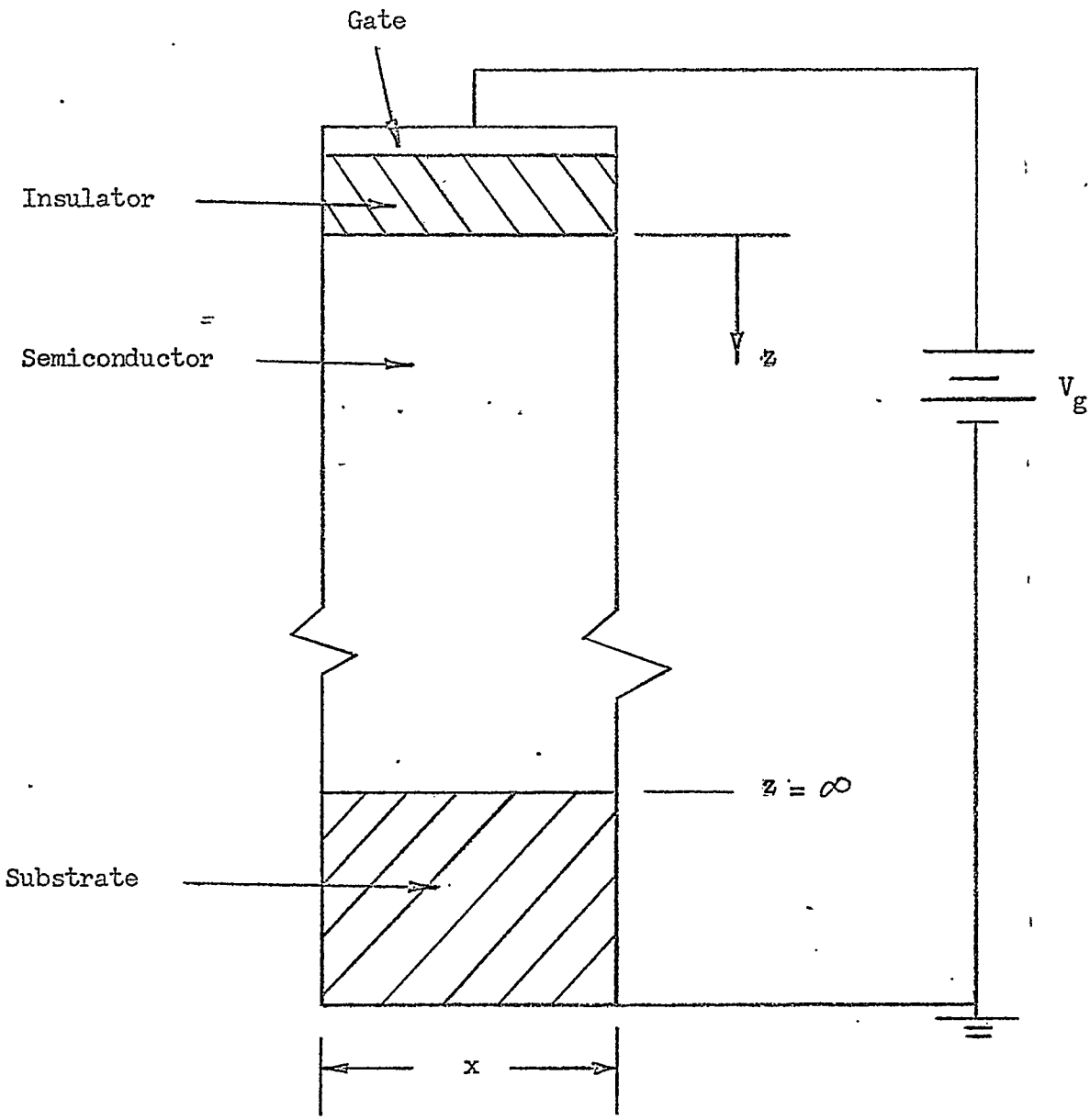


Figure 5.1 Semi-infinite TFT Section

into the semiconductor and, when equilibrium has been re-established, will be concentrated mainly near the semiconductor-insulator interface. Poisson's equation, written for the semiconductor yields

$$\frac{d^2V}{dz^2} = \frac{q(n - n_o)}{K_s \epsilon_o} \tag{5.1}$$

where V = electrostatic potential at any point in the semiconductor

q = charge on an electron

n = free electron density

n_o = free electron density in bulk semiconductor with zero applied gate voltage

K_s = dielectric constant of semiconductor

ϵ_o = permittivity of free space.

The boundary conditions to be imposed stipulate that $V = 0$ at $z = \infty$ and, since $n = n_o$ at $z = \infty$, $\frac{dV}{dz} = 0$ at $z = \infty$.

If Boltzmann statistics are assumed to be valid,

$$\frac{n(z)}{n_o} = \frac{e^{\frac{qV(z)}{kT}}}{e^{\frac{qV_\infty}{kT}}}$$

where V_∞ = potential at $z = \infty$.

Since $V_\infty = 0$,

$$n(z) = n_o e^{-\frac{qV(z)}{kT}} . \tag{5.2}$$

From (5.1) and (5.2)

$$\frac{d^2V}{dz^2} = \frac{qn_o}{K_s \epsilon_o}\left[e^{\frac{qV}{kT}} - 1\right] . \tag{5.3}$$

Multiply both sides by $\frac{dV}{dz}$ and integrate.

$$\frac{1}{2}\left[\frac{dV}{dz}\right]^2 = \frac{qn_o}{K_s \epsilon_o}\left[\frac{kT}{q} e^{\frac{qV}{kT}} - V\right] + A_1 \tag{5.4}$$

where A_1 = an arbitrary constant of integration.

To evaluate A_1 invoke the boundary conditions of $V = 0$ at $z = \infty$ and $\frac{dV}{dz} = 0$ at $z = \infty$.

$$A_1 = - \frac{n_o kT}{K_s \epsilon_o} .$$

Equation (5.4) therefore becomes

$$\frac{1}{2}\left[\frac{dV}{dz}\right]^2 = \frac{qn_o}{K_s \epsilon_o}\left[\frac{kT}{q} e^{\frac{qV}{kT}} - V - \frac{kT}{q}\right] . \qquad (5.4(a))$$

Since $E = - \frac{dV}{dz}$

where E = electric field,

$$E = \sqrt{\frac{2n_o kT}{K_s \epsilon_o}}\left[e^{\frac{qV}{kT}} - \frac{qV}{kT} - 1\right]^{\frac{1}{2}} . \qquad (5.5)$$

Consider now the insulator layer, in which the space charge is zero at all points.

$$E_i = \frac{V_g - V_s}{t_i} \qquad (5.6)$$

where E_i = electric field in insulator

V_s = potential at semiconductor-insulator interface

t_i = thickness of insulator.

If the assumption is made that there is no trapped charge at the interface, the flux density must be continuous across the interface. Therefore,

$$K_i \epsilon_o E_i = K_s \epsilon_o E_s \qquad (5.7)$$

where K_i = dielectric constant of insulator

E_s = electric field in semiconductor at interface.

From (5.6) and (5.7),

$$E_s = \frac{K_i}{K_s}\left[\frac{V_g - V_s}{t_i}\right] . \qquad (5.8)$$

From (5.5),

$$E_s = \sqrt{\frac{2n_o kT}{K_s \epsilon_o}} \left[e^{\frac{qV_s}{kT}} - \frac{qV_s}{kT} - 1 \right]^{\frac{1}{2}} . \qquad (5.5(a))$$

Equating (5.5(a)) and (5.8) yields

$$V_g = \frac{K_s}{K_i} t_i \sqrt{\frac{2n_o kT}{K_s \epsilon_o}} \left[e^{\frac{qV_s}{kT}} - \frac{qV_s}{kT} - 1 \right]^{\frac{1}{2}} + V_s . \qquad (5.9)$$

The effective conduction channel thickness is conveniently defined as the geometrical mean of the charge distribution. That is

$$L_c = \frac{\int_{z=0}^{z=\infty} z(n-n_o)\, dz}{\int_{z=0}^{z=\infty} (n-n_o)\, dz} .$$

since $$\frac{dE}{dz} = - \frac{q(n-n_o)}{K_s \epsilon_o} ,$$

$$L_c = \frac{\int_{E=0}^{E=E_s} z\, dE}{\int_{E=0}^{E=E_s} dE}$$

$$= \frac{zE \Big|_{z=0}^{z=\infty} - \int_{z=0}^{z=\infty} E dz}{E_s}$$

$$= \frac{0 - (-V_s)}{E_s} .$$

Therefore,

$$L_c = \frac{V_s}{E_s} . \qquad (5.10)$$

Consider, now, the situation if it is assumed that at the semiconductor-insulator interface there exists a sheet of immobile charge. Such a sheet of charge commonly occurs in actual devices because of carriers trapped at interfaces. The above equations will now be modified to account for this sheet of trapped charge.

Assume a surface density, Q_s, of trapped electrons exists at the semiconductor-insulator interface. Equations (5.1) through (5.6) and (5.10) are still valid. Since the flux density must be continuous across the interface,

$$K_i \epsilon_o E_i - K_s \epsilon_o E_s = q Q_s. \tag{5.11}$$

Substitution of (5.5(a)) and (5.6) into (5.11) yields

$$V_g = \frac{K_s}{K_i} t_i \sqrt{\frac{2n_o kT}{K_s \epsilon_o}} \left[e^{\frac{qV_s}{kT}} - \frac{qV_s}{kT} - 1 \right]^{\frac{1}{2}} + V_s + \frac{q Q_s t_i}{K_i \epsilon_o}. \tag{5.12}$$

Figures 5.2, 5.3, and 5.4 are qualitative descriptive curves demonstrating free electron concentration and potential and electric field distributions in the TFT section under consideration for both interface conditions considered. Equations (5.9), (5.10), and (5.12) were solved for a variety of possible conditions with the aid of the computer. Figures 5.5 through 5.8 illustrate some of the more descriptive results obtained.

An analysis of an incremental TFT section has been performed assuming an infinitely thick semiconductor. It is intended to use the derived results as an approximation to the practical case in which the semiconductor film thickness is substantially greater than the channel thickness.

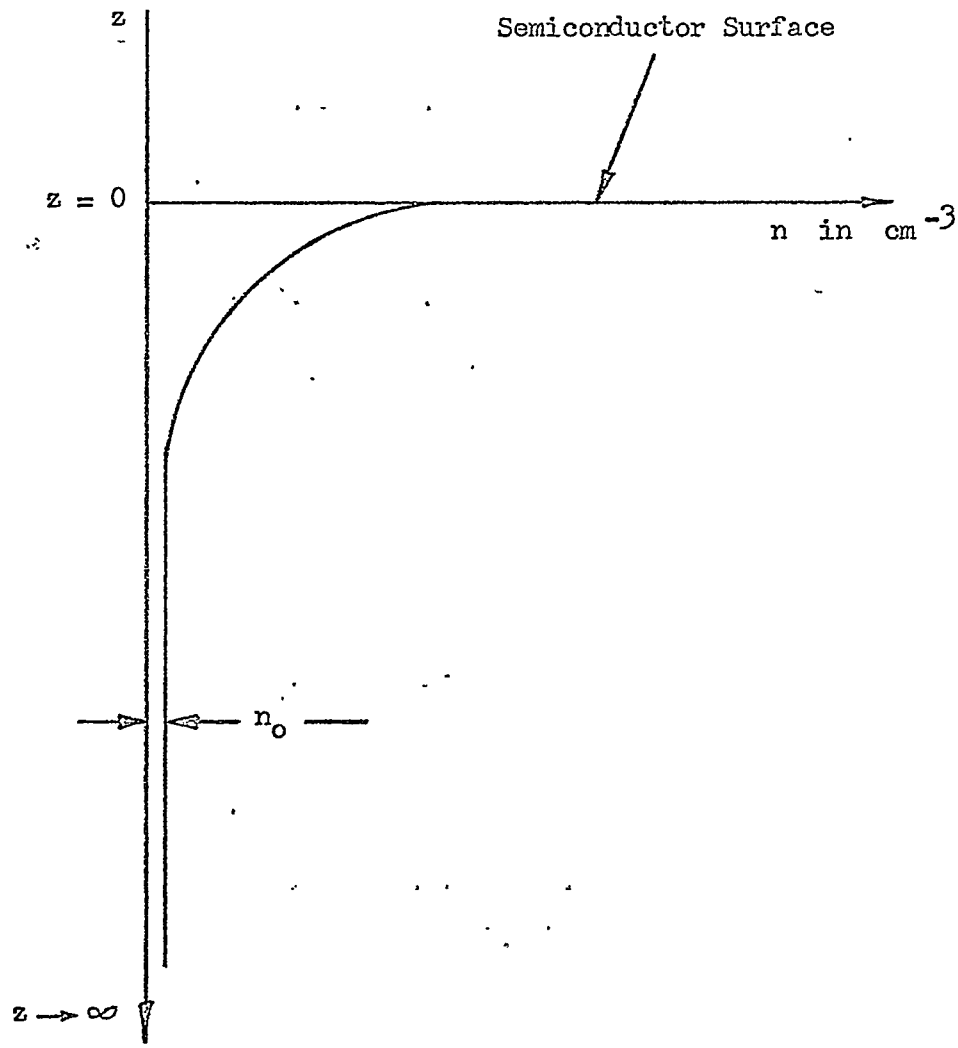


Figure 5.2 Qualitative Plot of Free Electron Density Versus z Coordinate

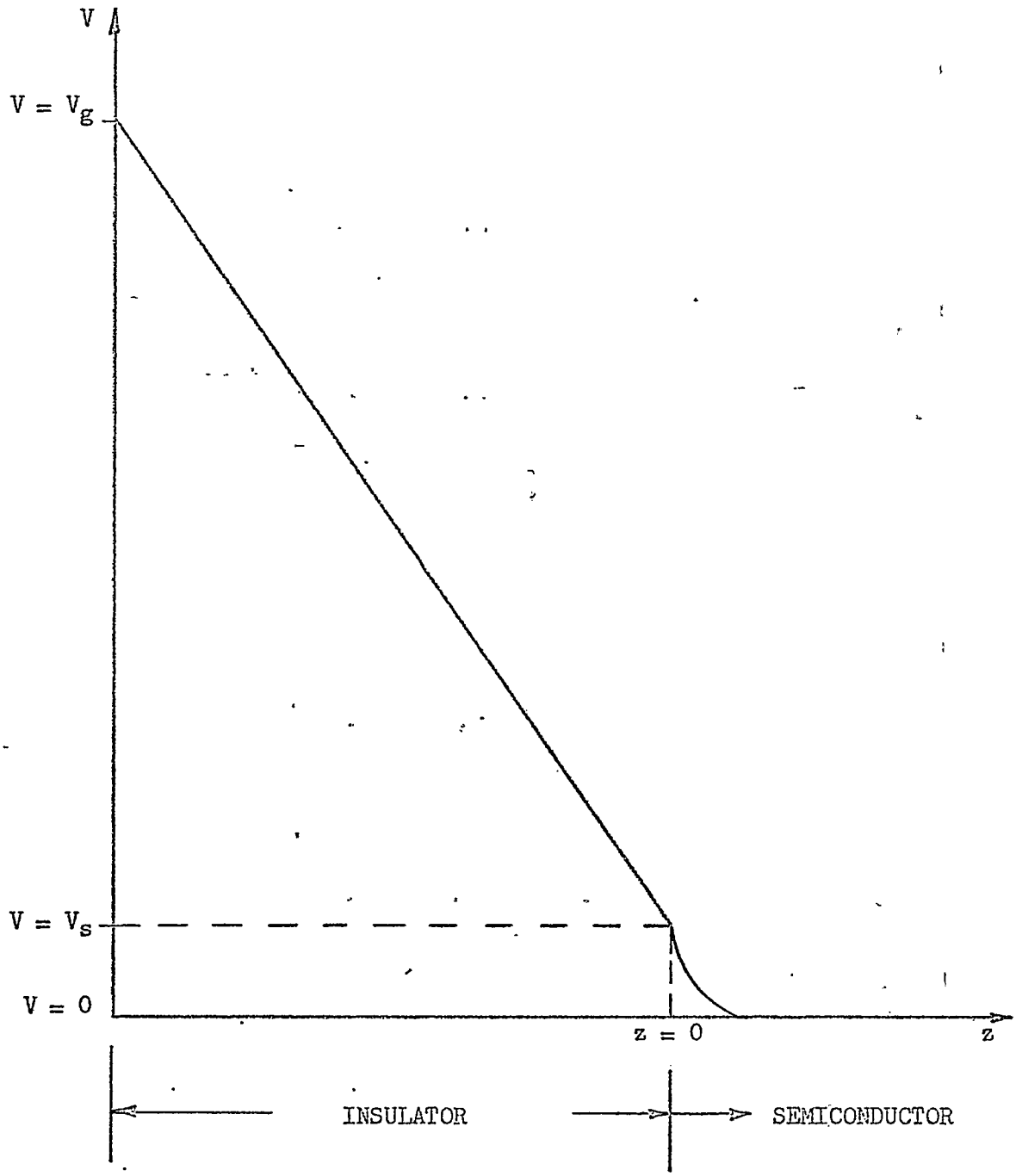
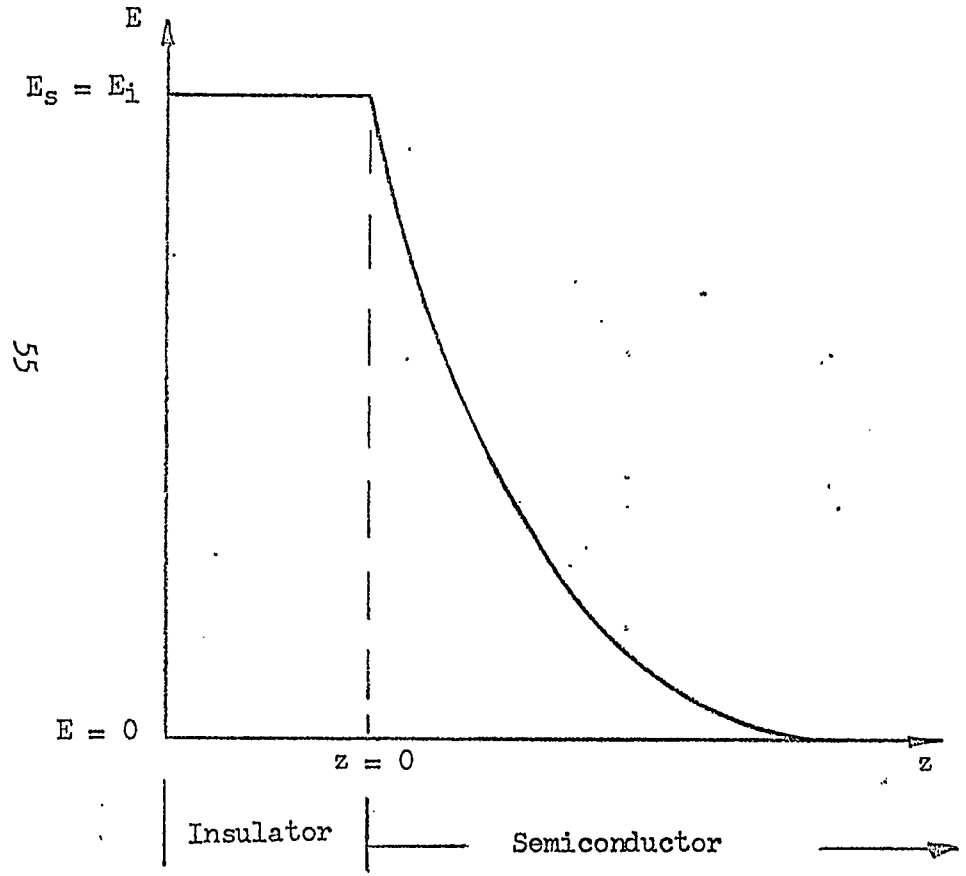
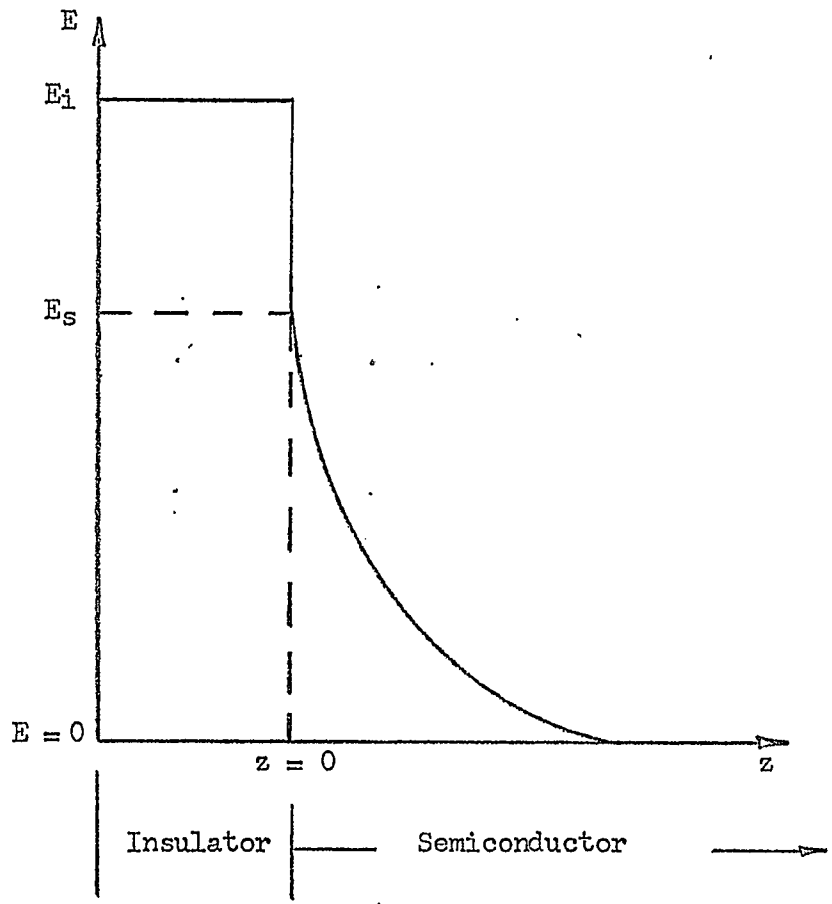


Figure 5.3 Potential Profile in z Direction For Cases of Both No Traps and Traps at Interface



(a) No Traps Present



(b) Traps Present

Figure 5.4 Electric Field Profile In z Direction

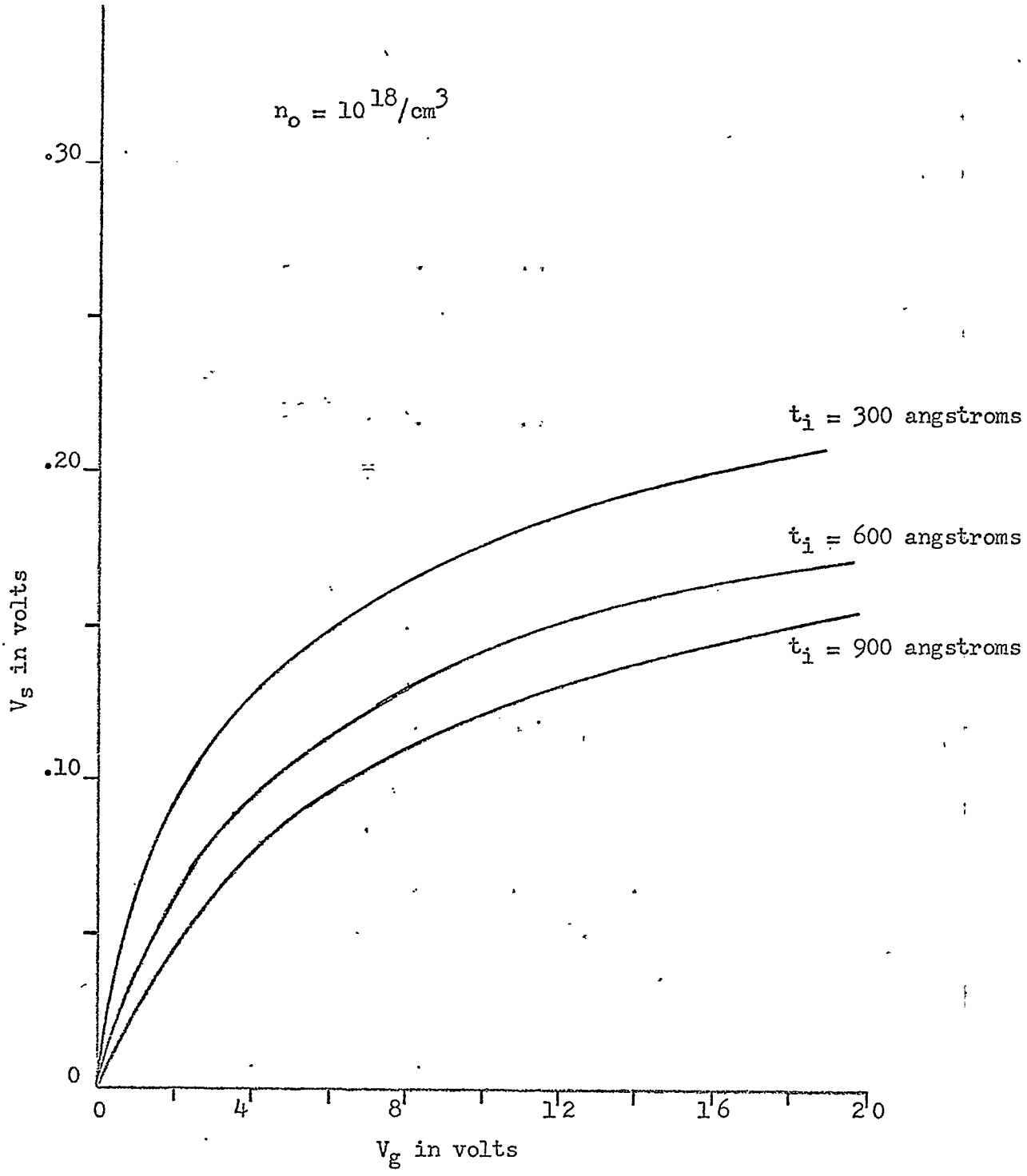


Figure 5.5 V_s As a Function of V_g and t_i.

No surface States.

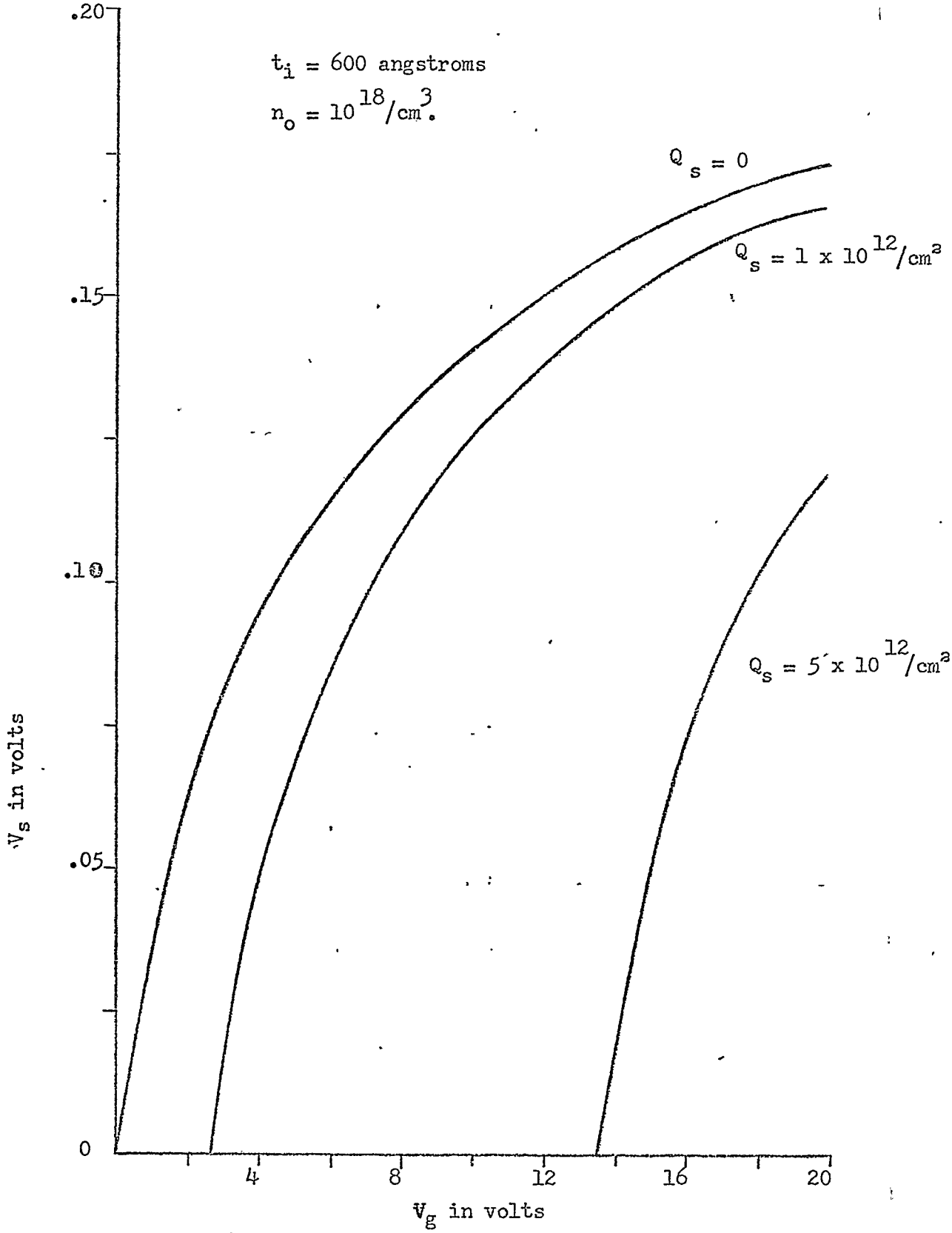


Figure 5.6 V_s As a Function of V_g and Surface State Density.

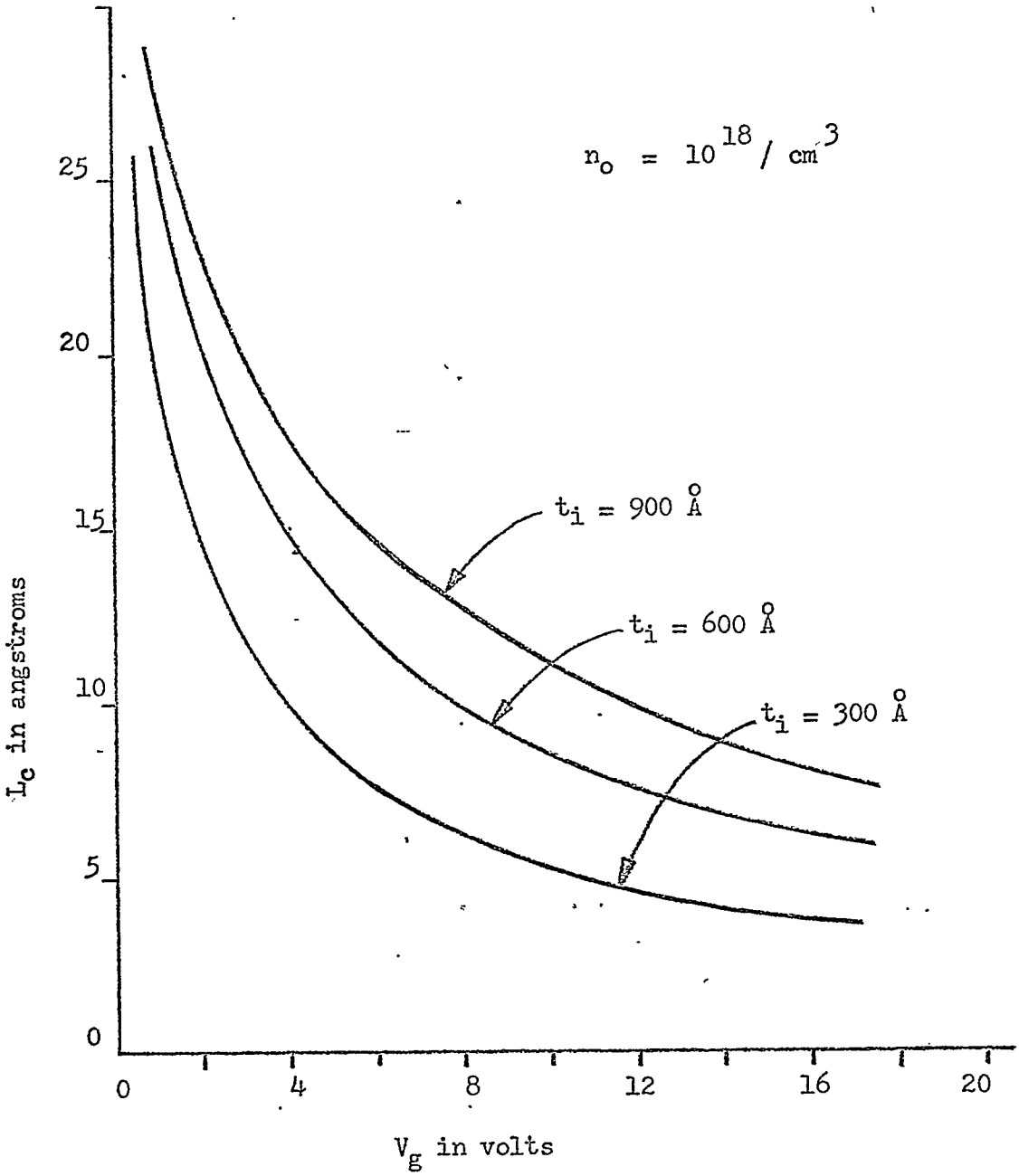


Figure 5.7 L_c as a Function of V_g and t_i.
No Surface States.

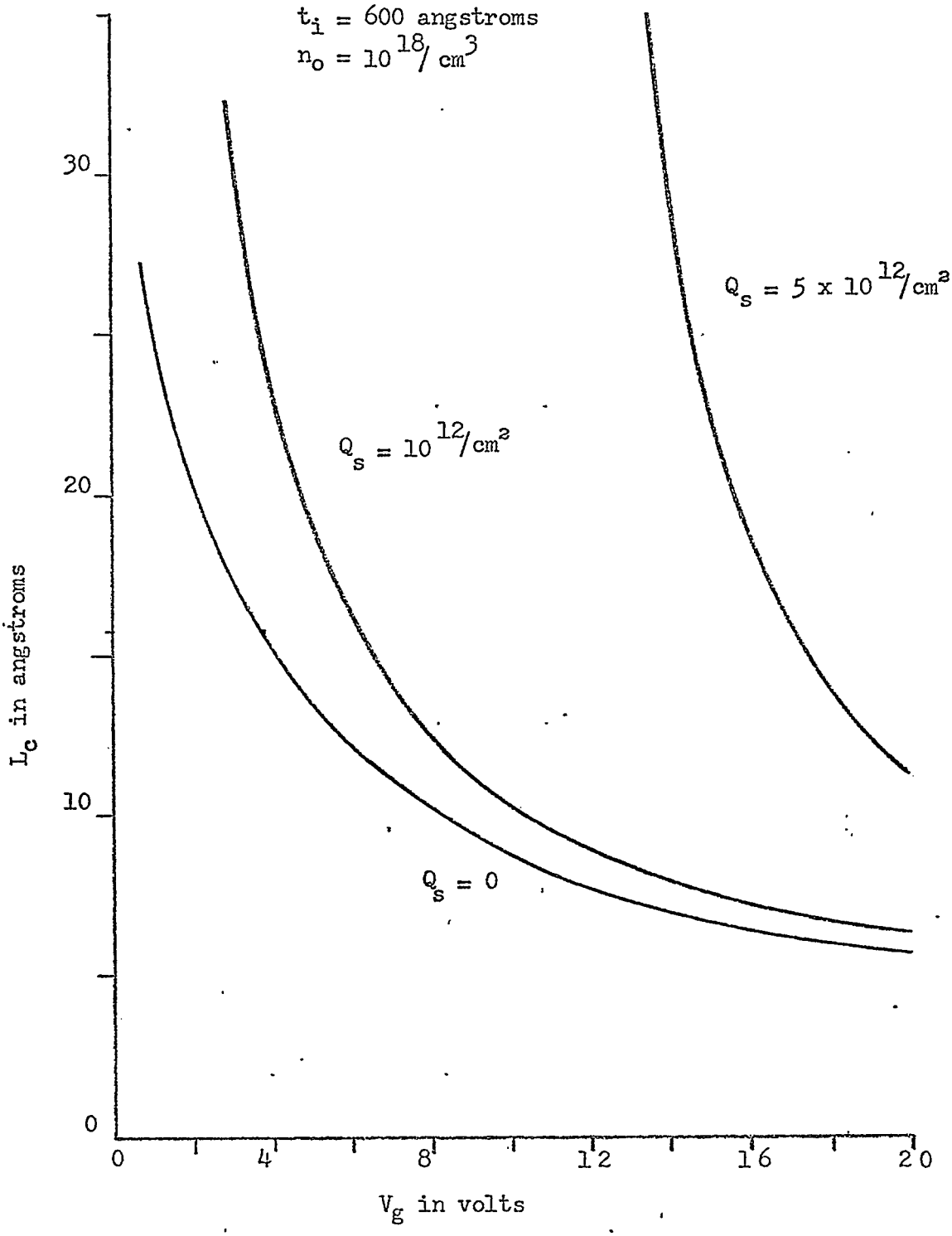


Figure 5.8 L_c As a Function of V_g and Surface State Density

5.3 TFT Conduction at D.C.

In this section an equation will be derived describing the conduction process in an TFT at D.C. All assumptions made during the derivation will be carefully noted. The degree of similarity between a set of characteristic curves predicted by the derived equation and those observed experimentally will be commented upon.

Consider the TFT of Figure 2.1 . Assume a homogeneous layer of semiconductor of thickness t_s, containing only electrons of constant mobility as carriers. The source and drain electrodes form ohmic contact with the semiconductor. Ohm's law, written for the semiconductor at an arbitrary x is,

$$I_d = g \frac{dV(x)}{dx} \tag{5.13}$$

where g^{-1} = resistance per unit length.

Therefore,

$$g = q\mu Z \int_0^{t_s} n dz \tag{5.14}$$

where μ = effective mobility of electrons.

The total free electron concentration per unit area in the channel, $\int_0^{t_s} n dz$, can be obtained using the gauss theorem of flux. If the assumption is made that the channel width is fairly uniform along its length, the flux lines are all nearly perpendicular to the semiconductor-insulator interface (Sah, 1964). This is the "gradual channel approximation" (Shockley, 1952) commonly used to analyze insulated-gate transistor operation up to pinch-off.

The one-dimensional form of the gauss theorem is

$$C_o W(x) = q \int_o^{t_s} (n-n_o) dz + q\, Q_s \tag{5.15}$$

where C_o = insulator capacitance per unit area

$$= \frac{K_i \epsilon_o}{t_i}$$

$W(x)$ = voltage drop across the insulator

$$= V_g - V(x)$$

Q_s = surface density of negative charge, interpreted physically as trapped electrons.

Rearranging terms in (5.15) and recognizing that n_o is constant throughout the semiconductor yields

$$q \int_o^{t_s} n dz = C_o W(x) - q(Q_s - n_o t_s). \qquad (5.16)$$

Substituting (5.16) and (5.14) into (5.13) gives

$$I_d = \mu Z \left[C_o W(x) - q(Q_s - n_o t_s) \right] \frac{dV(x)}{dx} . \qquad (5.17)$$

This differential equation can be easily integrated along the channel if it is assumed that C_o and Q_s are both independent of x and W(x). For convenience the total insulator capacitance over the channel, C_T, and the threshold gate voltage necessary for the onset of conduction, V_T, are introduced.

$$C_T = C_o Z L \qquad (5.18)$$

and

$$V_T = \frac{q (Q_s - n_o t_s)}{C_o} . \qquad (5.19)$$

V_T can be regarded as a "turn-on" voltage when it is positive and a "turn-off" voltage when it is negative. Integrating (5.17) along the channel from source to drain yields

$$I_d = \frac{\mu C_T}{L^2} \left[(V_g - V_T) V_d - \frac{V_d^2}{2} \right] . \qquad (5.20)$$

Equation (5.20) relates the channel current to both the drain and gate voltages. It is valid up to the point where $\frac{\partial I_d}{\partial V_d} = 0$, at $V_d = (V_g - V_T)$,

which corresponds to the knee of the characteristic curve. For $V_d > (V_g - V_T)$ the slope of the characteristic is determined by the resistance of the pinched-off portion of channel shunted by the resistance of the bulk semiconductor. If both these resistances are high, the slope will be small, signifying good saturation of drain current.

Figure 5.9 is a plot of (5.20) presented to demonstrate the shape of a family of characteristic curves predicted by (5.20). The degree of similarity between the shapes of the curves of Figures 2.2 and 5.9 indicates the degree of confidence with which the theory of this section may be applied.

Although agreement between plots of (5.20) and observed TFT characteristics is good, the assumptions made during the derivation of (5.20) are substantial. The assumptions of the "gradual channel approximation" and perfect saturation of channel current after pinch-off have already been mentioned. Although the effective mobility of electrons in the semiconductor was taken as constant throughout the derivation, it has been shown (Waxman, et al, 1964) that electron mobility in polycrystalline CdS films is a strong function of both gate voltage and temperature. It has also been shown (de Graaf, 1965) that the threshold voltage, V_T, is not constant but a function of V_g. In spite of these limitations the foregoing analysis has described the generally accepted model used to explain the operation of insulated-gate transistors in general and TFTs in particular.

A semi-emperical method exists by which the above analysis may be refined to the extent that the variation of V_T with gate voltage is taken into account. This approach also yields information on the

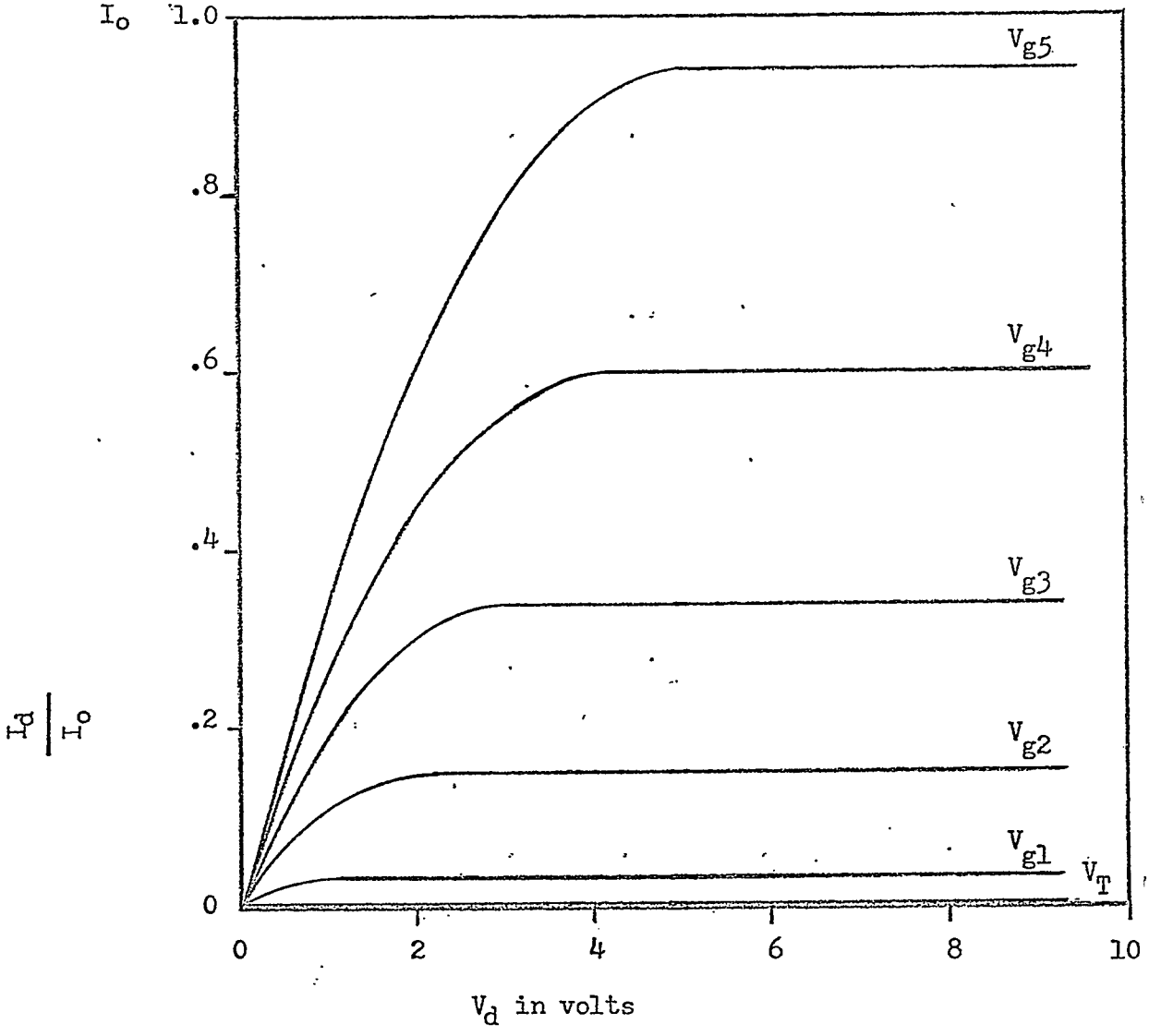


Figure 5.9 Plot of Equation 5.20

variation of channel potential in the x direction from source to drain.

One interpretation of the "gradual channel approximation" is that g in (5.13) can be considered to be solely a function of W (de Graaf, 1965). Expressing g as g(W) and integrating (5.13) from source to drain gives

$$I_d \int_o^x dx = \int_o^{V(x)} g(W)dV(x)$$

$$I_d = \frac{1}{x}\int_o^{V(x)} g(W)dV(x) .$$

For V_g held constant,

$$dW = -dV(x).$$

Therefore,

$$I_d = \frac{1}{x}\int_{V_g - V(x)}^{V_g} g(W)dW . \qquad (5.21)$$

For the specific case of x = L,

$$I_d = \frac{1}{L}\int_{V_g - V_d}^{V_g} g(W)dW . \qquad (5.22)$$

Differentiating (5.22) with respect to V_d and setting $V_d = 0$ gives

$$\left.\frac{\partial I_d}{\partial V_d}\right|_{V_d = 0} = \frac{1}{L} g(V_g) = G(V_g)$$

where $G(V_g)$ = total channel conductance for $V_d = 0$.

$G(V_g)$ may be very easily found for any TFT with the aid of a curve tracer and a plot of $G(V_g)$ versus V_g for a typical unit is shown in Figure 5.10. By graphical evaluation of the integral in (5.22) with the aid of Figure 5.11, the $I_d - V_d$ characteristic can be obtained for any given value of gate voltage. Figure 5.12 shows the good agreement that may exist between a measured characteristic curve and the corresponding curve calculated by the above method.

Fabrication run 73

Unit 5

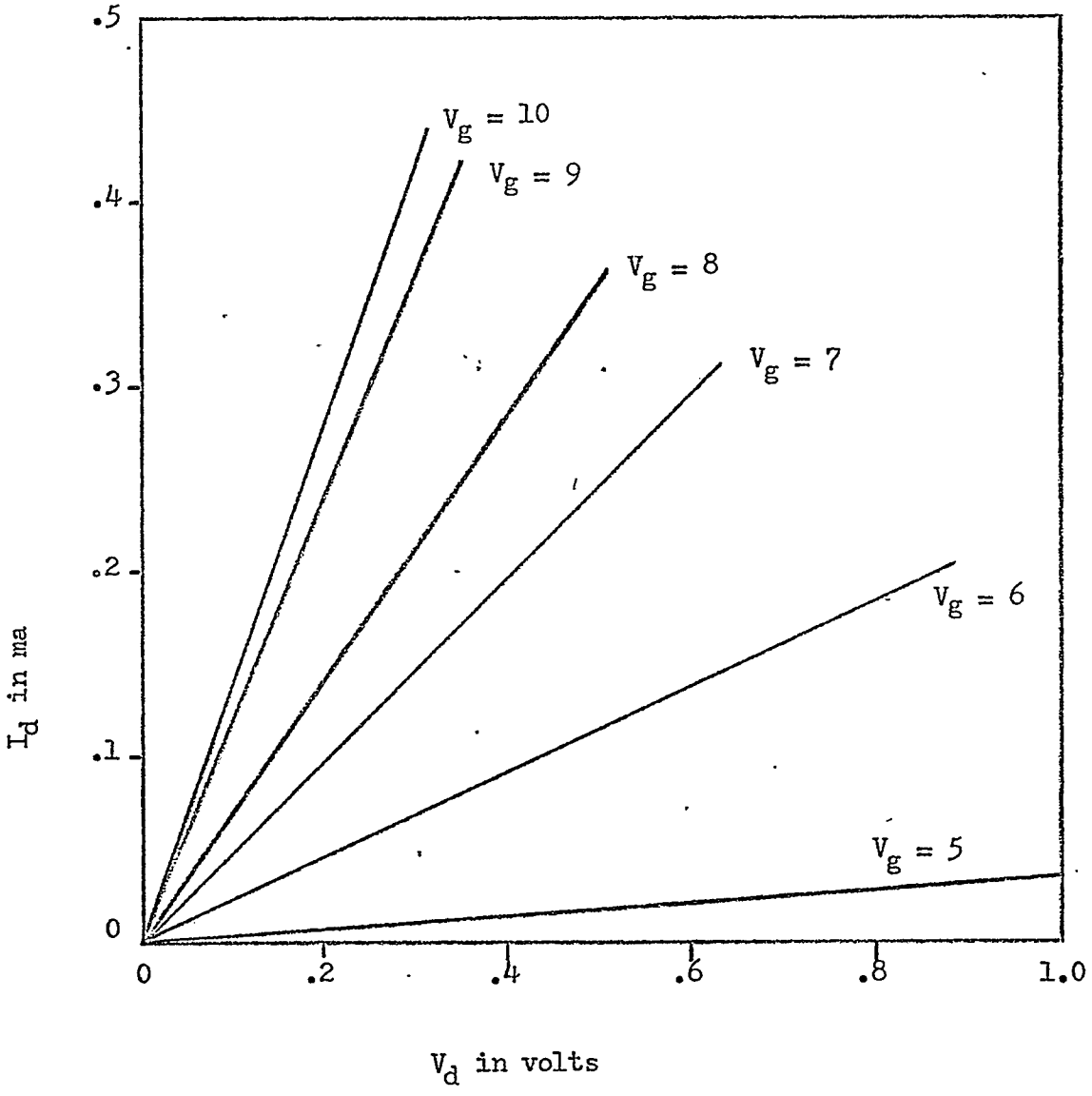


Figure 5.10 Tektronix 575 Curve Tracer Plot

Fabrication Run 73

Unit 5

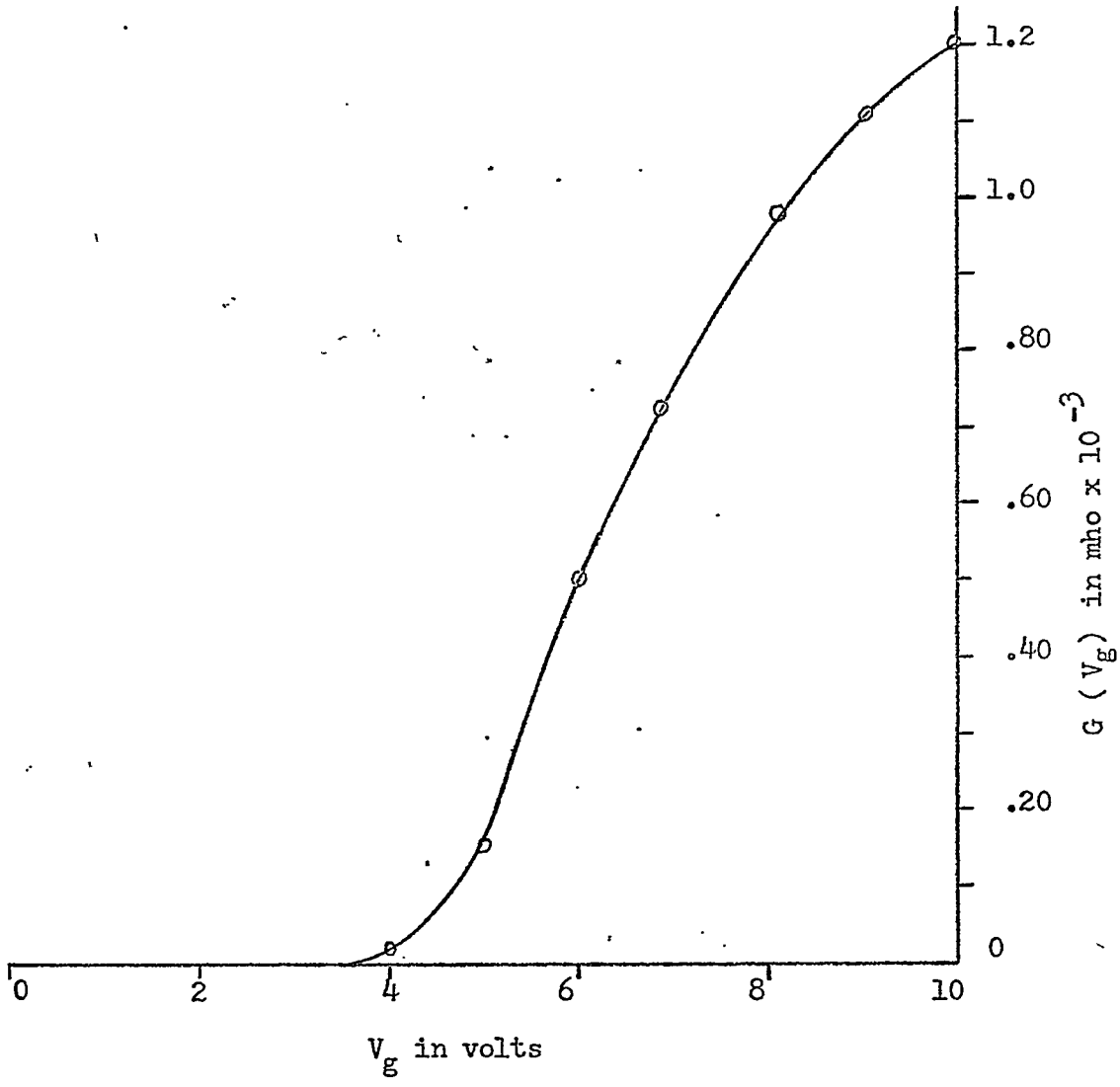


Figure 5.11 Plot of G (V_g) Versus V_g

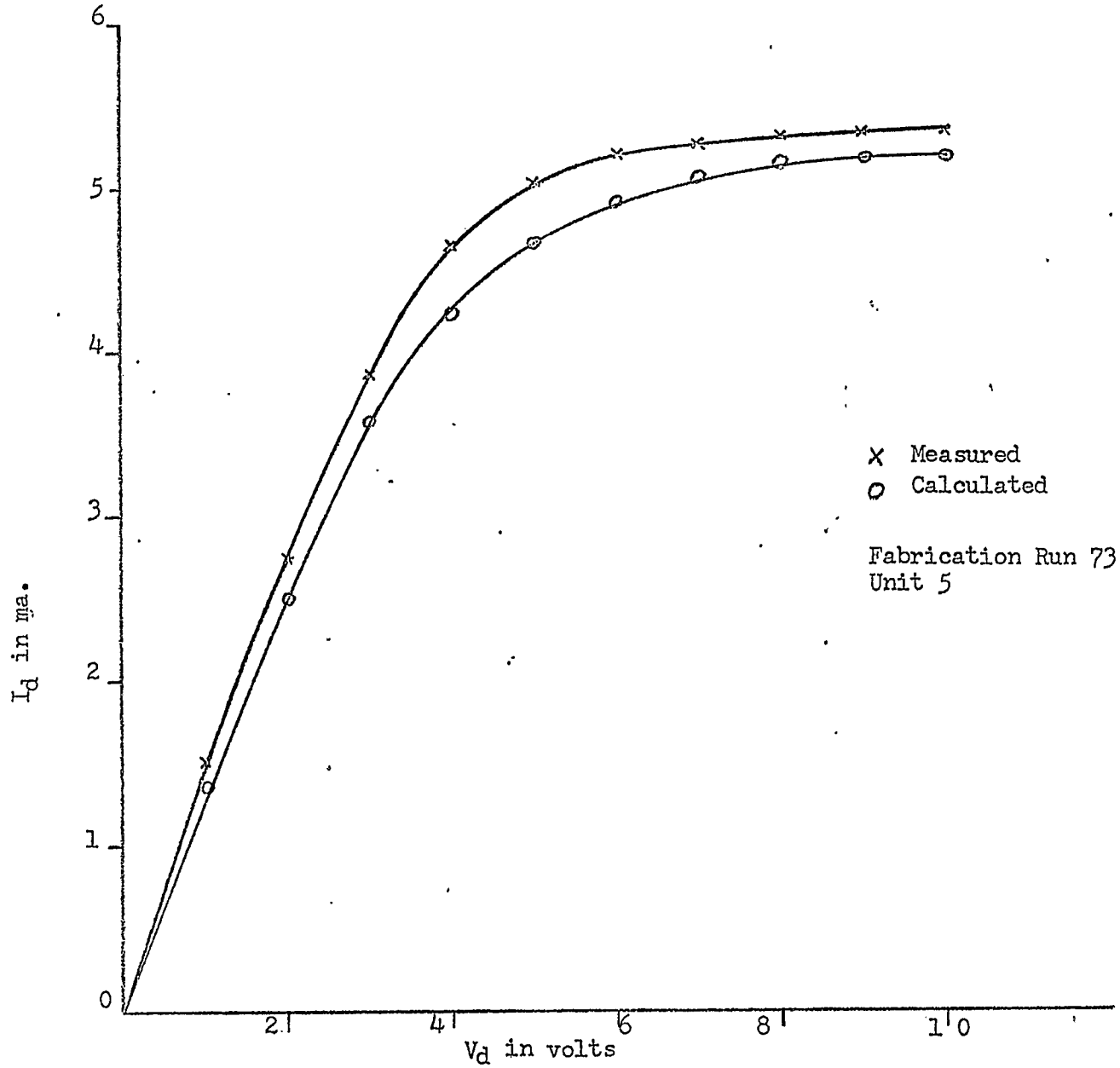


Figure 5.12 Measured and Calculated Characteristic Curve For $V_g = 10$.

Fabrication run 73
Unit 5

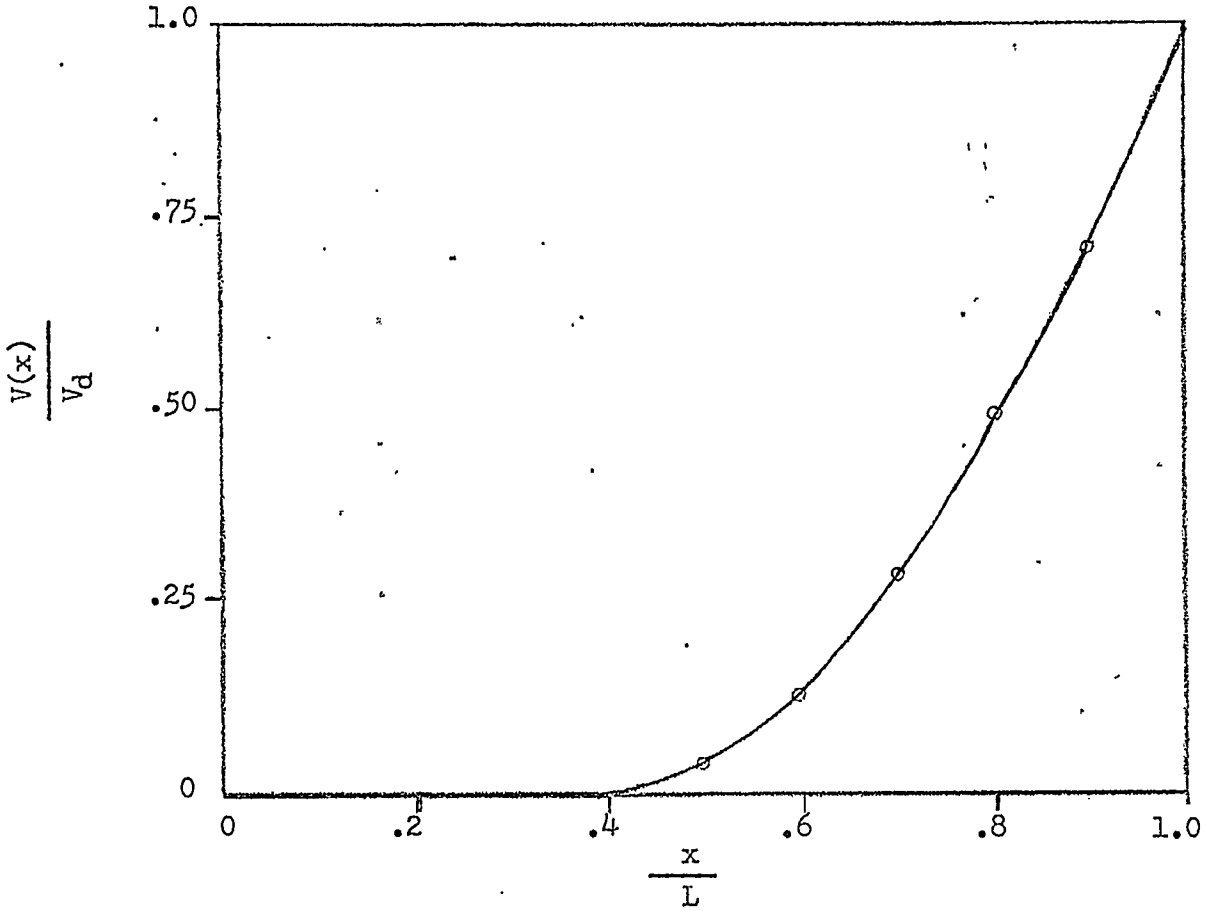


Figure 5.13 Potential Profile Along Conduction Channel

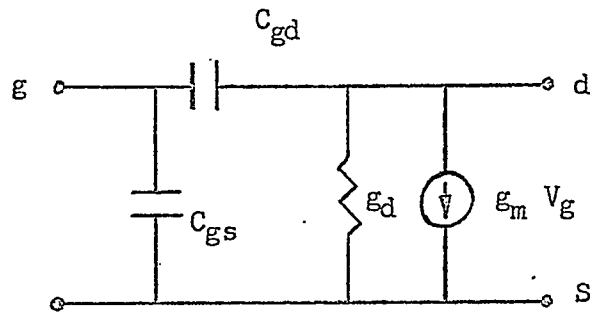
If (5.21) is divided by (5.22), since I_d must be equal at all points in the channel,

$$\frac{x}{L} = \frac{\int_{V_g-V(x)}^{V_g} g(W)dW}{\int_{V_g-V_d}^{V_g} g(W)dW} . \qquad (5.23)$$

A plot of V(x) versus x can now be obtained graphically from Figure 5.11 . The resulting potential profile from source to drain for the unit under consideration is shown in Figure 5.13 . It can be seen from Figure 5.13 that the rate of change of channel potential is greatest at the drain end of the channel. It is near the drain, therefore, that the gradual channel approximation would be expected to be least accurate.

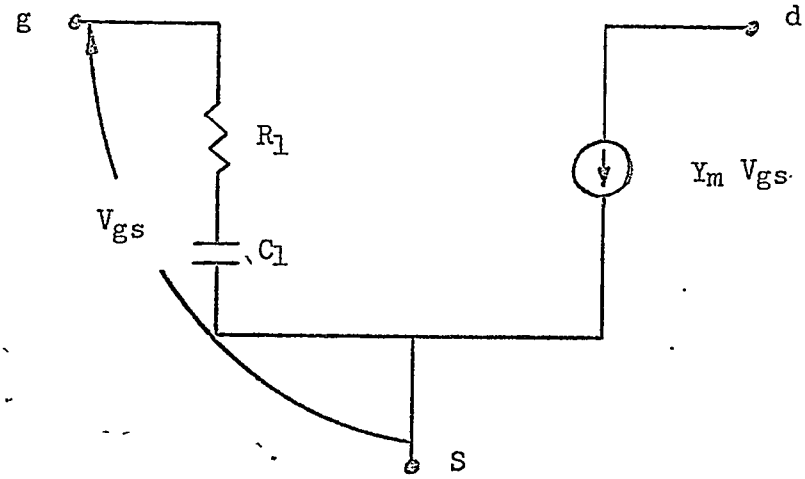
5.4 Small Signal Equivalent Circuits

In order to complete the present discussion of the conduction process in TFTs, two small signal TFT equivalent circuits are presented. Figure 5.14 shows an equivalent circuit representing the small signal operation of an insulated-gate transistor at low frequencies, while Figure 5.15 represents an insulated-gate transistor operating at high frequencies in the pinch-off mode. The high frequency circuit for the non-pinch-off region of operation has yet to be obtained. Both circuits shown are intrinsic equivalent circuits which do not include stray capacitances or lead or contact resistances. Perfect current saturation after channel pinch-off and negligible insulator conductance have been assumed.



Non - Pinch - Off	Pinch - Off
$g_m = \frac{\mu C_T}{L^2} V_d$	$g_m = \frac{\mu C_T}{L^2} (V_g - V_T)$
$g_d = \frac{\mu C_T}{L^2} (V_g - V_T - V_d)$	$g_d = 0$
$C_{gs} = \frac{2}{3} C_T \frac{[V_g - V_T][3(V_g - V_T) - 2V_d]}{[2(V_g - V_T) - V_d]^2}$	$C_{gs} = \frac{2}{3} C_T$
$C_{gd} = \frac{2}{3} C_T \frac{[3(V_g - V_T) - V_d][V_g - V_T - V_d]}{[2(V_g - V_T) - V_d]^2}$	$C_{gd} = 0$

Figure 5.14 Small Signal Equivalent Circuit for Insulated-Gate Transistor (After Sah, 1964).



$$R_1 = \frac{1}{5} \frac{L\, t_i}{K_i \epsilon_i \mu Z (V_g - V_T)}$$

$$C_1 = \frac{2}{3} C_T$$

$$Y_m = \frac{g_m}{1 + j\omega\tau}$$

$$g_m = \frac{\mu C_T (V_g - V_T)}{L^2}$$

$$\tau = \frac{4}{15} \frac{L^2}{\mu (V_g - V_T)}$$

Figure 5.15 High Frequency, Small Signal, Equivalent Circuit For Insulated-Gate Transistor At Pinch-Off (After Treleaven and Trofimenkoff, 1966).

The equivalent circuit parameters, g_m and g_d, of Figure 5.14 can be obtained directly from (5.20).

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d} \tag{5.24}$$

or

$$g_m = \frac{\mu C_T}{L^2} V_d \tag{5.25}$$

for the non-pinch-off case. To obtain g_m for the pinch-off case, $V_g - V_T$ is substituted for V_d in (5.25) resulting in

$$g_m = \frac{\mu C_T}{L^2}\left(V_g - V_T\right) \tag{5.26}$$

for the pinch-off case.

$$g_d = \left.\frac{\partial I_d}{\partial V_d}\right|_{V_g} \tag{5.27}$$

or

$$g_d = \frac{\mu C_T}{L^2}\left[(V_g - V_T) - V_d\right] \tag{5.28}$$

for the case of non-pinch-off and

$$g_d = 0 \tag{5.29}$$

for the pinch-off case.

The values of the remaining circuit elements of Figure 5.14 and those of Figure 5.15 are derived or indicated in the references on the appropriate diagrams. The presentation of these two small signal TFT equivalent circuits brings to a logical conclusion the subject of the conduction process in TFTs.

6. EXPERIMENTAL

6.1 Introduction

The experimental results, and information that can be derived therefrom, that comprise this chapter have been divided for convenience into two sections. The first section details an experiment concerned with the materials properties of the TFT semiconductor film. The semiconductor film is treated as a separate entity in this section and its application as a TFT element is not considered. The second section treats the electronic properties of the semiconductor film, and indeed is largely comprised of calculations of these properties from experimental data. Electronic parameters of interest for which a value will be obtained are conductivity and free electron concentration of the bulk semiconductor, effective electron mobility, conduction channel thickness, and Fermi energy level. These parameters are derived using a model in which the dominant traps are considered to be at the semiconductor-insulator interface. A numerical estimate is also made of this surface density of traps. The accuracy, limitations, and range of applicability of experimental results and calculations are discussed. Agreement or disagreement with the results of other workers in the field is commented upon where applicable.

6.2 Materials Properties of the Semiconductor

In order to investigate the basic properties of the semiconductor film used in TFT fabrication in the thin-film laboratory, an experiment was undertaken in which evidence of crystalline structure in the semiconductor film was sought. A special deposition run was made in which the thin-film structure shown in Figure 6.1(a) was deposited.

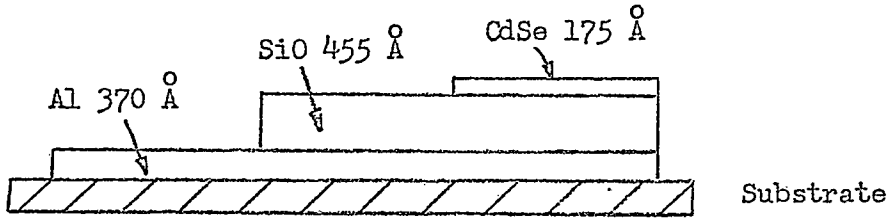


Figure 6.1(a)

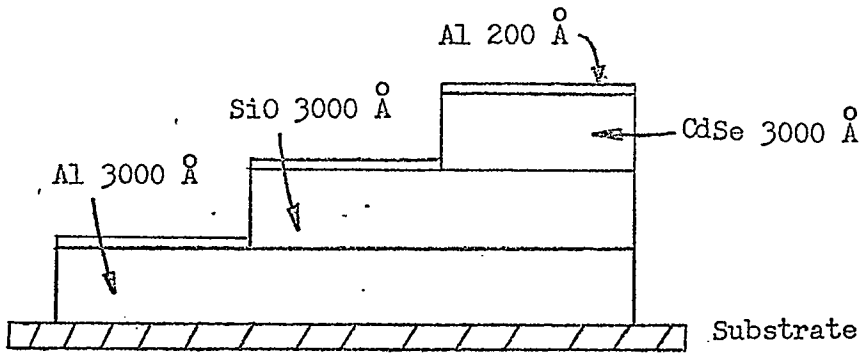


Figure 6.1(b)

Figure 6.1 Samples Used in X-ray Measurements

The deposition sequence and film thicknesses were designed to coincide with those used in the TFT fabrication process. Al of thickness 370 angstroms was deposited first because the Al gate is deposited first in actual fabrication runs. A thickness of 455 angstroms of SiO was then deposited as is done in insulator deposition, followed by 175 angstroms of CdSe.

The three discrete areas of the sample of Figure 6.1(a) were then investigated by X-ray techniques. Back reflection photographs were taken of all three areas using a Phillips X-ray machine with a Cu K_{α} source and a Universal flat plate X-ray diffraction camera. No evidence of preferred crystallite orientation or of appreciable crystallite size was found in the semiconductor film. It was therefore tentatively concluded that the semiconductor film was amorphous. The insulator was also found to be amorphous, as expected. Evidence of semiconductor film structure from X-ray techniques was also sought in the same sample using a Phillips Electronic Instruments diffractometer equipped with a Cu K_{α} source, a geiger counter detector and graphical readout. Once again, no evidence was found of crystalline structure in the semiconductor.

The substantially thicker sample shown in Figure 6.1(b) was then obtained and investigated as before using only the diffractometer. A definite reflected intensity peak indicating crystalline structure in the CdSe layer was obtained. The SiO layer once again proved to be amorphous. Two possible explanations are offered for the lack of evidence indicating crystalline structure in the CdSe from the experiments involving the thin-layered sample. It is possible that the CdSe

film begins to grow in an amorphous manner with the degree of crystallinity increasing as the film grows thicker. The 175 angstrom CdSe layer was too thin for detectable crystallinity to have appeared while the 3000 angstrom layer had developed an appreciable degree of crystallinity. A second explanation is that the thin CdSe layer was crystalline but that the intensity of diffracted X-rays was too small to detect. Studies of this nature of the crystalline form of the CdSe layer would be greatly aided by the availability of electron microscope techniques.

6.3 Electronic Properties of the Semiconductor

A reasonably complete characterization of the electronic properties of polycrystalline CdSe must include an estimate of the effective mobility of electrons, μ, in the semiconductor. The concept of effective mobility was discussed in Section 3.2. In order to obtain this estimate a comparison was made between observed TFT characteristic curves and the theoretical plot of Figure 5.9. An assumption implicit in this procedure is that (5.20) describes TFT action accurately. This assumption was discussed and shown to be reasonable in section 5.3. The following calculation will be done for one value of V_g. The value of μ obtained and the estimated experimental error will be for that value of V_g. Variations in μ with V_g up to a factor of two have been reported for polycrystalline CdS films with SiO insulators (Waxman, et al, 1964), over a range of values of V_g from 0 - 10 volts.

For the present calculation of μ, three TFTs of similar geometry were chosen from deposition lot 75. The data required for the calculation of μ and the results of those calculation are shown in Table 6.1.

From Fabrication lot 75

Unit	35	36	37
I_d in ma	1.50	1.35	1.45
V_d in volts	.25	.25	.25
V_g in volts	10	10	10
V_T in volts	-2	-2	-2
Z in mm	4.26	4.26	4.24
L in microns	65	70	70
t in angstroms	455	455	455
μ in cm^2/volt sec.	79	77	83

Table 6.1 Data for Calculation of Effective Electron Mobility

The essentials of the calculation for unit 35 will be presented here.

From (5.20),

$$I_d = \frac{\mu C_T}{L^2}\left[(V_g - V_T)\,V_d - \frac{V_d^2}{2}\right]$$

$$= \frac{K_i \epsilon_o Z}{Lt_i}\left[(V_g - V_T)\,V_d - \frac{V_d^2}{2}\right]. \qquad (6.1)$$

From experimental data, $I_d = 1.50$ ma for the bias conditions and geometrical measurements shown in Table 6.1. The dielectric constant of the insulator is taken as 5, a compromise between the SiO value of 6 and the SiO_2 value of 4 made necessary by the unknown composition of the insulator as described in Section 4.2. Substituting known values into (6.1) leaves μ as the only unknown. Solving for μ yields,

$$\mu = 79 \text{ cm}^2/\text{volt sec.}$$

Similar calculation for units 36 and 37 yield values of $\mu = 77$ cm^2/volt sec. and $\mu = 83$ cm^2/volt sec. An average value of 80 cm^2/volt sec. will be referred to in later sections. This value is reasonable in view of the rather extensive results published for CdS (Waxman, et al, 1964) that quote mobility values in the 30 cm^2/volt sec. range. The major source of error in this calculation would be expected to be in the value of K_i used because of the uncertainty of the composition of the insulator as already discussed. The worst case error due to this cause would be 25%. The value of μ calculated for the conditions given can therefore be taken as (60 - 100) cm^2/volt sec.

The next parameter of the semiconductor to be determined from experimental data is the bulk semiconductor free electron concentration, n_o. The necessary experimental data is summarized in Figure 6.2.

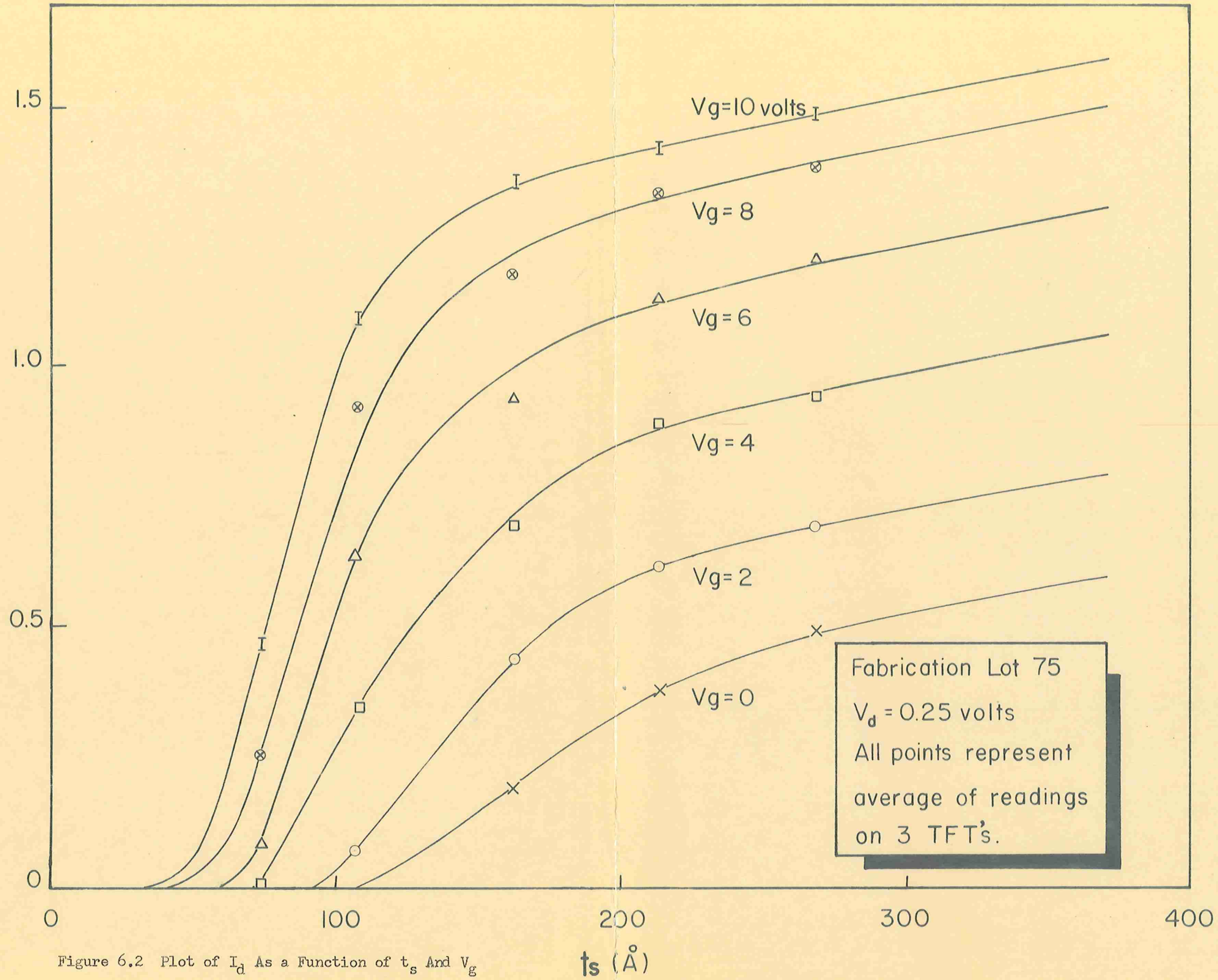


Figure 6.2 Plot of I_d As a Function of t_s And V_g

Before the determination of n_o is carried out, the shape of the curves of Figure 6.2 must be explained. The model proposed for this purpose consists of a semiconductor layer containing a uniform concentration of donors. The non-uniform shape of the I_d versus t_s curve of Figure 6.2 suggests a non-uniform distribution of traps in the semiconductor. The negligible conductance of the semiconductor film up to a significant value of t_s suggests surface traps. The existence of surface states in polycrystalline semiconductor films is well established (Weimer,1962). The shape of the curves of Figure 6.2 will therefore be explained in terms of a model consisting of a semiconductor film with a uniform distribution of donors and a surface density of interface traps. Consider the situation at a number of values of t_s. When t_s is small, for instance in the 25 angstrom range of Figure 6.2, the number of surface traps substantially outnumbers the number of donors in the semiconductor film. Most of the donor electrons are trapped and the conductance of the semiconductor is negligible. An alternate possibility for the negligible conductance at small values of t_s is that the initial nucleons that formed on the substrate have not yet grown together and the semiconductor film is not yet continuous. As t_s increases further, the conductance of the semiconductor film increases very rapidly with t_s for any specified value of V_g, as shown by the steeply rising curve sections of Figure 6.2. Three possible mechanisms are suggested to explain this sharp rise of I_d with t_s. Firstly, as t_s increases, the total number of donors in the film increases in proportion to the total volume of the semiconductor while the number of surface traps remains constant. At some intermediate value of t_s

sufficient donors are available in the semiconductor to fill the surface traps and to release sufficient electrons to the conduction band to cause the onset of conduction. The variation of t_s required for the onset of conduction with V_g is the result of additional electrons induced in the semiconductor by capacitor action. The higher V_g, the greater the number of induced electrons, and the smaller the value of t_s required for the onset of conduction. A second contributing factor to the rapid increase of I_d with t_s is an increase in μ due to decreased surface scattering. As t_s increases, so does the average distance of free electrons below the semiconductor-insulator interface. The effective electron mobility therefore increases due to decreased ion scattering by the charged surface traps. This argument in no way contradicts the prior use of the assumption of constant μ, in that t_s, now being considered as a variable, was constant in the former arguments. A third factor in the rapid rise of I_d with t_s in Figure 6.2 may be that the initial nucleons are growing together to form a continuous semiconductor film. However, the fact that g_m has increased to its greatest value, that of the relatively thick semiconductor film, for at least part of the steeply-rising curve portion indicates that this explanation does not alone account for the rapid increase in conductance. As t_s increases in value past the steeply rising portion of the curves, the slope of the I_d versus t_s curve for a given V_g decreases and remains at a small, constant value as t_s grows. In this region of the plot, t_s is large enough so that the conduction channel described in Section 5.2 has formed. The small rate of increase of I_d with t_s as t_s grows large is due to bulk semiconductor conductance being added in parallel with the channel. In this

thick semiconductor region, in which t_s is significantly greater than the channel thickness, there is a correlation between the theoretical model of Section 5.2 and the physical model under consideration.

To calculate the free electron density in the bulk semiconductor, n_o, the slope of the I_d versus t_s curves for the thick semiconductor region can therefore be used. For this region,

$$\frac{dI_d}{dt_s} = \frac{(q \mu n_o) \; Z \; V_d}{L} \; . \qquad (6.2)$$

From Figure 6.2, taking the $V_g = 10$ curve as well-defined and typical,

$$\frac{dI_d}{dt_s} = 3.1 \times 10^2 \text{ coulomb/cm sec.},$$

for t_s between 200 and 275 angstroms.

From the previous calculation of μ and the averages of measurements taken on the TFTs of lot 75 and listed in Table 6.1,

$\mu = 80$ cm^2/volt sec.

$Z = 4.25$ mm

$L = 68$ microns

$V = 0.25$ volts.

Substitution of values into (6.2) yields a bulk conductivity, $q \mu n_o$, of 20 mho cm^{-1} or a resistivity of 0.05 ohm cm, a not unreasonable figure. Substitution of values of q and μ into the conductivity expression yields,

$$n_o = 1.5 \times 10^{18} \text{ per cm}^3.$$

Besides the estimated error of 25% in the calculation of μ, the measurement errors might be expected to raise the accumulated error in the calculation of n_o to the neighborhood of a factor of two. The calculated value of n_o can therefore be taken as $(7.5 \times 10^{17} - 3 \times 10^{18})$ per cm^3.

Since μ varies with both V_g and t_s for small values of t_s, the above method for finding n_o is inconvenient in that μ must first be determined for each individual case. A much more direct method, valid for all regions of Figure 6.2, exists for obtaining n_o directly from Figure 6.2. This method will be demonstrated for the same set of conditions as the former calculations of μ and n_o. The previous calculations of μ and n_o were made for the region of Figure 6.2 of t_s = 200 angstroms, V_g = 10 volts, and I_d = 1.50 ma. In this region, as in the other regions of Figure 6.2, I_d is a function of both V_g and t_s. Consider the magnitude of increments of I_d for increments in V_g and t_s respectively. As the variations of μ with V_g and t_s would be expected to be slowly varying functions as compared to the variations of I_d with V_g and t_s, μ is considered to be essentially constant for small changes in V_g and t_s. The conductance of the semiconductor layer therefore varies directly with the number of free electrons in the semiconductor. Therefore,

$$\frac{\Delta I_{d1}}{\Delta I_{d2}} = \frac{n_o \Delta t_s}{\frac{\epsilon_o K_i \Delta V_g}{q t_i}} \qquad (6.3)$$

where I_{d1} = change in I_d due to change in t_s

I_{d2} = change in I_d due to change in V_g.

From Figure 6.2,

$$\frac{\Delta I_{d1}}{\Delta t_s} = 3.1 \times 10^5 \text{ ma/cm}$$

and

$$\frac{\Delta I_{d2}}{\Delta V_g} = 0.075 \text{ ma/volt.}$$

Substituting K_i = 5, t_i = 455 angstroms, and the above values into

(6.3) yields n_o directly.

$$n_o = 2.5 \times 10^{18} \text{ per cm}^3.$$

This value of n_o is within the experimental limits estimated for the former calculation of n_o.

The next parameter for which a value will be obtained is the surface density of charged traps, N_{ST} per cm^2, from the data of Figure 6.2. Inspection of Figure 6.2 reveals the $V_g = 0$ line intersecting the $I_d = 0$ line at $t_s = 100$ angstroms. In other words, at $t_s = 100$ angstroms the turn-on voltage is zero. The accuracy of the 100 angstrom figure is limited by the accuracy of the deposition thickness monitor described in Section 2.4. This monitor was calibrated by interference microscopy techniques, but an average error of 15% in t_s can still be anticipated with a worst-case error of 30%. The data summarized in Figure 6.2 was taken after initial stabilization of the TFT characteristics was reached on a Tektronix 575 Curve Tracer. The smallest current that can be conveniently detected with that instrument is .001 ma. If no traps were present the semiconductor film thickness needed to conduct this current is easily calculated. Assuming the simple bulk conductivity model,

$$I_d = \frac{q \mu n_o Z t_s V_d}{L}, \qquad (6.4)$$

Substituting $n_o = 2.0 \times 10^{18}/cm^3$

$\mu = 80$ cm^2/volt sec.

$I_d = 0.001$ ma

$V_d = 0.25$ volt

$Z = 4.26$ mm

$L = 70$ microns

into (6.4) yields $t_s = 0.25$ angstroms.

Since this figure is negligible with respect to 100 angstroms, and since the fact that the turn-on voltage is zero indicates that almost all electrons induced in the semiconductor when a gate voltage is applied are free, it can be concluded that essentially all the donor electrons from the 100 angstroms of semiconductor are required to fill all the traps.

Therefore $N_{ST} = n_o t_s$.

Substituting $n_o = 2.0 \times 10^{18}/cm^3$,

$t_s = 100$ angstroms

yields

$$N_{ST} = 2.0 \times 10^{12}/cm^2.$$

To illustrate the variation of N_{ST} with V_g, consider the situation at $t_s = 100$ angstroms, as before, and $V_g = 10$ volts. The total number of electrons per unit area that will be trapped or free, contributed by the bulk semiconductor, is

$$n_o t_s = 2.0 \times 10^{12}/cm^2.$$

The total number of induced electrons per unit area is

$$n_{in} = \frac{\epsilon_o K_i V_g}{q t_i}. \qquad (6.5)$$

For $K_i = 5$

$t_i = 455$ angstroms

$V_g = 10$ volts,

$n_{in} = 6.1 \times 10^{12}/cm^2.$

The total number of conduction electrons per unit area is

$$n_{ca} = \frac{I_d L}{q \mu Z V_d}. \qquad (6.6)$$

For I_d = 1.1 ma (from Figure 6.2)

V_d = 0.25 volt

μ = 80 cm^2/volt sec.

Z = 4.26 mm

L = 70 microns,

n_{ca} = 5.7 x $10^{12}/cm^2$.

Since all electrons in the semiconductor must be either free or trapped,

$$N_{ST} = n_o t_s + n_{in} - n_{ca}. \qquad (6.7)$$

Substituting known values into (6.7) yields

$$N_{ST} = 2.4 \times 10^{12}/cm^2.$$

The percentage of trapped electrons to total electrons is

$$\frac{N_{ST}}{N_{ST} + n_{ca}} \times 100\% \text{ which equals } 30\%.$$

The variation of N_{ST} with t_s can also be calculated. Table 6.2 describes the variation of N_{ST} with V_g and Table 6.3, the variation of N_{ST} with t_s. The values of N_{ST} found are similar to the estimated surface density of traps, (10^{12} - 10^{13}) per cm^2, for CdS TFTs with SiO insulators (Weimer, 1962). The values of N_{ST} discussed here are the total number of charged traps on both semiconductor surfaces. Depending on the geometry of the individual TFT, the number of trapped electrons may be divided in some proportion between the two interfaces of the actual TFT semiconductor film.

The conduction channel thickness, L_c, is of interest and can now be estimated. The assumption will be made that t_s is sufficiently greater than L_c so that the theory developed for the infinitely thick semiconductor of Section 5.2 can be applied. This assumption restricts

	$n_o t_s$	n_{in}	n_{tot}	$\frac{n_{in}}{n_{tot}} \times 100\%$	n_{ca}	N_{ST}	$\frac{N_{ST}}{n_{tot}} \times 100\%$
$V_g = 0$	4.0×10^{12}	0	4.0×10^{12}	0	2.1×10^{12}	1.9×10^{12}	48 %
$V_g = 2$	4.0×10^{12}	1.2×10^{12}	5.2×10^{12}	23 %	3.3×10^{12}	1.9×10^{12}	38 %
$V_g = 6$	4.0×10^{12}	3.7×10^{12}	7.7×10^{12}	48 %	5.7×10^{12}	2.0×10^{12}	27 %
$V_g = 10$	4.0×10^{12}	6.1×10^{12}	10.1×10^{12}	60 %	7.6×10^{12}	2.5×10^{12}	25 %

Table 6.2 Variation Of N_{ST} With V_g, t_s = 200 Angstroms

	$n_o t_s$	n_{in}	n_{tot}	$\frac{n_{in}}{n_{tot}} \times 100\%$	n_{ca}	N_{ST}	$\frac{N_{ST}}{n_{tot}} \times 100\%$
$t_s = 50\text{Å}$	1.0×10^{12}	3.7×10^{12}	4.7×10^{12}	76 %	0	4.7×10^{12}	100 %
$t_s = 100\text{Å}$	2.0×10^{12}	3.7×10^{12}	5.7×10^{12}	63 %	3.4×10^{12}	2.3×10^{12}	41 %
$t_s = 150\text{Å}$	3.0×10^{12}	3.7×10^{12}	6.7×10^{12}	55 %	4.6×10^{12}	2.1×10^{12}	31 %
$t_s = 200\text{Å}$	5.0×10^{12}	3.7×10^{12}	8.7×10^{12}	41 %	6.3×10^{12}	2.4×10^{12}	27 %

× Table 6.3 Variation of N_{ST} With t_s, $V_g = 6$ volts

the applicability of this calculation to the thick semiconductor region of Figure 6.2 where the conduction channel has formed and the small slope of the I_d versus t_s curves is due to the conductance of bulk semiconductor being added in parallel with the conductance of the channel.

For $V_g = 4$ volts, $t_i = 455$ angstroms, and $N_{ST} = 2 \times 10^{12}/cm^2$, interpolation on Figures 5.7 and 5.8 reveal that

$$L_c \simeq 23 \text{ angstroms.}$$

The last electronic parameter of polycrystalline CdSe to be estimated is the Fermi energy level. Fabrication lot 63, composed of groups of TFTs with different semiconductor film thicknesses, but otherwise identical, was chosen to be used for an experiment in which I_d was monitored as a function of temperature and gate voltage. The results of this experiment are summarized in Figure 6.3. Throughout the experiment V_d was held constant at 0.5 volt in order to stay well away from saturation and to keep W(x) approximately constant at all values of x between source and drain.

In order to interpret the results of Figure 6.3, including the activation energies suggested by the straight-line portions of the plot, certain assumptions are necessary. The effective electron mobility in the semiconductor is assumed to be constant and Boltzmann statistics are assumed to be valid. Because of the latter assumption the density of conduction electrons can be expressed by (3.4) as

$$n = N_c \exp\left[-\frac{E_c - E_F}{kT}\right] . \qquad (3.4)$$

The exponential factor in (3.4) leads to the interpretation of the activation energies indicated in Figure 6.3 as the energy difference

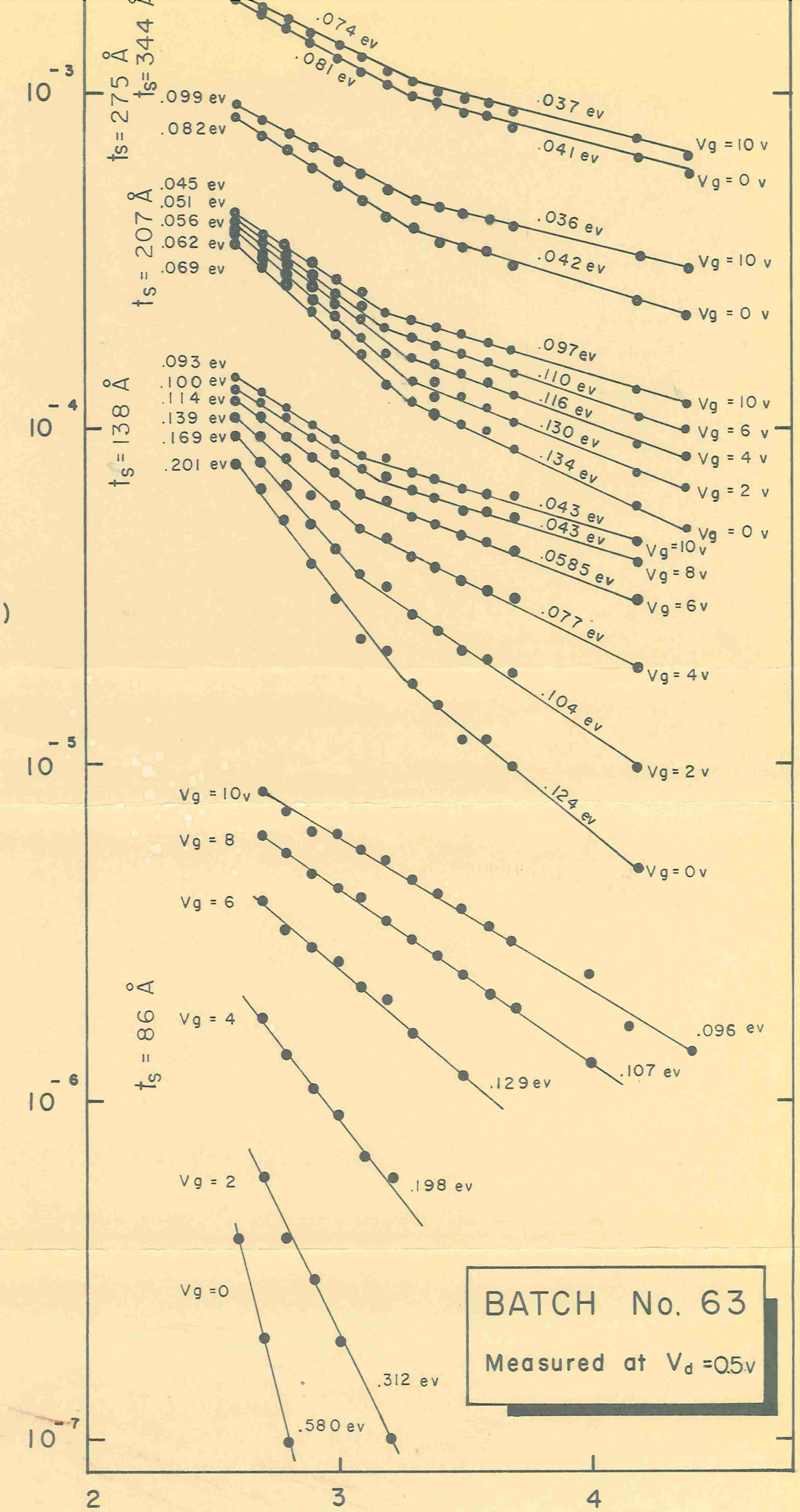


Figure 6.3 Plot of Log I_d Versus $\frac{1}{T}$

between the Fermi level and the bottom of the conduction band.

It can be seen from Figure 6.3 that Fermi level is a definite function of semiconductor film thickness with larger values of Fermi energy corresponding to larger values of semiconductor thickness. The results are expected in view of the semiconductor model presented earlier in this section. When t_s is small the number of donors is small, the traps are only partially occupied, and the Fermi level is low. When t_s is large the number of donors is large, the traps are relatively full, and the Fermi level is correspondingly high. The results of Figure 6.3 are therefore a further justification for the semiconductor model proposed in this section.

The bulk semiconductor conductivity and free electron density, the effective mobility of electrons, the surface density of charged interface traps, the conduction channel thickness, and the Fermi energy level have all been estimated for polycrystalline CdSe. The results have been shown to be self consistent and consistent with the published results of other workers in the field.

7. CONCLUSIONS

A theoretical and experimental study of the properties of the semiconductor layer of TFTs vacuum deposited in the Department of Electrical Engineering was carried out in conjunction with the current TFT research program.

Information from various sources on the properties of polycrystalline semiconductors and Cd Se was obtained and coordinated to describe polycrystalline Cd Se as a TFT element. Descriptive comparisons were made with the more familiar properties of single-crystal semiconductors. Because of it's energy band structure, Cd Se conducts current essentially only by electron flow. The effect of holes in the conduction process in Cd Se is negligible.

The potential, electric field, and free electron concentration in an incremental thin-film transistor section were described for the case of no surface traps and for the case of a sheet of negative charge, corresponding to trapped electrons, existing at the semiconductor-insulator interface. A surface conduction channel was found to form in the semiconductor, the depth of which was dependent on gate voltage and interface charge. An equation was derived describing TFT operation and good correlation with observed characteristic curves was noted. An equivalent circuit was developed to describe the small-signal, high frequency response of the intrinsic insulated-gate transistor structure for the pinch-off mode of operation.

Crystalline structure was found by X-ray diffraction to exist in a 3000 angstrom thick film. The bulk conductivity of the polycrystalline

CdSe films investigated was found to be approximately 20 mho cm^{-1}; the free electron concentration (1 - 3) 10^{18}/ cm^3; the effective electron mobility (60 - 100) cm^2/ volt sec; and the total number of charged traps per unit area approximately 2 x 10^{12}/ cm^2. The variation of this surface density of charged traps with both gate voltage and semiconductor film thickness was demonstrated. A theoretical model, used to account for experimental results, indicated that the thickness of the surface conduction channel was approximately 23 angstroms. The Fermi level in the semiconductor was determined from an Arrhenius plot and found to be a function of semiconductor film thickness in accordance with the model.

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