Presented to the Engineering Library

Andrew D Stanford

18.5.83

A STUDY OF
THE
THIN FILM TRANSISTOR

A Thesis

Submitted to the Faculty of Graduate Studies

in Partial Fulfilment of the Requirements

for the Degree of

Doctor of Philosophy

in the Department of Electrical Engineering

University of Saskatchewan

by

Eugene John Swystun

Saskatoon, Saskatchewan

March 1968

Dedication

This thesis is dedicated first,

to my wife, Corinne,

for her continual encouragement and understanding.

Secondly, dedication is made

to my mother and father

for their guidance throughout the years.

University of Saskatchewan

ELECTRICAL ENGINEERING ABSTRACT 68A99

"A Study of the Thin Film Transistor"

Student: E.J. Swystun Supervisors: J.M. Bradley
and A.C. Tickle

PH.D. Thesis presented to the College of Graduate Studies
March 1968

ABSTRACT

The thin film transistor appears to have significant potential. However, its practical applications are severly limited by difficulties which exist with the present device which arise from the fact that insufficient information is available concerning the TFT. The most formidable problem is that of the device's electrical instability. It was the aim of this work to provide some of the required information.

Two distinct forms of instability were observed in the TFT; a positive and negative drift. The positive drift was accounted for by a model which invokes mobile insulator ions. The observed asymmetrical drift rate observed with an Al-CdSe-SiO_2 system was accounted for by a difference in activation energy for the release of ions from insulator interface ionic traps. The activation energies were found to be 0.51 ev for the Al-SiO_2 interface, and 0.41 ev for the SiO_2-CdSe interface. The traps widths were found to be 15 Å and 13 Å respectively. The presence of water vapour enhanced the magnitude and rate

of the positive drift, but could not induce it if it was not present. The negative drift was accounted for by the presence of electron trapping states. These were found to be associated dominantly with the surfaces. A model was formulated in which one component was at the semiconductor-insulator interface while a second component was in the insulator immediately next to the semiconductor. Electrons from the semiconductor tunneled into these with a time constant which was an inverse exponential function of the distance of the trap from the interface.

Due to the dominant surface trapping conduction was shown to initiate in the interior of the semiconductor, at a point determined by the relative trap concentrations of the two semiconductor surfaces. The effects of surface trapping on the enhancement of the conduction with increasing gate voltage is discussed in detail.

Theory and experimental results are presented which show that a maximum semiconductor depletion depth phenomenon exists in the TFT. This is used to show what basic relationship exists between semiconductor thickness and current saturation of the devices electrical characteristics. A novel method for determining the ionized donor concentration, the electron mobility, and the back surface depletion region thickness is described. It makes use of simultaneous capacitance-voltage and transfer characteristic measurements.

An experimental thin film integrated circuit is described. It demonstrates some of the possible advantages of thin film circuitry.

ACKNOWLEDGEMENT

The author is grateful to Professors J. Bradley and A.C. Tickle for their supervision and consultation. He also wishes to thank Mr. O. Turriff and Mr. G. Skopik for preparation of the TFT's.

This work was supported by the National Research Council of Canada under Grants No. A-1818, E-847, A-3380, and A-3382, and the Defence Research Board of Canada under Grant No. 5501-30, and 5501-32.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. INTRODUCTION

1.1 General Introduction

The mass production of low-cost, microminiature, integrated circuits, incorporating active and passive elements in a single unit is expected to revolutionalize electronic technology. In recent years, the increasing demand for many complex circuits has been accompanied by severe restrictions on their permissable size and weight. However, with integrated circuits it is possible to achieve a very high packing density of extremely small components. An additional advantage is that due to the minute size of the actual components and the nature of their construction, they promise to be very resistant to extreme physical stresses.

Circuits whose active and passive components are formed within the surface of single crystal silicon are already commercially available.(1) However, due to complex production processes which incorporate a number of distinct operations such as cycles of oxidation, photoetching, diffusion, and epitaxial growth, such circuits tend to be relatively expensive. They are also limited in complexity by the electrical properties of the underlying chip of silicon.

An alternative approach which has received wide attention is to deposit all components and connections by thin film techniques upon an inert insulating substrate.[2] Much work has been done on the fabrication of thin film resistors and capacitors,[3] so that the techniques here have reached a high degree of advancement. The fundamental weakness of the thin film approach has been the lack of a suitable active device that could be prepared by thin film techniques. Research in recent years[2] has produced a device which appears to be most promising for the role. It is commonly known as the insulated gate thin film transistor (TFT).

The successful development of such an active device could have a profound effect on the electronics industry. Integrated circuits could be manufactured with a minimum of equipment and production procedure. Since all the components of the circuits would undergo the same fabrication process, the production system would lend itself easily to automation. This could bring the cost of electronics to a very low level.

1.2 History of the TFT

1.2.1 The field effect idea

The earliest reference for amplifying elements having a structure with an insulated control electrode is found in material patented by J.E. Lilienfeld in 1926[4] and later two succeeding patents filed in 1928[5,6] Lilienfeld

described a method controlling the flow of electric current in a solid of minute thickness by establishing an "electrostatic influence in the proximity of the current flow." His proposed device is seen in Figure 1.1.

In 1935 another patent application was made by O. Heil.[7] He describes a field effect device with either one or two "gate" electrodes for the control of current, as shown in Figure 1.1. Heil's idea of a field effect device was stated as follows:

> "An electrical amplifier or other control arrangement or device wherein one or more thin layers of semi-conductor transversed by current is or are varied in resistance in accordance with control voltage applied to one or more control electrodes arranged close to and insulated from said semi-conductor layer or layers so as to be in electrostatic association therewith."

It is remarkable how these statements made many years ago closely describe the field effect transistors including the thin film transistors only recently reported in literature.

1.2.2 Recent work

A more relevant reference for the thin film transistor (TFT) was a note by Shockley and Pearson[8] entitled "Conductivity Modulation" published in 1948. In their experiment, a thin film of germanium was evaporated on one side of a mica sheet between laterally spaced contacts. A metal film was evaporated on the other side forming the field electrode or "gate" as it is now commonly called. By

March 7, 1933. J. E. LILIENFELD 1,900,018

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig. 1.

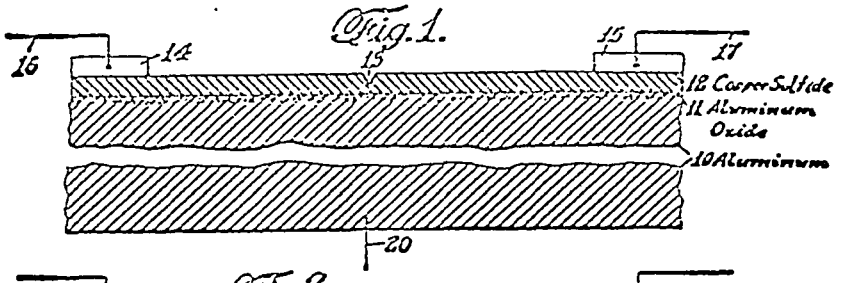
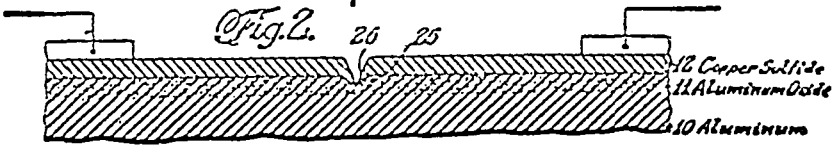


Fig. 2.



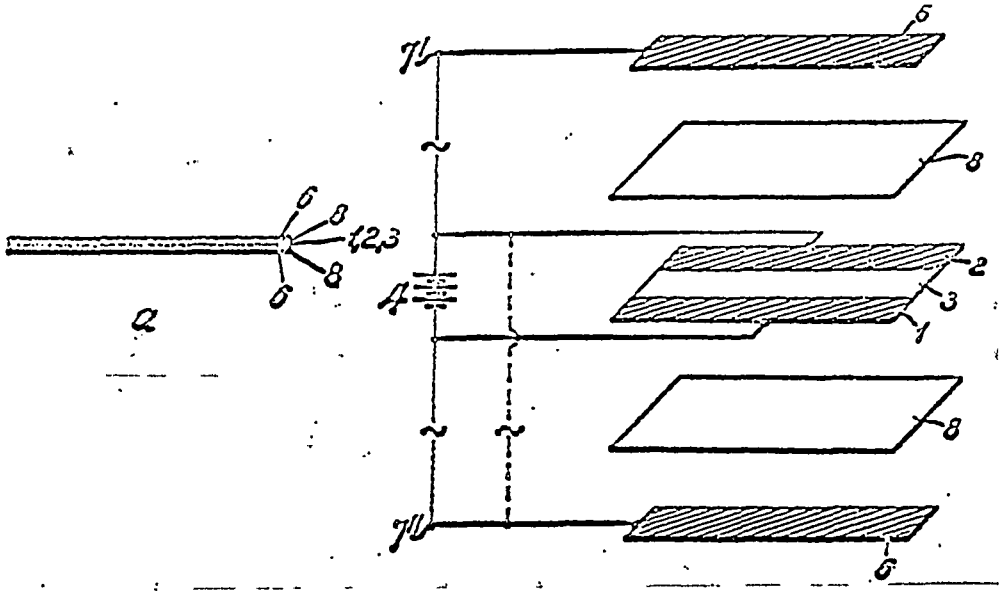


FIGURE 1.1 Early proposals for field-effect transistors.

varying the gate potential it was found that the conductance of the germanium film was modulated to some degree. Although the experiment did demonstrate the field effect phenomenon, perhaps its most striking feature was the effect of charge carrier trapping. It was found that only about 10% of the induced charge in the semiconductor contributed to changing the conductance; the remaining 90% became trapped in surface states which rendered it immobile. As a result of this difficulty in achieving a substantial conductance modulation, and with the discovery of the point contact and junction transistors, interest and work on a field effect modulation device appeared to have waned for some time.

As the idea of integrated circuits became a feasible concept and the advantages of a vacuum deposited active device became apparent, interest was again revived in the early 1960's. A variety of devices have been suggested. Some of these are:

(A) the tunnel-emission triode

(B) the semi-conductor-metal semiconductor triode

(C) the analog or "space charge limited" triode

(D) the bipolar junction transistor

These are shown in Figure 1.2. Another approach[9] was the field effect insulated gate thin film transistor also shown in Figure 1.2(E). A background of theoretical[10,11,12] and experimental studies of space chage limited currents in wide

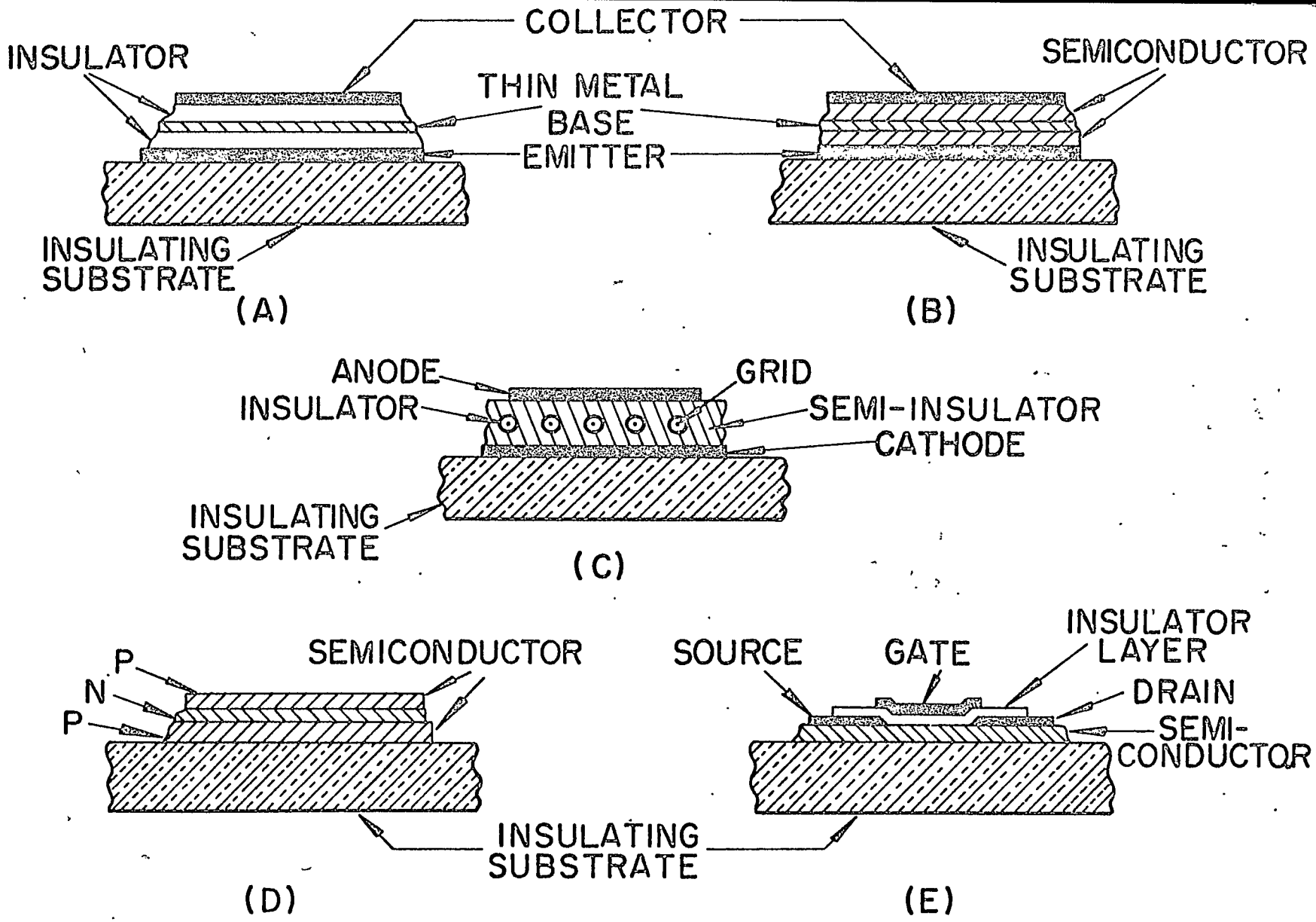


FIGURE 1.2 Proposed thin film active devices

bad gap material had indicated that a useful thin film triode of this type might be feasible. Ruppel and Smith[13] had demonstrated an analog triode using space charge limited currents in a cadmium sulfide crystal. Dresner and Shallcross[14] had studied space charge limited currents in evaporated cadmium sulfide diodes.

An early attempt at constructing a space charge limited triode was made by embedding an evaporated grid structure of tellurium lines in a double layer of cadmium sulfide.[15] Another approach was to use a single pair of laterally spaced electrodes with an intervening tellurium gate strip in contact with cadmium sulfide. Very poor control was obtained in these experiments, owing, in part, to the large trap density and low mobility in the cadmium sulfide films.

1.2.3 The insulated gate thin film transistor

With the introduction of the insulating layer into the gate structure an immediate improvement in the performance was noted. It appeared that as a result of a positive gate bias, the capacitance action between the gate and semiconductor caused electrons to be injected into the semiconductor. The electrons in the semiconductor were drawn to the semiconductor insulator interface filling the traps and establishing a conduction channel there.

Insulated gate thin film transistors have now been made in many laboratories.[15-23] Excellent modulation of semi-

conductor conductance has been obtained with transconductances of up to 10,000 umhos being reported.

However, difficulties exist with the present TFT which severely limit its use for circuit applications. These difficulties arise from the fact that a complete knowledge of the thin film transistor is not available. In particular, a detailed knowledge of the modulation mechanism is lacking. Thus it is often difficult to achieve the desired electrical characteristics. In addition the instability exhibited by the TFT further retards its present usefulness. The present work is largely concerned with these problems.

2. INTRODUCTION TO THE TFT AND THE THIN FILM DIODE

2.1 General

Before considering the detailed presentation and discussion of the TFT's electrical behaviour, a brief description of the physical aspects of the device as well as the basic modulation theory is presented. The formulae for the static electrical characteristics and the small signal parameters are derived. Some experimental results also appear in order to show some of the areas of agreement and disagreement between the actual electrical characteristics and those predicted theoretically.

In this chapter as throughout the thesis, only negative channel devices are considered but it is understood that in general the reasoning applies equally well to positive channel devices, with appropriate changes of polarity.

2.2 The Thin Film Transistor

2.2.1 Basic structure and operation

The common structure of the thin film transistor is similar to that of a parallel plate capacitor and consists of two conducting plates separated by an insulating dielectric. In the TFT, one of these plates is a semiconductor and the

other is a metal. By changing the potential difference between these plates the charge carrier concentration in the semiconductor layer can be altered, thus giving rise to a change in the conductance of the semiconductor layer. This change in conductance results from the fact that the charge carrier concentration for semiconductors is generally relatively small compared, for example, to metals. Thus the number of charge carriers removed or added to the semiconductor layer by the change in voltage can represent a large change in the total charge carrier concentration.

With electrodes making ohmic contacts with either end of the semiconductor, a current flowing through the semiconductor by way of the electrodes can be modulated by the voltage applied to the metal plate.

A schematic drawing of a TFT deposited on a substrate appears in Figure 2.1. The device's three electrical terminals are known as the gate, the source, and the drain. The gate electrode forms the metal plate of the TFT capacitor and is the control electrode. The source and drain are the electrical contacts to the semiconductor; the source electrode being the one which is taken to be at ground potential. Therefore all potentials are applied with respect to it.

A more detailed discussion of the physical aspects of the device may be found in Chapter 5.

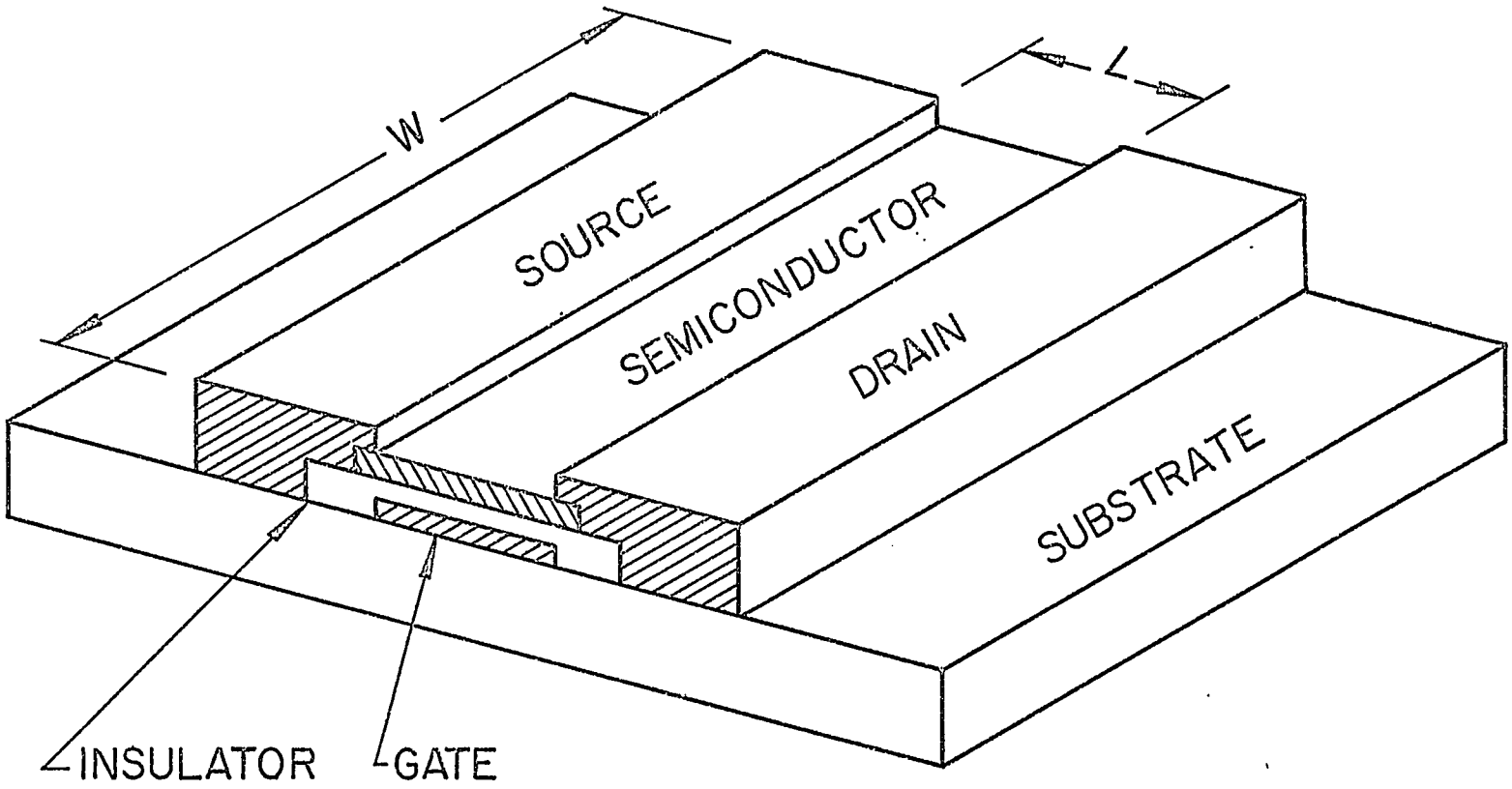


FIGURE 2.1 Schematic drawing of a TFT

2.2.2 Electrical characteristic

A basic analysis of the TFT's has been presented by P.K. Wiemer. He has suggested[24] that the operation of the TFT is similar to that of the conventional field effect transistor,[25,26] insofar as the observed characteristics result from changes in the conductivity of a channel connecting the source and drain electrodes. The analysis assumes a homogeneous layer of semiconductor, thin compared to the insulator, having constant mobility, and forming ohmic contacts with the source and drain electrodes. Only majority carriers are considered to exist in the semiconductor. Equation 2.1 is an expression for the drain characteristics below the onset of current saturation. It is developed in the Appendix according to the above assumptions:

$$I_d = \frac{\mu C_g}{L}\left[(V_g - V_o)V_d - \frac{V_d^2}{2}\right], \quad (V_g - V_o) \geq V_d \qquad 2.1$$

where, $$V_o = -\frac{qN_o t_I}{\varepsilon_o \varepsilon_x} - E_i t_I \qquad 2.2$$

and, I_d = drain current in amperes

μ = drift mobility in cm^2/volt-sec

C_g = capacitance/unit length across the insulator in farad/cm

L = length of the gap between the source and drain electrodes.

V_o = gate voltage required for the onset of drain current

V_g = applied gate voltage relative to the source electrode

V_d = applied drain voltage relative to the source electrode

q = the electronic charge

N_o = the concentration of free electrons in the semiconductor at $V_g=0$, expressed in number/c^3

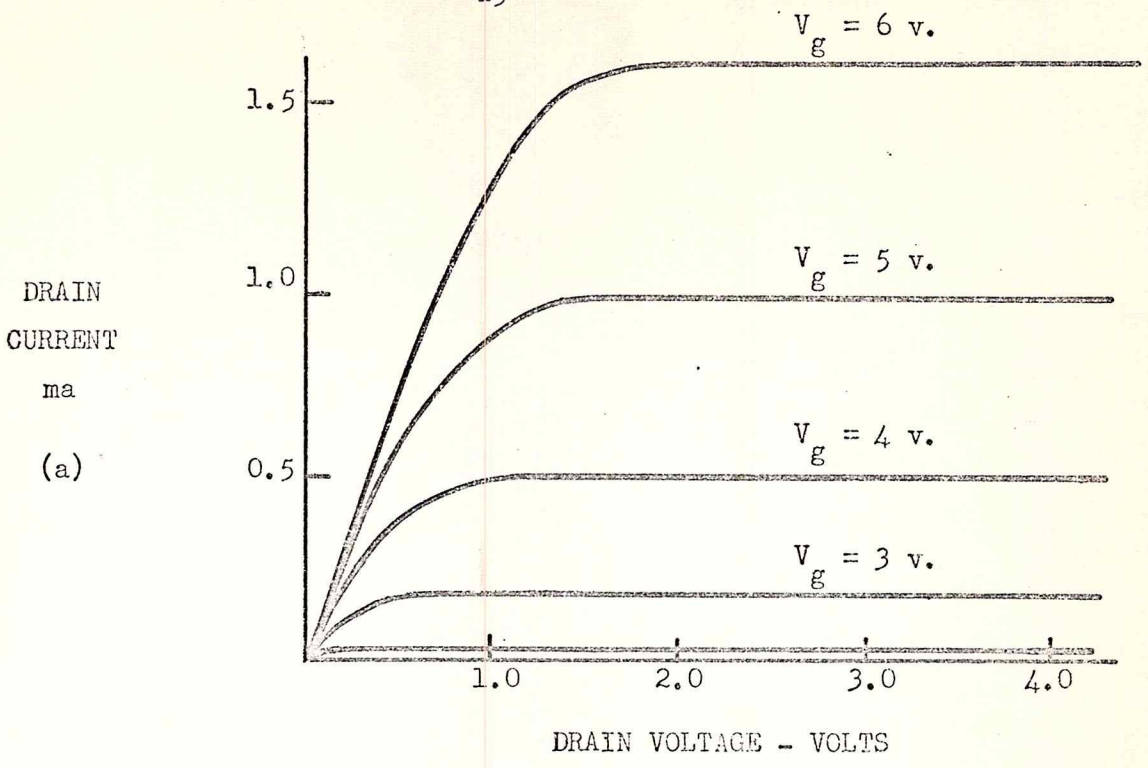
t_I = the thickness of the insulator in cm.

E_i = the component of the electric field at the insulator semiconductor interface which is not due to applied gate voltage, i.e. $E = {}^{V_g}/_{t_I}$

The expression for drain current derived here differs from that developed by Wiemer in that it makes allowances for non-ideal effects which can occur in the insulator layer such as slow dielectric relaxation or ion drifts. In the same way it facilitates consideration of the possibility of trapping of free electrons in semiconductor. In general these effects can be shown to be equivalent to a change in the electrical field at the insulator semiconductor interface, or a corresponding change in gate voltage. In equation 2.2 these effects are accounted for by the term E_i.

It is seen from equation 2.1 that two modes of operation are possible for a TFT. This depends on the value of V_o, the gate voltage required for the onset of drain current. If it is positive, the transistor will not "turn-on" or no significant current will flow from source to drain, until the gate voltage exceeds V_o. This TFT is said to be of the enhancement type. If the turn-on voltage is negative, it is then possible to achieve modulation with negative gate voltages, and the TFT is said to be of the depletion type. An illustration of both types is shown in Figure 2.2.

Equation 2.1 predicts a maximum in the drain current at the point where $(V_g-V_o)=V_d$. The drain current in the actual device saturates at this point, that is it becomes largely independent of the drain voltage. Shockley[30] anticipated this behaviour, and pointed out that no point in the conduction channel of a device, operating in a current saturation mode, does the free carrier density actually become zero. This topic of current saturation is discussed more extensively in Chapter 7. Figure 2.3 shows the predicted behaviour of drain characteristics of an enhancement TFT derived from equation 2.1, along with a set of experimental drain characteristics of a TFT. A reasonably good similarity between the two can be seen here. The theoretical drain characteristics have been separated into two regions by a dashed line. This line represents the locus of the knee of



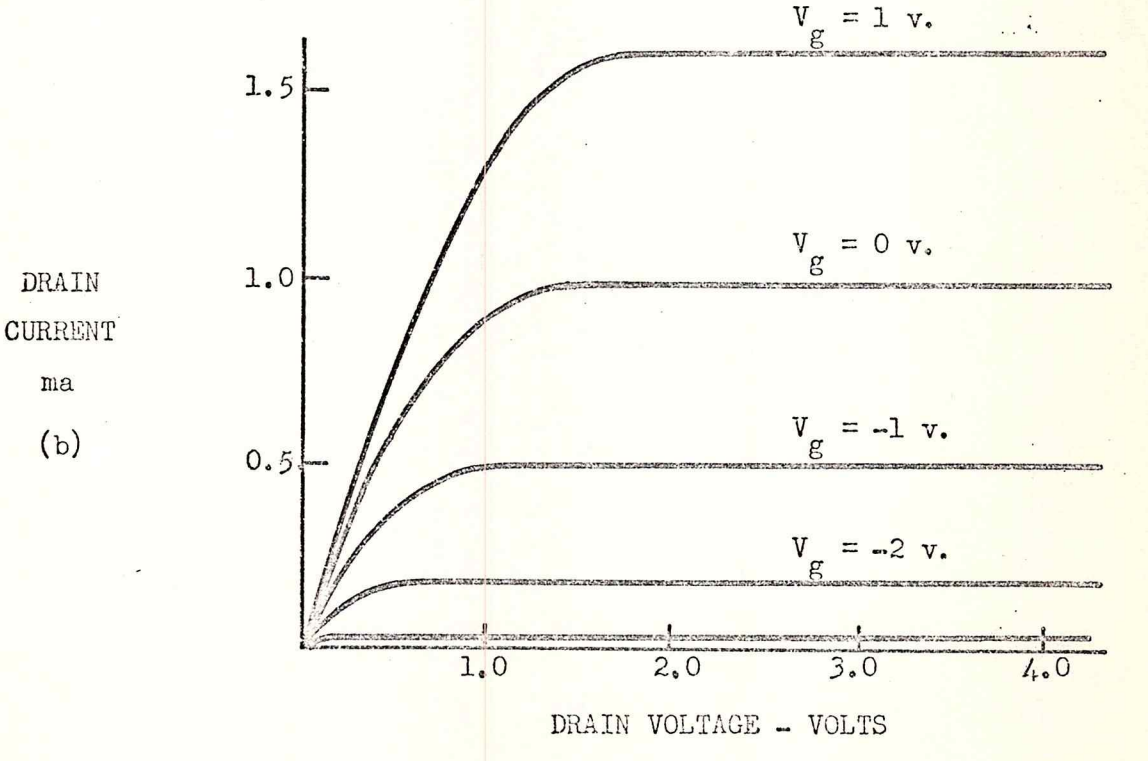
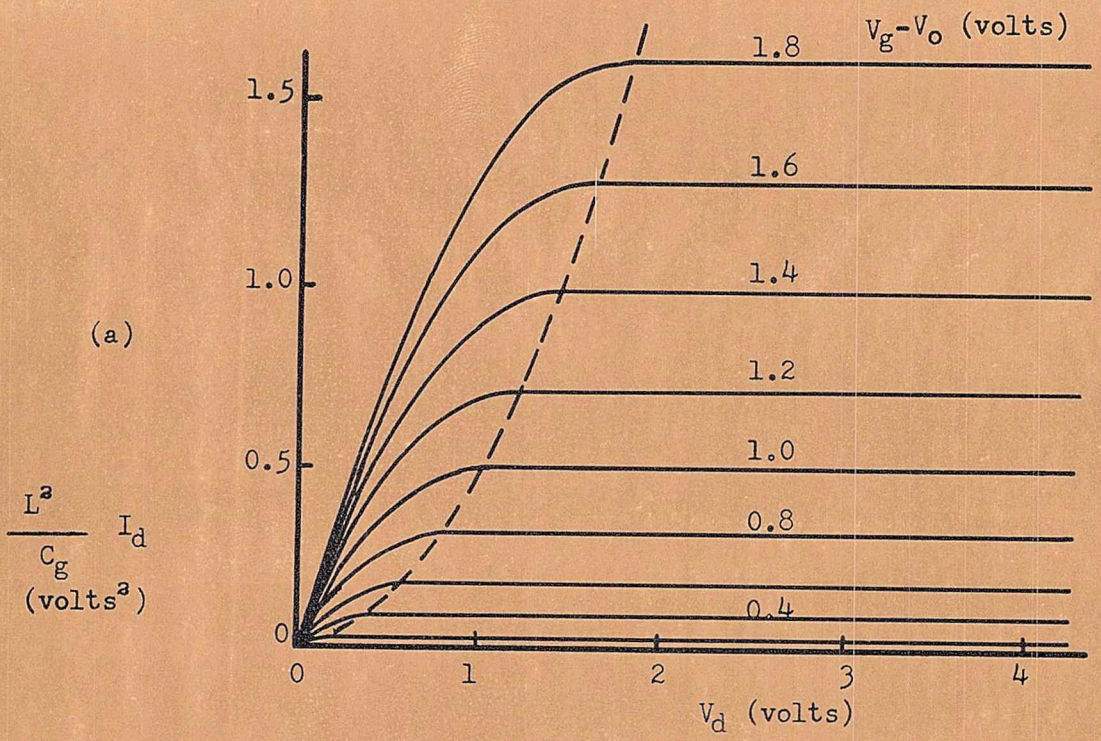


FIGURE 2.2 Illustration of the two types of TFT's

(a) Enhancement type

(b) Depletion type

(a)



(b)

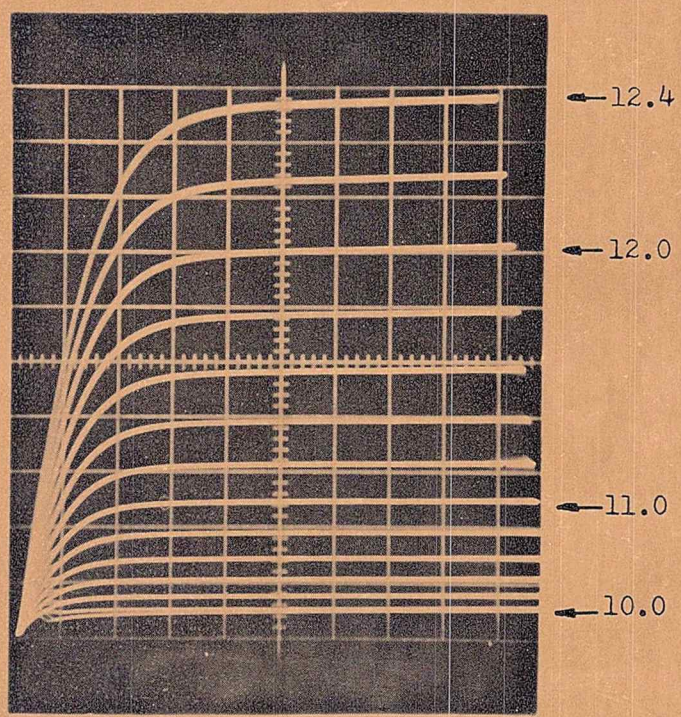


FIGURE 2.3 Drain characteristics of a TFT.

(a) Theoretical

(b) Experimental

the curves; the points where saturation occurs.

With gate voltages for which

$$(V_g - V_o) >> V_d$$

equation 2.1 can be reduced to the following form:

$$I_d = \frac{\mu C_g}{L} V_d (V_g - V_o) \qquad (2.3)$$

This equation describes a family of drain characteristics which are straight lines. The device would in fact be acting as a voltage controlled variable resistor. This effect is illustrated in Figure 2.4. A TFT operating in this fashion could be useful for particular applications.

In the non-saturated mode of operation, the transconductance is found to have a linear relationship with respect to the drain voltage. This is seen by differentiating equation 2.1 with respect to the gate voltage. The small signal transconductance is therefore:

$$gm = \frac{\mu C_g}{L} \cdot V_d \qquad (2.4)$$

An experimental result of this type appears in Figure 2.5. Although there is some scatter in the experimental points it tends to confirm equation 2.4.

In the saturated mode of operation, equation 2.1 reduced to the following form:

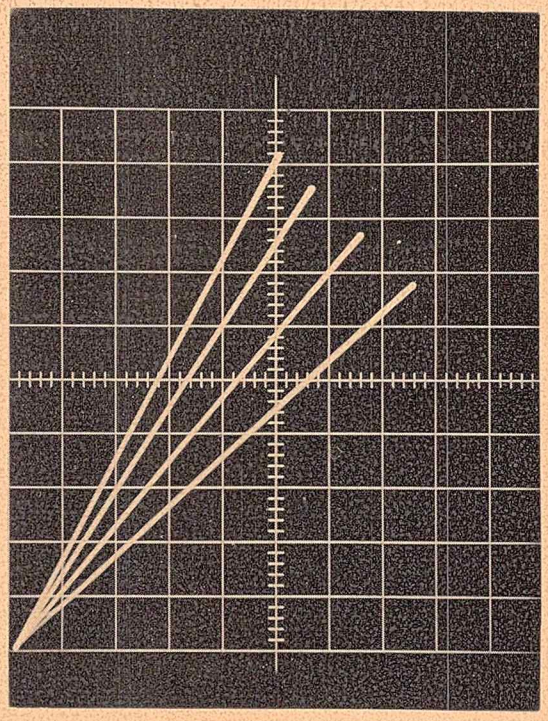


FIGURE 2.4 Linear portion of drain characteristic

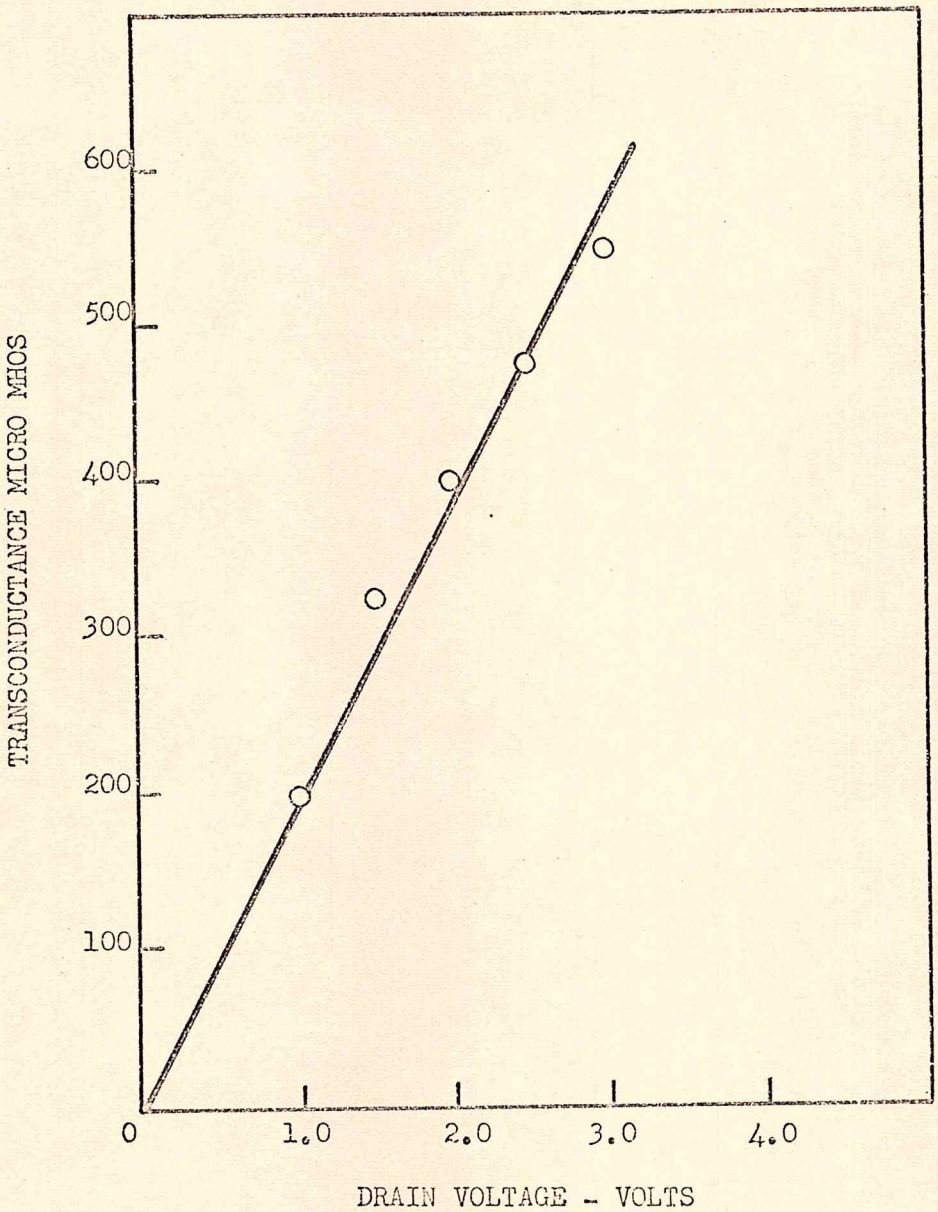


FIGURE 2.5 Experimental result showing a plot of transconductance verses drain voltage in the non-saturated mode of operation.

$$I_d = \frac{C_g}{2L} (V_g - V_o)^2 \quad , (V_g - V_o) \leq V_d \qquad 2.5$$

Hence, in saturation there is a square law relationship of drain current to gate voltage. A consequence of this, is that the transconductance is predicted to be proportional to the square root of the drain current. This result is obtained by differentiating equation 2.5 with respect to V_g and substituting equation 2.5 into the result. In doing this we obtain:

$$gm = \left[\frac{2\mu C_g}{L}\right]^{1/2} \cdot I_d^{1/2} \quad , (V_g - V_o) \leq V_d \qquad 2.6$$

Figure 2.6 shows a plot of the square root of drain current versus gate voltage for a saturated TFT. The result is not quite linear despite the linear relationship predicted by equation 2.5.

Figure 2.7 shows a result which is in accordance with equation 2.6. The square root of the transconductance is found to be proportional to the current for a TFT operating in the saturated mode.

2.3 The Thin Film Diode

Another attractive feature of using TFT's for integrated circuits is the ready availability of a thin film diode (TFD). Such a diode does not require fabrication of a new type of device, but can be had by merely connecting the drain and gate electrodes of a TFT together. In considering the drain

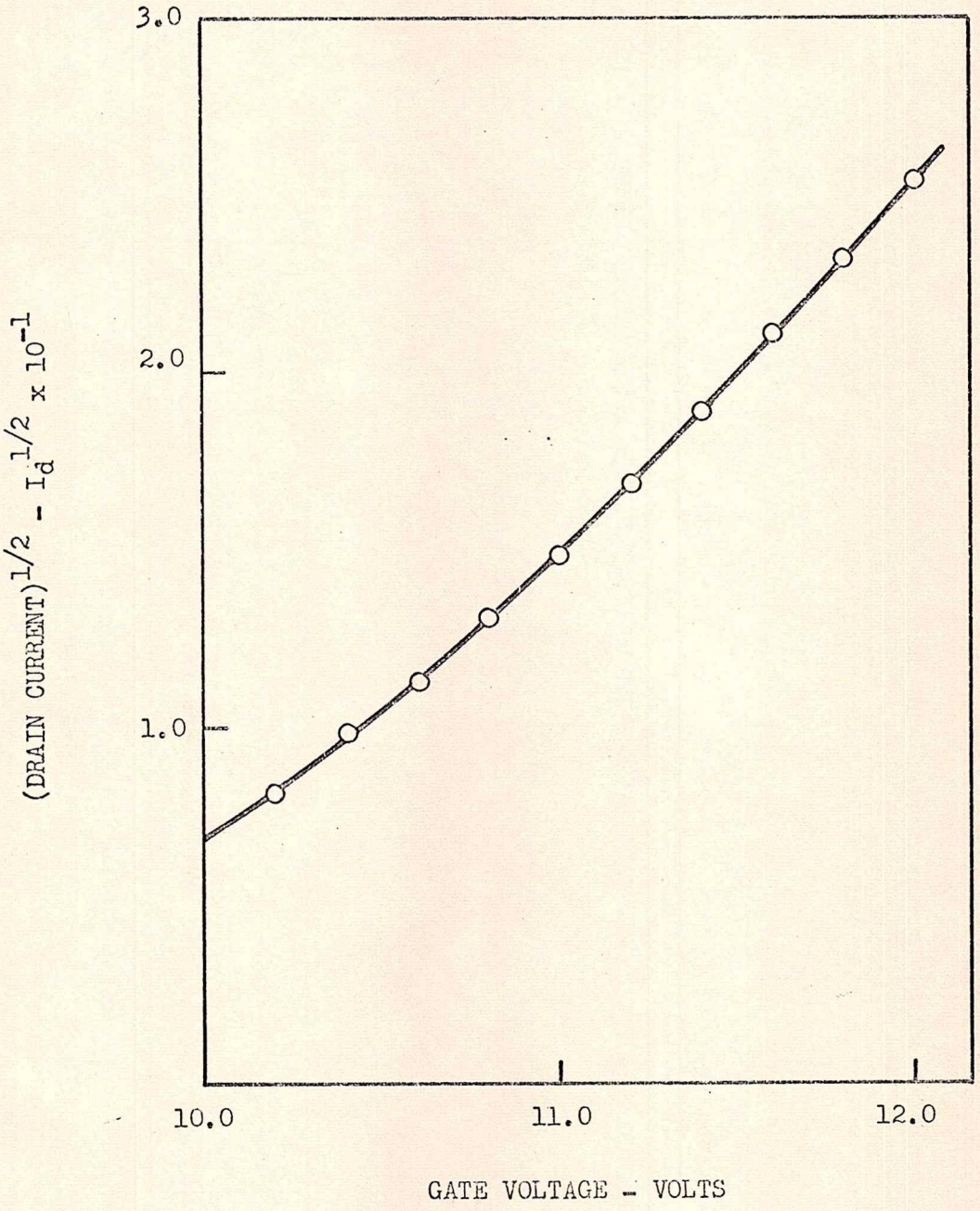


FIGURE 2.6 Experimental result showing the near square law dependance of drain current on gate voltage for a saturated enhancement TFT

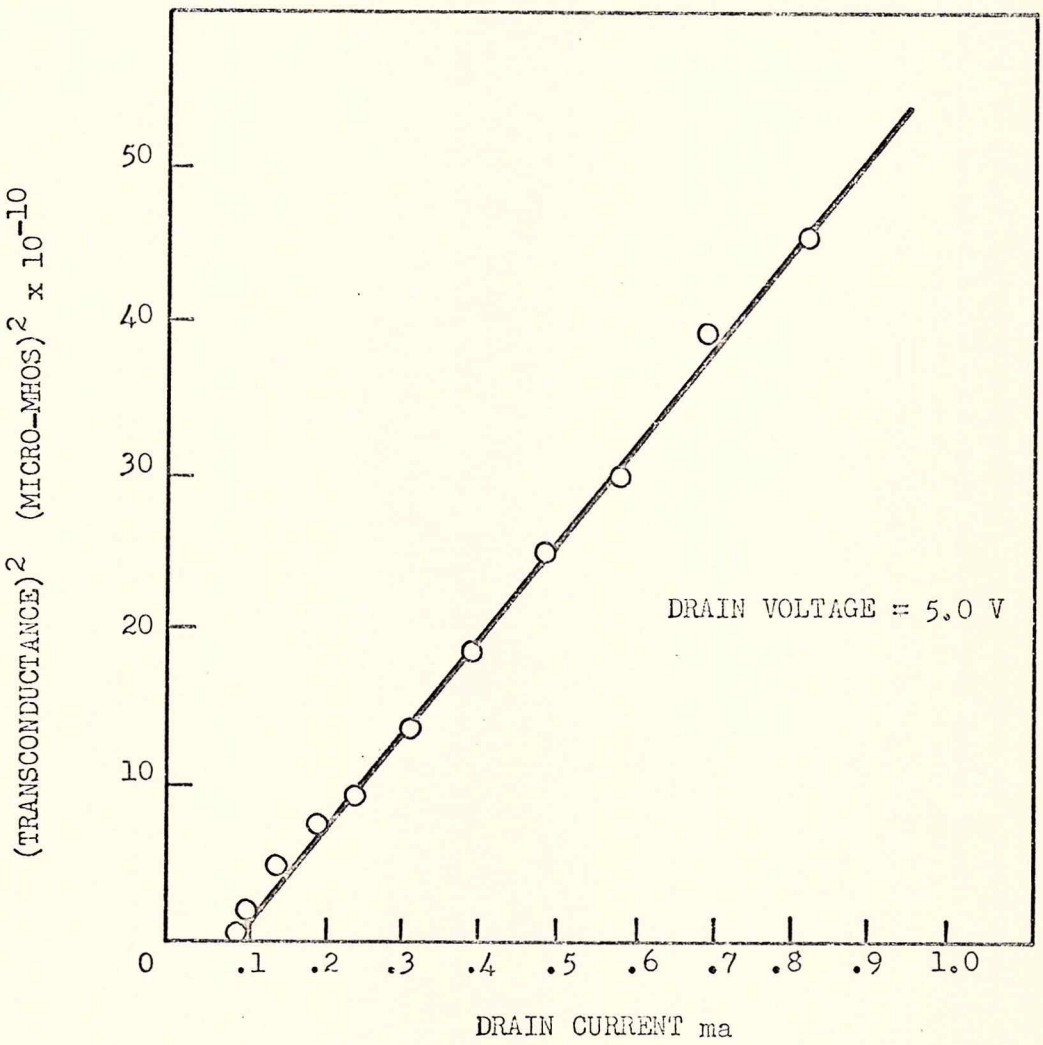


FIGURE 2.7 Experimental results showing a plot of transconductance squared, verses drain current for a saturated TFT

characteristics equation of the TFT, this would mean that the drain voltage would be equal to the gate voltage. The diode equation is then:

$$I_d = \frac{C_g}{2L} \cdot V_d(V_d - 2V_o) \qquad (2.7)$$

A plot of the diode equation for V_o=0.9 volts appears in Figure 2.8. An experimental characteristic of a diode with V_o=0.9 volts, appears in Figure 2.9. A good similarity between the two curves exists.

A comparison between the thin film diode and the junction diode can be made which shows some interesting features of the TFD. In general, once current starts to flow, the current will not increase as rapidly with voltage in the thin film diode, since it appears to obey a "squared" law, as opposed to the exponential voltage law of the junction diode. However, the leakage current of the thin film diode in the reversed bias state can be extremely small, with reverse bias resistances of 10^7 ohms. In addition, the thin film diode can be easily made with a variety of turn-on voltages both positive and negative, by slight alteration of the fabrication process.

Still, since the thin film diode is basically a TFT, it suffers from the same instability problems. This is normally manifested in the diode as a time variation of the turn-on voltage.

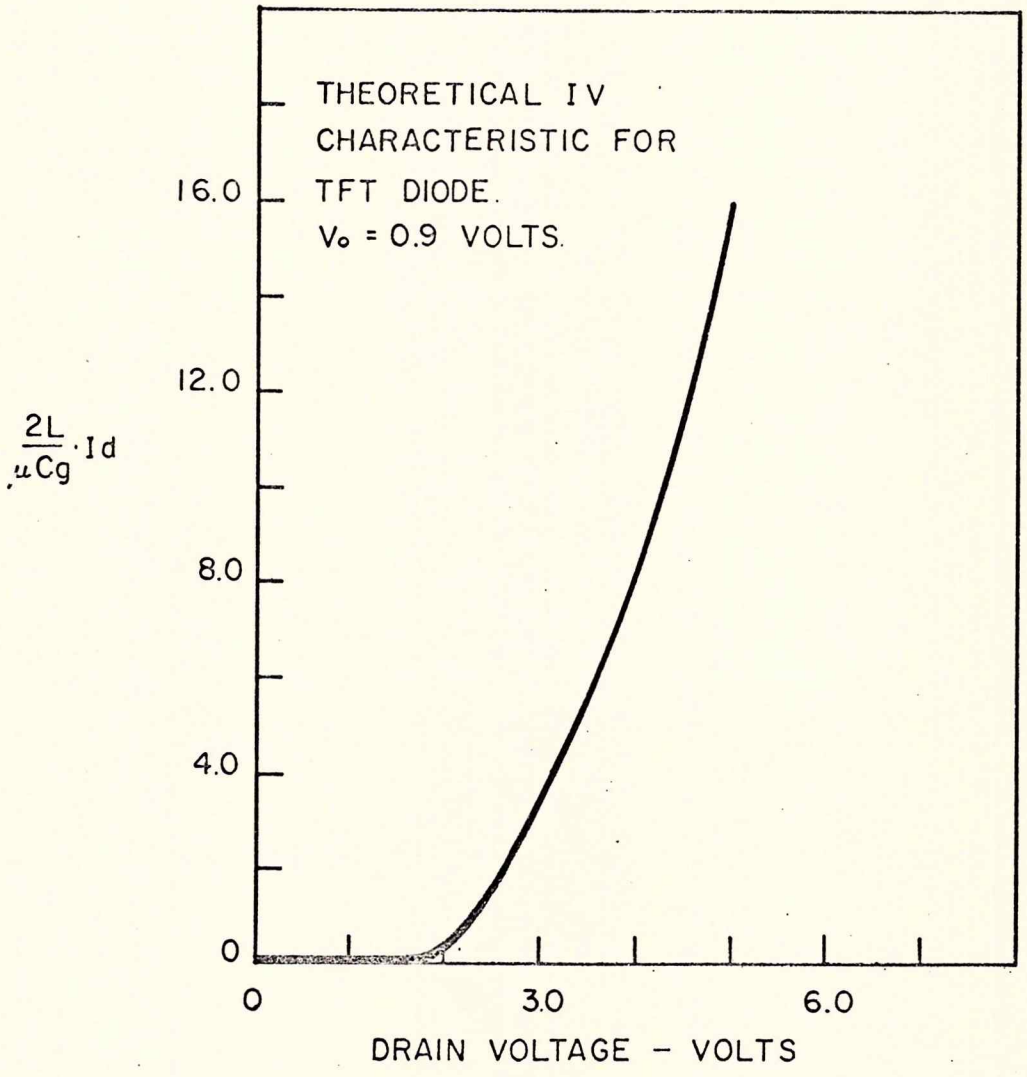


FIGURE 2.8 Theoretical thin film diode characteristic for which V_o = 0.9 volts.