AN ALGORITHM FOR PROTECTING POWER TRANSFORMERS

A Thesis

Submitted to the College of Graduate Studies and Research

in Partial Fulfillment of the Requirements

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in the

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by

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AN ALGORITHM FOR PROTECTING POWER TRANSFORMERS

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ABSTRACT

Electric power utilities have traditionally used electromechanical and solid-state relays for protecting power transformers. Differential protection is the conventionally used scheme for the purpose. With the advent of digital technology, researchers and designers have made remarkable progress in the development of microprocessor-based relays. These relays use algorithms similar in principle to their electromechanical counterparts. Several algorithms, based on differential principle and suitable for implementation on microprocessors, have been proposed in the past. However, these algorithms are adversely affected by current transformer saturation and ratio-mismatch conditions .

This thesis describes a technique that provides a new approach for protecting power transformers. The technique uses positive- and negative-sequence models of the power system in a fault-detection algorithm. While phase voltages and currents at the transformer terminals are used to detect fault, no information concerning parameters of the transformer and power system is required.

The performance of the proposed technique was studied for a variety of operating conditions using data generated by simulations on the electromagnetic transient program, EMTDC. Performance of the developed technique was also evaluated for saturation and ratio-mismatch conditions of the current transformers. A theoretical basis explaining the stable performance during such conditions is also established.

The proposed algorithm can be adapted to protect the transformer which is connected to a source but is not supplying any load. Occasionally, switch-on faults may occur when a transformer is energized. A criterion to detect such faults is proposed and test results verifying the same are also included in the thesis.

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Dedicated To Grandparents

Smt. Harnam Kaur

S. Gajjan Singh Gill

Smt. Surjit Kaur

S. Kartar Singh Cheema

TABLE OF CONTENTS

List of Tables

List of Figures

List of Symbols

B	Magnetic flux density
B_r	Remanent flux density
H	Magnetic flux intensity
CT	Current transformer
Z_{t1}	Positive-sequence impedance of the power transformer
Z_{t2}	Negative-sequence impedance of the power transformer
Z_{gx1}	Positive-sequence impedance of the generator G_x
Z_{gx2}	Negative-sequence impedance of the generator G_x
Z_{gy1}	Positive-sequence impedance of the generator G_y
Z_{gy2}	Negative-sequence impedance of the generator G_y
Z_{L1}	Positive-sequence impedance of the transmission line
Z_{L2}	Negative-sequence impedance of the transmission line
m	constant which defines the fault location in the transformer, $0<m<1$
K_a	Voltage-ratio of secondary to primary voltage of phase A in the power transformer
K_b	Voltage-ratio of secondary to primary voltage of phase B in the power transformer
K_c	Voltage-ratio of secondary to primary voltage of phase C in the power transformer
R, X	Resistive and reactive components of the impedance respectively
a	Phasor operator

1. INTRODUCTION

1.1. Background

An electric power system consists of four major divisions: generation, transmission, distribution, and utilization. An electric utility generates, transmits and distributes energy to a variety of consumers.

Since power systems are spread over vast territories and comprise of large number of components, the probabilities of component failure, abnormalities and faults are significant. Occurrence of faults can cause damage to the equipment and injury to personnel resulting in substantial monetary losses to utilities and consumers.

Each system element should, therefore, be protected from damage due to faults and adverse operating conditions. Protective relays, which activate trip circuits of circuit breakers for isolating the faulted components from the rest of the power systems, are used for this purpose.

1.2. Protection of power systems

The major function of protective devices is to detect the occurrence of faults and to isolate the faulted sections from the rest of the power system. A power system is divided into protection zones, as shown in Figure 1.1, to achieve the intended objective. Each zone usually includes one major element and is protected by using a set of protective relays [1]. The protective relays, responsible for protecting a zone, operate and disconnect the zone from the remaining system when a fault occurs. The relays also alert operators and start equipment for recording the waveforms of system currents and voltages.

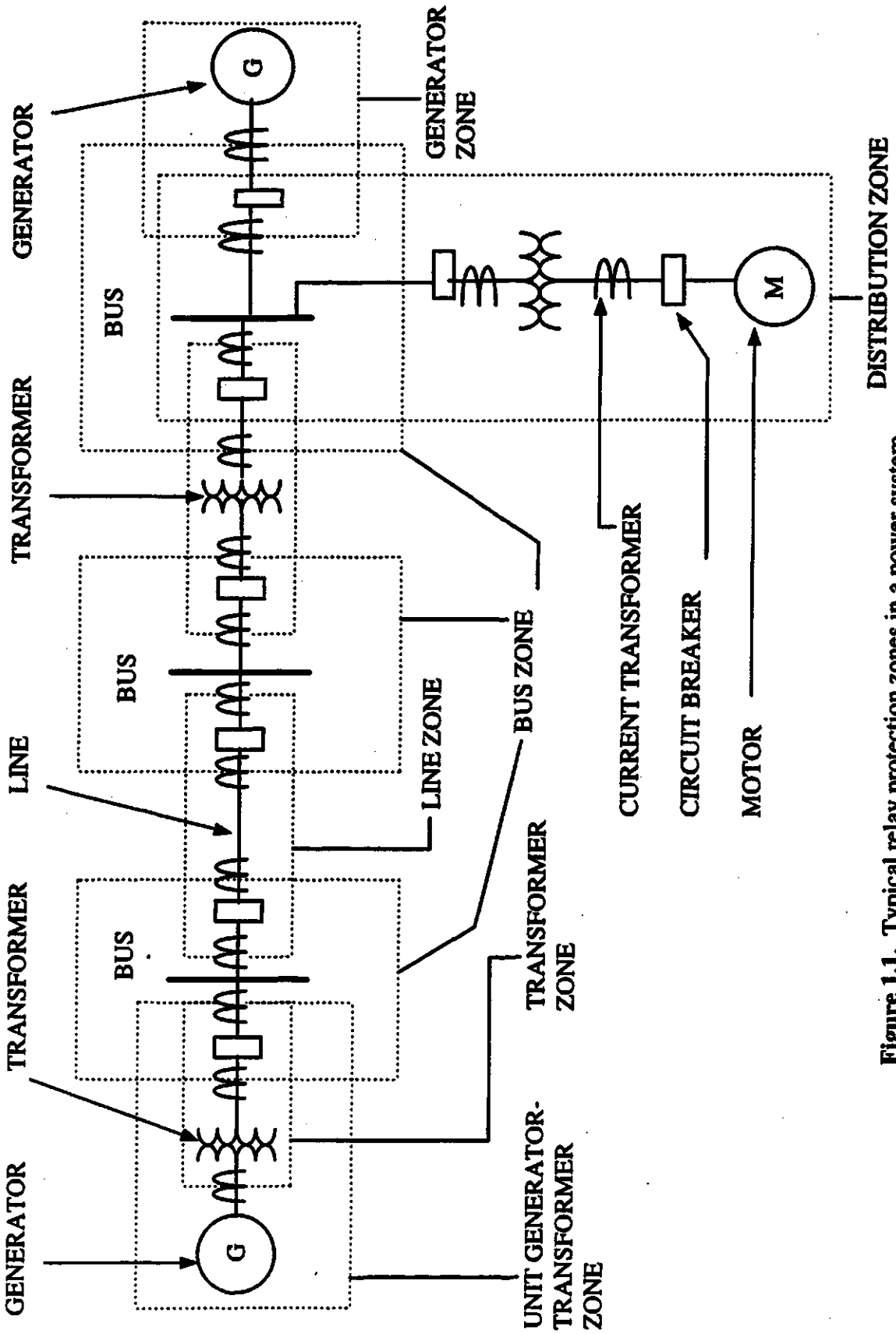


Figure 1.1. Typical relay protection zones in a power system.

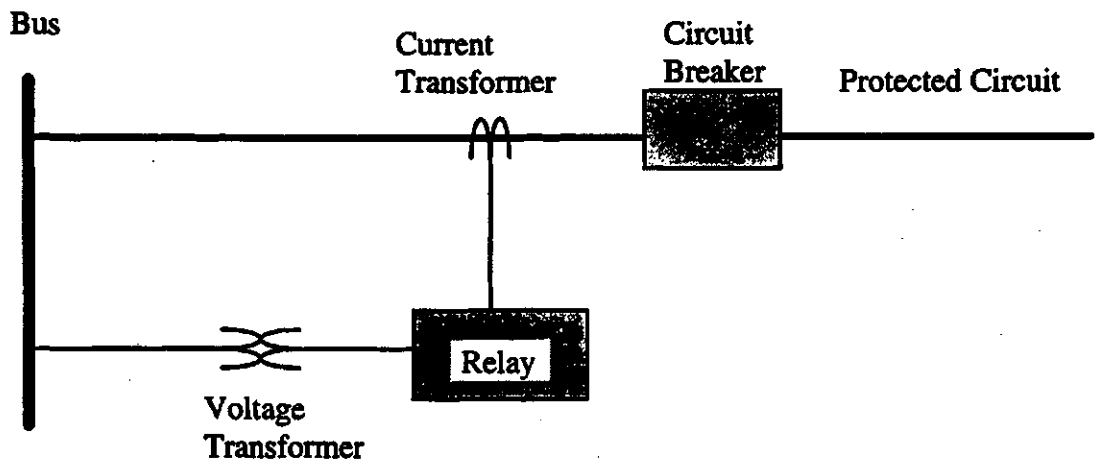
Adjacent zones overlap to ensure that no part of the power system is left unprotected. Back-up relays are also provided to ensure isolation of the faulted equipment in case the primary relays fail to operate. The back-up relays usually operate after a time-delay and isolate not only the faulted zone but also the adjoining zone(s).

Fuses were used as protective devices in the early developments of power systems. They were, and are still, in use for protection purposes. Fuses are effective and inexpensive but have inherent disadvantages, such as their inability to discriminate between supply and load side faults and to restore the circuit after the fault is cleared. Moreover, they need replacement after each operation.

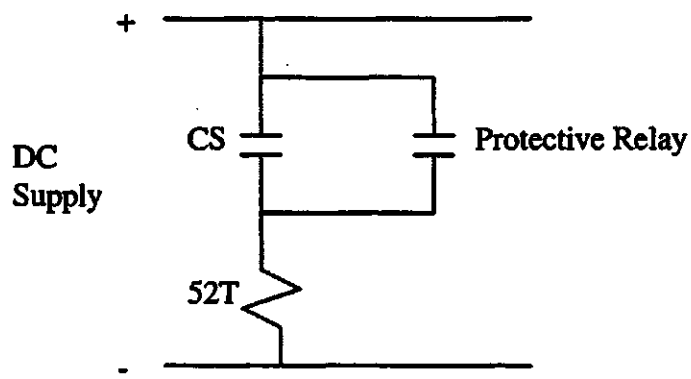
Development of electromechanical relays provided a significant improvement in the protection of power systems. The relays provided means for controlling the operating times and ability to reclose the circuits. This improved the sensitivity and selectivity of the protection schemes.

Solid state relays were introduced in early 1950s. These relays were not initially accepted by the users because of the their inadequate designs and high failure rates of electronic components. Later developments utilized newer semiconductor technology and introduced improved designs. Several kinds of solid state and electromechanical relays are being used in power systems today [2]. Recent advances in the very large scale integrated circuits have led to the development of microprocessors and data acquisition chips. These have resulted in the development of digital relays.

Relays energize trip circuits which result in the opening of circuit breakers. The single-line diagram of a typical relay set up is shown in Figure 1.2(a). The functional block diagram of the dc trip circuit, used for opening the circuit breaker, is shown in Figure 1.2(b). The relay senses the system voltages and currents through voltage and current transformers respectively. The protective relay senses the occurrence of a fault and activates the trip relay which, in turn, closes the breaker contact (CS). This energizes



(a)



(b)

Legend CS -- Contactor switch

52T-- breaker trip coil

Figure 1.2. (a) Single-line diagram of a protective relay arrangement (b) DC trip circuit.

the breaker coil (52T) and opens the circuit breaker to disconnect the faulted section from the rest of the power system.

1.3. A digital relay

A digital relay is a microprocessor-based device that uses software to process quantized signals for implementing the relay logic. Most of the research in the area of digital protection relates to the development of algorithms for specific applications.

The block diagram of a typical digital relay is shown in Figure 1.3. The relay can be divided into analog input, digital input and digital output subsystems, and a microcomputer.

The input to a digital relay consists of analog and digital signals derived from the power system. The analog signals, system voltages and currents, stepped down to appropriate levels are applied to the analog input subsystem. The outputs from the subsystem are fed to the analog interface of the microcomputer.

The digital input subsystem receives the status of circuit breakers and isolators. Isolation circuitry and transient protection is used in analog and digital input subsystems for preventing the relay from system transients. The outputs are provided through digital output subsystem.

The microcomputer, in a digital relay, consists of a central processing unit, non-volatile memory (ROM), random access memory (RAM), analog interface, and communications hardware and appropriate software. The voltages and currents are sampled and quantized, and are fed into the microcomputer. In most digital relaying applications, the data samples complete with time stamps are stored in a RAM. These are transferred to permanent memory storage (local or remote) as soon as possible. A nonvolatile memory, ROM, is used for storing relay programs and settings. The relay logic is executed in the central processing unit.

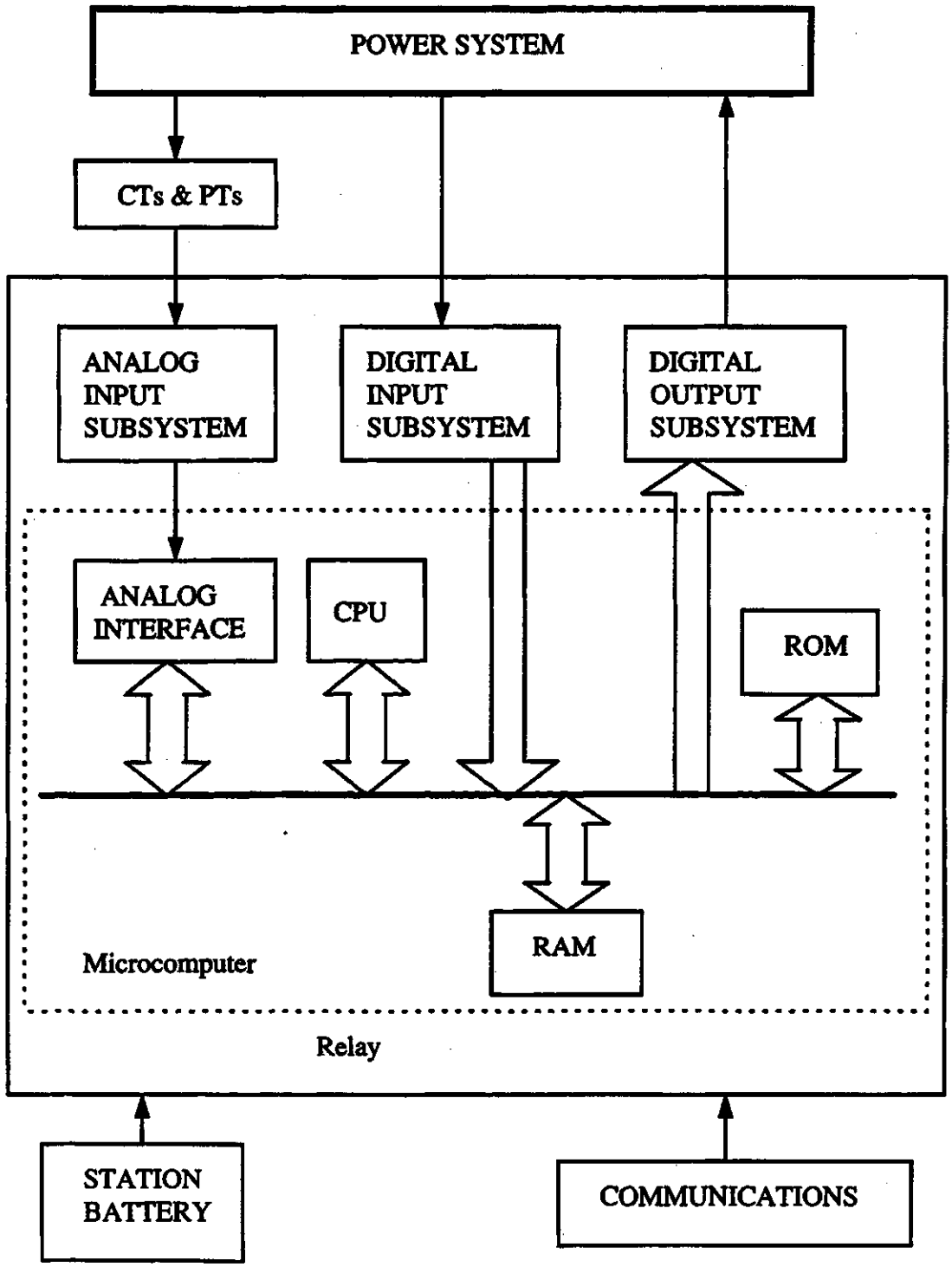


Figure 1.3. Functional block diagram of a digital relay.

Communication links are provided to share information with other devices. A self-diagnosis software resides in the relay and checks the relay state repeatedly. This feature allows the relay to remove itself from service when a malfunction (component failure) occurs and to alert the control center. Digital relays are usually powered from the station battery which is provided with a battery charger. This ensures relay operation during outages of the station ac supply.

A digital relay can perform as well as or better than its electromechanical and solid-state counterparts. A digital relay is continuously active and self-diagnosis routines are repeatedly carried out to detect failures to allow timely corrective actions. This makes digital relays more reliable than their electromechanical and solid-state counterparts. Additional diagnostic features to monitor peripherals are also implemented to further improve the reliability. Functions of a digital relay can be changed simply by changing the relay software, therefore, allowing the use of a common hardware platform. Also, the relay settings can be changed using communication interface. Moreover, flow of input data in the relay hardware can be changed through different routes under program control when trouble arises in normal input paths. This makes a digital relay more flexible and reliable in operation.

A digital relay can store fault data which can be used for diagnosis purposes and system improvements. Fault locations can be calculated from the stored data making it easier for the maintenance staff to carry out repairs.

1.4. Objective of the research

Transformer differential protection is adversely affected by phenomena, such as magnetizing inrush, current transformer (ct) ratio-mismatch and ct saturation. A literature survey revealed that most of the work on transformer protection using digital relays had concentrated on the development of algorithms to discriminate between magnetizing inrush, external faults and internal faults. No concerted effort seems to have been made to address the problem of ct ratio-mismatch and ct saturation.

The objective of this research was to develop a microprocessor based technique which can detect faults and determine if they are inside or outside the protection zone of a transformer. Moreover, the performance of the technique should not be affected by magnetizing inrush, ct saturation and ct ratio-mismatch.

1.5. Outline of the thesis

The thesis is organized in five chapters and five appendices. The first chapter introduces the subject of the thesis and describes its organization. It also presents a brief historical background of protective relays, their role in power systems, and an introduction to digital relays.

Chapter 2 gives an overview of the conventionally used differential protection scheme and outlines its limitations. An introduction to the percentage-bias and harmonic restraint principles is provided. A brief review of the previously proposed digital algorithms for power transformer protection is included and their pertinent characteristics are discussed.

The proposed fault-detection technique is developed in Chapter 3. An algorithm based on the technique is presented and the procedural steps involved in the algorithm are illustrated using a flow chart. The chapter also includes the study of the effects of ct ratio-mismatch and ct saturation on the proposed technique. A theoretical basis, describing the impact of ct saturation on the proposed technique, is developed. The chapter also proposes criteria for detecting faults when a transformer is switched on and when a transformer secondary is not connected to a load or system.

Chapter 4 describes system modeling and data processing steps that are used for evaluating the performance of the proposed technique. The electromagnetic transient simulation package, EMTDC, was used to generate simulation data. Results obtained using the simulated data for different type of faults are presented and discussed. The

impacts of ct ratio-mismatch and ct saturation are also studied and selected cases are presented.

Appendix A outlines the concept of symmetrical components, used for analyzing an unbalanced three-phase system by transforming it into a set of balanced networks. These networks, called sequence-networks, are briefly defined in this appendix. An introduction to the EMTDC and current transformer model used in the simulations is given in Appendix B. Appendix C lists the parameters of the power transformer and other components of the power system model used for generating simulation data. The design and frequency response of the anti-aliasing filters, used for off-line processing of the data, are presented in Appendix D. Appendix E includes additional test results which demonstrates the usefulness of the proposed technique.

The specific contributions made by this thesis are as follows.

1. An improved technique for protecting transformers has been developed. The technique is described in Chapter 3.

2. A digital algorithm based on the proposed technique is also reported in Chapter 3.

3. A theoretical analysis showing the effect of ct saturation on the proposed technique has been carried out. This is presented in Chapter 3 and verified by the test results given in Chapter 4. The effect of ct ratio-mismatch on the proposed technique is studied. The stable performance provided by the technique under such condition is shown by test results given in Chapter 4.

4. A criteria to detect faults occurring during switch-on and unloaded operation of the transformer are also developed. They are described in Chapter 3 and the performance results are included in Chapter 4.

1.6. Summary

This chapter has presented a brief introduction to the concepts of power system protection. The development of protective devices from fuses to the present day digital relays has been described. Block diagram of a typical digital relay and advantages of digital relays have also been outlined.

Most of the previously proposed algorithms for protecting transformers are based on the principle of differential protection. Some of these algorithms are reviewed in Chapter 2.

2. DIFFERENTIAL PROTECTION

Differential protection is conventionally used for protecting most power transformers and generators. During the last five years, differential protection of transmission lines has also become a viable technique. As the protection of each component of the power system is considered, differential protection is invariably a prime candidate, and is often selected to provide primary protection [1].

The differential protection technique applied to power transformers is discussed in this chapter. Its fundamental principle and limitations are examined. Special features, incorporated in differential relays, to prevent misoperations are briefly discussed. Digital algorithms, proposed in the past, for protection of power transformers are reviewed. This is followed by a discussion of the previously proposed algorithms.

2.1. The differential principle

The differential principle, as applied for protecting power transformers, can be described with the help of Figure 2.1. The levels of currents on the primary and secondary sides of the power transformer are reduced by the cts. The outputs of these cts are compared. The ratios of primary and secondary cts are selected such that each ct produces the same secondary current for nominal line currents. The operating coil of the relay is connected to secondary windings of two cts in such a way that the net current flowing through it equals the difference between the secondary currents of cts provided on the two sides of the power transformer. Net current through the operating coil of differential relay is zero for normal operation and external faults. An internal fault in the power transformer upsets this balance and causes a current to flow in the relay's operating coil. This is shown in Figure 2.1(b).

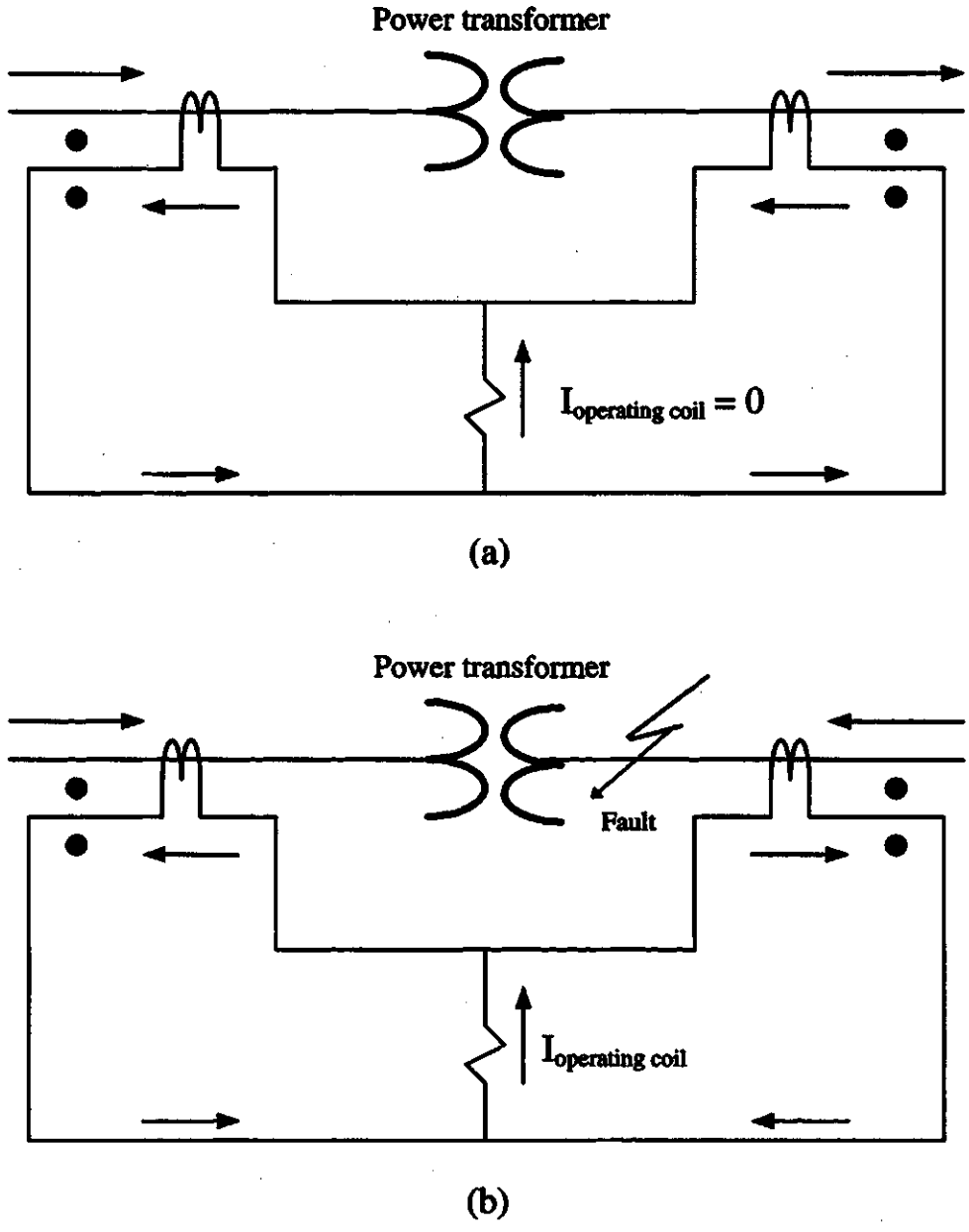


Figure 2.1. Basic differential scheme for (a) no-fault and (b) internal fault conditions of a power transformer.

An internal fault is not the only cause for the presence of differential currents. A small amount of current normally flows in the operating element because of current needed to magnetize the core, mismatch of cts ratios and differences in characteristics of the cts. Large amounts of currents in the operating elements are experienced due to ct saturation and magnetizing inrush. These phenomena are described briefly in the following section.

2.2. Problems with differential protection

As pointed out in the preceding section, the net current through the operating element of a differential relay is never zero. Non-linear phenomena such as magnetizing inrush and ct saturation are experienced which results in operating current in the differential relay even when there is no fault in the protection zone. These phenomena are described in the following sections.

2.2.1. Ratio-mismatch

Most power transformers are equipped with on-load tap changers which operate to change the turns ratio between the primary and secondary sides of the transformer as the system operating conditions change. Since the ct ratios are selected to match the transformer operation at its nominal tap setting, the operation of the tap-changer disturbs the balance between the outputs of the primary and secondary side cts and, consequently, causes currents to flow in the operating element of the differential relay.

To avoid tripping due to ratio mismatch, differential relays are provided with a percentage-bias feature which is described in Section 2.3.

2.2.2. Difference in current transformer characteristics and burdens

The primary and secondary current transformers (ct's) used for differential protection of power transformers are designed for operation at different voltage levels. Their characteristics are, therefore, difficult to match over their entire range of operation. Also, the length of the leads connecting the primary and secondary cts to the relay

cannot be exactly equal. The VA burdens on the cts are, therefore, unequal. This causes cts to produce different outputs for the same levels of input currents. The consequences is that some current flows in the operating element of the differential relay during through faults.

2.2.3. Current transformer saturation

The current transformer (ct) is a basic component in any relaying scheme. The primary winding of a ct is in series with the line and, therefore must carry the current that may happen to flow in the line. When a short-circuit occurs on the line, the line current becomes large which also flows in the ct primary. The secondary current also increases. Ideally, the secondary current should be proportional to the primary current and the ct must develop sufficient voltage to make this current flow in the secondary circuit. To generate this voltage, part of the primary current becomes the magnetizing current that produces flux in the core of the ct. Normally, the magnetizing current is small and the secondary current remains proportional to the primary current for all practical purposes. If the ct has to develop large voltage to overcome the voltage drop in the secondary circuit, the core flux levels must be high. If the flux approaches the saturation level, the exciting current becomes large and the secondary current does not increase proportionally. As the primary current increases beyond the saturation level, the core saturates during a part of the cycle [3]. The magnetizing current is large when the core is saturated. Consequently the secondary current out of ct is less than its level had the ct not saturated. The result is that the secondary current becomes distorted.

Figures 2.2 (a), (b) and (c) show the waveforms of ct primary current and the corresponding secondary currents for mild and severe ct saturation conditions respectively. Inductance in the burden (load connected to the ct) results in a more gradual drop-off, while a lower burden reduces the distortion of the secondary current. Since the cts used in differential protection schemes are in series with the line, they carry large amounts of currents during internal and external faults. A high level of current can cause

one or more ct(s) to saturate resulting in different secondary currents out of the cts which would have been otherwise equal.

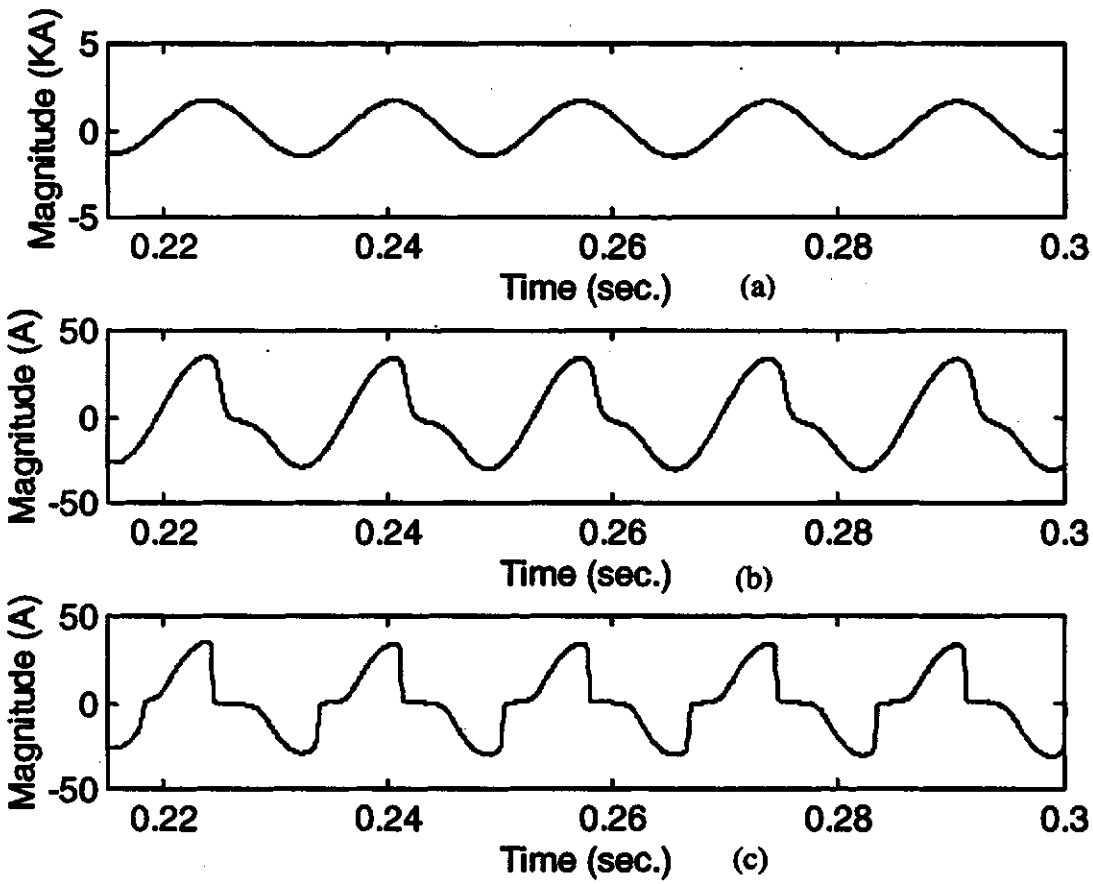


Figure 2.2. Current waveforms of ct's (a) primary current, and secondary currents for (b) mild and (c) severe ct saturation states.

This results in the flow of a differential current in the operating element of the relay even when the fault is outside the protection zone. Saturation of cts can cause the differential relays to operate during external faults and, therefore, steps must be taken to detect ct saturation and prevent the relay operation when it is necessary.

2.2.4. Magnetizing inrush

When a transformer is switched-on at a time when the normal steady-state flux should be different than that existing in the transformer core, magnetizing inrush currents occur [1]. The magnitude of the inrush currents can be several times the rated full-load current of the transformer. The factors controlling the magnitude and duration of the magnetizing inrush currents include the rating of the transformer, size of the power system it is connected to, resistance of the circuit from the source to the transformer, type of iron used to form the core and the level of the residual flux. The phenomenon of magnetizing inrush is random. It depends on the residual flux in the transformer core and the instant at which the voltage is applied to energize the transformer.

Consider the magnetizing curve of a transformer core shown in Figure 2.3. When power to the transformer is switched off at time $t=t_1$, the magnetizing current traces the hystersis loop to zero. The flux at that time is $+B_r$, which is now the remanent flux. If the transformer were not switched off, the magnetizing current (i_1) and the flux density (B_2) would have followed the dashed curves as shown in Figure 2.4 [4]. Assuming that the transformer is re-energized at time instant $t=t_2$, when the normal value of flux density would have been $-B_{max}$. Since the magnetic flux inside the transformer core cannot change instantaneously, the flux density starts at B_r and traces the curve B_3 instead of starting at the normal value of $-B_{max}$. This curve is a sinusoid riding a dc offset. The transformer core saturates. To provide the high value of flux density (B_3), a large magnetizing current is required which is drawn from the source. The current corresponding to the flux density B_3, is shown as i_3 in Figure 2.4. This current is substantially greater than the normal magnetizing current i_1, also shown in Figure 2.4.

Maximum inrush does not occur every time the transformer is energized because

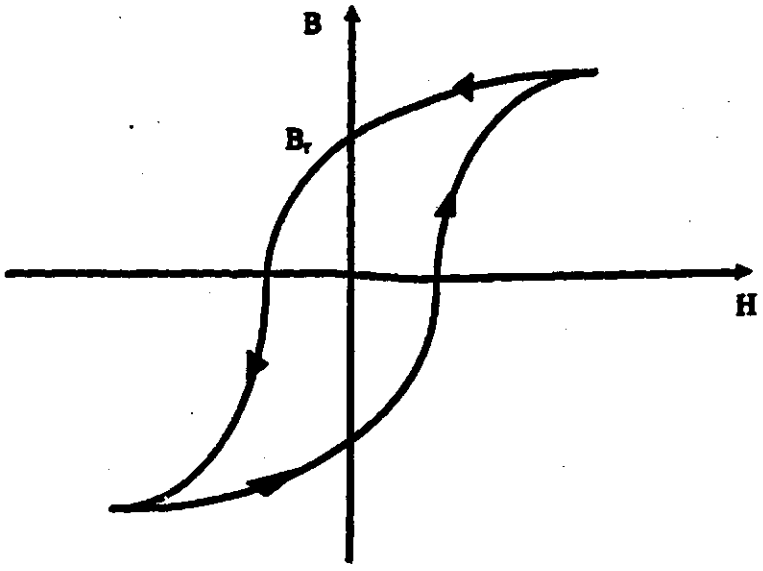


Figure 2.3. Magnetizing curve for a transformer core.

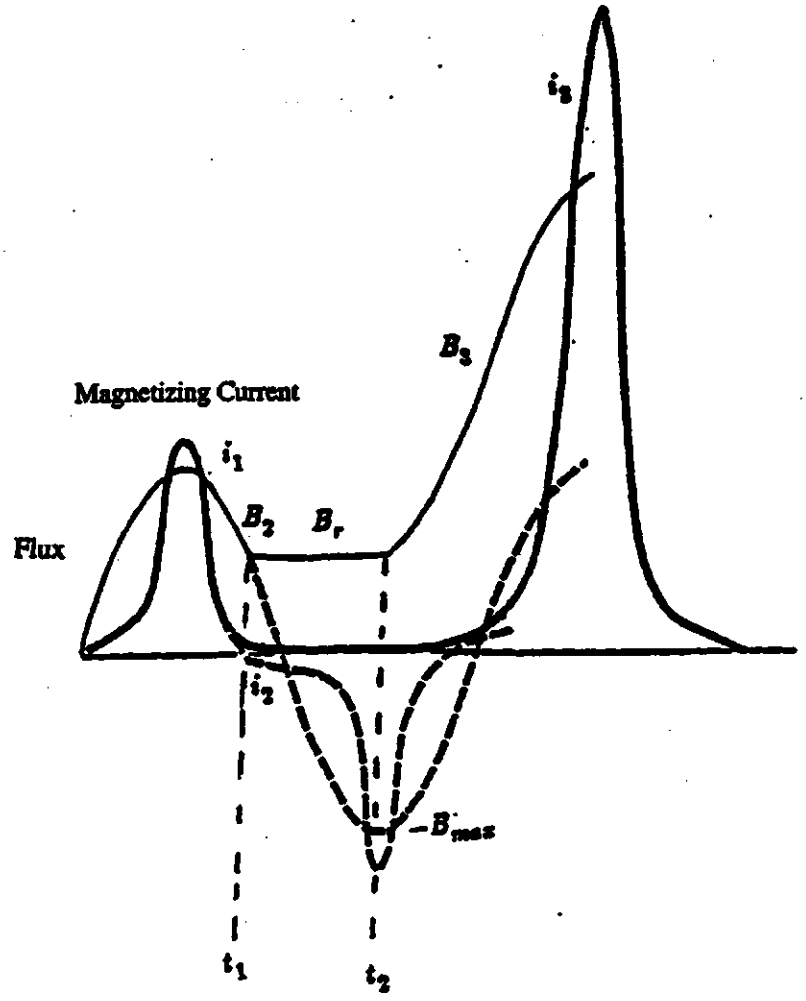


Figure 2.4. Magnetizing inrush phenomenon in a power transformer.

the probability is low for energizing at zero crossing point of the voltage waveform. Energizing at maximum voltage does not produce an inrush if there is no residual flux. If a transformer is energized at an instant of the voltage waveform which corresponds to the residual flux density in the core, the process of switching-in becomes a smooth continuation of the previous operation and does not cause any magnetizing inrush. In a three-phase transformer, the inrush will vary appreciably in the three phases and its magnitude will be different in different phases.

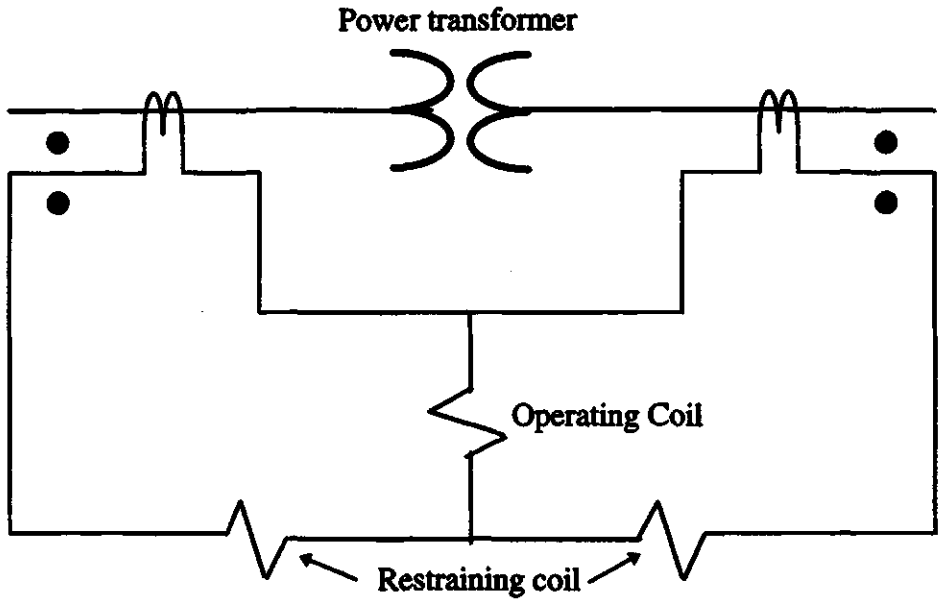
The waveform of the magnetizing inrush current is not sinusoidal. It is distorted due to core saturation and interphase coupling. Since the inrush currents flow in the primary windings of a transformer, they are interpreted as internal faults by differential relays.

To prevent differential relay from operating during magnetizing inrush, harmonic restraint is incorporated in the relays.

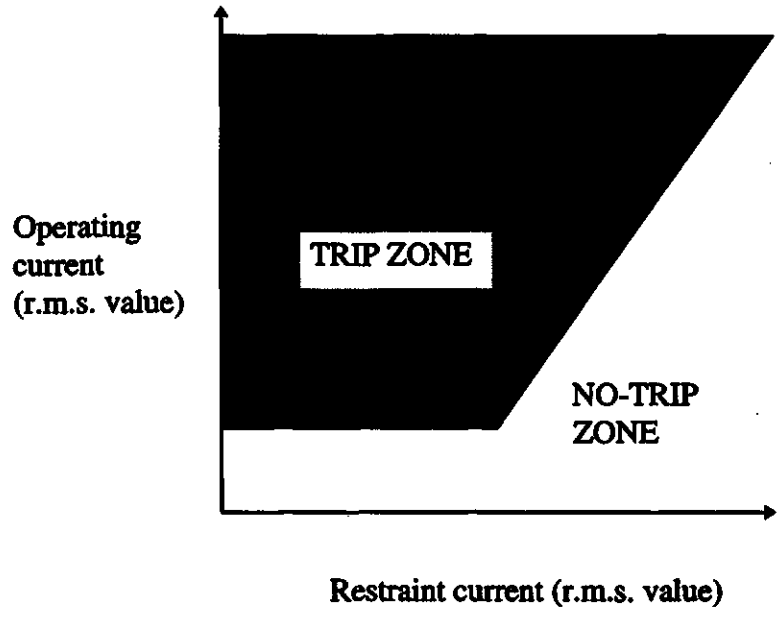
2.3. Percentage-bias and harmonic-restraint

The phenomena that affect the operation of a differential relay are reviewed in the previous section. The percentage-bias and harmonic restraint features are used to prevent differential relays from operating during magnetizing inrush and external faults.

A percentage-bias differential relay has two restraining windings as shown in Figure 2.5(a). Currents in the operating windings of a differential relay are equal to the differences between the currents in primary and secondary side cts. The restraint is proportional to the sum of ct currents. The differential current required to operate the relay must exceed a set percentage of the total restraint. The ratio of the operating current and restraining current expressed as a percentage is usually called the slope of the relay characteristic. A typical percentage-bias characteristic is shown in Figure 2.5(b). The slope is adjustable and can be made large enough to prevent the relay from operating due



(a)



(b)

Figure 2.5. Percentage-bias differential relay (a) circuit and (b) characteristics.

to inaccuracies of the cts and off-nominal taps of transformers. The differential current due to ct ratio mismatch is countered by the restraining current and the relay is restrained from operating improperly [5]. This feature increases the security of the relay while it keeps its sensitivity at a reasonable level.

Analysis of typical inrush currents indicate that the second harmonic current is predominant in these currents [6]. This component is extracted from the differential currents using frequency selective circuits and is used to restrain the operation of transformer differential relays. The basic purpose of using the harmonic restraint feature is to restrain the relay for all levels of magnetizing inrush but permit operation for internal faults.

2.4. Digital algorithms for transformer protection

The digital algorithms proposed for transformer protection can be broadly divided into the following categories:

1. Waveshape identification technique
2. Harmonic restraint algorithms
3. Model-based algorithms

These algorithms are briefly described in this section.

2.4.1. Waveshape identification technique

Substantial differential currents flow in the operating coil of a differential relay on the occurrence of an internal fault. However, as described before, magnetizing inrush, ct ratio mismatch and differences in ct characteristics also result in differential currents which do not represent actual faults in the protected zone. Rockefeller [7] suggested that the magnetizing inrush currents can be identified by monitoring the time duration between successive peaks of the currents. The two successive peaks of a magnetizing inrush current are either 4 or 16 ms apart whereas the successive peaks of a

fundamental frequency fault current occur at an interval of 7.5 to 10 ms. Also, the peak value of a fault current is within 75 to 125 percent of its previous peak and is of the opposite sign. Rockefeller, therefore, suggested the use of current waveshapes for identifying the inrush phenomenon.

2.4.2. Harmonic-restraint algorithms

These algorithms use harmonic components of the differential currents to restrain the relay during magnetizing inrush. As described earlier, unlike fault currents, magnetizing inrush currents contain large proportions of second harmonic frequency components. This fact is used in developing harmonic restraint algorithms. Digital differential relays sample the currents at regular intervals of time and calculate the peak values of their fundamental frequency and harmonic components. If the second harmonic component in a differential current exceeds a pre-specified percentage of its fundamental frequency component, it is concluded that magnetizing inrush is being experienced. The algorithms using the harmonic restraint principle utilize different techniques to estimate the magnitudes of the fundamental and harmonic frequency components of the currents. Some of the filtering techniques are briefly described in the following sections.

2.4.2.1. Least error squares technique

Sachdev and Baribeau [8] described the Least Error Squares (LES) approach for developing a digital filter which explicitly takes account of the decaying d.c. components in the system voltages and currents. This curve-fitting technique is based on minimizing the mean-square error between the actual and assumed waveforms. The technique uses the coefficients of the designed filter to compute the real and imaginary components of the voltage and current phasors.

In designing the LES filter, it is assumed that the power system currents and voltages are composed of an exponentially decaying dc component, a fundamental frequency component and components of a few harmonics.

Consider that the waveform of a voltage can be modeled as

$$v(t) = A_0 e^{-t/\tau} + \sum_{n=1}^{N} A_n \sin(n\omega_0 t + \theta_n). \qquad (2.1)$$

where:

- $v(t)$ is the instantaneous value of the voltage at any time t,
- τ is the time constant of the decaying dc component,
- N is the highest order harmonic component present in the voltage,
- ω_0 is the fundamental frequency of system in radians/seconds,
- A_0 is the initial value of the dc offset at time t=0,
- A_n is the peak value of the n^{th} harmonic component, and
- θ_n is the phase angle of the n^{th} harmonic component.

The Taylor series expansion for the decaying dc component gives

$$e^{(-t/\tau)} = 1 - \left(\frac{t}{\tau}\right) + \left(\frac{1}{2}\right)\left(\frac{t}{\tau}\right)^2 - \left(\frac{1}{6}\right)\left(\frac{t}{\tau}\right)^3 + \ldots$$

Applying the trigonometric identity sin(A+B)=sinAcosB+cosAsinB and using the first two terms of the Taylor series expansion of the decaying dc component, Equation (2.1) becomes

$$v(t) = A_0 - \left(\frac{A_0}{\tau}\right)t + \sum_{n=1}^{N} A_n\left[\sin(n\omega_0 t)\cos\theta_n + \cos(n\omega_0 t)\sin\theta_n\right]. \qquad (2.2)$$

If the fourth and higher order harmonics are assumed to be removed by the anti-aliasing filter, and $t = t_1$, Equation (2.2) becomes

$$v(t_1) = A_0 - \left(\frac{A_0}{\tau}\right)t_1 + (A_1\cos\theta_1)\sin(\omega_0 t_1) + (A_1\sin\theta_1)\cos(\omega_0 t_1) +$$

$$(A_2\cos\theta_2)\sin(2\omega_0 t_1) + (A_2\sin\theta_2)\cos(2\omega_0 t_1) +$$
$$(A_3\cos\theta_3)\sin(3\omega_0 t_1) + (A_3\sin\theta_3)\cos(3\omega_0 t_1). \qquad (2.3)$$

This equation can be expressed as

$$v(t_1) = a_{11}x_1 + a_{12}x_2 + a_{13}x_3 + a_{14}x_4 + a_{15}x_5 + a_{16}x_6 + a_{17}x_7 + a_{18}x_8. \qquad (2.4)$$

where:

$x_1 = A_0$, $x_2 = -\left(\frac{A_0}{\tau}\right)$, $x_3 = A_1\cos\theta_1$, $x_4 = A_1\sin\theta_1$, $x_5 = A_2\cos\theta_2$, $x_6 = A_2\sin\theta_2$,

$x_7 = A_3\cos\theta_3$, $x_8 = A_3\sin\theta_3$, and

$a_{11}=1$, $a_{12}=t_1$, $a_{13}=\sin(\omega_0 t_1)$, $a_{14}=\cos(\omega_0 t_1)$, $a_{15}=\sin(2\omega_0 t_1)$, $a_{16}=\cos(2\omega_0 t_1)$,

$a_{17}=\sin(3\omega_0 t_1)$, $a_{18}=\cos(3\omega_0 t_1)$.

The voltage signal is sampled at intervals of Δt s. Equation (2.4) can be rewritten in the following form by substituting $t_1 = \Delta t, 2\Delta t, \ldots\ldots, m\Delta t$ as follows.

$$v(\Delta t) = a_{11}x_1 + a_{12}x_2 + a_{13}x_3 + a_{14}x_4 + a_{15}x_5 + a_{16}x_6 + a_{17}x_7 + a_{18}x_8$$

$$v(2\Delta t) = a_{21}x_1 + a_{22}x_2 + a_{23}x_3 + a_{24}x_4 + a_{25}x_5 + a_{26}x_6 + a_{27}x_7 + a_{28}x_8$$

$$\vdots$$

$$v(m\Delta t) = a_{m1}x_1 + a_{m2}x_2 + a_{m3}x_3 + a_{m4}x_4 + a_{m5}x_5 + a_{m6}x_6 + a_{m7}x_7 + a_{m8}x_8. \qquad (2.5)$$

The a-coefficients can be redefined as follows:

$a_{m1}=1$, $a_{m2}=m\Delta t$, $a_{m3}=\sin(\omega_0 m\Delta t)$, $a_{m4}=\cos(\omega_0 m\Delta t)$, $a_{m5}=\sin(2\omega_0 m\Delta t)$,

$a_{m6}=\cos(2\omega_0 m\Delta t)$, $a_{m7}=\sin(3\omega_0 m\Delta t)$, $a_{m8}=\cos(3\omega_0 m\Delta t)$.

If S voltage samples are expressed as equations and S>8, the resulting equations can be written in the matrix form as

$$\underset{S\times 8}{[A]}\ \underset{8\times 1}{[x]} = \underset{S\times 1}{[v]}$$

The unknowns, [x], can be calculated as follows

$$[x]=[A]^{+}[v].$$

where $[A]^{+}$ is the left pseudo-inverse of [A] and is given by

$$[A]^{+} = [[A^{T}][A]]^{-1}[A^{T}].$$

The elements of the rows of $[A]^{+}$ are the coefficients of the LES filter that can be used for estimating the real and imaginary components of the fundamental frequency and harmonic frequency phasors of the voltages. These elements can be computed a priori in the off-line mode because Δt is known. The peak value of the fundamental and second harmonic components can then be calculated by using the equations given below.

$$V_1 = \sqrt{x_3^2 + x_4^2}$$

$$V_2 = \sqrt{x_5^2 + x_6^2}$$

A one cycle LES algorithm attenuates high-frequency components, noise and the decaying component.

Sachdev and Shah [9] applied the least error square technique for differential protection of transformers. They designed orthogonal fundamental and second harmonic frequency filters using a twelve sample window, a sampling rate of 720 Hz and the time reference coinciding with the center of the data window. They compared the peak values of the second harmonic components of the differential currents with their fundamental frequency components. If a second harmonic component exceeded 33 percent of the fundamental frequency component, their algorithm classified the situation as magnetizing inrush.

2.4.2.2. Discrete fourier algorithm

The Fourier algorithm [10] has also been used for computing phasors for use in differential relays. The following equations are used to calculate the real and imaginary components of phasors of the fundamental and harmonic frequencies.

$$v_r(k) = \frac{2}{m}\sum_{n=0}^{m-1} v(t).\sin\left(\frac{2\pi n}{m}\right), \text{ and} \tag{2.6}$$

$$v_i(k) = \frac{2}{m}\sum_{n=0}^{m-1} v(t).\cos\left(\frac{2\pi n}{m}\right) . \tag{2.7}$$

$$v_r(hk) = \frac{2}{m}\sum_{n=0}^{m-1} v(ht).\sin\left(\frac{2\pi n}{m}\right), \text{ and} \tag{2.8}$$

$$v_i(hk) = \frac{2}{m}\sum_{n=0}^{m-1} v(ht).\cos\left(\frac{2\pi n}{m}\right) . \tag{2.9}$$

where

v(t) is the voltage signal that can be expressed as $V_p \text{ Sin } (\omega_0 n \Delta t)$ in which V_p is the peak value of voltage, ω_0 is the fundamental frequency in rad/sec,

v(ht) is the voltage signal that can be expressed as $V_{ph} \text{ Sin } (h \omega_0 n \Delta t)$ in which V_{ph} is the peak value of h-th harmonic component of the voltage, $h\omega_0$ is the h-th harmonic frequency in rad/sec,

m is the number of samples per cycle,

$v_r(k)$ and $v_r(hk)$ are the real parts of the fundamental and harmonic frequency components of signal at time $t=k\Delta t$, and

$v_i(k)$ and $v_i(hk)$ are the imaginary parts of the fundamental and harmonic frequency components of signal at time $t=k\Delta t$.

The peak value and phase angle at t=k Δt can be expressed as follows:

$$V_p^2(k) = v_r^2(k) + v_i^2(k) \tag{2.10}$$

$$\theta_v(k) = \arctan\left(\frac{v_i(k)}{v_r(k)}\right) \tag{2.11}$$

The algorithm described in Reference [10] uses five signals, one trip signal and four restraining signals. The trip signal is the magnitude of the fundamental frequency component of the differential current. The first restraint signal is the through current to prevent tripping on heavy external faults. The second restraint signal prevents tripping when the transformer is operating with the primary circuit breaker open. The third and fourth restraint signals are the second and fifth harmonic components of the differential currents which provide restraint during magnetizing inrush and overexcitation respectively.

Like the LES technique, the Fourier algorithm is effective in attenuating high frequency harmonics, and constant dc, but the decaying component of the dc adversely effects the estimates of the phasors.

2.4.2.3. Kalman filter

The Kalman filter [11, 12, 13] is a recursive filter that estimates phasors from sampled data. The procedure of designing a Kalman filter consists of the following steps:

(i) Develop a state space model of the signal to be processed including the changes which may occur in the system operating states.

(ii) Identify the statistical properties of the signal.

(iii) Evaluate the Kalman gains which minimize the square of the expected errors between values of the actual and estimated system states.

(iv) Implement the filter using the calculated Kalman gains.

Sachdev, Wood and Johnson [11] explained the Kalman filtering technique in power system terminology and demonstrated its application for estimating phasors representing voltages and currents. Murty and Smolinski [14] used the approach in an algorithm for power transformer protection. Initially, they modeled the differential currents as sums of the fundamental component, the second harmonic component and a decaying dc component. Later, they used an eleven state model [15] which was previously reported in Reference [11]. Reference [15] computed the fundamental, second, fourth and fifth harmonic components in each differential current, and the fundamental frequency component in each through current. The second and fourth harmonic components of the differential currents were used to restrain tripping during magnetizing inrush. The fifth harmonic components were used to inhibit tripping during overexcitation.

The Kalman filter performs optimally if the statistical properties of the currents being processed are known, and are used in designing the filter. Since the statistical properties are not known and are estimated, the filter produces sub-optimal phasor estimates. The Kalman filter also has limited ability to handle effectively the decaying dc components of the fault currents.

2.4.3. Model-based algorithms

Some digital algorithms which do not use harmonic components of differential currents to discriminate magnetizing inrush from internal faults have been proposed in the past. These are based on transformer models.

Sykes [16] proposed an algorithm that used the saturation of the transformer core for identifying magnetizing inrush. The transformer model used in the algorithm involved resistance, and the self and mutual-inductances of the primary and secondary

windings. Mathematical equations were developed which expressed the voltages of the primary and secondary windings as functions of the primary and secondary currents and the parameters of the windings. It was suggested that the magnetizing inrush can be distinguished from the faults in the transformer by comparing the computed values of the voltages with their measured values. For magnetizing inrush, the computed and measured voltages are close whereas they are substantially different during internal faults.

Another algorithm, which used the electrical-magnetic interrelation of a transformer, was proposed by Jin and Sachdev [17]. The algorithm protects single-phase two-winding transformers. Transformer model was based on the equivalent-circuit of a single-phase transformer. Assuming that the hysteresis current is small, the magnetizing current is calculated by taking the difference of the primary current and the secondary winding currents referred to the primary side. For external faults, normal operating conditions and magnetizing inrush, the relation between the magnetizing current and the terminal voltage holds good. This relationship is not satisfied for faults in the transformer.

Inagaki et al. [18] proposed an algorithm based on the equivalent-circuit of a multi-circuit transformer. The equivalent circuit contains transfer susceptances and shunt susceptances. The model remains unchanged as the operating conditions change. The values of the transfer susceptances remain constant for all operating conditions but the values of shunt susceptances change as the operating parameters change. The fact, that the values of shunt susceptances are different for normal operating conditions (and external faults) and internal faults, was used to detect faults.

An algorithm that uses the relationship of the primary and secondary voltages and currents and parameters of the transformer was proposed by Sidhu, Sachdev and Wood [19, 20]. The algorithm estimates a phase voltage of the primary side by using samples of primary and secondary currents, secondary voltage and a previous sample of

primary voltage. The estimated and measured primary voltages are compared to detect winding faults in the transformer. Another approach, that used modal transformation, for detecting winding faults has been proposed by Sidhu and Sachdev [21]. Modal voltage drops, estimated from samples of transformer voltages and currents, are compared with the measured voltage drops. They are equal for magnetizing inrush and faults outside the transformer zone, but are not equal for faults in the transformer.

2.5. Discussion of the algorithms

Algorithms used in differential relays have been reviewed in Section 2.4. This section presents a critical analysis of these algorithms.

The operating voltages of power systems and lengths of transmission lines have increased substantially in recent years. Also, the loads are non-linear. Because of these factors, differential currents during internal transformer faults can contain large harmonic currents. Harmonic currents may also be present due to arcing and saturation of ct's, especially, during heavy faults. The algorithms based on harmonic restraint can, therefore, restrain a differential relay during internal faults. Also, if a faulted transformer is energized, magnetizing inrush currents and fault currents are experienced simultaneously. The harmonics in the inrush current can prevent the algorithms from issuing a trip command until the inrush currents have decayed substantially.

The algorithm of Reference 16 is based on a linear model of a two-winding single-phase transformer. The algorithm experiences errors during magnetizing inrush because the flux-current relationship of a transformer core is non-linear. The sensitivity of the relay is decreased when a transformer is energized and magnetizing inrush is expected. The algorithm is, therefore, not able to detect low-level internal faults. Reference 17 uses a tee-model consisting of the leakage inductances of the windings and the magnetizing inductance. The magnetizing inductance is not generally known and has to be determined experimentally. The application of this algorithm for protecting three-phase transformers requires further developmental work. The algorithm suggested

by Inagaki et al. [18] uses an equivalent pi-model of a three-winding single-phase transformer. The number of elements used in the pi-model increases considerably if the algorithm is to be applied for three-phase two-windings and three-phase three-windings transformers. The model becomes complex and computations increase.

The algorithms based on transformer models of Reference 16, 17 and 18 use winding currents to make decisions. All winding currents are not available in three-phase delta-wye transformers. The application of the model-based algorithms is, thus, limited to single-phase and three-phase wye-wye transformers. Algorithms of Reference 19, 20 and 21 will be affected by ct ratio-mismatch and saturation conditions since the fault-detection is based on combined use of primary and secondary side currents.

2.6. Algorithms dealing with CT saturation

Current transformer saturation is a serious problem which is encountered in many practical applications. As described in Section 2.2.3, the secondary current of a ct does not correctly represents the primary current in case the ct is saturated. Two algorithms, that deals with ct saturation, are briefly reviewed in this Section.

Mikrut, Winkler and Witek [22] assured correct performance of differential protective scheme during out-zone faults, leading to saturation of cts, by using the criterion based on the time-lag between the appearance of the restraint current and operating current waveforms. They suggested that during faults located beyond the protected zone, there is always a marked time-difference between the appearance of the restraint current and operating current waveforms. The latter one occurs not earlier than about 5-8 ms after the first impulse of the restraint current. The studies show that the second and fifth harmonics produced by saturated cts have an expedient influence on the performance of the differential protection scheme, since they additionally stabilize it during external faults, especially if large values of amplification factors for these harmonics are chosen. During an in-zone fault, the operating and restraint currents always appear immediately after the fault-inception. However, the second and fifth harmonics produced by saturated cts can be high which restrains the relay for a certain

time interval. This misoperation of the relay can be mitigated by the optimum choice of harmonics in the harmonic restraint circuits and control of the operating current.

Hosemann and Steigerwald [23] developed a saturation detector for current transformers. The secondary current of a ct is transformed into space phasors with a blocked backward rotating component. In the unsaturated state, the trajectory traversed by rotating component is a circle. The deviation from this characteristic indicates the inception of ct saturation. The detection of ct saturation can be utilized to adjust sensitivity of the differential relay.

The algorithms dealing with ct saturation have serious drawbacks. Special means are used to control relay decisions in the algorithm proposed by Mikrut, Winkler and Witek [22]. The harmonics generated by saturated ct's have adverse effect during internal faults as the differential relay using harmonic-restraint feature will be restrained for some time. This is because the presence of harmonics is attributed to condition of magnetizing inrush. As such, special criteria like proper choice of the amplification factor for harmonics in filters, threshold value of the operating current and determination of the time-interval between zero-crossings of the currents are required to ensure correct relay operation. Any error in implementing these criteria results in restraining the relay during internal faults.

The method of detecting ct saturation, reported in Reference 23, will not work very well in the case of switching-on of a faulted transformer. In such a situation, the currents will contain substantial level of harmonics. Therefore, the trajectories traversed by the phasors will not be circular. The proposed algorithm will consider this incorrectly as a case of ct saturation and operation of the relay is blocked. The blocking will continue until the signals become sinusoidal which happens after a considerable time.

2.7. Summary

An overview of differential protection has been presented in this chapter. Effects of magnetizing inrush, ratio-mismatch and saturation of cts have been briefly discussed. Harmonic-restraint and percentage-bias features of differential relays have been also described. Some previously proposed digital algorithms for protecting power transformers have been briefly reviewed. It is noted that most of these algorithms use comparison between the magnitudes of the fundamental and harmonic frequency components and differ basically in their computational methods only. Also, no substantive work has been reported on the phenomenon of ct saturation. Two algorithms proposed for this purpose use special criteria to make correct decisions which is a serious drawback.

3. THE PROPOSED TECHNIQUE

3.1. Introduction

A description of a commonly used protection scheme, differential protection, is given in the previous chapter. A brief review of previously proposed digital algorithms for protection of power transformers is also presented. Limitations associated with these algorithms are outlined. It is shown that including harmonic-restraint feature and percentage-bias characteristics prevents the relay from operating during magnetizing inrush and current transformer ratio-mismatch conditions.

The concept of symmetrical components [24] has been used in the past to develop algorithms for protection of power system equipments [25]. This chapter describes the development of a technique which can detect internal faults in the power transformers and distinguish them from external faults. The technique uses fundamental frequency voltage and current phasors computed from quantized samples of voltages and currents at the transformer terminals. From these voltage and current phasors, the positive- and negative-sequence phasors are calculated and manipulated to estimate the positive- and negative-sequence impedances. Using the seen impedance, the relay can distinguish between faults internal and external to the power transformer. Fault-detection characteristic and the digital algorithm based on the proposed technique are described in the chapter. The application of the proposed technique for protecting unloaded transformers is also discussed. The issue of switching-on of a faulted transformer is also addressed. A criterion to detect switch-on faults based on transformation ratio is developed. Linking of all the proposed algorithms is described with the help of a flow chart.

3.2. Development of the technique

Figure 3.1 shows a transformer connected to a system, represented by G_x, on one end and a transmission line on the other. The remote end of the transmission line is connected to a system G_y. The power transformer is protected by relays. The relays R_x and R_y consider the current flowing into the transformer as positive. This system is used to develop the proposed technique for protecting power transformers.

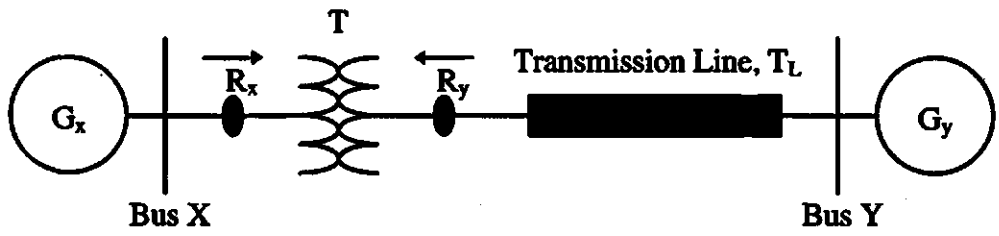


Figure 3.1. Circuit used for developing the proposed technique for protecting power transformers.

3.2.1. External fault

For an external fault at bus Y, the pre-fault and fault positive-sequence networks are as shown in Figures 3.2(a) and 3.2(b). The power transformer is represented by its positive-sequence impedance, Z_{t1} in the networks. The Thevenin equivalent circuit is shown in Figure 3.2(c). The fault impedance is shown as Z_f, which either could be the arc-resistance or could be the equivalent of a combination of the negative and zero-sequence networks of the system appropriately connected to represent selected unbalanced faults. The Thevenin voltage, V_{y1}, is the pre-fault positive-sequence voltage at the fault location. E_{x1} and E_{y1} are the positive-sequence internal voltages for the generators G_x and G_y respectively. The positive-sequence incremental voltages, ΔV_{x1} and ΔV_{y1}, and incremental currents, ΔI_{x1} and ΔI_{y1}, can be expressed as follows:

$$\Delta V_{x1} = V_{Rx1(fault)} - V_{Rx1\ (pre\text{-}fault)} \tag{3.1}$$

$$\Delta V_{y1} = V_{Ry1(fault)} - V_{Ry1\ (pre\text{-}fault)} \tag{3.2}$$

$$\Delta I_{x1} = I_{Rx1\ (fault)} - I_{Rx1(pre\text{-}fault)} \tag{3.3}$$

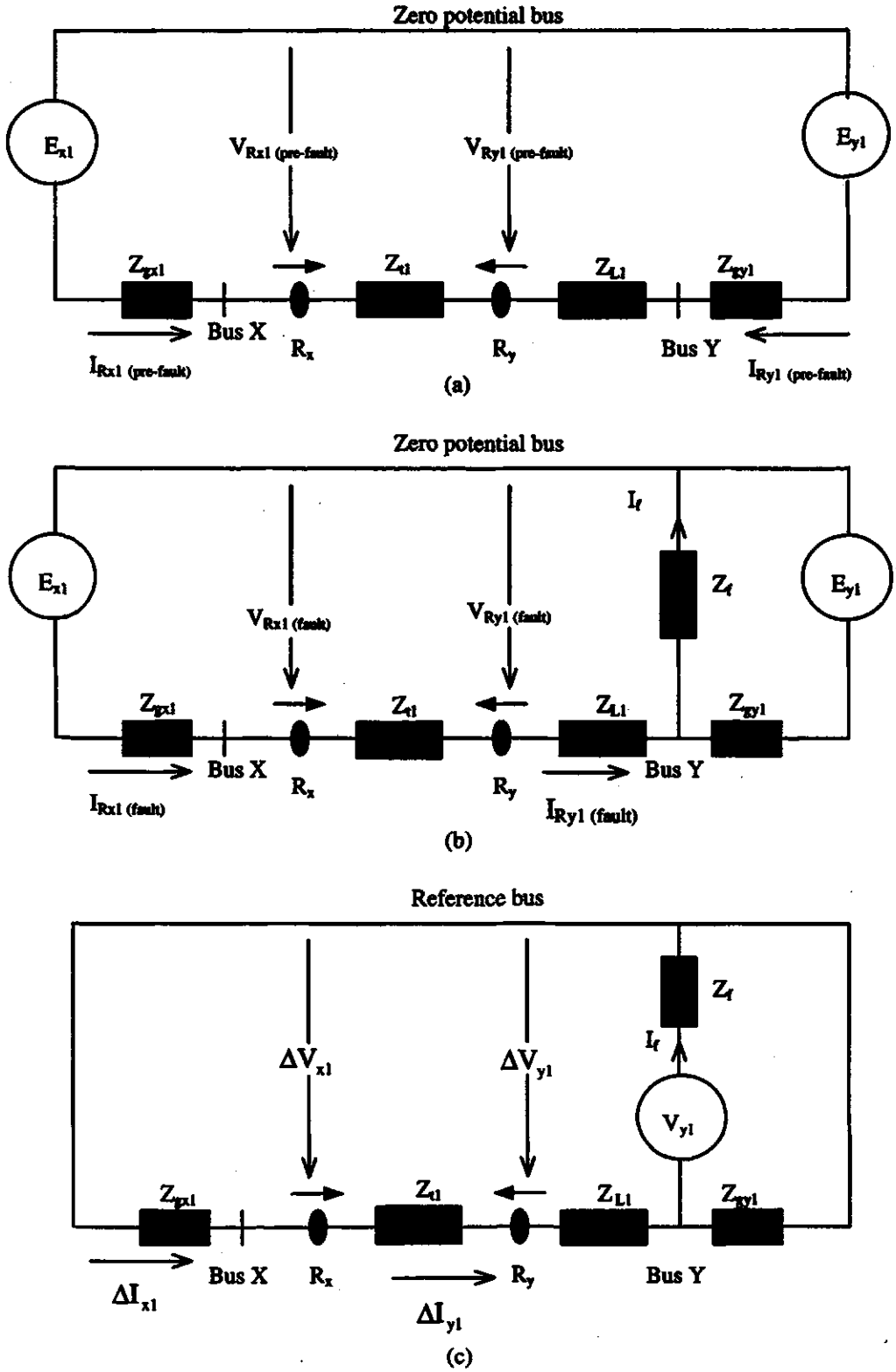


Figure 3.2. Positive-sequence networks for the power system of Figure 3.1 for an external fault (a) Pre-fault circuit, (b) fault circuit and (c) Thevenin's equivalent circuit.

$$\Delta I_{y1} = I_{Ry1\,(fault)} - I_{Ry1(pre\text{-}fault)} \quad (3.4)$$

where:

$V_{Rx1\,(pre\text{-}fault)}$ is the positive-sequence voltage at R_x before the occurrence of a fault,

$V_{Rx1\,(fault)}$ is the positive-sequence voltage at R_x after the occurrence of a fault,

$V_{Ry1\,(pre\text{-}fault)}$ is the positive-sequence voltage at R_y before the occurrence of a fault,

$V_{Ry1\,(fault)}$ is the positive-sequence voltage at R_y after the occurrence of a fault,

$I_{Rx1\,(pre\text{-}fault)}$ is the positive-sequence current at R_x before the occurrence of a fault,

$I_{Rx1\,(fault)}$ is the positive-sequence current at R_x after the occurrence of a fault,

$I_{Ry1\,(pre\text{-}fault)}$ is the positive-sequence current at R_y before the occurrence of a fault, and

$I_{Ry1\,(fault)}$ is the positive-sequence current at R_y after the occurrence of a fault.

The positive-sequence pre-fault and fault voltages at R_x can be expressed in terms of generator voltages, relay currents and the system parameters by the following equations.

$$V_{Rx1\,(pre\text{-}fault)} = E_{x1} - I_{Rx1\,(pre\text{-}fault)}\, Z_{gx1} \quad (3.5)$$

$$V_{Rx1\,(fault)} = E_{x1} - I_{Rx1\,(fault)}\, Z_{gx1} \quad (3.6)$$

where:

Z_{gx1} is the positive-sequence impedance of generator G_x.

Subtracting Equation 3.5 from Equation 3.6 provides

$$V_{Rx1\,(fault)} - V_{Rx1\,(pre\text{-}fault)} = (E_{x1} - I_{Rx1\,(fault)} Z_{gx1}) - (E_{x1} - I_{Rx1\,(pre\text{-}fault)} Z_{gx1}). \quad (3.7)$$

Simplifying the right hand side of this equation provides

$$V_{Rx1\,(fault)} - V_{Rx1\,(pre\text{-}fault)} = -(I_{Rx1\,(fault)} - I_{Rx1\,(pre\text{-}fault)}) Z_{gx1}. \quad (3.8)$$

Substituting Equations 3.1 and 3.3 in this equation provides

$$\Delta V_{x1} = -\Delta I_{x1} Z_{gx1}. \quad (3.9)$$

Rearranging this equation provides

$$\frac{\Delta V_{x1}}{\Delta I_{x1}} = -Z_{gx1}. \quad (3.10)$$

Similarly, the positive-sequence pre-fault and fault voltages at R_y can be expressed by the following equations.

$$V_{Ry1\,(pre\text{-}fault)} = E_{x1} - I_{Rx1\,(pre\text{-}fault)} (Z_{gx1} + Z_{t1}) \quad (3.11)$$

$$V_{Ry1\,(fault)} = E_{x1} - I_{Rx1\,(fault)} (Z_{gx1} + Z_{t1}) \quad (3.12)$$

where:

Z_{gx1} is the positive-sequence impedance of generator G_x, and

Z_{t1} is the positive-sequence impedance of power transformer.

Subtracting Equation 3.11 from Equation 3.12 provides

$$V_{Ry1\,(fault)} - V_{Ry1\,(pre\text{-}fault)} = (E_{x1} - I_{Rx1\,(fault)} (Z_{gx1} + Z_{t1})) - (E_{x1} - I_{Rx1\,(pre\text{-}fault)} (Z_{gx1} + Z_{t1})) \quad (3.13)$$

Simplifying the right hand side of this equation provides

$$V_{Ry1\,(fault)} - V_{Ry1\,(pre\text{-}fault)} = (I_{Rx1\,(pre\text{-}fault)} - I_{Rx1\,(fault)}) (Z_{gx1} + Z_{t1}). \quad (3.14)$$

Substituting Equations 3.2 and 3.4 in this equation provides

$$\Delta V_{yi} = \Delta I_{y1} (Z_{gx1} + Z_{t1}) \quad (3.15)$$

Rearranging this equation provides

$$\frac{\Delta V_{y1}}{\Delta I_{y1}} = + (Z_{gx1} + Z_{t1}). \tag{3.16}$$

The negative-sequence incremental quantities can be defined now by Equations 3.17 to 3.20 using Figures 3.3(a) and 3.3(b).

$$\Delta V_{x2} = V_{Rx2\,(fault)} - V_{Rx2\,(pre\text{-}fault)} \tag{3.17}$$

$$\Delta V_{y2} = V_{Rx2\,(fault)} - V_{Rx2\,(pre\text{-}fault)} \tag{3.18}$$

$$\Delta I_{x2} = I_{Rx2\,(fault)} - I_{Rx2\,(pre\text{-}fault)} \tag{3.19}$$

$$\Delta I_{y2} = I_{Ry2\,(fault)} - I_{Ry2\,(pre\text{-}fault)} \tag{3.20}$$

where:

$V_{rx2(pre\text{-}fault)}$ is the negative-sequence voltage at R_x before the occurrence of a fault,

$V_{Rx2\,(fault)}$ is the negative-sequence voltage at R_x after the occurrence of a fault,

$V_{Ry2\,(pre\text{-}fault)}$ is the negative-sequence voltage at R_y before the occurrence of a fault,

$V_{Ry2\,(fault)}$ is the negative-sequence voltage at R_y after the occurrence of a fault,

$I_{Rx2\,(pre\text{-}fault)}$ is the negative-sequence current at R_x before the occurrence of a fault,

$I_{Rx2\,(fault)}$ is the negative-sequence current at R_x after the occurrence of a fault,

$I_{Ry2\,(pre\text{-}fault)}$ is the negative-sequence current at R_y before the occurrence of a fault, and

$I_{Ry2\,(fault)}$ is the negative-sequence current at R_y after the occurrence of a fault.

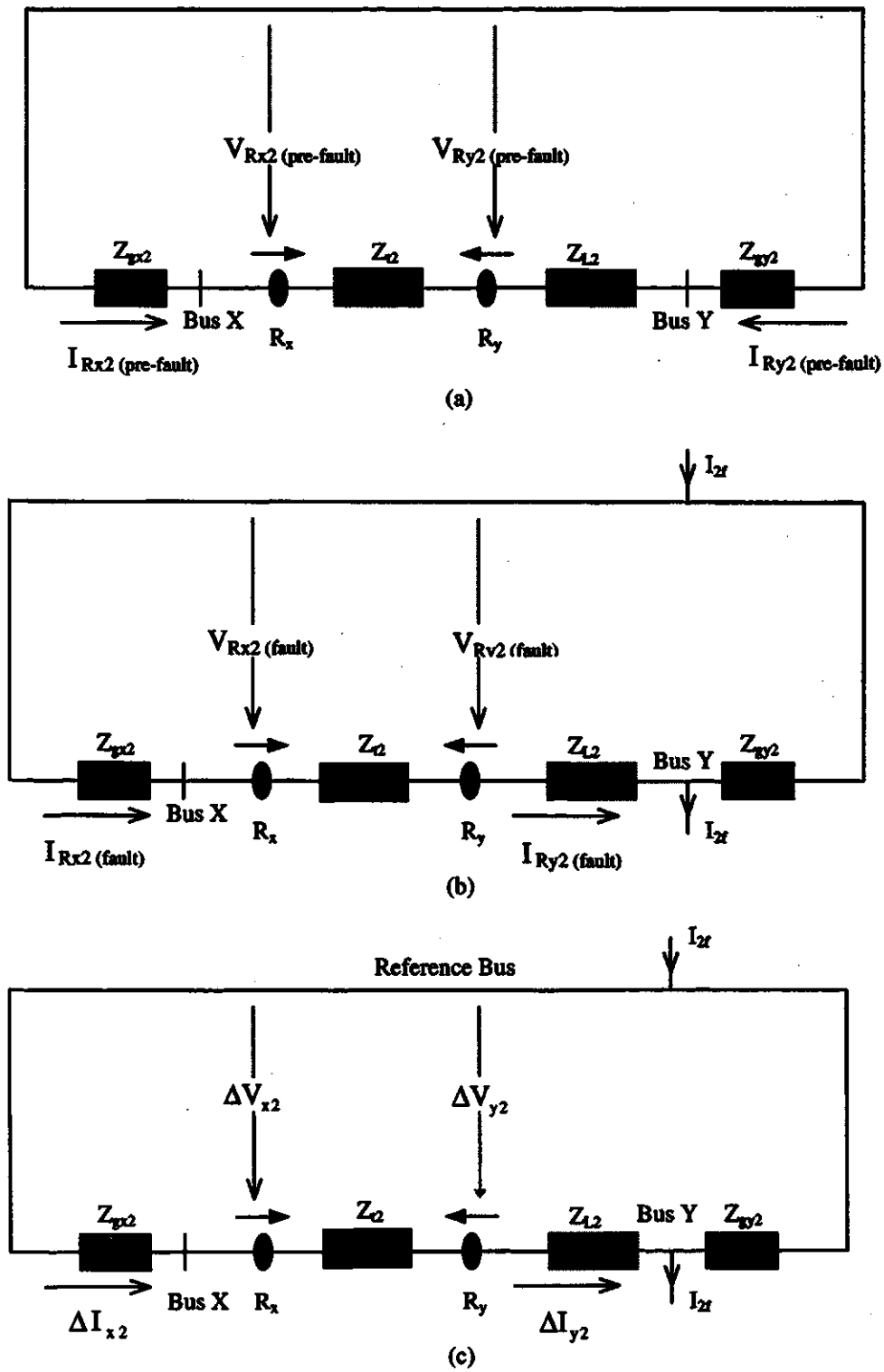


Figure 3.3. Negative-sequence networks for the power system of Figure 3.1 for an external fault (a) Pre-fault circuit, (b) fault circuit and (c) Thevenin's equivalent circuit.

The negative-sequence pre-fault and fault voltages at R_x can be expressed in terms of the relay currents and system parameters by the following equations.

$$V_{Rx2\,(pre\text{-}fault)} = - I_{Rx2\,(pre\text{-}fault)}\, Z_{gx2} \tag{3.21}$$

$$V_{Rx2\,(fault)} = - I_{Rx2\,(fault)}\, Z_{gx2} \tag{3.22}$$

where:

Z_{gx2} is the negative-sequence impedance of generator G_x.

Subtracting Equation 3.21 from Equation 3.22 provides

$$V_{Rx2\,(fault)} - V_{Rx2\,(pre\text{-}fault)} = (- I_{Rx2\,(fault)}\, Z_{gx2}) - (- I_{Rx2\,(pre\text{-}fault)}\, Z_{gx2}) . \tag{3.23}$$

Simplifying the right hand side of this equation provides

$$V_{Rx2\,(fault)} - V_{Rx2\,(pre\text{-}fault)} = -(I_{Rx1\,(fault)} - I_{Rx1\,(pre\text{-}fault)})\, Z_{gx2} . \tag{3.24}$$

Substituting Equations 3.17 and 3.19 in this equation provides

$$\Delta V_{x2} = - \Delta I_{x2}\, Z_{gx2} . \tag{3.25}$$

Rearranging this equation provides

$$\frac{\Delta V_{x2}}{\Delta I_{x2}} = - Z_{gx2} \tag{3.26}$$

Similarly, the negative-sequence pre-fault and fault voltages at R_y can be expressed by the following equations.

$$V_{Ry2\,(pre\text{-}fault)} = - I_{Rx2\,(pre\text{-}fault)}\, (Z_{gx2} + Z_{t2}) \tag{3.27}$$

$$V_{Ry2\,(fault)} = - I_{Rx2\,(fault)}\, (Z_{gx2} + Z_{t2}) \tag{3.28}$$

where:

Z_{gx2} is the negative-sequence impedance of generator G_x, and

Z_{t2} is the negative-sequence impedance of the power transformer.

Subtracting Equation 3.27 from Equation 3.28 provides

$$V_{Ry2\,(fault)} - V_{Ry2\,(pre\text{-}fault)} = (- I_{Rx2\,(fault)} (Z_{gx2} + Z_{t2})) - (- I_{Rx2\,(pre\text{-}fault)} (Z_{gx2} + Z_{t2})). \quad (3.29)$$

Simplifying the right hand side of this equation provides

$$V_{Ry2\,(fault)} - V_{Ry2\,(pre\text{-}fault)} = (I_{Rx2\,(pre\text{-}fault)} - I_{Rx2\,(fault)}) (Z_{gx2} + Z_{t2}). \quad (3.30)$$

Substituting Equations 3.18 and 3.20 in this equation provides

$$\Delta V_{y2} = \Delta I_{y2} (Z_{gx2} + Z_{t2}). \quad (3.31)$$

Rearranging this equation provides

$$\frac{\Delta V_{y2}}{\Delta I_{y2}} = + (Z_{gx2} + Z_{t2}). \quad (3.32)$$

3.2.2. Internal fault

The positive-sequence networks for a fault in the transformer zone are shown in Figure 3.4. Figure 3.4(a) shows the network representing the pre-fault operation and Figure 3.4(b) shows the network representing the system during the fault. The Thevenin equivalent circuit is shown in Figure 3.4(c). Z_{L1} is the positive-sequence impedance of the transmission line. The constant, m, defines the fault-location in the power transformer and can be assumed to have values in the range 0 to 1.

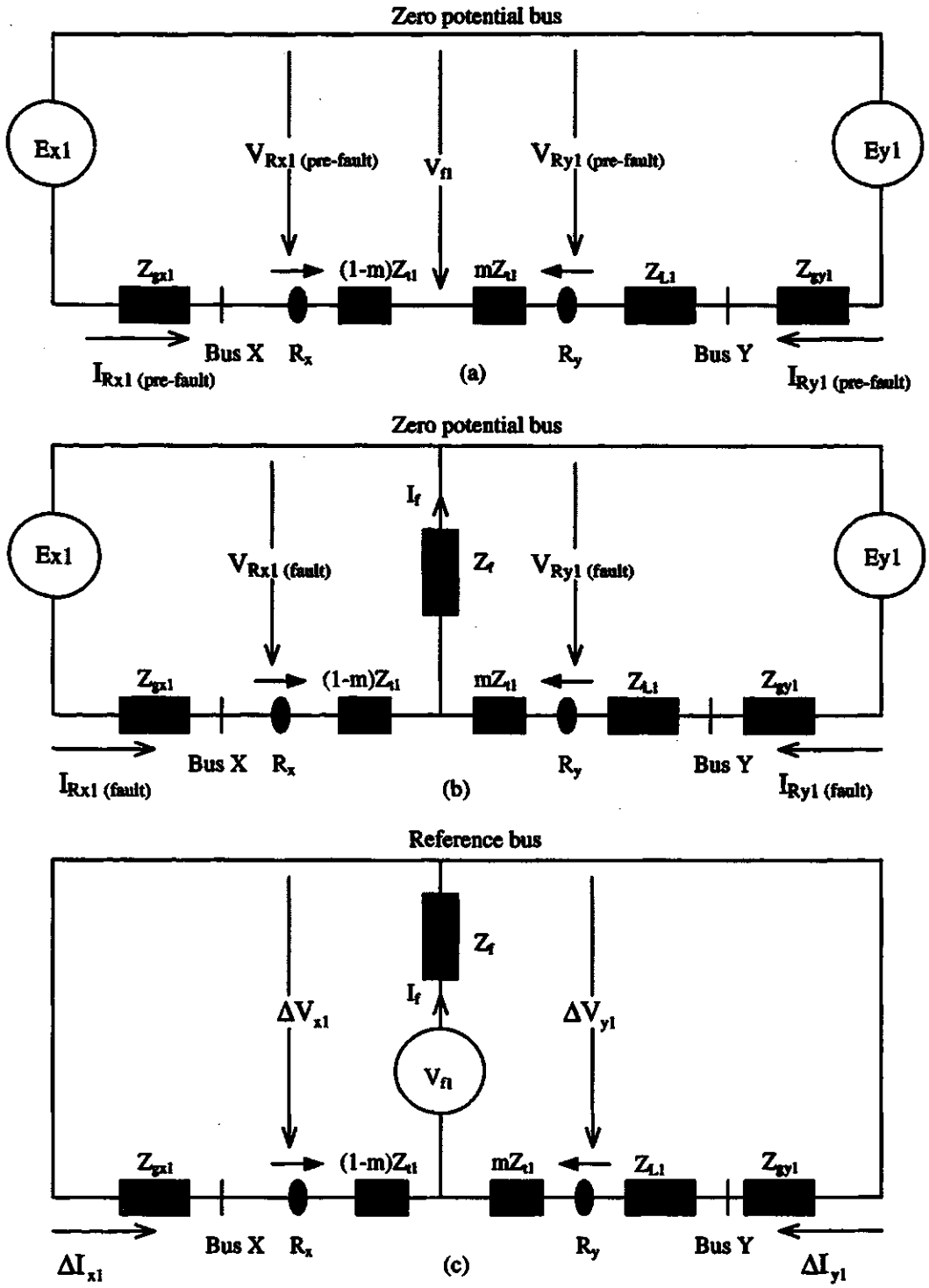
Using an approach similar to that used in Section 3.2.1, the incremental positive-sequence voltage computed by relay R_x is given by

$$\Delta V_{x1} = - Z_{gx1} \Delta I_{x1}. \quad (3.33)$$

Rearranging this equation provides the positive-sequence impedance seen by the relay R_x as follows.

$$\frac{\Delta V_{x1}}{\Delta I_{x1}} = -Z_{gx1}. \quad (3.34)$$

Similarly, the incremental positive-sequence voltage computed by relay R_y is given by



Note: A crude representation of the power transformer is shown for development of the technique for occurrence of an internal fault.

Figure 3.4. Positive-sequence networks for the power system of Figure 3.1 (internal fault). (a) Pre-fault, (b) fault and (c) Thevenin's equivalent circuit.

$$\Delta V_{y1} = - (Z_{gy1} + Z_{L1}) \Delta I_{y1} \quad (3.35)$$

Rearrangement of this equation provides the positive-sequence impedance seen by relay R_y as follows.

$$\frac{\Delta V_{y1}}{\Delta I_{y1}} = - (Z_{gy1} + Z_{L1}) . \quad (3.36)$$

The negative-sequence networks for a fault in the transformer zone are shown in Figure 3.5. Figure 3.5(a) shows the network representing the pre-fault operation and Figure 3.5(b) shows the network representing the system during the fault. The Thevenin equivalent circuit is shown in the Figure 3.5(c). It can be shown that, following the procedure already established, the negative-sequence incremental voltages at R_x and R_y are given by

$$\Delta V_{x2} = - Z_{gx2} \Delta I_{x2} \quad (3.37)$$

$$\Delta V_{y2} = - (Z_{gy2} + Z_{L2}) \Delta I_{y2} \quad (3.38)$$

where:

Z_{L2} is the negative-sequence impedance of the transmission line.

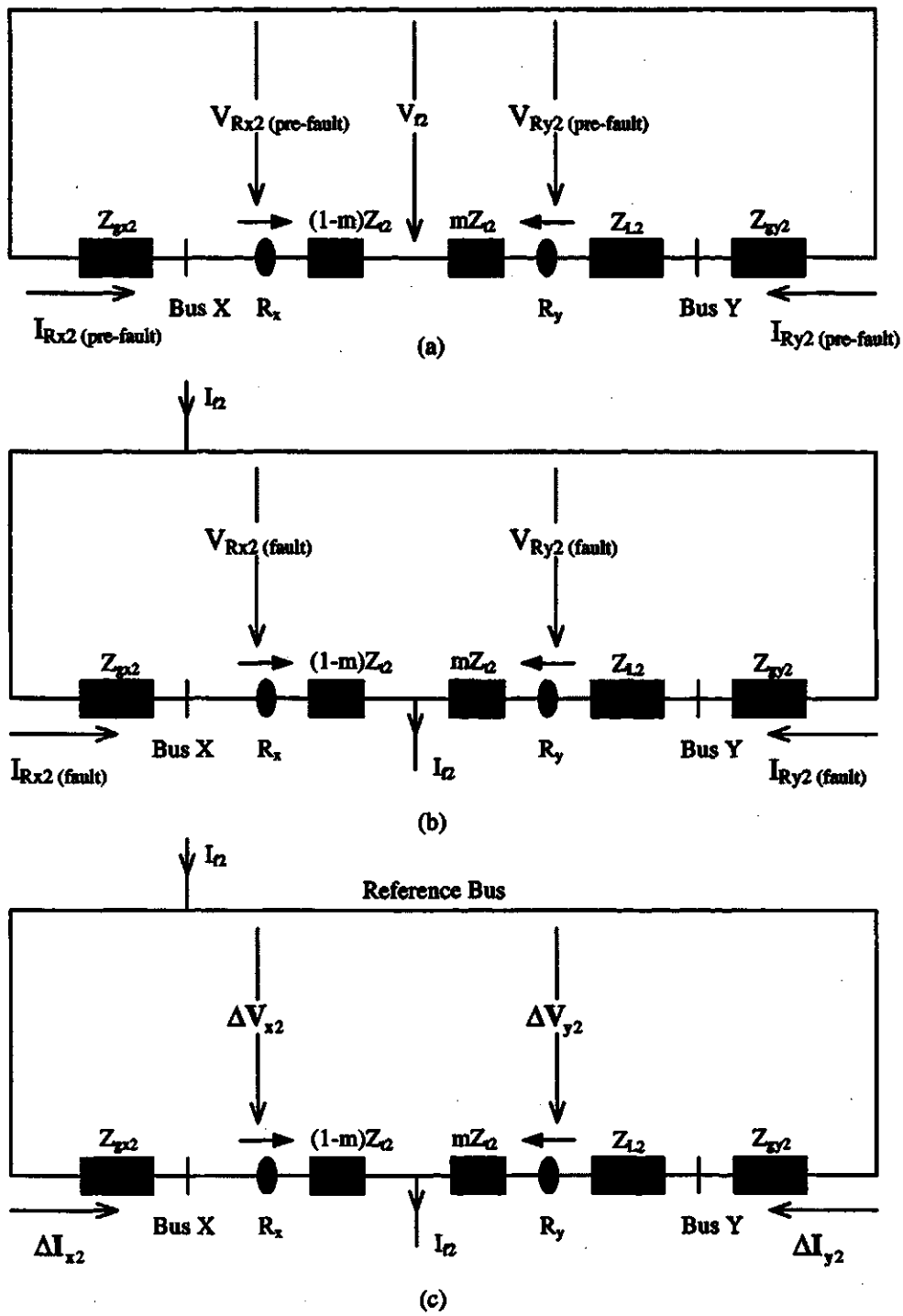
The negative-sequence impedance seen by the relay R_x and R_y can be obtained by rearranging these equations.

$$\frac{\Delta V_{x2}}{\Delta I_{x2}} = - Z_{gx2} \quad (3.39)$$

$$\frac{\Delta V_{y2}}{\Delta I_{y2}} = - (Z_{gy2} + Z_{L2}) \quad (3.40)$$

3.3. Fault-detection for unloaded transformers

The algorithm developed in Section 3.2 assumes that the transformer being protected is connected to power sources on both the primary and secondary sides. This



Note: A crude representation of the power transformer is shown for development of the technique for occurrence of an internal fault.

Figure 3.5. Negative-sequence networks for the power system of Figure 3.1 (internal fault). (a) Pre-fault, (b) fault and (c) Thevenin's equivalent circuit.

algorithm can be adapted to protect the transformer if it is connected to a source on the primary side and is not supplying any load.

Consider the system model shown in Figure 3.6, an operating state in which the system is experiencing a fault internal to the transformer zone, and another operating state in which the system is experiencing a fault external to the transformer zone.

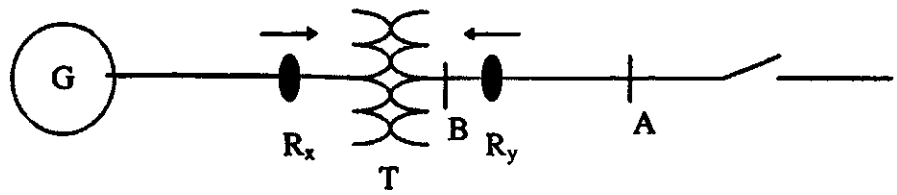


Figure 3.6. Unloaded power transformer.

3.3.1. External fault

The positive-sequence networks for pre-fault and fault at location A are shown in Figures 3.7(a) and 3.7(b). The incremental positive-sequence voltage at R_x as a function of the incremental positive-sequence current is given by

$$\Delta V_{x1} = -Z_{gx1}\ \Delta I_{x1}. \tag{3.41}$$

The positive-sequence impedance seen by the relay R_x is given by

$$\frac{\Delta V_{x1}}{\Delta I_{x1}} = -Z_{gx1} \tag{3.42}$$

Similarly, the incremental positive-sequence voltage at R_y as a function of the incremental positive-sequence current is given by

$$\Delta V_{y1} = -(Z_{gx1} + Z_{t1})\,\Delta I_{x1} \tag{3.43}$$

The positive-sequence impedance seen by the relay R_y is given by

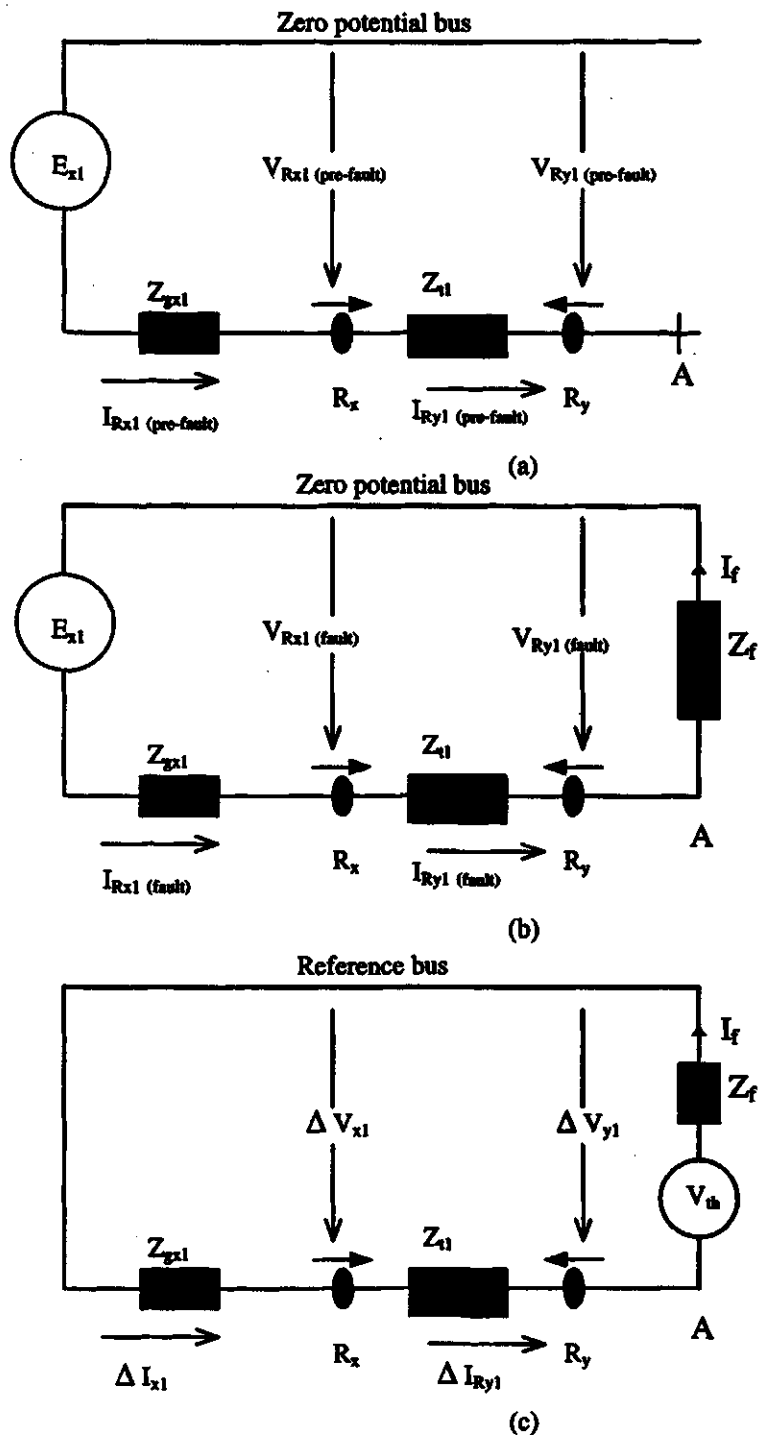


Figure 3.7. Positive-sequence networks for the power system of Figure 3.11 for an external fault at A). (a) Pre-fault, (b) fault and (c) Thevenin's equivalent circuit.

$$\frac{\Delta V_{y1}}{\Delta I_{y1}} = + (Z_{gx1} + Z_{t1}). \tag{3.44}$$

Following the procedure outlined for computation of positive-sequence impedances, the negative-sequence incremental voltages and currents for the relays can be derived using the negative-sequence pre-fault, fault and the Thevenin equivalent circuits shown in Figure 3.8. The incremental negative-sequence voltage at R_x as a function of the incremental negative-sequence current is given by

$$\Delta V_{x2} = - Z_{gx2}\ \Delta I_{x2}. \tag{3.45}$$

The negative-sequence impedance seen by the relay R_x is given by

$$\frac{\Delta V_{x2}}{\Delta I_{x2}} = - Z_{gx2}. \tag{3.46}$$

Similarly, the incremental negative-sequence voltage at R_y as a function of the incremental negative-sequence current is given by

$$\Delta V_{y2} = -(Z_{gx2} + Z_{t2})\,\Delta I_{x2}. \tag{3.47}$$

The negative-impedance impedance seen by the relay R_y is given by

$$\frac{\Delta V_{y2}}{\Delta I_{y2}} = + (Z_{gx2} + Z_{t2}). \tag{3.48}$$

3.3.2. Internal fault

The positive-sequence networks for a fault in the transformer protection zone are shown in Figure 3.9. The prefault, fault and the Thevenin equivalent representations are shown in this figure. As was done in Section 3.2.2, the positive-sequence incremental voltage at R_x is given by

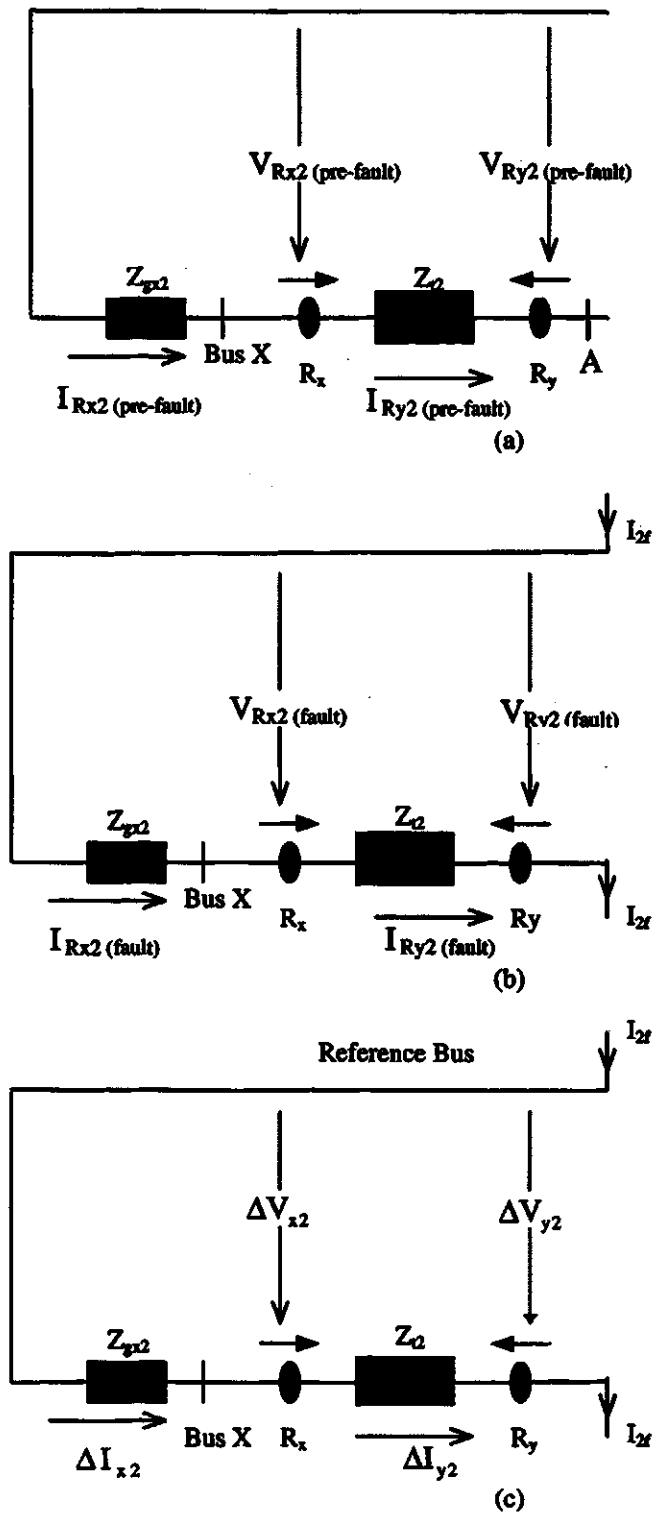
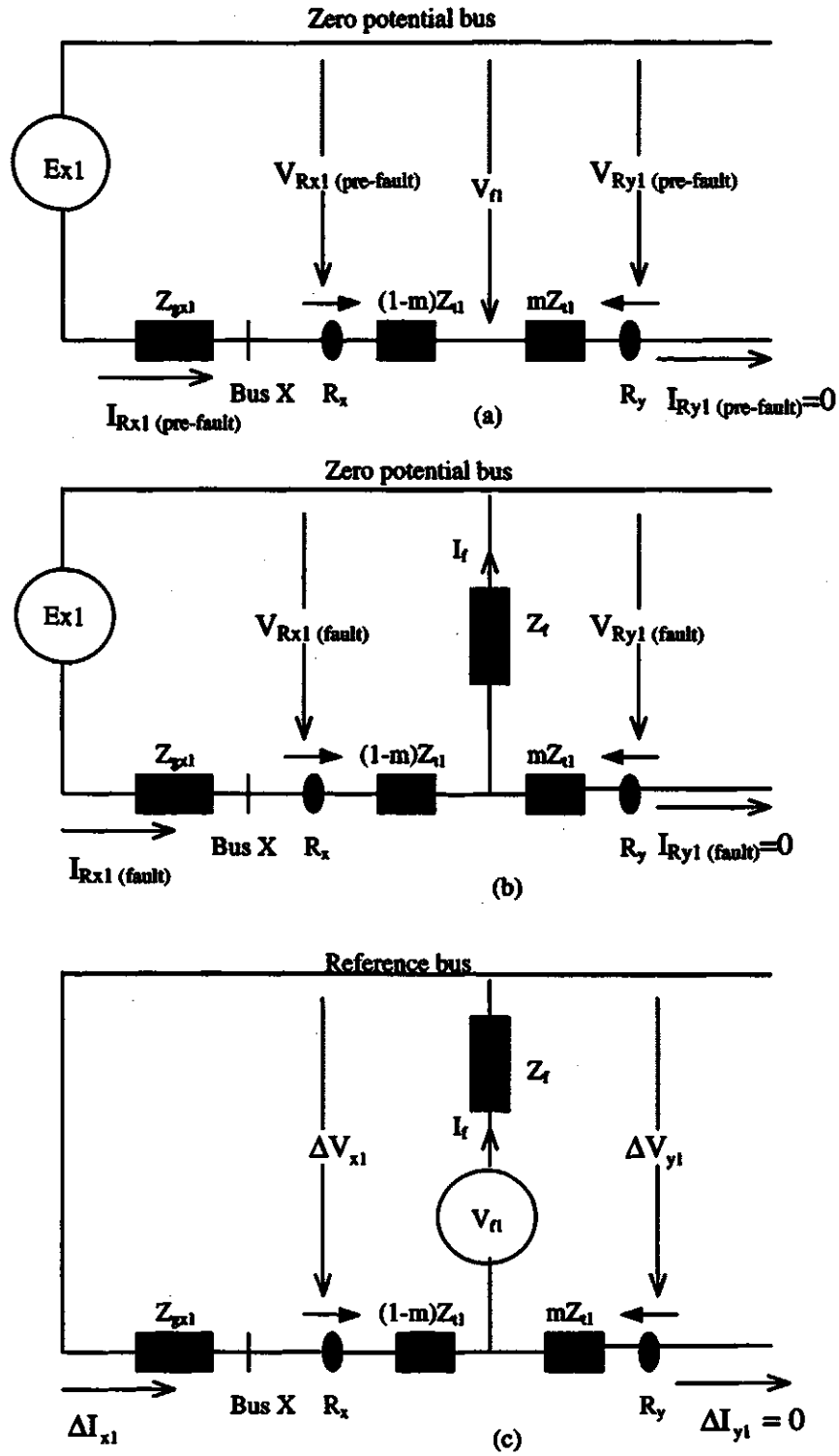


Figure 3.8. Negative-sequence networks for the power system of Figure 3.1 for an external fault. at A (a) Pre-fault, (b) fault and (c) Thevenin's equivalent circuit.



Note: A crude representation of the power transformer is shown for development of the technique for occurrence of an internal fault.

Figure 3.9. Positive-sequence networks for the power system of Figure 3.1 (internal fault). (a) Pre-fault, (b) fault and (c) Thevenin's equivalent circuit.

$$\Delta V_{x1} = - Z_{gx1}\ \Delta I_{x1}. \tag{3.49}$$

The positive-sequence impedance seen by the relay R_x can be expressed as

$$\frac{\Delta V_{x1}}{\Delta I_{x1}} = -Z_{gx1}. \tag{3.50}$$

There is no current at Relay R_y because the transformer is not supplying any load. The relay R_y does not sense any current and, therefore, does not compute the impedances.

Using a similar procedure, the negative-sequence impedance seen by relay R_x can be computed using the negative-sequence pre-fault, fault and Thevenin's representation of the system shown in Figures 3.10 (a), (b) and (c) respectively.

The negative-sequence incremental voltage at R_x is given by

$$\Delta V_{x2} = - Z_{gx2}\ \Delta I_{x2}. \tag{3.51}$$

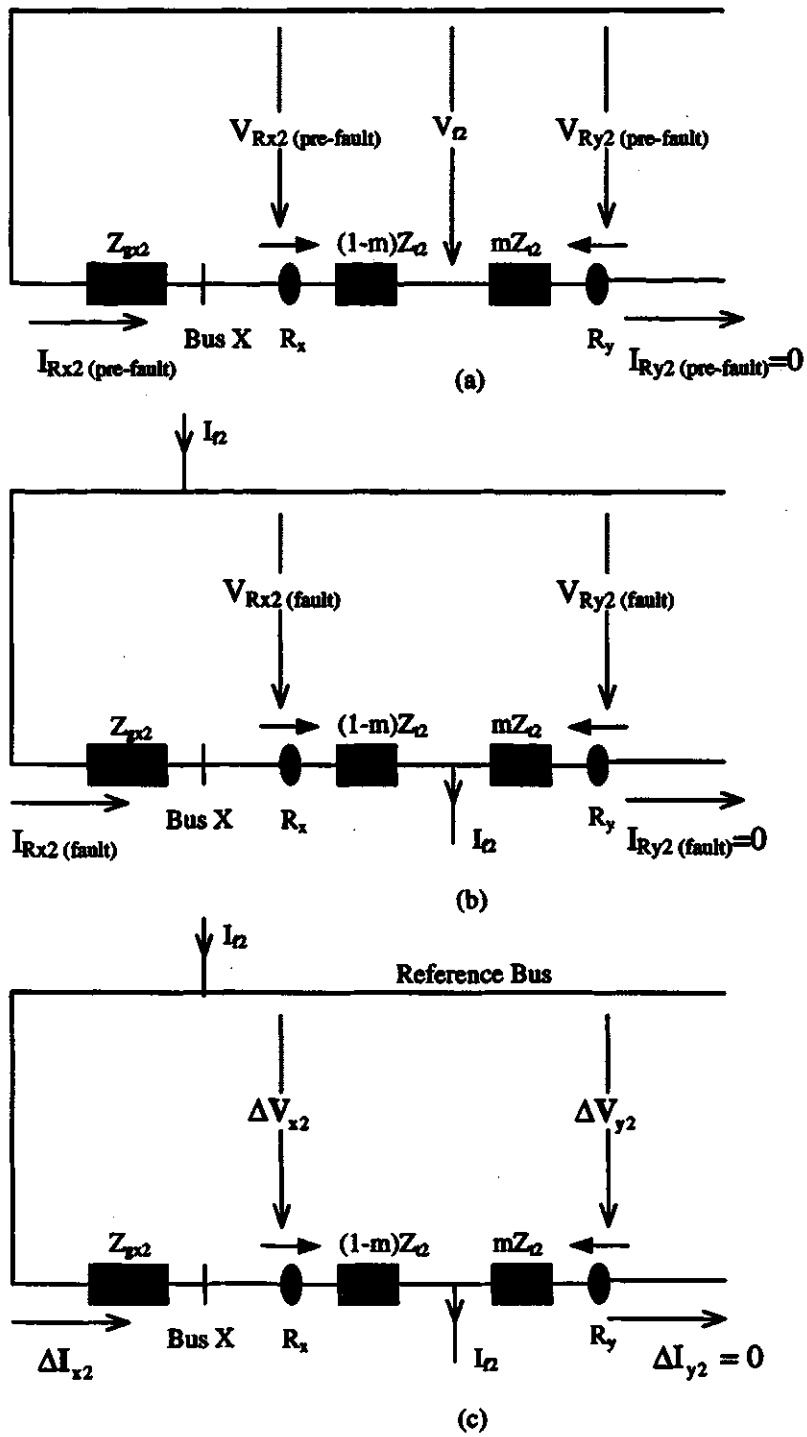
The negative-sequence impedance seen by the relay R_x is given by

$$\frac{\Delta V_{x2}}{\Delta I_{x2}} = -Z_{gx2}. \tag{3.52}$$

3.4. Computation of incremental voltages and currents

The voltage and current samples obtained from the power system are quantized and used for phasor calculations. At each sampling instant, the phasors and sequence-phasors are computed using a data window of fixed length. In the present work, a data window of 25 samples was used. The data window shifts continuously such that at every sampling instant a new sample is included and the oldest sample is discarded. The movement of data window is illustrated in Figure 3.11.

The sequence-phasors calculated using twenty five consecutive windows are saved in memory. The sequence-phasors calculated after the occurrence of fault (location



Note: A crude representation of the power transformer is shown for development of the technique for occurrence of an internal fault.

Figure 3.10. Negative-sequence networks for the power system of Figure 3.1 (internal fault). (a) Pre-fault, (b) fault and (c) Thevenin's equivalent circuit.

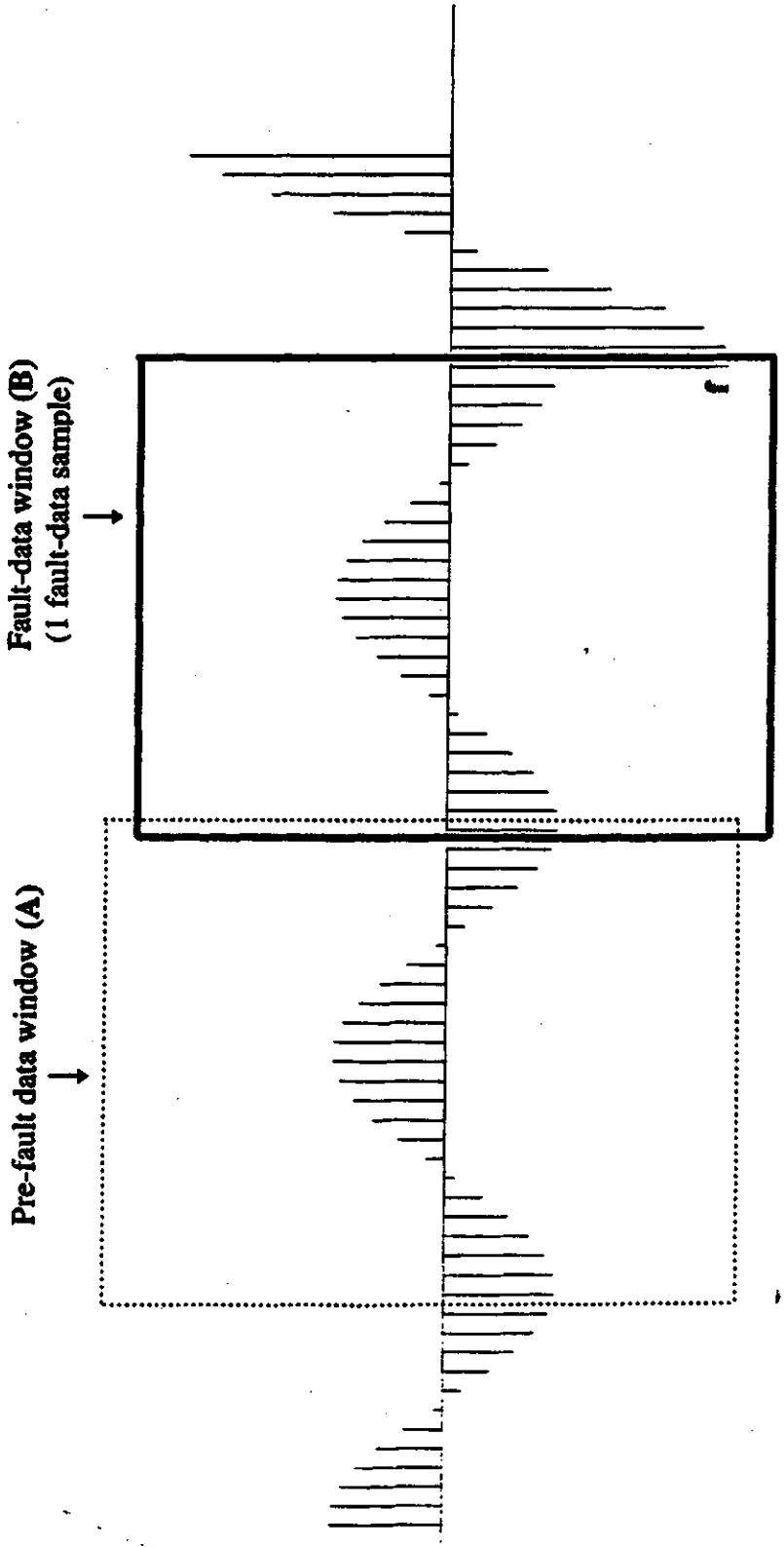


Figure 3.11. Location of data window at different sampling instants.

f in Figure 3.11) are used in conjunction with the corresponding pre-fault sequence phasors to compute the incremental sequence-phasors. For example, the sequence-phasor calculated using samples of data window B of Figure 3.11 is used alongwith the values of the sequence-phasors calculated using the pre-fault data window A. When the next sample is acquired, the fault data window is advanced by one sample from window B and the pre-fault phasor is calculated using the data window advanced by one sample from window A

3.5. The algorithm

A digital algorithm based on the fault-detection techniques proposed in Section 3.2 and 3.3 was developed for protecting power transformers. Each relay involved in the protection scheme executes the proposed algorithm, and the final decision is made by combining the observations made by the two relays. The algorithm uses the voltages and currents sampled simultaneously at a predefined rate, by the two relays. A flow chart of the proposed algorithm is shown in Figures 3.12. The following steps are performed in the algorithm:

1. Initialize the trigger indicator, TRIGGER, and trigger counters, TPOS and TNEG, corresponding to positive- and negative-sequence impedances to zero.
2. Check if it is the time to obtain samples of voltages and currents. If so, proceed to Step 3. Otherwise, wait for the next samples.
3. Sample and quantize phase voltages and currents at R_x and R_y.
4. Calculate the 60 Hz voltage and current phasors using the LES filters described in Section 3.5.1.
5. Calculate the positive- and negative-sequence phasors and store the sequence-phasors in the processor's memory.
6. Compare the most recent voltage and current samples with the voltage and current samples from one cycle before. If the change is greater than a pre- defined threshold, V_CHANGE for voltage and C_CHANGE for current, then increase TRIGGER by one, else decrease TRIGGER by one if it is not zero.

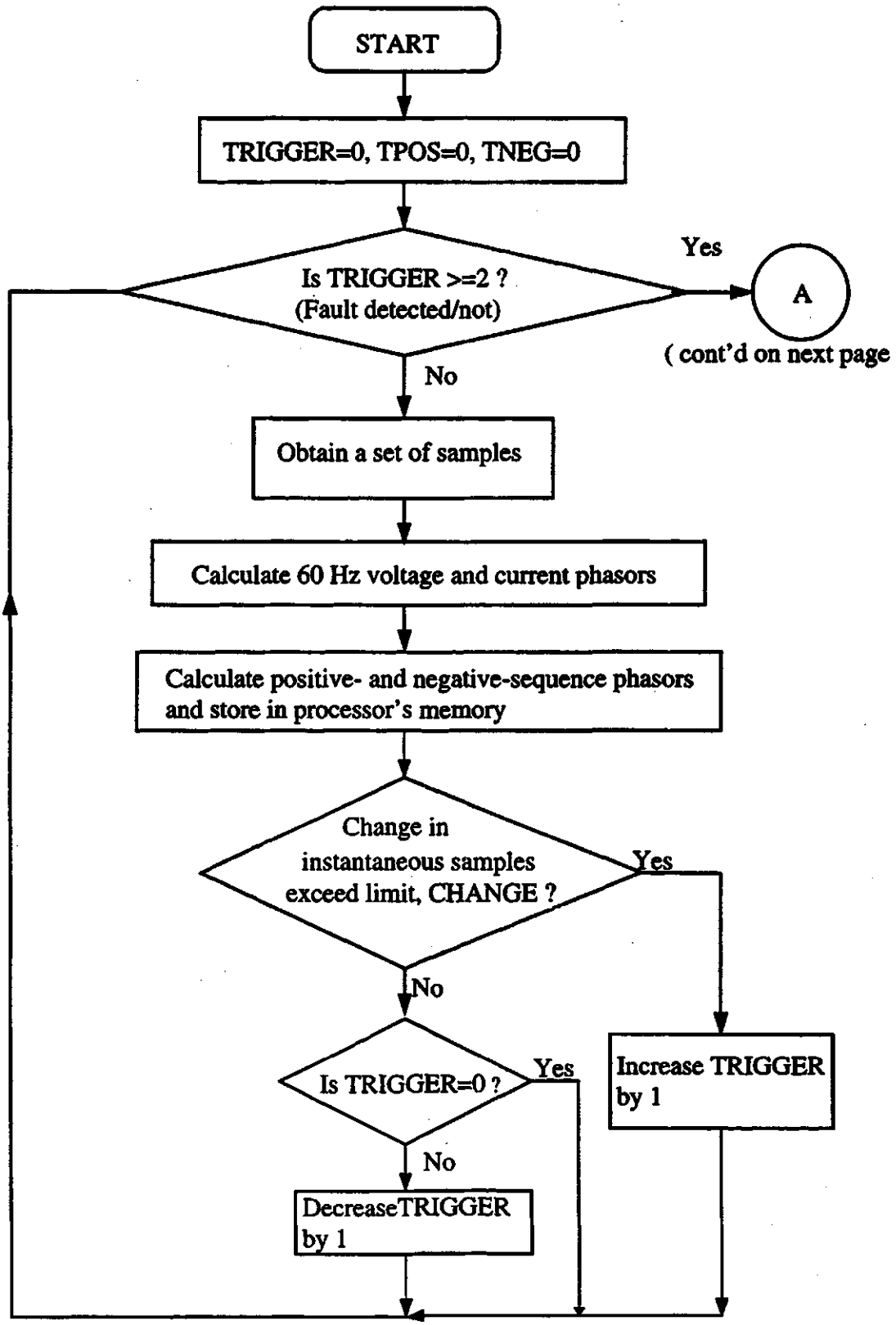


Figure 3.12. Flow chart of proposed algorithm (pre-fault section).

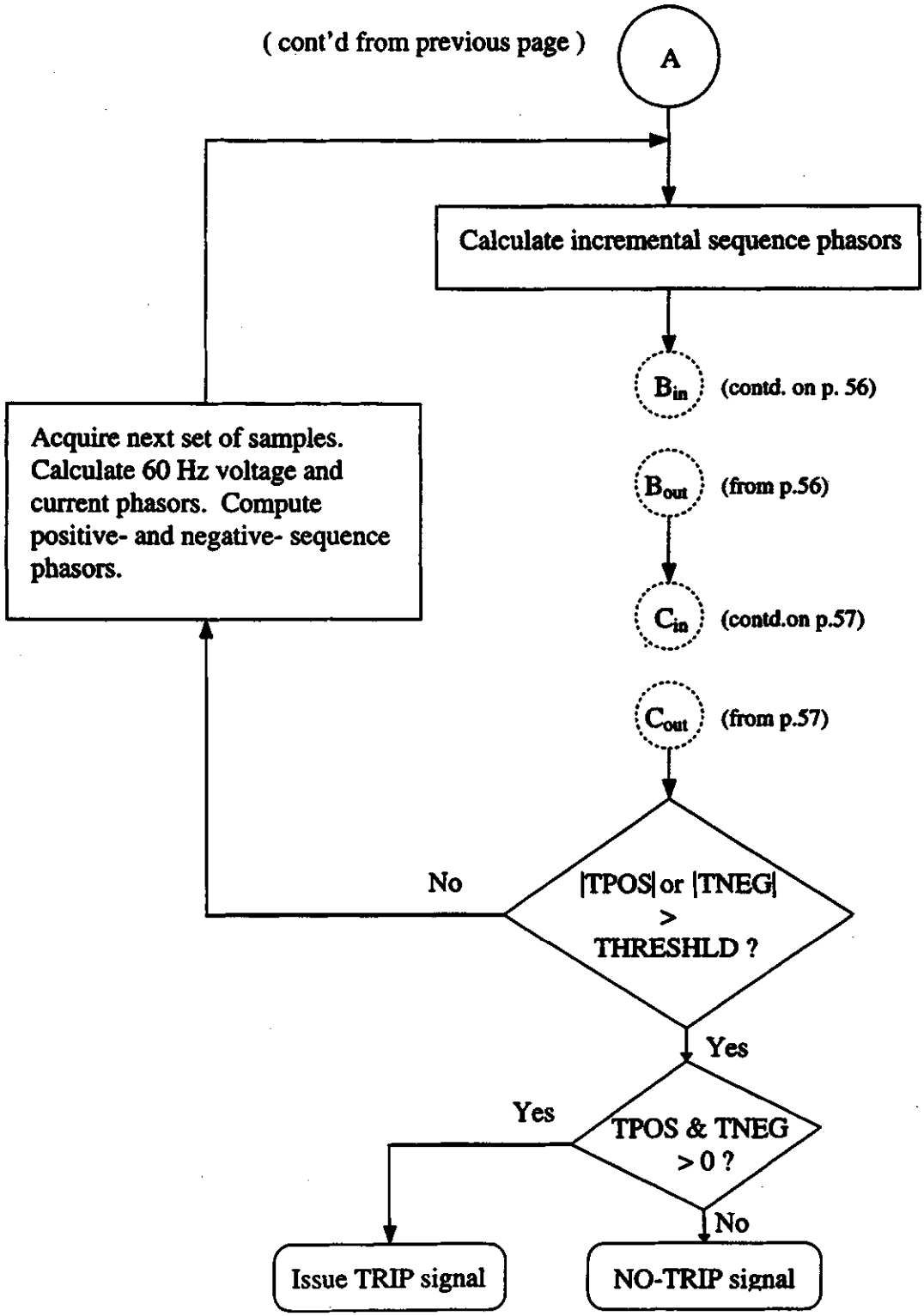


Figure 3.12 (contd.). Flow chart of proposed algorithm (fault section).

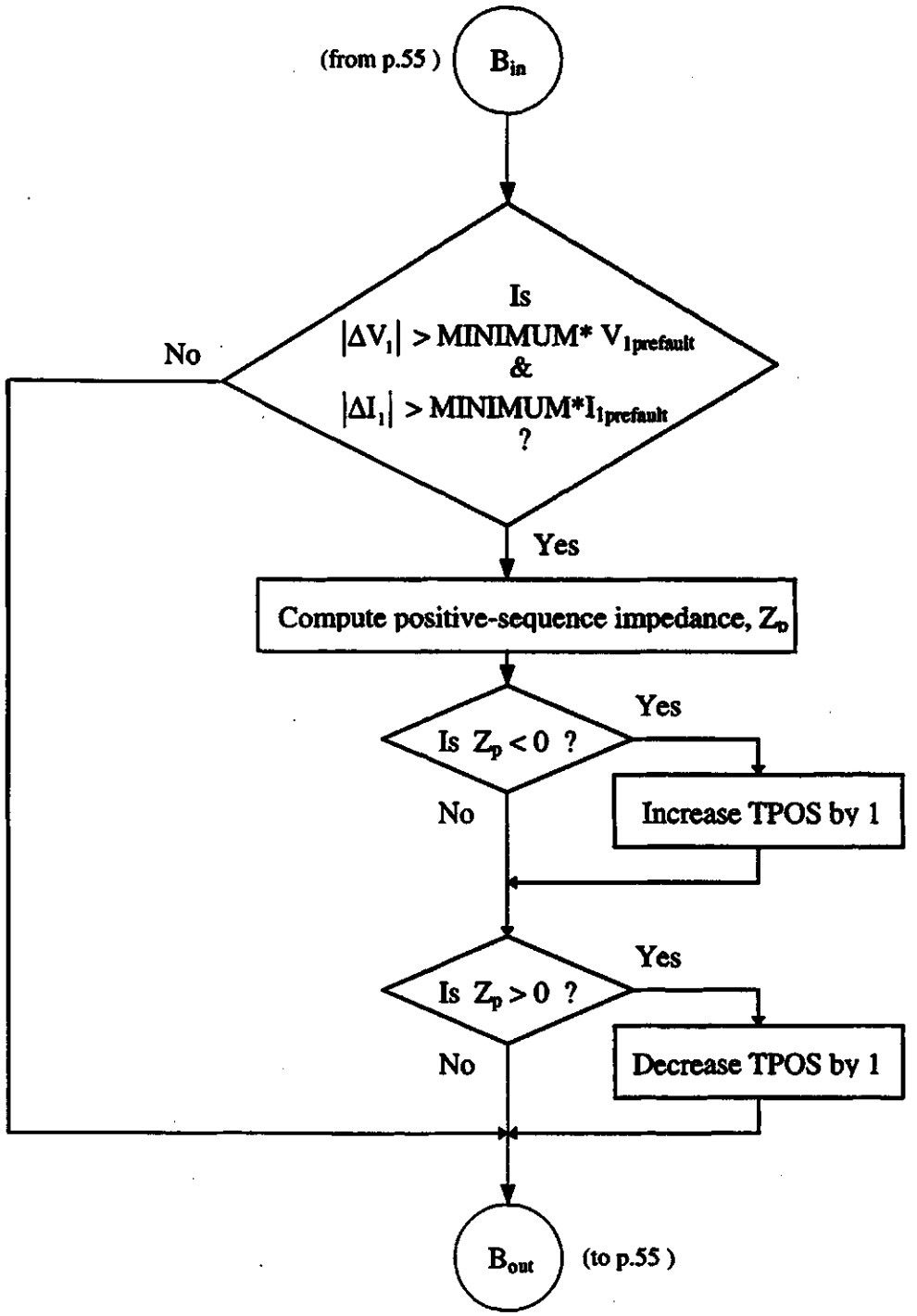


Figure 3.12 (contd). Segment to check threshold for positive-sequence voltage and current.

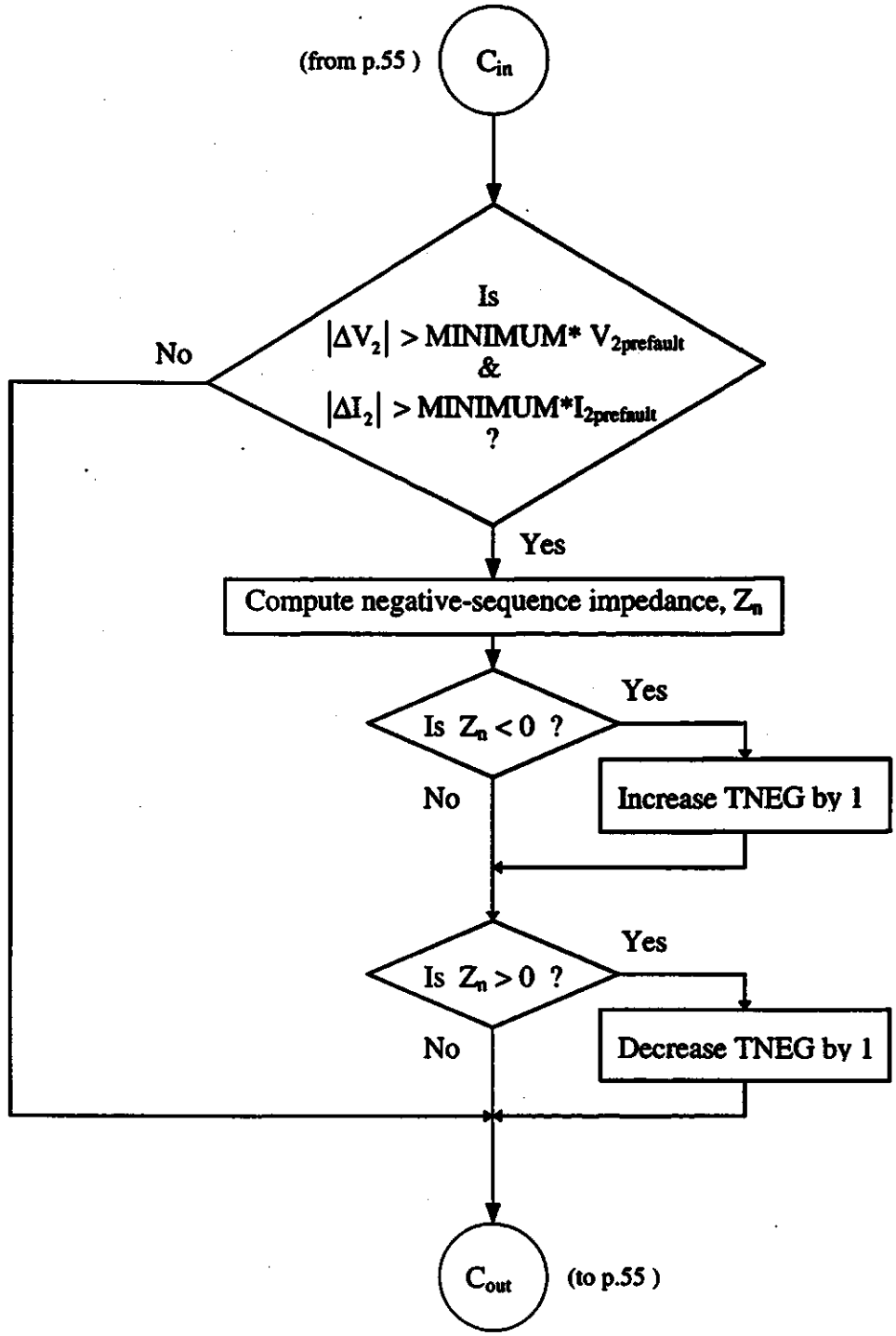


Figure 3.12 (contd). Segment to check threshold for negative-sequence voltage and current.

7. Check if the trigger indicator, TRIGGER, has been set to two. If so, proceed to Step 8, else revert to Step 2.

8. Compute the positive- and negative-sequence incremental voltages and currents using Equations 3.1 to 3.4 and 3.17 to 3.20 respectively.

9. Check if the magnitudes of the positive-sequence incremental-voltages and incremental-currents are greater than a predefined minimum value, MINIMUM, times the corresponding pre-fault values. If they are, compute the positive-sequence impedance, Z_p, seen by the relay, otherwise, proceed to Step 11.

10. Check if the positive-sequence impedance is in the third quadrant. If it is, increase the positive-sequence trip counter, TPOS, by one, otherwise decrease the trip counter by one.

11. Check if the magnitudes of the negative-sequence incremental-voltages and incremental-currents are greater than a predefined minimum value, MINIMUM, times the corresponding pre-fault values. If they are, compute the negative-sequence impedance value, Z_n, otherwise proceed to Step 13.

12. Check if the negative-sequence impedance is in the third quadrant. If it is, increase the negative-sequence trip counter, TNEG, by one, otherwise decrease the trip counter.

13. Check if the absolute value of either the positive-sequence trip counter or the negative-sequence trip counter has exceeded a pre-specified value, THRESHLD. If either counter has, proceed to Step 14, otherwise proceed to Step 15.

14. Issue a command to trip if the trip counter has exceeded the threshold and has a positive value, otherwise issue a no-trip command.

15. Revert to Step 2.

3.5.1. Design of the LES filter

In the work reported in this thesis, least error square filter was used to calculate phasors from quantized data. A sampling frequency of 1440 Hz., data window of 25 samples and time reference coinciding with the center of the data window were used. The filter coefficients were calculated and are listed in Table 3.1. These coefficients

Table 3.1. The filter coefficients for a 25 point LES filter based on a sampling rate of 1440 Hz.

Coefficient Number	Cosine Coefficients	Sine Coefficients
C[-12]	0.316490	-0.042553
C[-11]	-0.021568	-0.078721
C[-10]	-0.041667	-0.073942
C[-9]	-0.058926	-0.057153
C[-8]	-0.072169	-0.043440
C[-7]	-0.080494	-0.019795
C[-6]	-0.083333	-0.001773
C[-5]	-0.080494	0.023341
C[-4]	-0.072169	0.039894
C[-3]	-0.058926	0.060699
C[-2]	-0.041667	0.070396
C[-1]	-0.021568	0.082267
C[0]	0.000000	0.081560
C[1]	0.021568	0.082267
C[2]	0.041667	0.070396
C[3]	0.058926	0.060699
C[4]	0.072169	0.039894
C[5]	0.080494	0.023341
C[6]	0.083333	-0.001773
C[7]	0.080494	-0.019795
C[8]	0.072169	-0.043440
C[9]	0.058926	-0.057153
C[10]	0.041667	-0.073942
C[11]	0.021568	-0.078721
C[12]	-0.316490	-0.042553

were used for estimating the real (cosine) and imaginary (sine) components of the fundamental frequency phasors. The real and imaginary components of the fundamental frequency voltage (and current) phasors were calculated by multiplying the coefficients with the quantized values of the voltage (and current) samples. The frequency response of the two filters are shown in Figure 3.13. This figure shows that the filters attenuate components of higher frequencies.

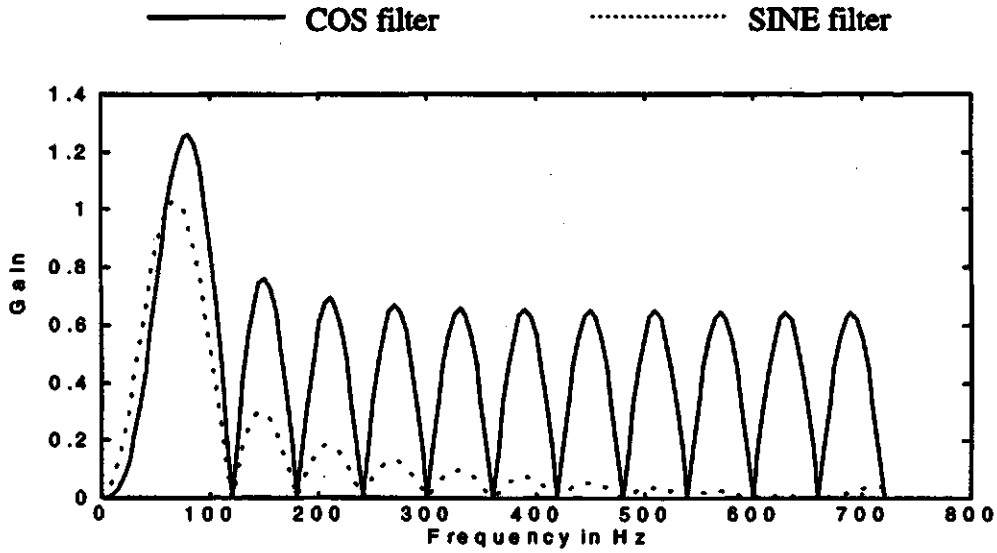


Figure 3.13. Frequency response of least error squares filter having a data window of 25 samples.

3.6. Switch-on transformers

A transformer is usually checked for its serviceability before switching-on but there is always a possibility that the transformer has a faulted winding or a bushing has failed. Also, if a transformer is connected to a line, or load, there is the possibility of there being a fault outside the transformer protection zone when the transformer is switched on. A check for the occurrence of these faults and their detection is, therefore, important.

It is shown in Chapter 2 that magnetizing inrush currents flow in the windings of a power transformer when it is energized. Fortunately, the voltage ratio of the primary voltage and secondary voltage is not affected. The presence of a fault in the transformer protection zone or outside the transformer protection zone is always accompanied with significant change in this ratio. The detection of the magnetizing inrush and presence of a fault on energizing a transformer is addressed in this section. Figure 3.14 is used to develop the detection algorithm.

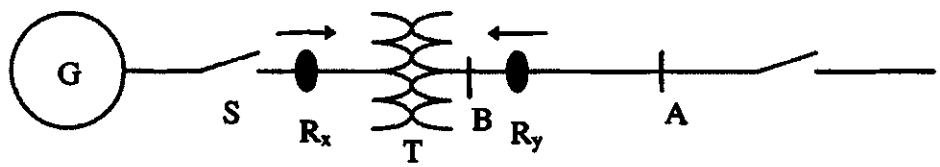


Figure 3.14. Switching-on of a power transformer.

3.6.1. External fault

Consider a network whose positive-sequence pre-fault and fault networks are shown in Figure 3.15 for occurrence of an external fault at A. Using the procedure similar to that described in Section 3.2.1, the incremental positive-sequence voltage at R_x can be expressed by

$$\Delta V_{1x} = +(Z_{s1} + Z_f)\,\Delta I_{1x}\,. \tag{3.53}$$

The positive-sequence impedance seen by the relay R_x is given as

$$\frac{\Delta V_{1x}}{\Delta I_{1x}} = Z_{s1} + Z_f\,. \tag{3.54}$$

Similarly, the incremental positive-sequence voltage at R_y is given by

$$\Delta V_{1y} = -(Z_f)\,\Delta I_{1y}\,. \tag{3.55}$$

The positive-sequence impedance seen by the relay R_y is given by

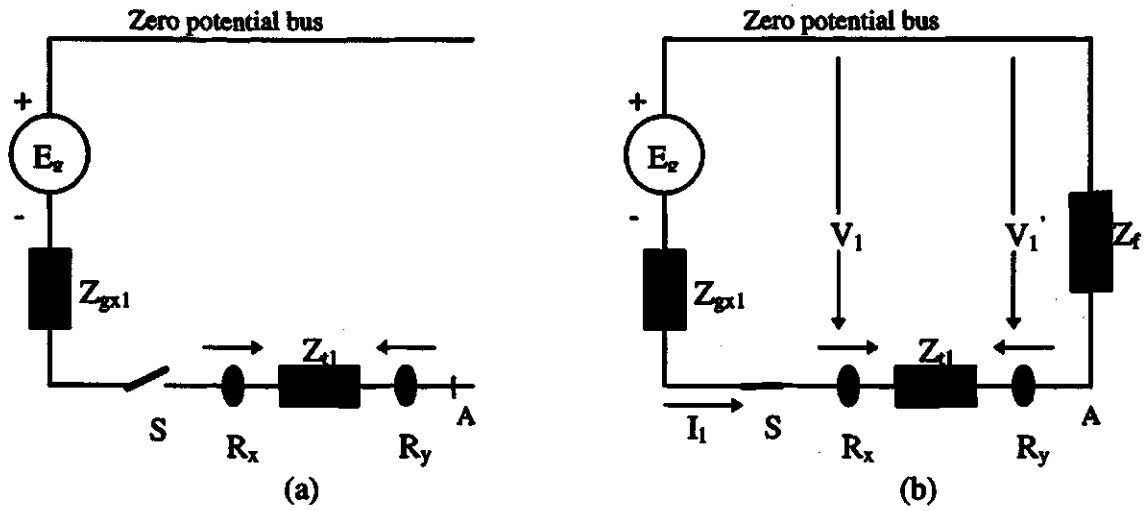


Figure 3.15. Positive-sequence networks for occurrence of an external fault at A (a) Pre-fault and (b) fault.

$$\frac{\Delta V_{1y}}{\Delta I_{1y}} = -Z_f . \tag{3.56}$$

The negative-sequence networks during pre-fault and fault conditions for occurrence of an external fault at A are given in Figures 3.16 (a) and (b) respectively.

The incremental negative-sequence voltage at R_x as a function of current and system parameters is given by

$$\Delta V_{2x} = -(Z_{gx2})\ \Delta I_{2x} . \tag{3.57}$$

The negative-sequence impedance seen by the relay R_x is given as

$$\frac{\Delta V_{2x}}{\Delta I_{2x}} = -Z_{gx2}. \tag{3.58}$$

Similarly, the incremental negative-sequence voltage at R_y is given by

$$\Delta V_{2y} = +(Z_{gx2} + Z_{t2})\ \Delta I_{2y} . \tag{3.59}$$

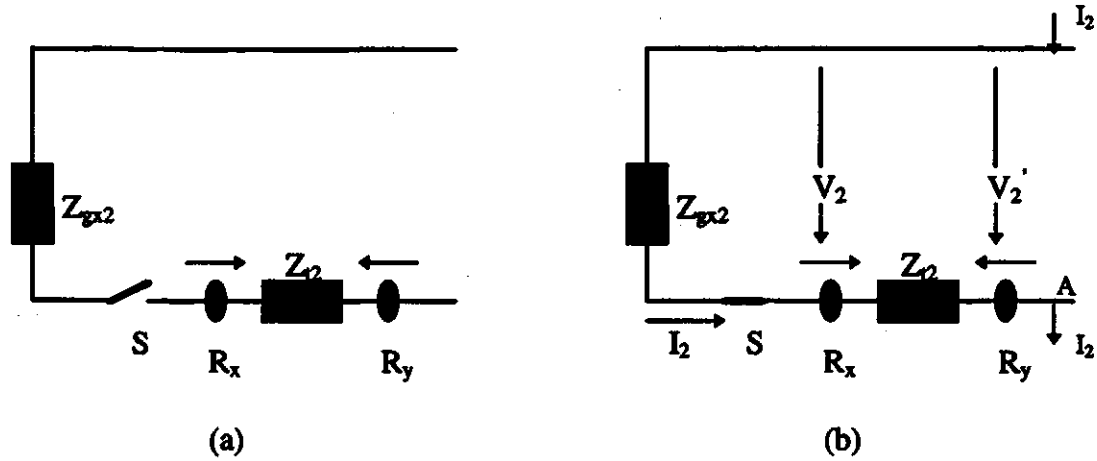


Figure 3.16. Negative-sequence networks for occurrence of an external fault at A (a) Pre-fault and (b) fault.

The negative-sequence impedance seen by the relay R_y is given as

$$\frac{\Delta V_{2y}}{\Delta I_{2y}} = +(Z_{gx2} + Z_{t2}) . \qquad (3.60)$$

3.6.2. Internal fault

For occurrence of a fault inside the transformer zone, the voltage ratio of all the phases is calculated using the respective phase voltage on primary and secondary sides of the transformer. These voltage ratios for different phases (A, B, C) are given by the following equations.

$$K_a = V_{A\,(secondary)} / V_{A\,(primary)} \qquad (3.61)$$

$$K_b = V_{B\,(secondary)} / V_{B\,(primary)} \qquad (3.62)$$

$$K_c = V_{C\,(secondary)} / V_{C\,(primary)} \qquad (3.63)$$

3.7. Fault-detection

Inspection of Equations 3.10, 3.16, 3.26, 3.32, 3.34, 3.36, 3.39 and 3.40 corresponding to the system model shown in Figure 3.1, leads to following observations:

The value of impedance seen by the relays R_x and R_y lies in the third quadrant of the impedance diagram for a fault in the protection zone of the transformer. For a fault outside the protection zone of the transformer, the impedance seen by one relay lies in the first quadrant and the impedance seen by second relay lies in the third quadrant. Thus, faults outside the protection zone of the transformer can be distinguished from those inside the protection zone by checking the quadrant in which the impedances seen by the two relays lie.

Figure 3.17 depicts the zones of fault-detection in the impedance plane for faults occurring inside and outside the protection zone. Both relays see impedance values in the third quadrant, shown in Figure 3.17(a), for faults occurring inside the protection zone. Figure 3.17(b) shows the regions of impedance values, seen by the relays, for faults occurring outside the protection zone of the transformer.

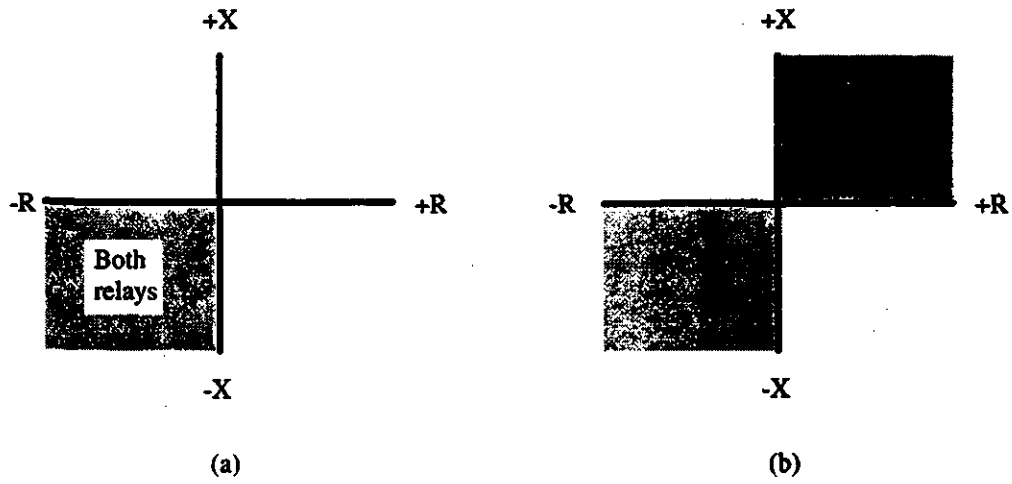


Figure 3.17. Fault-detection characteristics for a loaded transformer (a) Internal fault (b) External fault.

Inspection of Equation 3.42, 3.44, 3.46, 3.48, 3.50 and 3.52 corresponding to the system model for an unloaded transformer, shown in Figure 3.6, leads to the following observations:

The impedance seen by the relays R_x and R_y lies in third and first quadrants respectively for a fault outside the protection zone (at A) of the unloaded transformer. For a fault inside the transformer protection zone, the impedance seen by the relay R_x lies in the third quadrant. In this case, the relay R_y does not compute any impedance because the transformer is not supplying any load. Figures 3.18 (a) and (b) shows the fault-detection characteristics for faults occurring inside and outside the protection zone of the transformer.

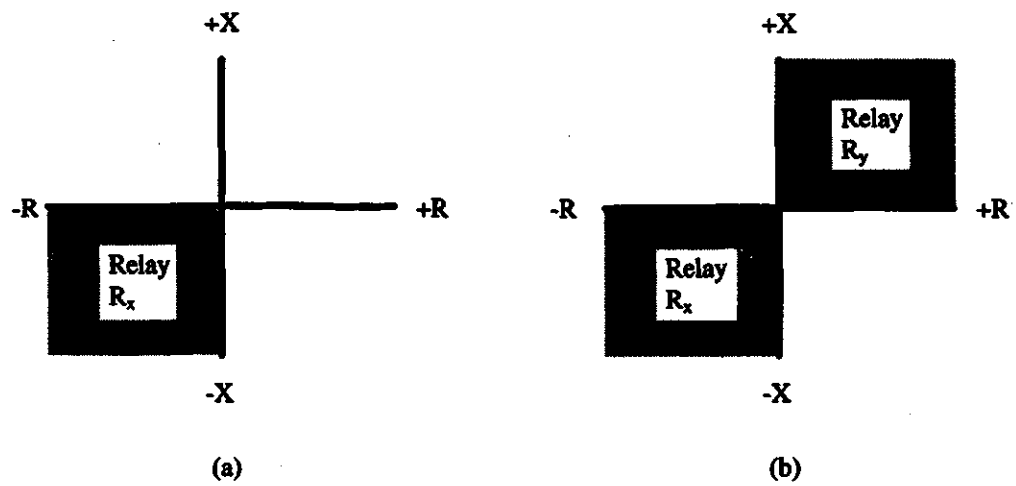


Figure 3.18. Fault-detection characteristics for an unloaded transformer (a) Internal fault (b) External fault.

The fact, that the presence of a fault inside or outside the transformer protection zone is always accompanied with significant changes in the voltage ratio(s) of the primary voltage and secondary voltage, is used by the algorithm of Section 3.6 for distinguishing phenomenon of magnetizing inrush from the switch-on faults, inside and outside the protection zone of the transformer.

The positive-sequence impedance seen by the relay R_x lies in the first quadrant of the impedance diagram for a fault outside the transformer protection zone. On the other hand, the positive-sequence impedance seen by the relay R_y lies in the third quadrant of the impedance diagram for these faults. For a fault inside the transformer protection zone,

one of the voltage ratios defined by Equations 3.61 to 3.63 is disturbed significantly such that it decreases below the pre-defined threshold, THRSWF.

i.e. One of K_a or K_b or K_c < THRSWF.

The phenomenon of magnetizing inrush is detected by the voltage ratios of all phases being above the THRSWF.

i.e. K_a > THRSWF, K_b > THRSWF and K_c > THRSWF.

Figures 3.19 (a) and (b) shows the fault-detection characteristics for switch-on faults occurring inside and outside the transformer protection zone respectively.

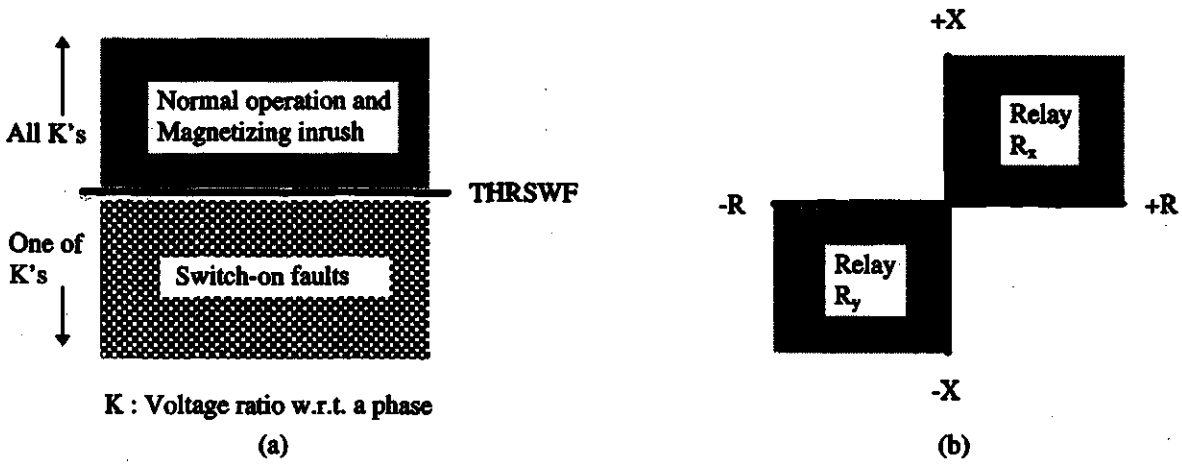


Figure 3.19. Switch-on fault-detection characteristics (a) Internal fault (b) External fault.

The algorithms developed in Sections 3.2, 3.3 and 3.6 are used together to protect the transformer. The process of linking these algorithms in described in the next section.

3.8. Linking the proposed algorithms

The algorithms developed in Sections 3.2, 3.3 and 3.6 are used together to carry out the transformer protection in different operating conditions. Figure 3.20 shows the flow-chart that can be used for linking the developed algorithms. The change-over among different algorithms is carried out as follows.

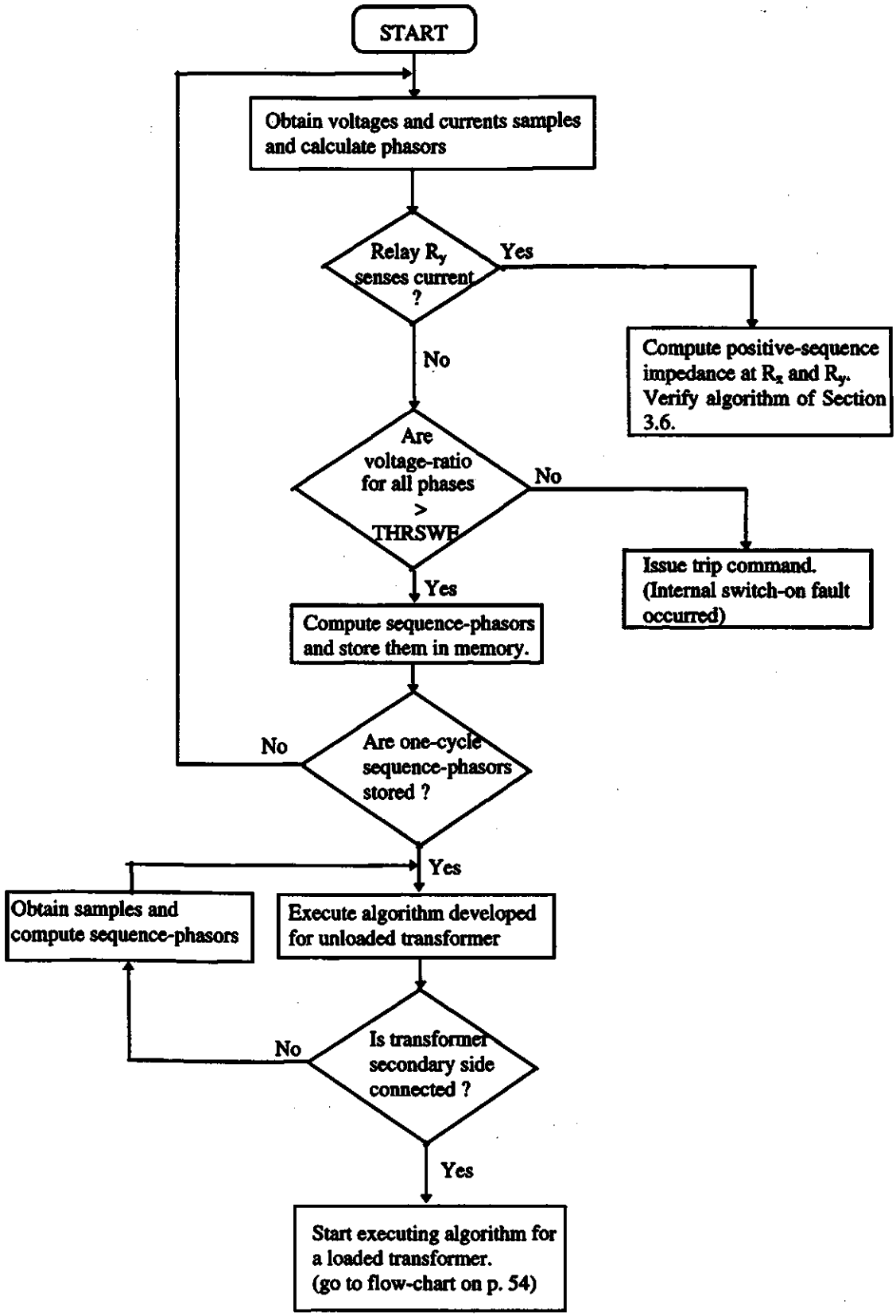


Figure 3.20. Flow-chart for combining the developed algorithms.

1. The algorithm developed for detecting switch-on faults is used when the transformer is energized from a source. This algorithm is continuously executed until two cycles and a sample to check if a switch-on fault has occured. The occurrence of switch-on fault, if any, is detected using this algorithm.

2. After two cycles and a sample, the execution logic shifts to the algorithm developed for a unloaded transformer. This will be used until the transformer is connected on the secondary side.

3. When the transformer is loaded, the algorithm developed in Section 3.2 is used. This will continuously monitor the transformer operation and detect the occurrences of faults inside and outside the protection zone of the transformer.

3.9. Current transformer saturation

The performance of a protection scheme is adversely affected by ct saturation. Algorithms proposed for protection in the past use special circuits to detect ct saturation and delay the operation of relays to avoid incorrect operations. The effect of ct saturation on the proposed technique can be explained by using the correlation technique used commonly for estimating phasors. The correlation technique estimates real and imaginary components of the phasor by correlating the waveform of the signal with full-cycle sine and cosine waveforms. The following two situations can be compared to evaluate the impact of ct saturation.

(i) The waveform is normal.
(ii) A ct is saturated and quantized values of several samples are much smaller than their normal values.

The waveforms, quantized samples (12 per cycle), and the computed values of the real and imaginary components of the phasors and the angles of the phasors are shown in Figures 3.21 (a) to (l). The real and imaginary components are computed by correlating

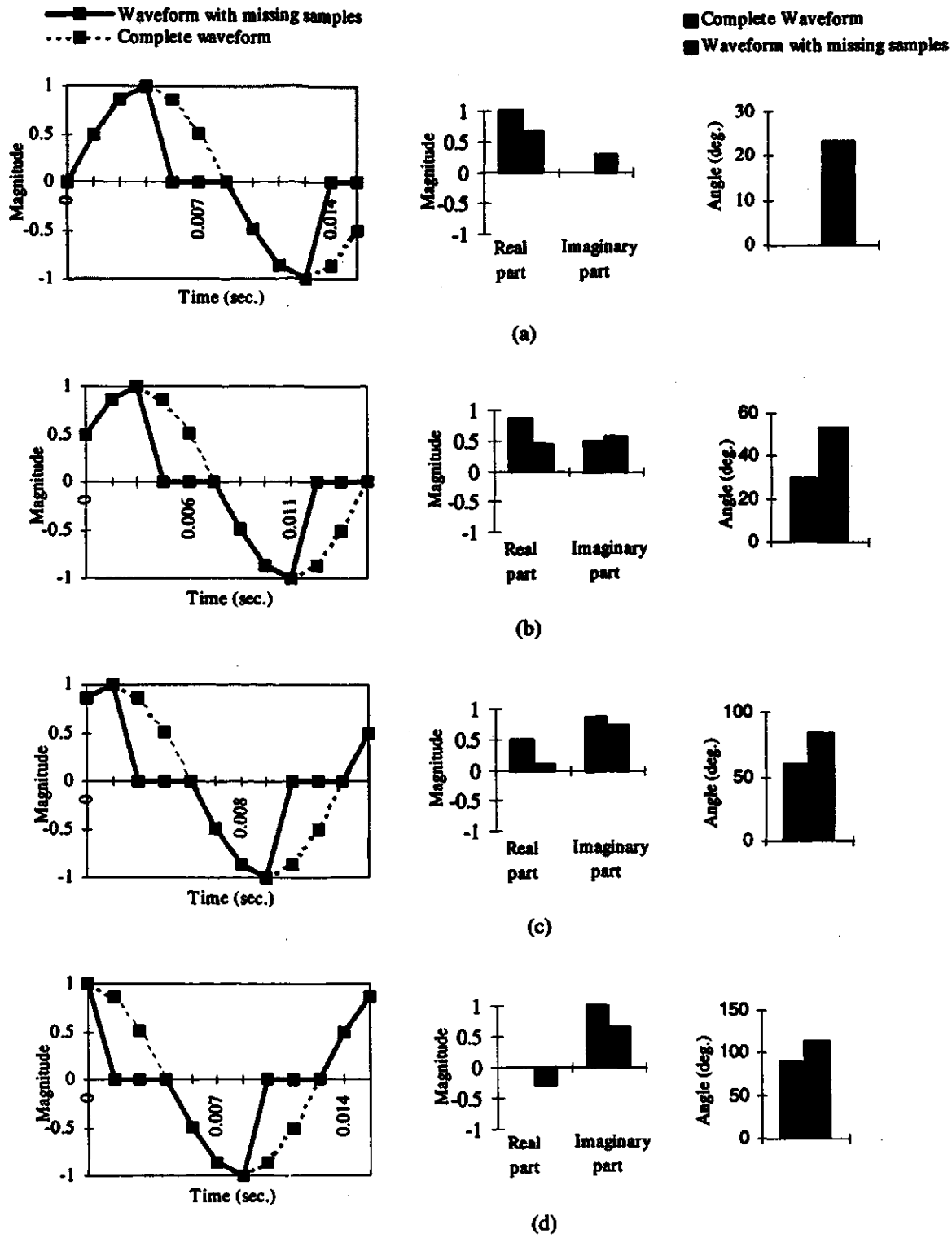


Figure 3.21. Correlation of complete current waveform(unsaturated ct) and waveform with samples of low value (saturated ct) with full-cycle Sine and Cosine waveforms - Waveform configurations, Magnitudes of Phasors' Real and Imaginary components & Phasor angle - at different instants of data window (a) 0^0 (b) 30^0 (c) 60^0 (d) 90^0 w.r.t. Sine and Cosine waveforms.

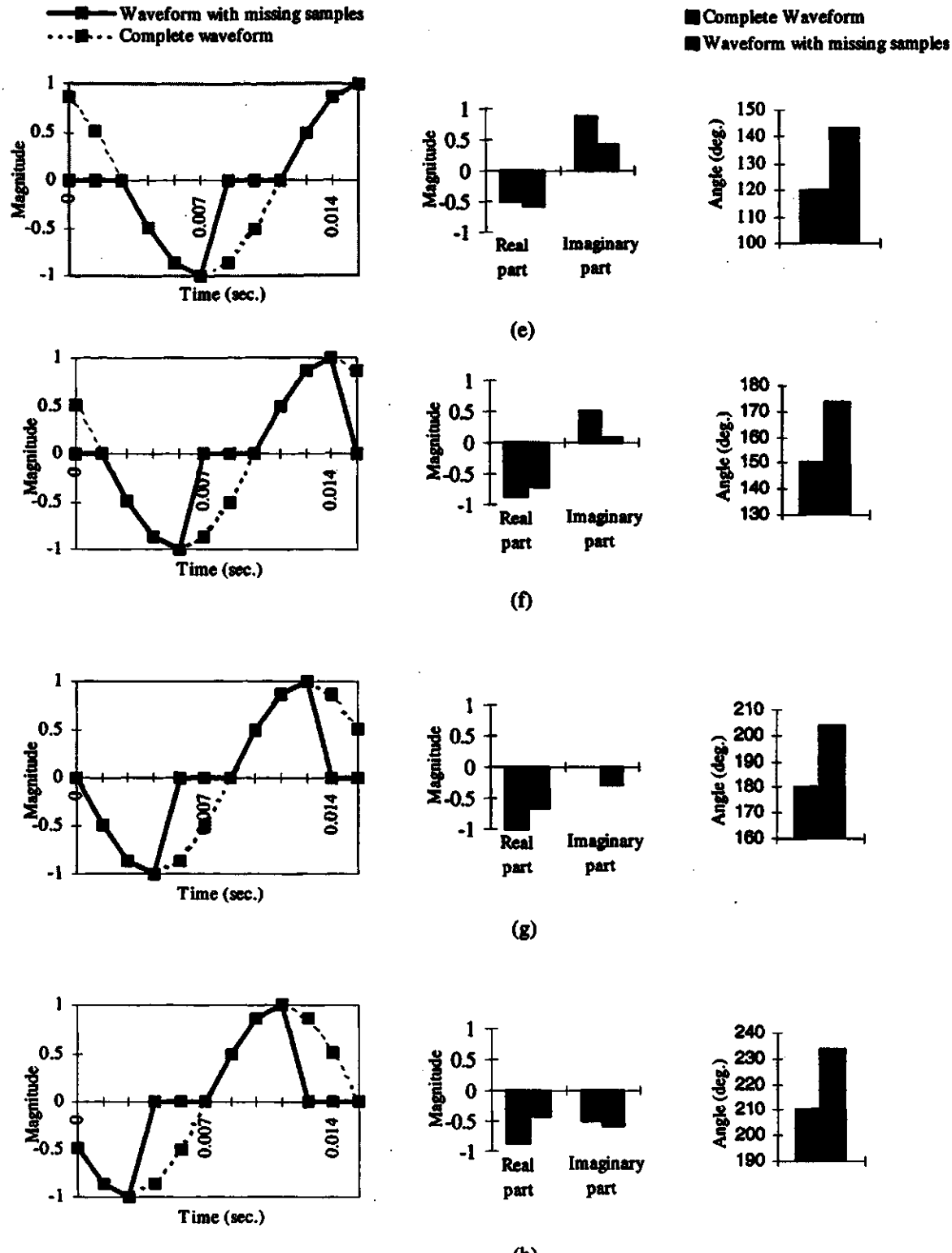


Figure 3.21. Correlation of complete current waveform(unsaturated ct) and waveform with samples of low value (saturated ct) with full-cycle Sine and Cosine waveforms - Waveform configurations, Magnitudes of Phasors' Real and Imaginary components & Phasor angle - at different instants of data window (e)12 0^0 (f) 150^0 (g) 180^0 (h) 210^0 w.r.t. Sine and Cosine waveforms.

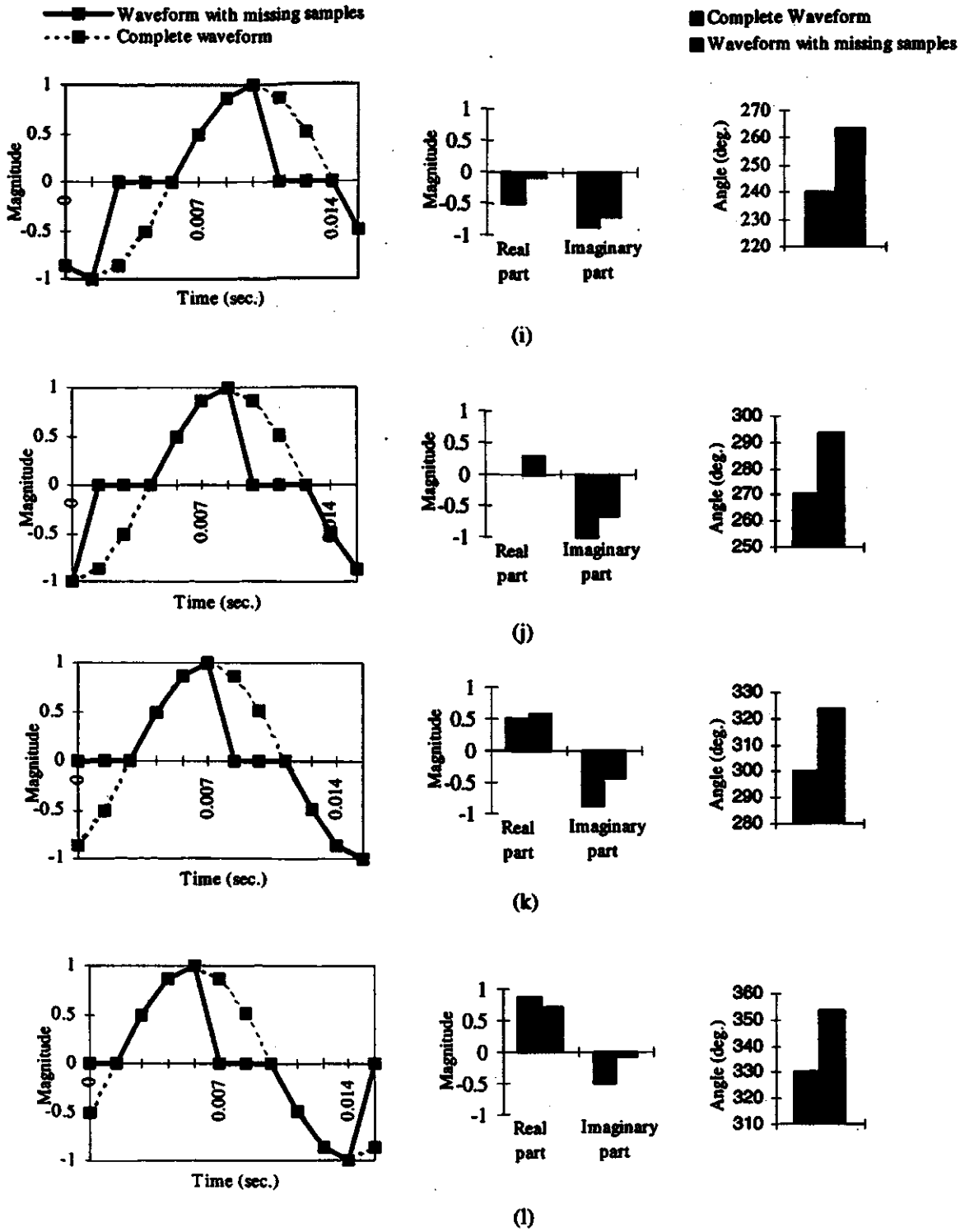
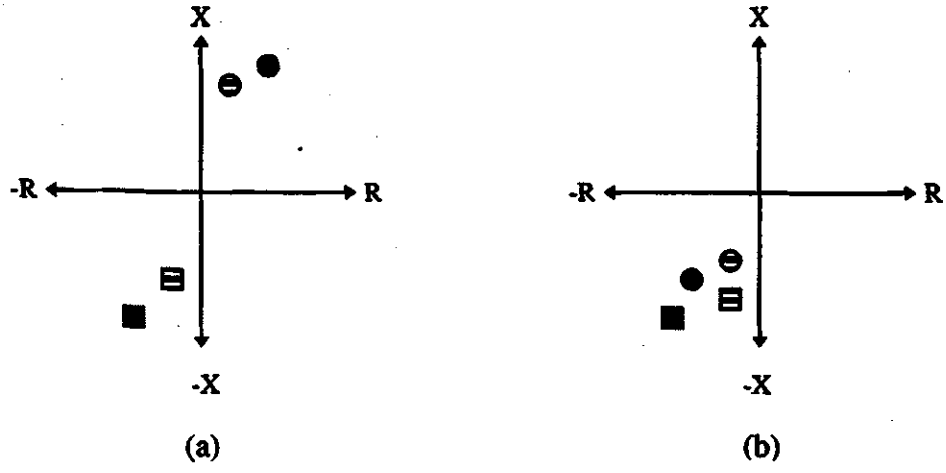


Figure 3.21. Correlation of complete current waveform(unsaturated ct) and waveform with samples of low value (saturated ct) with full-cycle Sine and Cosine waveforms -Waveform configurations, Magnitudes of Phasors' Real and Imaginary components & Phasor angle -at different instants of data window (i)240^0 (j)270^0 (k) 300^0 (l) 330^0 w.r.t. Sine and Cosine waveforms.

the outputs of the ct with full-cycle sine and cosine waveforms, and the phasor angles are calculated from the real component and imaginary component.

A perusal of Figures 3.21 (a) to (l) reveals that the magnitudes of the real and imaginary components of the current phasor are different for the normal and missing-sample waveforms. However, the phase angle calculated from the missing-sample waveform is always greater than the phase angle calculated from the normal waveform. This remains true as the data window is advanced one sample at a time for the duration of one cycle. An increase in the phase angle of the current phasor and a decrease in its magnitude results in a decrease in the phase angle of the computed impedance and an increase in its magnitude since impedance is inversely proportional to the current.

Figure 3.22 shows the impedances calculated by the relays R_x and R_y. It shows the impedance for faults occurring inside and outside the protection zone. It can be seen that the saturated impedance values are higher than the unsaturated impedance values and they lie well within the fault-detection zone.



Legend

ct condition	Relay R_x	Relay R_y
unsaturated	⊖	⊟
saturated	●	■

Figure 3.22. Effect of ct saturation on impedance seen by relays.

3.10. CT ratio-mismatch

Mismatch of ct ratios in conventional differential protection scheme can result in operating currents and cause misoperation of the relay. The ct ratios used in the differential scheme are, therefore, properly matched so that no current flows in the operating element of the differential relay during normal operation and external faults. However, ct ratios are very difficult to match exactly.

The proposed technique calculates the impedance angle using the voltage and current samples taken at the primary and secondary terminals of the transformer. The calculations performed using these data are independent of each other. The relay makes the decision from the quadrant(s) in which the impedances lie. The decision is independent of the calculations of the magnitude of the current which is adversely affected by ct saturation and ct ratio errors.

3.11. Features of the proposed technique

The proposed technique has some remarkable features which are enumerated below.

(a) The proposed technique calculates the sequence impedances and decides if the fault is in the protected zone from the quadrant in which the impedance lies. The calculations do not require the parameters of the transformer or the power system.

(b) The calculations are done independently from the currents and voltages observed on each sides of the power transformer. This eliminates the need to match the ratios of the cts.

(c) The proposed technique works well even if the cts are saturated.

3.12. Summary

A technique for protecting power transformers has been presented in this chapter. The technique uses samples of the three-phase voltages and currents taken at the terminals of the power transformer. These samples are used to compute positive- and negative-sequence voltage and current phasors which, in turn, are used to identify faults in the protection-zone of the transformer. A theoretical basis, for the technique to provide correct decisions under current transformer saturation, is also presented. The application of the proposed technique for distinguishing faults in an unloaded transformer is included. An approach for checking switch-on faults has also been established.

The technique does not require the values of the parameters of the power transformer or the power system. Current transformer saturation and ratio mismatch do not affect the performance of the proposed technique.

4. SIMULATION STUDIES

4.1. Introduction

Details of the proposed technique for detecting internal and external faults in power transformers are presented in Chapter 3. Fault-detection characteristics of the relay are also shown in that chapter. Fault data were generated by simulations using an electromagnetic transient program, EMTDC [26]. The data were used to verify the validity of the proposed technique. The impacts of ct saturation and ratio-mismatch were also evaluated. This chapter describes the procedures used in the simulation studies. The response of the proposed technique to the simulated data, obtained from the simulations, are also included.

4.2. System modeling and data processing

The data for testing the algorithm based on the proposed technique were generated on a Sun SPARC workstation using the electromagnetic transient program, EMTDC. Model of a power system shown in Figure 4.1 was selected for generating fault data. In the selected system, a transformer connects the equivalent sources, G_x , to a high-voltage transmission line which at the remote terminal is connected to the source G_y. Relays are located on the transformer terminals as shown in the figure. The ratings of the power transformer and the equivalent sources are also indicated in this figure. Various types of faults were applied at locations (1, 2, 3, 4 and 5 shown in Figure 4.1).

An overview of the EMTDC is given in Appendix B. The parameters of the system components of the model are given in Appendix C.

The fault data were generated from the simulations using calculation steps at 23040 Hz. High frequency sampling rate allows a reasonable approximation of the

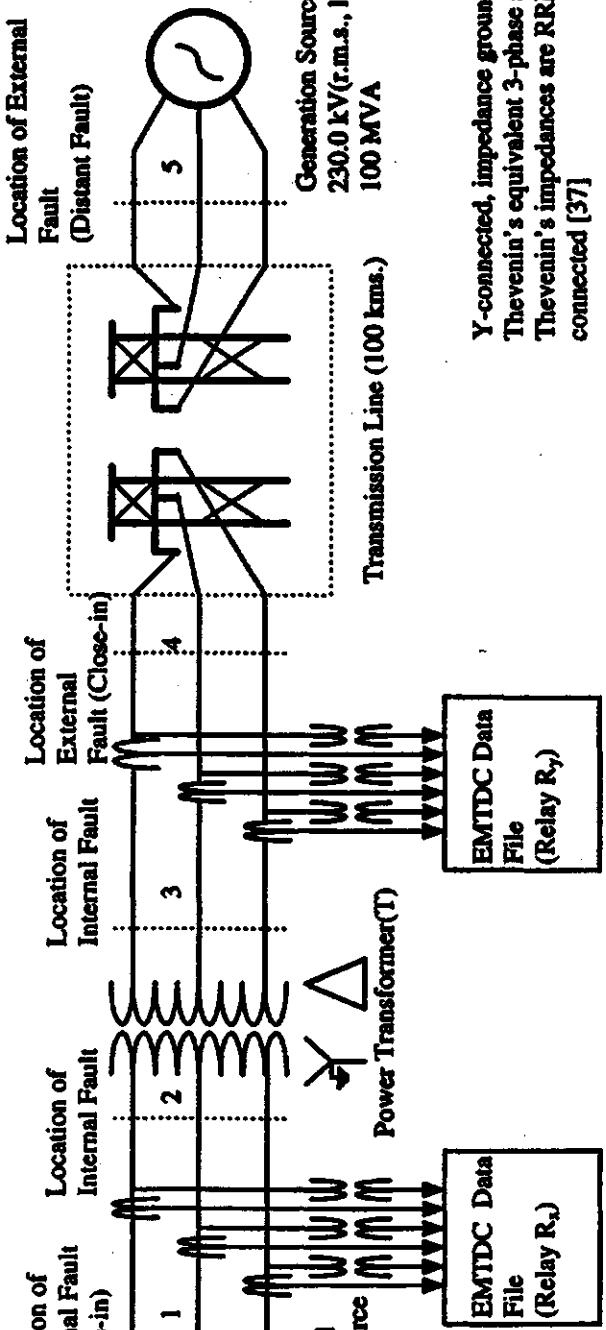


Figure 4.1. System model used for generating simulated data using EMTDC.

continuous-time domain signals. The output data from the EMTDC was then pre-processed using digital-equivalents of a 4th order Butterworth filters. The filters were implemented using the Matlab. The filtered data was re-sampled at 1440 Hz. Since the Nyquist criterion requires that all frequency components of 720 Hz and higher frequencies be suppressed to prevent aliasing, the cut-off frequency of 200 Hz was selected. Details of the anti-aliasing filter are given in Appendix D.

The least error squares (LES) algorithm was used for computing the phasors of the fundamental frequency components from sampled and quantized data. The LES filters were designed assuming that the samples are taken at 1440 Hz and a data window of 25 samples is used. An algorithm based on the proposed technique was implemented using a program written in ANSI C.

As stated in Chapter 3, a fault in a power transformer or in the system can be detected by comparing the recently quantized values of voltages and currents with those quantized one cycle earlier. The threshold values for the changes, V_CHANGE, and C_CHANGE, compared to changes observed one cycle earlier were set at 3.5% and 10% respectively. The value of MINIMUM, the minimum magnitude of positive- and negative-sequence incremental voltages and currents, was set at 1% of the pre-fault values respectively. To ensure algorithm sensitivity and maintain security against false trip decisions, the value of the trip counter THRESHLD was set at 12. The threshold, THRSWF, used in checking switch-on faults, was set at 0.8 times the nominal transformation ratio. Transformation ratios more than this limit were interpreted to represent healthy conditions and those less than this limit were interpreted to represent external or internal faults.

4.3. Test studies

Power system model shown in Figure 4.1 was simulated for generating data which was used to check the performance of the proposed technique. Different types of internal and external faults were simulated and the voltages and currents at the relay

locations were recorded in data files. The impacts of current transformer saturation and ratio-mismatch conditions were also studied. Some test results are presented in this section.

4.3.1. Internal faults

Internal faults were simulated at locations 2 and 3 shown in Figure 4.1. Some cases are presented in the following sections; additional cases are presented in Appendix E.

4.3.1.1. Single phase-to-ground fault : Phase A

A single phase-to-ground fault on phase A was simulated on the 230 kV side of the power transformer (location 3 shown in Figure 4.1). The unfiltered and filtered voltage and current waveforms are shown in Figures 4.2 and 4.3 respectively. The fault was applied at 0.3 s. Figure 4.4 shows the performance of the algorithm. The detection of the inception of the fault took the first two samples. After this delay, the positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of the sequence impedances (in polar form) are shown in Figures 4.4 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.4(c). For this case, the computed positive- and negative-sequence impedances indicate that the fault is in the protection zone of the transformer. The plots of the positive-sequence trip counters of the 13.8 kV and 230 kV sides reached the threshold (of 12) in 13 samples. The plots of the negative-sequence trip counters of the 13.8 kV and 230 kV sides also reached the threshold in 13 samples. At that time, the trip-logic confirmed the fault in the protection zone of the transformer. It took the algorithm 9 ms to make the final decision in this case.

4.3.1.2. Two-phase fault : Phase B - Phase C

A two-phase fault, involving phase B and phase C, was simulated on the 230 kV side of the power transformer (location 3 shown in Figure 4.1). The fault was applied at

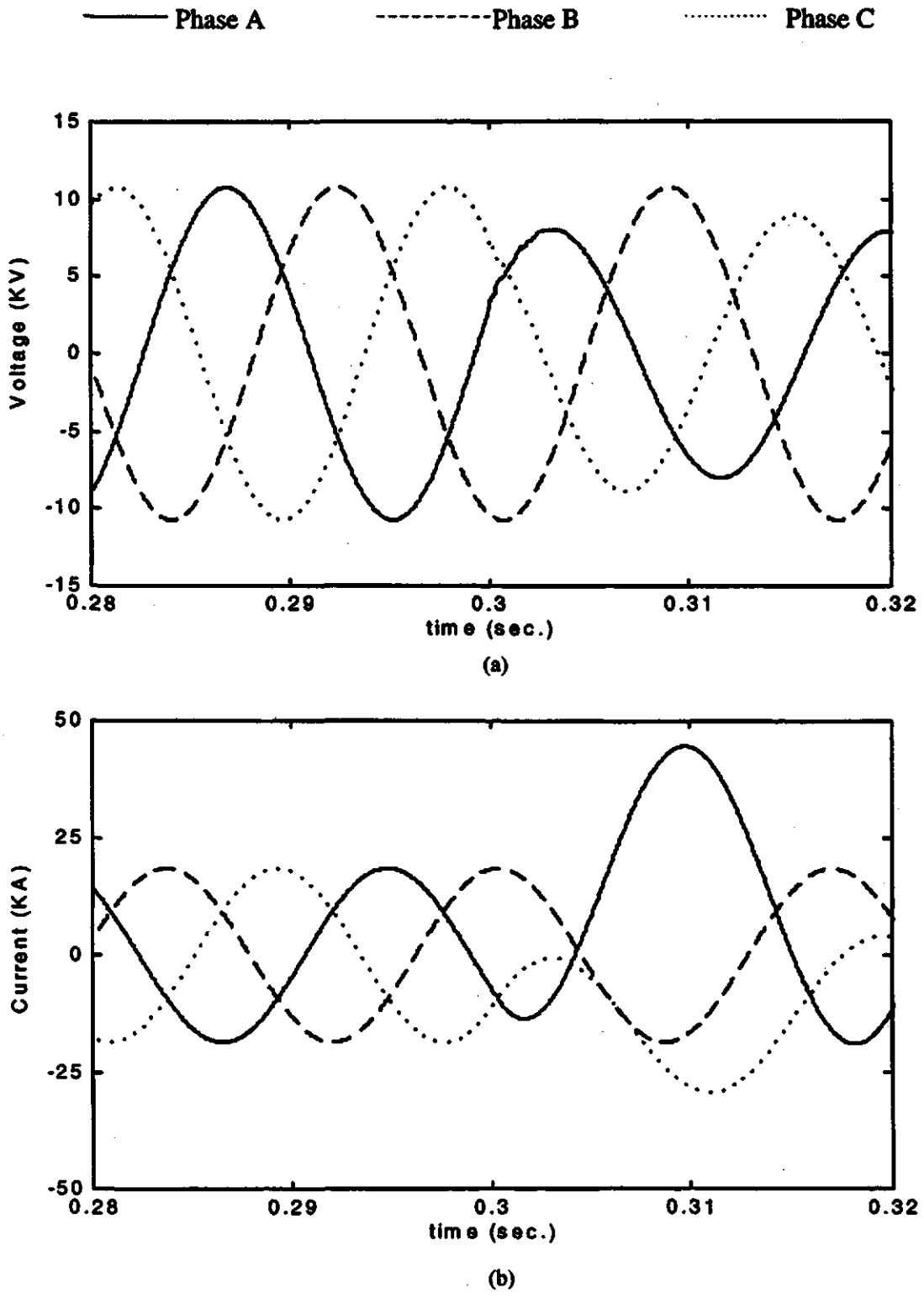
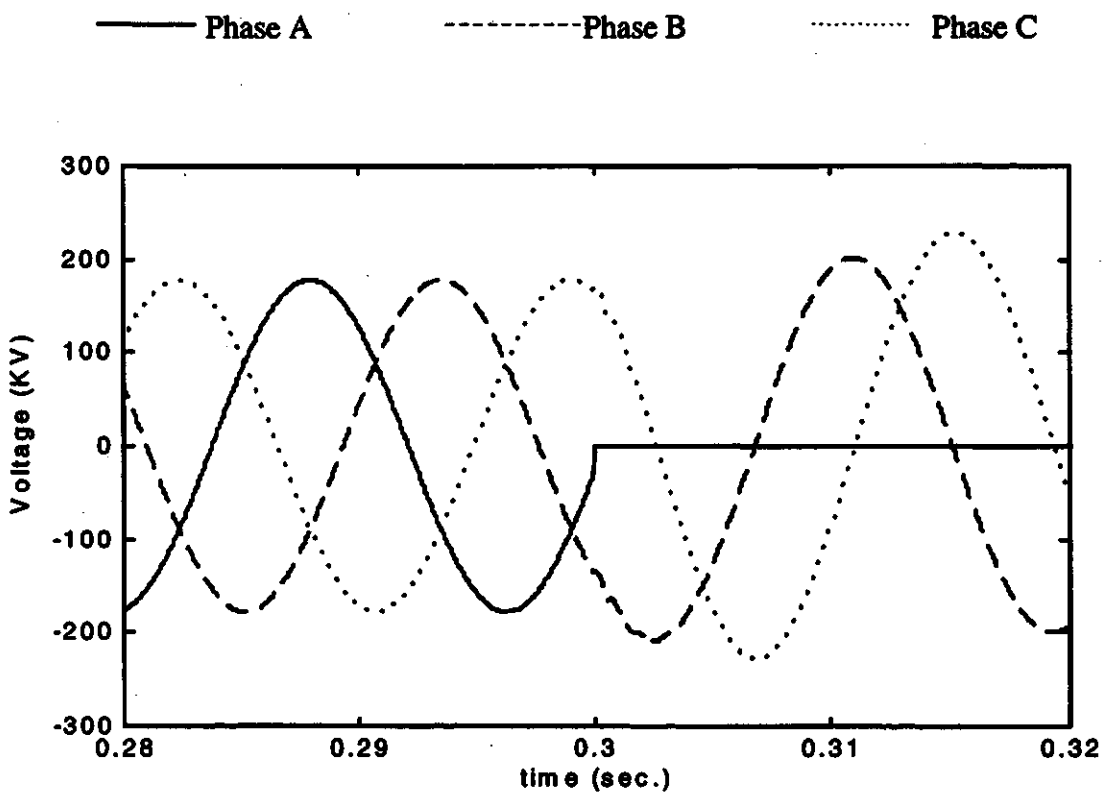
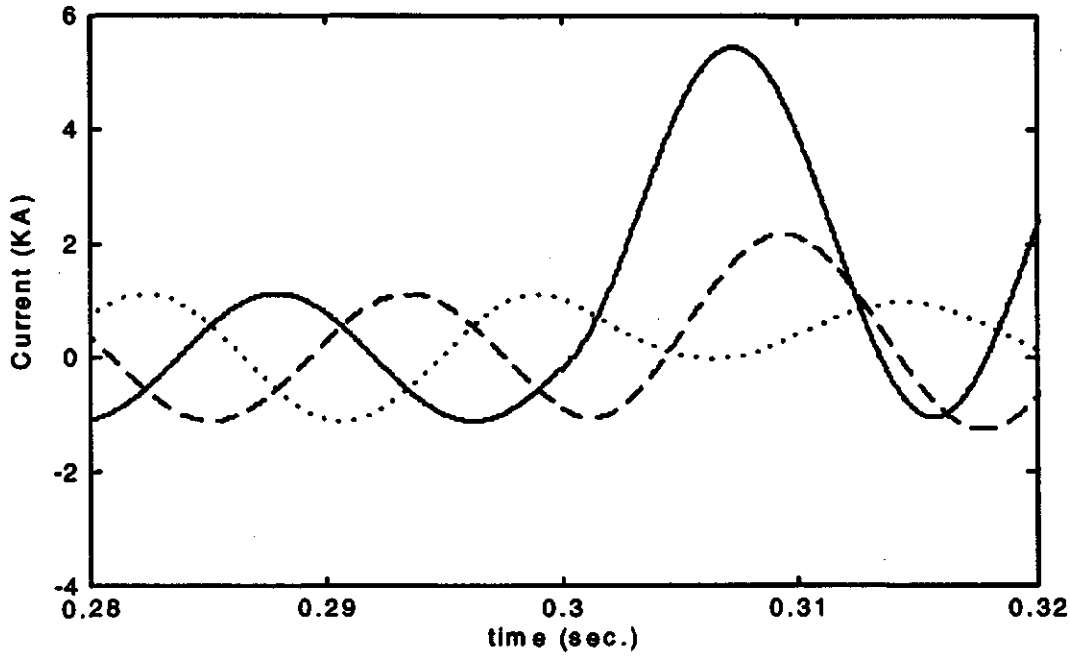


Figure 4.2. Plot of unfiltered (a) voltage and (b) current waveforms on the 13.8 kV side of power transformer for A-g internal fault in the 230 kV winding.



(c)



(d)

Figure 4.2(contd.). Plot of unfiltered (c) voltage and (d) current waveforms on the 230 kV side of power transformer for A-g internal fault in the 230 kV winding.

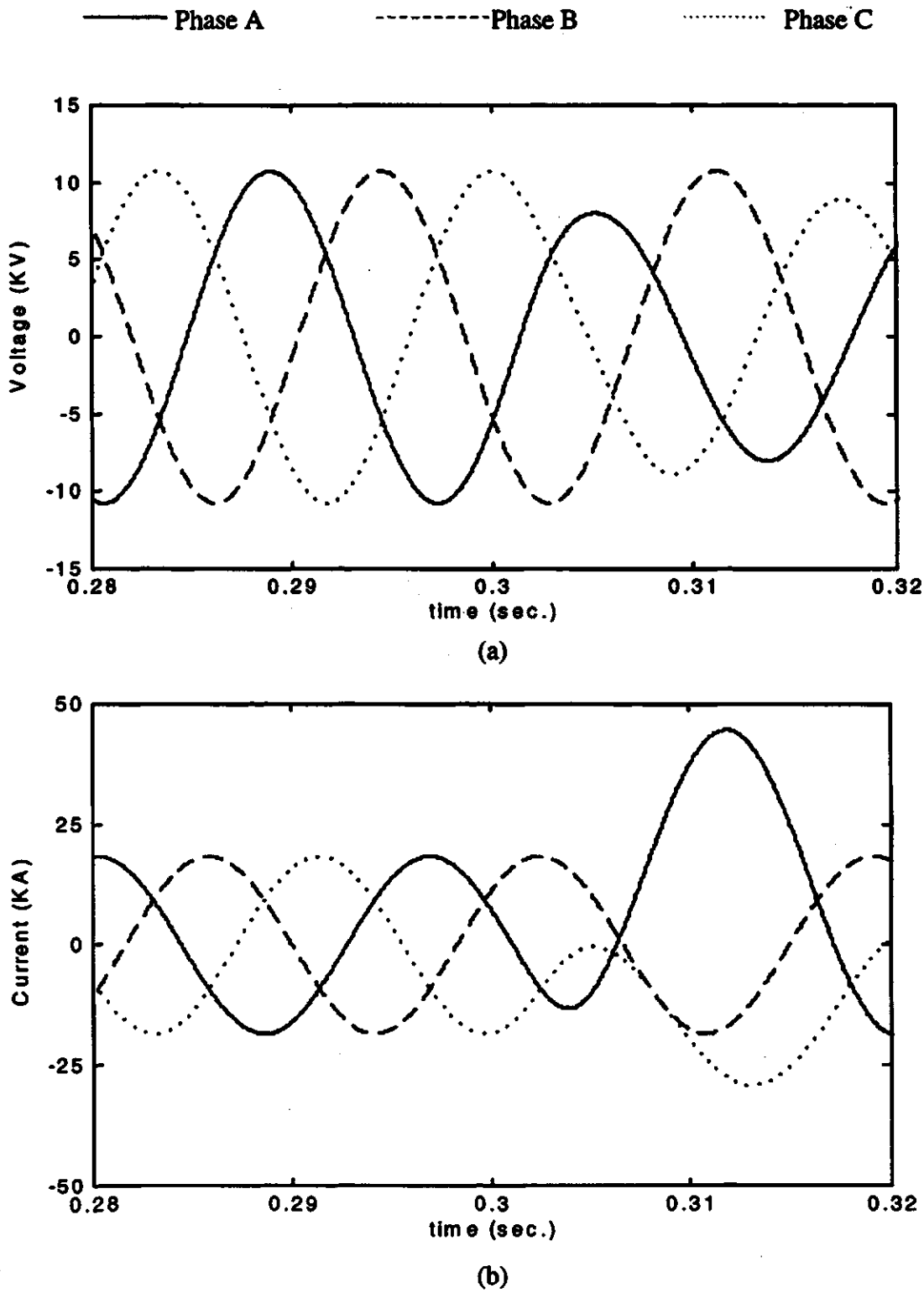


Figure 4.3. Plot of filtered (a) voltage and (b) current waveforms on the 13.8 kV side of power transformer for A-g internal fault in the 230 kV winding.

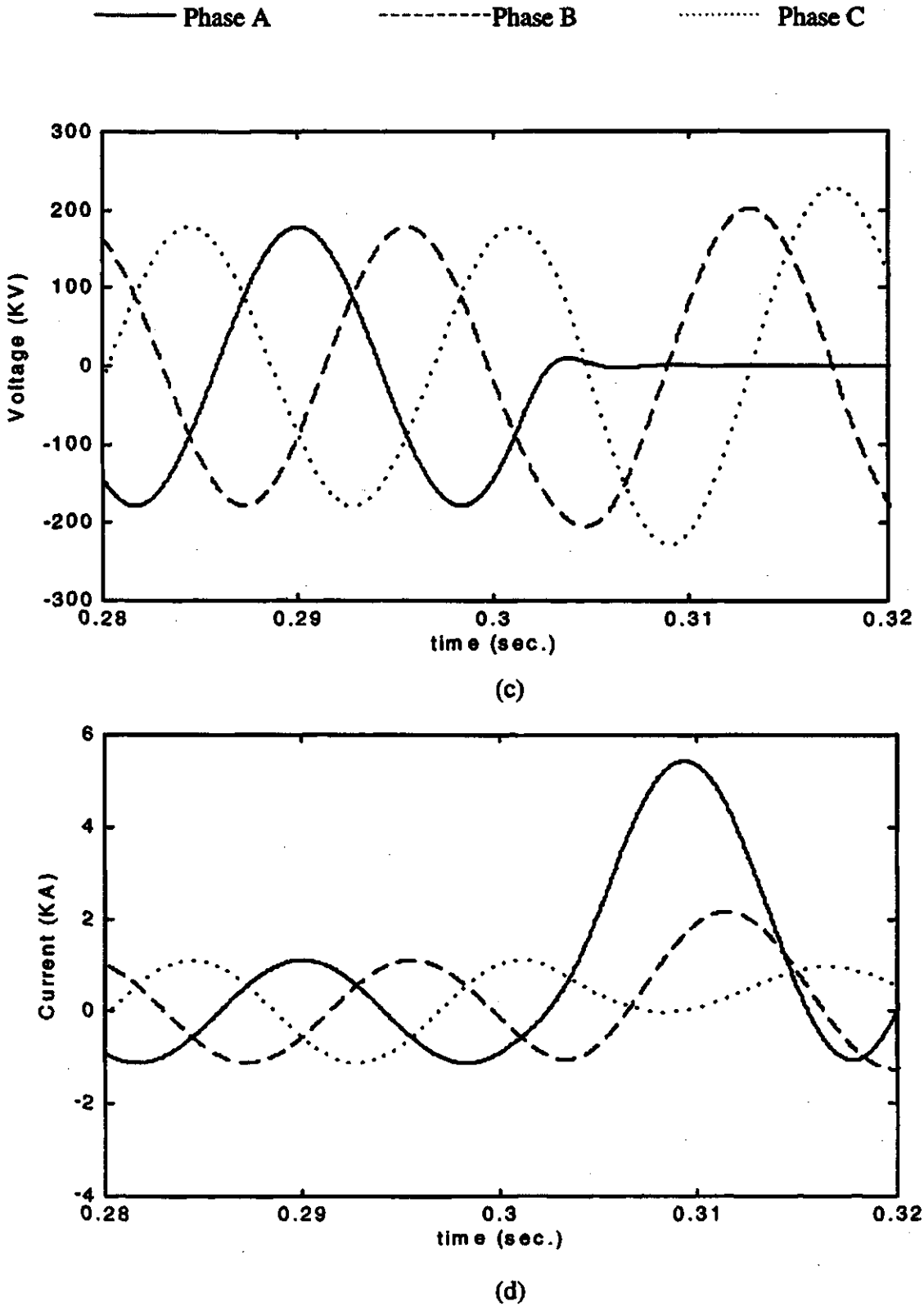
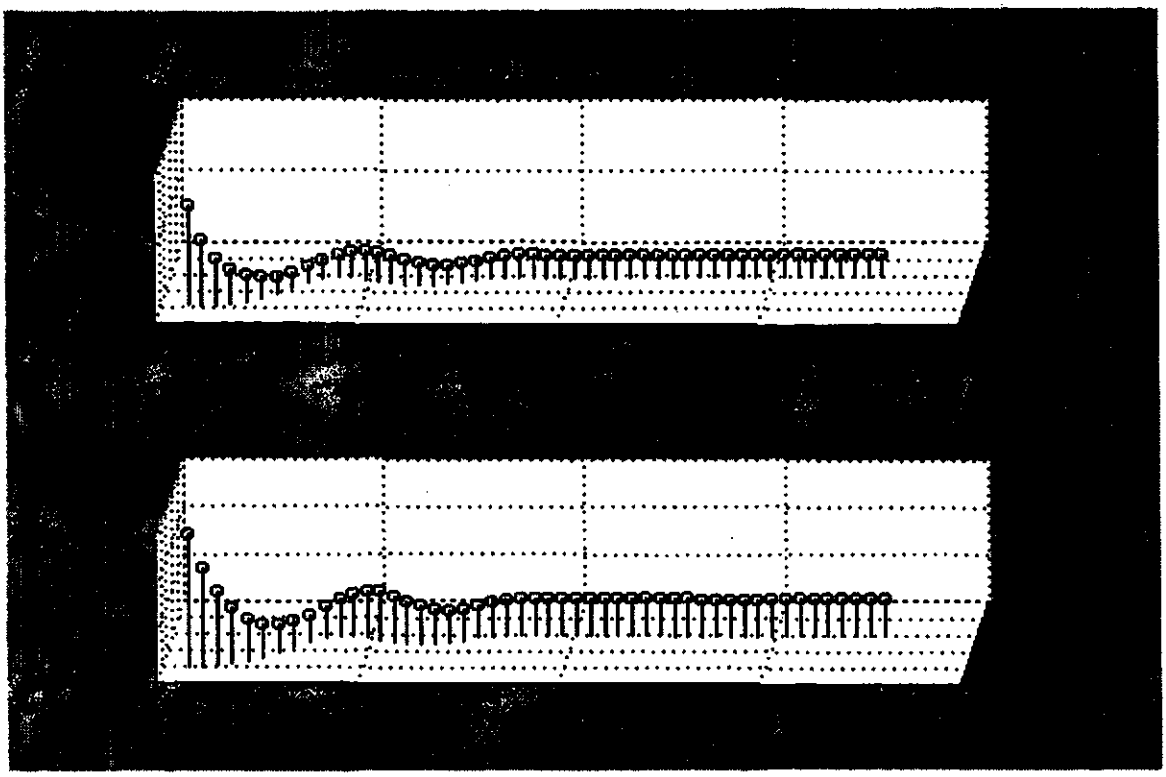
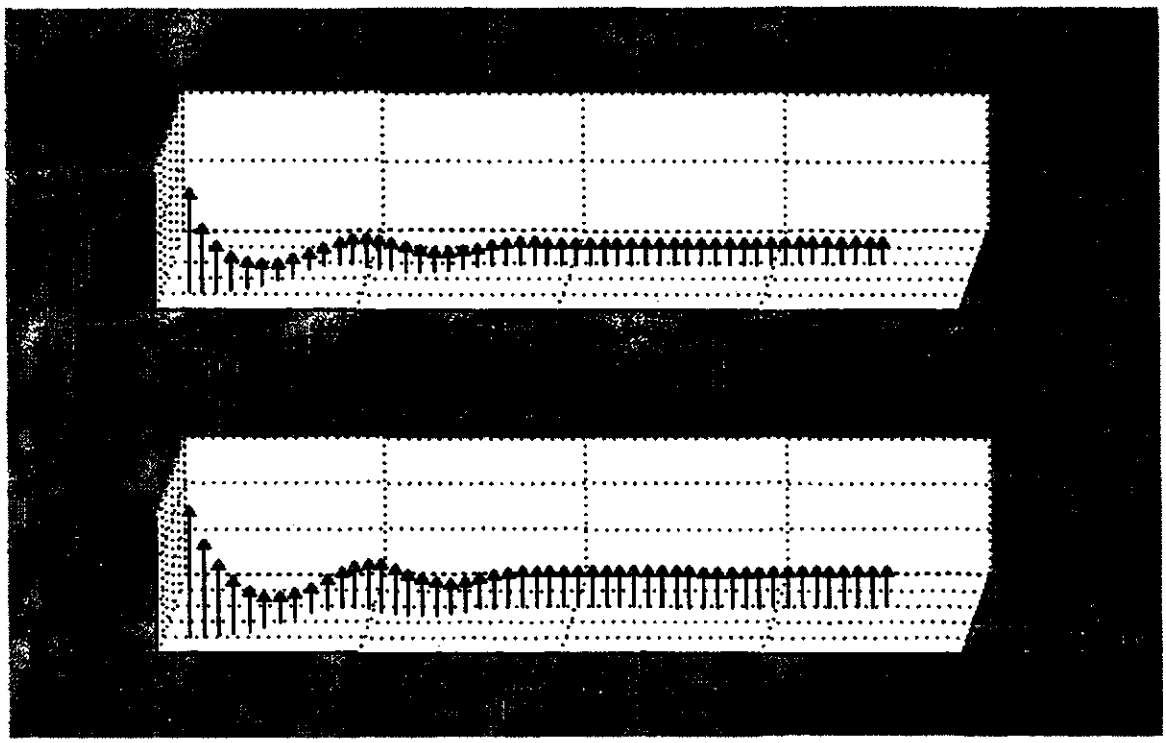


Figure 4.3(contd.). Plot of filtered (c) voltage and (d) current waveforms on the 230 kV side of power transformer for A-g internal fault in the 230 kV winding.

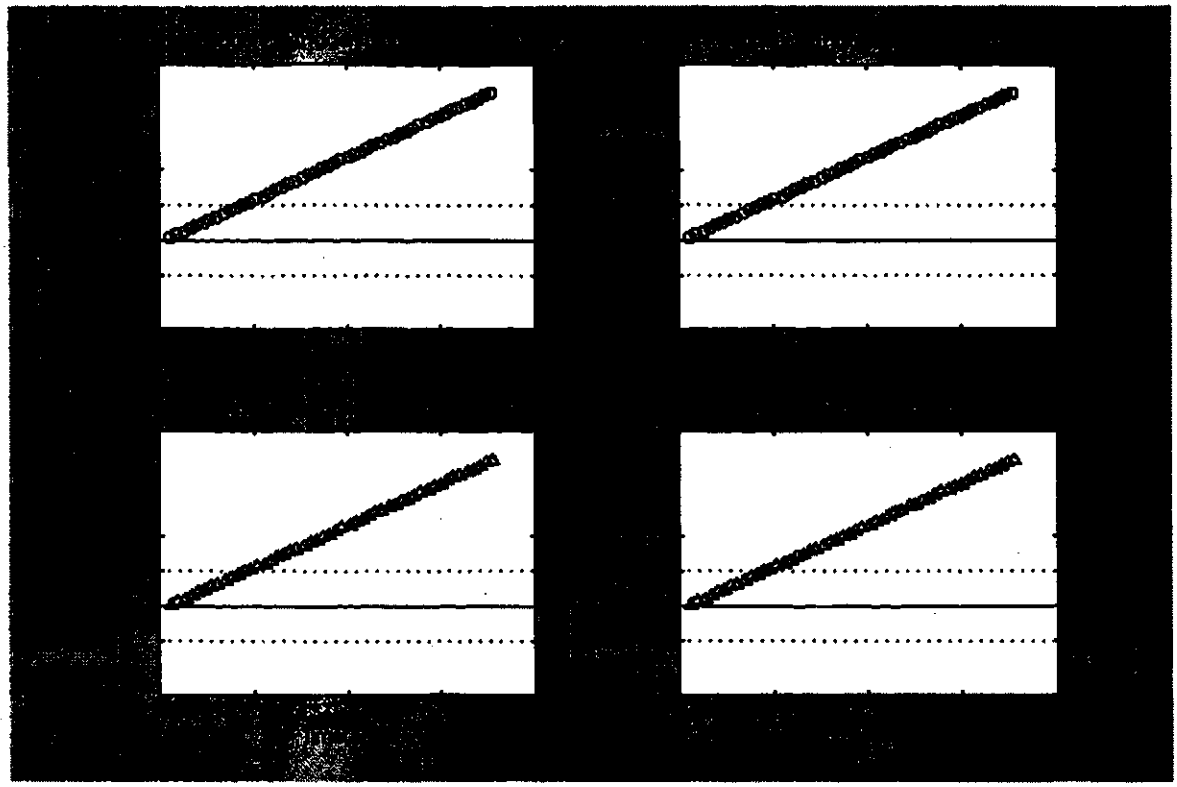


(a)



(b)

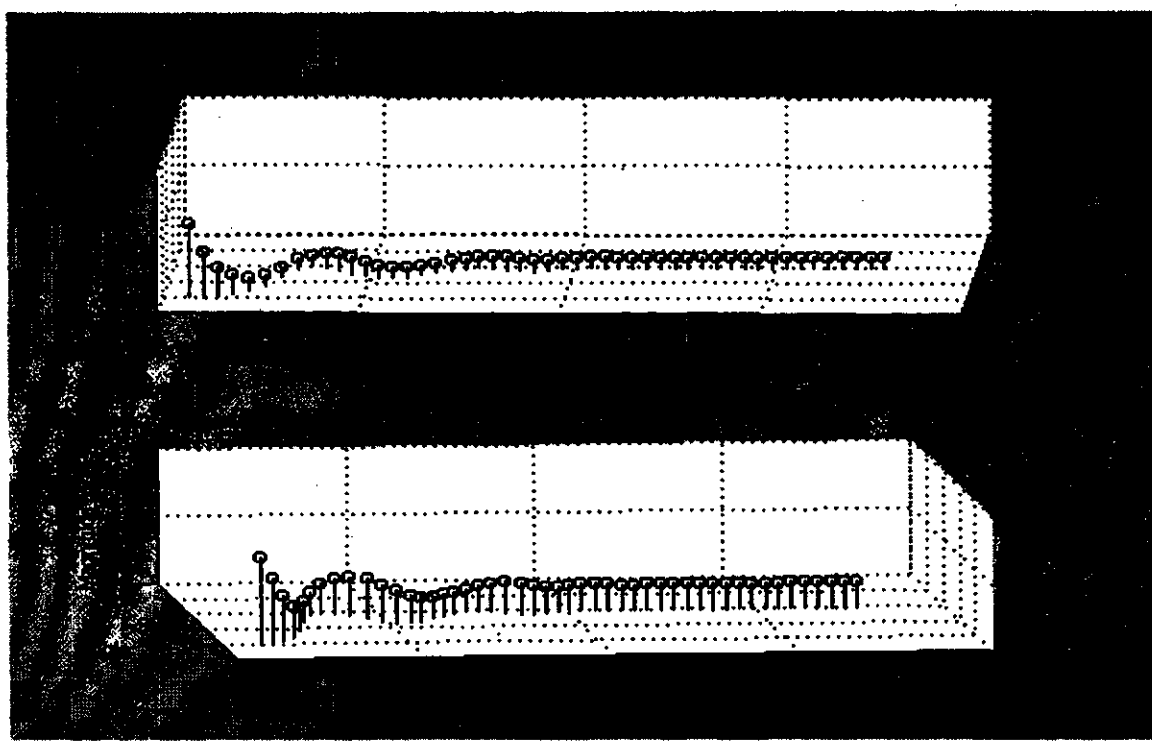
Figure 4.4. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground internal fault in the 230 kV winding of the power transformer (location 3, Figure 4.1).



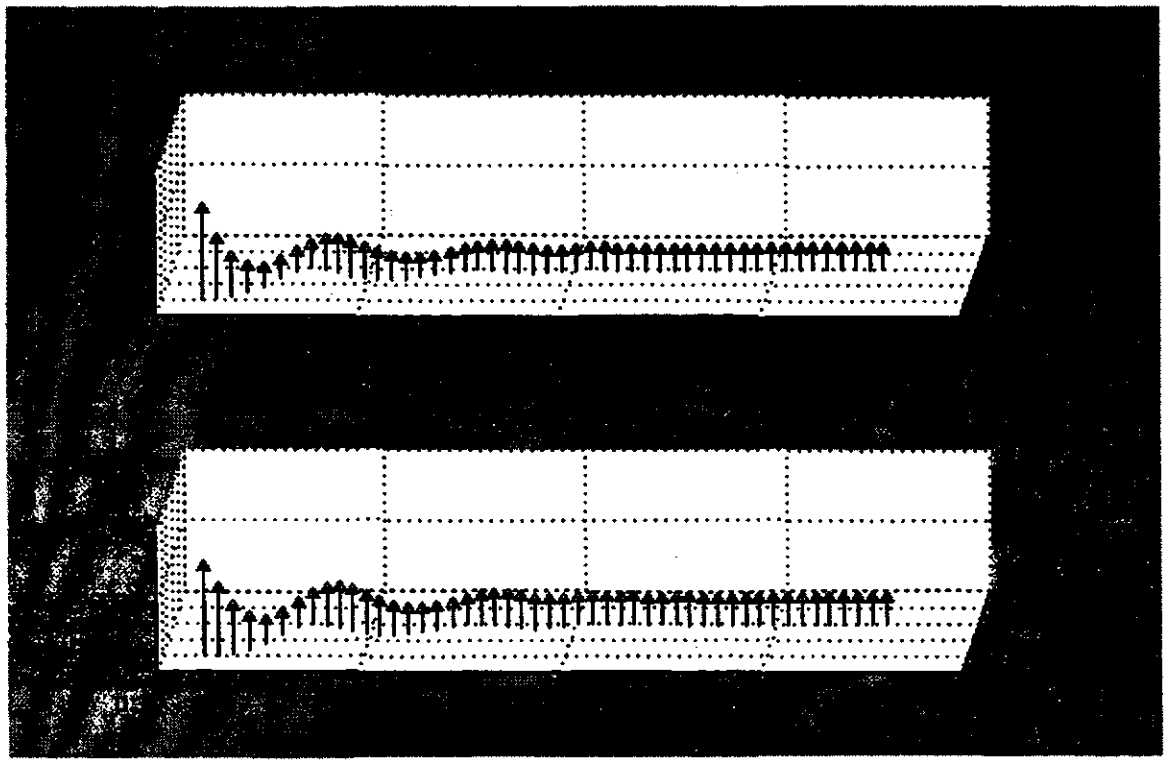
(c)

Figure 4.4. Plot of (c) trip counters for relays on two sides of power transformer for A-g internal fault in 230 kV winding.

0.3 s. Figure 4.5 shows the performance of the algorithm. The positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of the sequence impedances (in polar form) are shown in Figures 4.5 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.5 (c). For this fault, the computed positive- and negative-sequence impedances, indicate that the fault is in the protection zone of the transformer. The plots of the positive-sequence trip counters of the 13.8 kV and 230 kV sides reached the threshold in 14 samples. The plots of the negative-sequence trip counters of the 13.8 kV and 230 kV sides also reached the threshold in 14 samples. It took the algorithm 9.7 ms to make the final decision in this case.

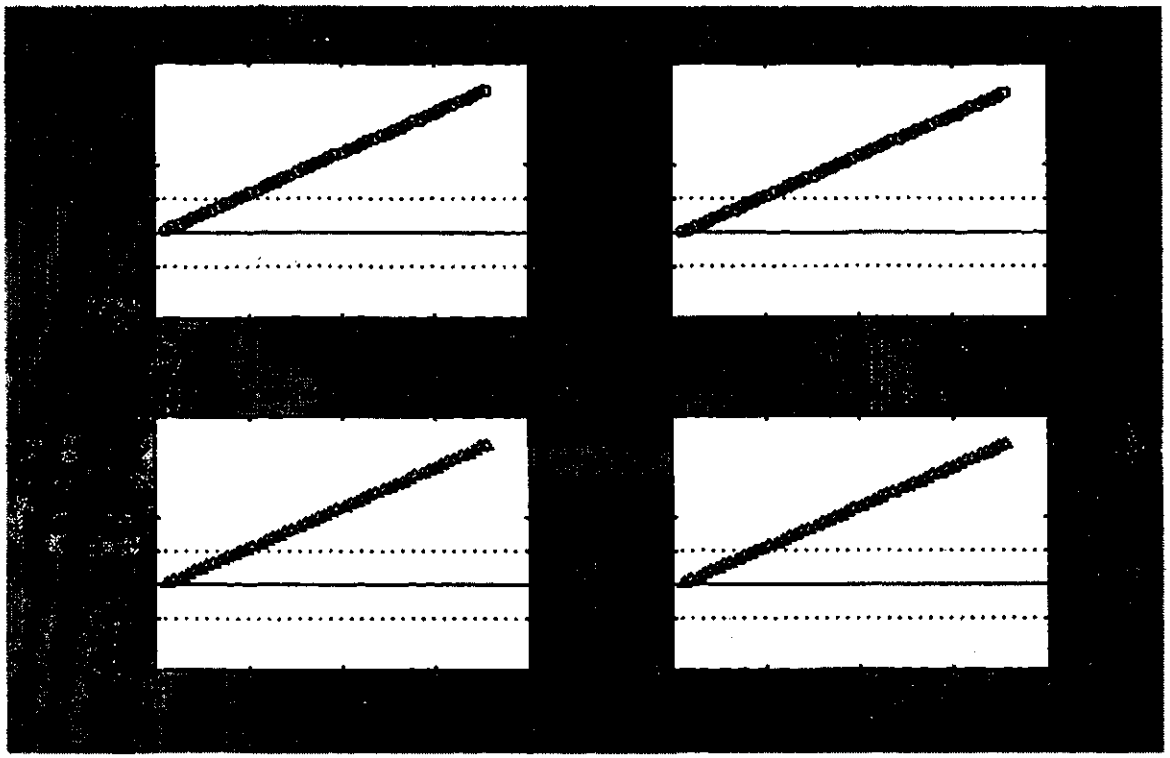


(a)



(b)

Figure 4.5. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase B-Phase C internal fault in the 230 kV winding of the power transformer (location 3, Figure 4.1).

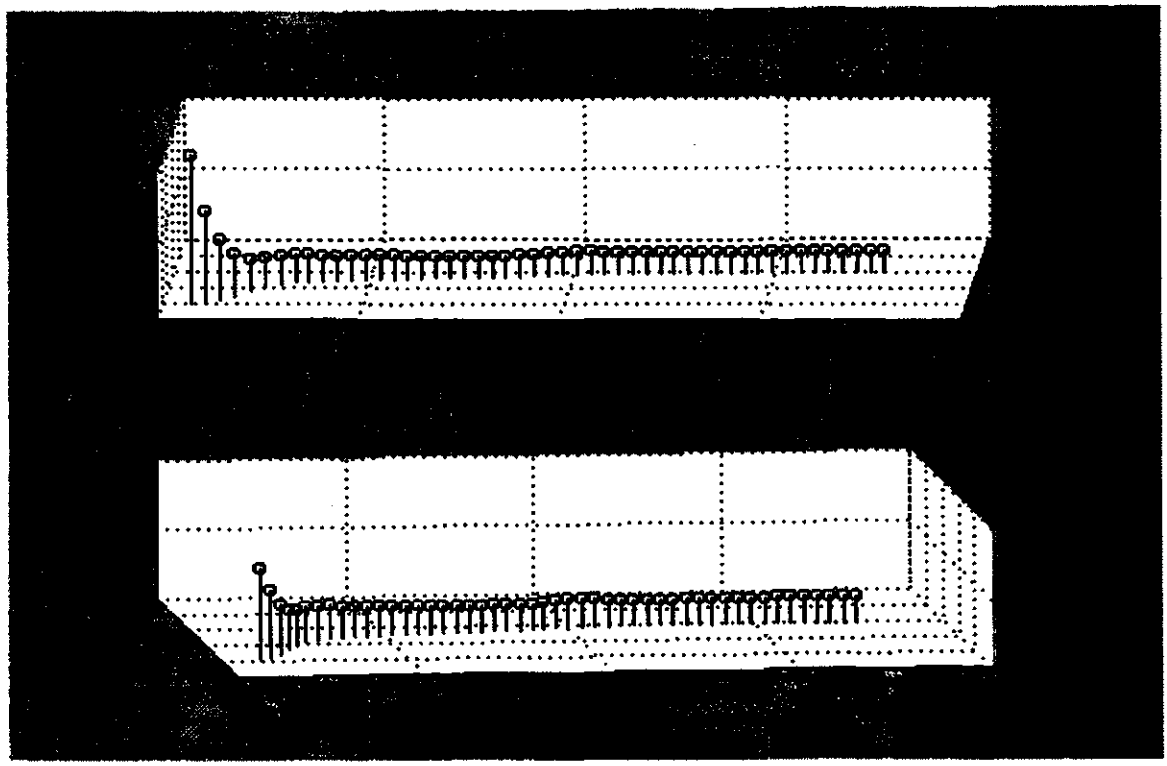


(c)

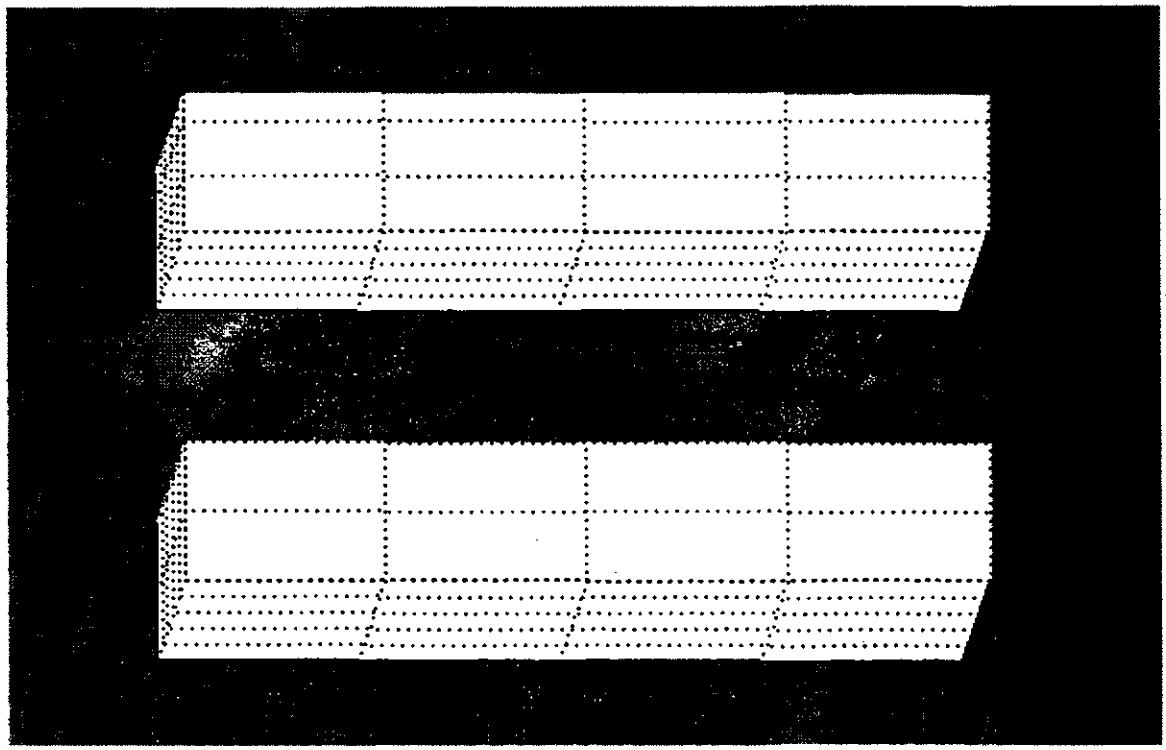
Figure 4.5. Plot of (c) trip counters for relays on two sides of power transformer for Phase B-Phase C internal fault in 230 kV winding.

4.3.1.3. Three - phase fault

A three-phase fault was simulated on the 13.8 kV side of the power transformer (location 2 shown in Figure 4.1). Figure 4.6 shows the performance of the algorithm. The fault was applied at 0.3 s. After the inception of the fault which took two samples, the positive- and negative-sequence impedances were computed from the incremental voltages and currents. The values of the sequence impedances (in polar form) are shown in Figures 4.6 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.6 (c). The plot of the trip counters show that the positive-sequence trip counter of the 13.8 kV side reached the threshold in 13 samples whereas the corresponding trip counter for the 230 kV side relay took 14 samples to reach the threshold. Also, the positive-sequence impedances seen by the relays on both sides of the transformer lie in the third quadrant. This indicated a fault in the protection zone of the transformer. The logic generated a trip 14 samples after the computation of

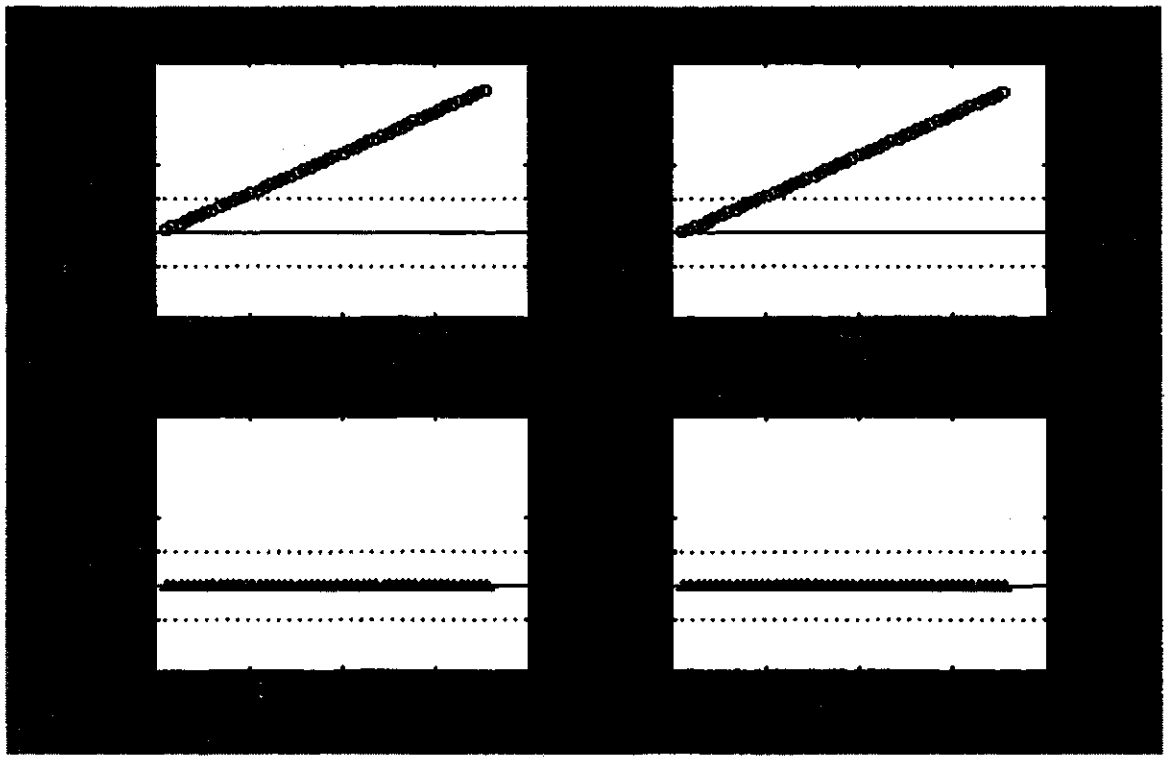


(a)



(b)

Figure 4.6. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a three-phase internal fault in the 13.8 kV winding of the power transformer (location 2, Figure 4.1).



(c)

Figure 4.6. Plot of (c) trip counters for relays on two sides of the power transformer for a three-phase internal fault in 13.8 kV winding.

the impedances started. The algorithm took 9.7 ms to detect this fault. Since negative-sequence voltages and currents are not experienced during three-phase faults, no decisions were generated from these signals.

4.3.2. External faults

External faults were simulated at locations 1, 4 and 5 shown in Figure 4.1. Selected case studies are presented in the following sections. Additional results for are presented in Appendix E.

4.3.2.1. Single phase-to-ground fault : Phase C

A single phase-to-ground fault on phase C was simulated on the 13.8 kV side of the power transformer (location 1 shown in Figure 4.1). The unfiltered and filtered voltage and current waveforms are shown in Figures 4.7 and 4.8 respectively. The fault

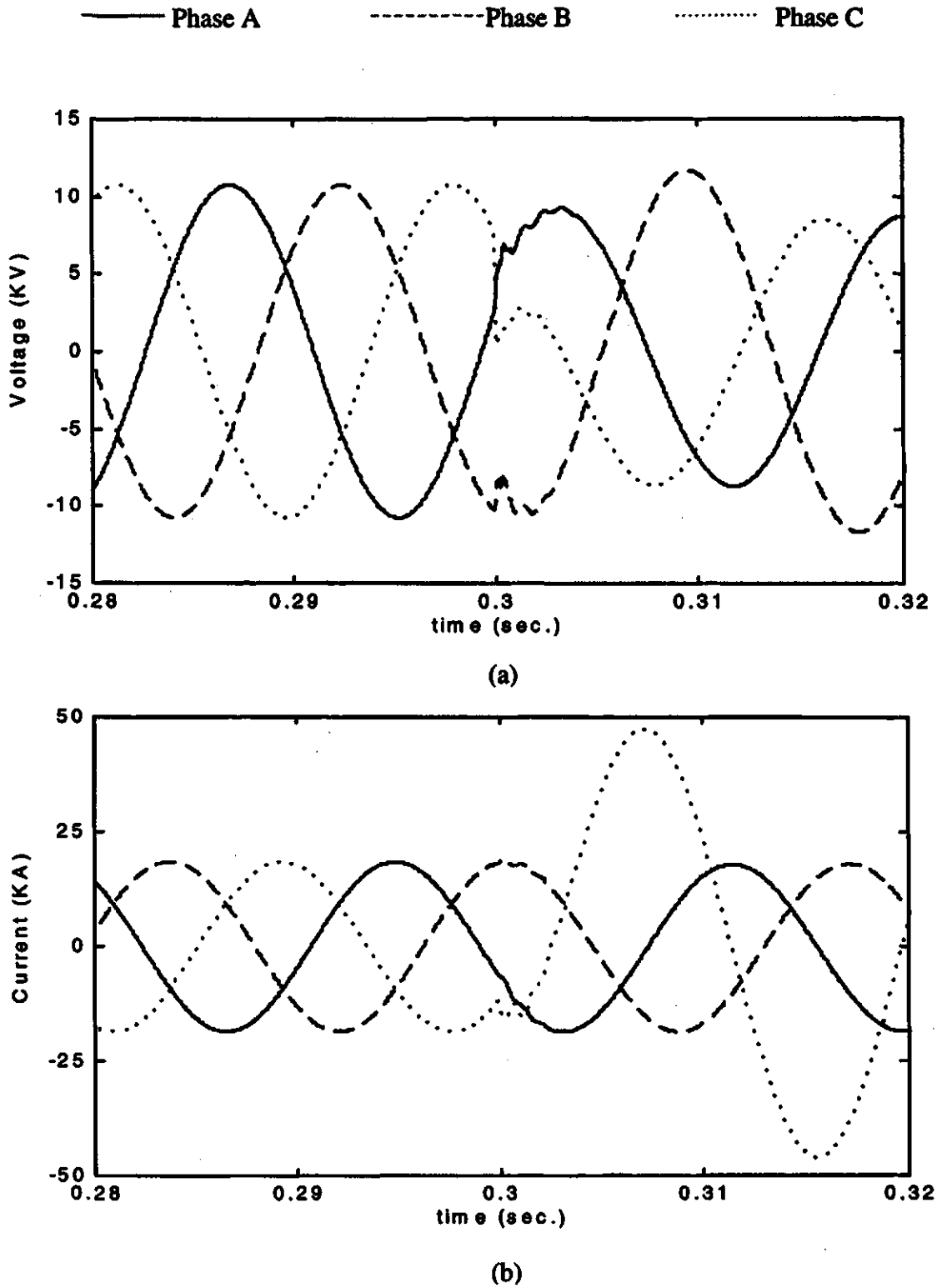
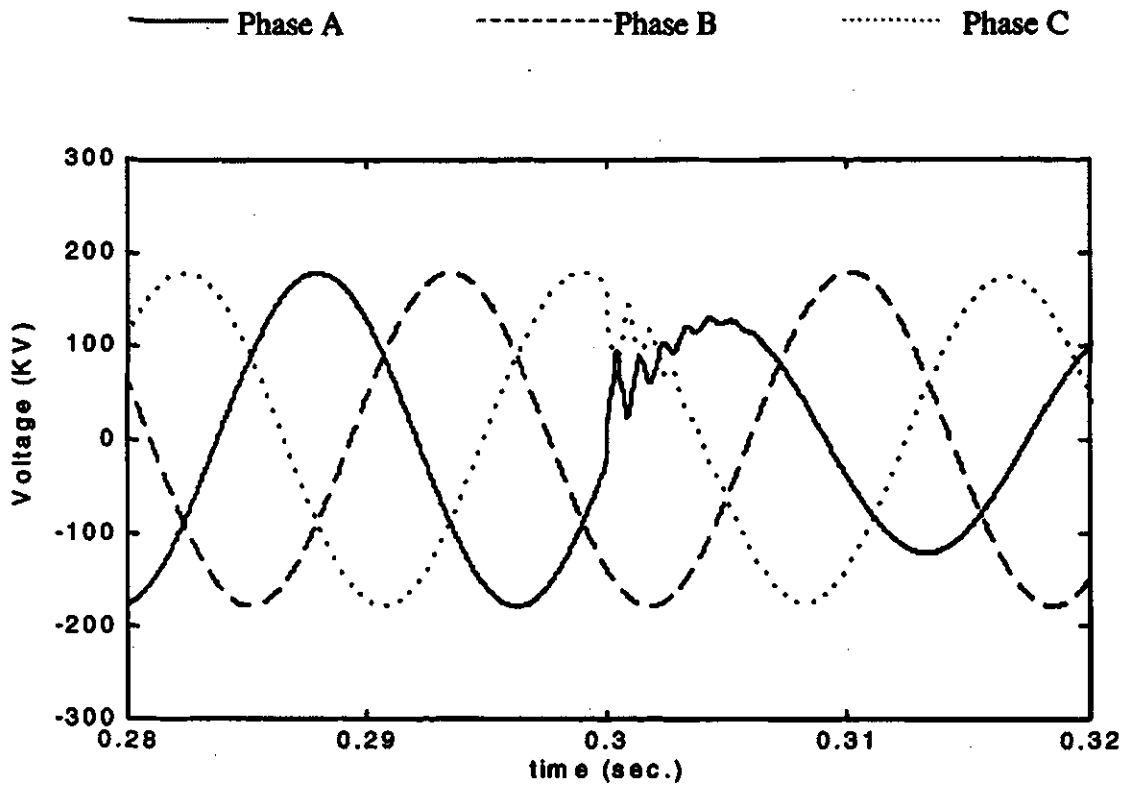
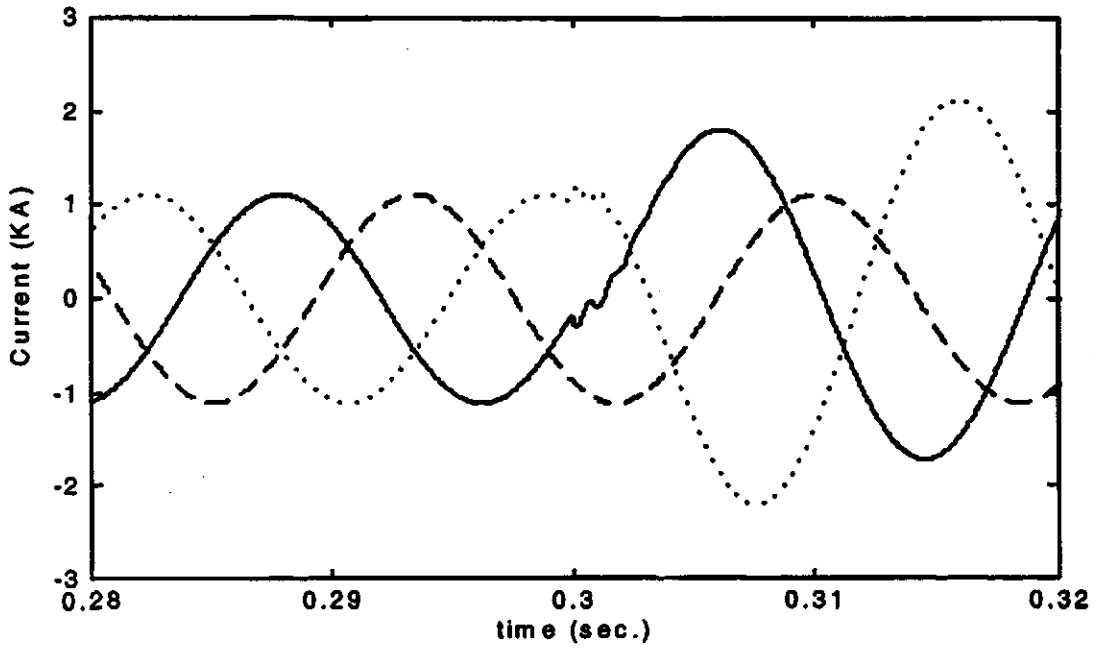


Figure 4.7. Plot of unfiltered (a) voltage and (b) current waveforms on the 13.8 kV side of the power transformer for C-g external fault on the 13.8 kV side (location 1, Figure 4.1).



(c)



(d)

Figure 4.7(contd.). Plot of unfiltered (c) voltage and (d) current waveforms on the 230 kV side of the power transformer for C-g external fault on the 13.8 kV side (location 1, Figure 4.1).

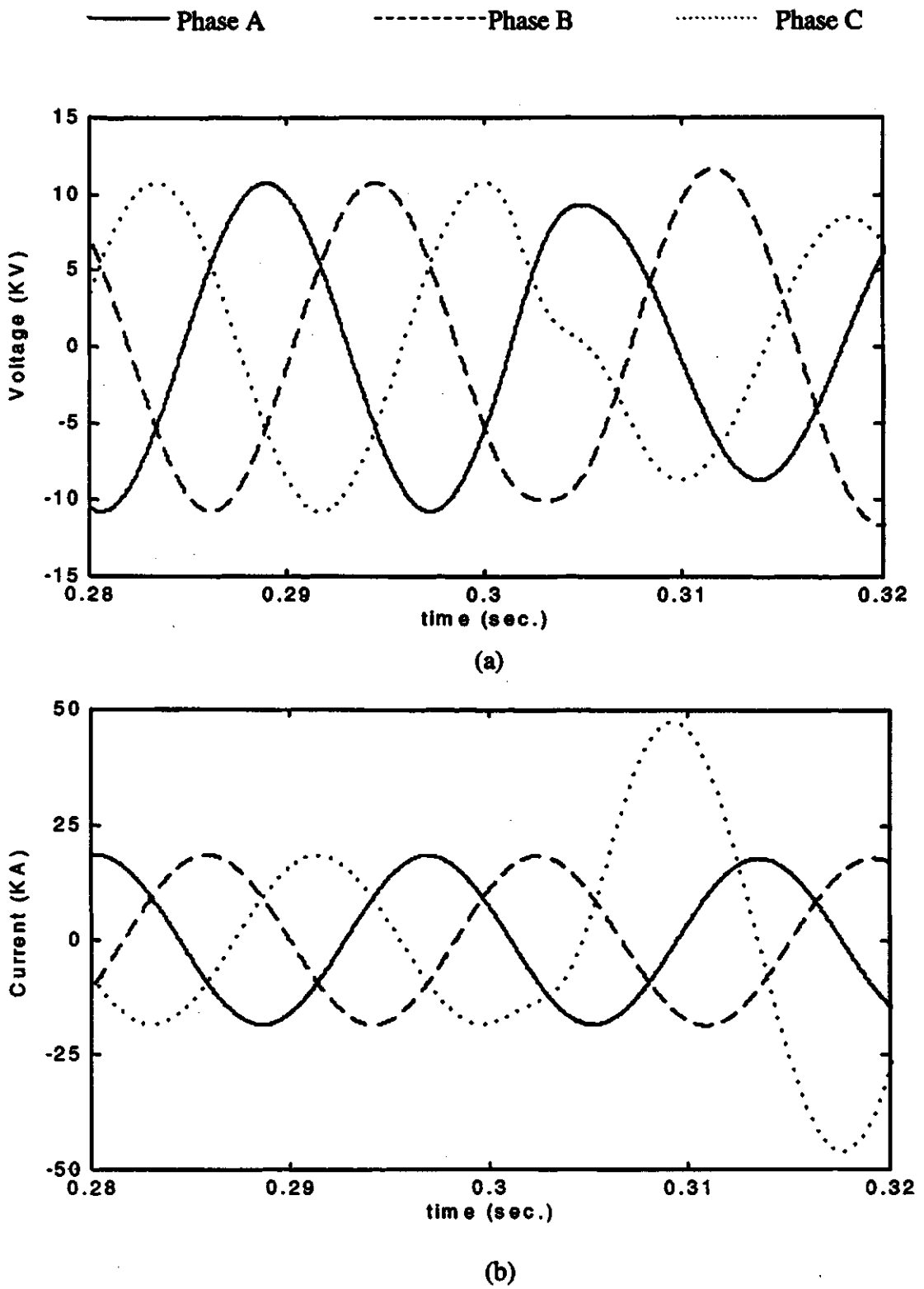


Figure 4.8. Plot of filtered (a) voltage and (b) current waveforms on the 13.8 kV side of the power transformer for C-g external fault on the 13.8 kV side (location 1, Figure 4.1).

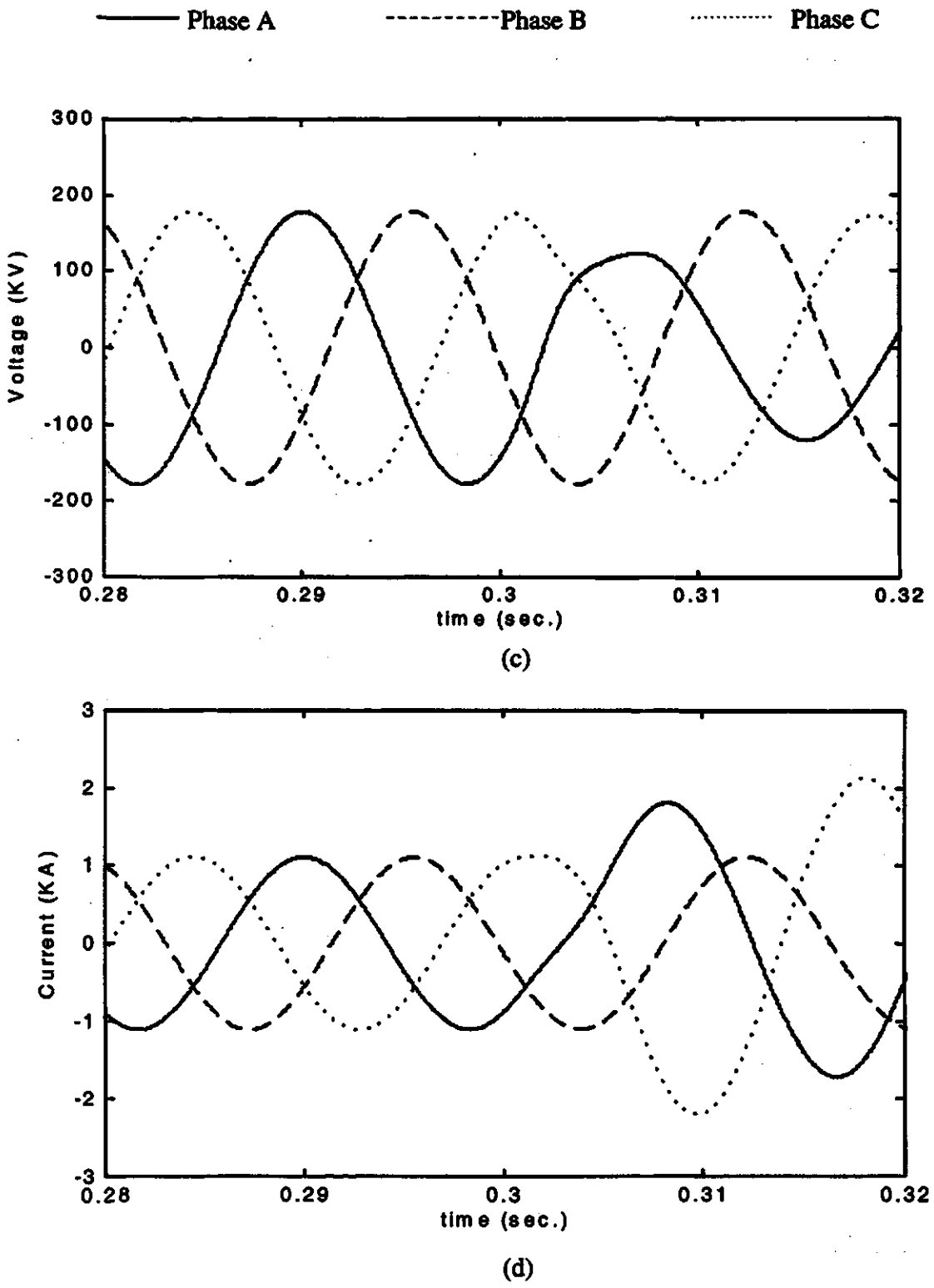
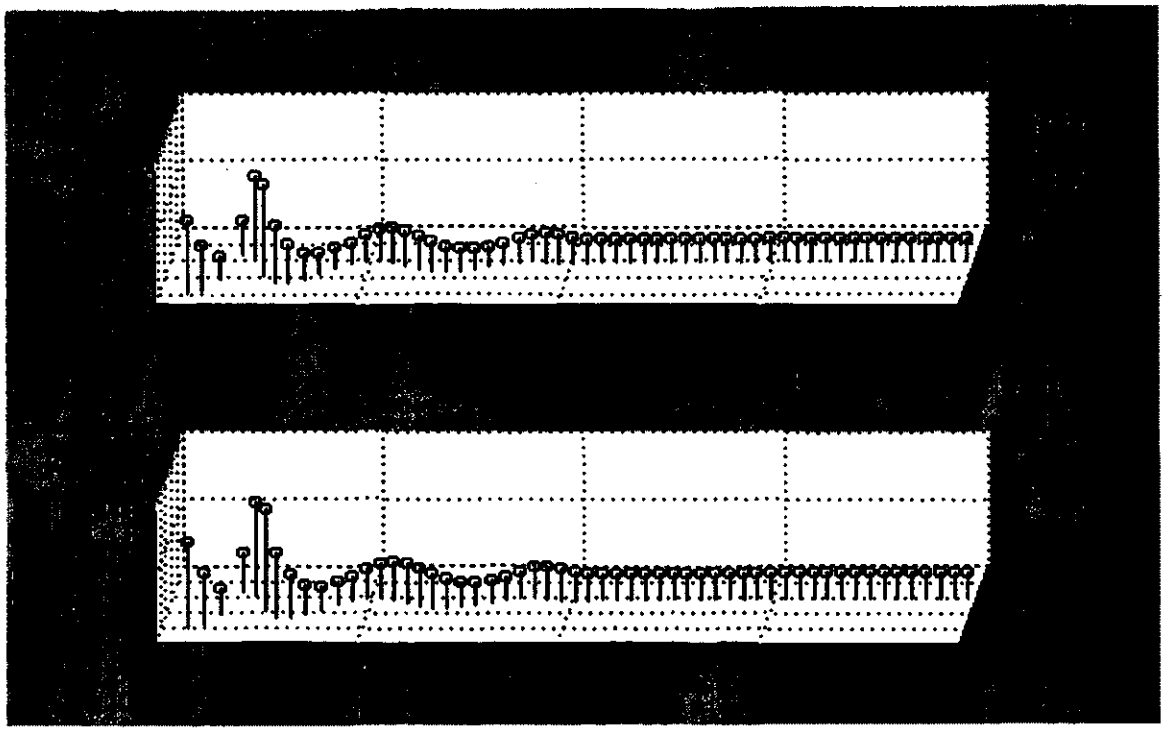


Figure 4.8(contd.). Plot of filtered (c) voltage and (d) current waveforms on the 230 kV side of the power transformer for C-g external fault on the 13.8 kV side (location 1, Figure 4.1).

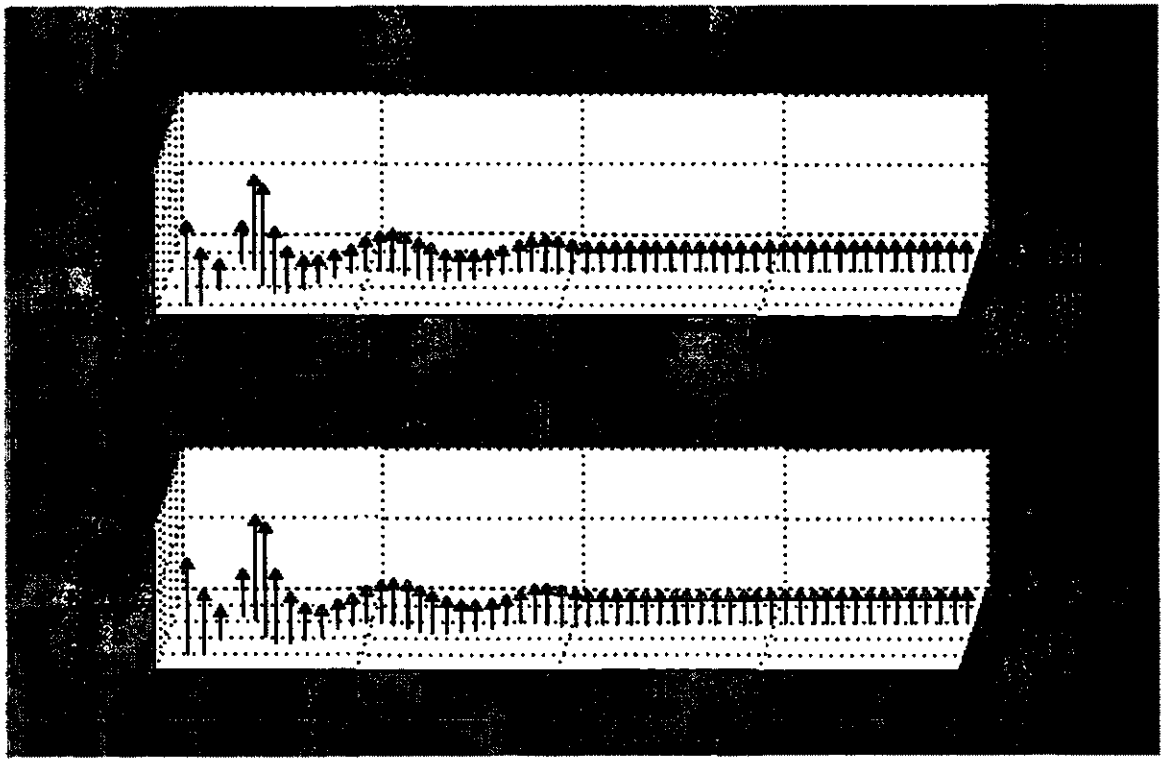
was applied at 0.3 s and a fault resistance of 0.1 ohm was used. Figure 4.9 shows the performance of the algorithm. The detection of the inception of the fault took the first two samples. After this delay, the positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of the sequence impedances (in polar form) are shown in Figures 4.9 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.9(c). For this case, the computed positive- and negative-sequence impedances calculated from the 13.8 kV data are in the first quadrant, whereas the impedances calculated from the 230 kV data are in the third quadrant. These conclusions led to the decision that the fault is outside the protection zone of the transformer. The positive- and negative-sequence trip counters of the 230 kV side reached the threshold in 15 samples. The positive-sequence trip counter of the 13.8 kV side reached the threshold in 16 samples whereas the negative-sequence trip counter of the 13.8 kV side reached the threshold in 15 samples. The trip-logic confirmed after 15 samples that the fault is outside the protection zone. The algorithm took 10.4 ms to make this decision.

4.3.2.2. Two-phase fault : Phase A - Phase B

A Phase A-Phase B fault was simulated on the 230 kV side of the power transformer (location 5 shown in Figure 4.1). The fault was applied at time 0.3 seconds. Figure 4.10 shows the performance of the algorithm. The detection of the inception of the fault took the first two samples. After this delay, the positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of sequence impedances (in polar form) are shown in Figures 4.10 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.10(c). For this case, the computed positive- and negative-sequence impedances on the 13.8 kV side are in the third quadrant, whereas the impedances calculated from the 230 kV data are in the first quadrant. These conclusions led to the decision that the fault is outside the protection zone of the transformer. All trip counters reached the threshold in 13 samples. It took 9.0 ms to make the final decision in this case.

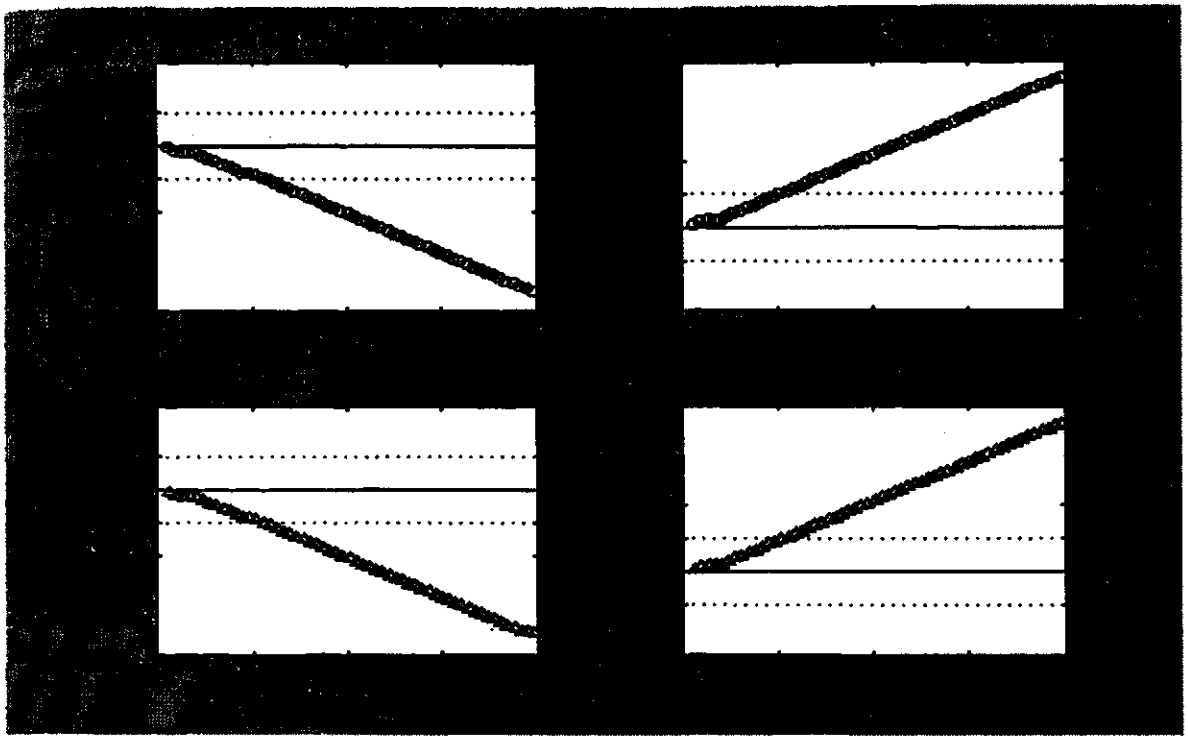


(a)



(b)

Figure 4.9. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase C-ground external fault on the 13.8 kV side of the power transformer (location 1, Figure 4.1).

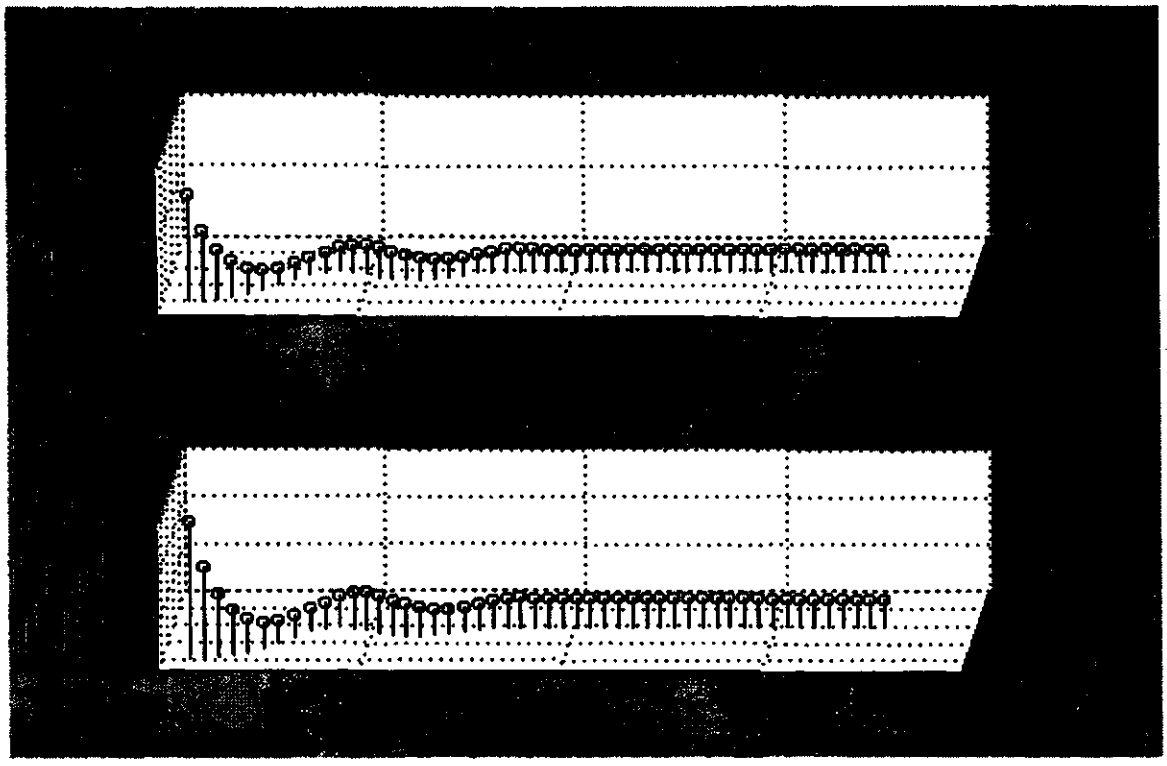


(c)

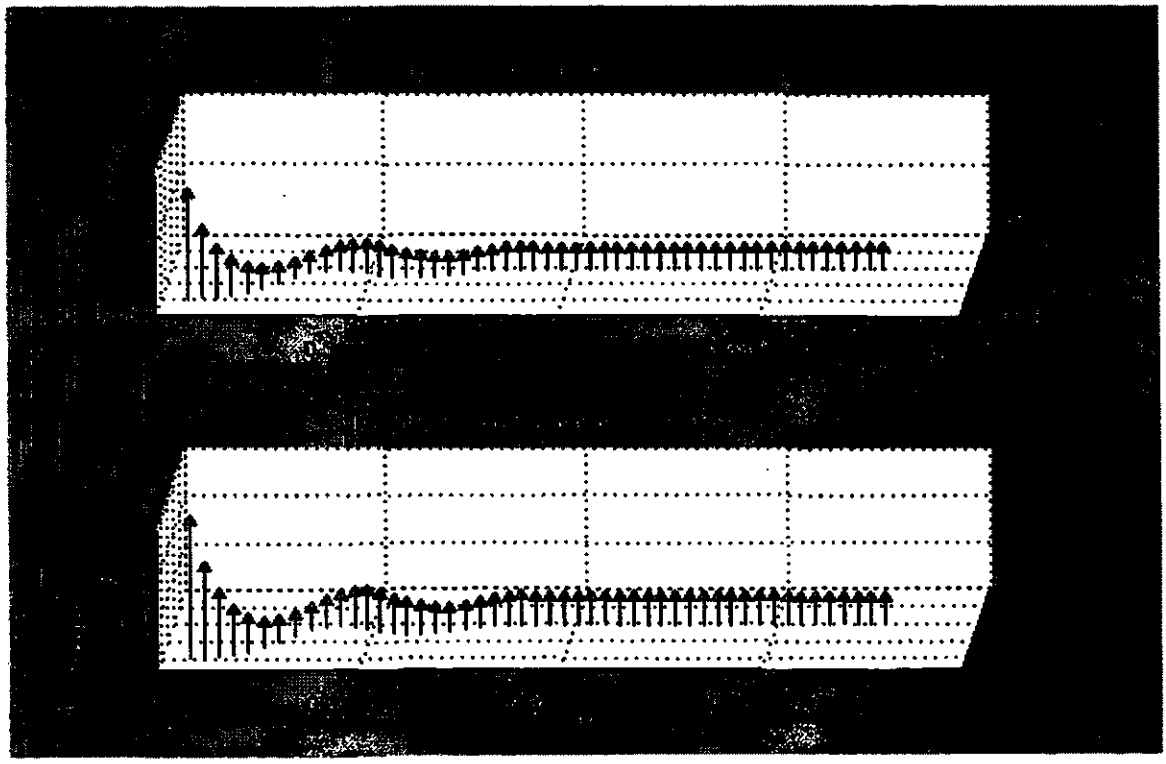
Figure 4.9. Plot of (c) trip counters for relays on two sides of power transformer for C-g external fault on 13.8 kV side (location 1, Figure 4.1).

4.3.2.3. Three - phase fault

A three-phase fault was simulated on the 230 kV side of the power transformer (location 5 shown in Figure 4.1). The fault was applied at 0.3 s. The performance of the algorithm is shown in Figure 4.11. The detection of the inception of the fault took the first two samples. After this delay, the positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of the sequence impedances (in polar form) are shown in Figures 4.11 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.11(c). The plot of the trip counters show that the positive-sequence trip counters for the 13.8 kV and 230 kV sides of the power transformer reached the threshold in 13 samples. The positive-sequence impedances seen by the relay R_x are in the third quadrant and those seen by the relay R_y are in the first quadrant. These conclusions led to the decision that the fault is outside the protection zone of the transformer. The algorithm confirmed at the end of 13 samples that the fault is outside the protection zone of the transformer. This is equivalent

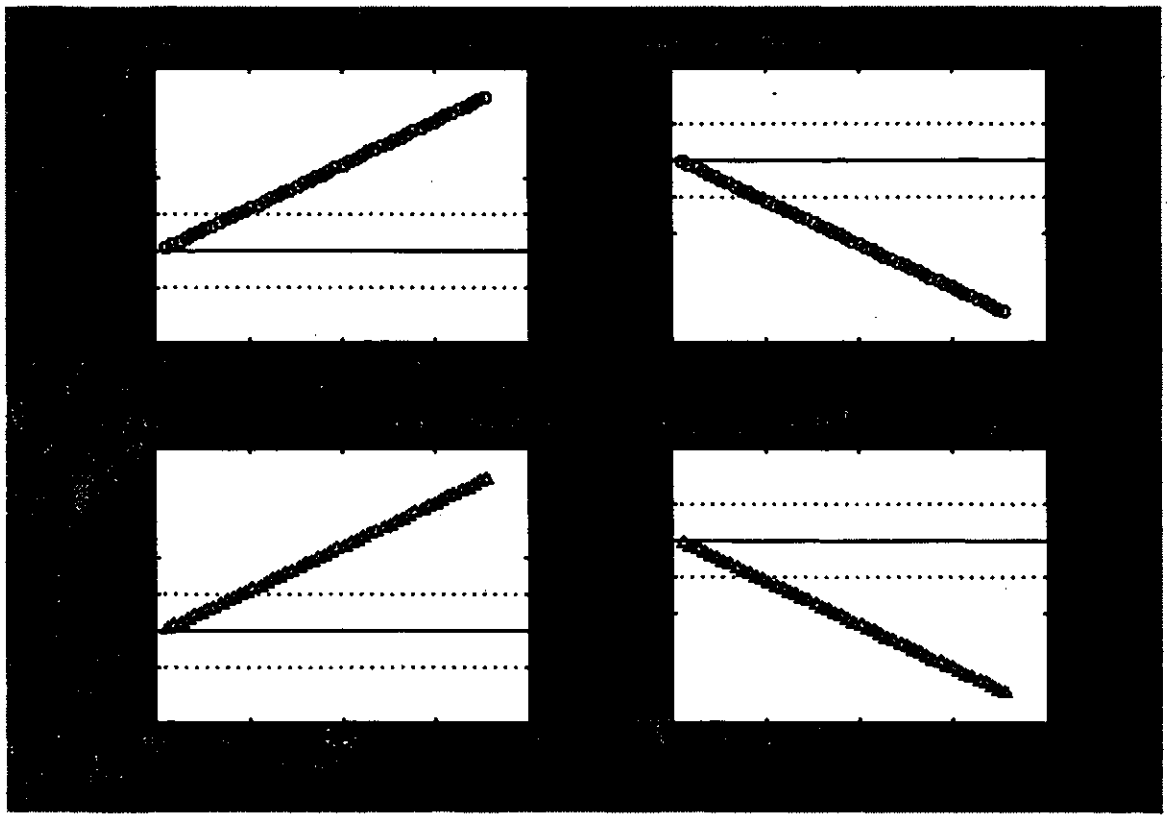


(a)



(b)

Figure 4.10. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B external fault on the 230 kV side of the power transformer (location 5, Figure 4.1).



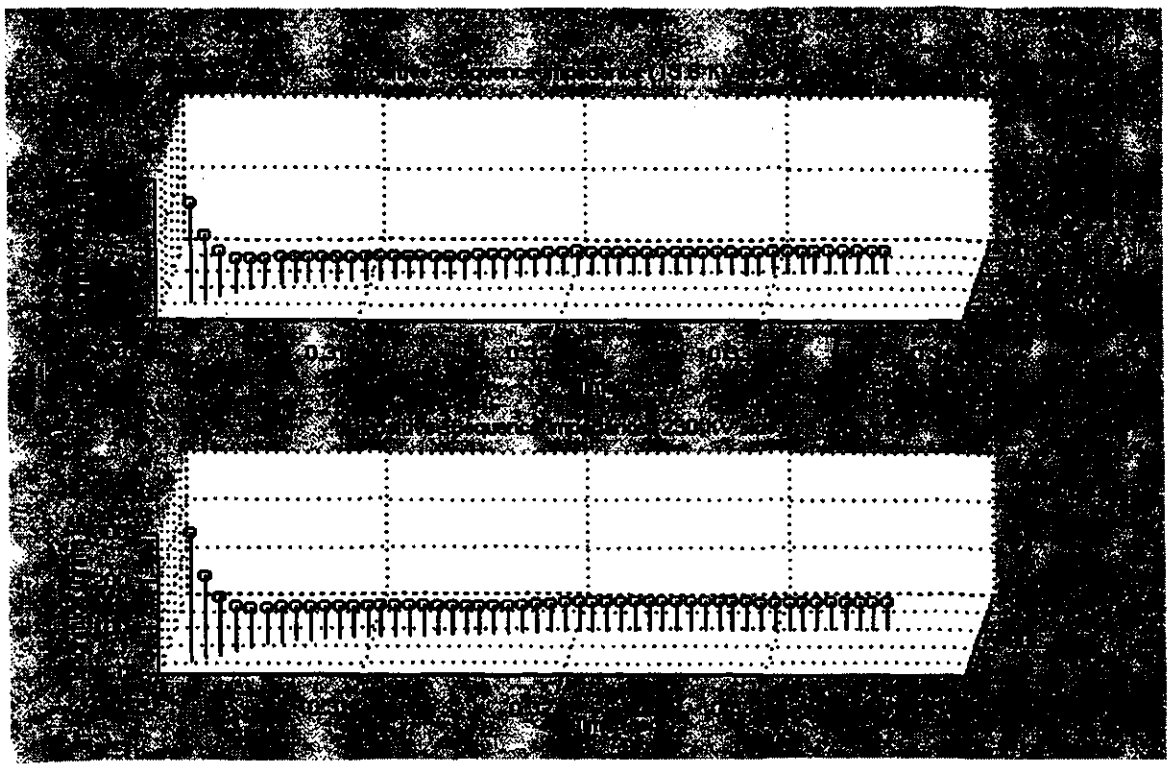
(c)

Figure 4.10. Plot of (c) trip counters for Phase A-Phase B external fault on 230 kV side of the power transformer (location 5, Figure 4.1).

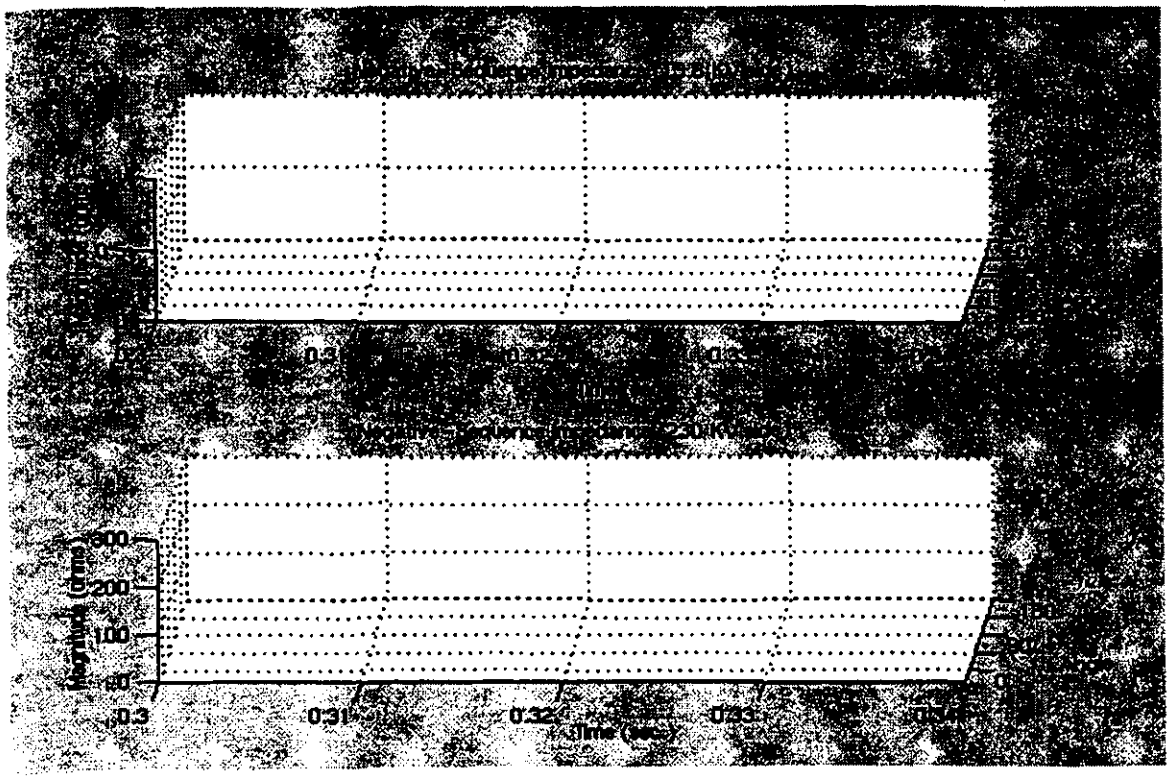
to an elapsed time of 9.0 ms. Since negative-sequence voltages and currents are not experienced during three-phase faults, the negative-sequence trip impedances were not calculated and the negative-sequence trip counters remain zero.

4.4. Effect of ratio-mismatch

The effect of ratio-mismatch between the 13.8 kV and 230 kV side cts was evaluated. Different levels of ct ratio-mismatch were simulated and studied and their impact on the proposed technique was studied. Two results are presented in this section which shows that the proposed technique remains stable inspite of ratio-mismatch conditions.

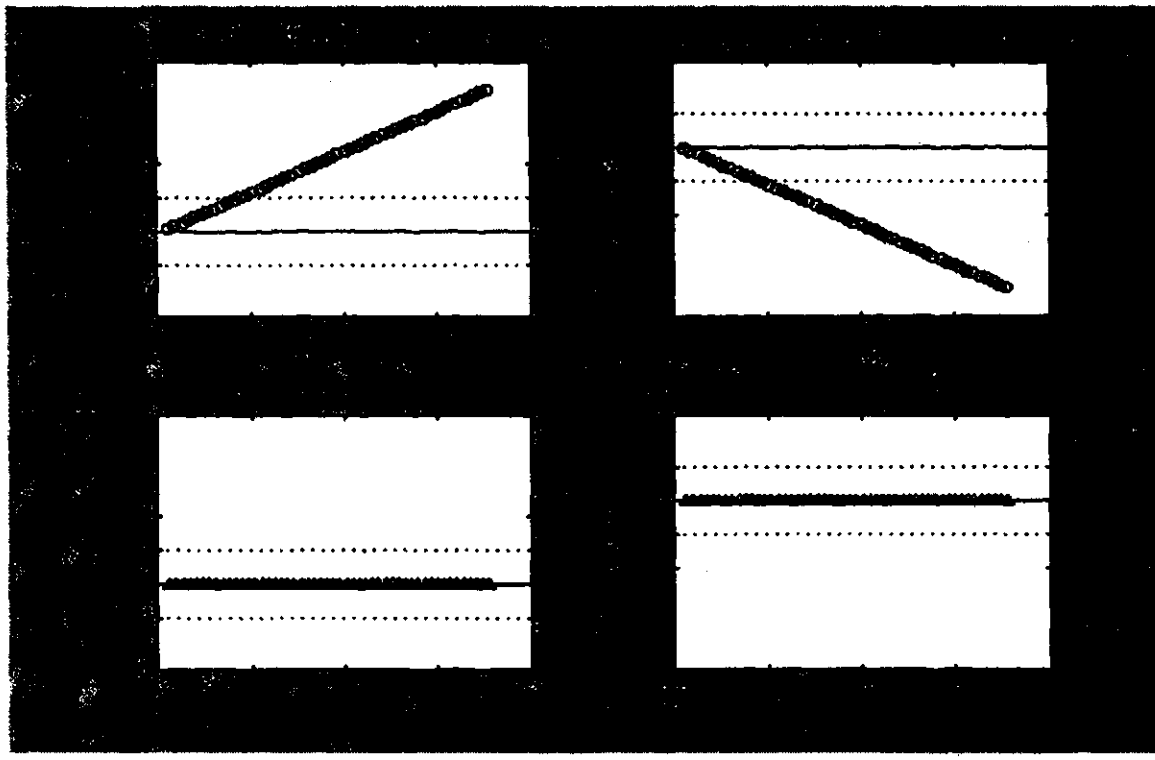


(a)



(b)

Figure 4.11. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a three-phase external fault on the 230 kV side of the power transformer (location 5, Figure 4.1).

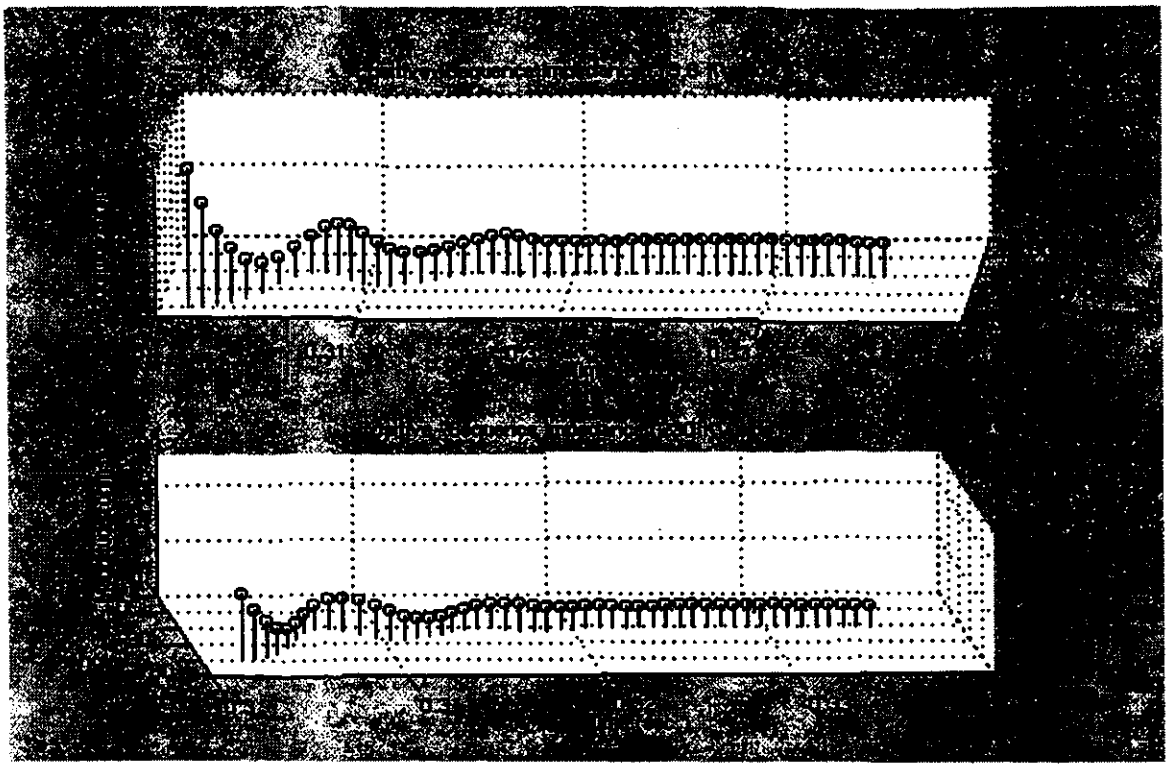


(c)

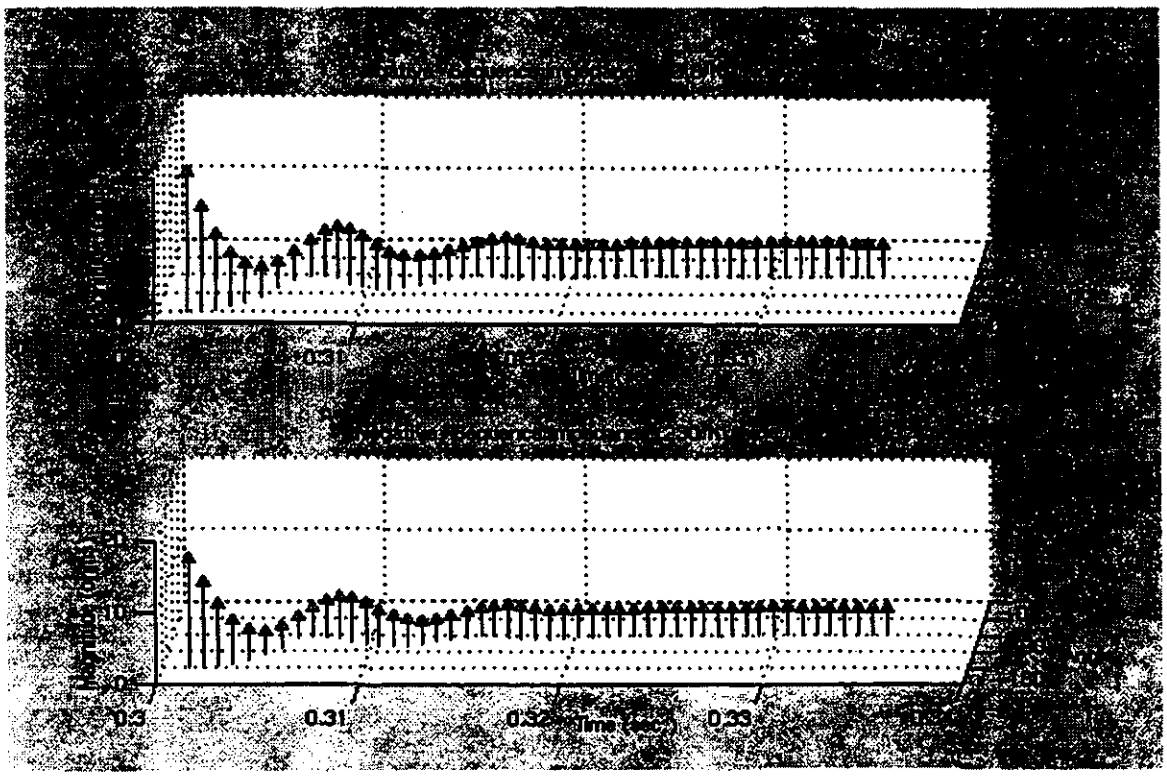
Figure 4.11. Plot of (c) trip counters for three-phase external fault on 230 kV side of the power transformer (location 5, Figure 4.1).

4.4.1. Single phase-to-ground fault : Phase A

A single phase-to-ground fault involving Phase A was simulated on the 13.8 kV side outside the transformer protection zone (location 1 shown in Figure 4.1). The matched nominal ratios for 13.8 kV and 230 kV side cts works out to 840 and 50 respectively. To study the impact of ratio-mismatch, a ct ratio of 1000 was set for the 13.8 kV side cts and a ratio of 50 (nominal value) was used for 230 kV side cts. The fault was applied at 0.3 s. The detection of its inception took the first two samples. After this delay, the positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of sequence impedances (in polar form) are shown in Figures 4.12 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.12(c). The impedance plots show that the computed positive- and negative-sequence impedances seen on the 13.8 kV side lie in

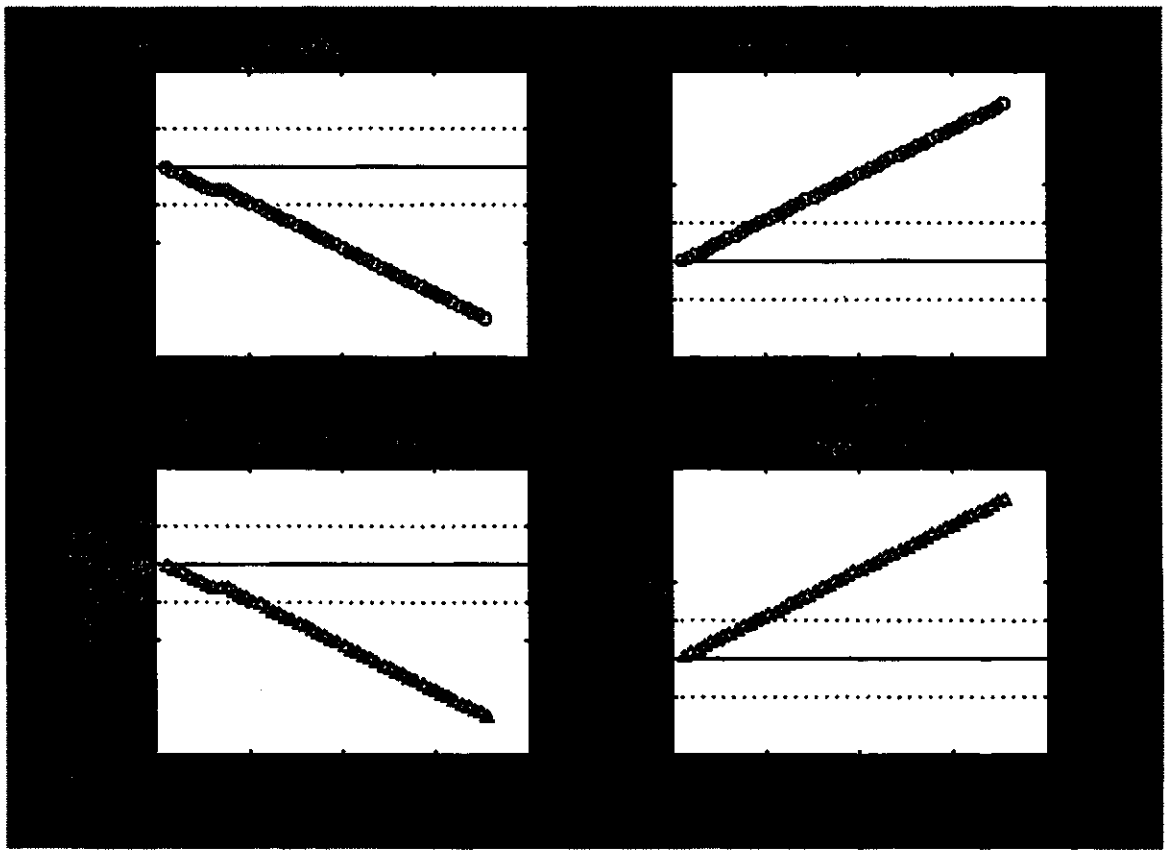


(a)



(b)

Figure 4.12. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground external fault on the 13.8 kV side of the power transformer (location 1, Figure 4.1).



(c)

Figure 4.12. Plot of (c) trip counters for Phase A-g external fault on 13.8 kV side of the power transformer (location 1, Figure 4.1).

the first quadrant. The positive- and negative-sequence impedances seen on the 230 kV side lie in the third quadrant. These conclusions led to the decision that the fault is outside the protection zone of the transformer. The positive-sequence trip counters of 13.8 kV and 230 kV sides reached the threshold in 15 samples. The negative-sequence trip counters of the 13.8 kV and 230 kV sides reached the threshold in 14 and 13 samples respectively. After 13 samples, the trip-logic confirmed that the fault is outside the protection zone. It took 9.0 ms to make the final decision. The result shows the ability of the proposed technique to provide correct decision inspite of a substantial ratio-mismatch.

4.4.2. Two-phase fault : Phase A - Phase B

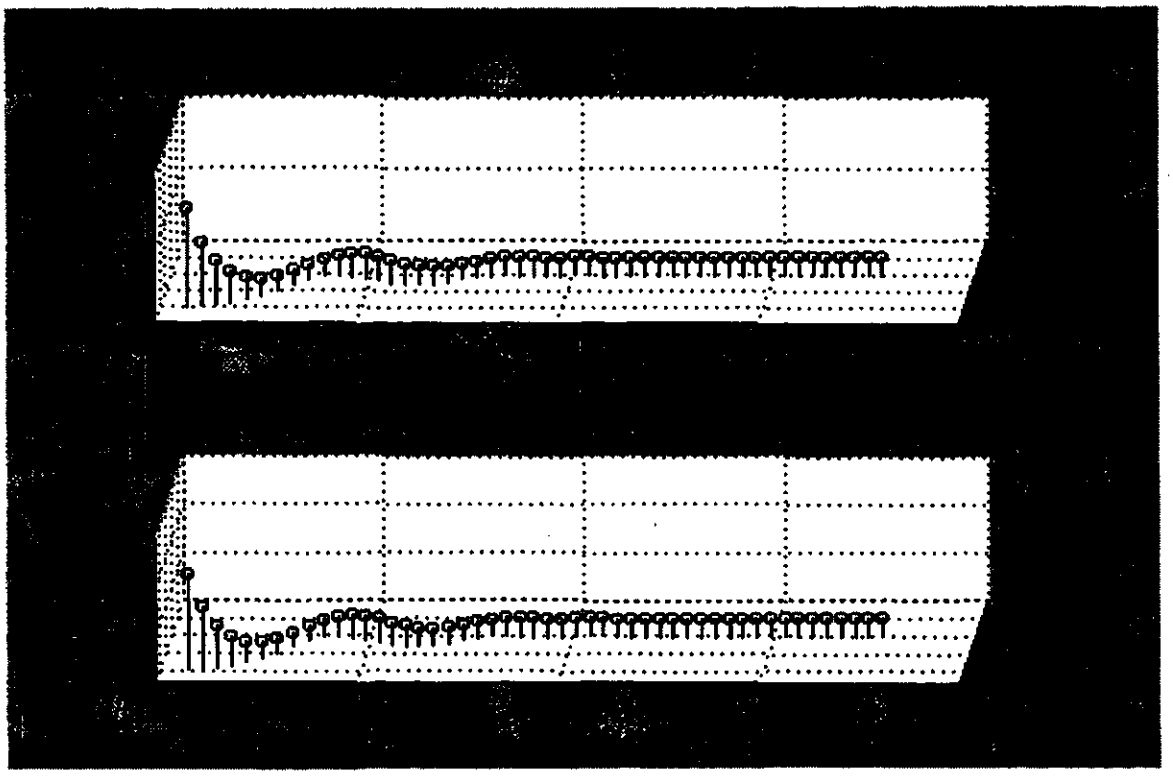
A two-phase fault involving Phase A and Phase B was simulated on the 230 kV winding of the power transformer (location 5 shown in Figure 4.1). A ratio of 840 was simulated for the 13.8 kV side cts whereas a ratio of 200 was simulated for the 230 kV side cts. Figure 4.13 shows the performance of the algorithm. The fault was applied at time 0.3 s and the detection of its inception took the first two samples. After this delay, the positive- and negative-sequence impedances were computed using the incremental voltages and currents. The values of sequence impedances (in polar form) are shown in Figures 4.13 (a) and (b). The profiles of positive- and negative-sequence trip counters are shown in Figure 4.13(c). The impedance plots show that the positive- and negative-sequence impedances seen on the 13.8 kV side of the power transformer lie in the third quadrant. The positive- and negative-sequence impedances seen on the 230 kV side lie in the first quadrant. These conclusions led to the decision that the fault occurred outside the protection zone. The positive- and negative-sequence trip counters of the 13.8 kV and 230 kV side reached the threshold in 13 samples when the trip-logic confirmed that the fault was outside the protection zone. The algorithm took 9.0 ms to make the final decision in this case.

4.5. Effect of CT saturation

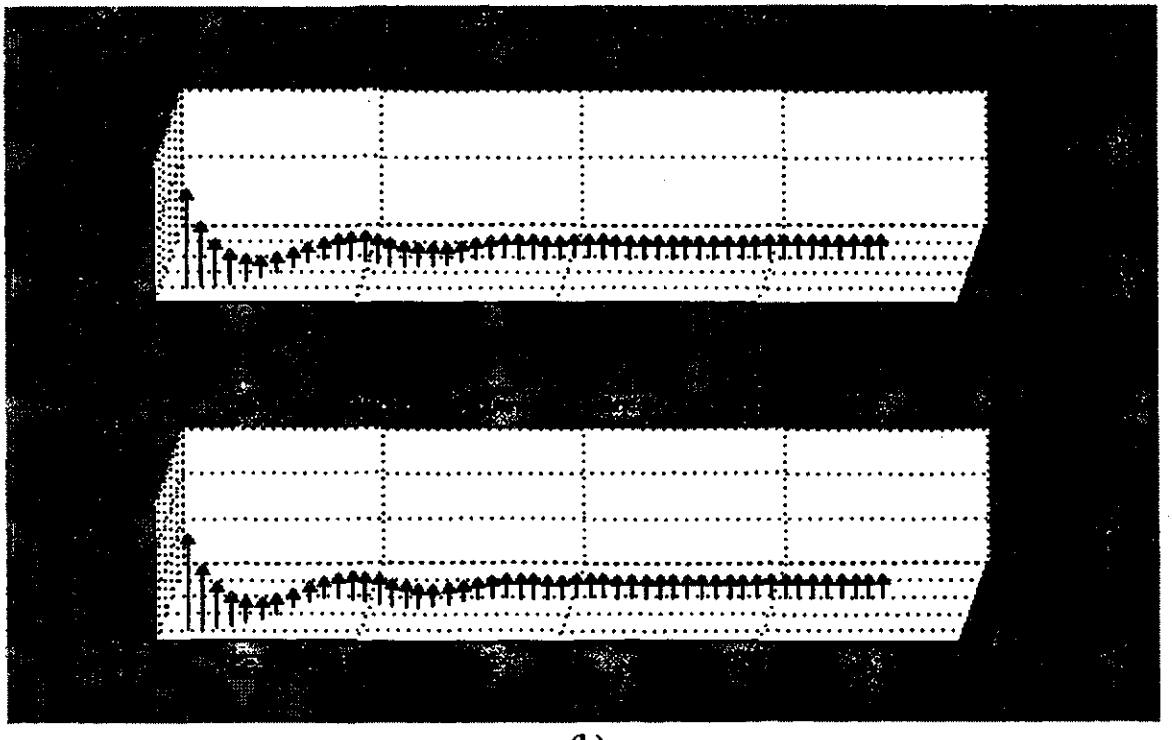
The effect of ct saturation on the performance of the algorithm was studied. Cases of various faults alongwith ct saturation were simulated. Four cases are presented in this section.

4.5.1. Three-phase fault

A three-phase fault was simulated at location 2 shown in Figure 4.1. Cts of 550 ratio and ct burdens of 40.0 ohm resistance on the 13.8 kV side were simulated. Cts of 50 ratio and ct burden of 8 ohm on the 230 kV side were also simulated. The fault was applied at 0.3 seconds. The waveforms of ct output are shown in Figure 4.14. These currents were processed by the algorithm in the manner described in Section 4.2.

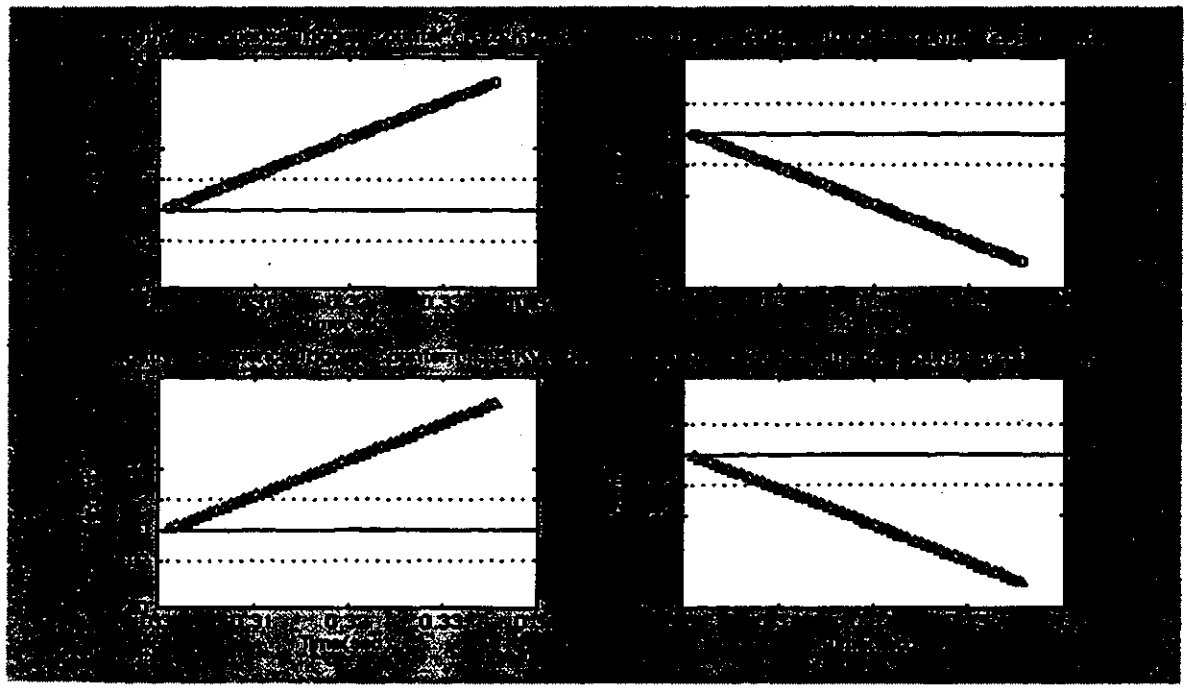


(a)



(b)

Figure 4.13. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B external fault on the 230 kV side of the power transformer (location 5, Figure 4.1).



(c)

Figure 4.13. Plot of (c) trip counters for Phase A-Phase B external fault on 230 kV side of the power transformer (at location 5, Figure 4.1).

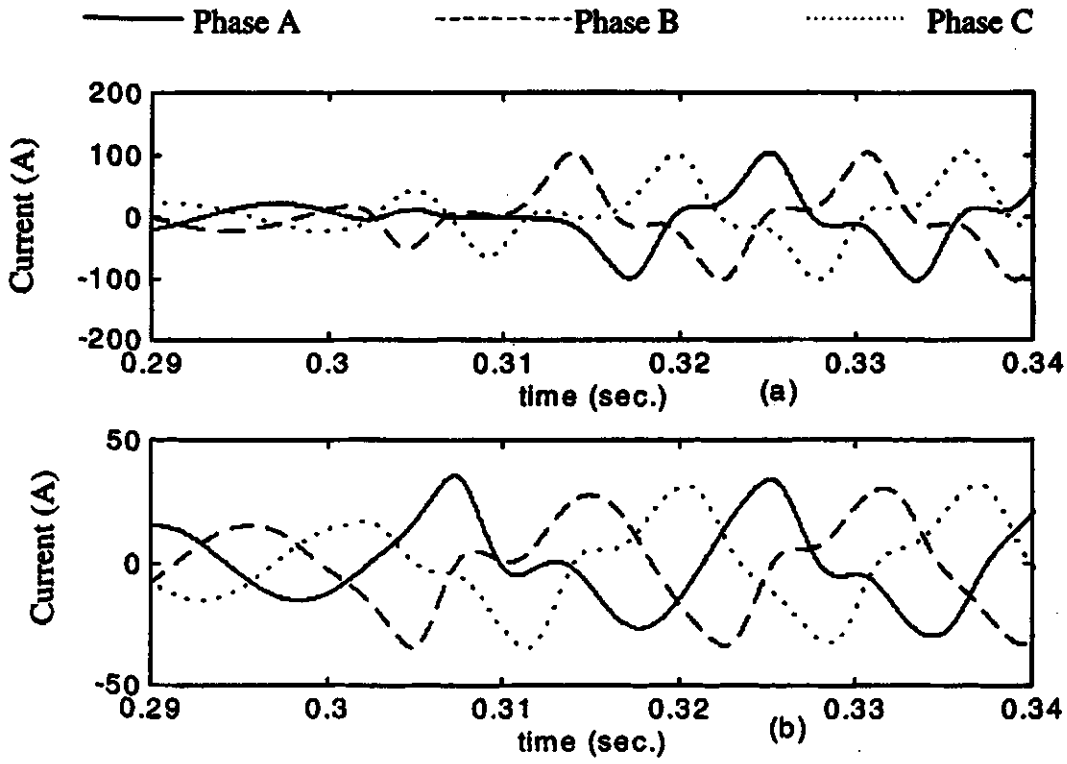
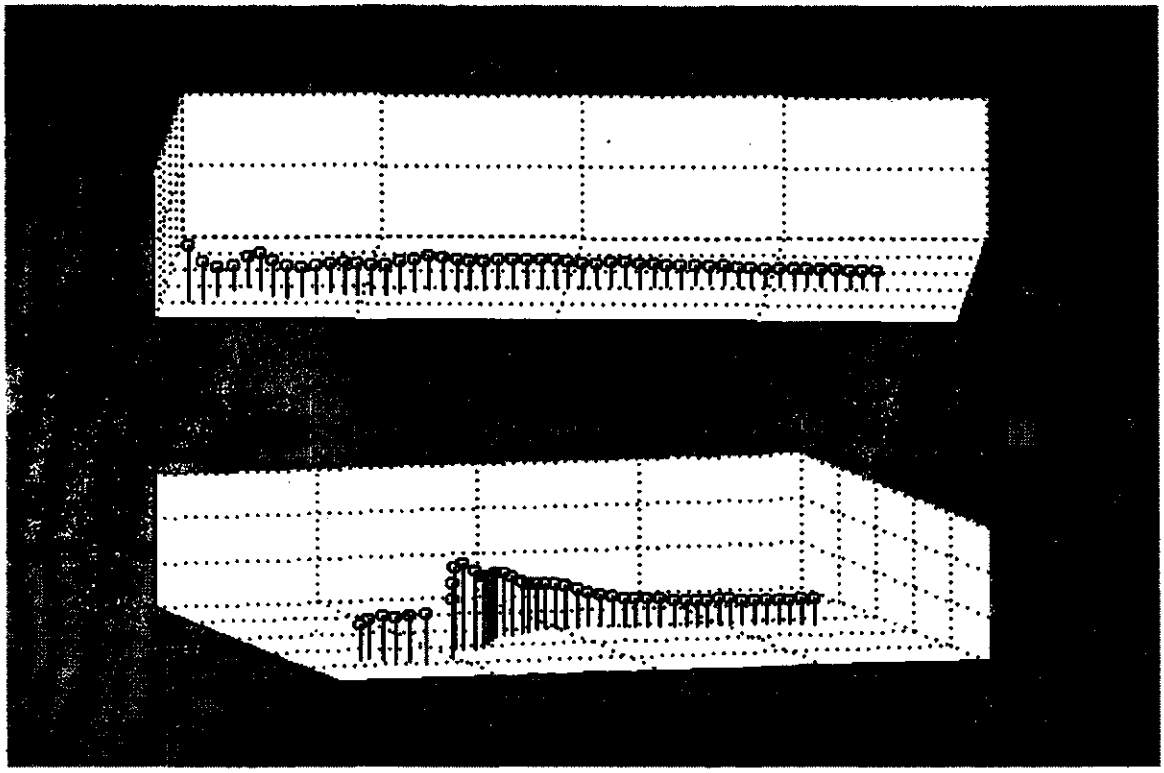


Figure 4.14. Plot of ct output waveforms on (a) 13.8 kV and (b) 230 kV sides of power transformer for a three-phase internal fault in 13.8 kV winding.

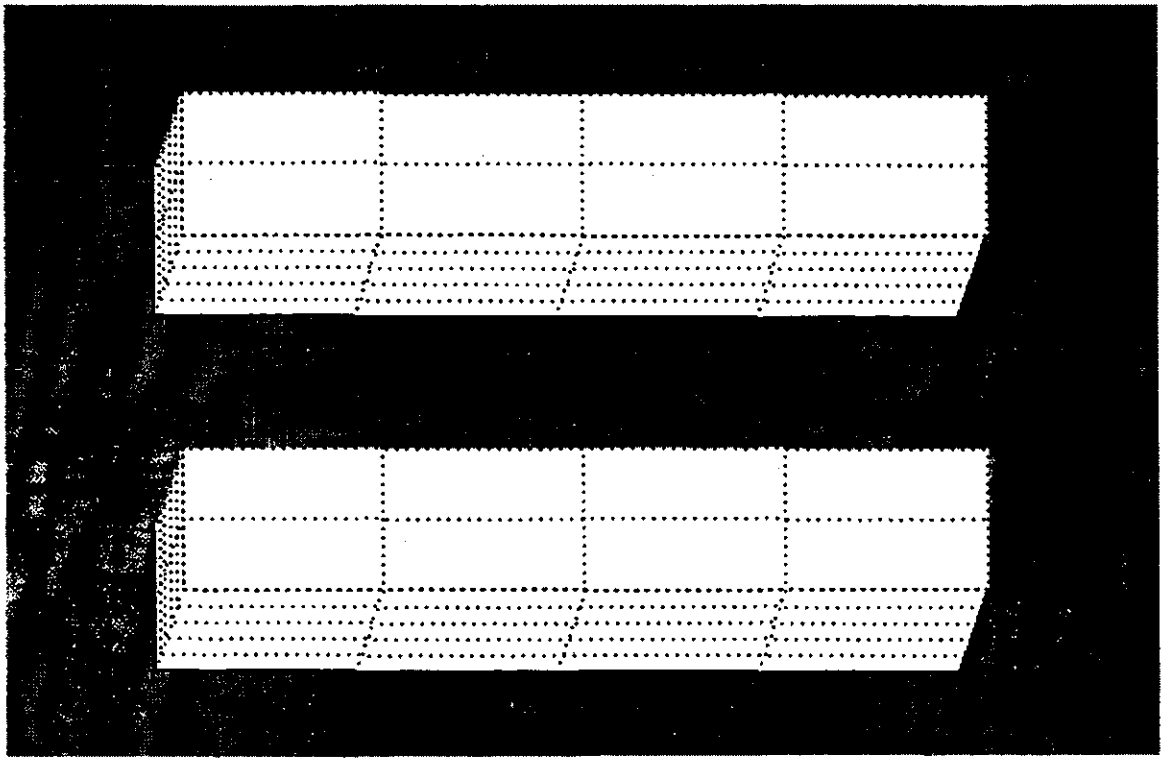
The computed sequence-impedances and trip counters are shown in Figure 4.15. The plots of trip counters show that the positive-sequence trip counter for the 13.8 kV side reached the threshold in 13 samples whereas the positive-sequence trip counter for the 230 kV side reached the threshold in 19 samples. The positive-sequence impedance seen from both sides lie in the third quadrant. This indicated that the fault is in the protection zone of the transformer. The logic initiated a trip after 19 samples. This is equivalent to an elapsed time of 13.2 ms. The results demonstrate that the algorithms works well even if the cts saturate.

4.5.2. Single phase-to-ground fault : Phase B

A single phase-to-ground fault involving Phase B was simulated at location 3 shown in Figure 4.1. Cts of ratio 840 were simulated on phases A and C of the 13.8 kV side. Ct of ratio 400 was simulated for Phase B on the same side. A burden resistance of 40.0 ohm was simulated for Phase B ct on the 13.8 kV side whereas cts of phases A and Phase C were simulated for a burden resistance of 0.5 ohm each. Cts of ratio 50 and burdens of 0.5 ohm resistance were simulated for all the phases on the 230 kV side. The fault was applied at 0.3 s. The waveforms of ct outputs are shown in Figure 4.16. These currents were processed by the algorithm. The computed sequence-impedances and trip counters are shown in Figure 4.17. The plots of trip counters show that the positive-sequence trip counter for the 13.8 kV side reached the threshold in 16 samples whereas the positive-sequence trip counter for the 230 kV side reached the threshold in 13 samples. Also, the positive-sequence impedances seen on 13.8 kV and 230 kV side lie in the third quadrant. The negative-sequence trip counters for 13.8 kV and 230 kV sides reached the threshold in 14 and 13 samples respectively. The negative-sequence impedances seen on both sides lie in the third quadrant. The location of sequence-impedances in the impedance plane led to the decision that the fault is inside the protection zone. The logic initiated a trip after 16 samples which is equivalent to an elapsed time of 11.1 ms. The results demonstrate that the algorithms perform well even if the cts saturate.

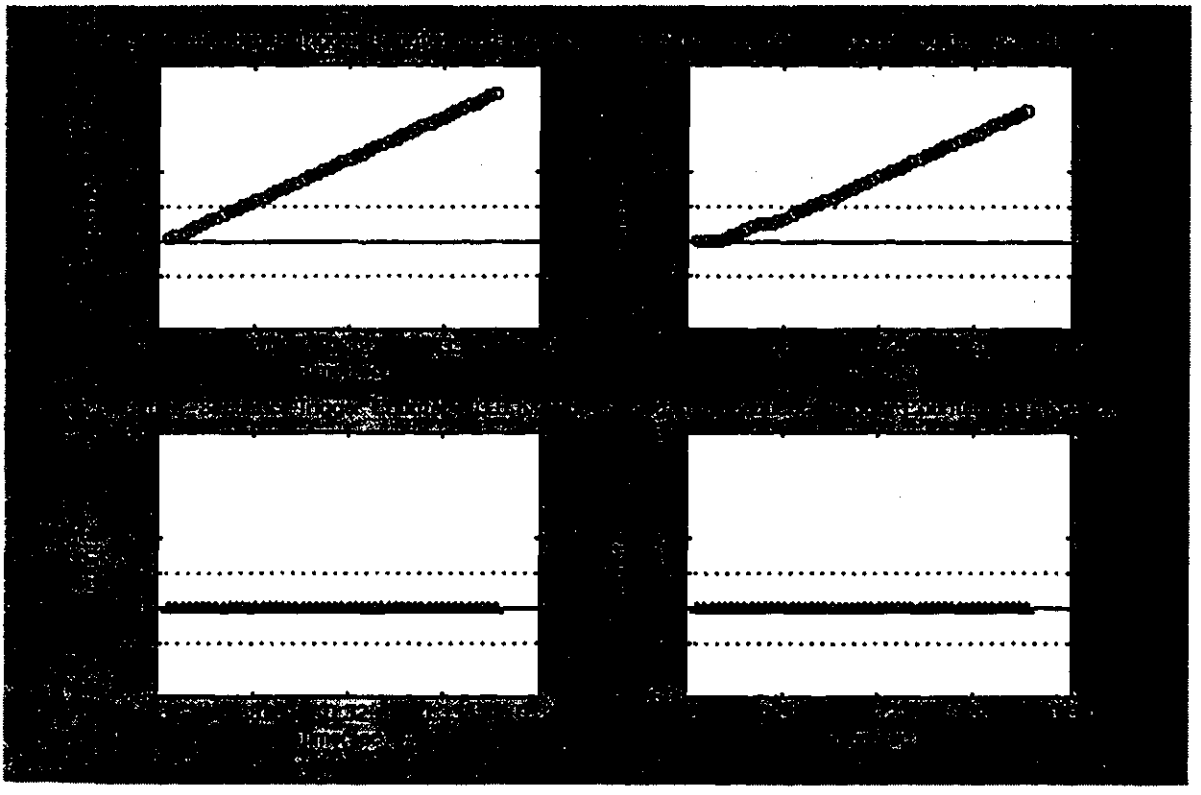


(a)



(b)

Figure 4.15. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a three-phase internal fault in the 13.8 kV winding of the power transformer (location 2, Figure 4.1).



(c)

Figure 4.15. Plot of (c) trip counters for a three-phase internal fault in the 13.8 kV winding (location 2, Figure 4.1).

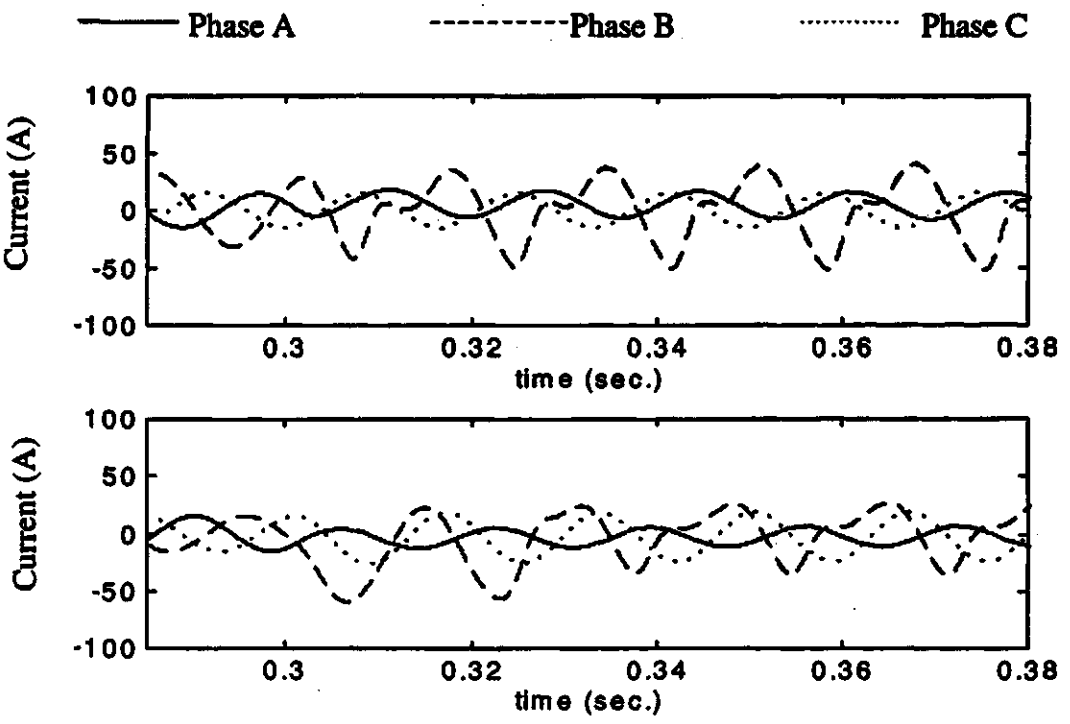
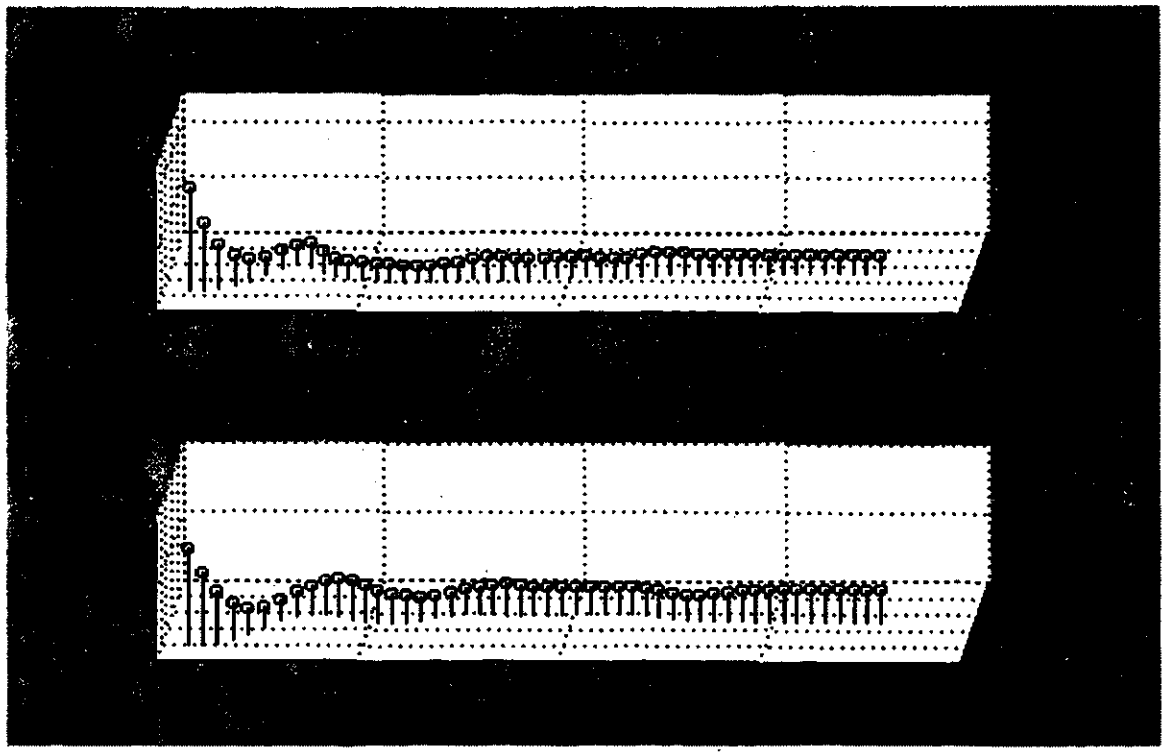
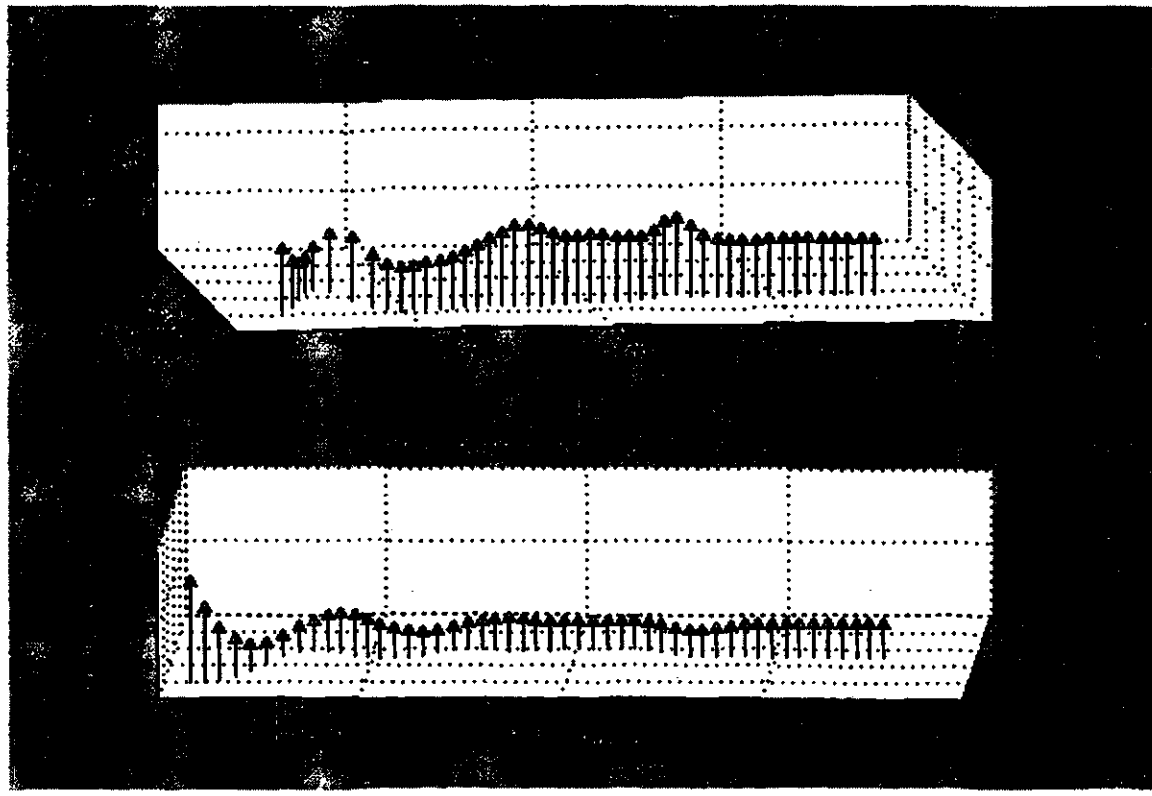


Figure 4.16. Plot of ct output waveforms on (a) 13.8 kV and (b) 230 kV sides of power transformer for B-ground internal fault in 230 kV winding.



(a)



(b)

Figure 4.17. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase B-ground internal fault in the 230 kV winding of the power transformer (location 3, Figure 4.1).

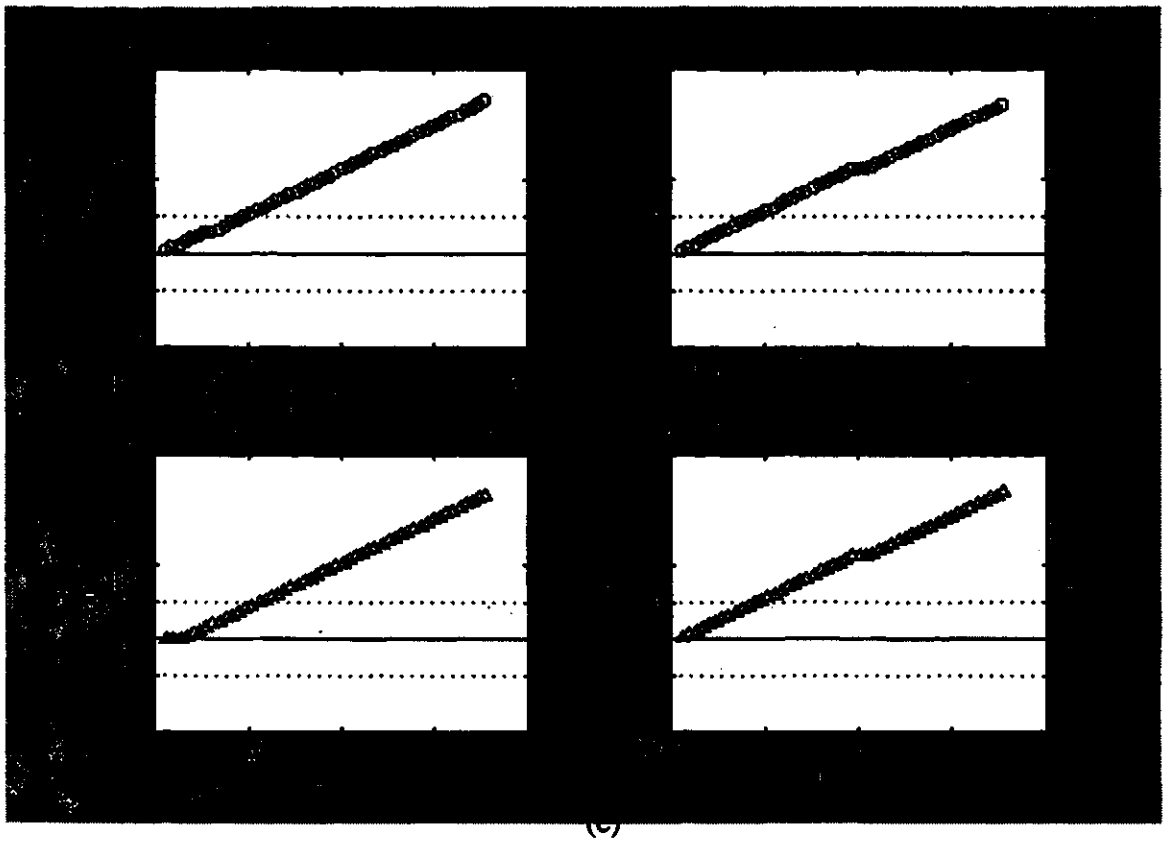


Figure 4.17. Plot of (c) trip counters for Phase B-ground internal fault in the 230 kV winding of the power transformer (location 3, Figure 4.1).

4.5.3. Two-phase fault : Phase A- Phase B

A two-phase fault, involving phases A and B was simulated at location 5 shown in Figure 4.1. Cts of ratio 840 were simulated for all phases on the 13.8 kV side whereas cts of ratio 50 were simulated for all phases on the 230 kV side. A burden of 40.0 ohm resistance each was simulated for phases A and B on the 13.8 kV side. The ct of phase C was simulated for a burden of 0.5 ohms resistance. On the 230 kV side, cts of phases A and B were simulated for a burden of 10 ohm resistance whereas the ct for phase C was simulated for a burden of 0.5 ohm resistance. The fault was applied at 0.3 seconds. The waveforms of ct outputs are shown in Figure 4.18. These currents were processed by the algorithm. The computed sequence-impedances and trip counters are shown in Figure 4.19. The positive-sequence and negative-sequence impedances seen on the 13.8

kV side lie in the third quadrant. The positive- and negative-sequence impedances computed on the 230 kV side are in the first quadrant. These conclusions led to the decision that the fault occurred outside the protection zone. The plots of trip counters show that the positive-sequence trip counters for both sides reached the threshold in 13 samples. The negative-sequence trip counter on the 13.8 kV side reached the threshold in 13 samples whereas the negative-sequence trip counter on the 230 kV reached the threshold in 15 samples. The trip-logic

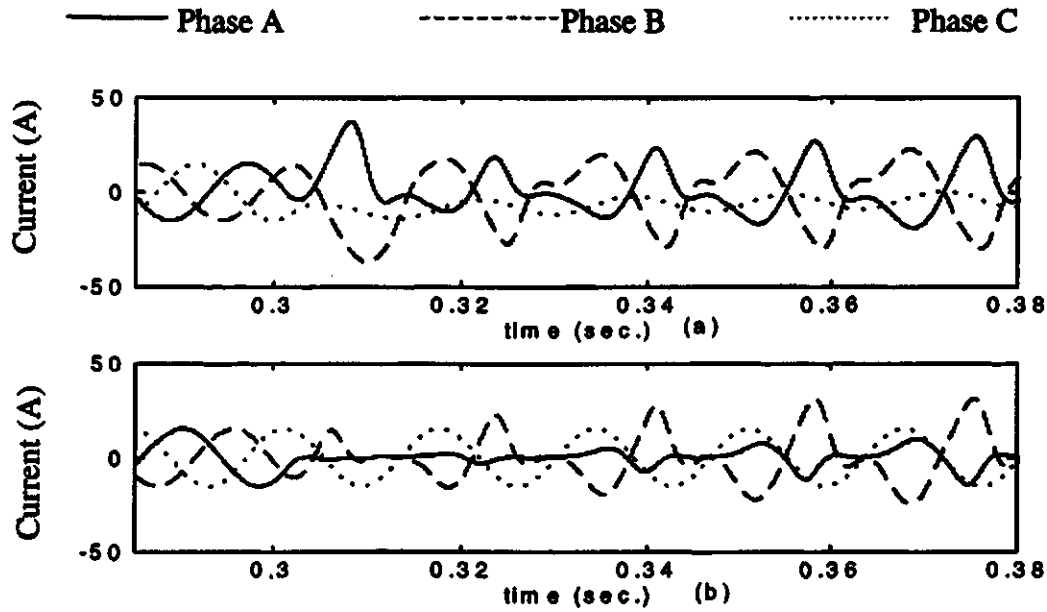
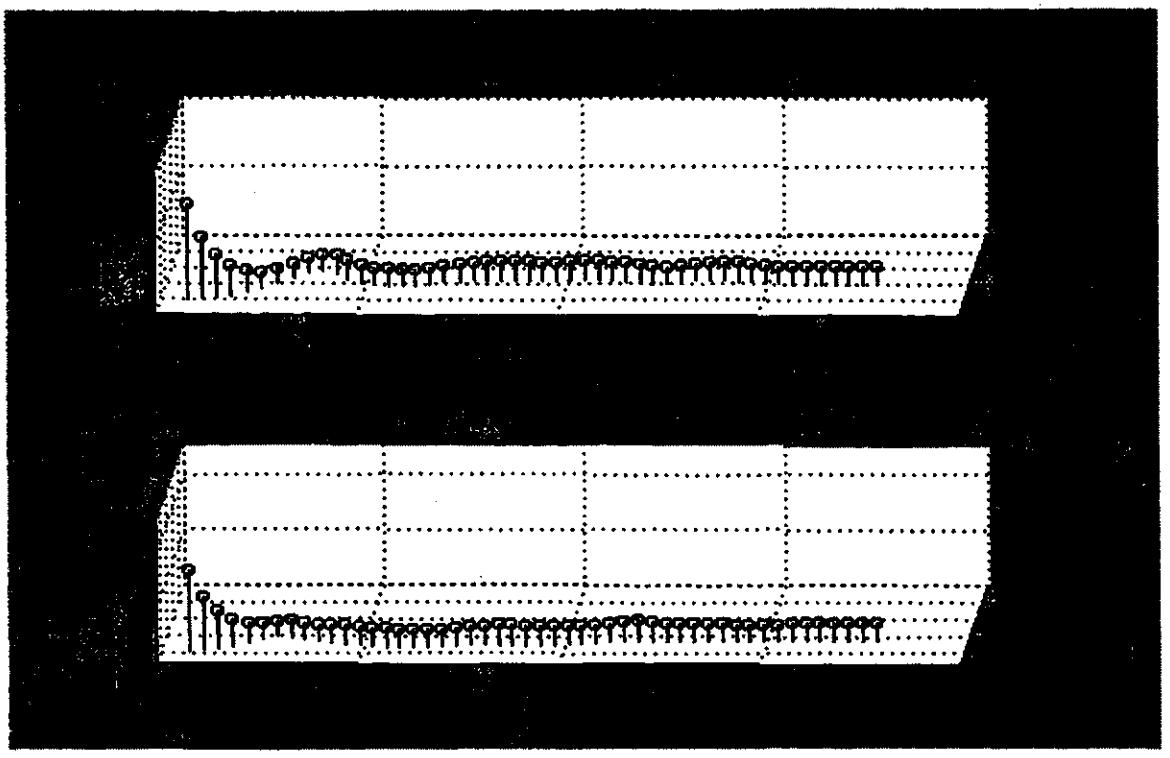


Figure 4.18. Plot of ct output waveforms on (a) 13.8 kV and (b) 230 kV sides of power transformer for Phase A - Phase B external fault on 230 kV side (location 5, Figure 4.1).

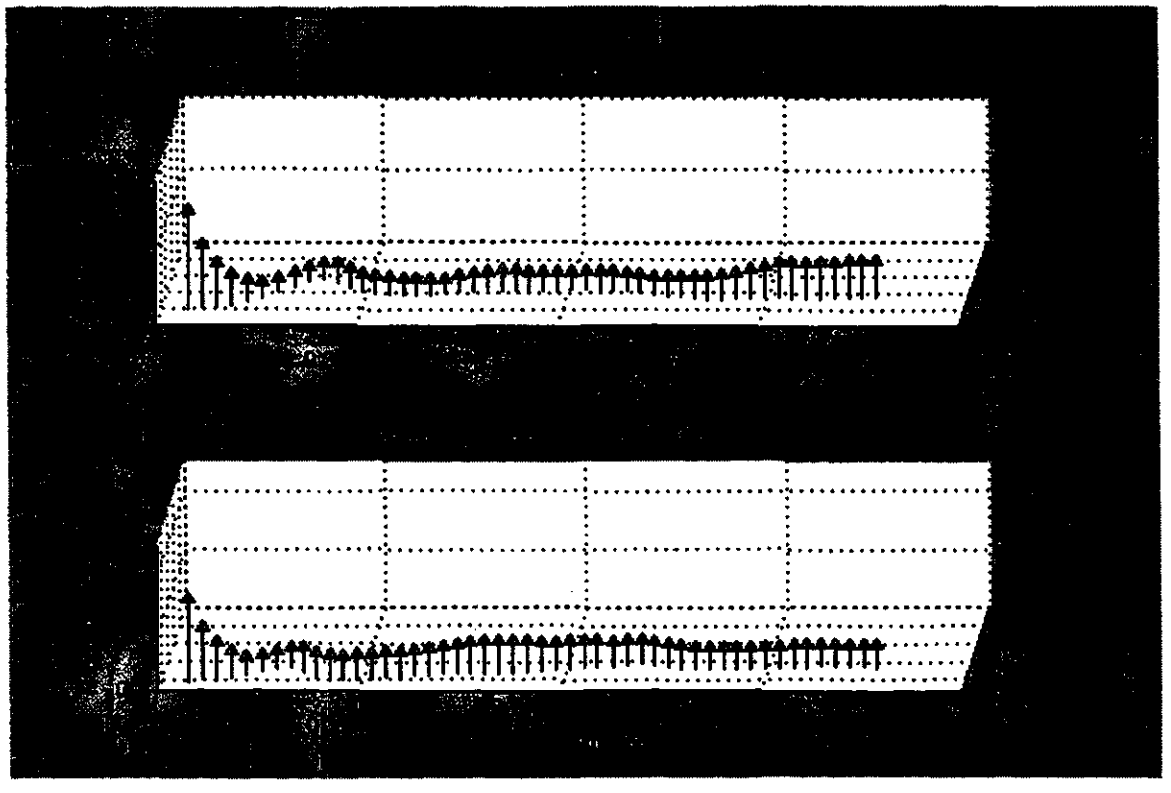
confirmed after 13 samples that the fault is outside the protection zone. This is equivalent to an elapsed time of 9.0 ms. The results demonstrate that the performance of the algorithm is stable even when the cts saturate.

4.5.4. Two-phase-to-ground fault : Phase A-Phase B-ground

A two-phase-to-ground fault, involving phases A and B, was simulated at location 4 shown in Figure 4.1. Cts of ratio 840 and 50 were simulated on the 13.8 kV and 230 kV sides respectively. Ct burden of 36.0 ohm resistance was simulated for the

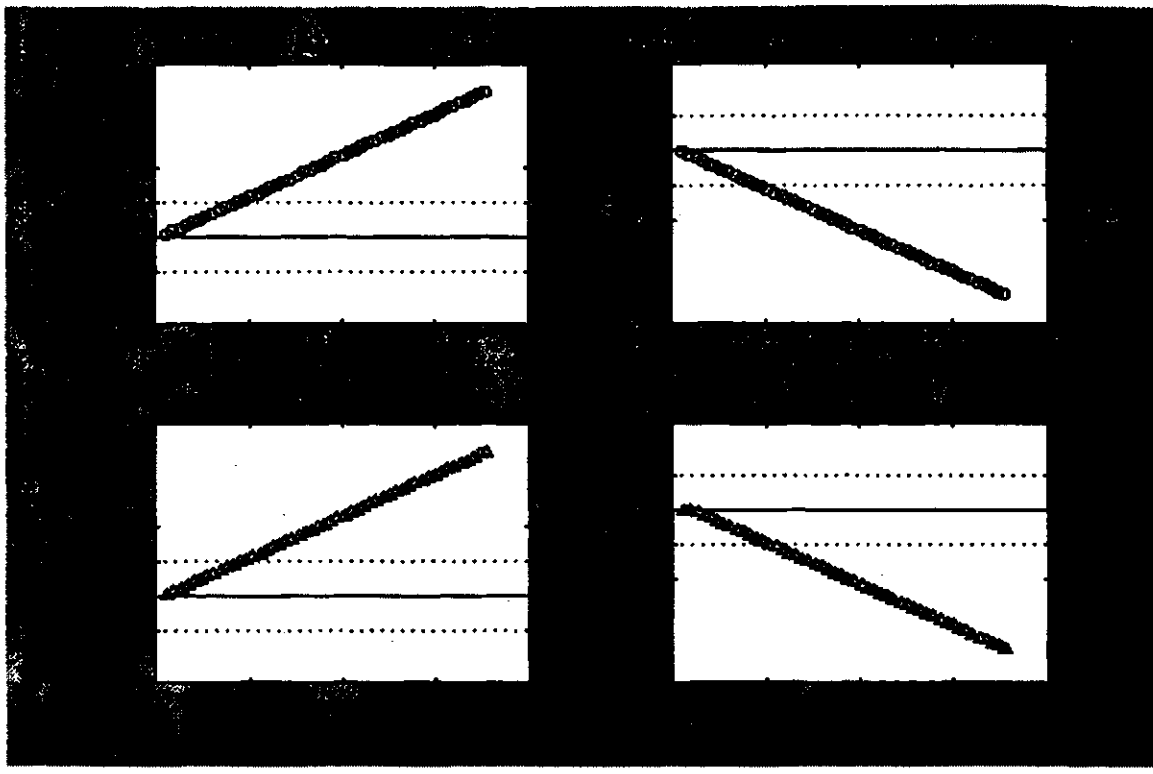


(a)



(b)

Figure 4.19. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B external fault on the 230 kV side of the power transformer (location 5, Figure 4.1).



(c)

Figure 4.19. Plot of (c) trip counters for Phase A-Phase B external fault on 230 kV side of the power transformer (Location 5, Figure 4.1).

Phase A on the 13.8 kV side whereas ct burdens of 0.5 ohm resistance each were simulated for the phases B and C. The ct burdens of 0.5 ohm resistance each were simulated for phases A and C on the 230 kV side whereas a ct burden of 8 ohm resistance was simulated for Phase B on this side. The fault was applied at 0.3 seconds. Figure 4.20 shows the waveforms of ct outputs. The computed sequence-impedances and trip counters are shown in Figure 4.21. The plots of trip counters show that the positive-sequence trip counter for both the relays reached the threshold in 13 samples. The positive-sequence impedance seen on the 13.8 kV side lies in the third quadrant whereas the positive-sequence impedance seen on the 230 kV side lies in the first quadrant. The negative-sequence trip counters on the 13.8 kV and 230 kV sides reached the threshold in 13 and 14 samples respectively. The negative-sequence impedances seen on the 13.8 kV and 230 kV side lie in same quadrants as their positive-sequence counterparts. The respective locations of sequence-impedances led to the conclusion

that the fault is outside the transformer protection zone. The trip-logic confirmed the fault after 13 samples. This is equivalent to an elapsed time of 9.0 ms. The results demonstrate that the performance of the algorithm is stable even when the cts saturate.

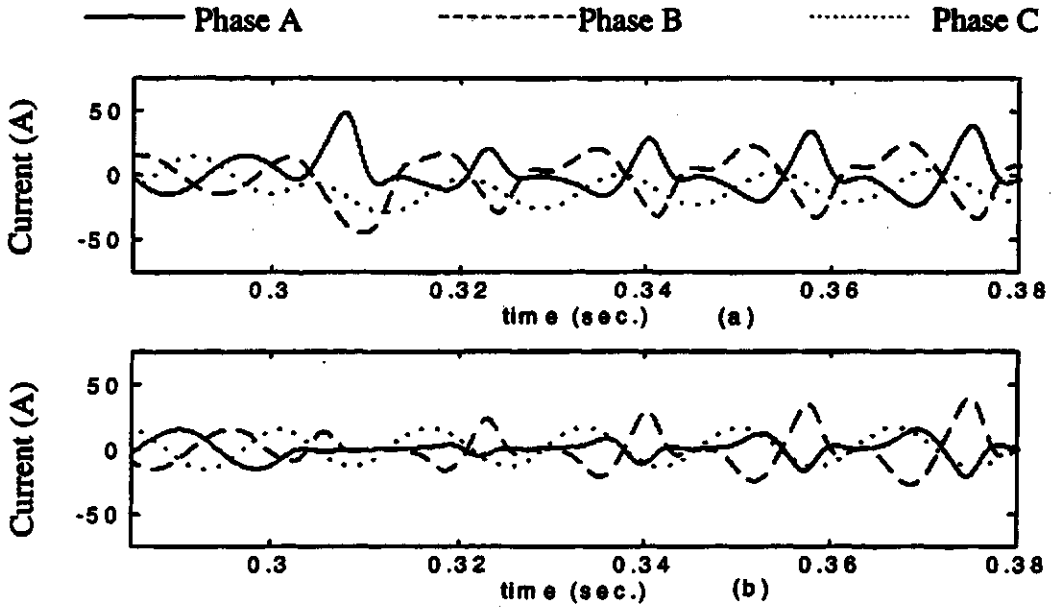


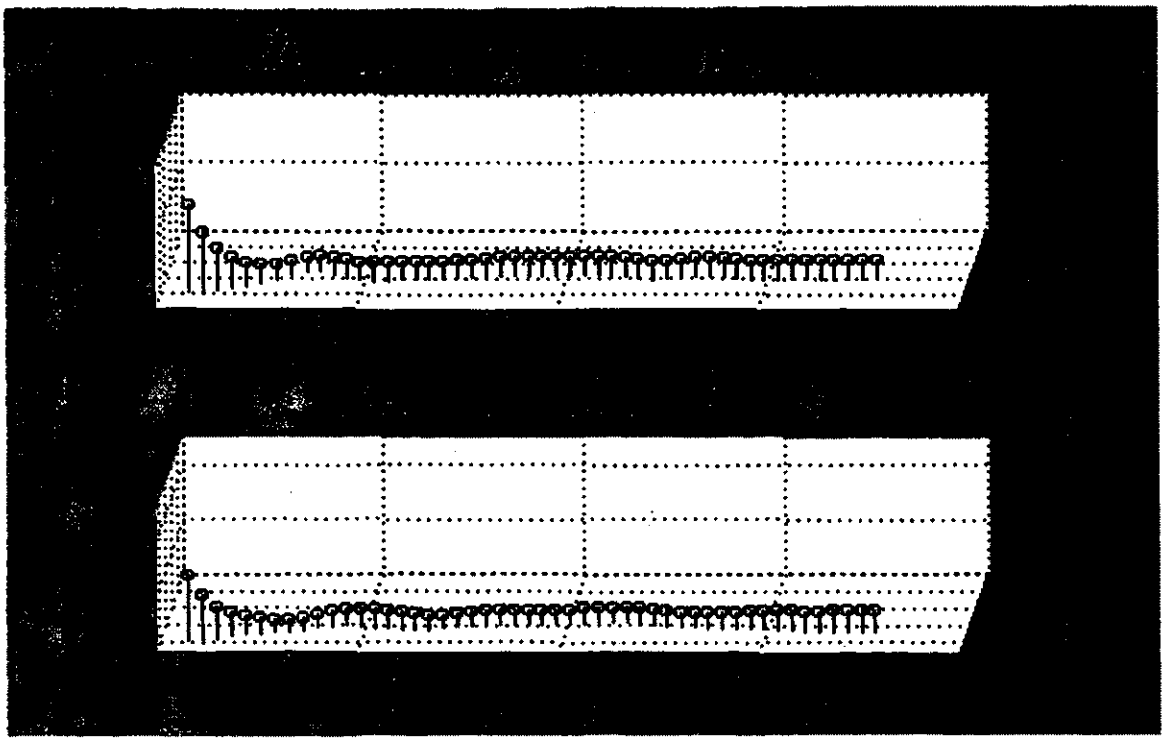
Figure 4.20. Plot of ct output waveforms on (a) 13.8 kV and (b) 230 kV sides of power transformer for Phase A - Phase B-ground external fault on 230 kV side (location 4, Figure 4.1).

4.6. Faults in unloaded transformers

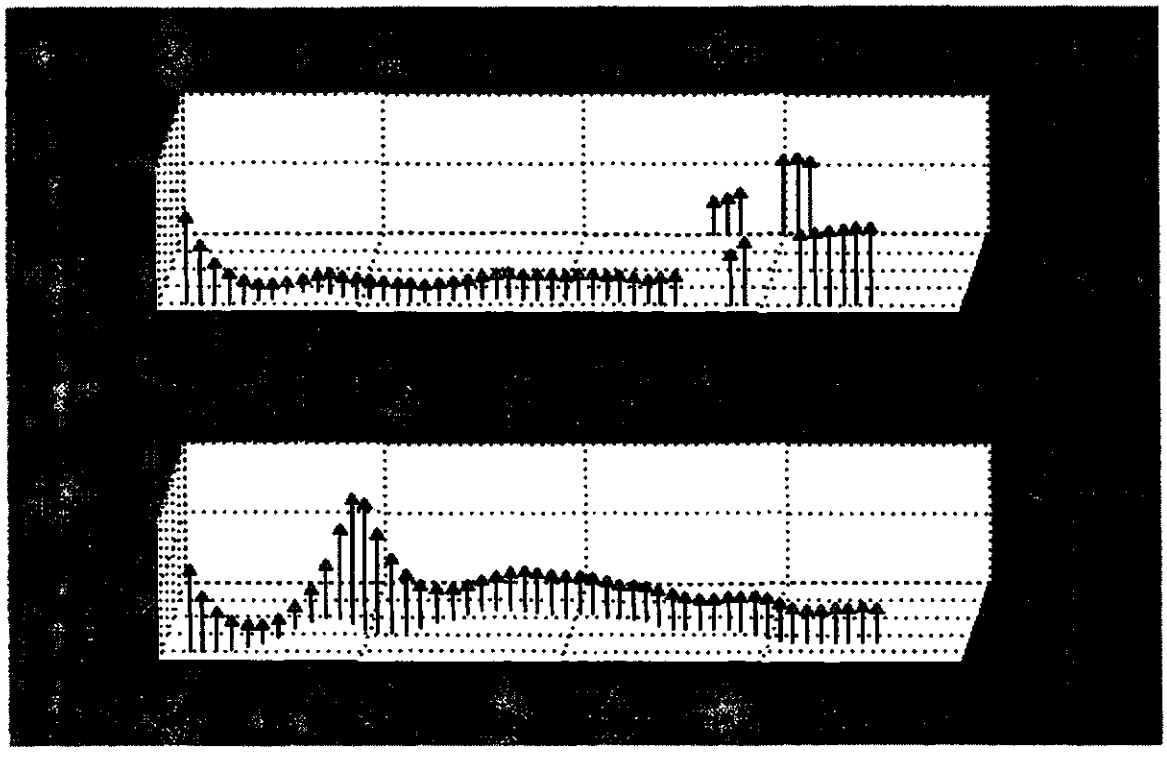
The algorithm developed in Section 3.3 for detecting faults in unloaded transformers was tested with simulation data. Two test cases are presented in this section. Additional results are given in Appendix E.

4.6.1. Three-phase (internal) fault

A three-phase fault was simulated at location B shown in Figure 3.6. The fault was initiated at 0.3 s. The detection of the inception of the fault took the first two samples, after which the positive-sequence impedance on the 13.8 kV side is calculated using the incremental voltage and current. Since there are no currents in the lines on the 230 kV side, no calculations were performed for that side. Figure 4.22 shows the plots of

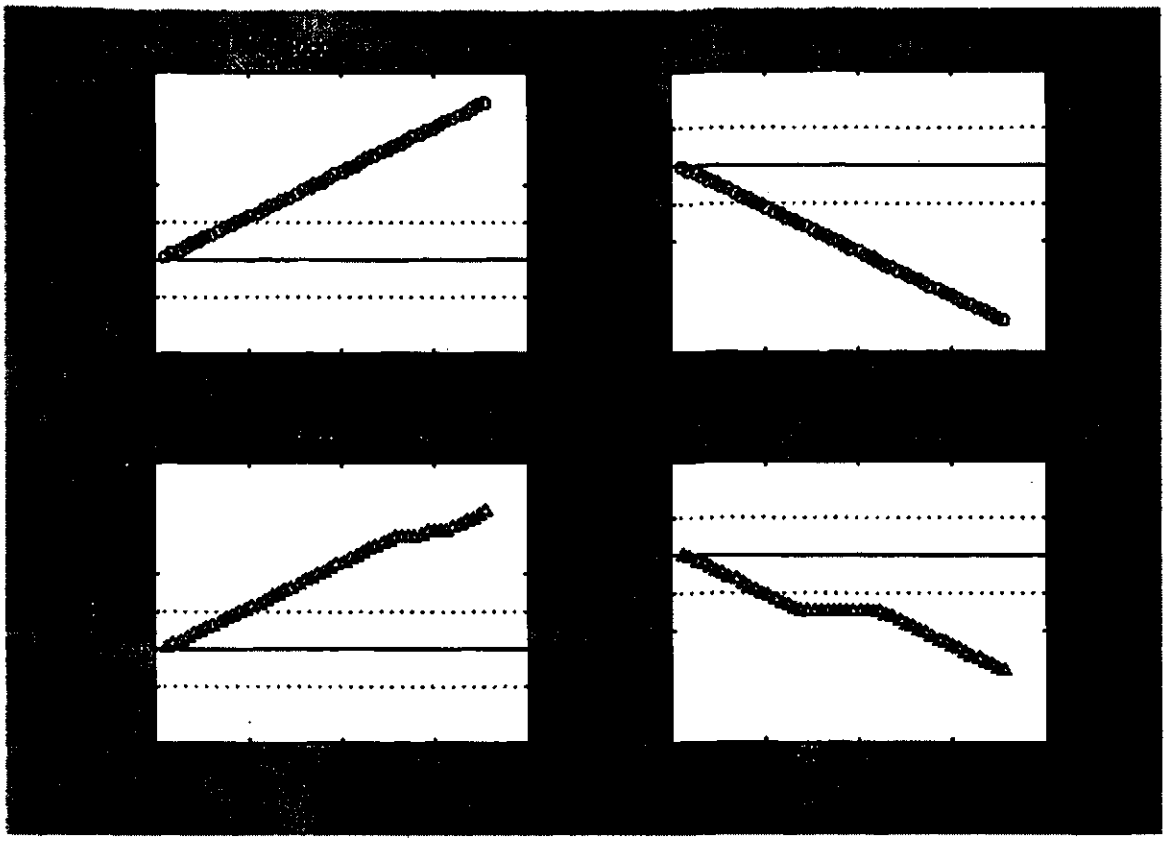


(a)



(b)

Figure 4.21. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B-ground external fault on the 230 kV side of the power transformer (location 4, Figure 4.1).



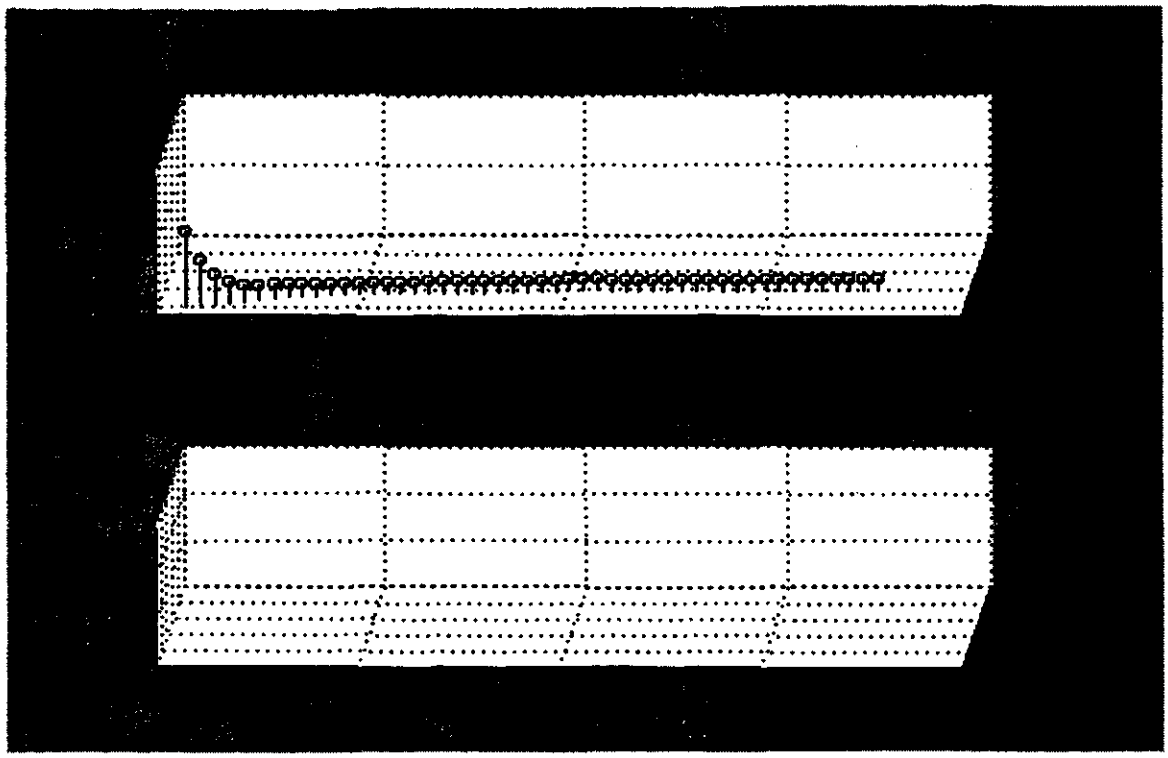
(c)

Figure 4.21. Plot of (c) trip counters for Phase A-Phase B-ground external fault on 230 kV side of the power transformer (location 4, Figure 4.1).

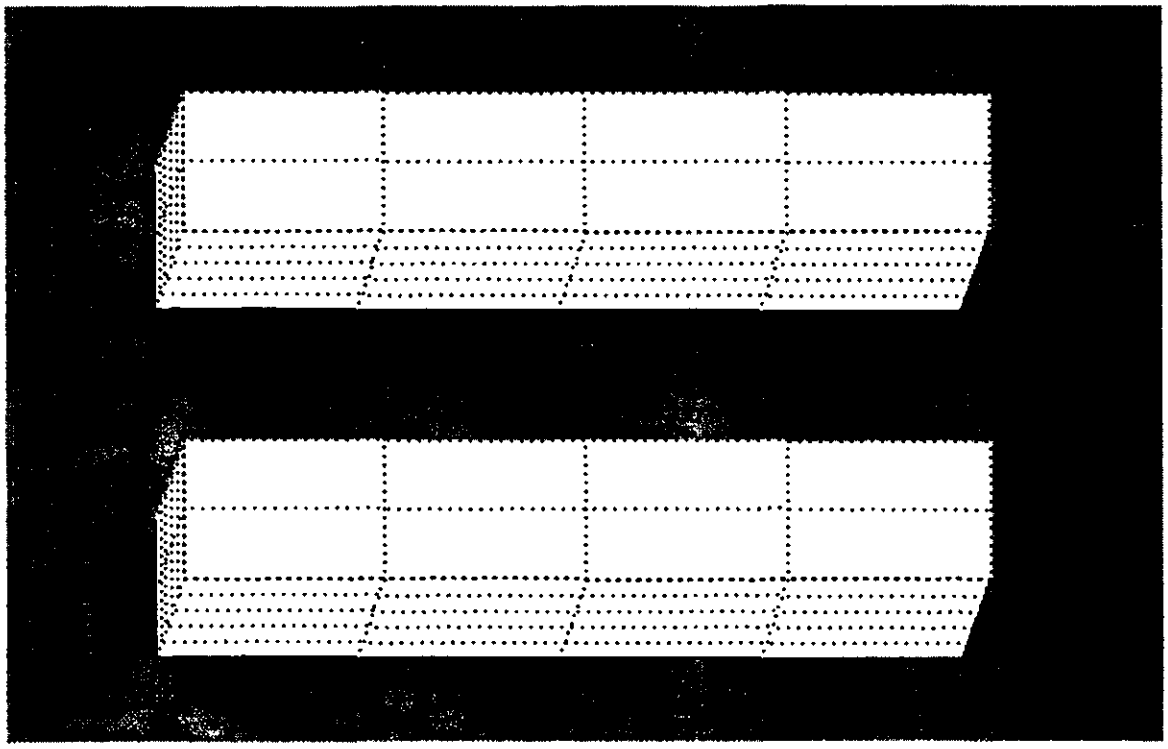
the sequence-impedances and the trip counters. For this case, the positive-sequence sequence computed on the 13.8 kV side lies in the third quadrant. This indicates that the fault is in front of the relay of the 13.8 kV side. Since there is no computation from on the 230 kV side due to lack of current, it was concluded that the fault occurred in the protection zone of the transformer. It took the algorithm 9.0 ms. to detect the fault. As no negative-sequence voltages and currents are experienced during a three-phase fault, hence, no conclusions could be generated from these signals.

4.6.2. Two-phase (external) fault : Phase B - Phase C

A two-phase fault involving phases B and C was simulated at location A shown in Figure 3.6. The fault was applied at 0.3 s. and the detection of its inception took the first two samples. After this delay, the sequence-impedances were computed on the 13.8 kV

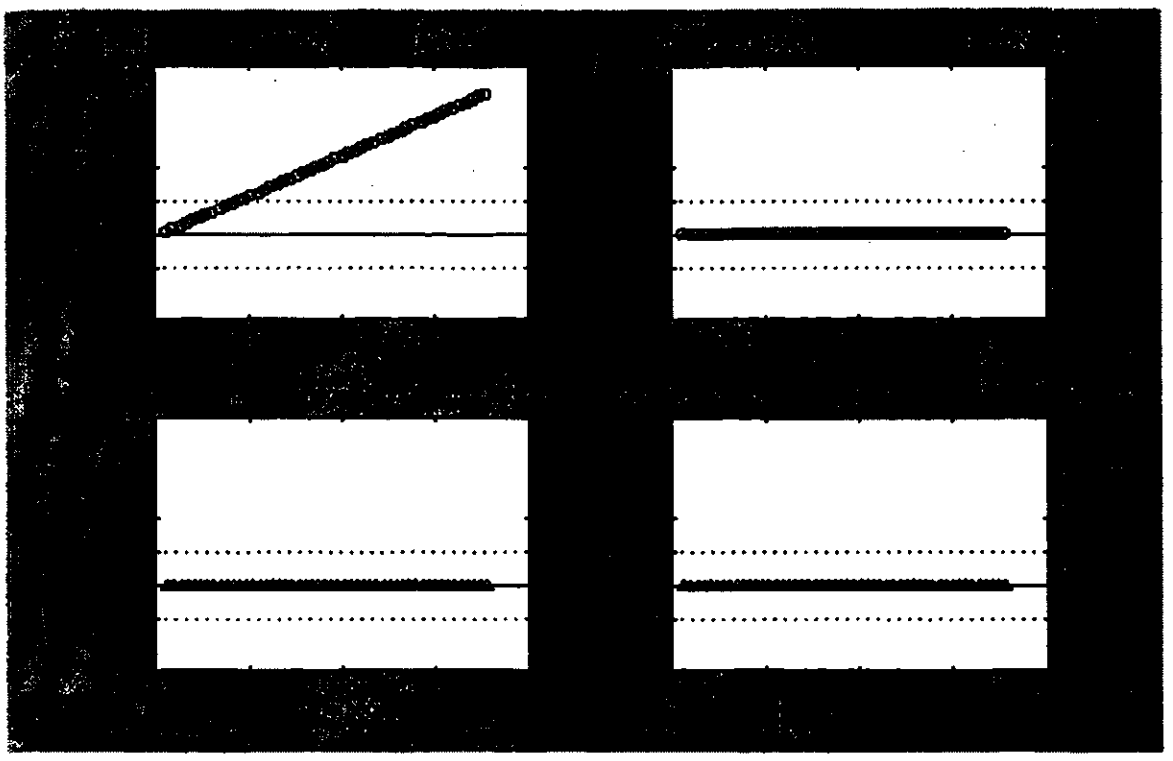


(a)



(b)

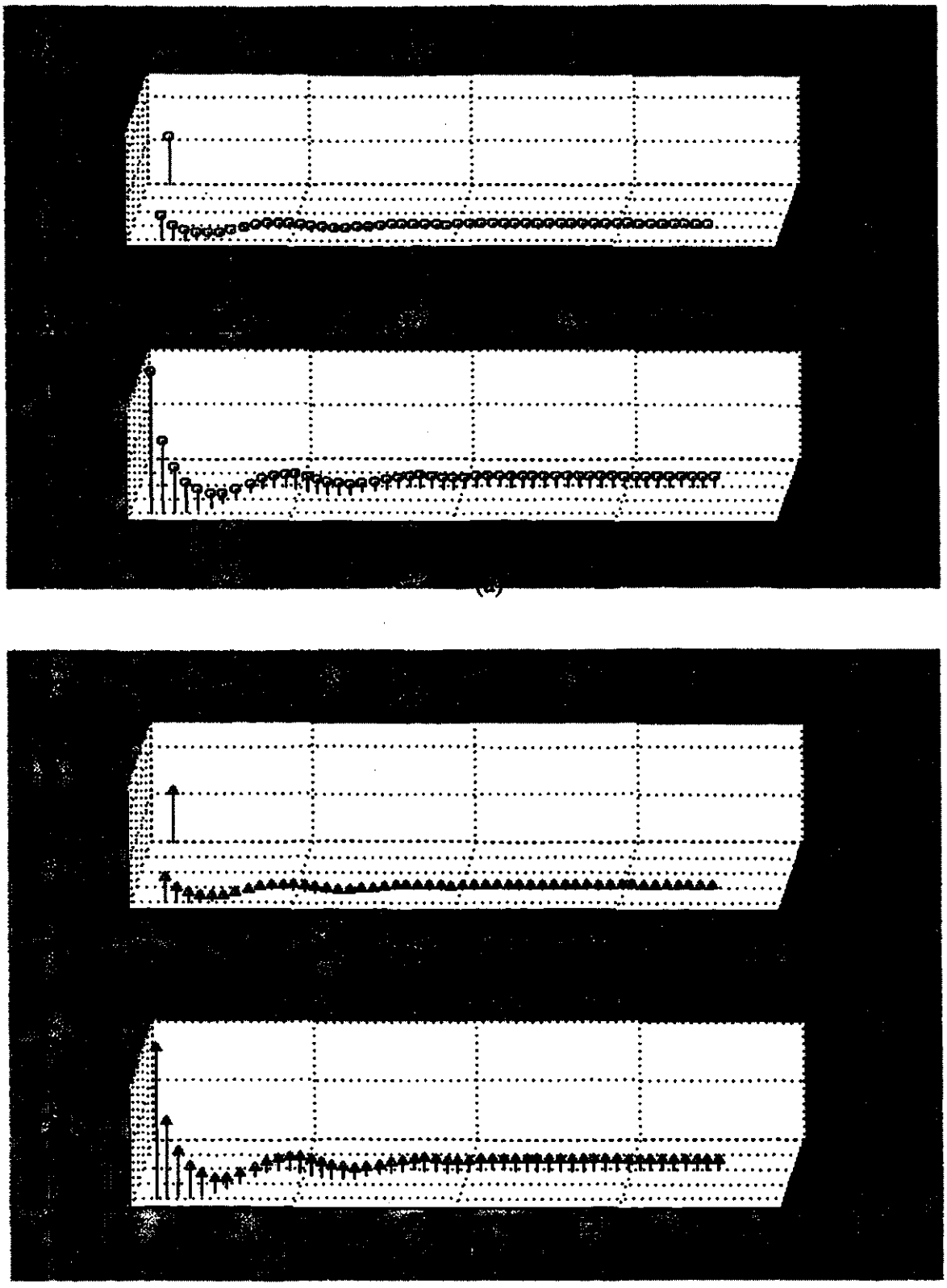
Figure 4.22. Plot of (a) positive-sequence and (b) negative-sequence impedances on 13.8 kV and 230 kV sides of the unloaded transformer for a three-phase fault in the 230 kV side.



(c)

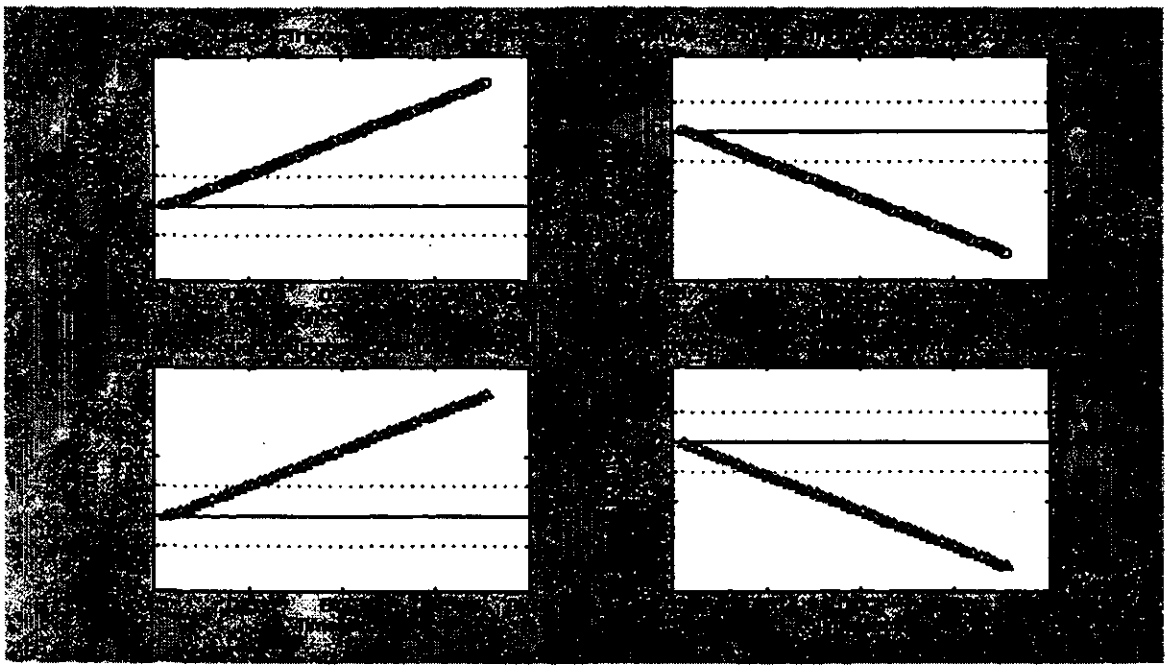
Figure 4.22. Plot of trip counters on the 13.8 kV and 230 kV sides of the unloaded transformer for a three-phase fault in the 230 kV side.

and 230 kV sides. The values of the sequence-impedances (in polar form) are shown in Figures 4.23 (a) and (b). The profiles of the trip counters are shown in Figure 4.23(c). For this case, the positive-sequence and the negative-sequence impedances computed on the 13.8 kV side lie in the third quadrant. The positive-sequence and negative-sequence impedances on the 230 kV side are in the first quadrant. These conclusions led to the decision that the fault is outside the protection zone of the transformer. The positive-sequence trip counters on both the sides reached the threshold in 14 samples. The negative-sequence trip counter of 13.8 kV side reached the threshold in 14 samples whereas the negative-sequence trip counter of the 230 kV side reached the threshold in 13 samples. It took the algorithm 9.0 ms. to detect the fault.



(b)

Figure 4.23. Plot of (a) positive-sequence and (b) negative-sequence impedances on 13.8 kV and 230 kV sides of the unloaded transformer for a Phase B - Phase C fault on the 230 kV side.



(c)

Figure 4.23. Plot of trip counters on the 13.8 kV and 230 kV sides of the unloaded transformer for a Phase B - Phase C fault on the 230 kV side.

4.7. High-impedance faults

Several high-impedance faults were simulated and the proposed algorithm was tested with the data provided by the simulations. Selected test cases are presented in this section.

4.7.1. Single phase-to-ground (external) fault : Phase A

A single phase-to-ground fault involving Phase A was simulated at location 5 shown in Figure 4.1. A fault resistance of 10 ohms was used. The fault was initiated at 0.3 s. The unfiltered and filtered voltage and current waveforms are shown in Figures 4.24 and 4.25 respectively. The detection of the inception of the fault took the first two samples after which the positive- and negative-sequence impedances are computed using the incremental voltages and currents. The values of the sequence impedances (in polar form) are shown in Figures 4.26 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.26(c). For this case, the positive- and

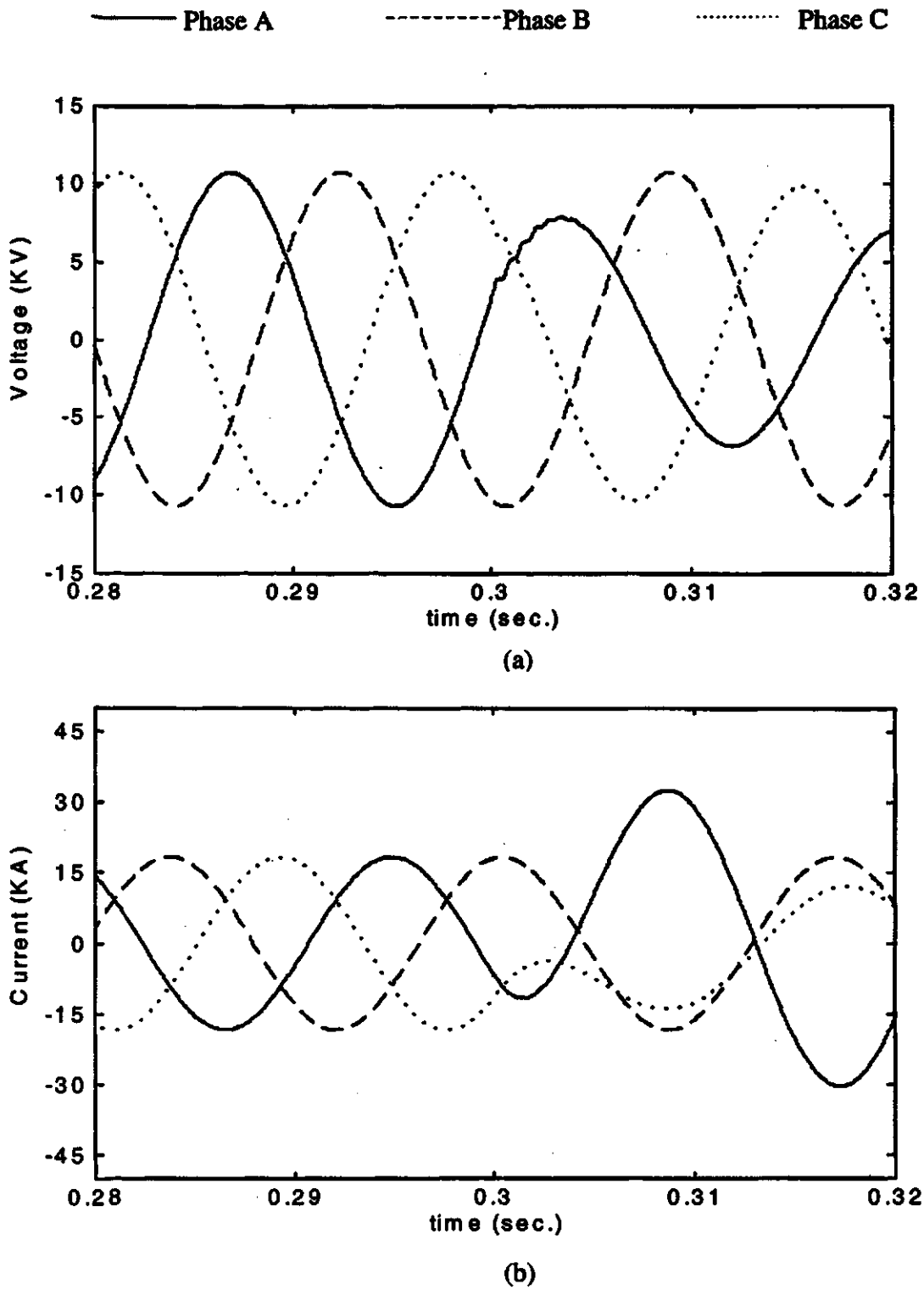
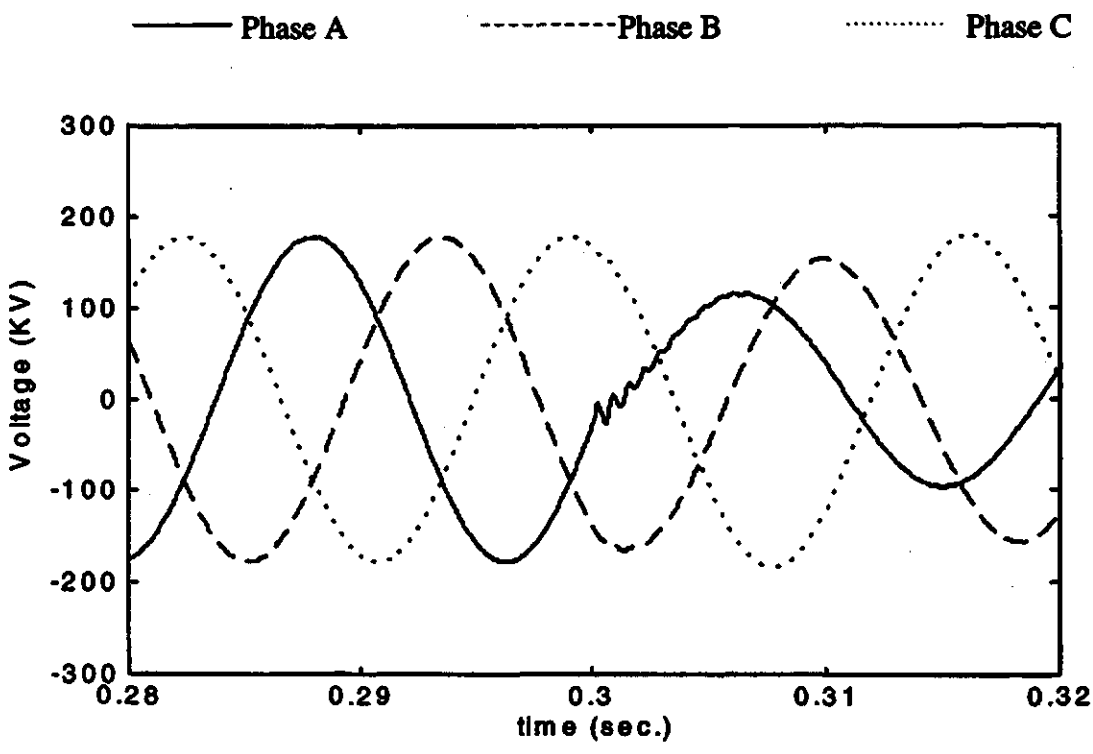
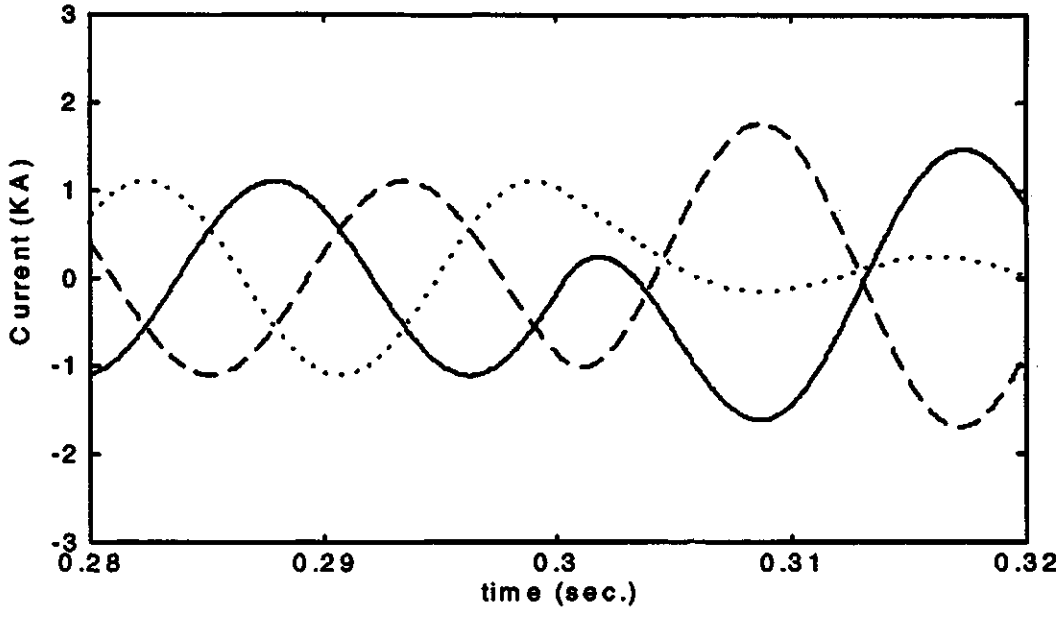


Figure 4.24. Unfiltered (a) voltage and (b) current waveforms on the 13.8 kV side of power transformer for Phase A-ground external fault on 230 kV side (location 5, Figure 4.1).



(c)



(d)

Figure 4.24(contd.). Unfiltered (a) voltage and (b) current waveforms on the 230 kV side of power transformer for Phase A-ground external fault on 230 kV side (location 5, Figure 4.1).

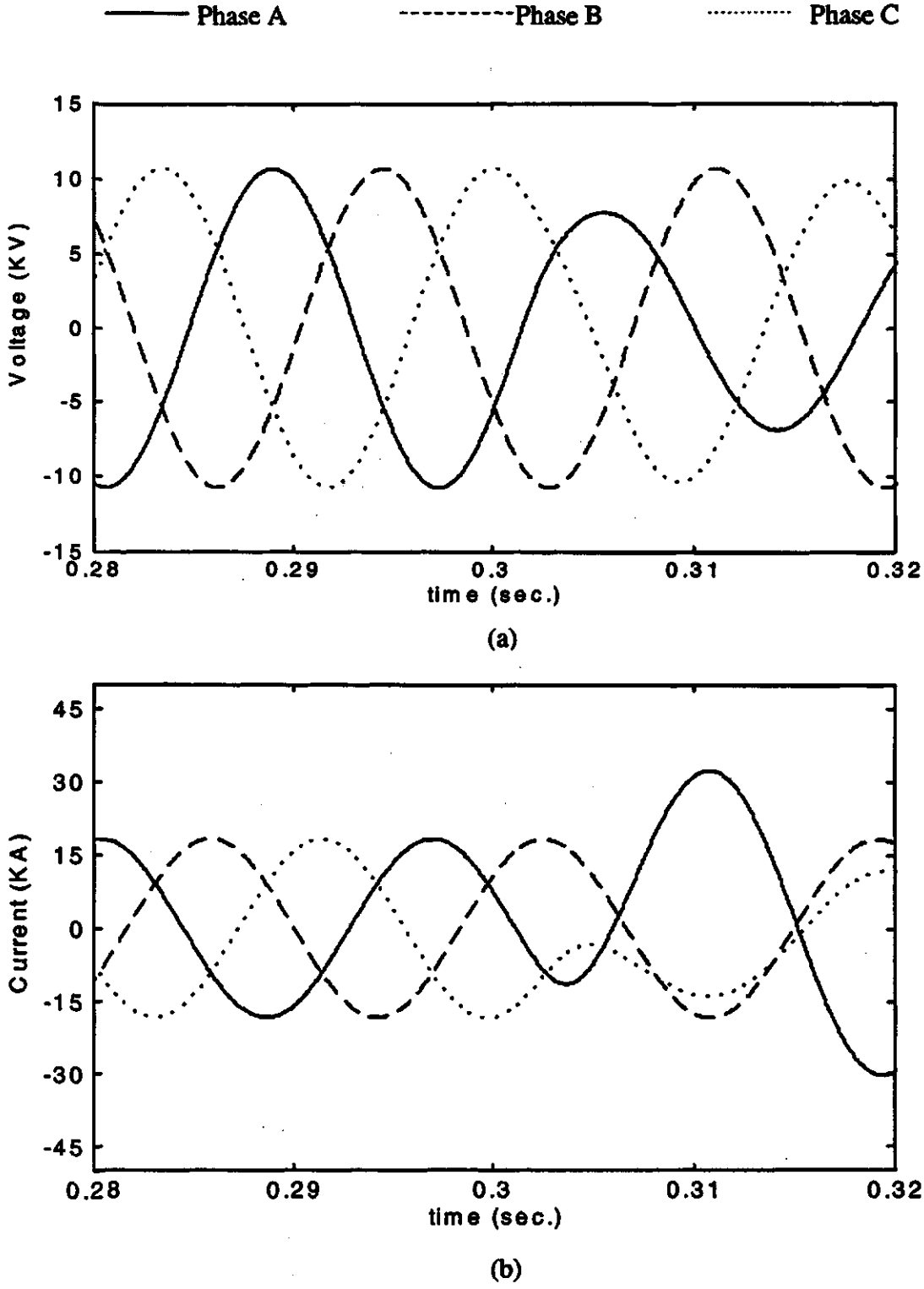


Figure 4.25. Filtered (a) voltage and (b) current waveforms on the 13.8 kV side of power transformer for Phase A-ground external fault on 230 kV side (location 5, Figure 4.1).

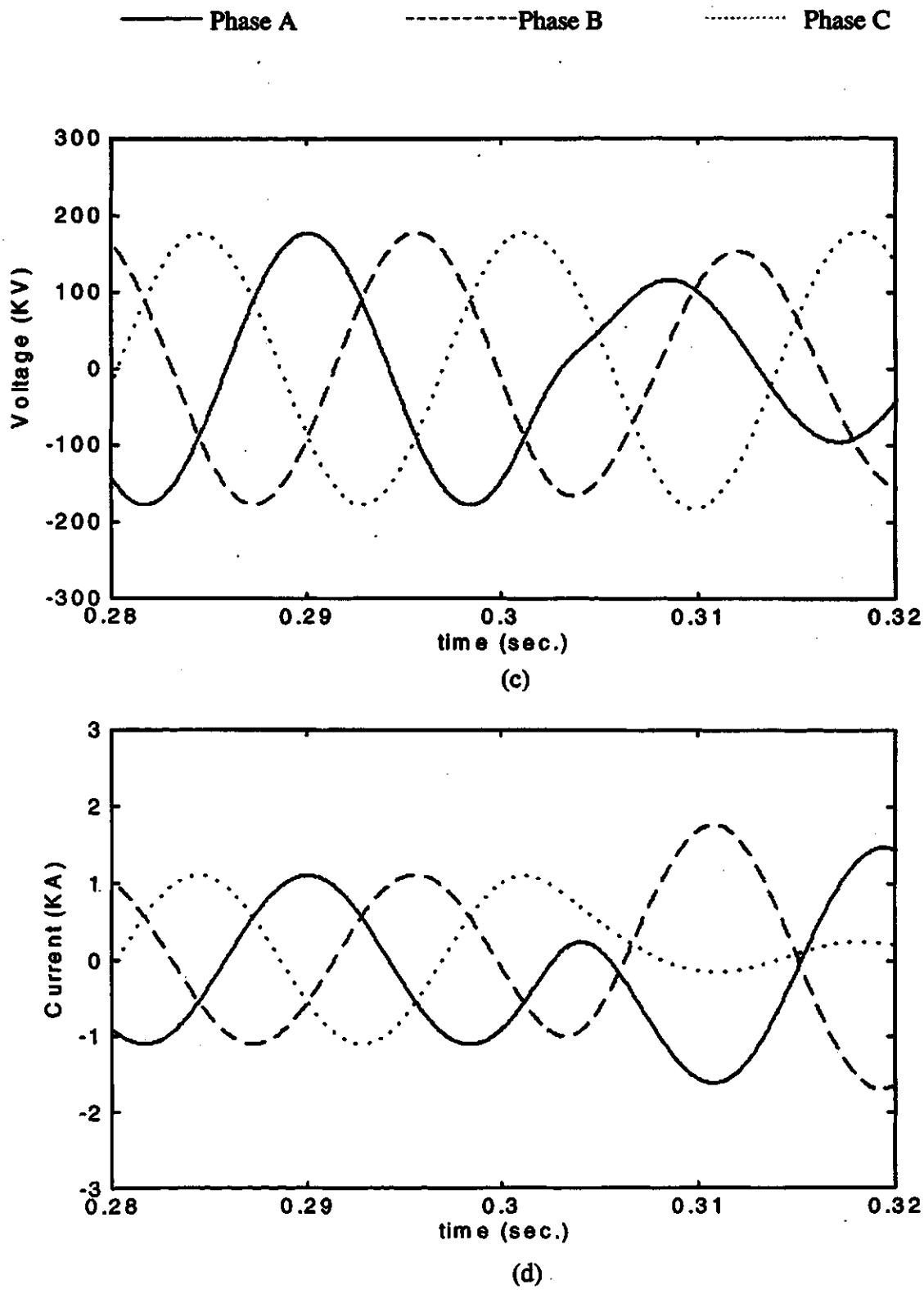
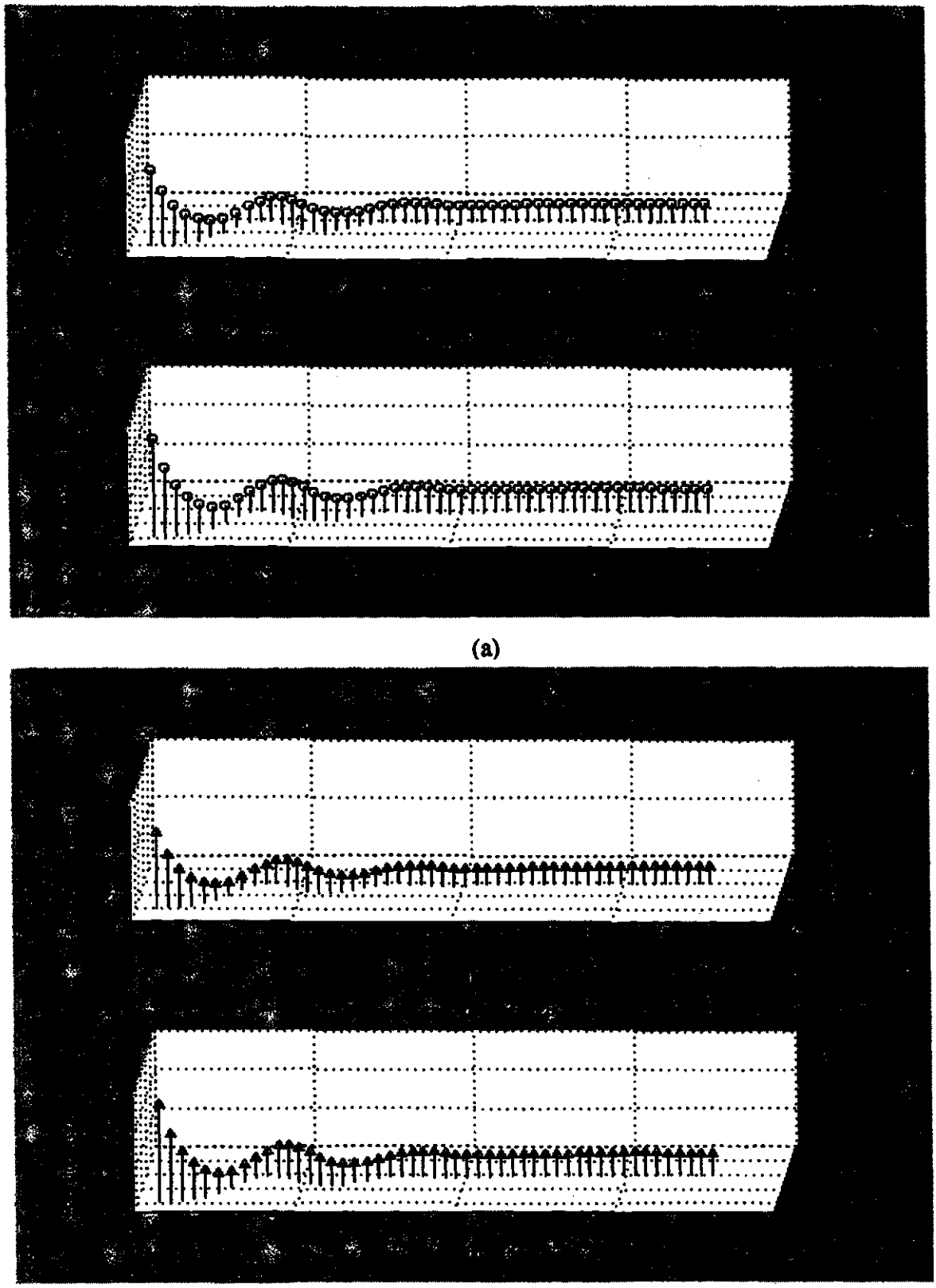


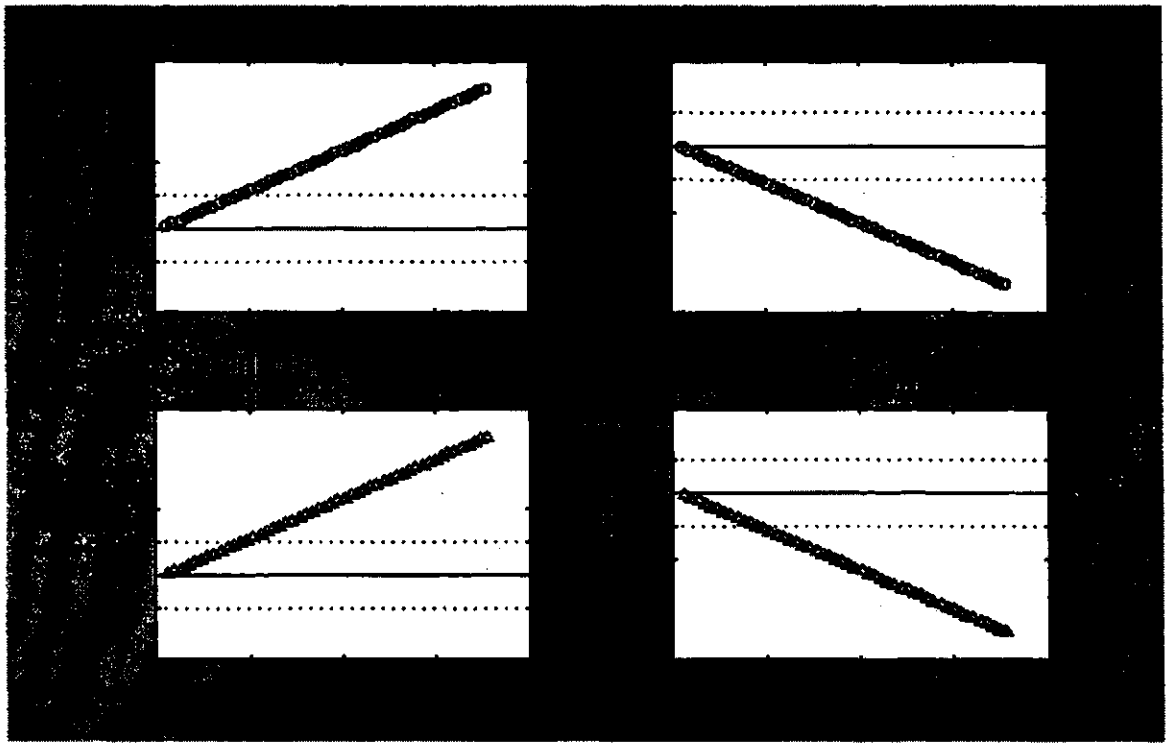
Figure 4.25(contd.). Filtered (c) voltage and (d) current waveforms on the 230 kV side of power transformer for Phase A-ground external fault on 230 kV side (location 5, Figure 4.1).



(a)

(b)

Figure 4.26. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground external fault on the 230 kV side of the power transformer



(c)

Figure 4.26. Plot of (c) trip counters for a high-impedance Phase A-ground external fault on 230 kV side of the power transformer (location 5, Figure 4.1).

negative-sequence impedances computed on the 13.8 kV side of the power transformer were in the third quadrant. The positive- and negative-sequence impedances computed on the 230 kV side lie in the first quadrant. These conclusions led to the decision that the fault is outside the protection zone. The positive-sequence and negative-sequence trip counters of 13.8 kV and 230 kV sides reached the pre-defined threshold in 13 samples when the trip-logic confirmed that the fault is outside the protection zone. It took 9.0 ms to make the final decision in this case.

4.7.2. Single phase-to-ground (internal) fault : Phase B

A single phase-to-ground internal fault involving Phase B was simulated at location 2 shown in Figure 4.1. A fault resistance of 1 ohm was used. The fault was initiated at 0.3 s. The unfiltered and filtered voltage and current waveforms are shown in Figures 4.27 and 4.28 respectively. The algorithm took two samples to detect the

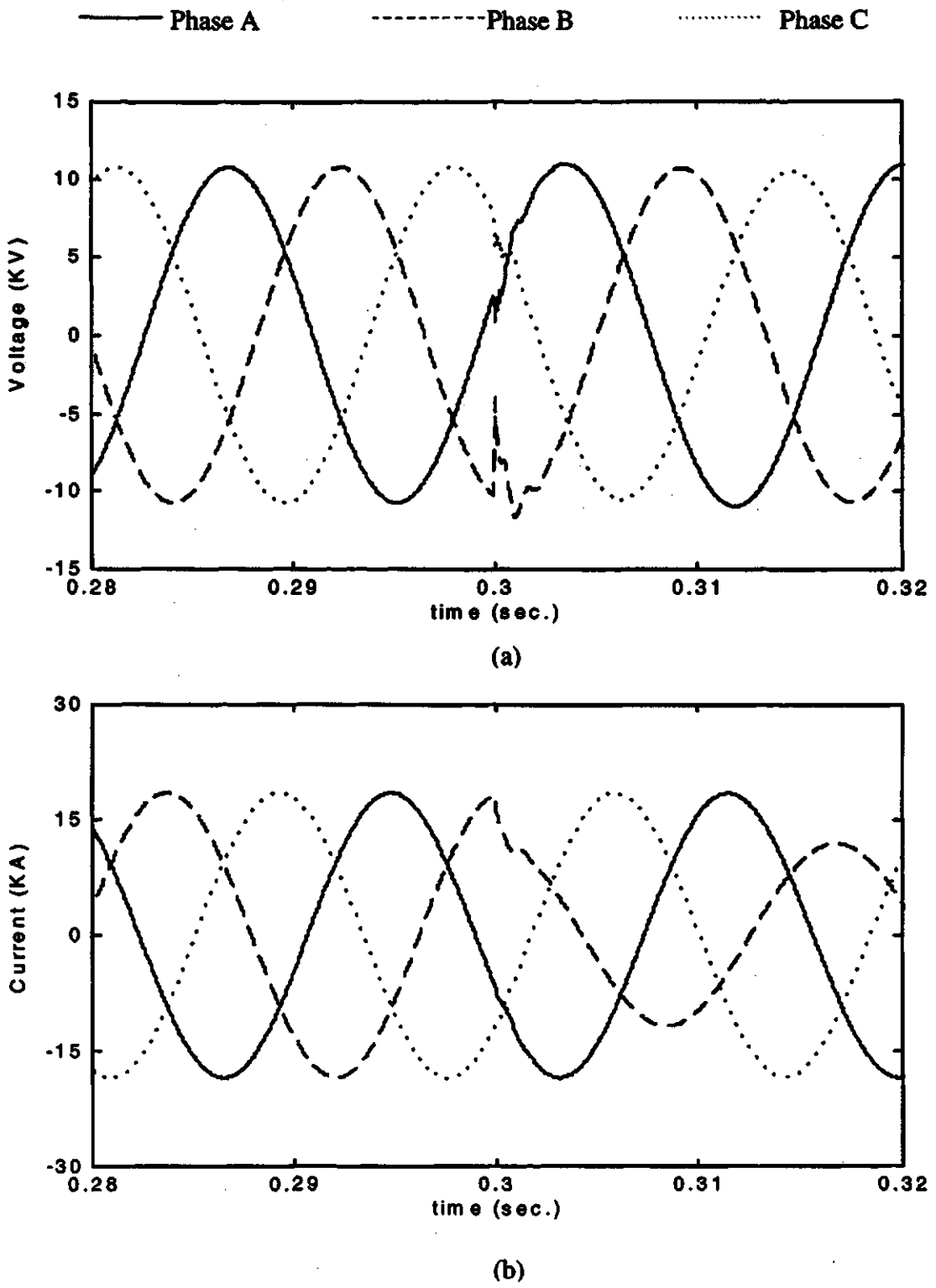
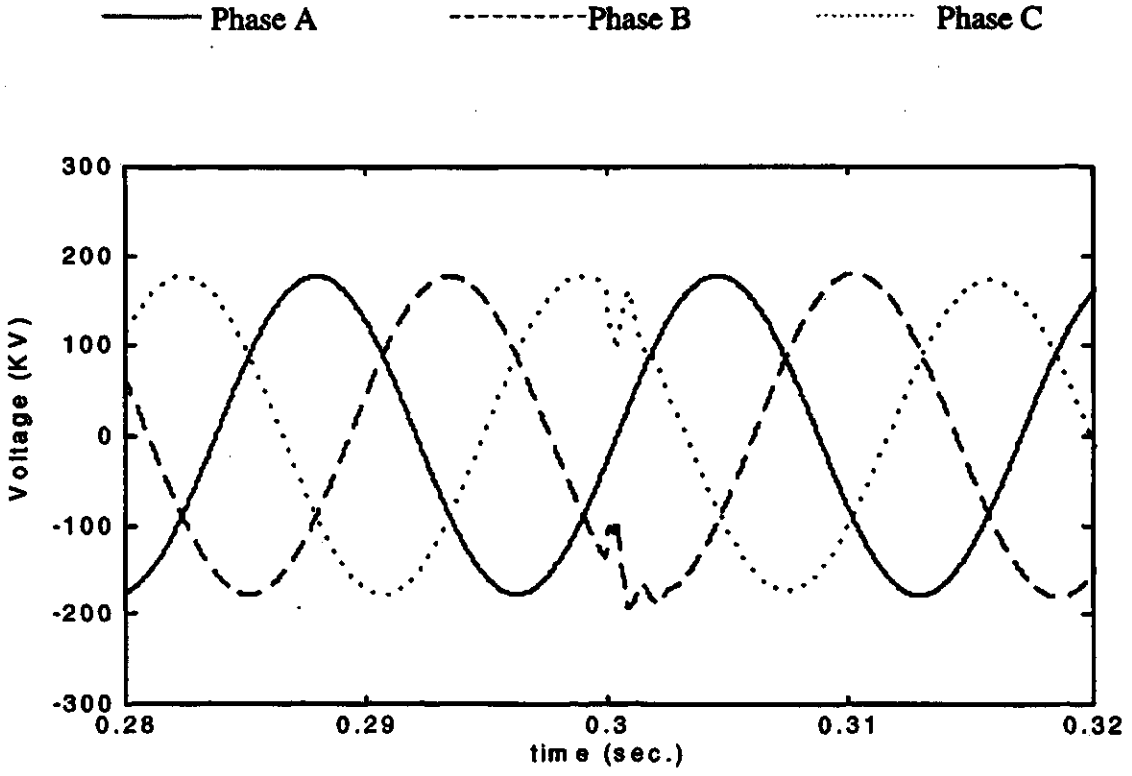
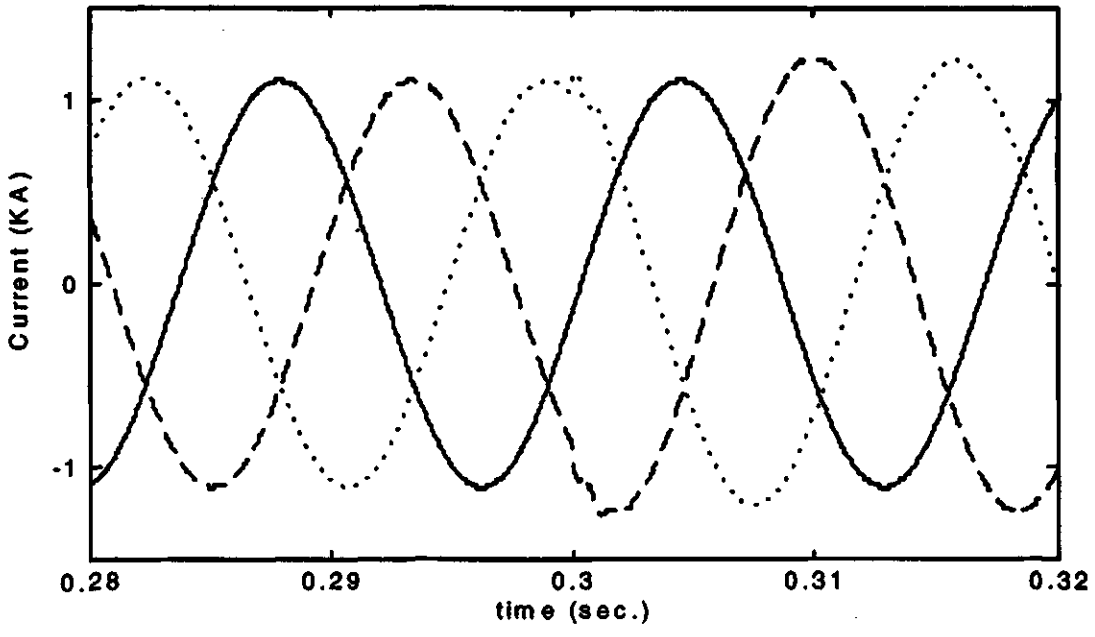


Figure 4.27. Unfiltered (a) voltage and (b) current waveforms on the 13.8 kV side of power transformer for Phase B-ground internal fault in 13.8 kV winding (location 2, Figure 4.1).



(c)



(d)

Figure 4.27(contd.). Unfiltered (c) voltage and (d) current waveforms on the 230 kV side of power transformer for Phase B-ground internal fault in 13.8 kV winding (location 2, Figure 4.1).

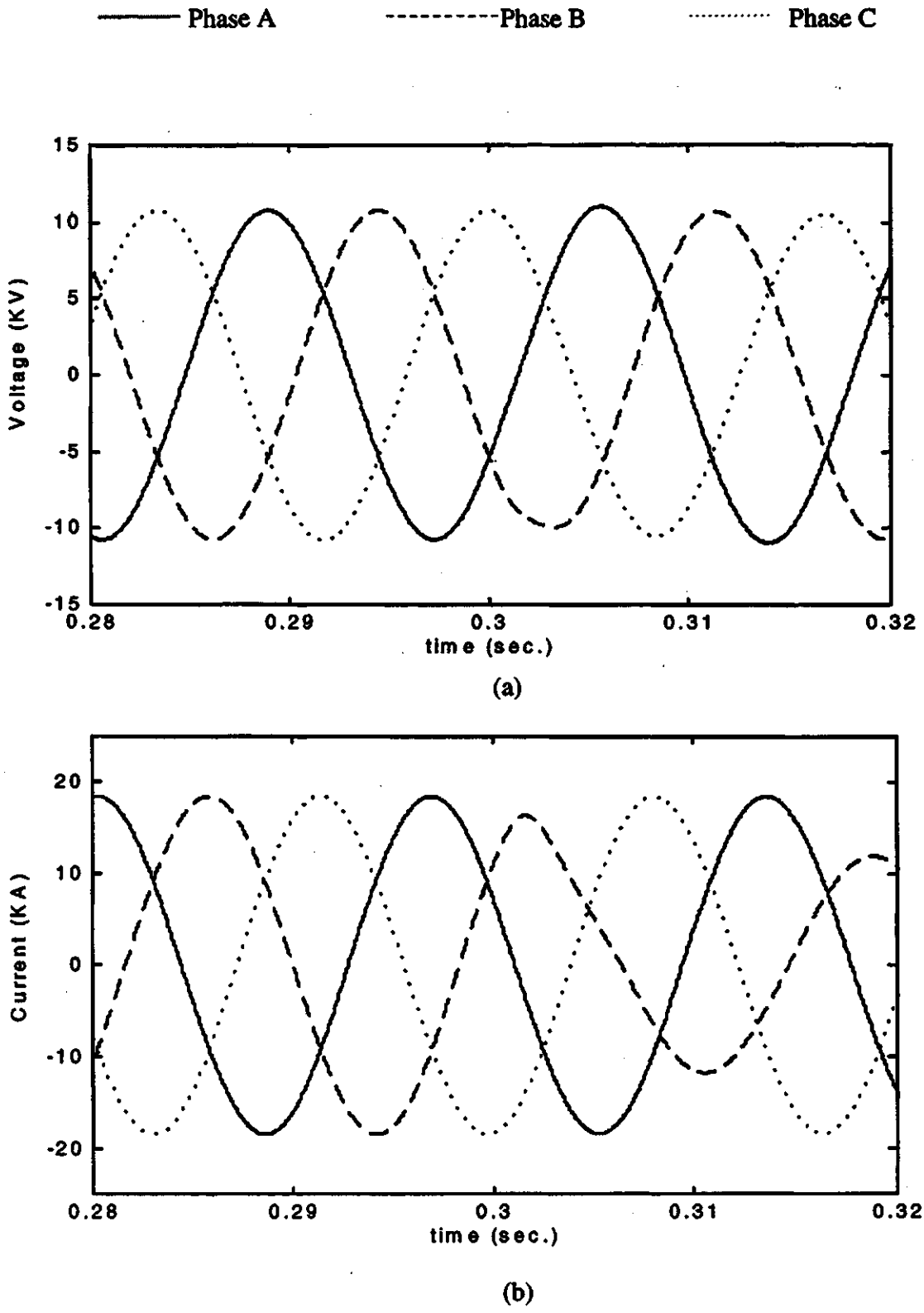


Figure 4.28. Filtered (a) voltage and (b) current waveforms on the 13.8 kV side of power transformer for Phase B-ground internal fault in 13.8 kV winding (location 2, Figure 4.1).

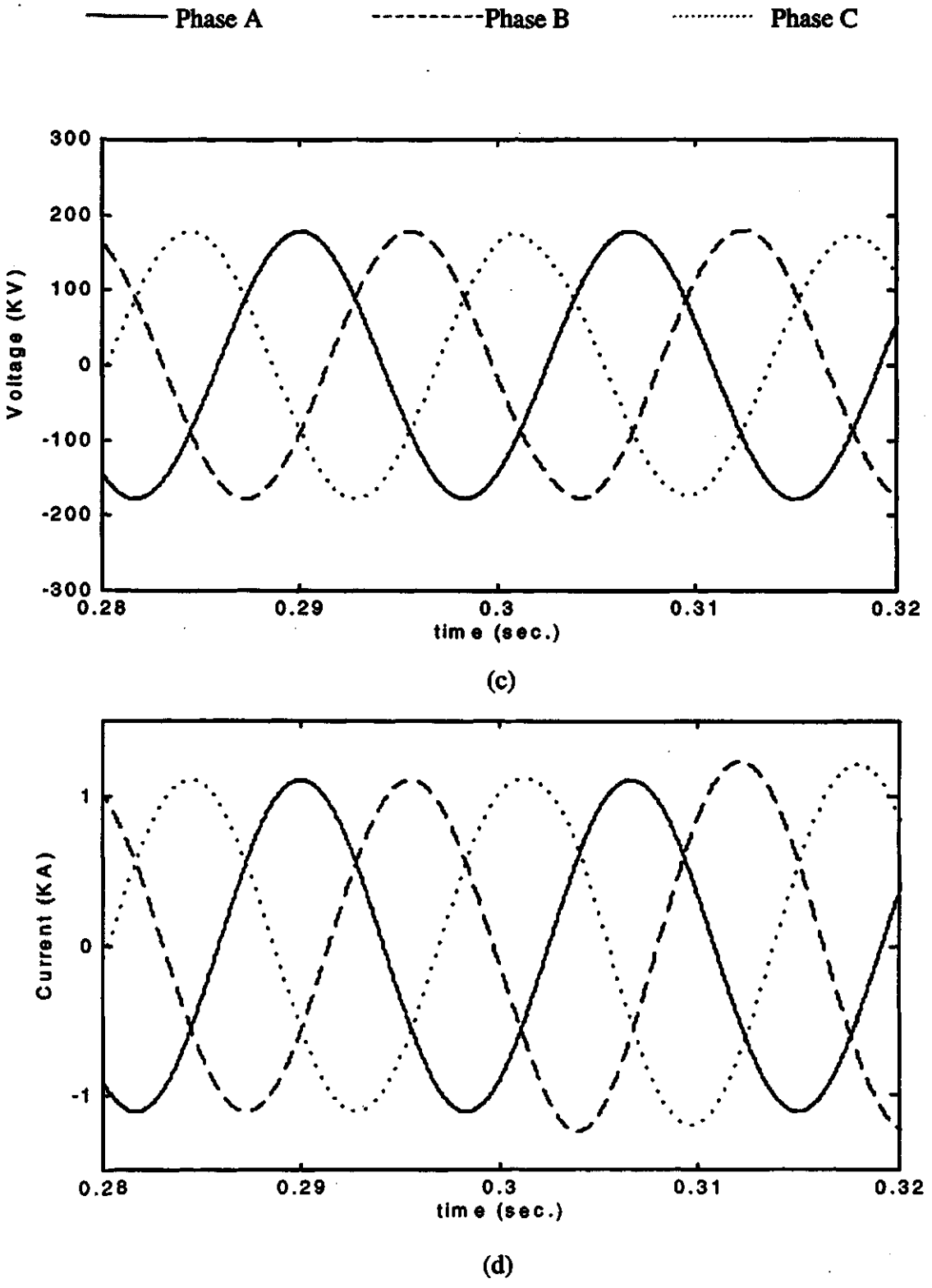


Figure 4.28(contd.). Filtered (c) voltage and (d) current waveforms on the 230 kV side of power transformer for Phase B-ground internal fault in 13.8 kV winding (location 2, Figure 4.1).

inception of the fault after which the positive- and negative-sequence impedances are computed using the incremental voltages and currents. The computed sequence-impedances (in polar form) are shown in Figures 4.29 (a) and (b). The profiles of the positive- and negative-sequence trip counters are shown in Figure 4.29(c). The computed positive- and negative-sequence impedances from both sides of the power transformer were in the third quadrant. This led to the decision that the fault is inside the transformer protection zone. The positive-sequence and negative-sequence trip counters of the 13.8 kV and 230 kV sides reached the threshold in 15 samples when the trip-logic confirmed that the fault is in the protection zone of the transformer. The algorithm took 10.4 ms to make the final decision in this case.

4.8. Switch-on faults

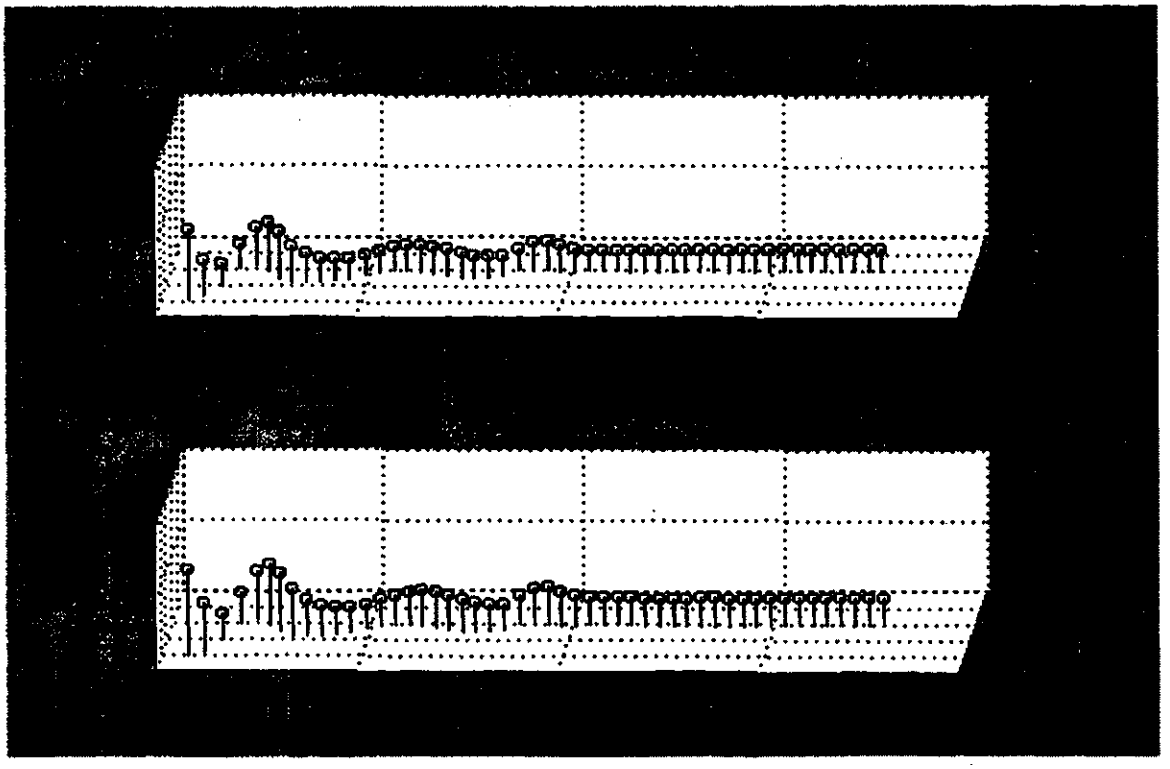
Different types of switch-on faults, internal and external to the power transformer, were simulated using the system shown in Figure 3.14. Selected test studies are presented in the following sections.

4.8.1. External faults

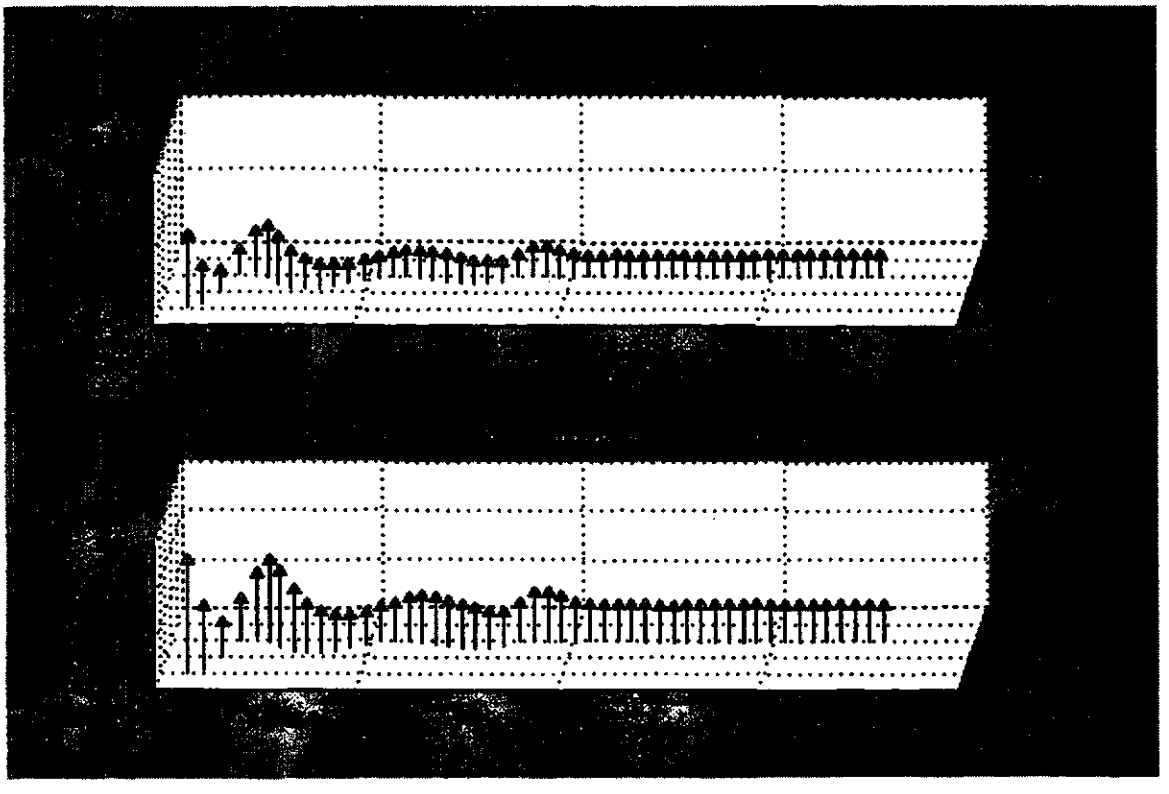
External faults were simulated at location A shown in Figure 3.14. The occurrence of the fault was synchronized with switching-on of the power transformer. The switching-on to a faulted transformer was simulated in this manner. Different types of external faults were studied. Selected cases are presented in this section.

4.8.1.1. Two-phase fault : Phase A - Phase B

A Phase A to Phase B fault was simulated on the 230 kV side of the power transformer at location A shown in Figure 3.14. The transformer was switched on at time 0.3 seconds. Figure 4.30 depicts the results showing the performance of the algorithm. The positive-sequence impedances were computed using the incremental positive-sequence voltages and currents. The positive-sequence impedance (in polar

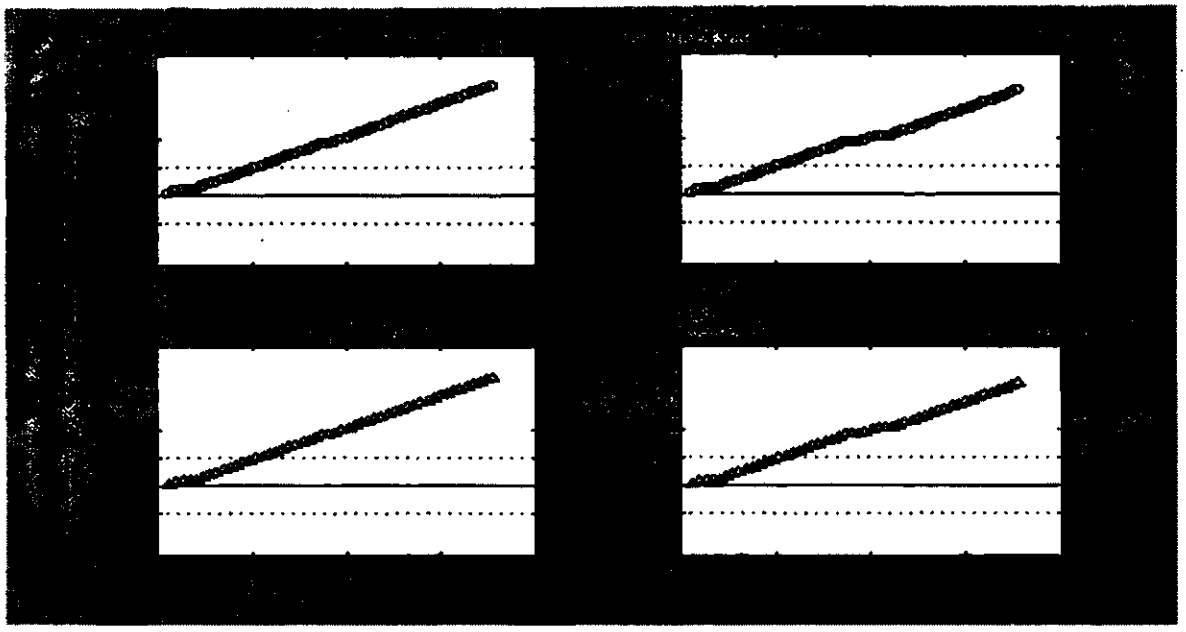


(a)



(b)

Figure 4.29. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase B-ground internal fault in the 13.8 kV winding of the power transformer (location 2, Figure 4.1).



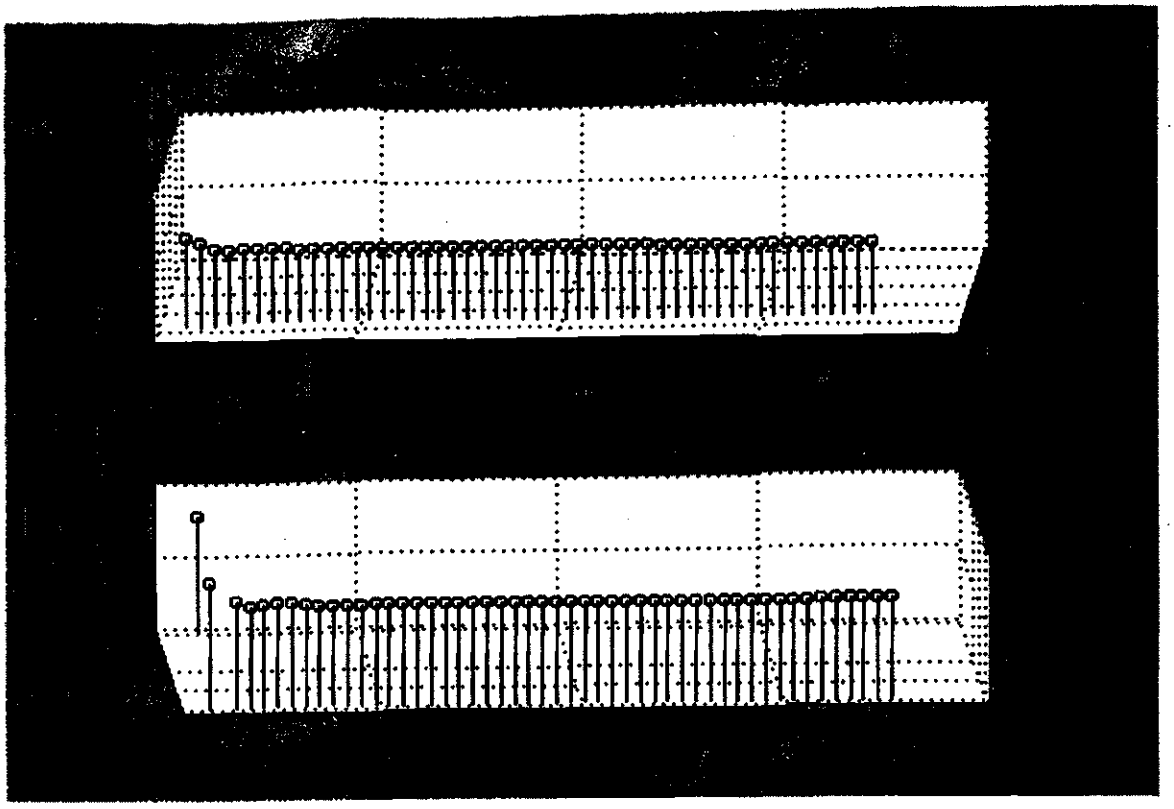
(c)

Figure 4.29. Plot of (c) trip counters for a high-impedance Phase B-ground internal fault in 13.8 kV winding of the power transformer (location 2, Figure 4.1).

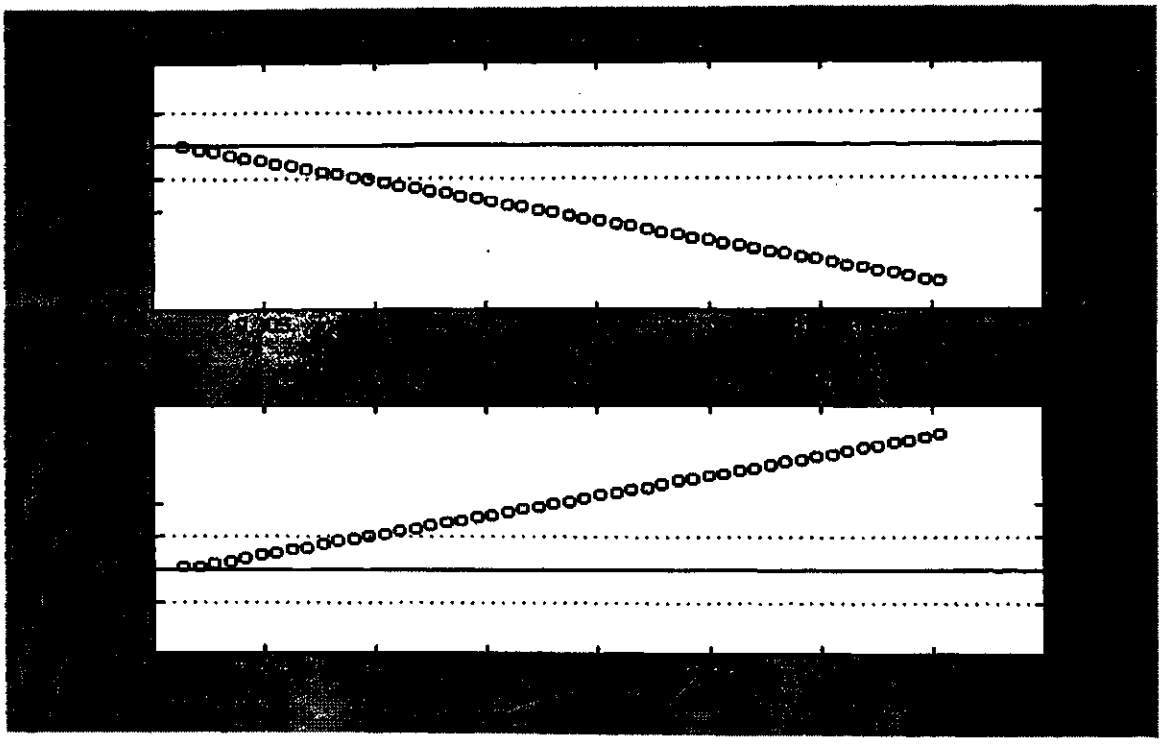
form) and the positive-sequence trip counters are shown in Figure 4.30. The figure shows that the positive-sequence impedances computed on the 13.8 kV side of the power transformer were in the first quadrant whereas the impedances computed on the 230 kV side were in the third quadrant. These conclusions led to the decision that the fault is outside the protection zone of the transformer. The positive-sequence trip counters of the 13.8 kV and 230 kV sides reached the threshold in 13 samples. The algorithm took 9.0 ms to make the final decision in this case.

4.8.1.2. Single phase-to-ground fault : Phase A

A ground fault on Phase A was simulated on the 230 kV side of the power transformer at location A shown in Figure 3.14. The transformer was switched on at time 0.3 seconds. Figure 4.31 depicts the results showing the performance of the algorithm. The positive-sequence impedance were computed by the relays using the incremental positive-sequence voltages and currents. The values of the positive-sequence impedance (in polar form) are shown in Figure 4.31. The figure also shows the profiles of the positive-sequence trip counters. The figure shows that the positive-sequence

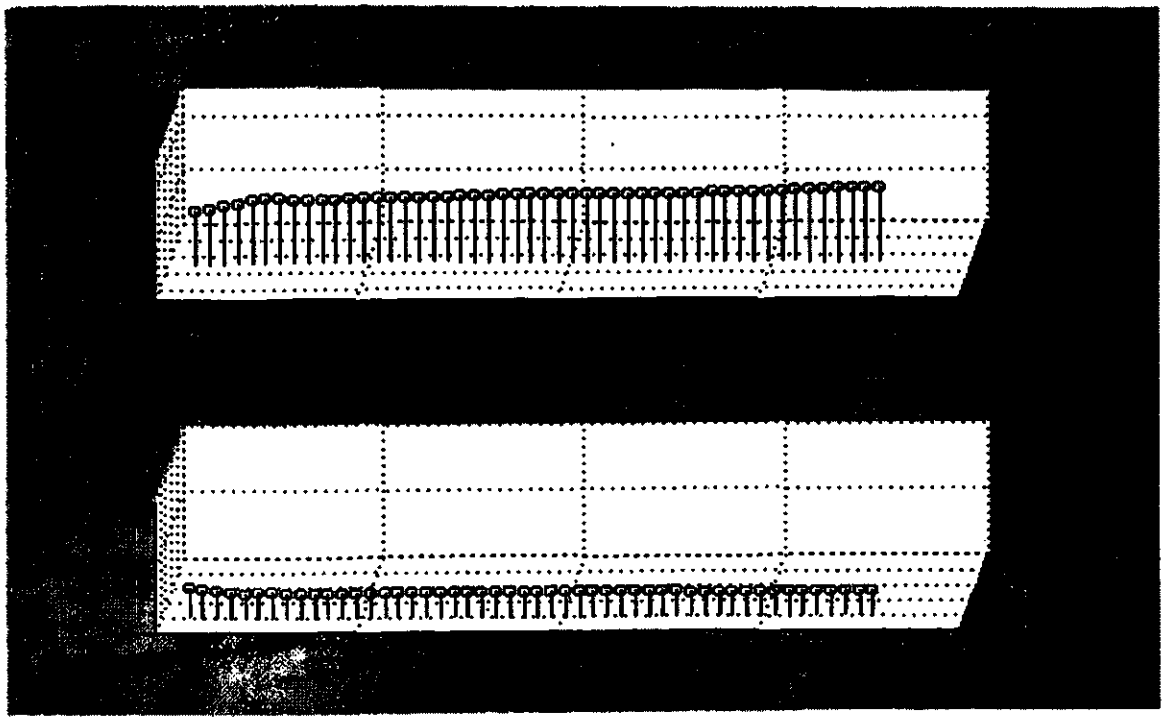


(a)

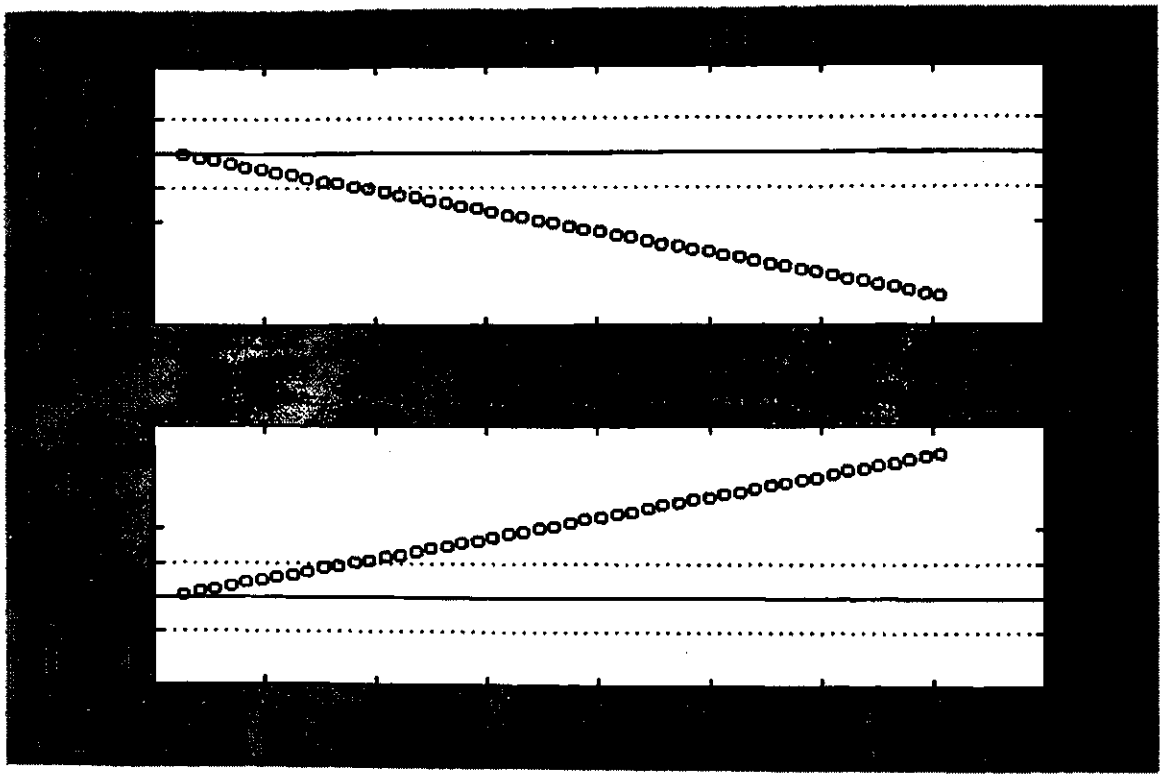


(b)

Figure 4.30. Plot of (a) positive-sequence impedance computed by the relays and (b) trip counters for Phase A-Phase B switch-on external fault for the power transformer (location A, Figure 3.14).



(a)



(b)

Figure 4.31. Plot of (a) positive-sequence impedance computed by the relays and (b) trip counters for Phase A-ground switch-on external fault for the power transformer (location A, Figure 3.14).

impedance computed on the 13.8 kV side of the transformer were in the first quadrant and positive-sequence impedance computed on the 230 kV side of the transformer were in the third quadrant. The algorithm concluded from this information that the fault is outside the protection zone of the transformer. The positive-sequence trip counters reached the threshold in 13 samples. The algorithm took 9.0 ms to make the final decision in this case.

4.8.2. Internal faults

Several internal faults were simulated to verify the fault-detection criterion described in Section 3.6.2. Selected test cases are presented in this section.

4.8.2.1. Single phase-to-ground fault : Phase B

A single phase-to-ground switch-on fault on Phase B was simulated on the 13.8 kV side of the power transformer (location 2 shown in Figure 4.1). A fault resistance of 0.1 ohms was used. The voltage and current waveforms from this simulation are shown in Figure 4.32. The voltage ratios were computed using the peak values of the primary and secondary voltages. These ratios were 16.0617 (i.e. 186.207 kV/11.5932 kV), 18.735 (i.e. 171.473 kV/9.15254 kV) and 12.3302 (i.e. 137.931 kV/11.1864). The voltage ratio of the phase C was less than the threshold, THRSWF (0.8*230 kV/13.8 kV=13.3334), for switch-on faults. The low voltage ratio and the absence of currents on the 230 kV side indicated an internal fault.

4.8.2.2. Three-phase-to-ground fault

A three-phase-to-ground fault was simulated on the 230 kV side of the power transformer (location B shown in Figure 3.14). A fault resistance of 50 ohms was used. The voltage and current waveforms from this simulation are shown in Figure 4.33. The voltage ratios were computed using the peak values of the primary and secondary voltages. These ratios were 0.9037 (i.e. 6.06558 kV/6.71186 kV), 0.702 (i.e. 4.71143 kV/6.71186 kV) and 0.8277 (i.e. 5.5551 kV/6.71186). The voltage ratios of all the

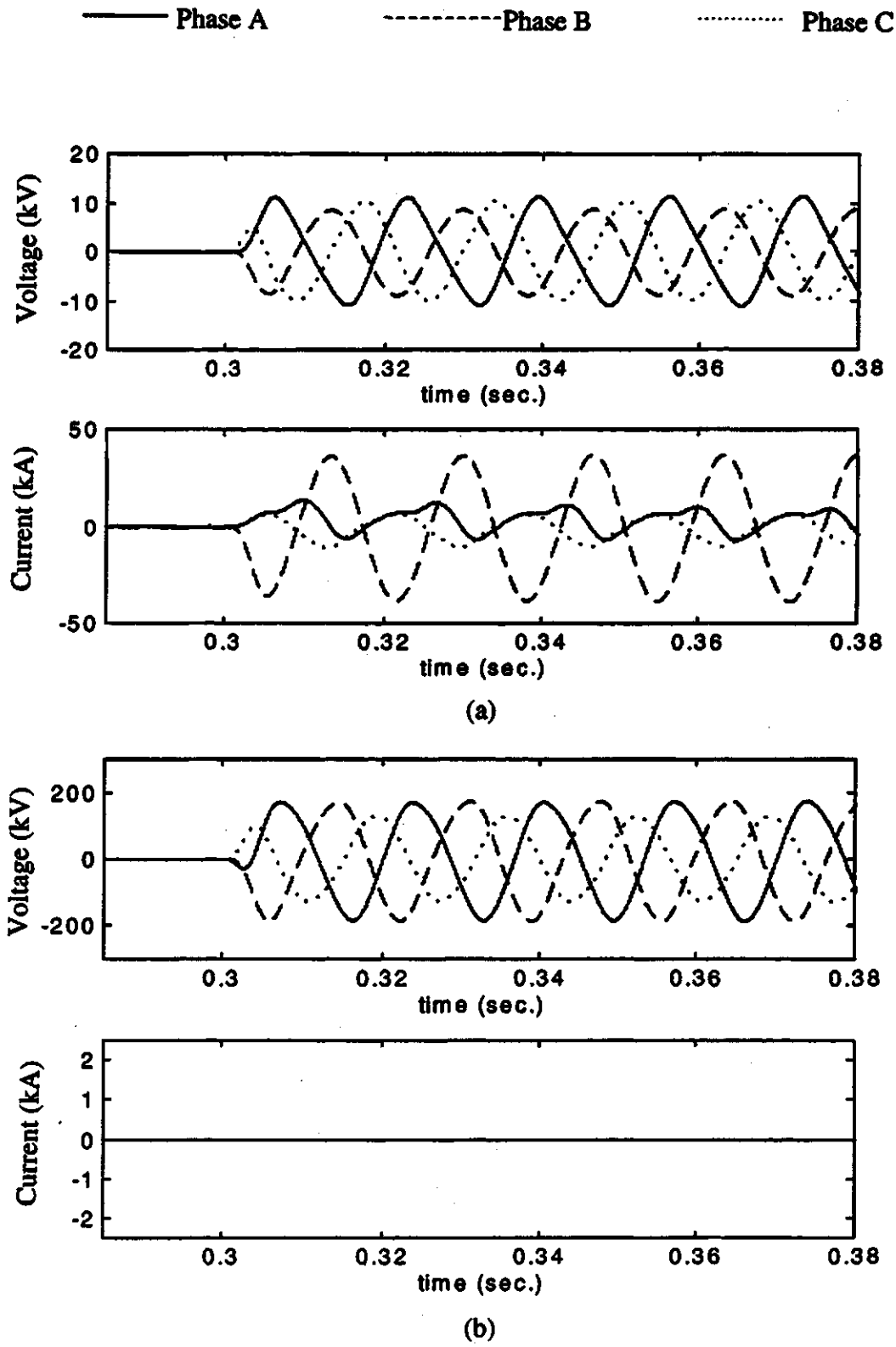


Figure 4.32. Voltage and current waveforms on (a) 13.8 kV and (b) 230 kV sides of power transformer for Phase B-ground switch-on internal fault in 13.8 kV winding.

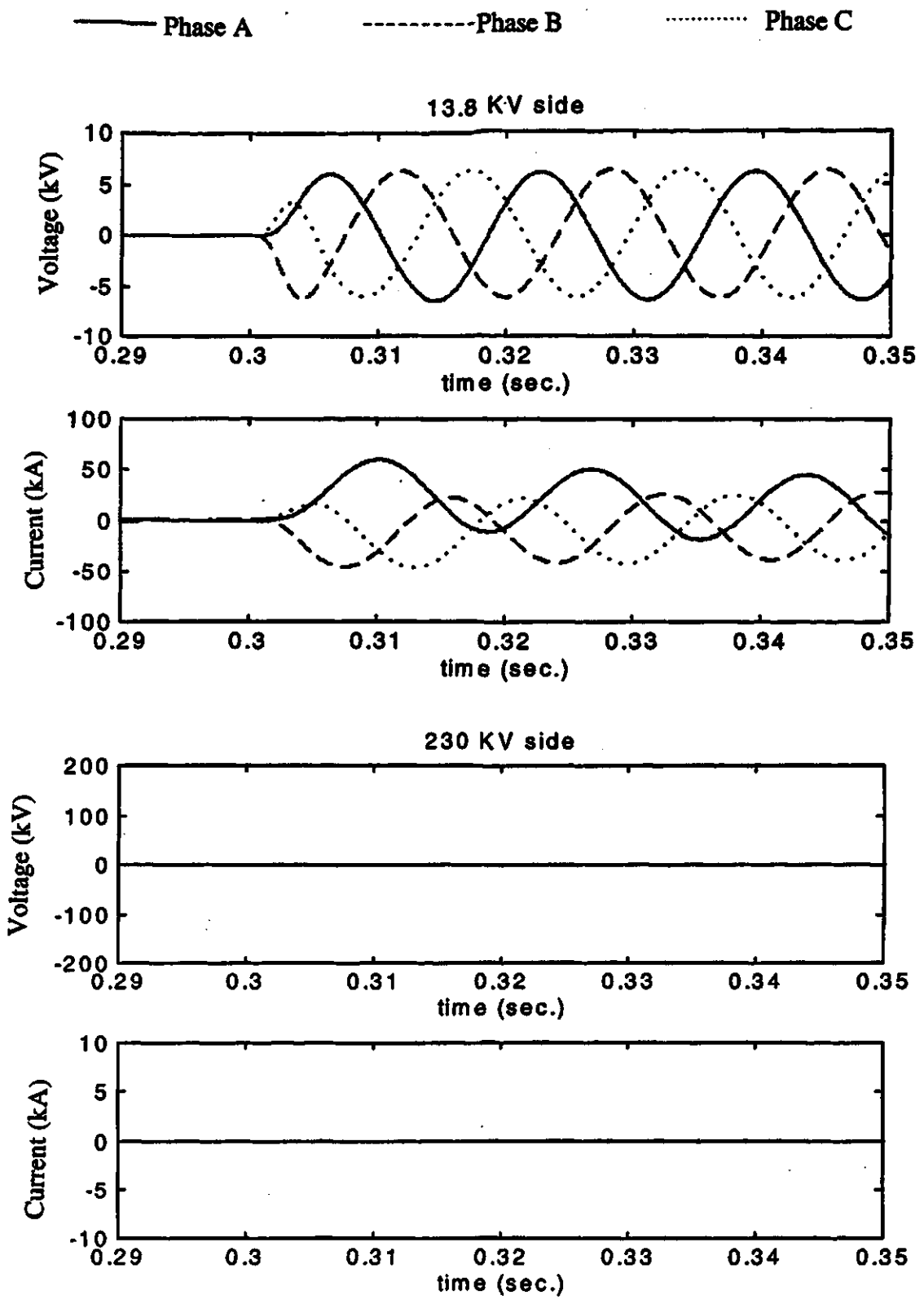


Figure 4.33. Voltage and current waveforms on 13.8 kV and 230 kV sides of power transformer for a three-phase-ground switch-on internal fault in the 230 kV winding.

phases were less than the threshold, THRSWF (13.3334), for switch-on faults. The low voltage ratios and the absence of currents on the 230 kV side indicated an internal fault.

4.8.2.3. Two-phase fault : Phase B - Phase C

A two-phase fault involving phases B and C was simulated on the 230 kV side of the power transformer (location B shown in Figure 3.14). A fault resistance of 0.1 ohm was used. The voltage and current waveforms from this simulation are shown in Figure 4.34. The voltage ratios were computed using the peak values of the primary and secondary voltages. These ratios were 17.2739 (i.e. 186.207 kV/10.7797 kV), 14.1928 (i.e. 100.92 kV/7.11064 kV) and 9.5966 (i.e. 103.448 kV/10.7797 kV). The voltage-ratio of 9.5966 was less than threshold, THRSWF (13.3334), for switch-on faults. The low voltage-ratio and absence of currents on the 230 kV side indicated an internal fault.

4.9. Magnetizing inrush

Condition of magnetizing inrush were simulated by energizing the transformer from its 13.8 kV terminals at 0.3 s. The waveforms of the currents are shown in Figure 4.35. The waveforms of the voltages at the 13.8 kV and 230 kV terminals are also shown. The voltage ratios were computed using the peak values of the primary and secondary voltages and were found to be 16.0714 (i.e. 186.207 kV/11.5862 kV). The voltage ratios were more than the threshold, THRSWF (13.3334) and the absence of the currents in the 230 kV lines indicated that the transformer is not experiencing a fault.

4.10. Summary

The simulation procedure suitable for evaluating the performance of the proposed technique of protecting power transformers has been described in this chapter. A single-line diagram of the system used in EMTDC simulations has been presented.

Different types of faults were simulated and the data from these simulations were used to evaluate the technique proposed in Chapter 3. The impact of current transformer

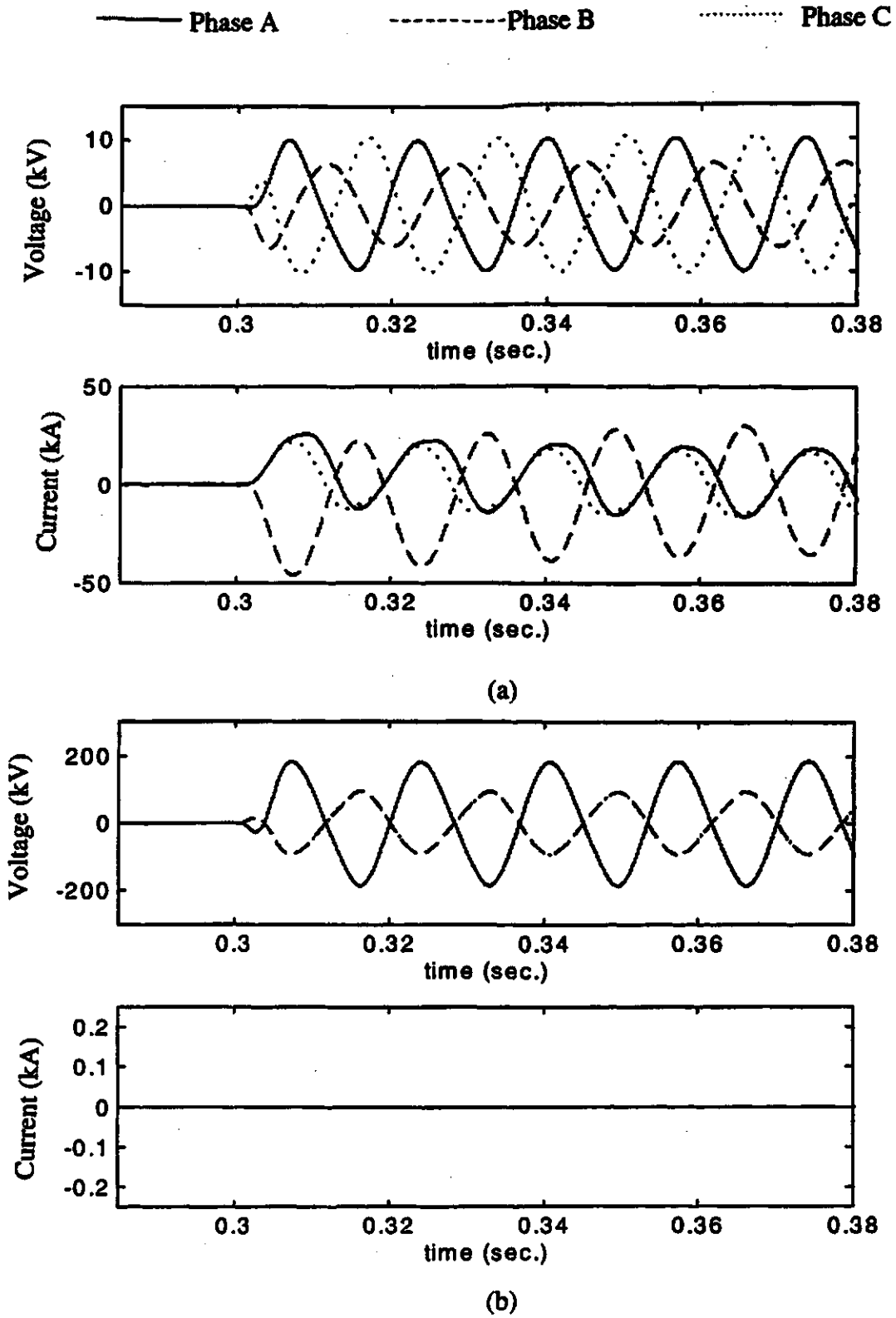


Figure 4.34. Voltage and current waveforms on (a) 13.8 kV and (b) 230 kV sides of power transformer for Phase B - Phase C switch-on internal fault in the 230 kV winding.

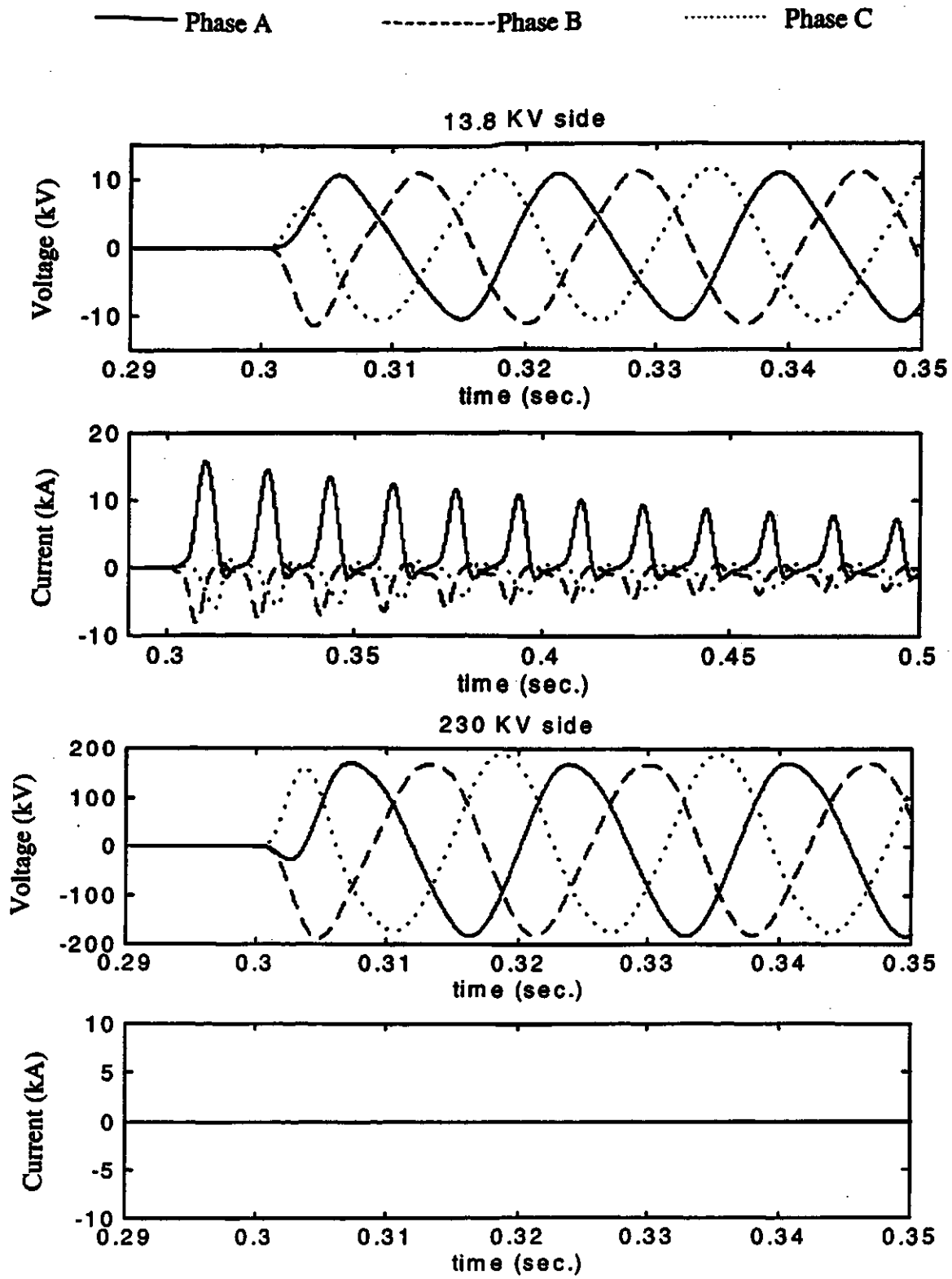


Figure 4.35. Voltage and current waveforms on 13.8 kV and 230 kV sides of the power transformer for magnetizing inrush condition (transformer switched-on at 0.3 seconds).

saturation and ratio-mismatch on the performance of the proposed technique have also been investigated. It has been noted that the impedance seen by a relay for saturated ct(s) is higher in magnitude than the corresponding value observed for an unsaturated ct(s). Also, the impedance value lies well within the fault-detection zone for saturated ct(s). These two observations conform to the theoretical basis developed in Section 3.9.

The technique is stable when the ct ratios do not match. This can be attributed to the fact that the impedance calculations made on primary and secondary sides of the transformer are independent of each other.

The performance of the proposed technique was also verified by simulating high-impedance faults. Switch-on faults and magnetizing inrush situations have also been investigated to validate the feasibility of the proposed technique.

The studies have shown that the proposed technique distinguishes correctly between internal and external faults. The time needed for making the decisions ranges from 9.0 to 13.2 ms.

5. SUMMARY AND CONCLUSIONS

A power system occasionally experiences faults which can cause extensive damage to the equipment besides injury to personnel. This results in substantial monetary losses to utilities and consumers. A system element should, therefore, be protected from damage due to faults and abnormal operating conditions.

The first chapter of the thesis has described power system protection concepts and developments leading to and including the use of microprocessor-based relays. Majority of the research work in this area has concentrated towards developing suitable algorithms for protecting different power system equipments.

Major algorithms proposed in the past for protecting transformers have been explained in Chapter 2. These algorithms compare the fundamental and harmonic frequency components, and differ basically in the methods used for computing phasors. A discussion of these algorithms is included in the chapter. All of these algorithms are affected by ct saturation and ct ratio-mismatch. No effort in describing the effects of these conditions on the proposed algorithms have been reported and remedial measures have not been suggested. Only two schemes dealing with the phenomenon of ct saturation have been reported in the past. These schemes require special criteria for their correct implementation, which is a major deficiency. No algorithm proposed in the past provides a way of handling the ct ratio-mismatch condition.

The major objective of this thesis was to develop and test an algorithm for protecting power transformers, and study the effects of ct saturation and ratio-mismatch on the performance of the proposed algorithm.

A technique, based on the concept of symmetrical components, was developed for protecting power transformers; the technique has been reported in Chapter 3. It uses fundamental frequency voltage and current phasors computed from quantized samples of voltages and currents at the transformer terminals. The computed phasors are used to calculate the positive- and negative-sequence phasors. These sequence-phasors are manipulated to estimate the positive- and negative-sequence impedances. The relay uses the arguments of the impedances to distinguish between the faults inside and outside the transformer protection zone. The proposed technique was adapted to protect unloaded transformers. A criterion based on the voltage-ratios of the primary and secondary voltages of the transformer was developed to detect the occurrence of faults while a transformer is energized. Fault-detection characteristics and an algorithm based on the proposed technique have also been described in Chapter 3.

A theoretical basis to describe the impact of ct saturation on the developed technique was formulated. It is based on the correlation principle which is commonly used for estimating the voltage and current phasors. It proves the ability of the technique to provide correct decisions during ct saturation. The effect of ct ratio-mismatch on the performance of the technique has also been discussed in Chapter 3.

Chapter 4 presents the performance evaluation of the proposed technique. Fault-data generated for a power system model simulated on an electromagnetic transient program, EMTDC, were used for this purpose. The fault-data were pre-processed using anti-aliasing filters. A program written in ANSI C was used to implement the proposed technique. Test studies were carried out for different types of faults and different operating conditions including loaded and unloaded transformers and switch-on faults. The impact of ct saturation and ratio-mismatch on the performance of the technique were also investigated. Test results showed that the proposed technique correctly detects the faults that occur inside and outside the transformer protection zone. Typical relay operating times ranged from 9.0 to 13.2 ms.

It was noted that the impedance seen by a relay for a saturated ct(s) is higher in magnitude than that observed for an unsaturated ct. However, the impedance values remained well within the fault-detection zone. This conformed the theoretical basis developed in Chapter 3. It was also noticed that fault-detection times remain similar irrespective of the fact whether a ct saturates or not.

Test studies to check the impact of ct ratio-mismatch on the performance of the proposed technique were carried out. Different levels of ct ratio-mismatch were simulated. The results show that the decisions made by the technique are not affected by mismatch of ct ratios. This results from the fact that the impedances calculated from data obtained from the primary terminals are independent of those calculated from the data obtained from the secondary terminals. This makes the proposed technique inherently immune to mismatch of the ct ratios.

The technique performs equally well for protecting an unloaded transformer. Test studies to check the performance of the technique to detect in-zone faults for an unloaded transformer were conducted. The technique provided correct decisions in 9.0 to 13.2 ms.

The fault-detection criterion for detecting switch-on faults in the transformer was also verified by simulating different types of faults. It was found that the condition of magnetizing inrush can be correctly identified when a transformer is energized. Both, external and internal switch-on faults, were detected correctly by the proposed criterion.

Performance results have established the suitability of the proposed technique for providing effective protection of transformers.

The specific contributions made by this thesis are as follows.

1. A technique for protecting power transformers, operating in unloaded and loaded conditions, has been developed and an algorithm based on the same has been proposed. The technique does not require information concerning parameters of the

transformer and the power system. Only the arguments of the sequence-impedances computed by the relay are used to make decisions.

2. A theoretical basis describing the effect of ct saturation on the proposed technique has been formulated and tested. The technique also handles the condition of ct ratio-mismatch.

3. A criterion to detect occurrence of faults during energization of transformers has been developed and verified.

5.1. Suggestions for future work

Fault-detection times of the proposed protection algorithm depend on the speed with which phasors and sequence-components are computed. These can be possibly improved by using faster algorithms for estimating phasors and sequence-components. Real-time implementation of the proposed technique needs to be carried out to validate its feasibility for use in digital relays.

Performance of the proposed technique for detecting inter-winding faults could not be evaluated due to the inability of EMTDC to simulate such faults. The performance of the technique to detect such faults needs to be investigated in the future. Further developmental work is also required to apply the proposed technique for detecting simultaneous faults.

Stable performance provided by the technique during ct saturation and ratio-mismatch conditions makes it viable for use in protecting busbars where large magnitude of fault currents are usually experienced. Further research work could involve an investigation of applying the proposed technique for busbar protection.

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A. SYMMETRICAL COMPONENTS & SEQUENCE-NETWORKS

Symmetrical components

The method of symmetrical components was first proposed by C.L. Fortescue and has been found very useful in analyzing unbalanced polyphase circuits. The concept of symmetrical components allows decomposition of any unbalanced 3-phase system of vectors (whether representing currents or voltages) into three balanced systems of vectors which are called its 'symmetrical components' [27]. The balanced set of phasors are-positive-sequence, negative-sequence and zero-sequence components. Figure A.1 shows the relation between the unbalanced set of phasors and the corresponding symmetrical components.

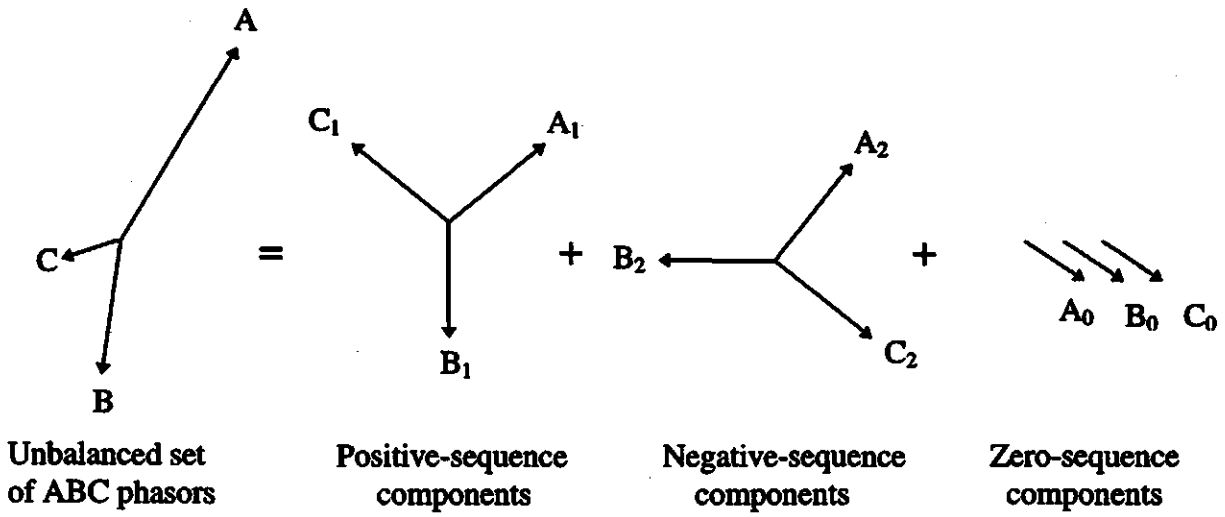


Figure A.1. Decomposition of an unbalanced set of ABC phasors into symmetrical components.

Positive-sequence components are the balanced systems of 3-phase vectors having the same phase sequence as the unbalanced set unlike the negative-sequence components

which have an opposite phase sequence from the original unbalanced set of phasors. Zero-sequence components are equal in magnitude and are in phase with each other.

In equation form, symmetrical components for an unbalanced set of voltages can be written as

$$V_a = V_{a1} + V_{a2} + V_{a0}$$

$$V_b = V_{b1} + V_{b2} + V_{b0}$$

$$V_c = V_{c1} + V_{c2} + V_{c0} \quad . \qquad \text{(A.1)}$$

Also,

$$V_{b1} = a^2 V_{a1}\ ,\ V_{c1} = a V_{a1}\ ,\ V_{b2} = a V_{a2}\ ,\ V_{c2} = a^2 V_{a2}\ ,\ V_{b0} = V_{c0} = V_{a0} \qquad \text{(A.2)}$$

where:

- a — is an operator that causes a phase shift of 120 degrees and is defined as -0.5 + j 0.866,
- a^2 — is an operator that causes a phase shift of 240 degrees and is defined as -0.5 - j 0.866.

From Equations (A.1) and (A.2), it follows that

$$V_a = V_{a1} + V_{a2} + V_{a0}$$
$$V_b = a^2 V_{a1} + a V_{a2} + V_{a0}$$
$$V_c = a V_{a1} + a^2 V_{a2} + V_{a0} \quad . \qquad \text{(A.3)}$$

In matrix form,

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_{a0} \\ V_{a1} \\ V_{a2} \end{bmatrix}$$

The symmetrical components can, thus, be represented in terms of the unbalanced set of

phasors as

$$\begin{bmatrix} V_{a0} \\ V_{a1} \\ V_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad . \tag{A.4}$$

Sequence-networks

The voltage drop caused by current of a particular sequence depends upon the impedance offered to the current of that sequence. Therefore, sequence-impedances are termed positive-, negative- and zero-sequence impedance depending upon the respective sequence currents [24].

The analysis of an unsymmetrical fault in a symmetrical system consists of finding the symmetrical components of the unbalanced currents flowing in the circuit. Since the sequence current of one type differs from the other, and causes voltage drop of like sequence only, it may be considered to flow in an independent network composed of the impedances to the current of that particular sequence only. The single-phase equivalent circuit comprising impedances to current of one sequence type only is called the sequence-network for that particular sequence. This network shows all the paths for the flow of current of that sequence in a system.

The method of symmetrical components, thus, involves determination of sequence impedances to form sequence-networks and their appropriate connections to analyze a fault.

B. EMTDC & CT MODEL

This appendix gives a brief description of the power systems simulation software, EMTDC[26], which was used for the generation of simulated fault data for the power transformer, and the ct model used to simulate ct saturation and ratio-mismatch conditions. Complex power system networks can be modeled using EMTDC to represent practical systems. A user interface, called Power Systems Computer Aided Design(PSCAD), enables the user to select preprogrammed models of power system components which are used to graphically build the power system networks. The built-in library of PSCAD includes models of voltage and current sources, machines, transmission lines, switches, measuring instruments, transformers and control blocks and many other power system apparatus models.

Compilation of the PSCAD network generates FORTRAN source code. The source code is then compiled using EMTDC which generates executable code that runs in the UNIX environment of the SunSPARC workstation. Fault data generated by EMTDC was stored in a file. This data file was used for testing the proposed protection algorithm.

The ct model used in the research project was downloaded from the ftp site of the University of Manitoba [28]. This model was initially written by Dr. J. Mohan Lucas and later revised by Dr. W.W.L. Keerthipala and Rohitha P. Jayasinghe respectively. The model can be represented as in Figure B.1.

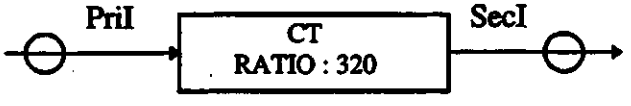


Figure B.1. CT model.

The model has two wire labels for representing the primary and secondary currents of the current transformer respectively. The primary wire label is given the same name as the current label used in the EMTDC simulation model. The secondary wire label then gives the equivalent ct output for the given input current. The ct ratio can be selected in the model . Saturation state of the ct can be simulated by using very high value for the burden resistance. Typical burden impedance in practice is much less than the values used in the model. The default values for the saturation and loss characteristics match with those of the 'silectron 53' core material.

C. DATA

The data used for power transformer and other system components in the power system model shown in Figure 3.1 is given below:

Parameter	Generation G_x	Generation G_y
Base MVA (3 phase)	100 MVA	100 MVA
Rated volts(L-L, RMS)	13.8 KV	230.0 KV
Initial phase	0.0 deg	10.0 deg
Positive-sequence RRL:		
Resistance (series)	0.01 ohms	0.1 ohms
Resistance (parallel)	2000.0 ohms	2000.0 ohms
Inductance (parallel)	0.0004 H	0.1 H
Negative-sequence RL:		
Resistance (parallel)	50.0e+6 ohms	50.0e+6 ohms
Inductance (parallel)	0.0001 H	0.025 H

Power Transformer (T)

3 phase MVA	100 MVA
13.8 KV winding	Star connected
230.0 KV winding	Delta connected
Positive-sequence leakage reactance	0.1 p.u.

Transmission Line (TL)

Line length	100.0 Kms.
V(KV)L-L, rms	230.0 KV
Ideally transposed	
Frequency-dependent model used	

Current Transformer model

*Nominal ct ratio on 13.8 KV	840
*Nominal ct ratio on 230.0 KV	50
Burden Resistance	0.5 - 40.0 ohms
Burden Inductance	0.8e-3 H

* Nominal ct ratio=((Rated MVA*100)/Rated KV)/5

ct produces an output current of 5A for rated current in its primary.

D. ANTI-ALIASING FILTER DESIGN

The fault voltages and currents are associated with decaying dc, fundamental frequency (60 Hz) and high frequency components [29, 30, 31]. The high frequency components result due to traveling wave phenomenon and their frequencies depends on the distance to the fault. Non-linearities in the power system produce harmonics of 60 Hz components.

Depending on the sampling rate of voltages and currents, some of the high frequency components can appear as components of power frequency [32]. An anti-aliasing filter was designed to pre-process the voltage and current samples obtained by simulation before being presented to the LES algorithm. The principle of anti-aliasing dictates that the cut-off frequency of the low-pass filter should be less than or equal to one-half of the sampling frequency of the LES algorithm. The sampling frequency of least error squares algorithm used to estimate the fundamental frequency components of voltage and current signals was selected as 1440 Hz. A 4th order Butterworth filter with a cut-off frequency of 200 Hz was selected as an anti-aliasing filter. The filter was designed using a Matlab program . Equation D.1 gives the transfer function for the designed filter.

$$\frac{Y(z)}{X(z)} = \frac{1.0x10^{-5}(0.0515546 + 0.2062183z^{-1} + 0.3093274z^{-2} + 0.2062183z^{-3} + 0.0515546z^{-4})}{(1.0z^{-1} - 3.8574847z^{-2} + 5.5825215z^{-3} - 3.5921775z^{-3} + 0.8671489z^{-5})} \quad \text{(D.1)}$$

Figure D.1 shows the magnitude response of the designed low-pass filter.

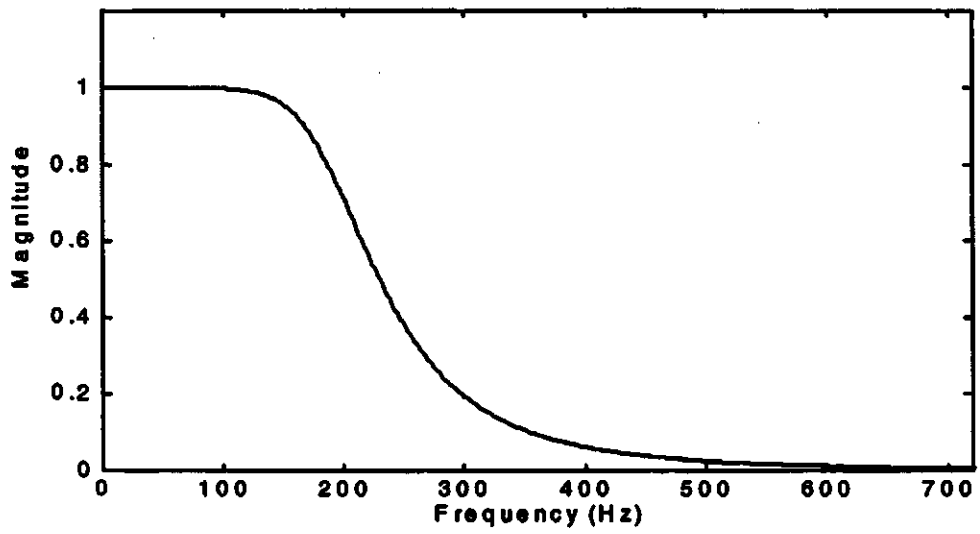
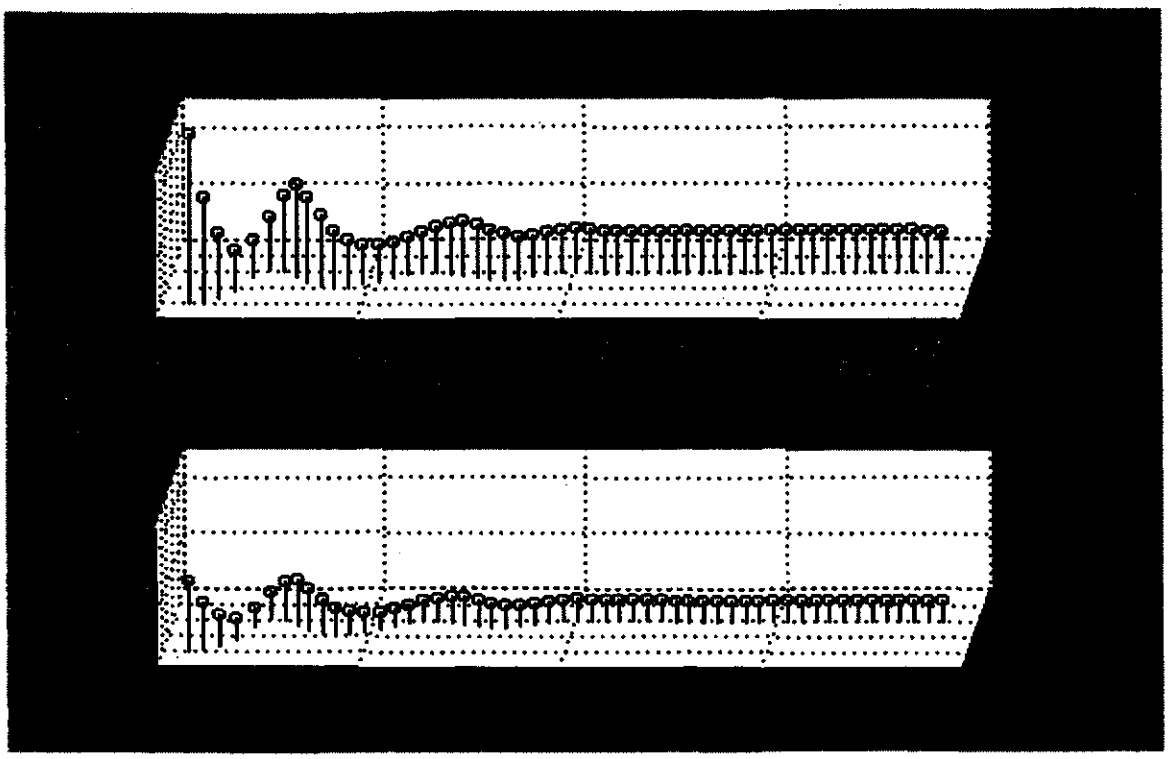


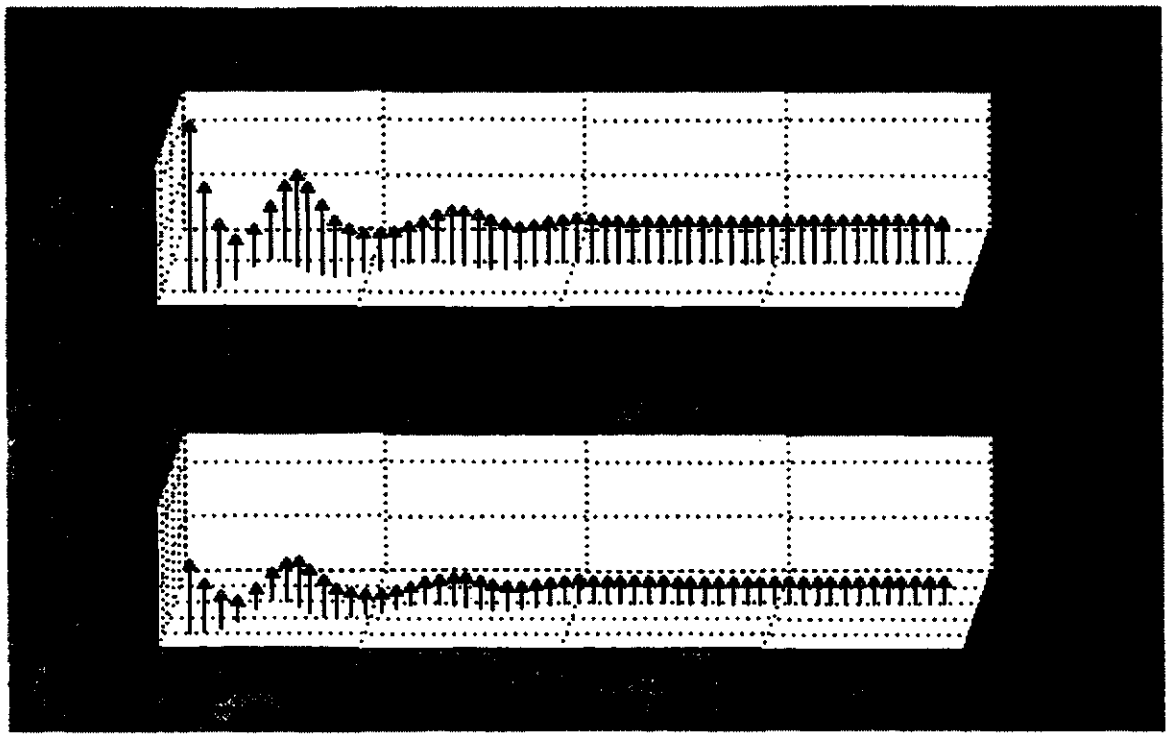
Figure D.1. Magnitude response of anti-aliasing filter.

E. ADDITIONAL TEST RESULTS

The test results illustrating the performance of the proposed technique for power transformer protection for selected simulation cases were presented in Chapter 4. The criterion proposed for discriminating switch-on faults was also evaluated using test results, a few of which were included in Chapter 4. This appendix provides additional test results for various types of faults and current transformer conditions. Figures E.1 to E.6 shows the plot of sequence-impedances seen by the relays (ref. Figure 4.1.) and the profiles of sequence trip-counters for a loaded transformer. Additional test results for an unloaded transformer operation are presented in Figures E.7 to E.9. Two more high-impedance fault results are shown by Figures E.10 and E.11 respectively. Figures E.12 and E.13 present additional results for the switch-on fault and magnetizing inrush Table E.1 presents the summary of additional results and provides a detailed information such as the parameters of current transformers, fault locations and the time required by the proposed technique to make decision on the type of faults.

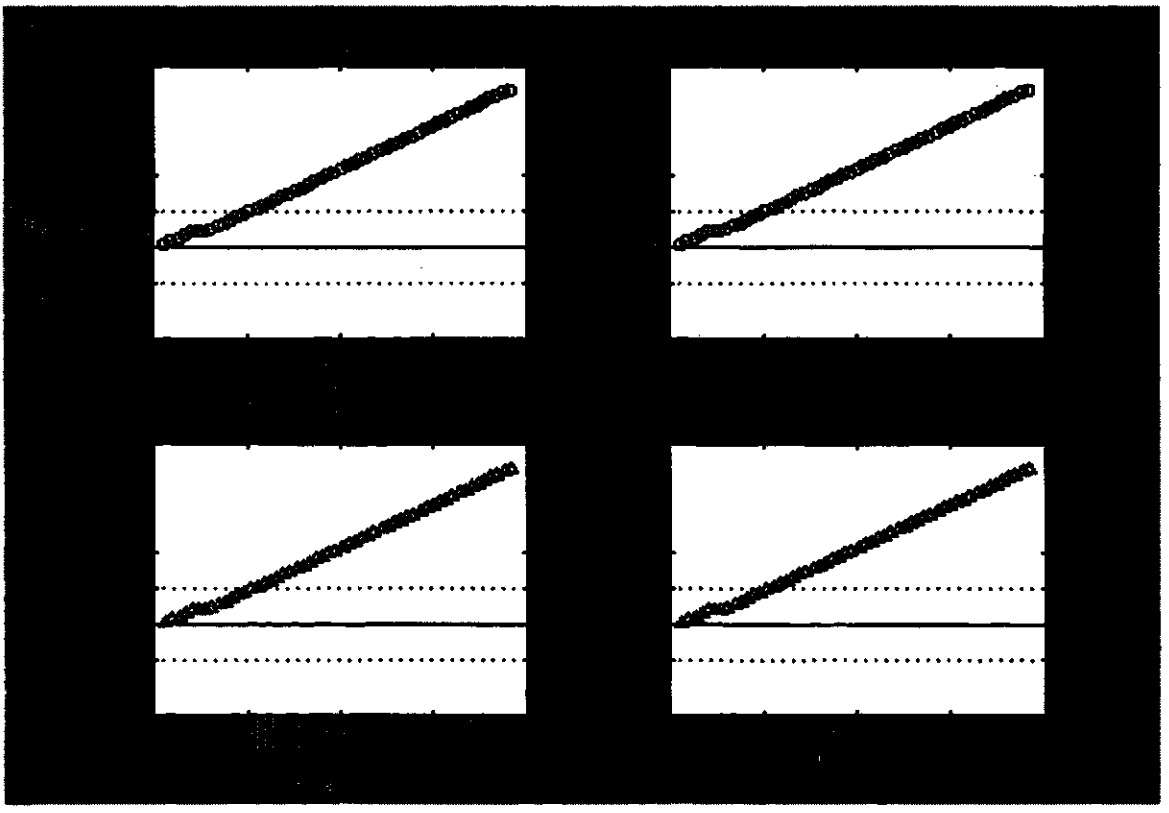


(a)



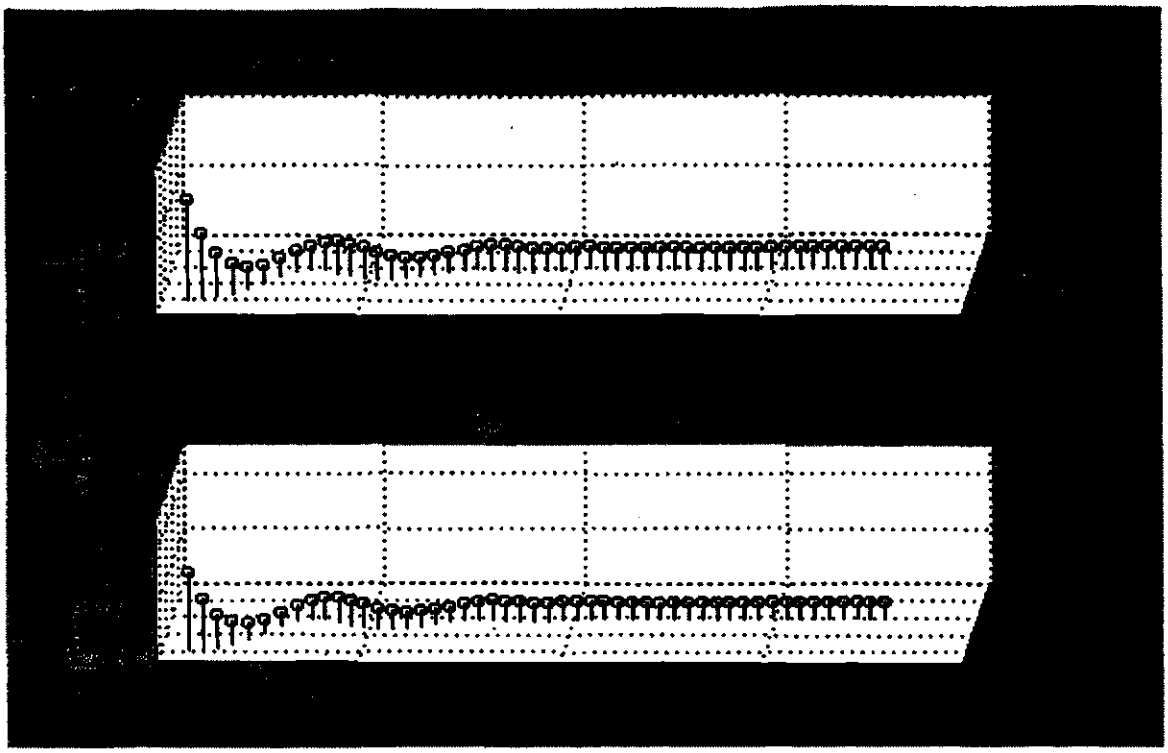
(b)

Figure E.1. Plot of (a) positive-sequence and (b) negative-sequence impedances for relays on two sides of power transformer for C-g internal fault in the 230 KV winding (location 3, Figure 4.1).

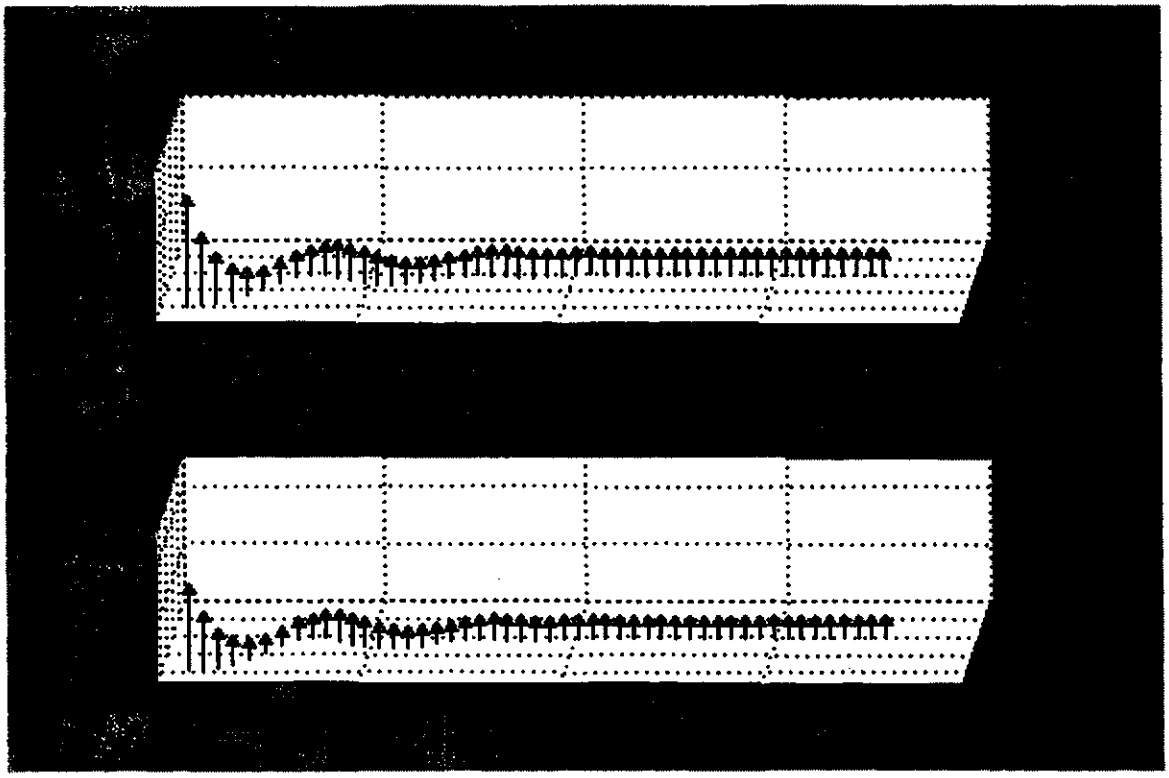


(c)

Figure E.1. Plot of (c) trip counters for relays on two sides of power transformer for C-g internal fault in the 230 KV winding (location 3, Figure 4.1).

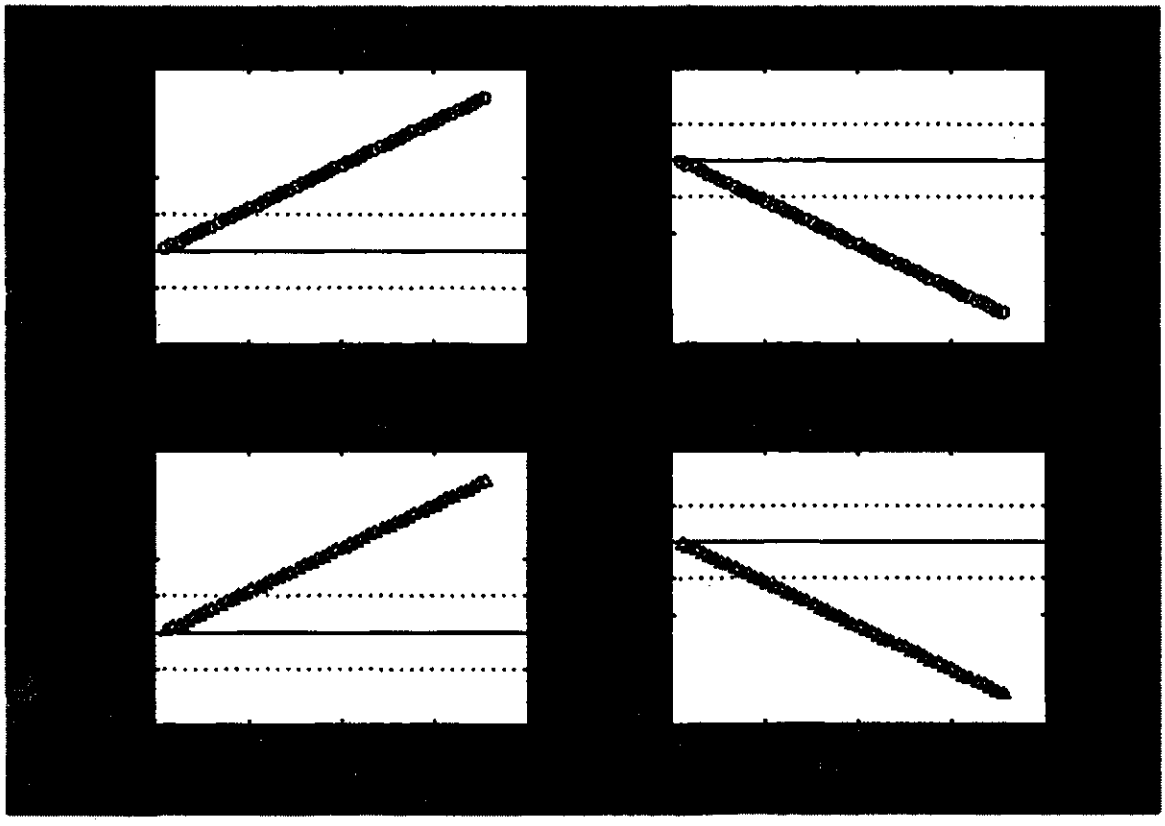


(a)



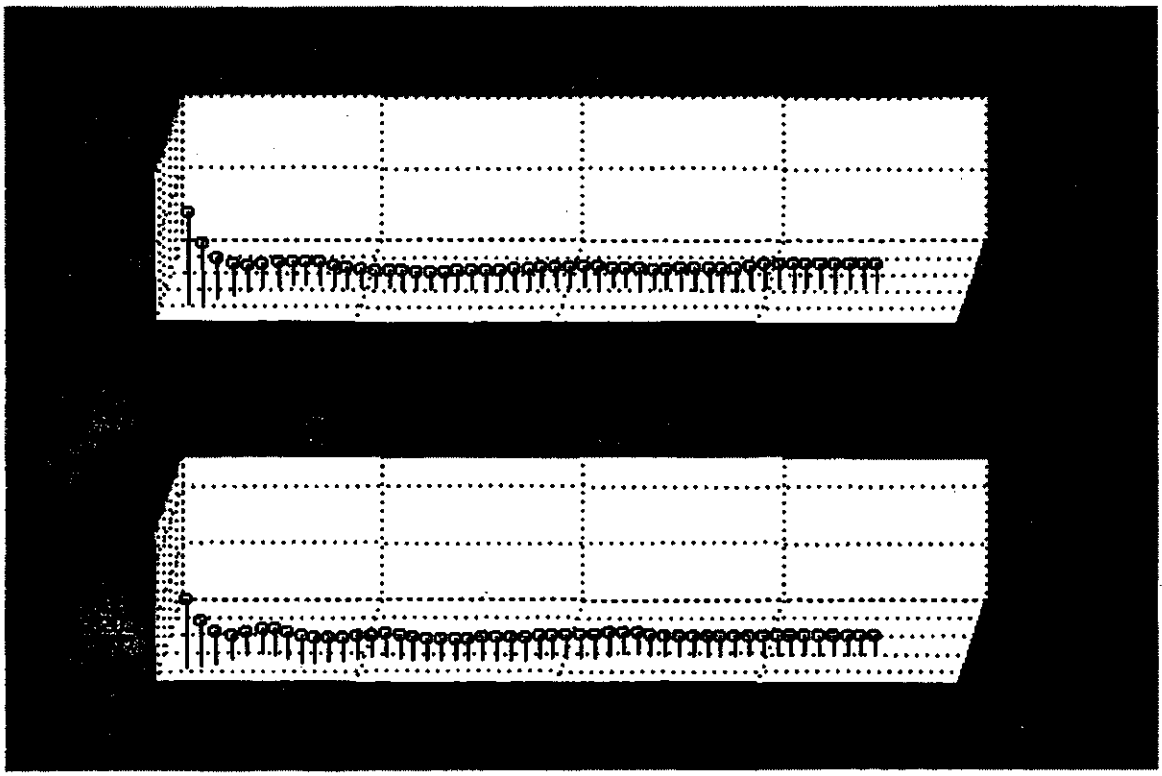
(b)

Figure E.2. Plot of (a) positive-sequence and (b) negative-sequence impedances for relays on two sides of power transformer for B-g external fault in the 230 KV winding (location 5, Figure 4.1).

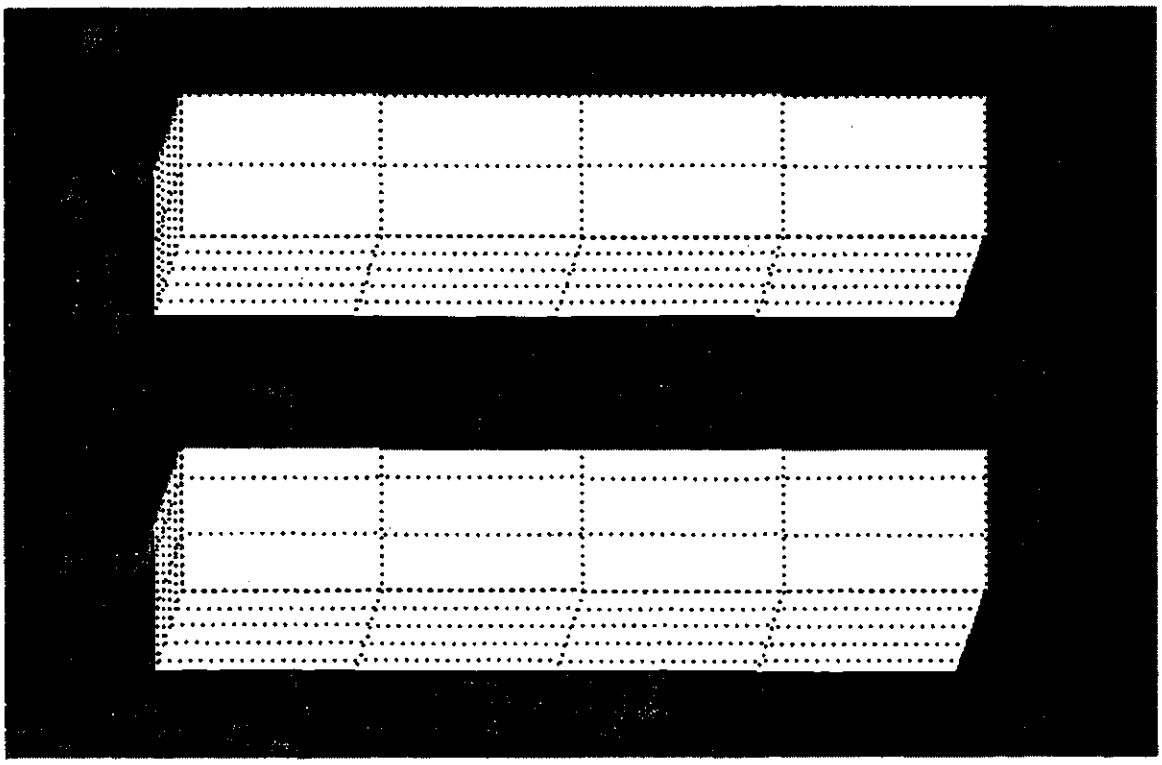


(c)

Figure E.2. Plot of (c) trip counters for relays on two sides of power transformer for B-g external fault on 230 KV side (location 5, Figure 4.1).

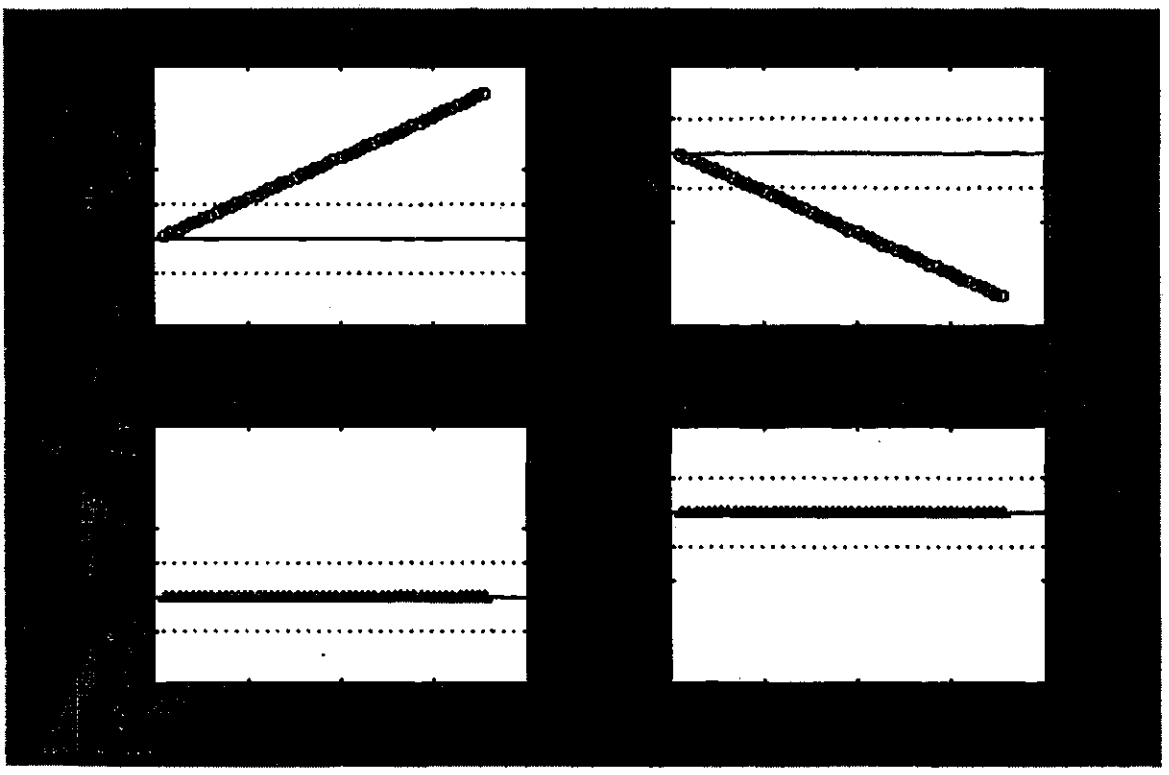


(a)



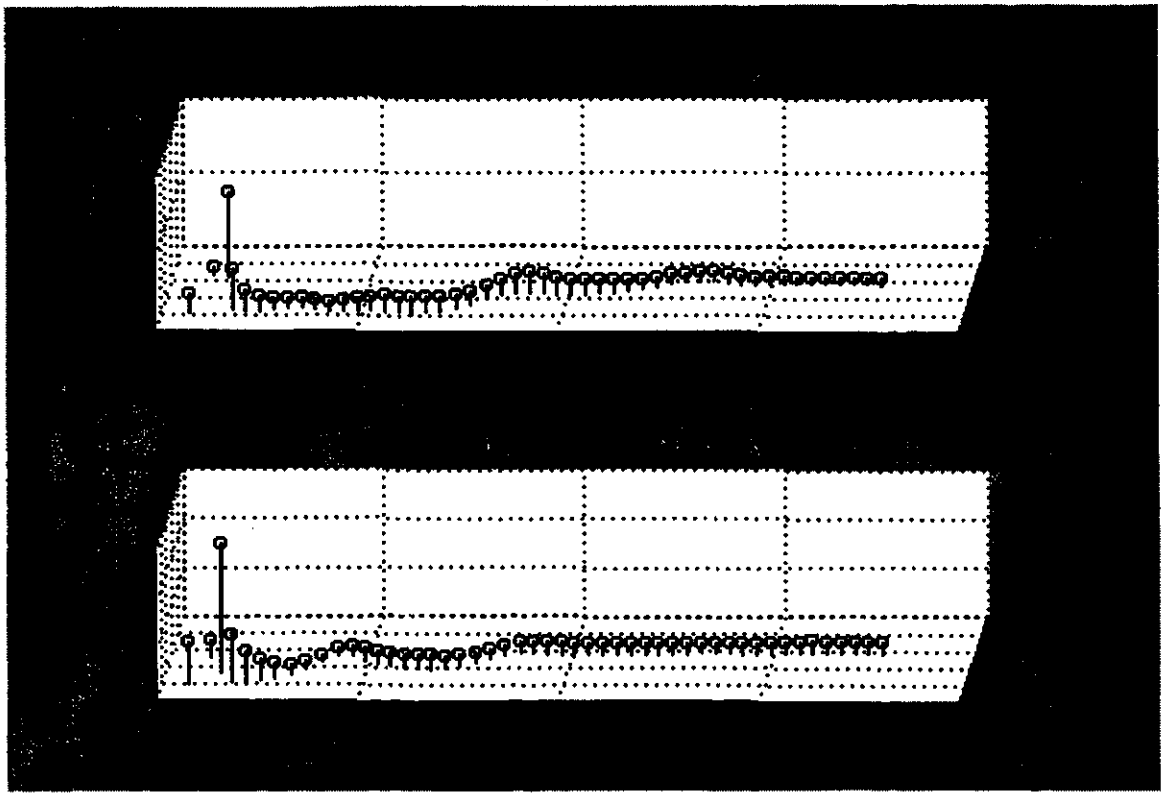
(b)

Figure E.3. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a three-phase external fault on the 230 kV side of the power transformer (location 5, Figure 4.1).

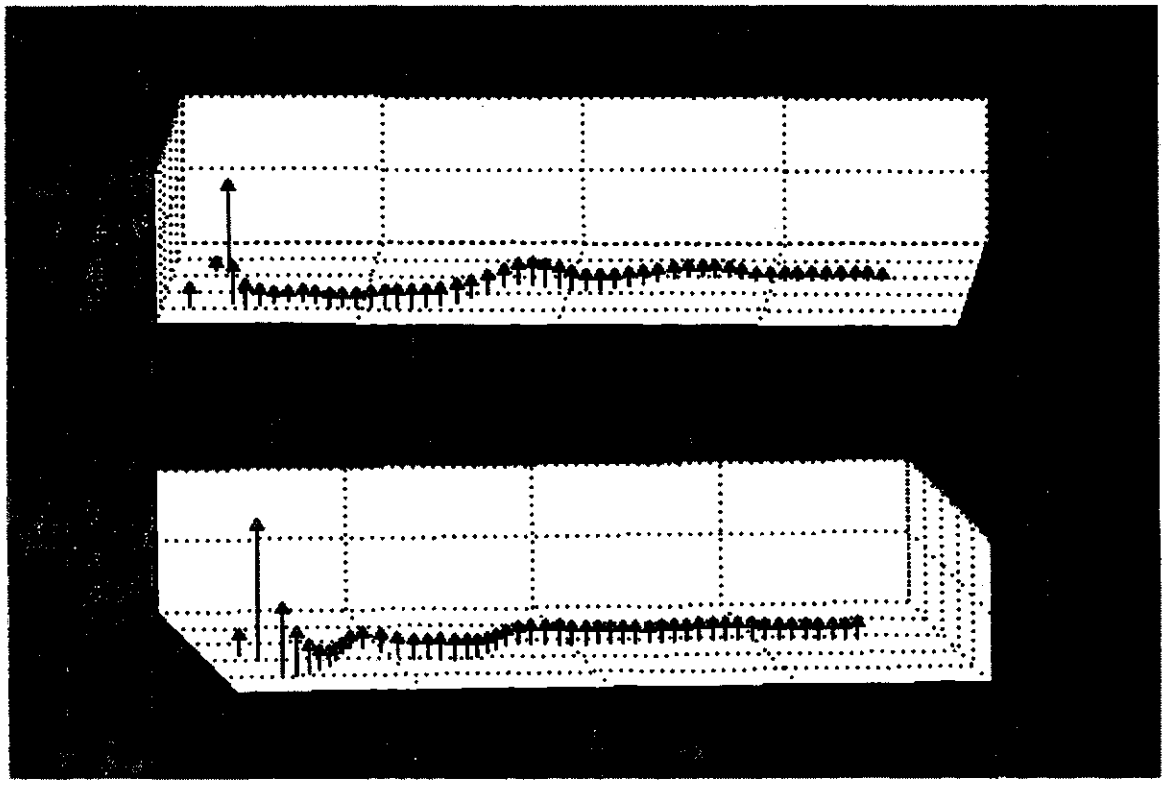


(c)

Figure E.3. Plot of (c) trip counters for three-phase external fault on 230 KV side of the power transformer (location 5, Figure 4.1).

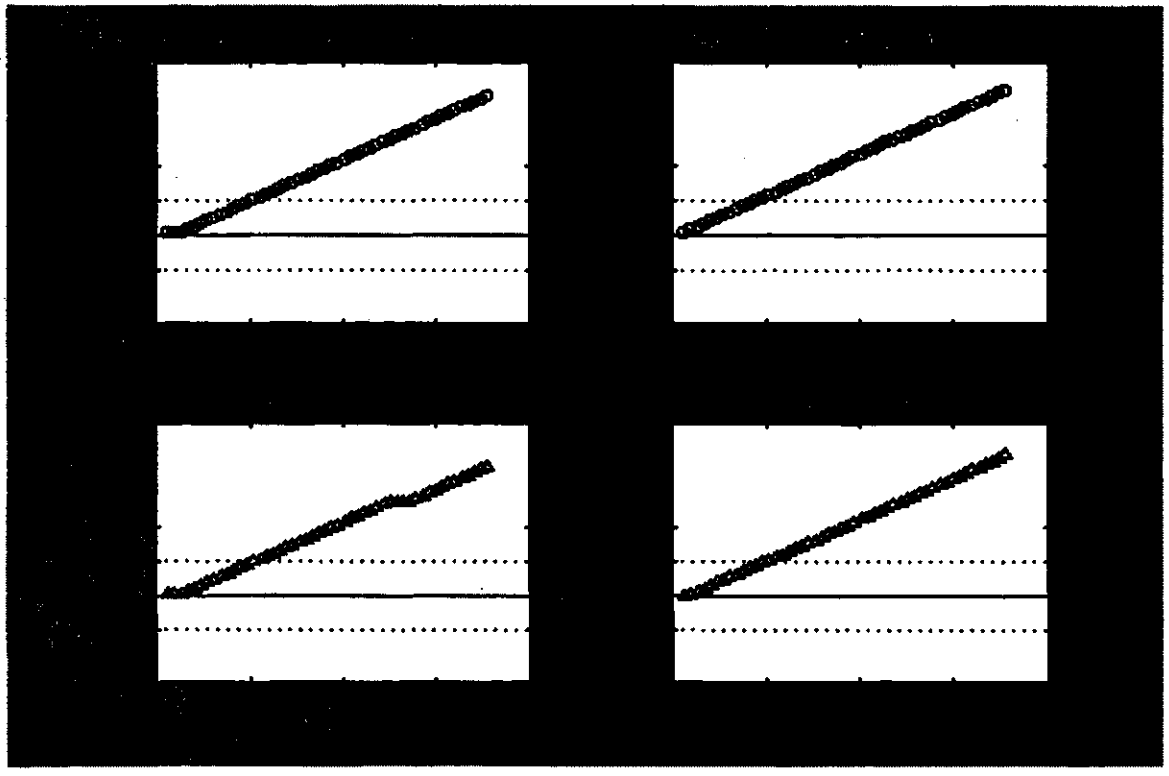


(a)



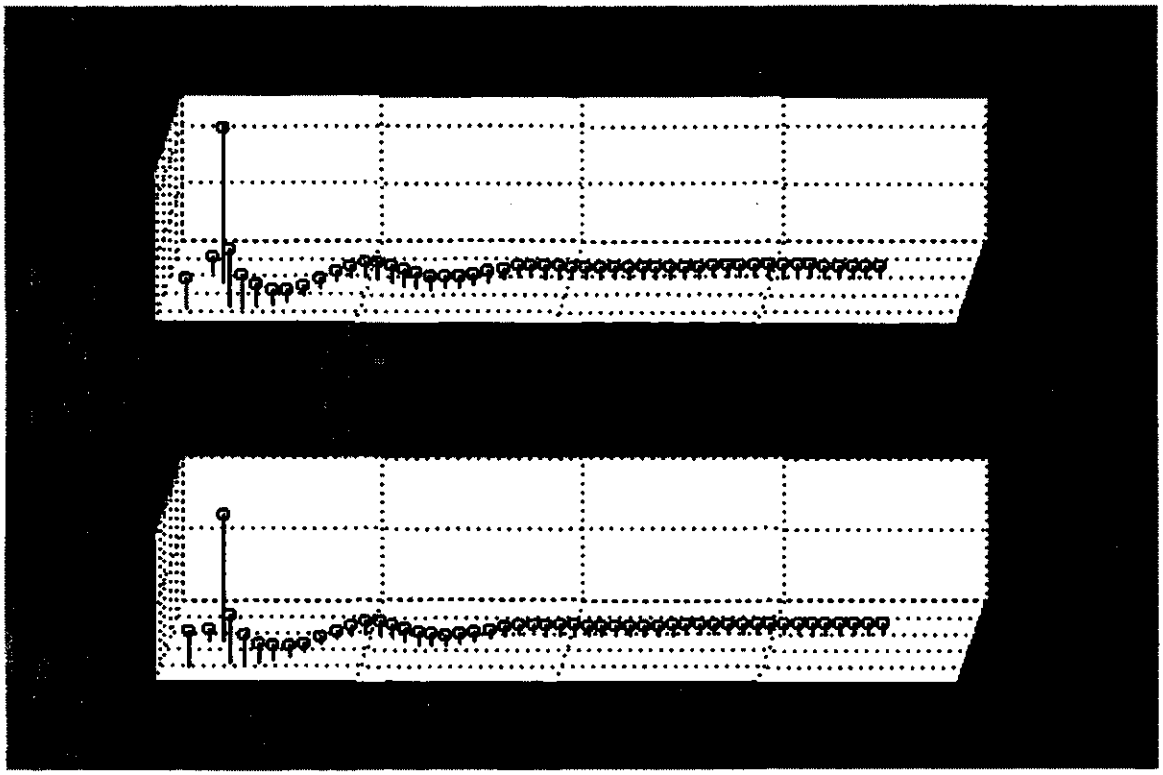
(b)

Figure E.4. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase C internal fault in the 13.8 kV winding of the power transformer (location 2, Figure 4.1).

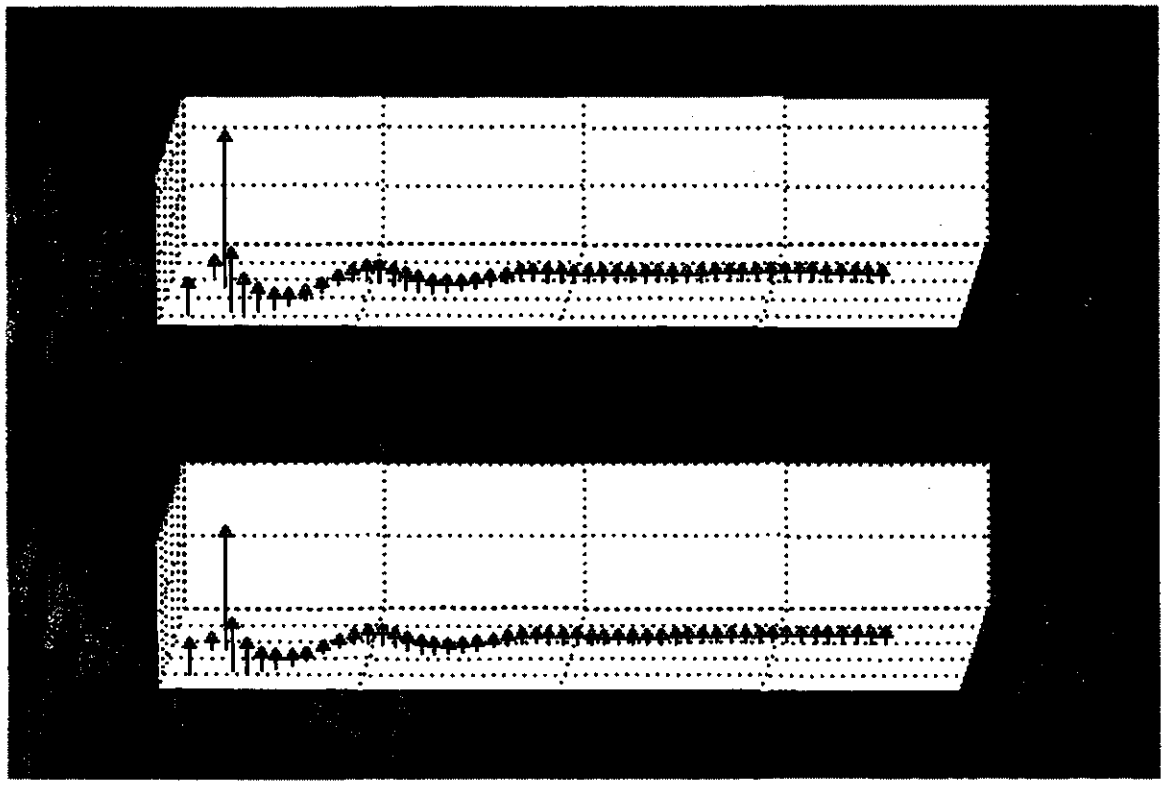


(c)

Figure E.4. Plot of (c) trip counters for Phase A-Phase C internal fault on 13.8 KV winding of the power transformer (location 2, Figure 4.1).

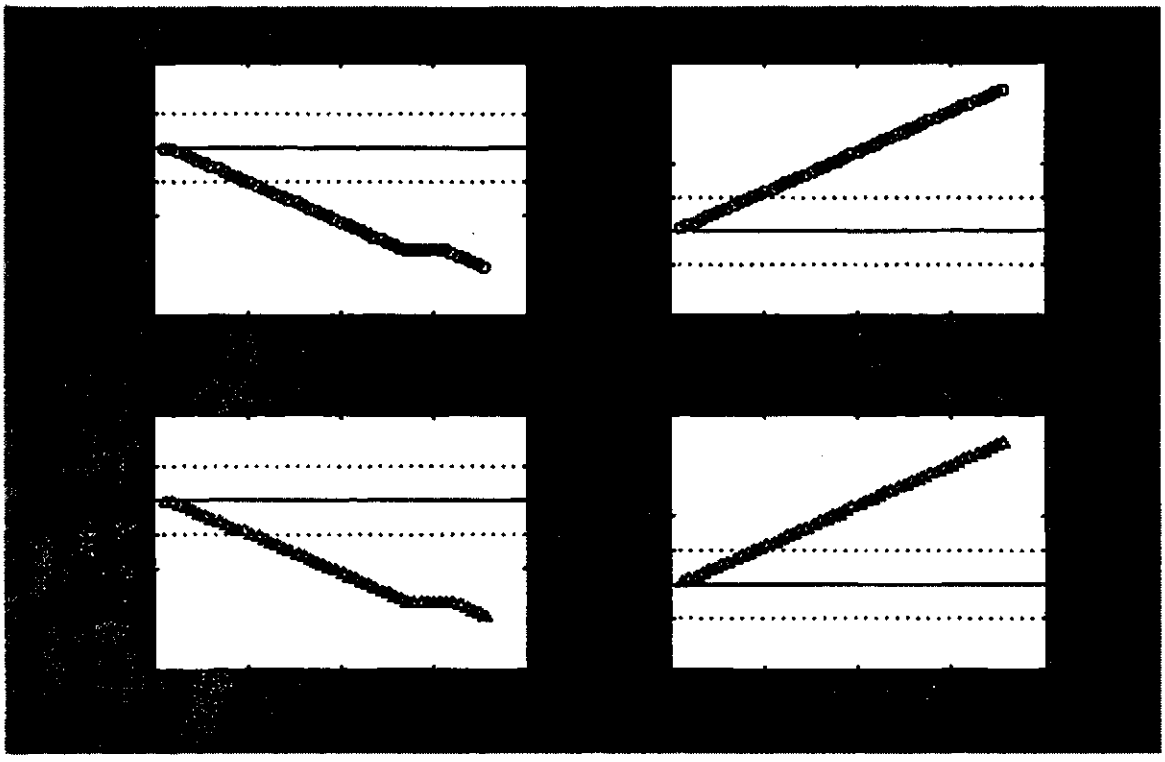


(a)



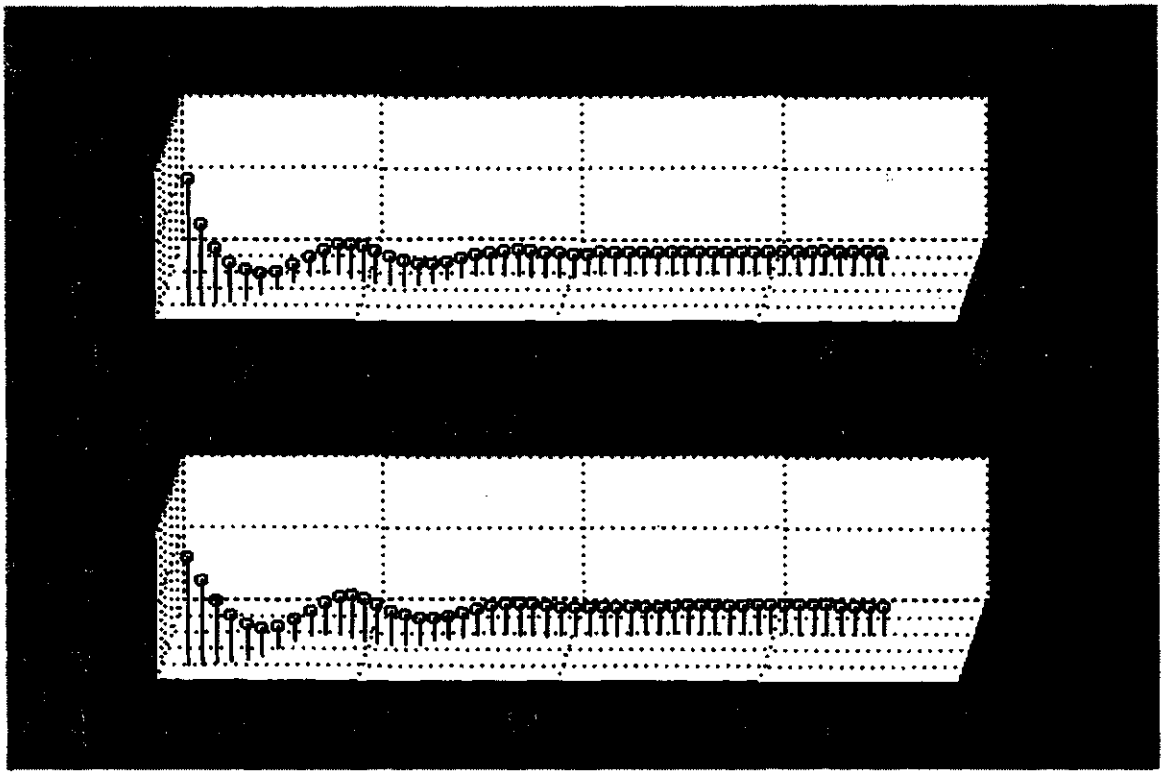
(b)

Figure E.5. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase C external fault on the 13.8 kV side of the power transformer (location 1, Figure 4.1).

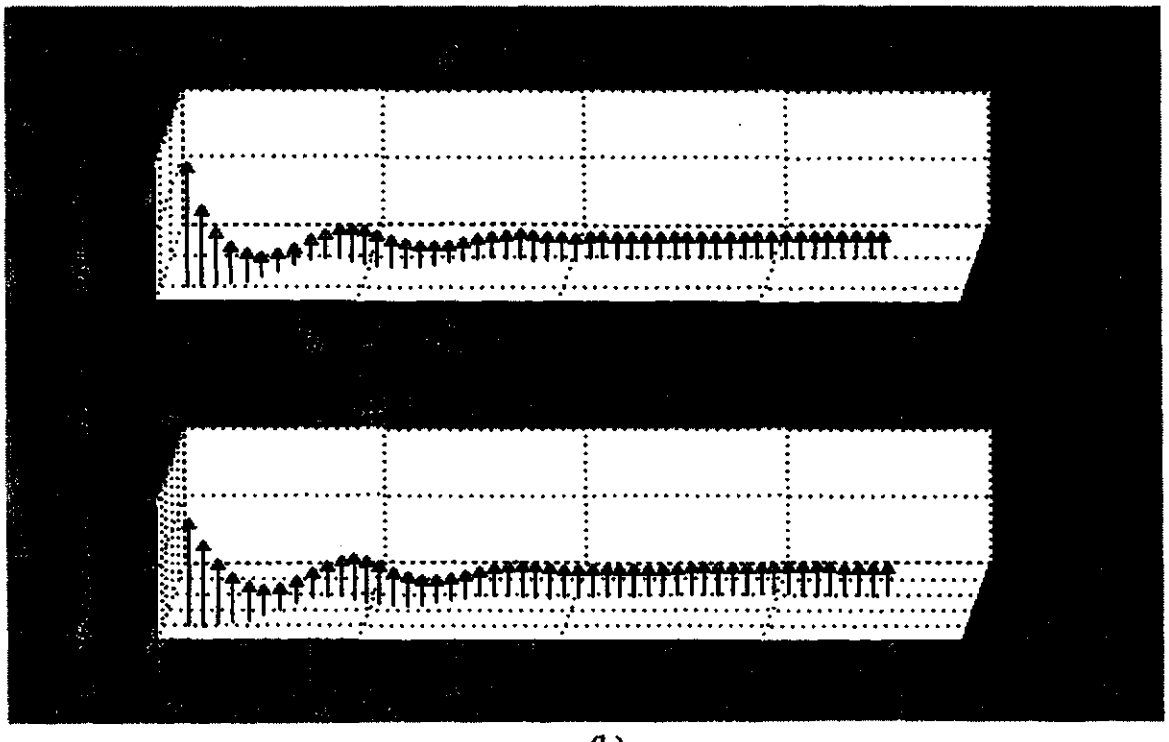


(c)

Figure E.5. Plot of (c) trip counters for Phase A-Phase C external fault on 13.8 KV side of the power transformer (location 1, Figure 4.1).

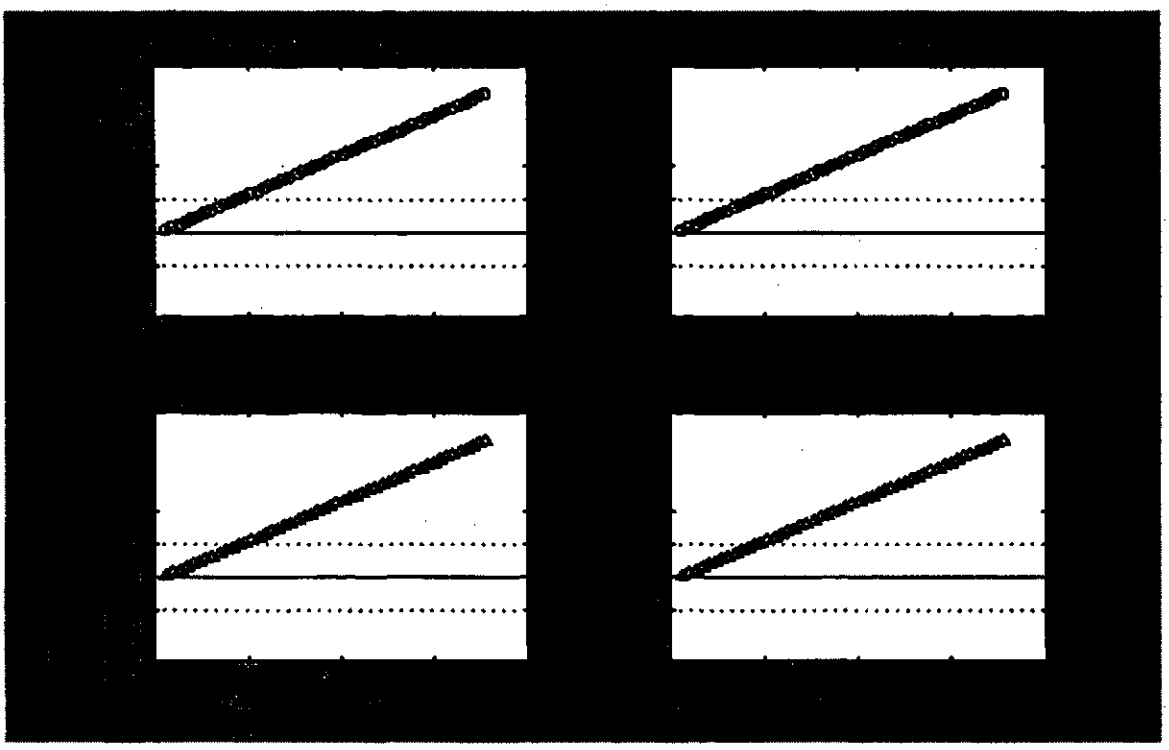


(a)



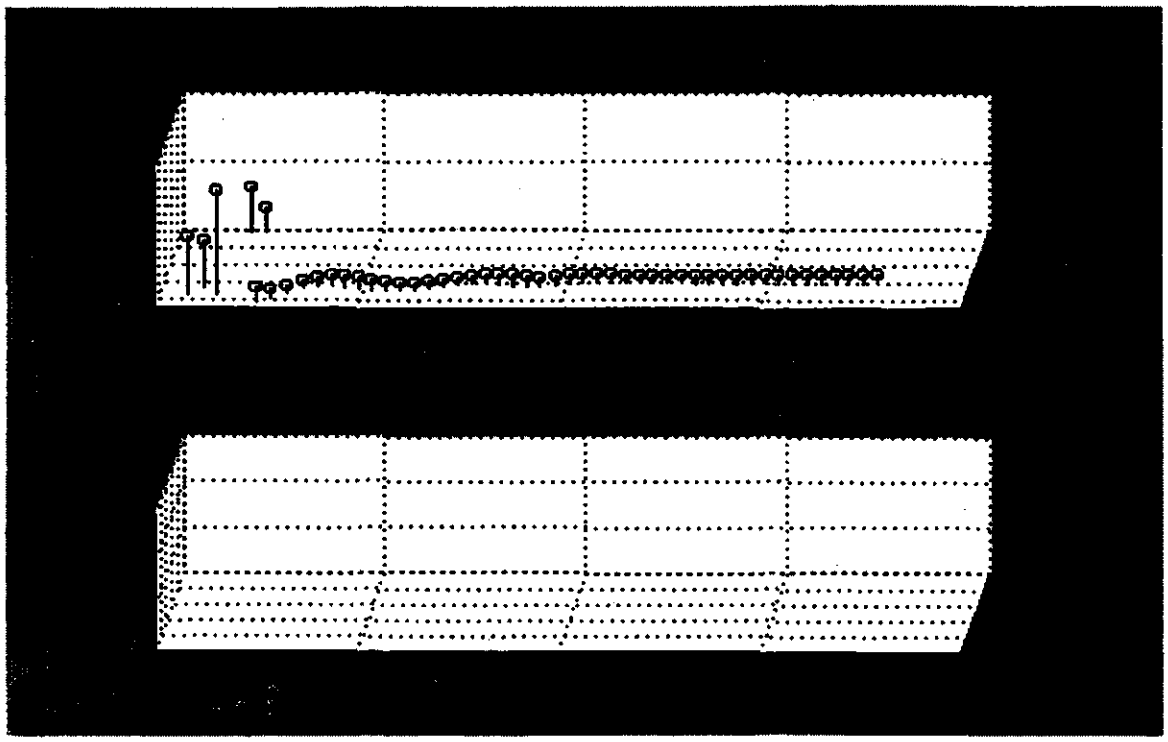
(b)

Figure E.6. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground internal fault on the 230 kV winding of the power transformer (location 3, Figure 4.1).

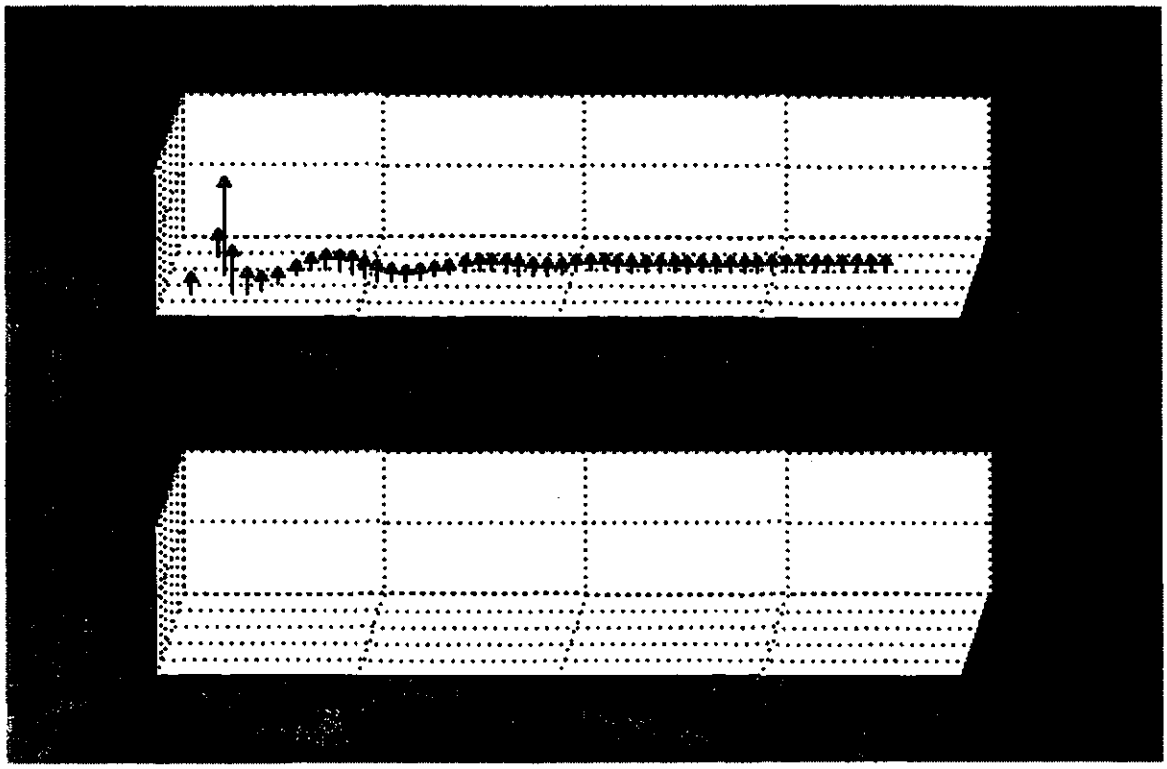


(c)

Figure E.6. Plot of (c) trip counters for Phase A-g internal fault in 13.8 KV winding of the power transformer (location 3, Figure 4.1).

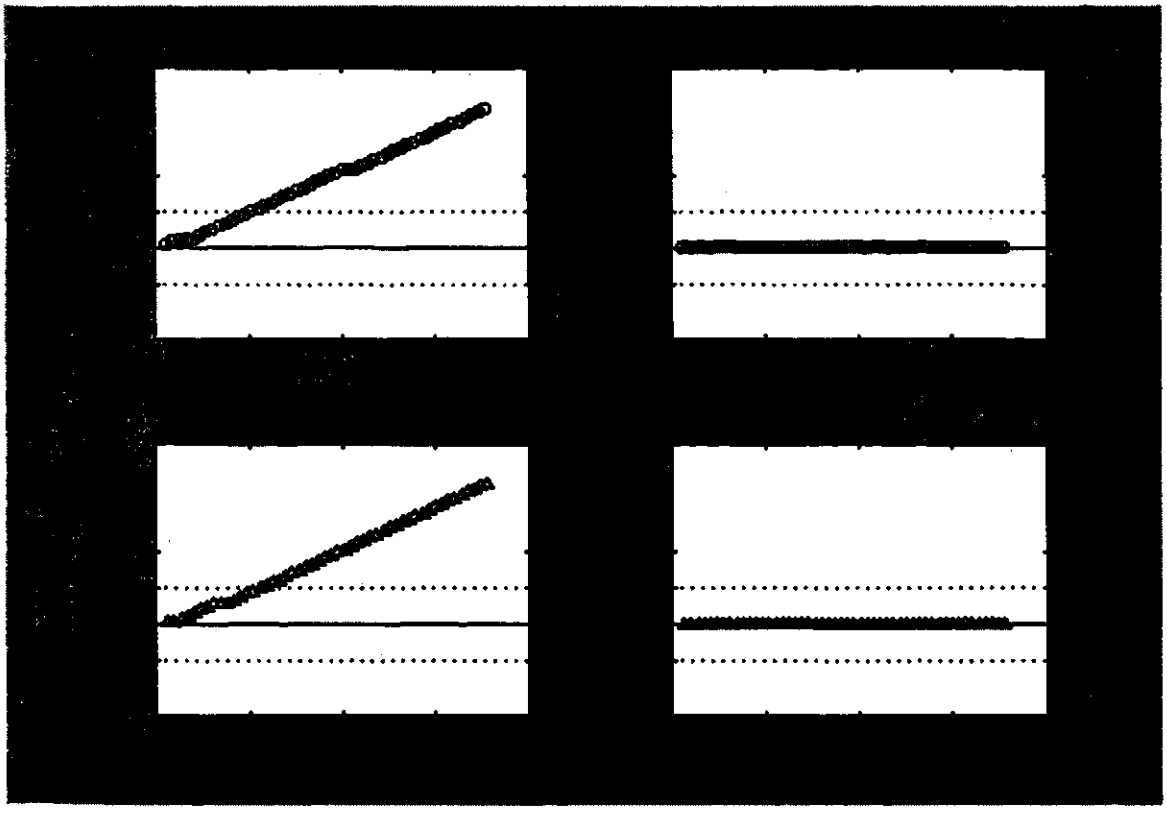


(a)



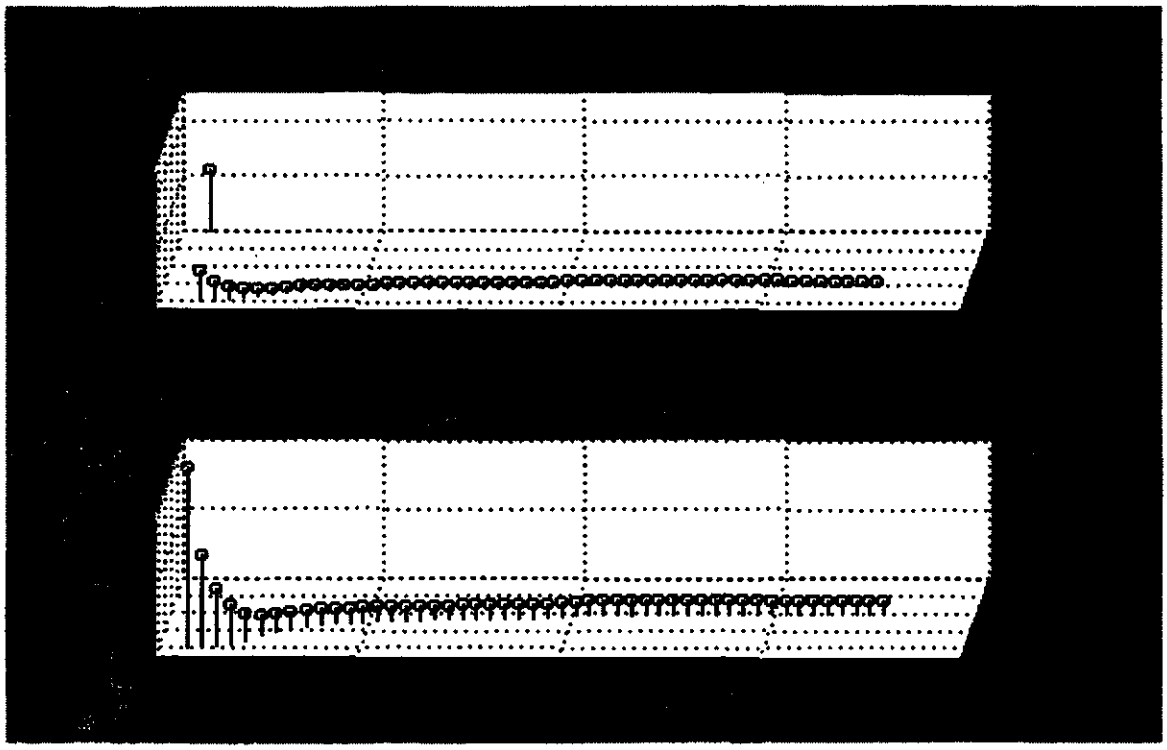
(b)

Figure E.7. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground internal fault on the 230 kV side of the unloaded transformer (location B, Figure 3.6).

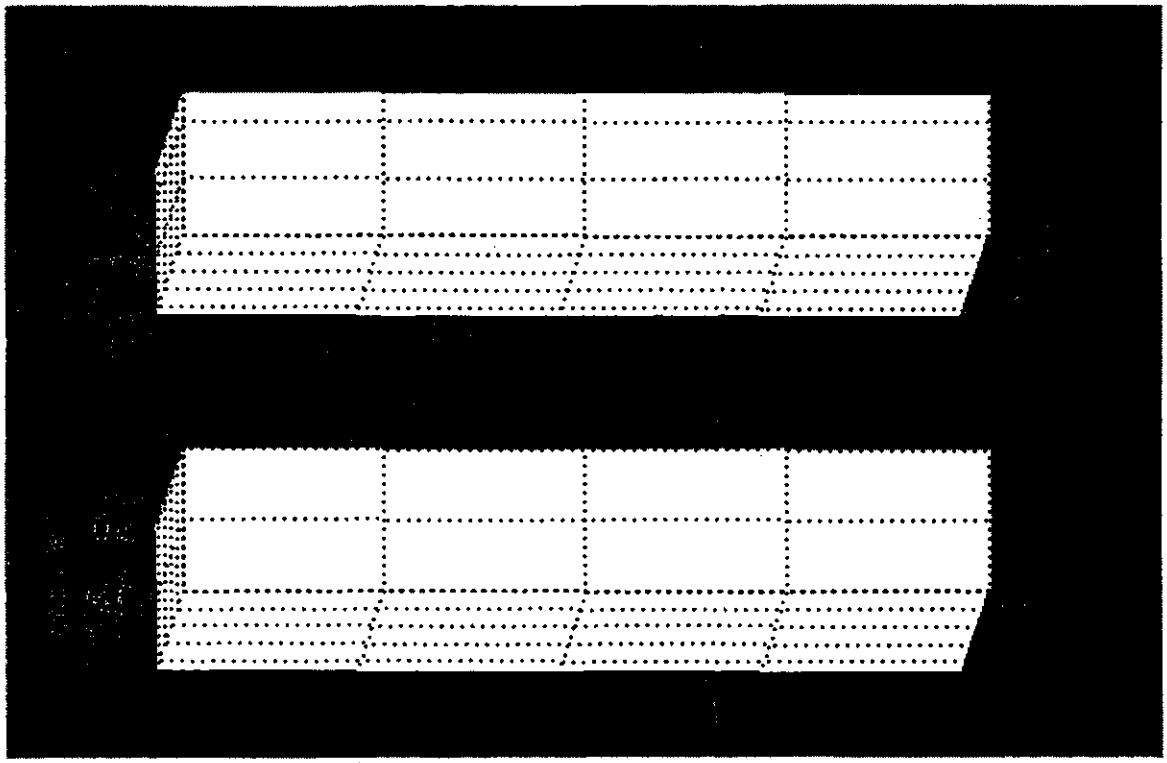


(c)

Figure E.7. Plot of (c) trip counters for a Phase A-ground internal fault on 230 kV side of the unloaded transformer (location B, Figure 3.6).

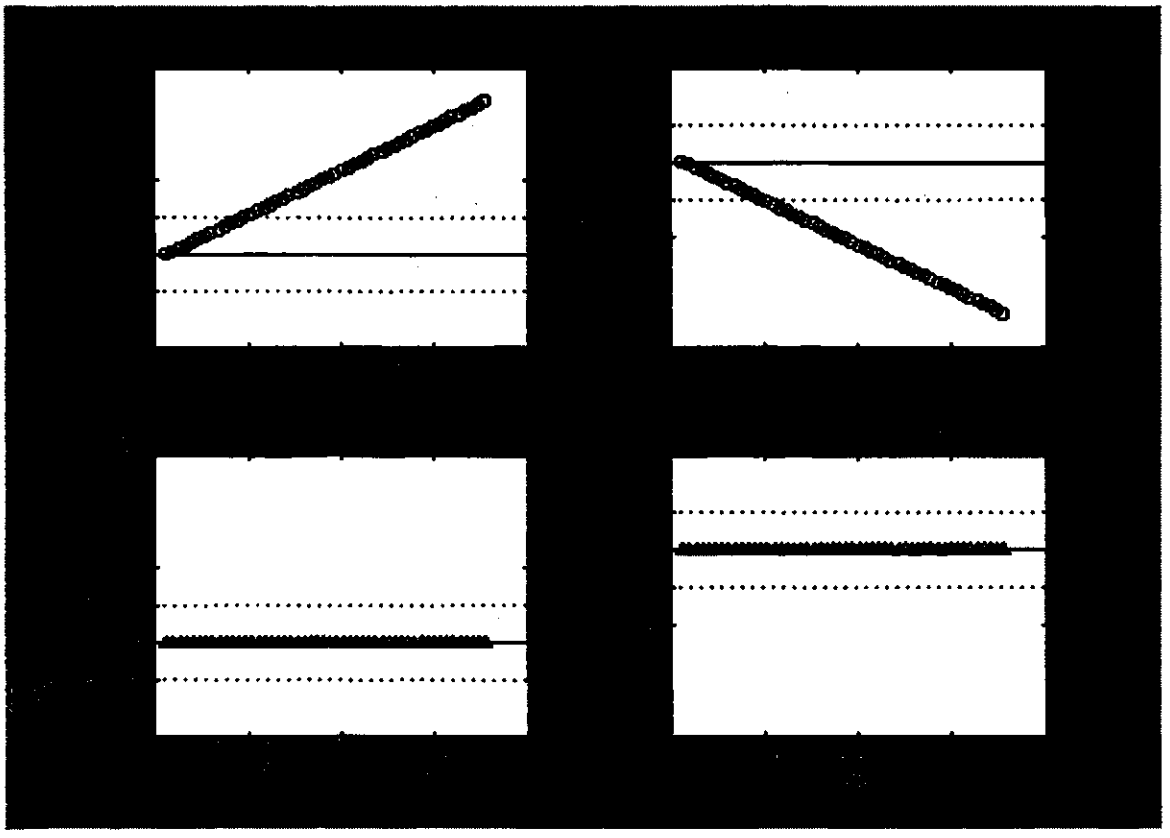


(a)



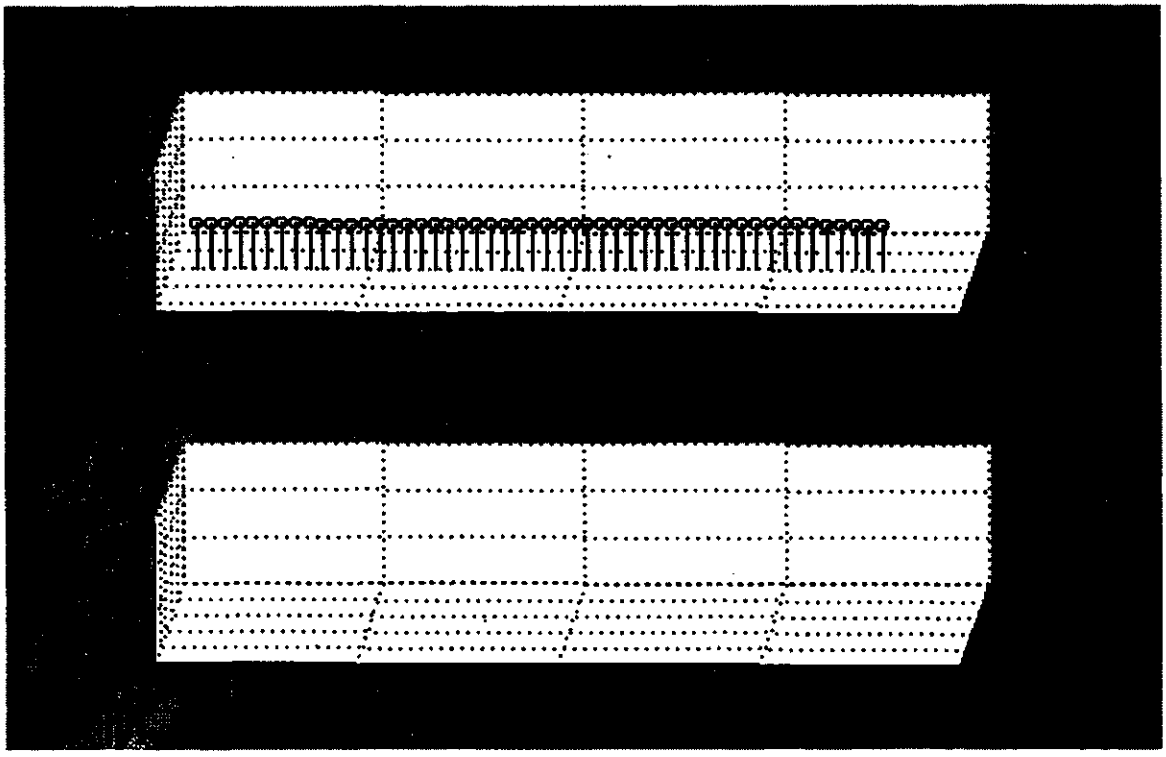
(b)

Figure E.8. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a three-phase external fault on the 230 kV side of the unloaded transformer (location A, Figure 3.6).

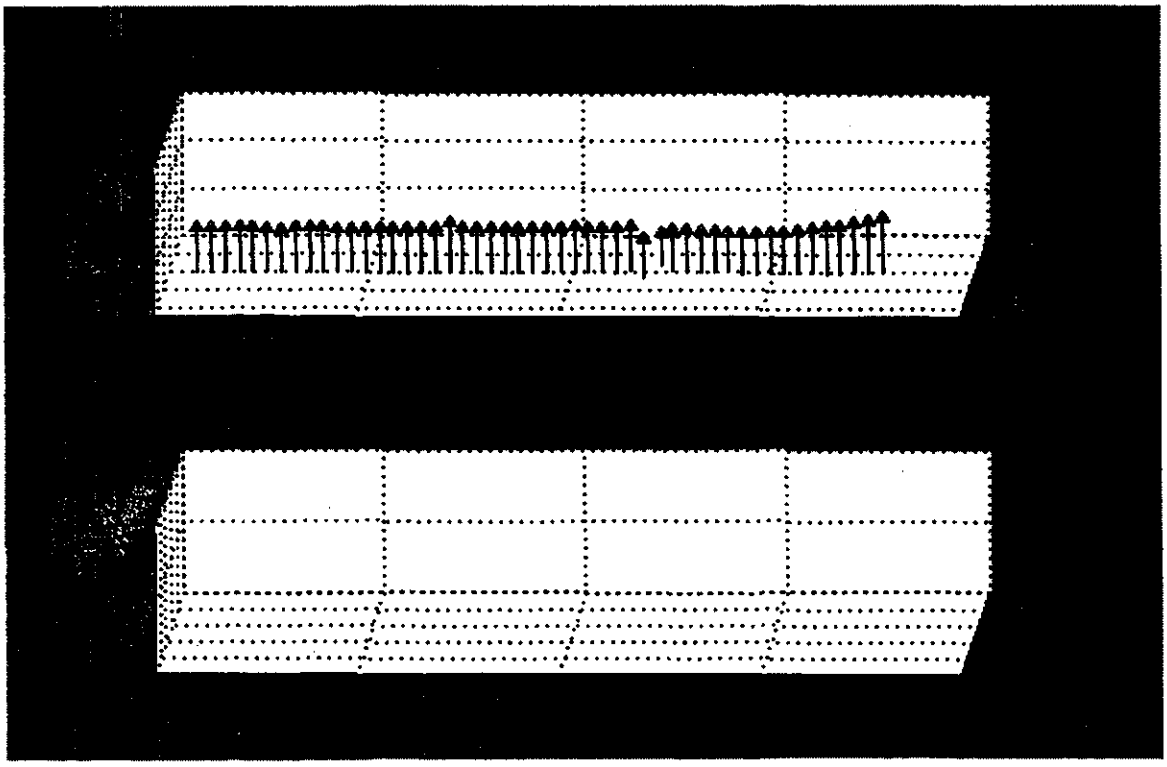


(c)

Figure E.8. Plot of (c) trip counters for a three-phase external fault on 230 kV side of the unloaded transformer (location A, Figure 3.6).

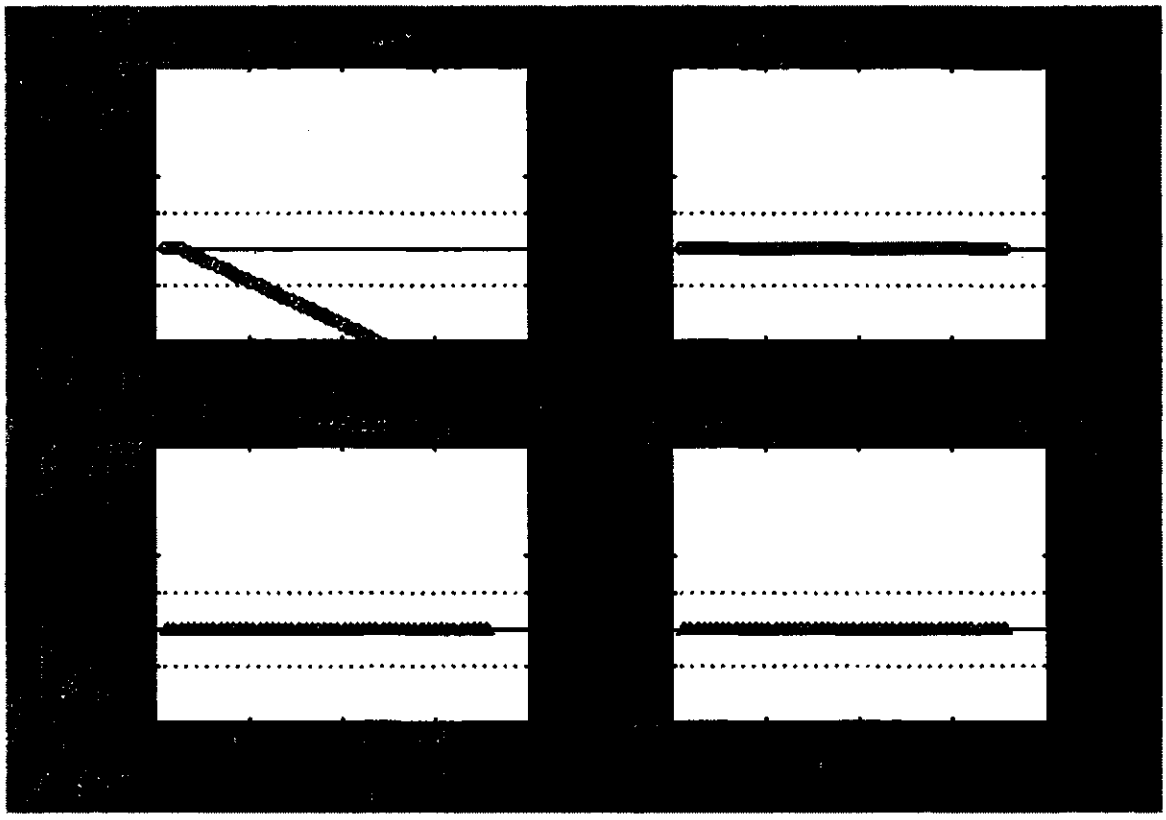


(a)



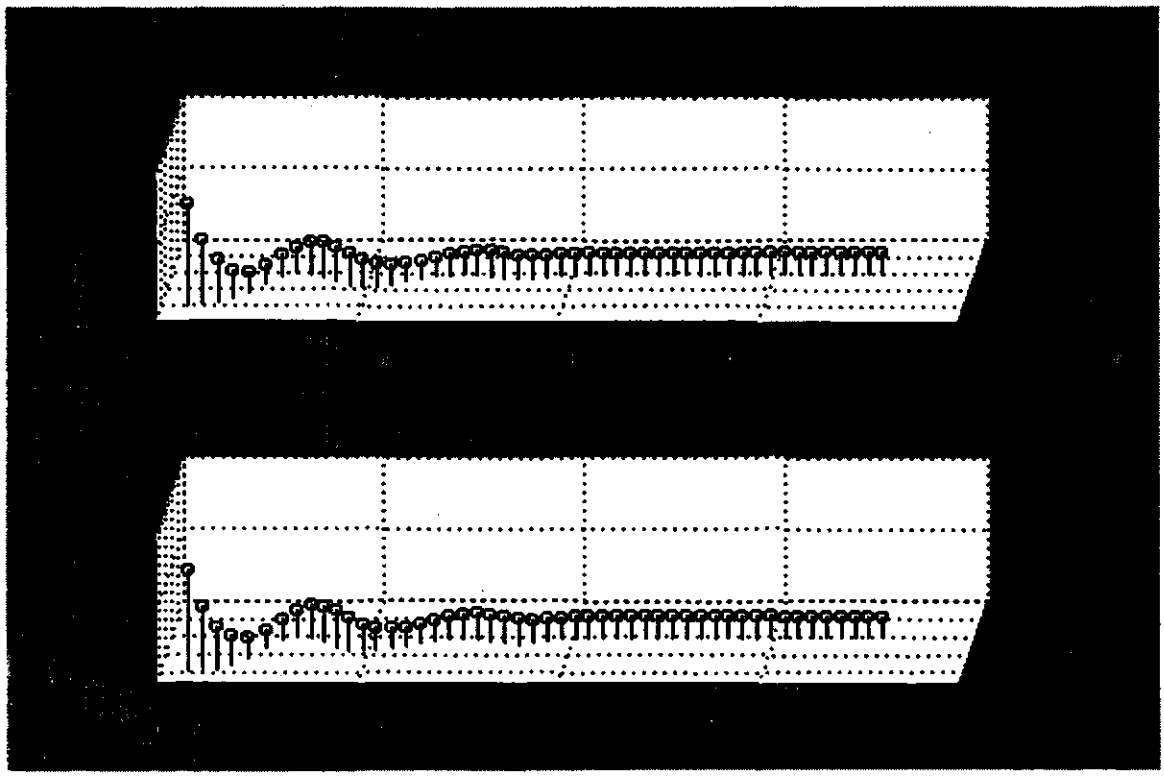
(b)

Figure E.9. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a three-phase external fault on the 13.8 kV side of the unloaded transformer.

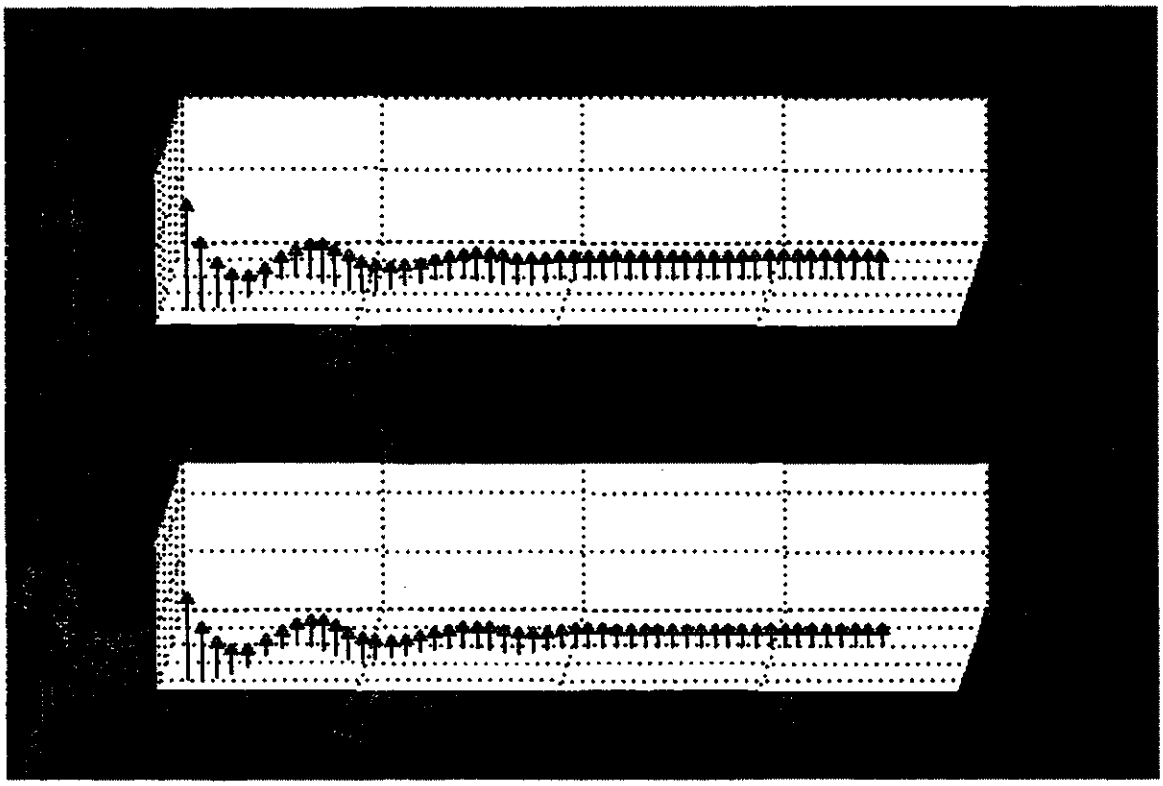


(c)

Figure E.9. Plot of (c) trip counters for a three-phase external fault on 13.8 kV side of the unloaded transformer.

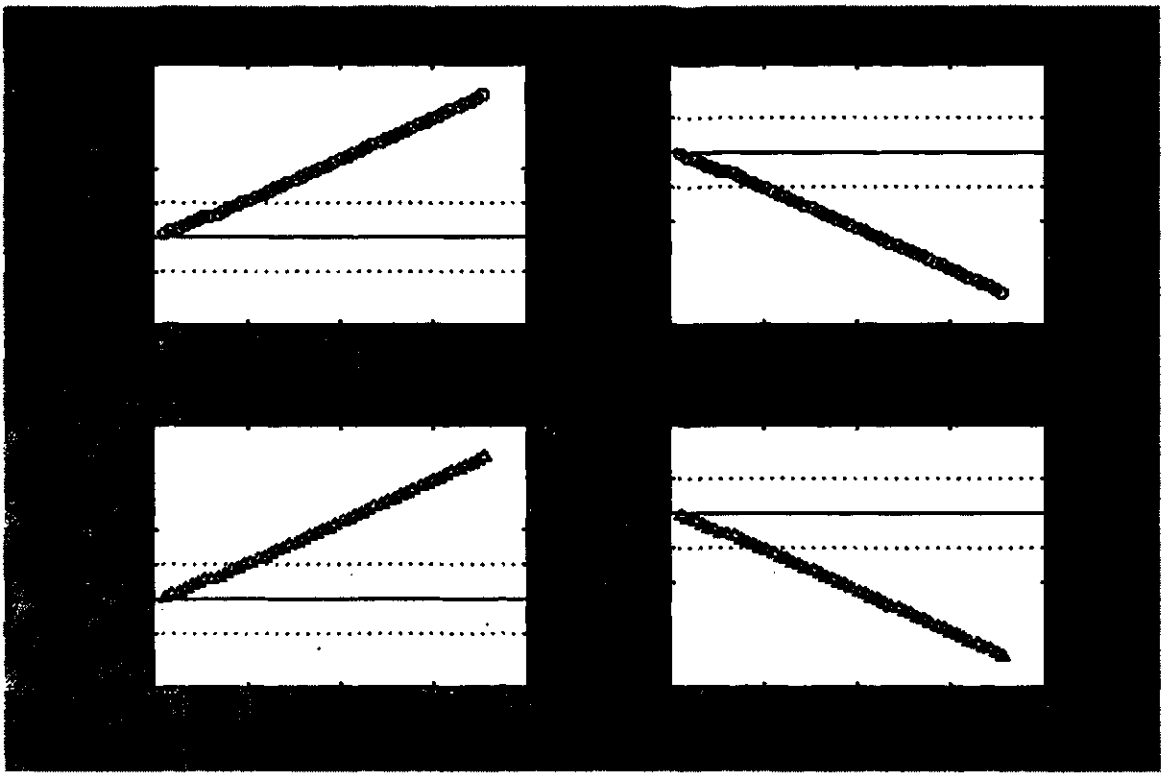


(a)



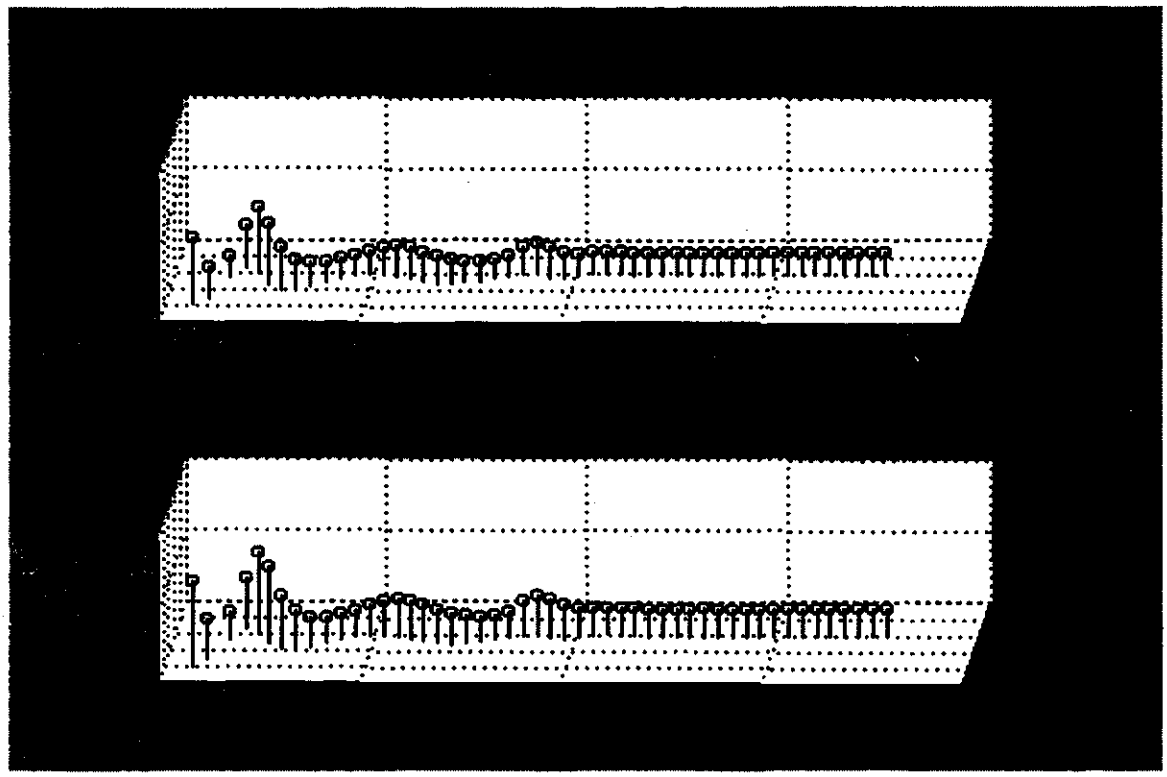
(b)

Figure E.10. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B external fault on the 230 kV side of the power transformer (location 5, Figure 4.1).



(c)

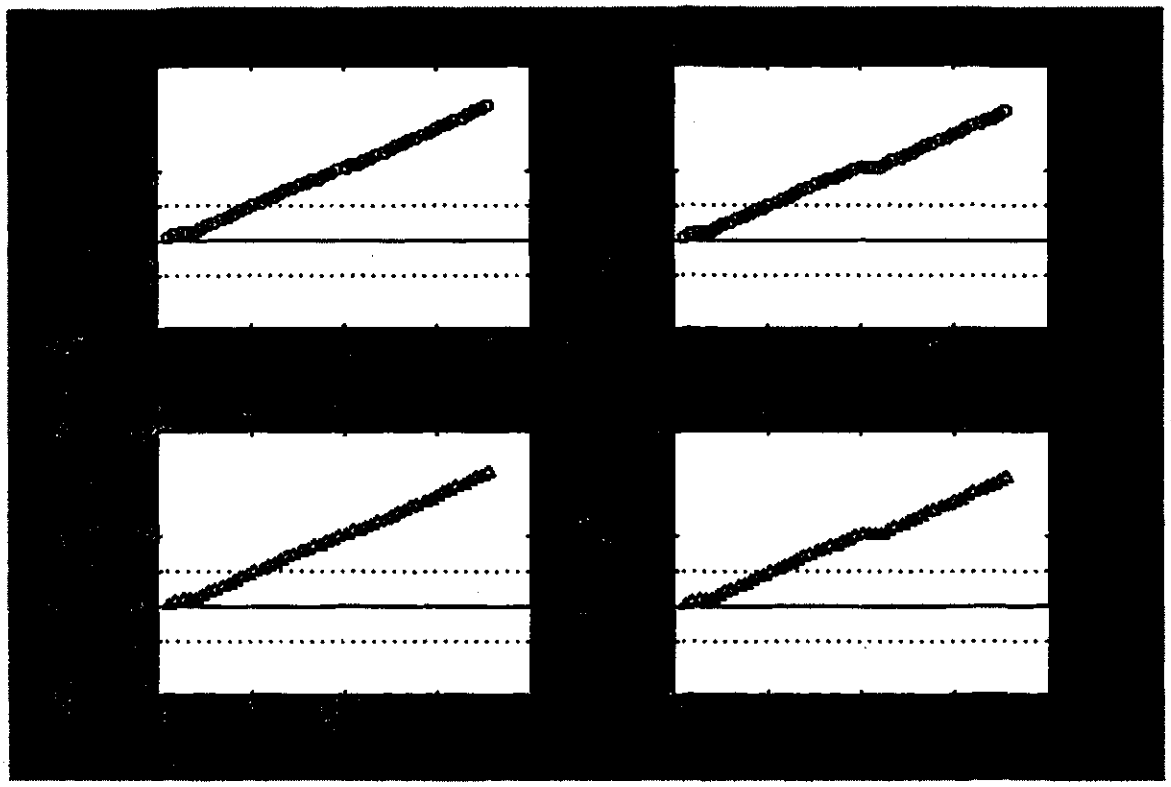
Figure E.10. Plot of (c) trip counters for a high-impedance Phase A-Phase B external fault on 230 KV side of the power transformer (location 5, Figure 4.1).



(a)

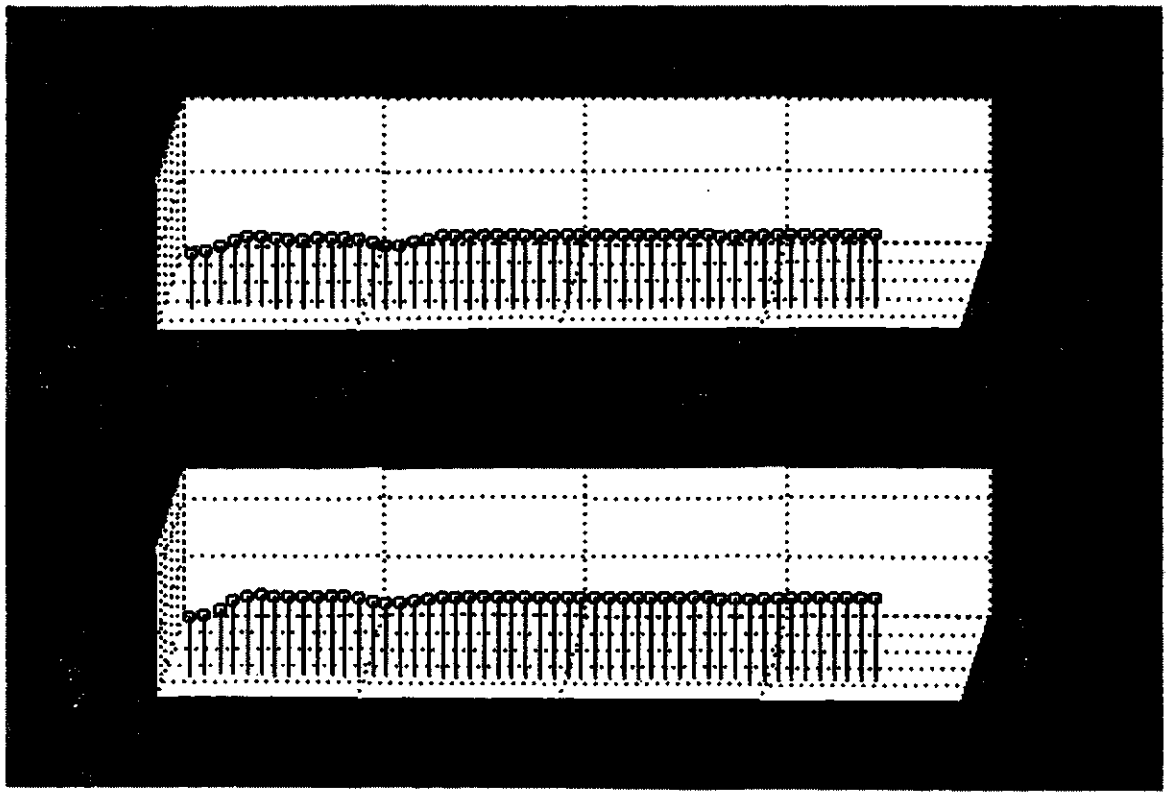
(b)

Figure E.11. Plot of (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase B-Phase C internal fault in the 13.8 kV winding of the power transformer (location 2, Figure 4.1).

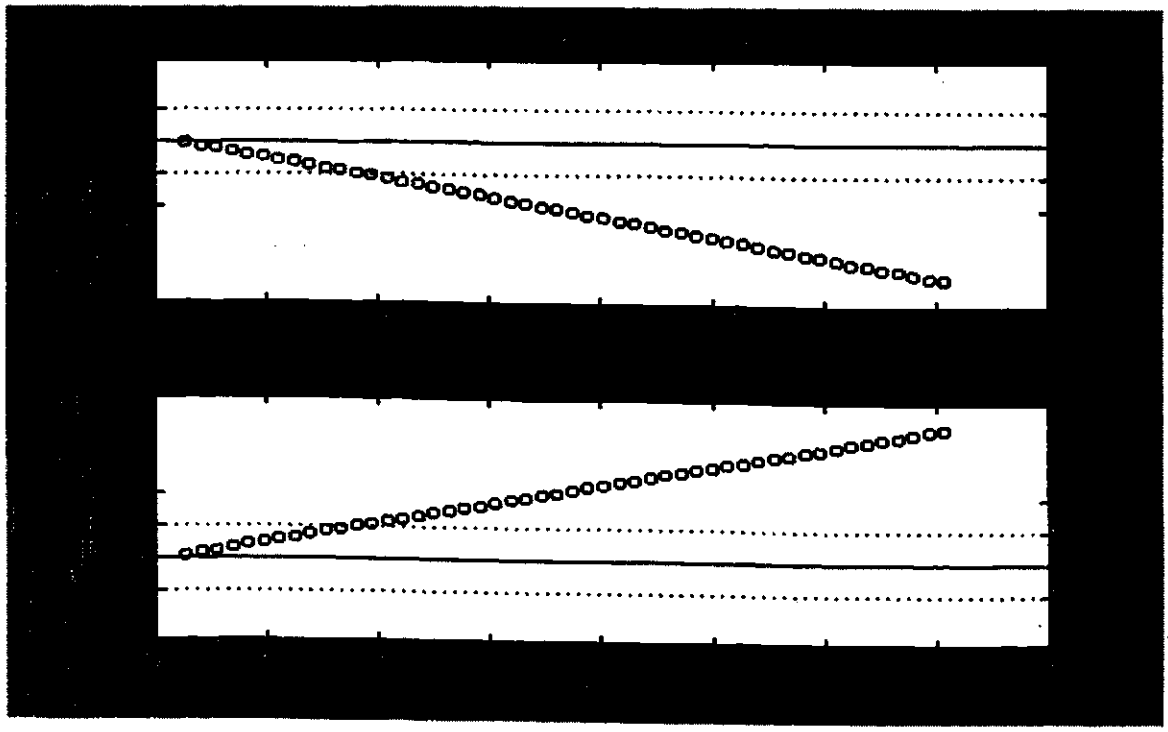


(c)

Figure E.11. Plot of (c) trip counters for a high-impedance Phase B-Phase C external fault on the 13.8 KV side of the power transformer (location 2, Figure 4.1).



(a)



(b)

Figure E.12. Plot of (a) positive-sequence impedance computed by the relays and (b) trip counters for Phase B-Phase C switch-on external fault for the power transformer (location A, Figure 3.14).

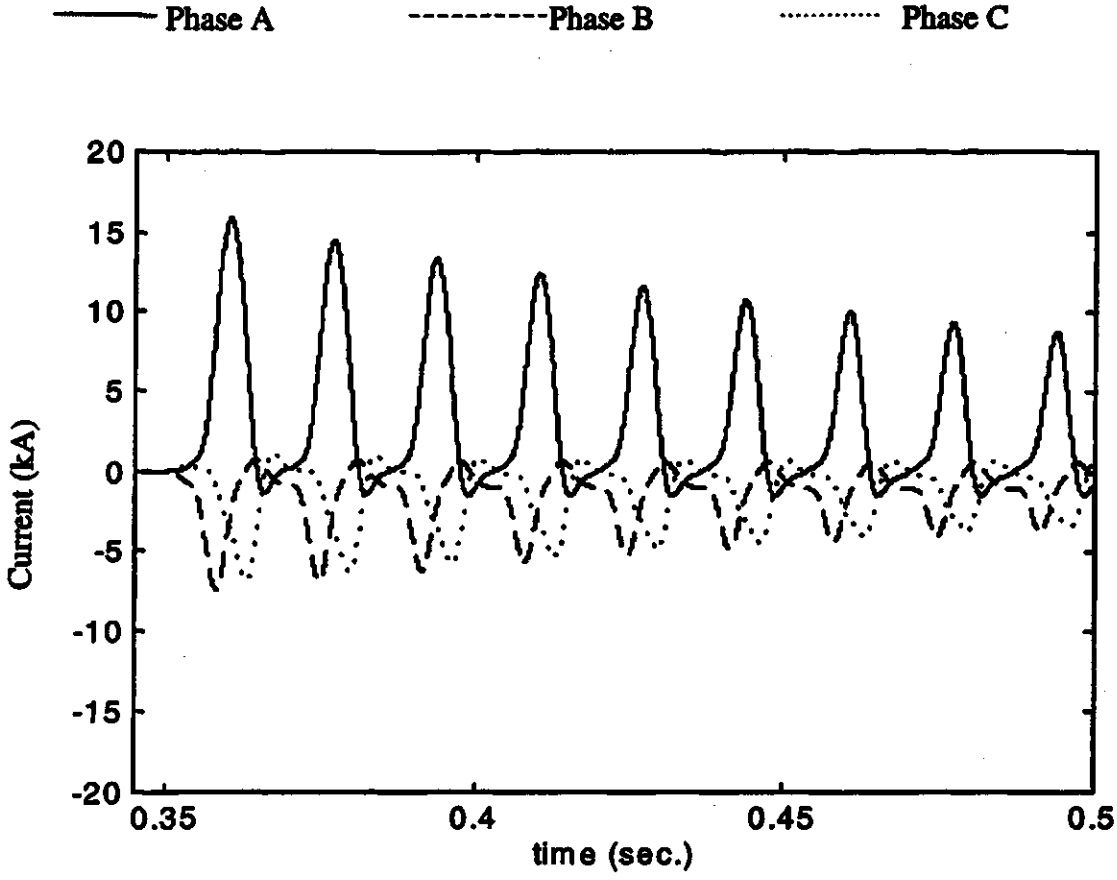


Figure E.13. Current waveforms on 13.8 KV side of the power transformer for magnetizing inrush condition (transformer switched-on at 0.35 seconds).

Table E.1. Summary of additional test results.

Figure No.	Fault Location (ref. Figure 4.1.)	Particulars	Fault-decision time (milliseconds)
E.1.	3	Phase C - ground fault	10.4
E.2.	5	Phase B - ground fault	9.0
E.3.	5	Three - phase fault, ct saturated. Phase 13.8 KV 230 KV A *(840,40.0) *(50,10.0) B *(840,0.5) *(50,10.0) C *(840,40.0) *(50,10.0)	9.0
E.4.	2	Phase A - Phase C fault, ct saturated. Phase 13.8 KV 230 KV A *(600,30.0) *(50,5.0) B *(840,0.5) *(50,0.5) C *(600,30.0) *(50,5.0)	10.4
E.5.	1	Phase A - Phase C fault, Ratio-Mismatch condition. Ratio of all cts on 13.8 KV=840 Ratio of all cts on 230 KV=35	9.7
E.6.	3	Phase A - ground fault, Ratio-Mismatch condition. Ratio of all cts on 13.8 KV=1000 Ratio of all cts on 230 KV=50	9.0
E.7.	B (Fig. 3.6)	Internal fault in 230 kV side Unloaded transformer	11.1

*(ct ratio,burden resistance)

Table E.1 (contd.). Summary of additional test results.

Figure No.	Fault Location (ref. Figure 4.1.)	Particulars	Fault-decision time (milliseconds)
E.8.	A (Fig. 3.6)	External fault in 230 kV side Unloaded transformer	9.7
E.9.	13.8 kV side (Fig. 3.6)	External fault in 13.8 kV side Unloaded transformer	11.1
E.10.	5	Phase A - Phase B fault, High-impedance fault Fault Resistance=70.0 ohms	9.7
E.11.	2	Phase B - Phase C fault, High-impedance fault Fault Resistance=3.5 ohms	10.4
E.12.	A (Figure 3.14)	Phase B - Phase C fault, Switch-on external fault.	9.0
E.13.	(Figure 3.14.)	Magnetizing Inrush condition, Transformer switched-on at 0.35 seconds.	