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UNIVERSITY OF SASKATCHEWAN

DEPARTMENT OF ELECTRICAL ENGINEERING

CERTIFICATION OF THESIS WORK

We, the undersigned, certify that Chandrasekara Sivakumar, candidate for the Degree of Master of Science in Electrical Engineering, has presented his thesis on the subject Regenerative Frequency Divider

that this thesis is acceptable in form and content, and that this student demonstrated a satisfactory knowledge of the field covered by his thesis in an oral examination held on March 20, 1990.

External Examiner: George J. Gabor

of Physics Department

Internal Examiners:

A. E. Kramer

Arun Bhattacharyya

Ron Botton

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REGENERATIVE FREQUENCY DIVIDER

A Thesis

Submitted to the College of Graduate Studies and Research

in Partial Fulfilment of the Requirements

for the Degree of

Master of Science

in the

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by

C. Sivakumar

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UNIVERSITY OF SASKATCHEWAN

Electrical Engineering Abstract 89 A317

Regenerative Frequency Divider

Student: C. Sivakumar Supervisor: Dr. S. Kumar

M. Sc. Thesis Presented to the
College or Graduate Studies and Research

April 1990

ABSTRACT

A broad-band microwave frequency divider at "C" band (4-8 GHz) is designed using the regenerative frequency division concept. A simple method of obtaining a non-linear model to characterise the actual active device is followed in this thesis. The various non-linear phenomena occuring in a GaAs FET are used in designing the divider.

The divider with an input matching circuit and an output matching circuit with a GaAs FET for the purpose of regeneration is implemented through the use of a computer-aided-design, which leads to an accurate and reliable design ready for MIC realisation. A schematic design procedure for such a divider along with the measured and simulation results are presented.

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LIST OF ABBREVIATIONS

S-parameter	Scattering parameter
f_{in}	Input frequency
f_o	Output frequency
S^{-1}	Inverse scattering parameter
H.B.	Harmonic balance
Freq	Frequency
GaAs FET	Galium Arsenide Field-Effect-Transistor
dBm	Decibel per milliwatt
C-A-D	Computer-aided-design
P_{in}	Input power
P_{out}	Output power
V_{bi}	Built in potential
Psub	Subharmonic power
Pfund	Fundemental power

1. INTRODUCTION

1.1. Background

A microwave frequency divider circuit has applications in a wide variety of microwave sub-systems. One common example is its use in dividing down the frequency of an output sample of a microwave phase-locked-oscillator or direct microwave modulator. The divided down signal is then processed to generate the feedback control signal for the oscillator or modulator. A Frequency Shift Keying (FSK) direct modulator [7] which employs microwave frequency division is shown in Figure 1.1.

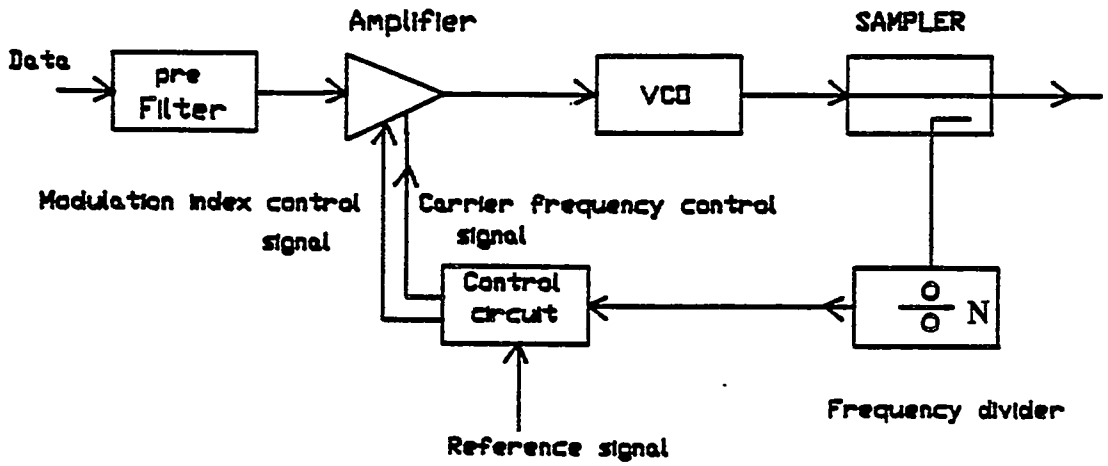

Figure 1.1: Block Diagram of an FSK Modulator

As shown in Figure 1.1 a voltage controlled oscillator (VCO) is frequency-shift-keyed

with prefiltered data. Before feeding the prefiltered data to the VCO, it is passed through an amplifier whose gain is controlled by the modulation-index control signal. A sample of the modulated output is frequency divided to a low frequency range and is then fed to the control circuit. Here the divided signal is compared with the reference clock signal to generate feedback control signals for the nominal carrier frequency and modulation-index. These modulation-index and nominal carrier frequency control signals are used to control the AC gain and DC bias output of the control amplifier respectively.

Frequency dividers are also used in a variety of other microwave sub-systems such as counters and carrier recovery circuits. Some of the common methods of obtaining frequency division are by:

1. Using varactors for parametric subharmonic generation [3].
2. Using an active device with suitable feedback or regenerative frequency divider [4].

Varactor is the name given to a voltage variable capacitor obtained by using a diode. Varactors are commonly used as two-terminal nonlinear reactance devices in frequency dividers. A varactor equivalent circuit used in a divider is shown in Figure 1.2. The elements L_s and L_e are the parasitic elements due to the package. The current i(v) is the current passing through the p-n junction. When the applied voltage changes, charge is added or removed in the p-n junction. This causes the width of the depletion region to vary. The depletion region widens for the reverse bias ($v<0$) and shrinks for the forward bias ($v>0$). The charge resulting when the p-n junction is reverse biased is called depletion layer charge. A forward bias voltage causes a change in the minority carrier distribution giving rise to injected minority carrier charge. Frequency division with varactors is realized by using the nonlinear current variation of the p-n junction current [3]. The varactor frequency divider circuit is designed and optimized by using a nonlinear

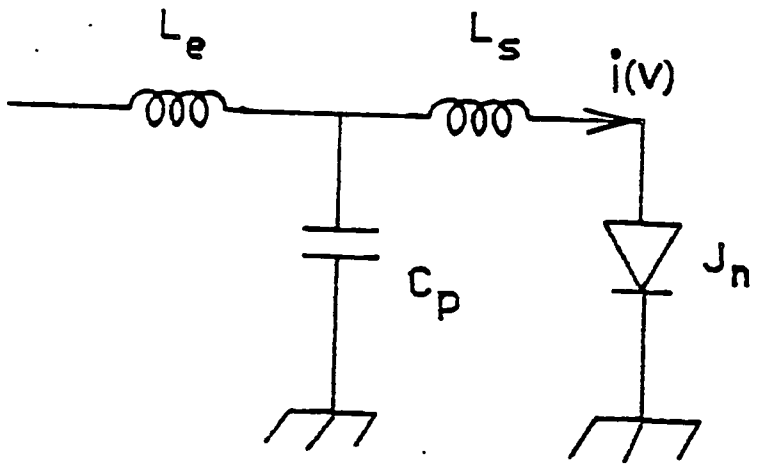

Figure 1.2: Nonlinear Model of a Varactor [3]

signal analysis method. Proper matching circuits are also required at the input and output of the varactor. The input matching circuit couples the fundamental power into the varactor. Similarily the output circuit couples the power at the divided down frequency to the output. The design procedure is discussed in a greater detail in the third chapter.

Of the two frequency divider methods mentioned above, the regenerative frequency division concept is the most popular one because of its simplicity in design and the quality of performance. The concept of regenerative frequency division was described in 1984 by Rauscher [4]. The regenerative frequency division is obtained by making use of a mixer with feedback from the output as shown in Figure 1.3. As seen in the figure, the input signal is mixed with a subharmonic feedback signal. For regeneration to occur, a finite signal at the output frequency f_o must be present in the loop initially due either to noise or input transients. The internally generated signal due either to noise or transients is mixed with an incident signal to produce a upper and lower sideband at the subharmonic (this is valid only in the case of division by two). The resulting upper sideband is

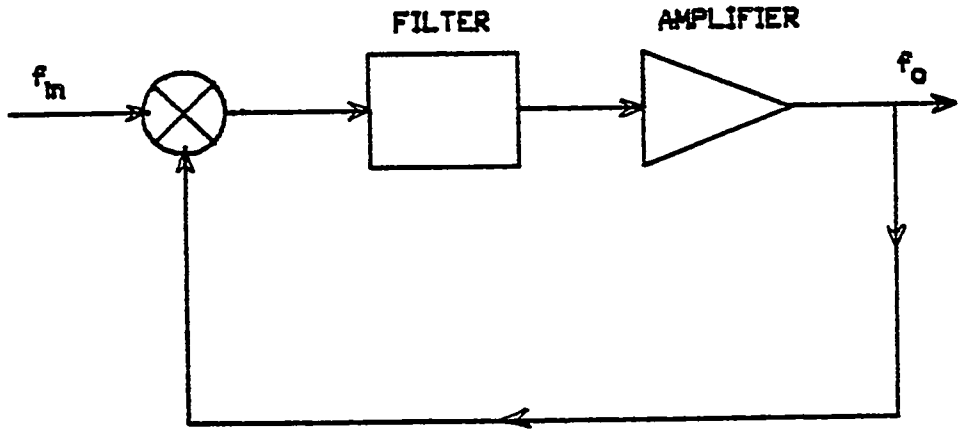

Figure 1.3: General Concept of Regenerative Frequency Divider [4]

filtered, leaving the lower sideband to be amplified and fed back to the mixer. However, to avoid any spurious oscillation in the absence of an input signal, the loop gain must be initially set below unity. As the input drive level increases, the mixer contribution to the loop gain increases and when the loop gain reaches unity, oscillation takes place at the subharmonic frequency. Although the regenerative circuit of Figure 1.2 consists of four circuit blocks, a regenerative divider may be realized by using a single GaAs FET [4]. A detail discussion on the GaAs FET operation is given in Chapter 3. In this realisation, the transconductance nonlinearity of the GaAs FET is used for the mixing action. Also the gain of the GaAs FET is used to obtain the desired gain for the regenerative process. Thus an inexpensive frequency divider with the required gain may be realized using a single active device.

1.2. Thesis Objectives

The primary and the secondary objective of this thesis are as follows:

1. The primary objective is to study theoretically the nonlinear behaviour of a GaAs FET device and investigate the possibility of computer-aided-design for a C band (6-8 GHz) regenerative divider using a single GaAs FET device. The divider should have an operating bandwidth higher than 500 MHz as this bandwidth is required for a typical 'C' band satellite transmitter. Good insertion loss performance and output return loss is also desirable.

2. The secondary objective is to study the application of harmonic balance methods to the divider and implement CAD optimization for the divider using this method. CAD software packages are available for microwave circuit analysis and optimization [LIBRA [1], SPICE [2] and TOUCHSTONE [2]]. These packages are used in designing GaAs FET regenerative divider.

1.3. Thesis Outline

1. In Chapter 2, the concept of frequency division is discussed in detail and the results of a literature search of existing dividers are presented.

2. In Chapter 3, the general theory behind the small and large signal models of a GaAs FET is studied. Also, the application of harmonic balance analysis in the design of a divider incorporating a varactor is introduced.

3. In Chapter 4, the design procedure of the divider is discussed in detail. The design incorporates harmonic balance analysis.

4. In Chapter 5, the simulated and measured results for a "C" band microstrip divider are presented.

5. In the final Chapter conclusions and the direction for further research are briefly presented.

2. LITERATURE REVIEW

2.1. Introduction

A number of different methods of realizing a microstrip frequency divider have been reported in the literature [3], [4], and [5]. Dividers making use of parametric subharmonic generation in varactors and regenerative frequency division are most common and these are described in detail in this chapter.

2.2. Parametric Frequency Dividers using Varactors

Parametric frequency division using a varactor is used in a number of practical applications because of its broad bandwidth and simple circuit configuration. Recently a simple varactor divider making use of a modified version of the harmonic balance technique was implemented by Lipparni and Rizzoli [3]. The harmonic balance technique is a method of analyzing and optimizing nonlinear circuits. This method is discussed in detail in chapter 3. The schematic of such a type of divider is shown in Figure 2.1. The divider basically consists of three blocks, namely an input network, an output network and a varactor for subharmonic generation. The input network acts as a filter to isolate the divided frequency from the generator and the output network minimizes feedthrough of the input frequency to the load. The overall circuit is analyzed using a version of the harmonic balance technique that simultaneously optimizes the elements of the entire network. The method of designing a divider using the harmonic balance technique is given in more detail in the next chapter.

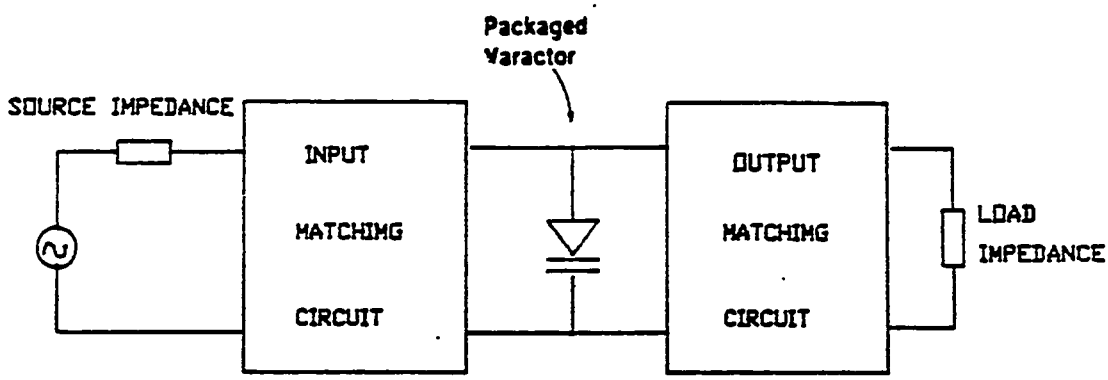

Figure 2.1: Schematic Topology of Parametric Frequency Divider [3]

To improve the transient response and eliminate the need for RF filtering, Harrison [5] made use of a balanced design, in which a pair of varactor diodes were used to provide subharmonic amplification and mixing simultaneously. The schematic of this divider is shown in Figure 2.2. It consists of a coupled pair of adjacent transmission lines of equal electrical length θ. Each line is reactively loaded with a varactor. The characteristics of these coupled lines can be specified in terms of Y_{oe} and Y_{oo}, their even and odd mode admittances, respectively. The even mode admittance, Y_{oe}, is defined as the characteristic admittance of one line to ground when equal currents are flowing in the two coupled lines. The odd mode admittance Y_{oo} is defined as the characteristic admittance of one line to ground when equal and opposite currents are flowing in the two lines. Figure 2.3 illustrates the electric field configuration over the cross section of the lines when they are excited in even and odd modes. In Figure 2.2 the common input point to

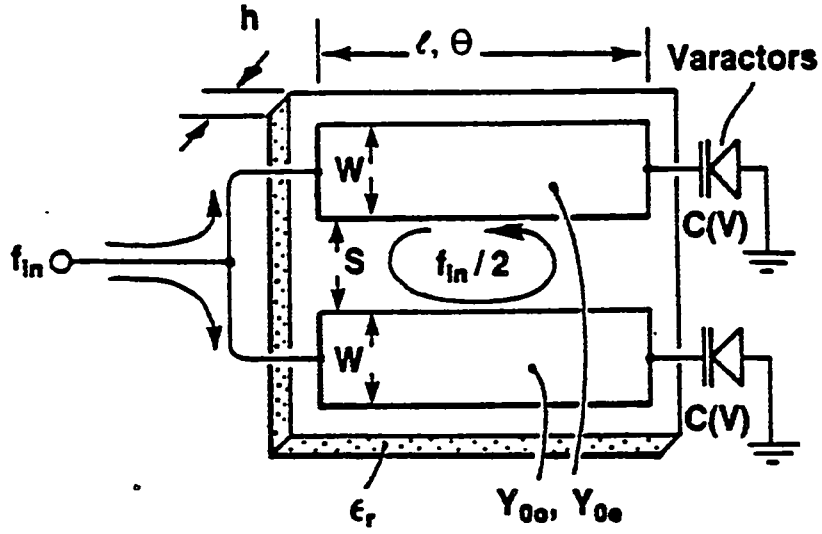

Figure 2.2: Basic Balanced Sub-Harmonic Resonator Circuit [5]

the coupled lines is a voltage null at half the input frequency. The graphical representation of Figure 2.2 leads to Figure 2.4 [6]. The admittances Y_1 and Y_2 in Figure 2.4 are equal to [6]

$$Y_1 = j\omega C_o - jY_{oe}\cot\theta, \tag{2.1}$$

$$Y_2 = -j\frac{1}{2}(Y_{oo} - Y_{oe})\cot\theta, \tag{2.2}$$

where θ is the electrical angle of the line and C_o is the capacitance at a given bias voltage. The condition for resonance at the output frequency f_o is given by:

$$Y_1 + 2Y_2 = 0. \tag{2.3}$$

Substitution for Y_1 and Y_2 in the above Equation, gives

$$\omega_o C_o = Y_{oo}\cot\theta, \tag{2.4}$$

as the odd-mode resonance condition. The resonator is designed to support oscillation at the half of the input frequency. The energy is transferred from input frequency f_{in} to $f_{in}/2$ via nonlinear reactance of the varactors. The odd admittance of the line pair determines the resonant behaviour at this frequency $f_{in}/2$. A balance to unbalance transformer is

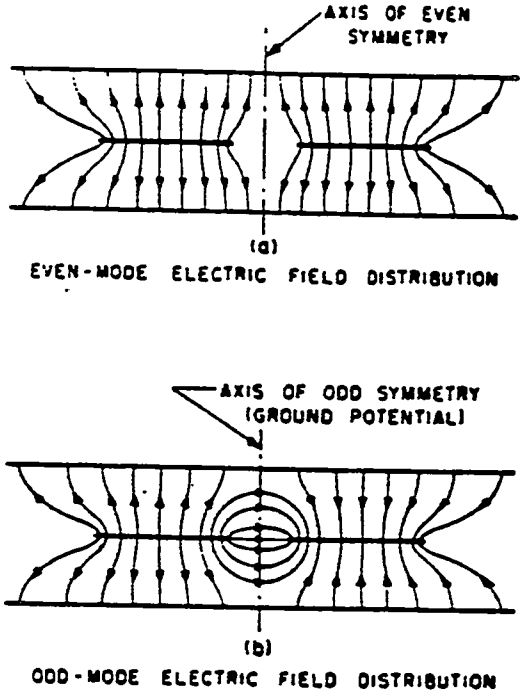

Figure 2.3: Cross Section view of the line when excited in Even and Odd mode

coupled to the microstrip resonator and converts the balanced $f_{in}/2$ signal to an unbalanced output. Figure 2.5 shows the performance of this design for an input frequency of 4-8 GHz. As seen from Figure 2.5 a minimum input power is required to achieve an output at the divided frequency. When the input power is increased from zero, frequency division commences abruptly at point "a". If the input power is reduced, the output at the divided frequency persists down to point "b", where it suddenly drops to zero. The frequency response of the divider for fixed input power is shown in Figure 2.6.

Though the 3-dB bandwidth of a varactor divider is found to be in the range of approximately 600 MHz relative to the input frequency, the main disadvantage of the varactor divider is that it requires a preamplifier and a postamplifier to minimize the insertion loss.

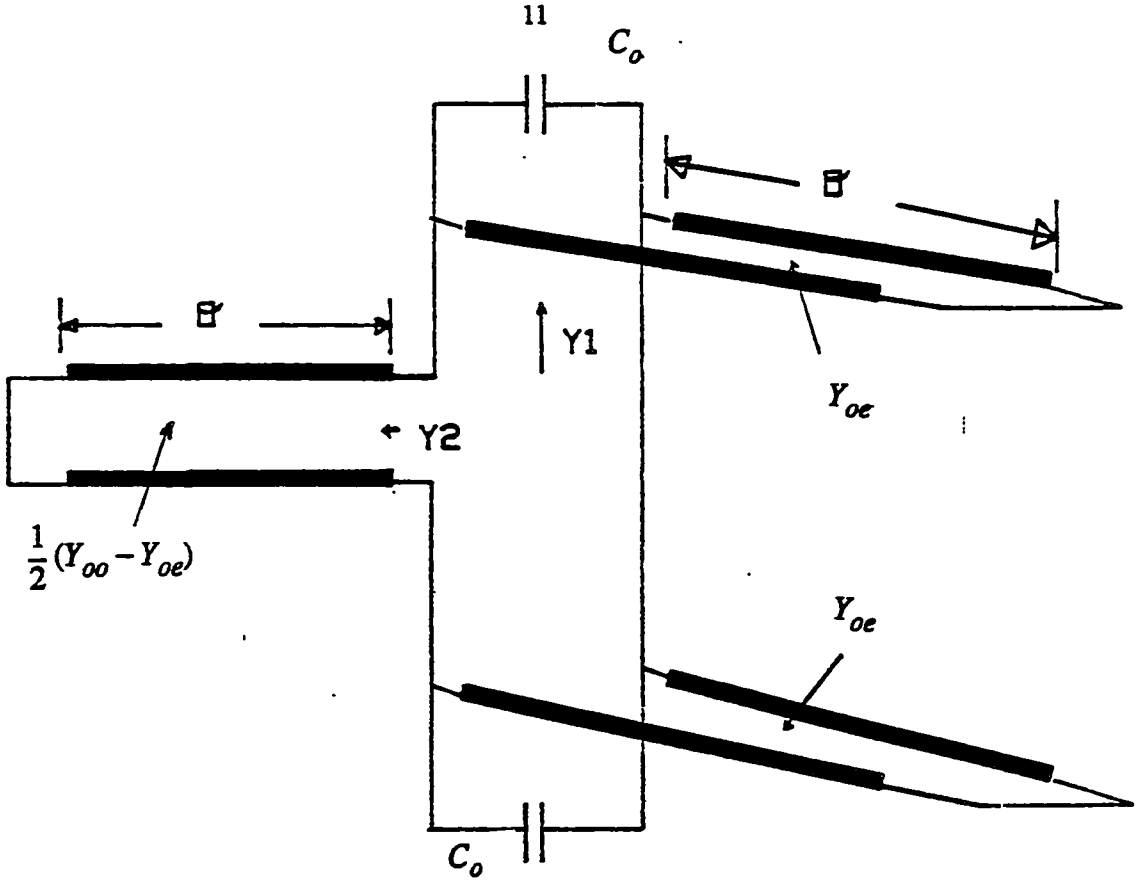

Figure 2.4: Open-Wire Equivalent Circuit at 1/2 f_{in} [5]

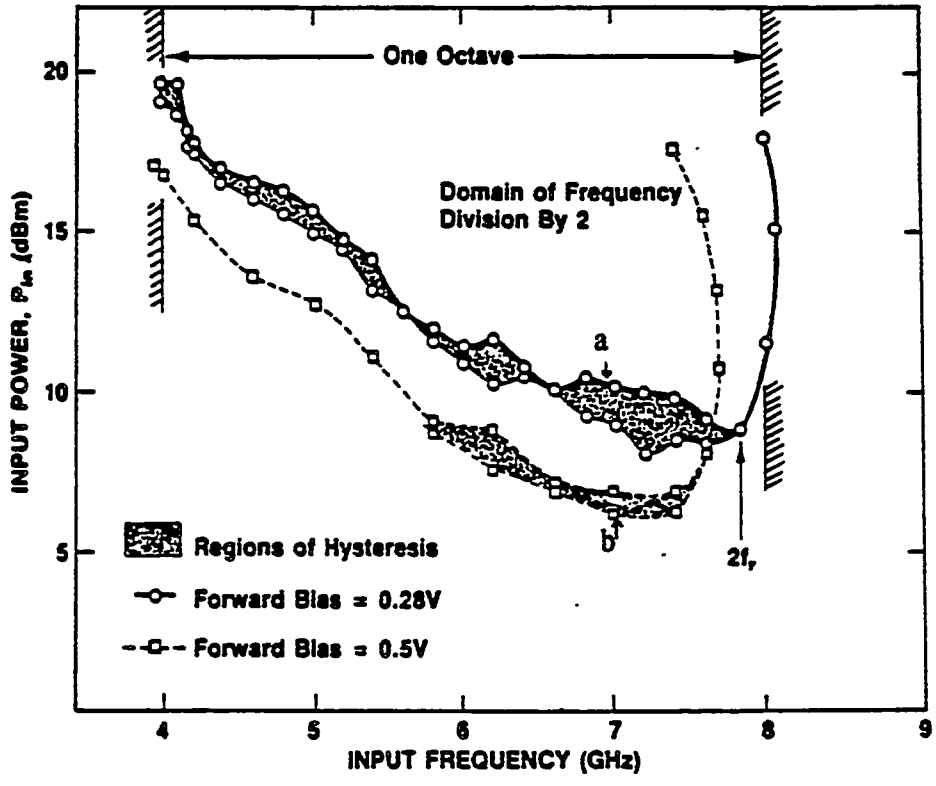

Figure 2.5: Domain of Frequency Division

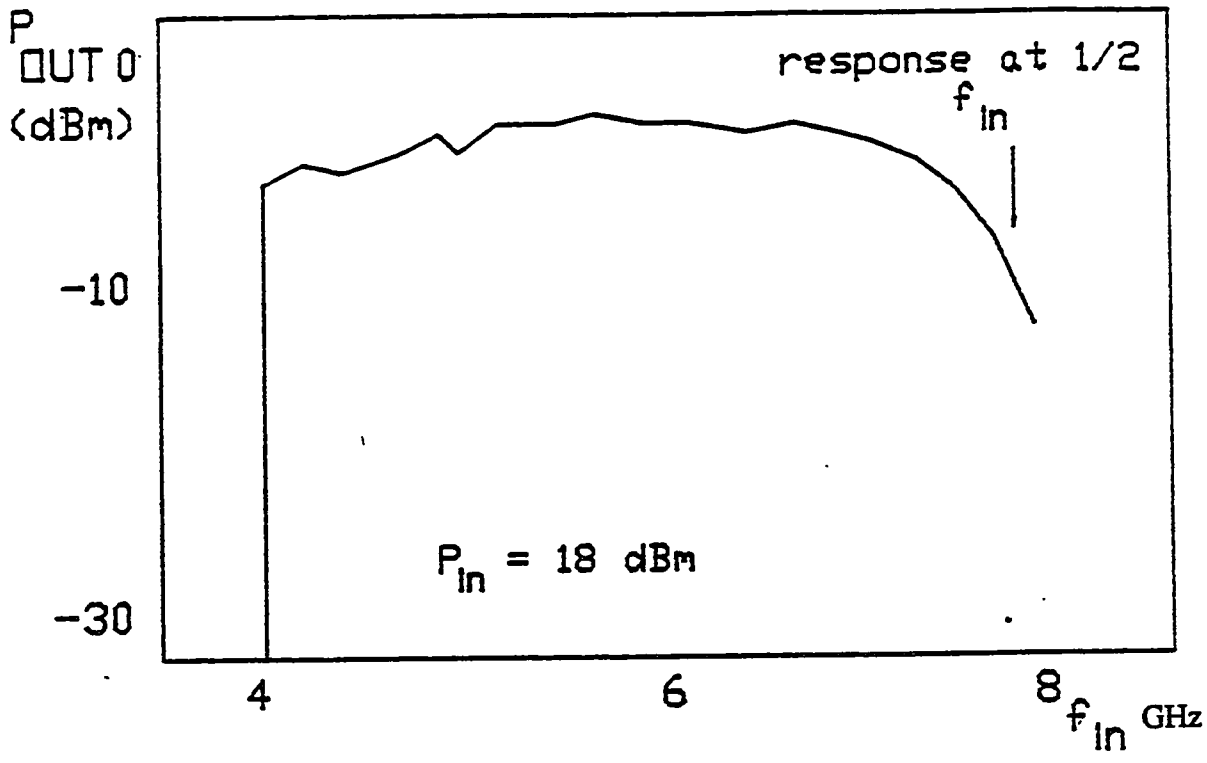

Figure 2.6: Frequency Response of the Divider [5]

2.3. Regenerative Frequency Divider

As mentioned in chapter one the regeneration can be achieved by a single active device with an appropriate feedback. Rauscher [4] has designed a frequency divider making use of a GaAs FET in the common source configuration with parallel feedback for regeneration. The block diagram of this type of divider is shown in Figure 2.7. As seen from the figure, the divider consists of three blocks, namely an input matching network, a GaAs FET with a parallel feedback and an output matching network. The GaAs FET is biased near the pinch-off voltage so as to offer a pronounced quadratic-type transconductance nonlinearity for efficient amplification and mixing. An input network at the front end of the GaAs FET matches the gate-source port of the transistor with the generator, and prevents the internally generated signal from reaching the generator. An output network matches the drain-source port of the transistor with the load at the divided

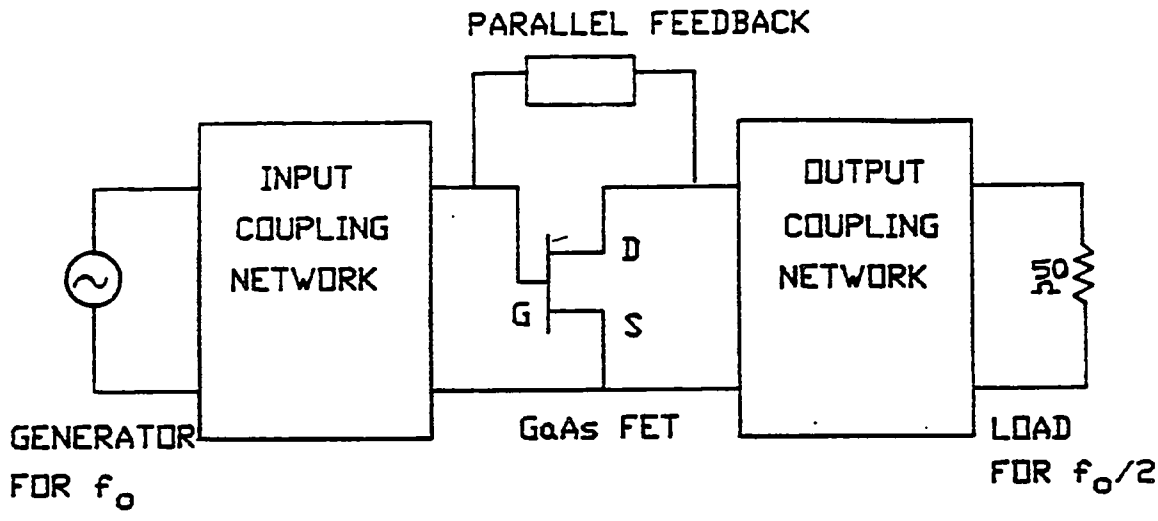

Figure 2.7: Frequency Divider incorporating GaAs FET in Common-Source Configuration [3]

frequency. In Rauscher's design an oscillator making use of a GaAs FET in common-source configuration is designed at the subharmonic frequency. The gain of the external feedback loop is then reduced by 3db in order to prevent any unwanted oscillation taking place in the absence of an input signal.

The 16 GHz divide by 2 circuit was implemented by Rauscher using a microstrip structure on a 0.25 mm thick fibre glass-reinforced teflon substrate as shown in Figure 2.8. Subharmonic feedback was implemented by a feedback circuit consisting of a 300 micrometer diameter coil inductor L_1 and a 5pf Silicon nitride capacitor C_3.

The performance results of the above divider are shown in Figures 2.9 and 2.10. In Figure 2.9, the output power vs input power is plotted for a fixed input frequency. It can be seen from Figure 2.9 that, initially as the input power is increased, output power in-

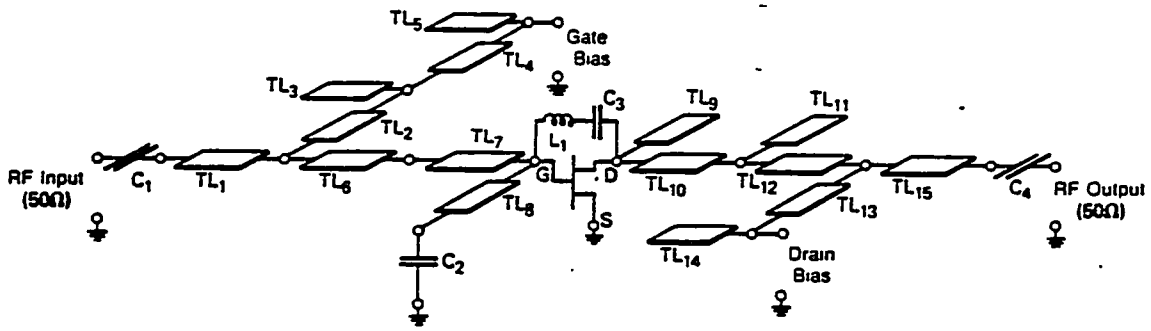

Figure 2.8: Physical Layout of a Practical 16/2 Divider [4]

creases in a linear fashion. Towards the upper end of the input power scale, the output response levels off as the subharmonic oscillation approaches saturation. In between these two extremes, there is a rather limited range where the divider response can be considered reasonably linear. In Figure 2.10 the conversion gain is plotted as a function of the input drive level. Also shown in the same figure is the dc drain-source current of the transistor. This current increases with the drive level due to the rectifying action associated with operation in the vicinity of pinch off.

Though the regenerative frequency divider works well over a moderate bandwidth, it has some disadvantages too. Some of the main disadvantages are:

1. For a pulsed signal, the leading-edge delays can be too long [4]. The delay in the leading edge corresponds to the time taken by the subharmonic signal to build up from noise. The response of the divider to the RF signal for various input powers is shown in Figure 2.11. Figure 2.11 depecits the 8.0 GHz frequency divided response for a range of pulse amplitudes. One can

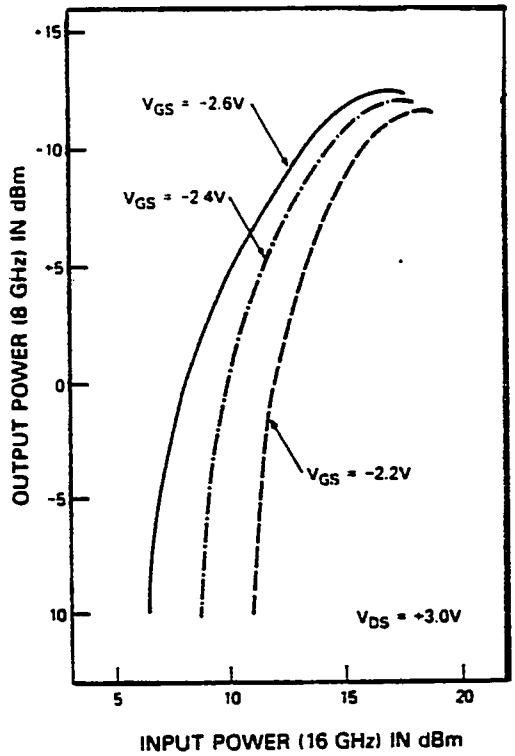

Figure 2.9: Output Sub-Harmonic Power as a Function Input Drive Level

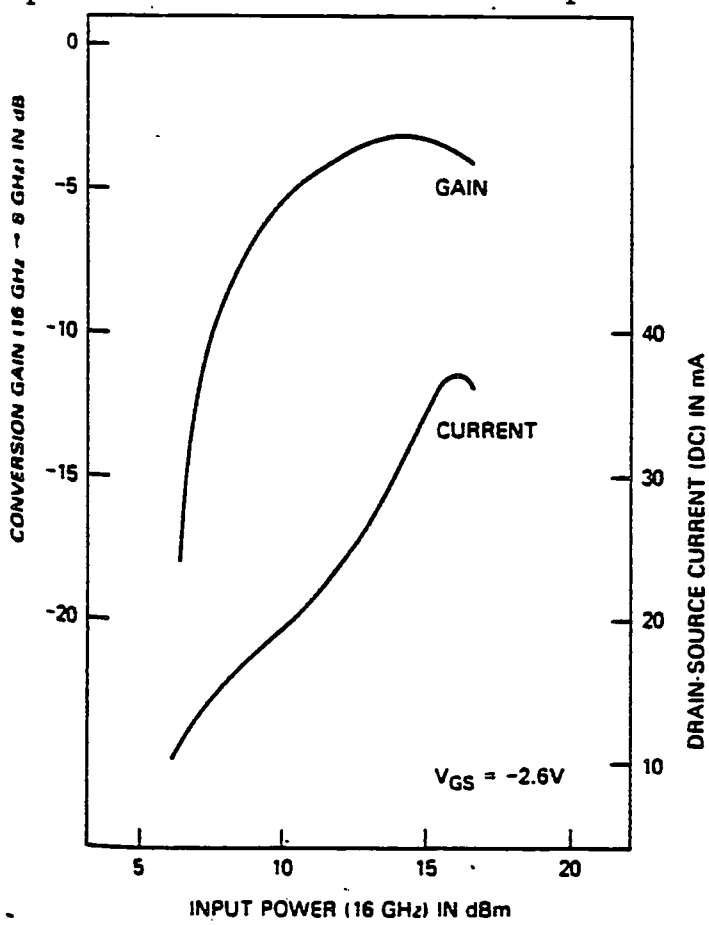

Figure 2.10: Conversion Gain as a Function of Input Drive Level [4]

see from the figure that the leading edge delay decreases as the input power

increases. This is because the loop gain increases with the increase in the input drive level.

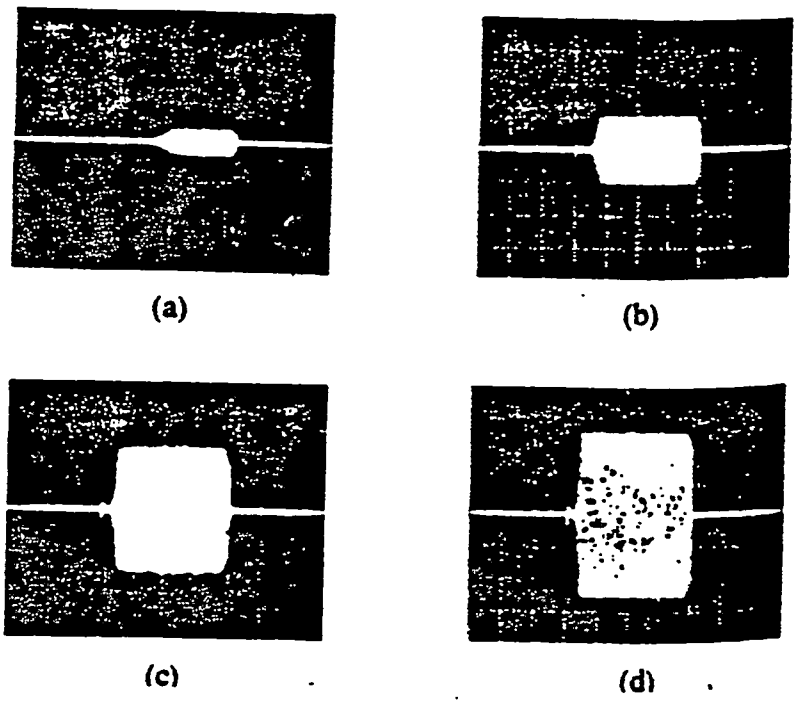

Figure 2.11: Response of a Divider to RF signal [8GHz pulsed output response for 16GHz incident power levels of:{a}7dbm {b}10dbm {c}13dbm {d}16dbm][4]

2. Regenerative dividers can exhibit noisy behaviour for multiple input signals which are close to each other in frequency [4].

3. Regenerative dividers have a tendency to enter into a spurious oscillation mode.

The main advantage of the regenerative divider incorporating a GaAs FET is that it makes use of the gain in a GaAs FET to minimize the insertion loss, thereby eliminating the need for a pre and post amplifier as in a parametric divider. This thesis is mainly concerned with the application of the harmonic balance technique for the analysis and optimization of a regenerative frequency divider. The design procedure developed in this

thesis leads to a cost effective, compact high performance frequency divider using a single active device.

3. GENERAL THEORY AND ANALYSIS

3.1. Introduction

This chapter contains three sections. In the first section the operation of a GaAs FET is studied . In the second section a nonlinear model of a GaAs FET is analyzed and in the last section the application of the harmonic balance technique in designing a non-linear circuit is briefly explained.

3.2. Operation of a GaAs FET

The cross sectional view of a GaAs FET is shown in Figure 3.1.

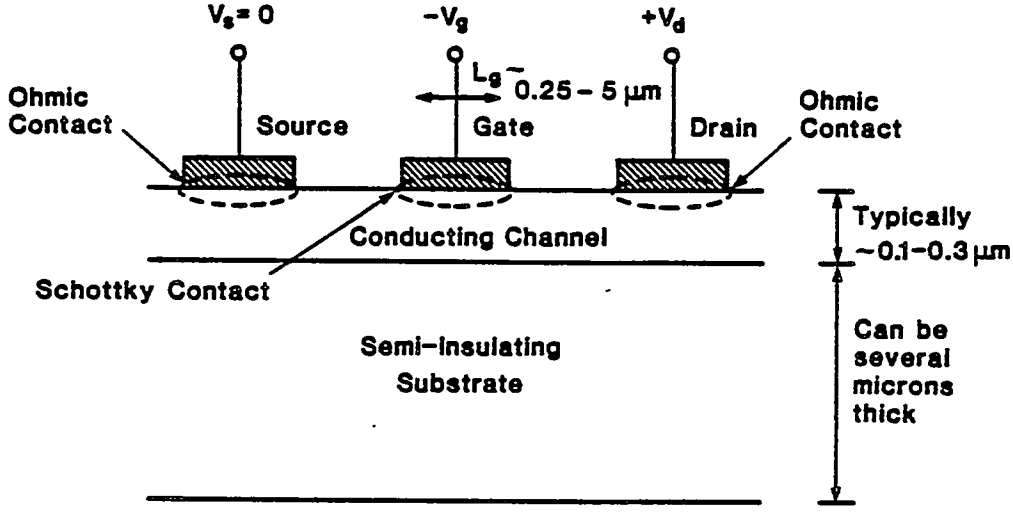

Figure 3.1: Cross Sectional View of GaAs FET [7]

It has a semi-insulating GaAs substrate at the bottom. Its main purpose is to act as a mechanical support for the rest of the device. In addition, it enables a thin epitaxial layer to be deposited on its upper face. This epitaxial layer which is deposited on the semi-insulating substrate is conductive. This layer is very thin, typically in the order of 0.1-0.3 micrometer. On top of this layer there are three metallic contacts produced by vacuum deposition. The source and drain contacts are formed from a gold-germanium alloy enabling an ohmic contact to be made. The gate is made of aluminium so as to form a Schottky rectifying junction.

The GaAs FET is biased by two sources, namely V_{gs}, gate-source voltage and V_{ds}, drain-source voltage. When both the voltages are applied a depletion layer below the gate metal is formed. The bias voltage controls the width of the depletion region and thereby influences the flow of current through the channel. The bias voltage controls the channel current not only by varying the width of the depletion region formed below the gate metal, but also by varying the longitudinal electric field. When V_{gs}=0, the width of the depletion region is small and as V_{ds} is increased, the voltage across the depletion region in the drain end is greater than that in the source end, resulting in a larger depletion width below the drain end than in the source end. When the gate reverse bias is increased keeping V_{ds} constant, the depletion region widens and the conductive channel becomes narrower thereby reducing the current. Regardless of the value of V_{ds}, the drain current becomes zero when V_{gs} equals the pinch-off voltage, as the channel is fully depleted. In this region the GaAs FET is said to be in its linear or voltage controlled region. If V_{ds} is increased keeping V_{gs} constant, the depletion region widens and the conductive channel becomes narrower near the drain end. Since the current clearly must be constant throughout the channel, the electrons move faster. After some point, increasing V_{ds} causes the velocity of electrons to saturate as the velocity of electrons can not exceed the saturated drift velocity. If V_{ds} is increased beyond the value that causes

velocity saturation [V_{ds}(sat)], the electron concentration must increase rather than velocity in order to maintain current continuity. This causes accumulation of electrons near the drain end. Because the channel becomes progressively narrower near the drain, the negative charge density increases towards the drain. Between the edge of the depletion region and the drain contact, the electrons remain at saturated velocity. But the channel after a point opens abruptly, resulting in a net electron depletion and a net positive channel charge (from the ionized donor atoms) as shown in Figure 3.2.

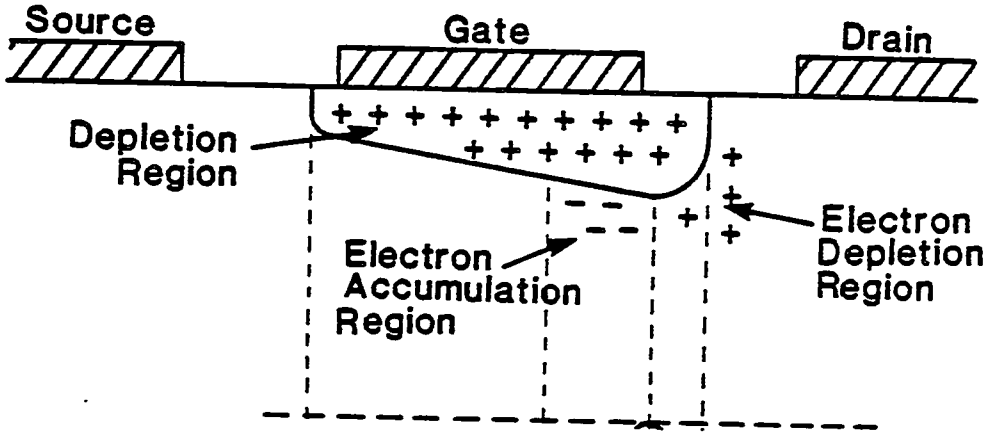

Figure 3.2: Gate Depletion Region for $V_{ds}=V_{ds}$[sat] [7]

If V_{ds} is increased further, virtually all of the voltage increase is dropped across this dipole layer, increasing the stored charge, but causing very little increase in current. At this point the GaAs FET is said to be in the saturated region.

3.3. GaAs FET Modelling

The model for a GaAs FET that can be used in small signal or large signal analysis is shown in Figure 3.3.

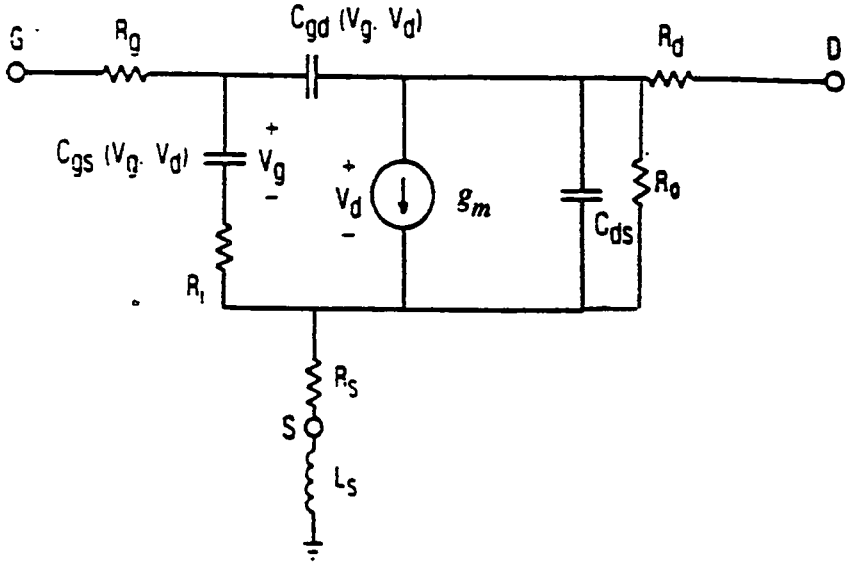

Figure 3.3: Model for GaAs FET Suitable for both Small and Large Signal Analysis

The equivalent circuit consist of both passive parasitic elements and the elements responsible for the active characteristic of the device. R_g is the ohmic resistance of the gate, R_s and R_d are the source and drain ohmic contact resistances respectively. C_{gs} and C_{gd} are the gate to source capacitance and gate to drain capacitance and are functions of both V_{gs} and V_{ds}. Both these capacitances account for the displacement current through the gate depletion region and are mathematically defined as

$$C_{gs} = \left.\frac{\delta Q_d}{\delta V_g}\right|_{V_d - V_g = const,} \tag{3.1}$$

$$C_{gd} = \left.\frac{\delta Q_d}{\delta V_d}\right|_{V_g = const,} \tag{3.2}$$

where Q_d is the the charge in the gate depletion region, V_g the voltage across C_{gs} and V_d the voltage across the voltage controlled current source. These voltages V_g and V_d are sometime referred to as internal gate and drain voltages. R_o and g_m are the channel resistance and transconductance respectively and are mathematically defined as

$$R_o \approx \left.\frac{-\delta V_{ds}}{\delta I_d}\right|_{V_g,} \tag{3.3}$$

$$g_m \approx \left.\frac{-\delta I_d}{\delta V_{gs}}\right|_{V_d.} \tag{3.4}$$

The elements C_{gs}, C_{gd} and g_m exhibit strong dependence to bias condition and are the main nonlinear elements of GaAs FET. The bias dependence of these elements is dealt with in more detail in chapter 5. Over the past years GaAs FET's have become commonly used for a wide variety of microwave applications. To study the large signal performance of a GaAs FET device an accurate nonlinear device model is needed. A number of large signal models for GaAs FET's have been reported in literature [8], [2]. Most of these models are based on some form of nonlinear circuit, with parameters often determined by large-signal measurements on the active device or by determining the small-signal element values from the device parameters such as gate width, gate length and epitaxial thickness [7] and then relating these small-signal element values to the large-signal element values [9].

3.4. Harmonic Balance

3.4.1. General Theory

The harmonic balance (H.B.) technique is quite useful for analyzing nonlinear circuits. To describe this method, let us consider a general equivalent circuit shown in Figure 3.4 that describes many types of nonlinear microwave circuits. The circuit consists of an input matching, an output matching and a nonlinear solid state device. Some of the elements in this solid state device may be linear and some nonlinear.