PROTECTIVE RELAYING FOR PARALLEL-TEED TRANSMISSION LINES

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XIANPING LIU

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PROTECTIVE RELAYING FOR PARALLEL-TEED TRANSMISSION LINES

Student: Xianping Liu Supervisor: Dr. M.S. Sachdev

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ABSTRACT

Parallel-teed transmission lines (PTTLs) have economic and environmental advantages and have, therefore, been widely used in power systems all over the world. However, protection of PTTLs has remained a difficult task. Conventional protection method for transmission lines do not provide satisfactory solution in most cases. The situation becomes even severe if the PTTL has unequal branch lengths and system operating states vary widely.

Recent advance in communication technology and development of microprocessor-based relays has encouraged researchers to apply differential principle for protecting transmission lines. A differential algorithm is developed in this thesis. This development uses distributed parameter model of the transmission line. The algorithm, therefore, provides better relay performance in terms of sensitivity and security, speed and faulted phase selectivity.

To facilitate the use of this algorithm, a technique for synchronizing the data sampled at the line terminals and a criterion for detecting fault are also developed. The synchronization method needs minimum use of the communication media and can, therefore, be used on communication carrier facilities usually available in transmission lines. Problems in implementing PTTL relays based on the developed algorithm are also discussed.

Intensive simulation tests were conducted to examine the relay performance. The results show that the algorithm has stable output during normal or external fault conditions. Also the level of spurious output is low and, therefore, low level of restraining signals can be selected. The algorithm has high sensitivity and fast operating speed without jeopardizing security. Results obtained from simulations are included in this thesis.

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LIST OF SYMBOLS

I, i	current
V, v,	voltages
HV	high voltage
EHV	extra high voltage
UHV	untra high voltage
A, kA	current unit: ampare, kiloampare
kV	voltage unit: kilovoltage
f	frequency
Hz	frequency unit
a, b, c	phases in a three-phase system
MTMC	multi-terminal and multi-circuit (line)
PTTL	parallel-teed transmission line
S_x	source connected at x terminal
P, Q, R	terminals of a three terminal-line
Z, R, L	impedance, resistance and inductance
Ohm, Ω	resistance unit
r, g, l and c	unit length of line parameters
Z_0	characteristic inpedance
γ	propagation constant of tranvelling waves
A, B, C, D	line parameters defined by 2-port theory
K, M, T	thresholds of relay settings
Δ	delta (difference) of two quantities
$\angle$	angle of a phasor
T	time unit for relay
ms	time unit: millisecond
μs	time unit: microsecond
op	subscript for operational quantities of relay
res	subscript for restraining quantities of relay
l_{xy}	line length from x to y.
k	the ratio of lengths of the part from relay to the location of fault to the whole line

FD	Forward looking unit of directional relay
S	Backward looking unit of directional relay
CMD	trip command
R/T	Receiver/Transmitter of signals
θ, τ, φ	angles quantities used at equations
ccvt, vt	(capacitance coupling) voltage transducer
ct	current transducer
MUX	multiplexer device
S/H	sample/dolder device
LPF	low pass filter
A/D	analog to digital convertion
I/O	input/output unit
N	number of samples per nominal cycle
DFT	discrete Fourier transform
CCITT	International Telegragh and Telephone Consultive Committee
CRC	cyclic redundancy check
HDLC	communication protocal: high level data link control

1. INTRODUCTION

1.1. Power Transmission Systems

Power systems are composed of power generating plants, and transmission and distribution networks. Because natural resources that are needed to generate electrical energy are not usually located close to the load centers, large quantities of electrical energy are transported to users over transmission lines. For maintaining the continuity of supply to the customers, a transmission system should meet the bulk energy exchange requirements during normal operation and during transients caused by loss of generation, unbalanced loads and faults.

Power transfer limits of ac lines are proportional to the square of the operating voltage and inversely proportional to the inductive reactance from the source to load. High transmission voltages are, therefore, required to transport large amount of power. Transmission voltages presently used in power systems can be classified in the following three categories [3]:

1. High voltage (HV; 110 - 230 kV),
2. Extra high voltage (EHV; 330-800 kV) and
3. Ultra high voltage (UHV; over 1,000 kV).

High voltage overhead transmission lines, and more so the underground cables, have significant capacitance and, therefore, substantial charging currents are experienced.

Construction and operation of power systems need large capital investments. For better utilization of the investments, power systems are interconnected, which reduces the reserve capacity needed to maintain a desired degree of reliability. Using multi-terminal transmission lines is also one of the measures taken to reduce the capital investments in power systems.

Short circuits can cause extensive damage to the system if they are not promptly detected and taken care of. Relays are used to identify the onset of faults and their locations, and to take appropriate actions for isolating the faulted section.

1.2. Multi-Terminal and Multi-Circuit Transmission Lines

To increase power transfer limits and security of transmission, double-circuit lines are used in modern power systems. Multi-circuit lines on a single right-of-way can also reduce the cost substantially [9]. Further reduction in costs is achieved by using multi-terminal circuits. Their use also alleviates the problems associated with the availability of right-of-way and environmental concerns.

Most multi-terminal multi-circuit (MTMC) lines are in the form of parallel-teed transmission lines (PTTLs). A single line diagram of a PTTLs is shown in Figure 1.1. The lines interconnect three power systems P, Q and R. When one of the lines is disconnected, for maintenance or to isolate a fault, the arrangement reduces to a single three-terminal line. A three-terminal line could also be coupled partially with another circuit that would be physically on the same right-of-way for some of the distance between the terminal buses. Protection for a PTTL is the subject of this thesis.

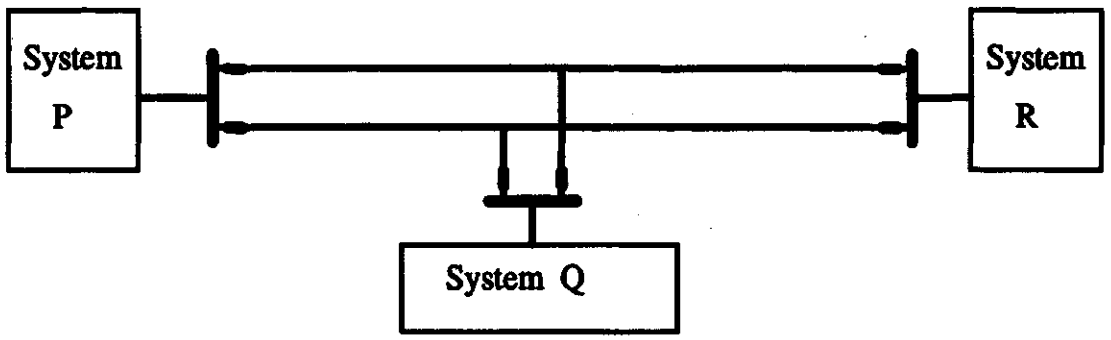


Figure 1.1. Single line diagram of a PTTL.

1.3. Power System Protection

Power system faults are caused by failure of insulation between phases and/or between a phase and the ground. Such failures are accompanied by substantial increase of currents, reduction of voltages and distortion of voltage and current waveforms. Protection systems are designed to detect these changes, determine the location of the

fault and isolate the faulted section by tripping corresponding circuit breakers to prevent further damage, and to keep the system in stable operation.

Power systems are physically divided into several sections by circuit breakers which can interrupt large amounts of currents. The circuit breakers are arranged in such a manner that they are able to isolate any section while maintaining the continuity of supply to as many load centers as possible.

A protection zone is physically associated with the equipment placed between circuit breakers. Each zone is equipped with a dedicated protection system which consists of one or several relays. Neighboring protection zones are overlapped to ensure that no part of the system remains unprotected. Figure 1.2 illustrates the basic principle of protection zones in power system. The zones are shown by encircling them with dotted lines. In the diagram, B_i and L_i (i=1,2,...) denote bus and line protection zones respectively.

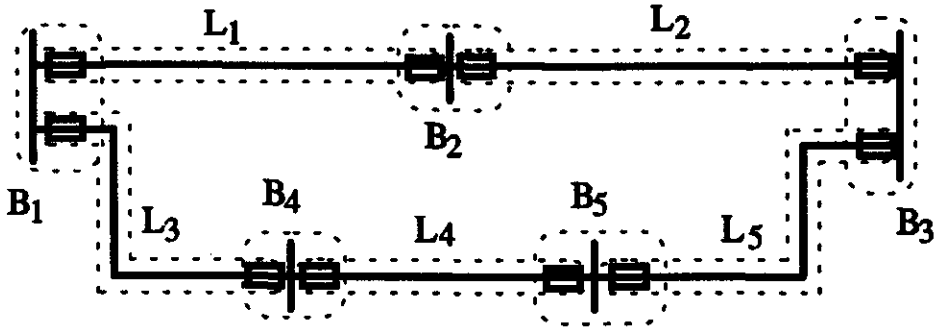


Figure 1.2. Protection zones of a transmission system.

A protection system should correctly identify faults in the protected zone as internal faults and those in the other zones as external faults. A relay monitors voltage and/or currents and compares them, and/or their combinations, with pre-defined settings. It issues a trip command if the threshold criteria are met.

The design of a protection system is influenced by many factors, such as measuring techniques, coordination and economics. Usually decisions are made after discussions between engineers in system planning, protection and control departments of the utility, and relay manufacturers.

1.3.1. Transmission Line Protection

Overcurrent relays were the earliest devices used for protecting lines and other equipments. The operation of these relays depends on the magnitude of current in the protected circuits. They issue trip commands if the currents in the relays exceed specified values.

Directional overcurrent relays were then introduced. They monitor the phasors representing terminal voltages and line currents. From observing the differences between the voltage and current phasors, they are able to discriminate faults on the line side of the relay from those on the bus side. This feature is useful when a protected line is a part of an interconnected network.

Overcurrent and directional overcurrent relays were superseded by impedance relays. They monitor the voltages and currents at the relay location and operate if the ratio of the voltage phasor to the current phasor reduces to values less than specified thresholds. During a fault, this ratio reflects the distance from the relay to the fault. For this reason, impedance relays are sometimes called distance relays.

The overcurrent, directional overcurrent and distance relays use voltages and currents observed at the local terminal of the line. These arrangements, which are classified as non-unit protections, save the expenses for the relays to communicate with the devices at the remote terminals of the lines. Unfortunately, these relays can not determine the location of a fault accurately. Each line is, therefore, protected by relays set for two to four protection zones. The first zone can cover 70-80% of the total line. For faults in this zone, the relays issue trip commands without any intentional time delays. The second zone covers the whole line and part of the line (or lines) beyond the remote terminal. In case of faults in the second zone, the relays issue trip commands after time delays that are typically 0.3 - 0.5 seconds. Coordination with the relays protecting other lines emanating from the same substation and those emanating from the substation at the remote terminal of the line is necessary but, in some situations, it is difficult to achieve. To overcome the problems of coordination and to reduce the time to trip for faults at the far end of the line, unit protection schemes were developed.

A unit protection scheme identifies a fault by using information from both terminals of the line. Relays located at different terminals of the line observe local currents and/or voltages, process them and send their parameters to the other terminal. Trip commands are issued after comparing information from both terminals of the line. Directional comparison, phase comparison and differential protection are the three techniques used in unit protection schemes.

A directional comparison system consists of directional relays at each terminal of a line. The relays monitor the direction of the fault by examining the angle between the phasors of local terminal voltages and line currents. For an internal fault, all units sense the fault to be in the forward direction but for an external fault, at least one of the directional relays will sense the fault to be on the bus side of the relay. Trip commands are disabled if any relay does not sense the fault to be on the line side. Since the information to be exchanged between relays is the direction of fault only, the communication requirements are minimal.

Phase comparison protection compares the flow of current at the two terminals of the protected line. During normal and external fault conditions, current flows into the line at one terminal and flows out of the other terminal. Flow of currents into both terminals of the line, or out of both terminals of the line, indicates a fault on the protected line. The advantage of the technique over directional comparison is that it does not use voltages and, therefore, voltage transformers are not needed at the line terminals.

Differential protection is based on Kirchhoff's current law which monitors the net input current (or differential current) flowing into the protected line from all terminals. During normal conditions, and external faults, this current is equal to the line charging current. During internal faults, however, this current becomes large. The differential schemes compare the differential current of the line with the through current. Trip commands are issued to circuit breakers of the faulted phases when a specified condition is met. To build valid operating and restraining currents, synchronized current signals are required to be sent over wideband communication channels.

Most faults are of a temporary nature and can be removed by de-energizing the line for a short period of time. Automatic reclosing has, therefore, been a practice to restore lines to service after transient faults, such as faults caused by lightning. Further

discussion of auto-reclosing practices in HV and EHV transmission systems is included in the next chapter.

1.3.2. Protection of MTMC Lines

Many MTMC lines are developed from two terminal lines by building tapped branches. These additional network connections introduce several phenomena, such as infeed effects, flow-out of fault current and simultaneous loss of double circuits. To protect a tapped line, distance and directional protections, originally used on these lines, were usually retained [11,12,13]. To achieve reliability and security of the protection system, many restrictions were usually included which increased the fault clearing times considerably. This was especially true when the faults were close to the boundaries of the relay characteristics. These aspects are further discussed in chapter three.

Application of traveling wave phenomena, to identify internal faults on MTMC lines, was also attempted [16]. The sign of the voltage wave with respect to the current wave is observed immediately after the inception of a fault. For internal faults, the waves of a current and voltage of a phase are of opposite polarities at all terminals of the line. On the other hand, the waves are of similar polarities at the terminal closest to the external fault. To avoid confusion by multiple reflections of the waves, relays only used the first wave after the inception of a fault.

Because of the unsatisfactory performance of the systems used to protect MTMC lines, recent developments have focused on using the differential principle [17, 18, 21, 13, 14]. Algorithms have been proposed which deal with the problems such as mutual couplings and data synchronization. Their development will be further discussed in later chapters.

1.4. Research Objectives

Most multiterminal lines are parallel-teed transmission lines (PTTLs). Many investigations have dealt with the protection of teed-transmission lines; these investigations formed the basis of relaying PTTLs. Unfortunately, the performance of most relaying systems for protecting PTTL's is either restricted or unsatisfactory [13].

The objective of this project is to investigate the techniques for protecting PTTLs and to develop a new algorithm which could form the basis for a new approach.

1.5. The Outline of This Thesis

The thesis is divided into eight chapters and six appendices. The first chapter presents the background information on transmission line protection. The concept of MTMC lines and problems experienced in protecting these lines are briefly introduced.

Chapter 2 provides an overview of the techniques conventionally used for transmission line protection. The underlying principle of these techniques are briefly presented. The next chapter reviews the recent developments in computer relaying. The advantages of using microprocessor-based relays are outlined. Typical hardware and relaying algorithms used in these relays are briefly discussed.

Application of the conventional techniques to protect parallel teed transmission lines (PTTLs) is discussed in Chapter 4. The advantages and shortcomings of these techniques are summarized. These techniques are compared qualitatively with respect to their performance in terms of selectivity, speed, reliability and adaptivity to operating conditions.

Chapter 5 outlines the theory which can assist in developing a new differential algorithm for PTTLs. A new algorithm is also presented. The suitability of the proposed algorithm is examined. A protection system which uses the proposed algorithm is described in Chapter 6. The techniques used for implementing the proposed differential algorithm are developed.

Chapter 7 describes the simulation of the relay and its use for protecting PTTLs. The results obtained from the simulation are discussed and the performance of the proposed algorithm is evaluated. Chapter 8 provides a summary of the research and draws conclusions from the discussion in the thesis. A list of references follows this chapter.

Six appendices are included in this thesis. Appendix A encloses the basis of calculating the distribution of zero sequence currents in a PTTL. Appendix B describes the modal transformation for use in multi-phase electrical systems. An approach for

modeling mutually coupled parallel three-phase lines is presented in Appendix C. In Appendix D, the parameters of a power system with parallel-teed transmission lines, which is used for testing the designed protection system, are presented. Appedix E presents examples of fault case studies for a 500 kV PTTL and Appendix F includes additional results of the case studies conducted on 345 kV PTTLs.

2. METHODS FOR PROTECTING TRANSMISSION LINES

2.1. Faults on Transmission Lines

Faults are experienced on transmission lines because they are continuously exposed to atmospheric disturbances. Short circuits occur due to high winds, insulation failure, flying objects and natural disasters. The largest number of faults are caused by lightning strikes on or close to the lines.

A short circuit between two phase conductors is called a phase-to-phase fault whereas a short circuit between a phase conductor to ground is called a phase-to-ground fault. Similarly, a short circuit between two phases to ground is classified as a phase-to-phase-to-ground fault. On high voltage transmission lines, which have phase conductors spaced wide apart, a majority of faults are from a phase to ground. Table 2.1 lists the distribution of faults on HV and EHV transmission systems [8].

Table 2.1. Incidence of faults on HV and EHV transmission lines

Voltage	phase-to-ground faults	phase-to-phase faults	phase-to-phase-to-ground faults	3-phase faults
HV	70%	15%	10%	5%
EHV	93%	4%	2%	1%

In modern power systems, two or more transmission lines are often placed on common structures. In such cases, short circuits can involve phases of different circuits. These faults are called inter-circuit, or cross-country faults. Faults can also occur simultaneously at different locations of a circuit or on different circuits. These faults are called simultaneous faults.

2.2. Transmission Line Models

Relay principles must be based on reasonably accurate models of power systems, including the transmission lines. The lines of a single-phase transmission system, shown in Figure 2.1.(a), can be represented by their series impedances if the lengths of the lines are less than 30 km. This is shown in Figure 2.1.(b). The voltages at buses Q and R can be expressed in terms of the voltages at buses P and Q and the line currents as

$$\begin{aligned} V_q &= V_p - I_{pq}Z_{pq}, \\ V_r &= V_p - I_{pr}Z_{qr}, \\ V_r &= V_q - I_{qr}Z_{qr}, \\ Z_{pq} &= Z_{pr} + Z_{rq}, \end{aligned} \qquad (2.1)$$

where:

I_{pq}, I_{pr} and I_{qr}	are the currents in lines PQ, PR and QR respectively,
V_p, V_q and V_r	are the voltages at buses P, Q and R respectively, and
Z_{pr}, Z_{qr}, and Z_{pq}	are the series impedances of the transmission lines.

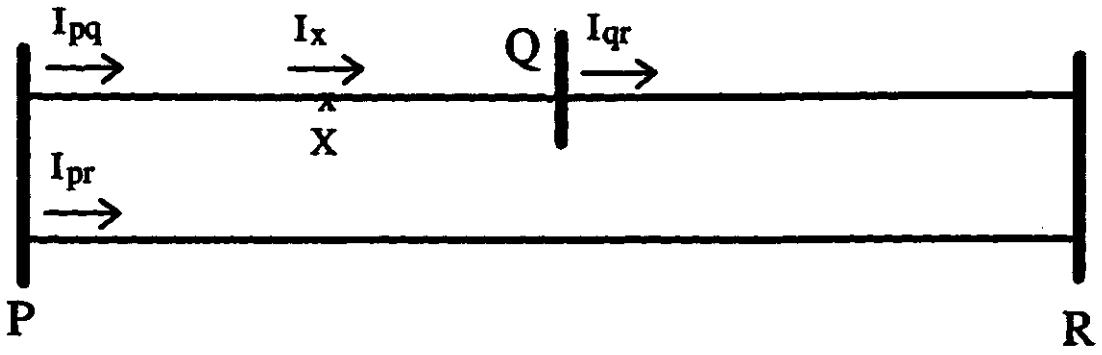
If the lines are of medium length, they can be represented by nominal π models as shown in Figure 2.1 (c) where the shunt branches represent the line charging phenomena. Quite often the transmission lines are long; these lines must be represented by distributed parameter models. If the line from bus P to bus Q, shown in Figure 2.1.(a), is long, the relationships between the voltages and currents at x are

$$\begin{aligned} \frac{dv_x}{dx} &= ri_x + l\frac{di_x}{dt}, \\ \frac{di_x}{dx} &= gv_x + c\frac{dv_x}{dt}, \end{aligned} \qquad (2.2)$$

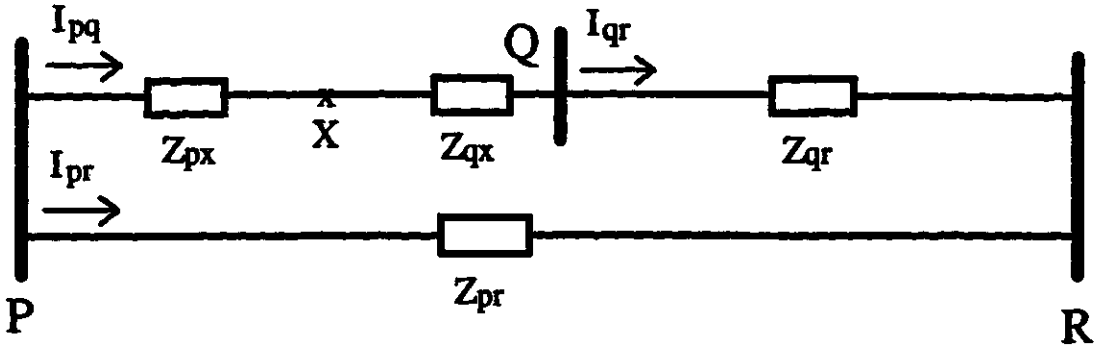
where:

v_x and i_x	are the instantaneous voltage and current at x and
r, g, l and c	are the resistance, conductance, inductance and capacitance per meter of the line respectively.

The solution of these differential equations provides the following voltage and current phasor equations.



(a)



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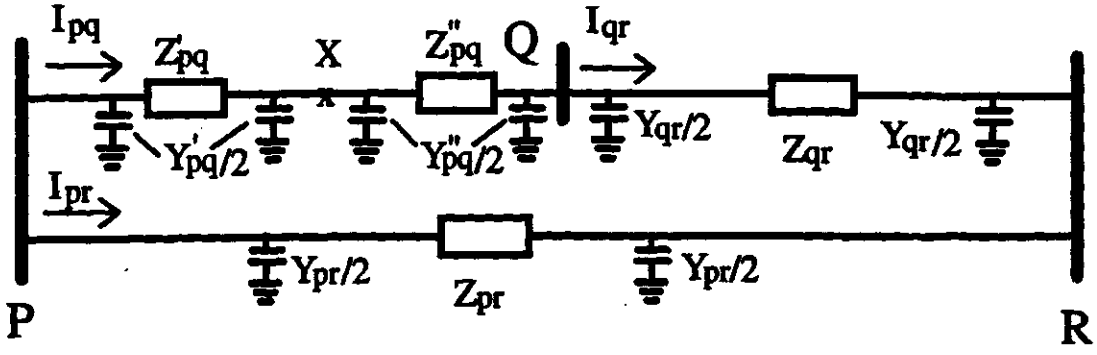

(c)

Figure 2.1. Transmission line modeled by lumped parameters (a) A typical single-phase transmission system; (b) The system represented by lumped parameter models; (c) The system represented by nominal π models.

$$V_x = A_{px} V_P - B_{px} I_{pq},$$
$$I_x = -C_{px} V_P + D_{px} I_{pq}, \qquad (2.3)$$

where:

$A_{px} = D_{px} = \cosh(\gamma_{pq} l_x)$,
$B_{px} = Z_0 \sinh(\gamma_{pq} l_x)$,
$C_{px} = \sinh(\gamma_{pq} l_x)/Z_0$ are the ABCD parameters of the line,
l_x is the length of the line from bus P to x,
$Z_0 = \sqrt{(r + j\omega l)/(g + j\omega c)}$ is the surge impedance of the line,
$\gamma_{pq} = \sqrt{(r + j\omega l)(g + j\omega c)}$ is the propagation constant of the line and
ω is the angular frequency in radians per second.

Similar equations can be derived in three-phase lines after they are de-coupled by proper transformations; this will be discussed in Chapter 5.

2.3. Protection of Transmission Lines

The functions of a transmission line protection system are to discriminate faults from other operating conditions, to identify faults in a designed protection zone from faults outside the zone, and to initiate the opening of circuit breakers for isolating the zone in which a fault has been detected.

A protection system usually consists of cts, ccvts, cables, protective relays and circuit breakers. To reduce the time required to disconnect a faulted circuit, communication channels are used. A typical line protection system is illustrated in Figure 2.2.

It is essential that EHV and UHV transmission lines be equipped with reliable, discriminative and high-speed protection systems. Economics is usually not an issue because the capital cost of a line is substantial and the cost of the protection system is a very small fraction of the line cost.

The levels of power system voltages and currents are reduced by cts and ccvts, to typically 110 V and 5 A, for applying to relays and other instruments. In addition to

reducing the levels of signals, cts and ccvts isolate the relays from the hostile electrostatic and electromagnetic environment of the power system.

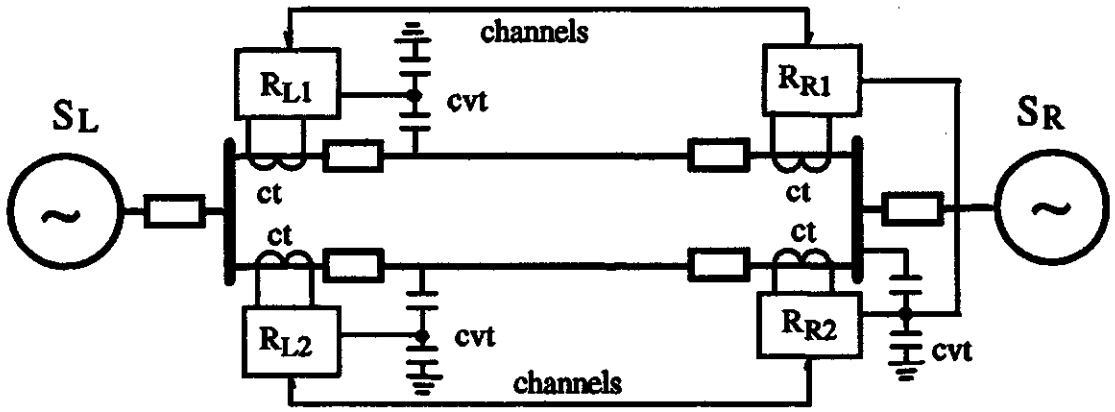

Figure 2.2. A typical transmission line relaying system.

Relays monitor changes in voltages and currents, and make appropriate decisions to open the circuit breakers when a fault occurs in the protected zone. The techniques used for transmission line protection can be classified as

(1) overcurrent and directional overcurrent,
(2) impedance measurement,
(3) directional or phase comparison,
(4) differential and
(5) traveling wave techniques.

2.3.1. Overcurrent and Directional Overcurrent Protection

The most commonly experienced phenomenon associated with faults on transmission lines is that the line currents at the relay location increase substantially. Overcurrent relays take advantage of this feature to protect lines, and also other devices. These relays operate when the current in the protected circuit exceeds a prespecified threshold. To reduce the relay operating time for faults close to its location, compared to the operating times for faults farther away from the relay, inverse-time overcurrent relays are used. This approach works well on radial configurations but fails when applied to interconnected networks.

In interconnected networks, faults on both the bus and line sides of the relay are associated with excessive current flows. To prevent the relays from operating for bus side faults, directional elements are included in overcurrent relays. The performance of a directional element can be expressed as

$$V_r I_r \cos(\theta - \tau) > K_0, \tag{2.4}$$

where:

V_r and I_r	are the voltage and current phasors,
K_0	is the minimum torque to operate the relay,
θ	is the angle between the voltage and current phasors and
τ	is the maximum torque angle of the relay.

Usually the voltages and currents of power systems are balanced during normal operating conditions but are unbalanced during single phase, two-phase and two-phases-to-ground faults. To detect ground faults, zero sequence overcurrent and zero sequence directional relays are used. Since the zero sequence currents are insignificant during normal operation, zero sequence current settings of about 30% of the line rating can be used.

2.3.2. Distance Protection

The principle of distance relays is briefly discussed in the first chapter. These relays are used universally on all levels of two terminal transmission lines. The main advantages of using distance relays are [4]

(1) the measurements of distance relays are independent of the system operating conditions and, to a large degree the magnitudes of fault currents and
(2) the relays have minimal transient overreach.

The phasors of voltages and currents applied to a measuring unit, V_r and I_r, must be carefully selected to obtain correct measurements. Six measuring units are usually used for the ten types of shunt faults. Table 2.2 lists voltages and currents applied to the measuring units and the faults they are able to detect.

Table 2.2. Measuring units, inputs applied to them and the faults they detect.

Measuring Unit	Phase Fault Unit 1	Phase Fault Unit 2	Phase Fault Unit 3	Ground Fault Unit 1	Ground Fault Unit 2	Ground Fault Unit 3
Voltages Applied to Relay	V_a-V_b	V_b-V_c	V_c-V_a	V_a	V_b	V_c
Current Applied to Relay	I_a-I_b	I_b-I_c	I_c-I_a	I_a+3kI_0	I_b+3kI_0	I_c+3kI_0
Suitable for faults	a-b, a-b-g, a-b-c	b-c, b-c-g, a-b-c	c-a, c-a-g, a-b-c	a-g	b-g	c-g

The accuracy of relay measurements depends on the selection of fault type. For example, to detect a phase a to phase b fault, shown in Figure 2.2.(b), the Phase Fault Unit 1 measures

$$\frac{V_r}{I_r}=\frac{V_a-V_b}{I_a-I_b}=kZ_l, \tag{2.5}$$

where:

Z_l is the impedance per unit length of the transmission line and
k is the distance from the relay to the fault.

Assuming that, $I_c= 0$, and V_c is not affected by the fault and has the rated value, the Phase Fault Unit 2 measures

$$\frac{V_r}{I_r}=\frac{V_b-V_c}{I_b-I_c}=\frac{I_bkZ_l-V_c}{I_b-I_c}=kZ_l-\frac{V_c}{I_b}. \tag{2.6}$$

The term V_c / I_b is an error of measurement that is not related to the distance of the fault. Other units also measure the distance incorrectly. A device for selecting the type of fault must be, therefore, used to activate the appropriate measuring unit.

A general equation that expresses the performance of distance relays is

$$|Arg(\frac{V_r - I_r Z_{set}}{V_{pol}})| \geq 90°, \qquad (2.7)$$

where:

Z_{set} is the impedance setting of the relay, and

V_{pol} is the polarization voltage applied to the relay.

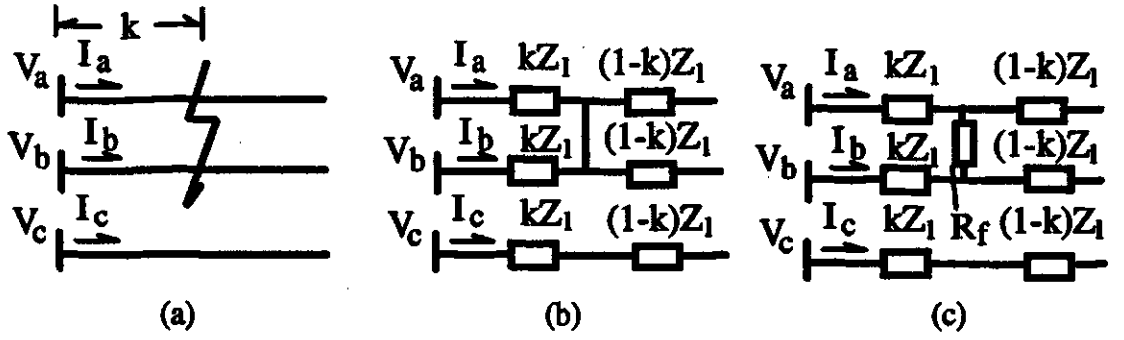

Figure 2.3. Equivalent circuit diagram of a phase a to phase b fault;
(a) system at the fault, (b) equivalent circuit and
(c) equivalent circuit with fault resistance, R_f.

Relaying characteristics can be changed by selecting different polarization voltages. Some of the characteristics achieved in this manner are shown in Figure 2.4. More sophisticated characteristics can be achieved by combining these characteristics.

At least two protection zones are required to protect the total length of a line. The first protection zone usually covers about 70 ~ 85% length of the line. Faults in this section are cleared instantaneously. The zone two relays, whose operation is delayed to coordinate with other relays, cover the whole length of line and a section of the other lines emanating from the remote terminal. The time delay is used to coordinate the operation with the relays protecting other lines. A third zone is conventionally used for backing up the operations of zone one and zone two relays.

The operation of distance relays is sensitive to the infeed from the remote terminal when fault resistance is present. In such a case, shown in Figure 2.3.(c), the measured impedance becomes

$$\frac{V_r}{I_r} = \frac{V_a - V_b}{I_a - I_b} = kZ_1 + R_f\left(1 + \frac{I'_a - I'_b}{I_a - I_b}\right).$$

The last term in this expression is the error in measuring the fault distance. The infeed causes the sending end relays to overreach and the receiving end relay to underreach. These situations are illustrated in Figure 2.5.

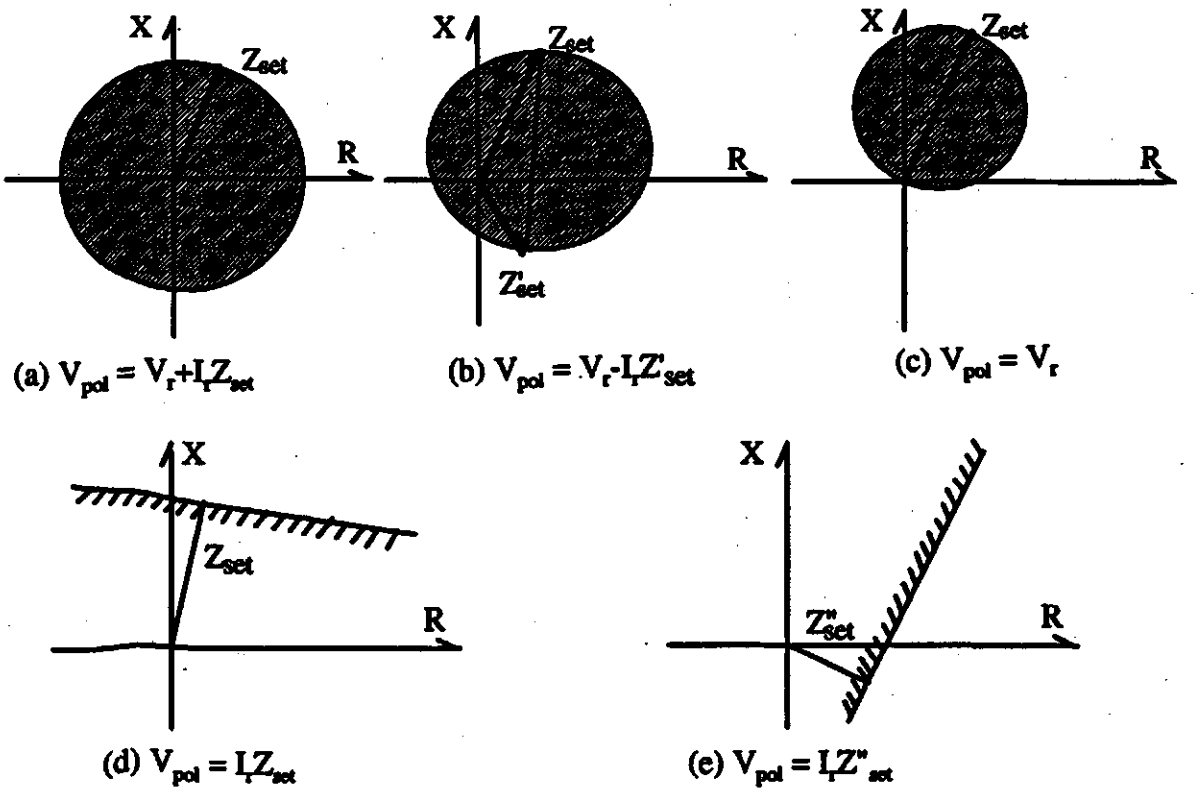

Figure 2.4. Typical relay characteristics used to protect transmission lines.

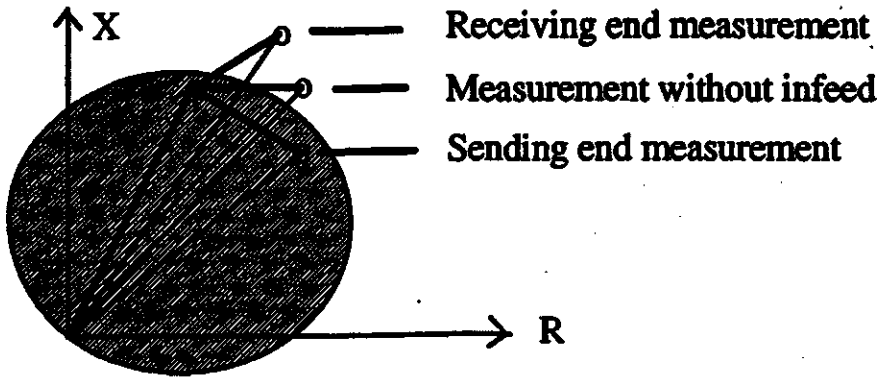

Figure 2.5. Impact of fault resistance on measured impedance.

2.3.3. Directional and Phase Comparison Protection

Directional comparison protection (DCP) discriminates fault by comparing the direction of power flow at the terminals of the protected line. A DCP consists of communication channels and directional relays located at each terminal. MHO distance relays, characteristic shown in Figure 2.4 (c), are commonly used to determine the direction of the faults.

Directional information is transmitted in the form of on-off signals. The bandwidth of the channel required to transmit this information is, therefore, relatively narrow. Power line carrier is commonly used in such application. The schemes used in practice include

1 directional comparison blocking,
2 directional comparison unblocking,
3 overreaching transfer trip,
4 permissive underreaching transfer trip and
5 non-permissive underreaching transfer trip.

The choice is based on system conditions, requirements and personal preferences.

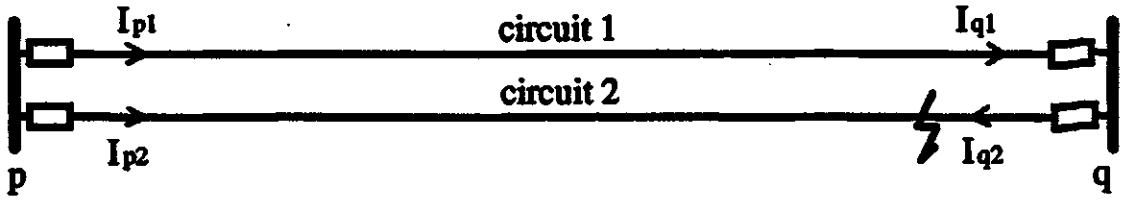

Figure 2.6. Phase relationship of terminal currents during a fault.

Phase comparison protection (PCP) takes advantage of the phase relationships of currents entering into the protected line from both terminals during normal operation. The operation of PCP can be illustrated by the system in Figure 2.6. If the line is free from faults, current flows into one terminal and flows out of the other terminal as is the case in Circuit 1. The two currents have a phase difference of approximately 180°. During faults, as in the case of Circuit 2, the phase difference reduces substantially.

Each relay transfers phase information to the other terminal on the operation of an overcurrent relay. Current waveforms are usually converted to square waves before transferring information. When the difference between the phases of the currents at the two terminals is less than a specified threshold, commands to trip the line circuit breakers are issued.

PCP schemes are relatively slow because they need at least one-half cycle data for comparison. Also, current waveforms often contain decaying dc and high frequency components, and filters are used to extract the fundamental frequency components.

2.3.4. Differential Protection

The principle of differential protection is derived from the Kirchhoff's current law. During the normal operating states, the net currents flowing into the line is zero if the line charging currents are neglected. The amplitude of the net in-flow of currents can provide an indication of the onset of an internal fault. Currents measured at the line terminals are combined to form a signal for operating the relay. A restraining signal is used to keep the relay from operating during the normal operating conditions and external faults.

Differential protection schemes require high quality channels to transfer the information concerning the waveforms of the currents. This becomes a limiting factor in the application of differential protection on short lines.

The characteristic of a typical differential protection is shown in Figure 2.7. The boundary between the operating and restraining regions can be described as

$$I_{op} - kI_{res} > I_{th}, \tag{2.8}$$

where:

I_{op}, I_{res}	are the operating and restraining currents in the differential relay,
I_{th}	is the threshold which prevents the relay from operating during light load conditions and
k	is the restraining coefficient.

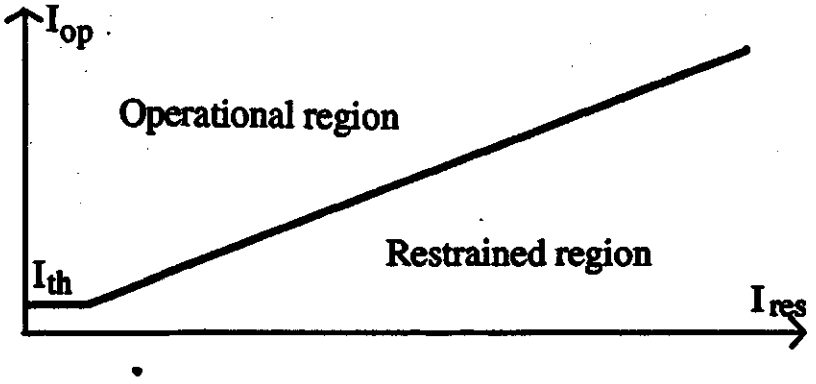

Figure 2.7. A typical biased differential protection characteristic.

2.3.5. Travelling Wave Protection

Disturbances on power systems generate travelling waves on transmission lines. These waves propagate from the fault to the line terminals. The wave propagation phenomena can be used to measure the direction and distance of a line fault. The phenomenon of travelling waves is the first to provide an indication of a line fault. It can, therefore, be used to achieve high speed protection. Many algorithms based on using travelling wave phenomena have been proposed [48-53].

2.4. Communication Channels Used for Protections

Basically two types of signals are transferred over relaying channels, signals containing information concerning the currents and voltages, and commands that are sent to trip remote circuit breakers. A variety of channels have been used for these purposes. The reliability and availability of the channels must be high because the functioning of the protection system depends on their performance. Relaying signals can either be transferred on dedicated communication channels or on channels rented from the Post Office. Five types of relaying channels are often used [4].

1. Pilot wires

Pilot wires, owned by power companies, provide a connection between relays installed at the terminals of a protected line; they usually follow the route of the line. The frequencies of transmitted signals can be dc, 50/60 Hz ac, or uncoded or coded audio tones [4].

The distance for which they can be applied is limited to about 30 km when uncoded low frequency signals are used. Pilot wires are vulnerable to electromagnetic interference (EMI) and, open and short circuit faults. The accumulation of charge on the station grounding mats during faults reduces the quality of the communication.

2. Rented telephone lines

Relay signals are also transmitted on rented telephone lines. Signals are modulated by audio tones and are transmitted at 600 or 1200 baud [4]. Unlike the dedicated relaying channels, the system is designed to tolerate occasional interruption by other users and to accept the consequences of the delay in tripping the lines. Rented telephone lines also suffer the same problems as pilot wires.

3. Power Line Carrier Systems (PLCs)

Relaying signals can be transmitted directly on the protected transmission lines. Radio frequencies in the 30 ~ 300 kHz range are used [4]. Other system signals, such as control, supervision and audio communication, are also transmitted by PLCs. Frequency band is allocated keeping in mind mutual interference between different bands and parallel lines.

4. Microwave channels

The frequency of microwave channels ranges among 2 ~ 12 GHz [4]. Multi-channel signals can be transferred within this band. Repeater stations must be within line of sight distance to transfer information by this media. The attenuation of signals is a function of weather and other ambient conditions.

5. Fiber Optic Links (FOL)

The frequency bandwidth of a FOL is in the video frequency range [4]. The advantages of FOLs include their immunity from EMI and their multi-channel transmission capacity. FOLs are expected to provide economic and reliable channels for both short and long distance communication.

Continuous transmission of signals between stations is not desired, particularly when rented facilities are used and channels are shared with other users. It is, therefore, desirable that transmission of information for relaying be started after a transient has been detected.

2.5. Single and Multi-pole Auto-reclosing Applications

More than 80 - 90% of transmission line faults are of temporary nature; they are caused by flashovers of insulators, swinging of conductors due to wind and contact with trees. They usually clear without any intervention from the operating staff. System can, therefore, be restored by automatically reclosing the circuit breakers after the arc plasmas have deionized.

Switching of major transmission lines can cause power swings. To avoid them, single phase tripping in the event of a phase-to-ground fault is sometimes implemented. This maintains the exchange of a major portion of the power being transmitted before the fault. On reclosing the open phase, the system resumes normal operation if the fault has cleared. If the fault has not cleared, all three phases are opened [9].

Similarly, multi-pole tripping and auto-reclosing on double circuit lines can improve system performance. This can be illustrated by the system in Figure 2.8. When two faults are simultaneously applied as shown in the figure, relays can trip and reclose faulted phases, leaving the other phases in operation. Even when the fault persists and the faulted phases are disconnected, the system in operation is a three-phase circuit.

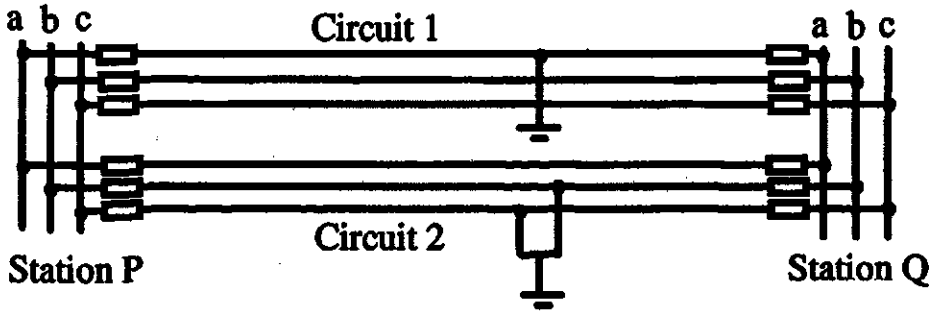

Figure 2.8. Simultaneous faults on a double-circuit line.

Single-pole tripping and reclosing improves system stability and reliability, especially in the case of long distance transmission lines. It also reduces switching overvoltages on the systems. For these reasons, single-pole tripping and reclosing has been widely used in EHV and UHV transmission lines as well as on important HV lines [4].

2.6. Summary

Protection practices for transmission lines are discussed in this chapter. The choice of protection for a particular line is based on the system configuration, importance of the line and economic benefits.

Non-unit protection schemes utilize local information only. Their performance does not depend on the quality of communication channels because none are used. They also provide back up protection in case other relays fail to clear faults. On the other hand, non-unit protections cannot rapidly remove faults near the far end of the protected line; some times this can cause system instability. Unit protection systems provide high speed protection of lines and provide better discrimination, but only if reliable channels are used for exchanging information between the line terminals.

The practice of auto-reclosing in power transmission lines must be taken into account when protection systems are designed. Relays should have the ability to coordinate with other restoration schemes used by the utility.

3. DEVELOPMENT OF COMPUTER RELAYING

3.1. Background

Performance of relays during faults on a line can be expressed by mathematical equations which express operating torques in terms of the inputs. Traditionally, relays were designed using electromechanical and electronic circuits. Electromechanical relays typically consisted of balanced beam, plungers, and induction discs and cup structures. These relays are robust and can withstand hostile electromagnetic and electrostatic enviornments experienced in power systems. Energized by currents and voltages from the secondary sides of cts and ccvts, they need large amounts of energy to operate. Their sensitivity and speed of operation are limited by their large mechanical inertias.

The development of solid state relays began about 30 years ago. Early designs had poor reliability and were susceptible to electromagnetic interference. Later designs were realized by using operational amplifiers and other integrated circuits, and with improvements in shielding techniques, their performance became acceptable. They consume less power compared to the power needed by their electromagnetic counterparts. Solid state relays also take less time to operate than the time their electromechanical counterparts take.

During the last ten years, microprocessor-based relays have been designed, marketed and used in power systems. They have several advantages over the electromechanical and solid state designs, especially in respect of reliability, economics, flexibility and new features, such as saving fault data and communicating with other devices. While several designs are presently available, there is a substantial scope for further research.

3.2. Basic Hardware of Microprocessor-based Relays

The hardware of a typical microprocessor-based relay is no more complicated than most off-the-shelf single-board computers. A block diagram of a microprocessor-based relay is shown in Figure 3.1.

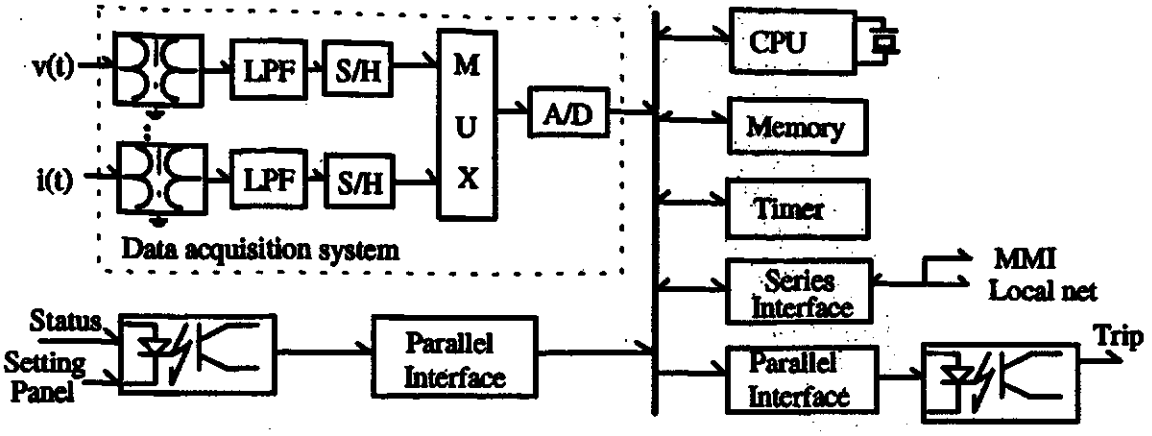

Figure 3.1. Block diagram of the hardware of a typical microprocessor-based relay.

The data acquisition system converts analog signals to digital data for use by the processor. Auxiliary cts and vts reduce the levels of voltages and currents, and provide isolation between the relay circuits and the power system. The outputs of the auxiliary cts and vts are applied to low-pass filters which attenuate the high frequency components in the signals. The cut-off frequency of the filter is decided by the Nyquist criteria and the sampling rate used. The outputs of the low-pass filters are applied to sample and hold circuits. A multiplexer connects one analog signal at a time to the A/D converter under control of the processor. The A/D converter quantifies the sample and provides it to the processor.

3.3. Relay Software

Relaying softwares can be divided into several functional blocks. A flow chart of a typical relay software is shown in Figure 3.2.

3.3.1. The Sampling Rate

In most on-line applications, sampling rate is critical to the software, especially when execution of the programs must be completed in one inter-sampling interval. The sampling rate should be, therefore, selected after considering the time it will take to execute the program during the most unfavorable condition. Even when a multi-microprocessor configuration is employed, care should be taken to avoid bottlenecks during critical situations.

Most algorithms are based on frequency domain analysis. Digital filtering techniques are used to obtain the fundamental frequency components of the inputs. A digital filtering algorithm usually needs one cycle of data to get a steady output. Short data windows generally lead to inadequate filtering. A variable data window can be used to achieve a compromise between fast operation and accuracy of measurement.

Unlike the frequency-domain analysis, algorithms based on differential equations are derived from the time domain relationships of voltages and currents. They, therefore, require no filtering [36]. Some of the differential algorithms need only small data windows. But the results are affected substantially by noise. To prevent relays from operating incorrectly, it is a common practice to hold their operation until the output is consistent for three or four successive decisions [1,2,3].

3.3.3. Fault Detection

The function of a fault detector, in a digital relay, is to sense the onset of a fault and start the algorithm. A fault detector, which usually monitors transient changes in voltages and/or currents, must have adequate sensitivity to operate under all system conditions; its failure could result in the relays not detecting the presence of a fault. The most commonly used fault detector function can be expressed as

$$|i_k - i_{k-N}| > T_{set}, \tag{3.1}$$

where:

i_k, i_{k-N} are k^{th} and $(k-N)^{th}$ samples of a current,
N is the number of samples in one cycle of the nominal frequency and
T_{set} is a preset threshold.

An alternative function, which is less susceptible to power swings, is

$$|i_k + i_{k-N/2}| > T_{set}. \tag{3.2}$$

3.3.4. Selection of the Faulted Phase

Selecting a faulted phase is important for a protection algorithm because only a few programs can be executed in the inter-sampling intervals usually encountered. It is also required when single- or multi-pole tripping schemes are used. A line protection algorithm, therefore, should be able to identify faulted phases of a circuit. Some

algorithms are inherently good at providing this information, while other algorithms require extra logic. A commonly used phase selection logic monitors the increases in phase currents after the inception of a fault. Table 3.1 lists the fault types and the current changes experienced due to the faults.

Table 3.1. Fault type and expected current change.

Current	a-b	b-c	c-a	a-g	b-g	c-g	3-phase
Δi_a	√	x	√	√	x	x	√
Δi_b	√	√	x	x	√	x	√
Δi_c	x	√	√	x	x	√	√

√ -- large current change, x -- small current change

Unfortunately, this logic does not always operate correctly because of mutual couplings between phases and because of the presence of noise in the observed currents. Better logic, therefore, is needed.

3.3.5. Self Diagnosis

The operation of conventional relays is routinely monitored and the relays are tested by the maintenance personnel to ensure that they continue to operate correctly.

Faults are frequently experienced on transmission lines, but the systems operate normally for most of the time. Relays monitor the power systems during their normal operation. Computer relays have the ability to monitor themselves. Self-monitoring programs carry out most tests automatically and without interfering with their operation. This enhances the reliability of these relays.

3.4. Algorithms

Relay algorithms can be classified into two categories

(1) algorithms that use voltage and current phasors and
(2) algorithms that use instantaneous values of voltages and currents.

Majority of the algorithms of digital relays use the voltage and current phasors of the nominal frequency of the power system. Because the current and voltage waveforms during a fault are rich in transient components, the algorithms are designed to have inherent filtering qualities.

3.4.1. Calculating Phasors

(1) Cross-Correlation with Orthogonal Functions

This technique assumes that power system voltages and currents are composed of the fundamental frequency and harmonic frequencies as well as dc components. Cross-correlation methods extract the components of the frequency of interest by projecting the signal on to a pair of orthogonal functions of that frequency.

At the k^{th} sample of a signal, the fundamental frequency component in it can be extracted by correlating the samples with the orthogonal functions. This procedure can be expressed as

$$X_r(k) = \frac{2}{N}\sum_{j=0}^{N-1} x(k-j)h(N-j),$$
$$X_i(k) = \frac{2}{N}\sum_{j=0}^{N-1} x(k-j)g(N-j), \qquad (3.3)$$

where:

x(m)	is the time sequence of a signal,
$X_r(k)$, $X_i(k)$	are the real and imaginary parts of the phasor,
h(m), g(m)	are a pair of the orthogonal functions and
N	is the data samples in one cycle of the specified frequency.

Two commonly used algorithms in this category are Fourier transform (DFT) and the Walsh transform algorithms [46, 47]. These algorithms extract the dc, and components of the fundamental frequency and harmonics. But the estimates they provide are adversely affected by the decaying dc component and by the components of the non-harmonics frequencies.

(2) Curve Fitting

Curve fitting techniques approach the filtering problem by assuming that the signals can be expressed by a polynomial consisting of a decaying dc and sinusoids of a few harmonics, such as

$$x(t) = K_0 e^{-t/\tau} + \sum_{j=1}^{M} \sqrt{2} K_j \sin(j\omega_0 t + \theta_j), \tag{3.4}$$

where:

K_j is the amplitude of the component of the j^{th} harmonic,
τ is the time constant of the dc component and
θ_j is the phase angle of the j^{th} harmonic.

Using the first two terms of the Taylor series expansion of $e^{-t/\tau}$ and expanding the terms of $\sin(j\omega_0 t+\theta_j)$ using the trigonometric identities, the following equation can be obtained [38].

$$x(t) = K_{01} + K_{02} t + \sum_{j=1}^{M} (K_{sj} \sqrt{2} \sin(j\omega_0 t) + K_{cj} \sqrt{2} \cos(j\omega_0 t)). \tag{3.5}$$

After n samples are obtained (n > 2(M+1)), the following matrix equation can be formed.

$$[X]_{nx1} = [A]_{nx2(M+1)} [K]_{2(M+1)x1}, \tag{3.6}$$

where

$[X]_{nx1}$ is a vector of n samples of data;
$[K]_{2(M+1)x1}$ is a vector of the unknown amplitudes which are to be determined.
$[A]_{nx2(M+1)}$ is the coefficient matrix.

The estimate of [K] can be obtained by

$$[K]_{2(M+1)x1} = [A]^{\dagger} [X]_{nx1}, \tag{3.7}$$

where

$[A]^{\dagger} = [[A]^T [A]]^{-1} [A]^T$ is 2(M+1) x n left pseudo-inverse of [A].

The advantage of this technique is that the effect of the decaying dc component and other non- harmonic frequencies can be taken into account.

(3) Kalman Filter

When power systems are in normal operation, currents and voltages are mainly composed of the fundamental frequency components. On the occurrence of a fault, the major components of the waveforms continue to be of the fundamental frequency. The dc and components of other frequencies can be considered as "noise".

Kalman filtering technique assumes that the components of the non-fundamental frequency can be expressed as "white noise". The design is, therefore, expressed by a stochastic state space equation.

$$[X]_{k+1} = [\varphi]_k[X]_k + [\Gamma]_k[W]_k ,$$
$$[Y]_k = [H]_k[X]_k + [\varepsilon]_k, \qquad (3.8)$$

where:

$[X]_{k+1}$ and $[X]_k$	are the $(k+1)^{th}$ and K^{th} estimate of the state variables respectively,
$[\Gamma]_k$	is the k^{th} noise coefficient matrix
$[\varphi]_{k+1}$	is the $k+1^{th}$ state transition matrix,
$[H]_k$	is the k^{th} measurement matrix and
$[W]_k$ and $[\varepsilon]_k$	is the k^{th} state noise and measurement noise matrices respectively.

A recursive Kalman filter is given by

$$[\hat{X}]_{k+1} = [\varphi]_k[\hat{X}]_k + [K]_{k+1}\{[Y]_k - [H]_k[\hat{X}]_k\}, \qquad (3.9)$$

where:

$$[K]_{k+1} = [P]_{(k+1)/k}[H]^T_{k+1}\{[H]_{k+1}[P]_{(k+1)/k}[H]^T_{k+1} + [R]_{k+1}\}^{-1},$$
$$[P]_{(k+1)/k} = [\varphi]_k[P]_{k/k}[\varphi]^T_k + [\Gamma]_k[Q]_k[\Gamma]^T_k \text{ and}$$
$$[P]_{(k+1)/(k+1)} = \{[I] - [K]_{k+1}[H]_{k+1}\}[P]_{(k+1)/k}$$

3.4.2. Differential-Equation Algorithm

Differential-equation algorithms are based on the series R-L models of transmission lines. For a single-phase model, the voltage can be expressed as

$$v(t) = R\, i(t) + L \frac{di(t)}{dt}, \tag{3.10}$$

where:

R and L are the line parameters.

Using the trapezoidal rule of integration, R and L can be estimated from three samples of the voltage and three samples of the current as follows [55]

$$R=\frac{(v_{k+1}+v_k)(i_{k+2}-i_{k+1})-(v_{k+2}+v_{k+1})(i_{k+1}-i_k)}{(i_{k+1}+i_k)(i_{k+2}-i_{k+1})-(i_{k+2}+i_{k+1})(i_{k+1}-i_k)},$$

$$L=\frac{(v_{k+2}+v_{k+1})(i_{k+1}+i_k)-(v_{k+1}+v_k)(i_{k+2}+i_{k+1})}{(i_{k+1}+i_k)(i_{k+2}-i_{k+1})-(i_{k+2}+i_{k+1})(i_{k+1}-i_k)}. \tag{3.11}$$

Because these equations use only three samples, the response is faster. However, both denominators are time functions and, therefore, errors are cyclically amplified. Least square method can also be used in conjunction with this approach to estimate the line parameters.

3.5. Summary

In this chapter, the recent developments of computer relaying are reviewed. These developments have provided a powerful tool for implementing complicated protection algorithms. Some basic techniques commonly used in computer relaying are discussed and compared. These discussions are the basis for the development of a relaying algorithm in chapter 6.

4. TRADITIONAL RELAYING METHODS FOR PROTECTION OF PARALLEL-TEED LINES

The benefits of having parallel-teed transmission lines (PTTLs) in modern power systems and the difficulties of protecting them are briefly discussed in Chapter 1. The basic techniques used for transmission line protection are outlined in Chapter 2. This chapter reviews the suitability of those techniques for protecting PTTLs.

The discussion is divided into two parts, one reviews the non-unit protection techniques and the other reviews the unit techniques. Examples are used to illustrate their suitability and limitations. Recent trends in protecting teed lines and PTTLs are briefly investigated to find clues for developing new approaches.

4.1. Non-Unit Protection Techniques

Non-unit protection techniques use local measurement of voltages and currents observed at a line terminal. Relays issue trip commands without using signal transferred from the other terminals.

4.1.1. Balanced-Current Protection

Balanced-current technique was originally developed for protecting two-terminal parallel transmission lines. The principle is illustrated with the help of Figure 4.1. Under normal conditions, a specified distribution ratio exists between the phase currents of the two lines. When a line experiences an internal fault, the distribution of current changes. The ratios of currents in each phase of the two circuits provide simple and efficient criteria for detecting the fault.

This principle can be extended to protect double-circuit PTTLs, such as, a fully parallel-teed arrangement with all branches in service. The currents of each phase of the two circuits at a location are equal if the circuits are identical. For the lines shown in Figure 4.1(a), an external fault does not cause the current ratios, I_2/I_1, I'_2/I'_1 and I''_2/I''_1, to change from their normal values. On the other hand, an internal fault, shown in Figure

4.1(b), causes the ratios I_2/I_1, I'_2/I'_1 and I''_2/I''_1 to change. When an internal fault is close to one of the terminals, the changes of the ratios of the currents at the remote terminals are too small to be detected but the changes of the ratios of the currents at the near end terminal are large. The relays at the remote terminals can not operate until the circuit breaker controlling the near-end terminal of the faulted line has tripped.

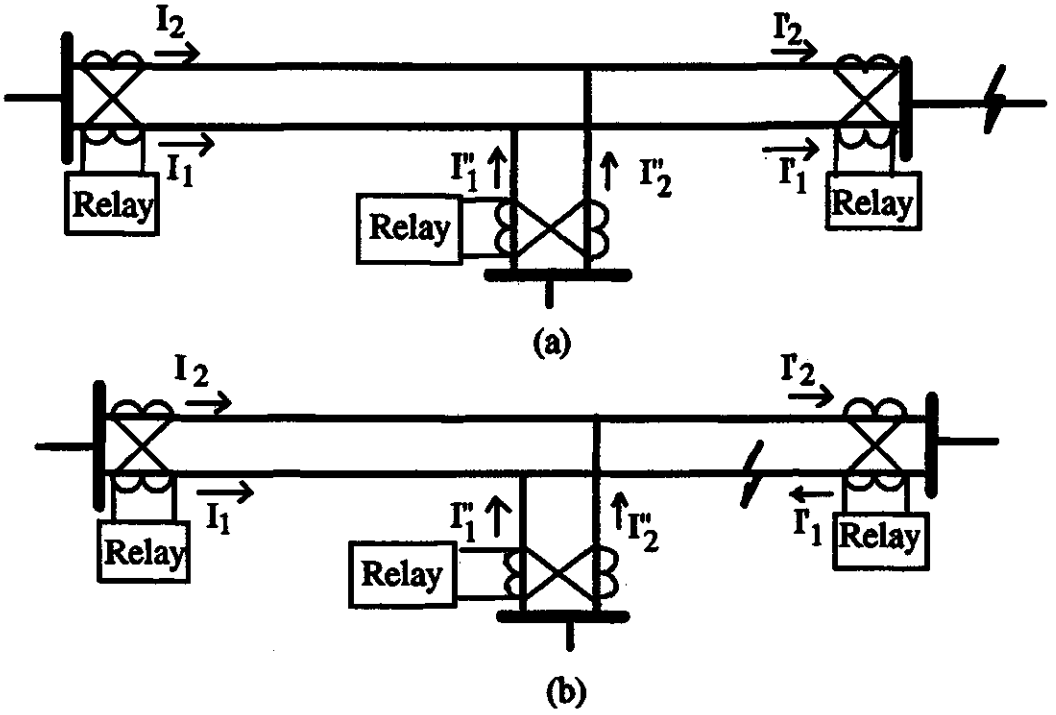

Figure 4.1. A balanced current protection arrangement.
(a) an external fault case, (b) an internal fault case.

The current unbalances in most parallel lines are substantial. A large threshold is, therefore, used. The performance equation used by the balanced current protection is

$$|I_\varphi\ (1) - K_r I_\varphi\ (2)| \geq M, \qquad (4.1)$$

where:

K_r is the ratio of the currents in the two lines,
M is a threshold to offset the unbalances,
φ represents the phases of the three phase line and
1, 2 represents Circuits 1 and 2 respectively.

The ratios of the line currents in parallel lines are the same during both the transient and the steady-state operation. It is, therefore, possible to use instantaneous values of currents in Equation 4.1; this is likely to increase the operating speed of the relay.

While it is easy to implement Equation 4.1, it can not be used when one of the two circuits is out of service. Appropriate logic and reliable communication between terminals are needed to monitor the line configuration. Also, the balanced circuit protection can not detect faults of the same type experienced simultaneously at the same location on both circuits. Moreover, the sensitivity of the relay changes with the location at which the faults are experienced. When the relay is disabled, backup protection must detect the inception of fault and open the controlling circuit breakers.

This technique is a simple and efficient method for protecting parallel lines. Interest in its use has been renewed with the advent of microprocessor-based relays [7, 8].

4.1.2. Impedance Protection

The principle of impedance relays is briefly discussed in Chapter 2. The performance of these relays when applied to parallel-teed transmission lines is examined in this section.

The impedance relays generally use inputs from transducers at the local terminal and, therefore, do not include the influence of current infeeds at other terminals. As discussed in Chapter 2, the current infeed causes large errors in measuring impedance if the fault resistance is large. In PTTLs, errors are introduced by current infeed and current outfeed at the terminals in addition to the fault resistance. If a ground fault is experienced on the line from bus R to the tap of the single circuit system shown in Fig. 4.2, the voltage at the relay location and impedance measured by the relay provided at P are

$$V_p = (I_p Z_p) + (I_p + I_r) k Z_q + (I_p + I_q + I_r) R_f,$$
$$Z_{app} = V_p / I_p = (Z_p + kZ_q + R_f) + (I_r / I_p) kZ_q + ((I_q + I_r) / I_p) R_f, \qquad (4.2)$$

where:

V_p is the voltage phasor measured by the relay at P,

I_p, I_q, I_r are current phasors measured by the relays at P, Q and R respectively,

Z_p, Z_q are the impedances of the line sections from buses P and R to the tap and
R_f is the resistance at the fault.

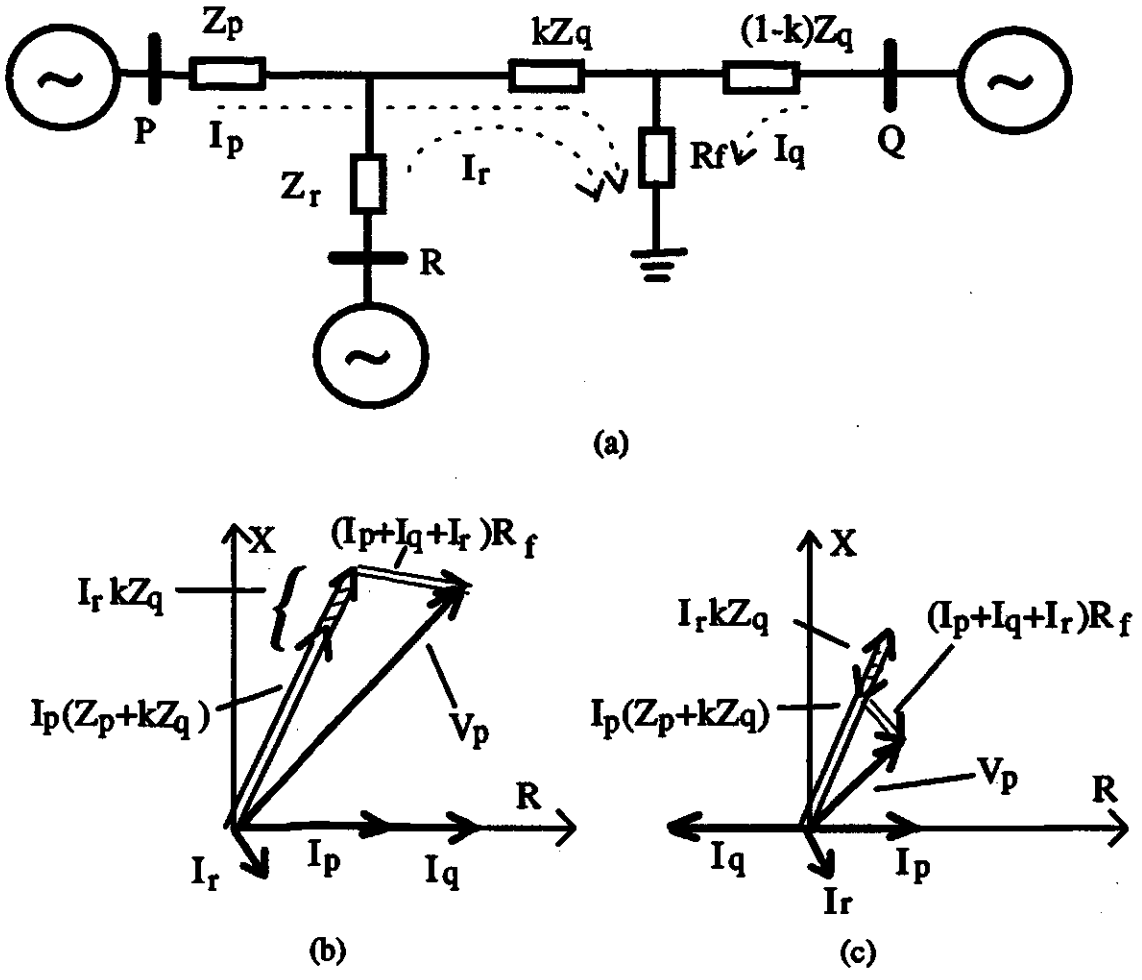

Figure 4.2. Impact of current infeed and outfeed on the impedance measurement.
(a) Single line diagram of a three phase fault, fault resistance is R_f.
(b) Apparent impedance as seen by the relay at *P* with current infeed from *Q* and
(c) Apparent impedance as seen by the relay at *P* with current outfeed from *Q*.

The phasor diagrams in Figures 4.2(b) and 4.2(c) show that the current infeed from *Q* causes the apparent impedance measured by the relay at *P* to be larger than the correct value, Z_p+kZ_r, whereas the current outfeed at Q causes the apparent impedance to be

smaller than the correct value. In both cases, the measured impedance to the fault is incorrect.

The relative branch lengths play an important role in selecting the settings of impedance relays. It is easy to set the relays when the lengths of the lines from the tee point to the remote terminals are equal. Unfortunately, most teed lines do not fall in this category. In one of the unfavorable situations, inputs from two physically close sources are brought to a tee junction which is then connected to a remote station. The first protection zone of the relay can include only a small portion of the line, while the second zone can protect only a small section beyond the tee point. This problem is shown in Figure 4.3.

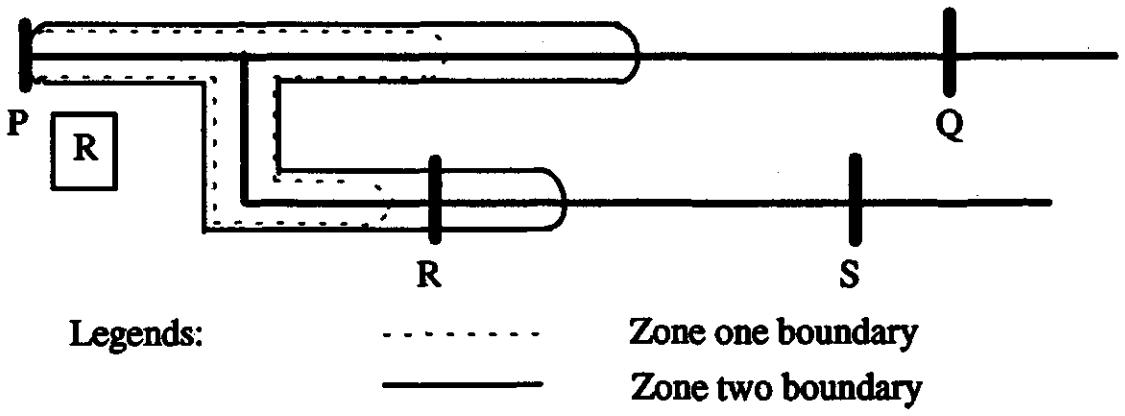

Figure 4.3. Relay settings for a teed line with branches of unequal length.

The electromagnetic coupling between parallel circuits also has an undesirable influence on the operation of relays, especially during ground faults when zero sequence currents in the parallel circuits are not properly compensated for. A phase selecting logic is required to provide compensation to ensure proper operation of the relays.

The relay performance can be improved by using information from the remote terminals or by updating the relay settings, to adapt to the prevailing system operating condition [30, 31]. The performance of the impedance relays can also be improved by using inter-trip schemes. This aspect is discussed later in the chapter.

Although there are reports that claim successful application of the impedance relays on teed lines, the level of success is not as high as is in their use on two-terminal lines.

4.1.3. Zero Sequence Over-Current Protection

Zero sequence overcurrent relays are widely used for transmission line protection but a number of problems arise when they are applied to PTTLs.

4.1.3.1. Current Variation Due to Operating Conditions

The amplitudes of the zero sequence fault currents depend on the fault location and the parameters of the line sections. Figure 4.4 shows the profile of the zero sequence current for faults along the line when one of the circuit breakers is open. It is seen that, to avoid incorrect operation of the relay at Q, the first zone should cover faults from P to B, which is only a small part of the line from P to Q.

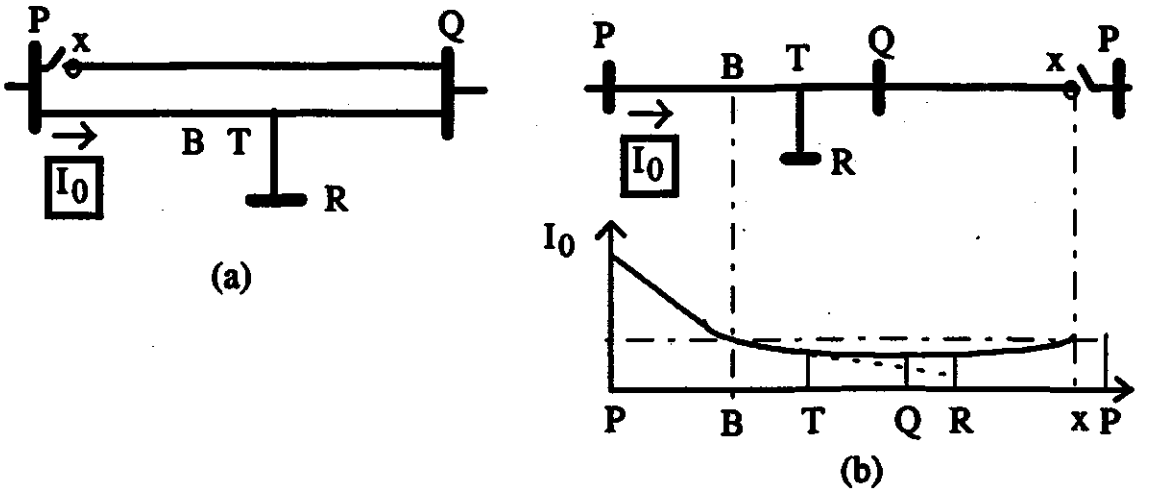

Figure 4.4. The amplitude of the zero sequence currents vs. the fault location along the line; (a) a single line diagram and, (b) a profile of the amplitude of I_0 with changing fault location.

Current level is also influenced by the change of the system configuration. For example, when one of the parallel lines is disconnected for maintenance, it is grounded at both terminals for reasons of safety. This is shown in Figure 4.5(a). In this case, zero sequence currents in the live circuit induce currents in the grounded circuit. For an

external fault on the bus at the remote terminal, the zero sequence circuit is as shown in Figure 4.5(b). The voltage equations for the two circuits are

$$V_0 = -I_{10}(Z_{10}+Z_{p0}) + I_{20} Z_m \quad \text{and} \tag{4.3}$$

$$0 = I_{20} Z_{10} - I_{10} Z_m , \tag{4.4}$$

where:

Z_m	is the zero sequence mutual impedance between the two circuits,
Z_{10}, Z_{p0}	are the zero sequence impedances of the line and source S_p,
V_0	is the zero sequence voltage at the fault location.

The equivalent zero sequence impedance of the line obtained from Equations 4.3 and 4.4 is

$$-V_0 / I_{10} = Z_{p0}+Z_{10} - (Z_m)^2/Z_{10}. \tag{4.5}$$

In this equation, $Z_{10} - (Z_m)^2/Z_{10}$ is the equivalent zero sequence impedance of the line, which is small when the mutual coupling between the parallel lines is large.

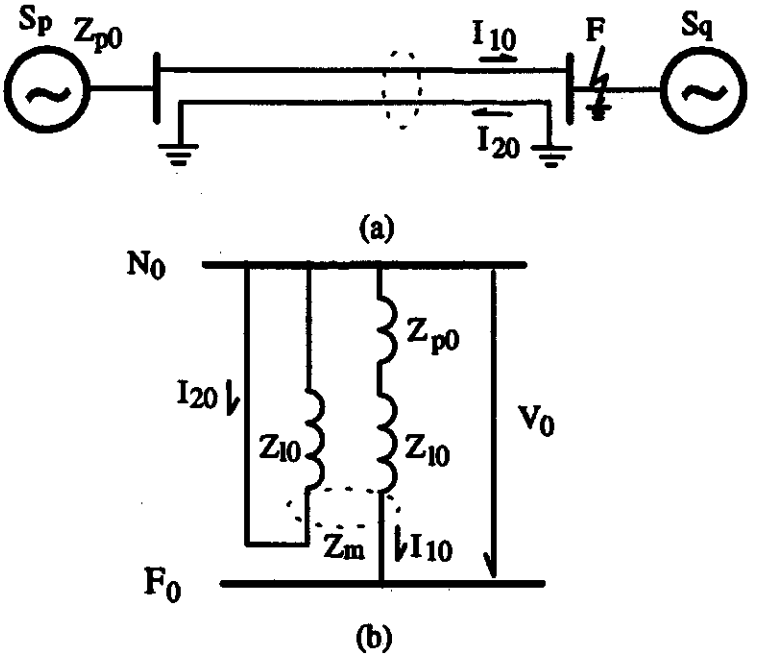

Figure 4.5. A double-circuit line with one circuit grounded at both ends; (a) a single line diagram of the faulted system, and (b) an equivalent zero sequence circuit.

Zero sequence overcurrent relays have to be disabled during certain abnormal operating conditions. For example, when one of the three phases is disconnected during single-phase tripping, the levels of zero sequence currents in the circuits are sufficiently large for the relays to operate.

4.1.3.2. Zero-sequence Current vs Fault Location

An effort was made to find the dependence of the level of zero sequence currents at a terminal of the parallel lines on the location of a fault. It was hoped that these changes might provide useful information for discriminating internal faults from those external to the parallel lines. The system shown in Figure 4.6 was considered. It was found that for a ground fault at F_1, the ratio of the zero sequence currents in the two circuits at terminals P is

$$\frac{I_{p1}}{I_{p2}} = \frac{Z_{qs} + (1-k')q(Z_{ps} + Z_{qs} + Z_l + Z_m) + A_q(Z_{ps} + pZ_m)/(Z_r + Z_{rs})}{Z_{qs} - (1-k')q(Z_{ps} + Z_{qs}) - A_q(Z_{ps} + pZ_m)/(Z_r + Z_{rs})}, \qquad (4.6)$$

where:

A_q	$= q[Z_{qs} + (1-k')(Z_{qs} + q(Z_l + Z_m))]$,
p and q	are the ratios of the lengths of the branches PT_1 and QT_1 to the length of the line PQ,
I_{p1} and I_{p2}	are zero sequence currents in circuits 1 and 2 respectively,
Z_{ps}, Z_{qs} and Z_{rs}	are the zero sequence impedances of the sources connected to P, Q and R buses,
Z_m	is the zero sequence mutual impedance between the two circuits,
Z_l	is the zero sequence impedance of the line and
k'	is the ratio of line length from P to the fault to that of length of line PQ.

For a fault at F_2, the ratio of the zero-sequence currents at P becomes

$$\frac{I_{p1}}{I_{p2}} = \frac{(k''C_{rm} + (p/q + k''))Z_{qs} + (1-k'')Z_{ps} + (1-k'')qk''C_{rm}}{(p/q + k'')B_q + (1-k'')Z_{ps} - C_{rm}k''Z_{qs} - [(1-k'')(2Z_{qs} + (1-k'')q(Z_m + Z_l)]}, \qquad (4.7)$$

where:

B_q $= Z_{qs} + (1-k'')q(Z_m + Z_l)$,

C_{rm} $= \dfrac{Z_{ps} + pZ_m}{Z_r + Z_m}$,

k" is the ratio of line length from the terminal T_1 to F_2 to the length of line T_1Q.

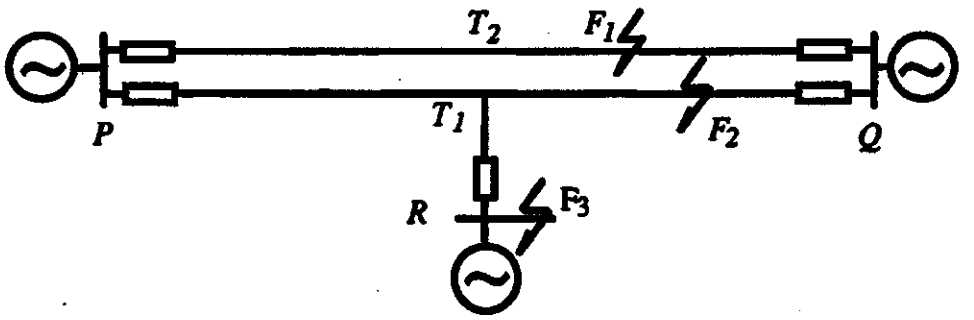

Figure 4.6. The fault locations considered for calculating the zero sequence currents.

When a fault is at F_3, the ratio of the currents is

$$\frac{I_{p1}}{I_{p2}} = \frac{pZ_{qs} - qZ_{ps}}{pZ_{qs} + qZ_{ps} + pq(Z_l + Z_m) - q(2Z_{qs} + q(Z_l + Z_m))}. \qquad (4.8)$$

These equations, derived in Appendix A, show that the distribution of the zero-sequence currents during internal faults vary with the location of the fault and the source impedances. Efforts to find suitable settings for the zero-sequence impedance relays on a double circuit transmission line were recently reported [58]. Neural network techniques were proposed to find a suitable compensating coefficient in the impedance calculation. However, this technique needs the knowledge of the prevailing source impedances at all the terminals and the up-to-date mode in which the parallel circuits are operating; these details are not always known in practice.

4.2. Unit Protection Methods

A unit-protection usually consists of communication channels and several relay units that are located at the line terminals. The examples of conventional unit protections include directional comparison, phase comparison and differential protection.

4.2.1. Directional Comparison

The principle of directional comparison protection was outlined in Chapter 2. A directional relay provided at a line terminal determines if the fault being experienced by the system is on the line-side or on the bus-side of the relay. Appropriate signals are sent to the other terminals to compare their power directions. Relays at each terminal make a decision to trip the circuit breakers after considering the decisions made by the remote relays from their own observations.

Since directional comparison relays are widely used in two terminal lines, it is often preferred to use them when two terminal lines evolve into teed or parallel teed lines. The blocking directional scheme is usually used to protect teed transmission lines [4]. The block diagram of the arrangement at one terminal of the system is shown in Figure 4.7. A Zone two distance relay at each terminal of the line monitors the power flow direction at the terminal. All relays are blocked if power flows out of any terminal of the protected line.

Two directional fault detectors are used at each terminal. The forward looking unit, FD, operates if power flowing into the line from this terminal exceeds a pre-set level. A trip signal is enabled if no blocking signal is received from the other terminals of the line. The operation of FD also disables the transmission of a blocking signal to the other terminal. A blocking signal is produced by a reverse looking unit, S, which monitors the power flowing out at the terminal of the line. The blocking signal is transmitted to disable the operation of relays at other terminals.

The sensitivity of the fault detectors provided at different terminals must be carefully coordinated to ensure correct operation. The local reverse looking unit, S, must operate for all phase and ground faults on the bus side, especially if they are likely to cause the FD units at other terminals to operate. For a parallel-teed line, the coordination is often difficult because the variations in fault current levels are large.

The power sources that are connected to a PTTL change considerably. Under some operating condition, a directional relay at a terminal connected to a weak source is not likely to operate; for example, when terminals P and Q are connect to load centers by transformers, as is shown in Figure 4.8(a). During an internal fault at F, currents contributed by the two terminals are small. The worst case is when the weak terminal

does not contribute sufficient fault currents to operate the relay but is able to maintain the arc at the fault point.

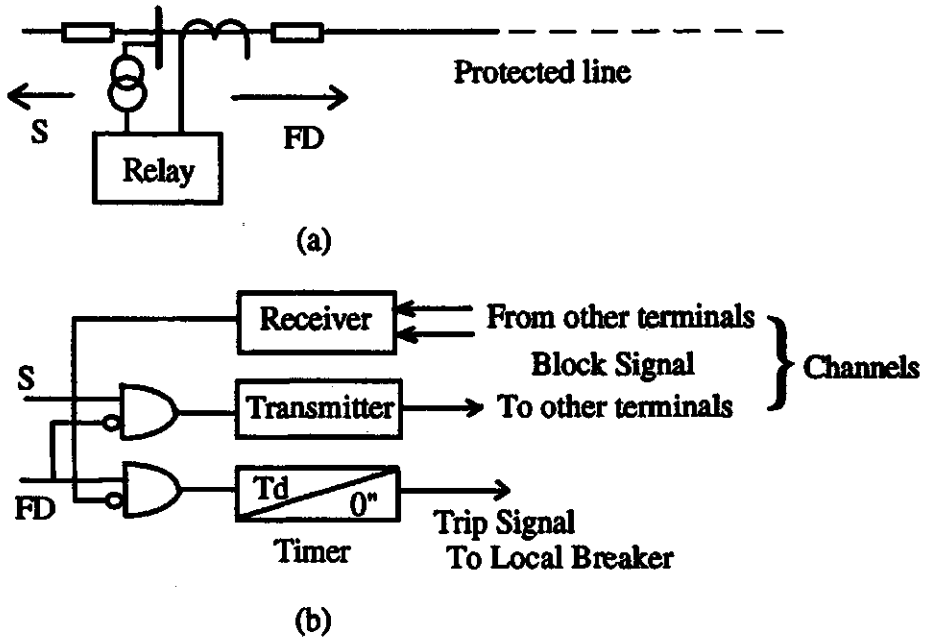

Figure 4.7. A block diagram of a directional relay system.

During an internal fault, currents may flow out from one terminal of the faulted line. This situation is shown in Figure 2.8.(b). Directional relays at this terminal sense an external fault and initiate blocking signals which disable the tripping of circuit breakers controlling the line.

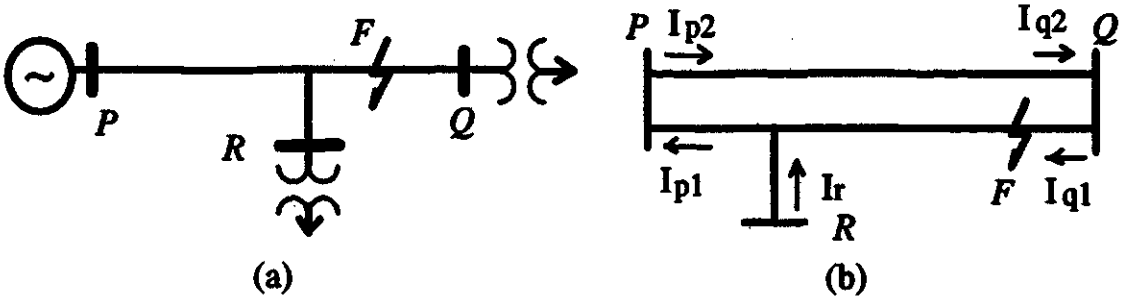

Figure 4.8. Examples that may produce mal-operation of directional protection.
(a) weak infeed at Side Q and R, and
(b) current outflow at terminal P.

4.2.2. Phase Comparison Protection

The principle of phase comparison protection is briefly outlined in Chapter 2. A phase comparison scheme does not require voltage signals and can save the expense of vts.

A phase comparison scheme requires two starting elements, operating at different levels, one to initiate the carrier transmitter and the other to enable tripping of circuit breakers controlling the line. The coordination of the starting elements at different terminals of a PTTL is difficult. Insufficient sensitivity of the starting element at a terminal results in a failure of the keying element to start the process phase comparison.

4.2.3. Differential Protection Scheme

Differential principle, as mentioned in the second chapter, uses the net current flowing in to or out of all terminals of the protected line as the operating current. When a line is shorter than 20 km, pilot-wire or rental telephone lines are conventionally used to transmit information between terminals.

Problems experienced by pilot protection systems, such as the requirement of good maintenance and inspection procedures to monitor open or short circuits on the pilot line, induction between the transmission line and the pilot line, and the uneven increase of ground voltages at the terminal stations, become more severe in PTTLs.

Interest in applying the differential principle on teed lines has been renewed with the improvements in communication technique and the developments of microprocessor-based relays. The increase of channel capacity due to the use of digital techniques have helped in reducing the cost of channels by sharing them with other users. It has also made it possible to use the differential principle on long transmission lines. Recent developments in differential protection for teed lines are reported in [16-25].

4.3. Summary

The advantages and disadvantages of protecting teed or parallel-teed lines by traditional relaying techniques are discussed in this chapter. The continuously changing

operating conditions dictate that large compromises be made when conventional protection techniques are used. In most situation, these compromises result in the performance being far less than desirable. Directional and phase comparison techniques are the often used unit protection techniques. Unfortunately, these technique fail to operate during certain operating conditions of PTTLs. The application of the differential principle is limited by the performance of the communication channels. With the advancements in communication techniques, differential protection has become the most promising technique for protecting PTTL's.

5. A COMPENSATED DIFFERENTIAL ALGORITHM

Among the relaying techniques discussed in the last chapter, differential protection is considered to the most suitable approach for protecting teed lines and PTTLs. The major benefits from applying differential protection on teed lines or PTTLs are as follows.

1. The performance of the differential principle does not depend on the change of current distribution, direction of fault and circuit breaker status at the terminals.

2. It is able to identify faulted phases, which facilitates the use of single- or selective-phase tripping and reclosing.

The operation of the differential protection scheme depends on the proper performance of the communication channels. The scheme also requires an effective method to synchronize the sampling of signals at all the terminals. The synchronizing method must not be affected by channel characteristics.

Errors due to the current transducers (cts) and inaccuracies of the line models impact the performance of differential protection adversely. The use of bundle conductors in HV and EHV transmission lines appreciably increases the charging currents [57]. With the development of microprocessor-based relays, it has become possible to improve the relay performance by compensating for the line charging currents.

5.1. Voltages and Currents at the Junction of a PTTL

A single line diagram of a general PTTL is shown in Figure 5.1. A single circuit teed line is similar to a PTTL when one of its circuits is out of service. Buses P, Q and R are the three terminals of the general PTTL model. Each terminal is either connected to different systems of the same power system.

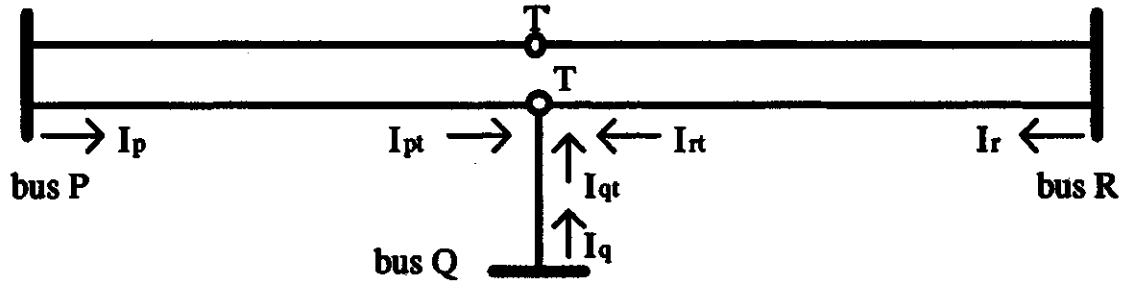

Figure 5.1. Single line diagram of a teed and parallel line.

5.1.1. The Single-Phase Teed Line Case

It is shown in Chapter 2 that, for a single circuit teed line, the voltages at the junction T and the currents entering the junction on the line from bus P can be expressed in terms of the voltages and currents at bus P as follows.

$$\begin{bmatrix} V_{t.p} \\ I_{t.p} \end{bmatrix} = \begin{bmatrix} A_{pt} & -B_{pt} \\ -C_{pt} & D_{pt} \end{bmatrix} \begin{bmatrix} V_p \\ I_p \end{bmatrix}, \tag{5.1}$$

where:

V_p, I_p are the voltage and current phasors at the terminal P,

V_{tp}, I_{tp} are the voltage and current phasors at the junction as estimated from V_p and I_p, and

A_{pt}, B_{pt}, C_{pt} and C_{pt} are the ABCD parameters of the line from bus P to the junction t.

When the line is represented by a distributed parameter model, the ABCD coefficients are

$$\begin{bmatrix} A_{pt} & -B_{pt} \\ -C_{pt} & D_{pt} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_{pt} l_{pt}) & -Z_{pt} \sinh(\gamma_{pt} l_{pt}) \\ -\sinh(\gamma_{pt} l_{pt})/Z_{pt} & \cosh(\gamma_{pt} l_{pt}) \end{bmatrix}, \tag{5.1.a}$$

where:

Z_{pt} is the surge impedance of the line and

γ_{pt} is the propagation constant of the line.

Similar equations for the voltages at the junction and currents entering the junction from buses Q and R in terms of the voltages and currents at buses Q and R can be obtained. These equations are as follows.

$$\begin{bmatrix} V_{t.q} \\ I_{t.q} \end{bmatrix} = \begin{bmatrix} A_{qt} & -B_{qt} \\ -C_{qt} & D_{qt} \end{bmatrix} \begin{bmatrix} V_q \\ I_q \end{bmatrix}, \tag{5.2}$$

$$\begin{bmatrix} V_{t.r} \\ I_{t.r} \end{bmatrix} = \begin{bmatrix} A_{rt} & -B_{rt} \\ -C_{rt} & D_{rt} \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix}, \tag{5.3}$$

where:

V_q, V_r, I_q, I_r	are the voltage and current phasors at bus Q and R,
$V_{t.q}$, $V_{t.r}$, $I_{t.q}$, $I_{t.r}$	are the voltage and current phasors at the junction estimated from the voltages and currents at bus Q and R.
Subscript qt, rt	denote the line parameters of the line Q-T and R-T respectively.

5.1.2. Three-Phase Teed Lines

There are mutual couplings between the conductors of three-phase transmission lines. Using the modal transformation technique, described in Appendix B, a three-phase system can be transformed into three independent modal systems. Equations 5.1 to 5.3 are valid for each of the modal systems. For example, modal currents flowing into the junction T on the line from bus P to bus T can be calculated from the modal voltages and currents at the bus P as follows.

$$\begin{aligned} I_{t.p.1} &= -C_{pt.1}V_{p.1} + D_{pt.1}I_{p.1}, \\ I_{t.p.2} &= -C_{pt.1}V_{p.2} + D_{pt.1}I_{p.2}, \\ I_{t.p.0} &= -C_{pt.0}V_{p.0} + D_{pt.0}I_{p.0}, \end{aligned} \tag{5.4}$$

where:

$I_{t.p}$	is the current phasor at the junction as estimated from the voltage and current at terminal P,
V_p and I_p	are the voltage and current phasors at the terminal P, and
1, 2 and 0	denote the mode 1, 2 and 0 quantities respectively.

If the lines are fully transposed, the parameters of the aerial modes, mode 1 and mode 2, are identical. The phase a current entering the junction can be estimated as follows.

$$I_{t.p.a} = I_{t.p.1} + I_{t.p.2} + I_{t.p.0} = -C_{pt.1}\,(V_{p.1} + V_{p.2} + V_{p.0}) + D_{pt.1}\,(I_{p.1} + I_{p.2} + I_{p.0})$$
$$-(C_{pt.0} - C_{pt.1})\,V_{p.0} + (D_{pt.0} - D_{pt.1})\,I_{p.0} =$$
$$= -C_{pt.1}\,(V_{p.a} + K_{cp}\,V_{p.0}) + D_{pt.1}\,(I_{p.a} + K_{dp}\,I_{p.0}), \qquad (5.5.a)$$

where:

$D_{pt.1}$ $= \cosh(\gamma_{pt.1} l_{pt})$

$C_{pt.1}$ $= \sinh(\gamma_{pt.1} l_{pt})/Z_{pt.0}$,

γ_1, γ_0 and γ_0' are the mode propagation constants of the line, and

the k_{dp} and k_{cp} are given by

$$k_{dp} = \frac{\cosh(\gamma_{pt.0} l_{pt}) - \cosh(\gamma_{pt.1} l_{pt})}{\cosh(\gamma_{pt.1} l_{pt})},$$

$$k_{cp} = -\frac{\sinh(\gamma_{pt.0} l_{pt})/Z_{pt.0} - \sinh(\gamma_{pt.1} l_{pt})/Z_{pt.1}}{\sinh(\gamma_{pt.1} l_{pt})/Z_{pt.1}},$$

Similarly, by using phases b and c as references, the following equations can be obtained.

$$I_{t.p.b} = -C_{pt.1}(V_{p.b} + K_{cp}\,V_{p.0}) + D_{pt.1}\,(I_{p.b} + K_{dp} I_{p.0}), \qquad (5.5.b)$$
$$I_{t.p.c} = -C_{pt.1}(V_{p.c} + K_{cp} V_{p.0}) + D_{pt.1}\,(I_{p.c} + K_{dp} I_{p.0}). \qquad (5.5.c)$$

By applying a similar procedure, the phase currents entering the junction from the lines from bus Q and bus R can be calculated as follows.

$$I_{t.q.a} = -C_{qt1}(V_{q.a} + K_{cq} V_{q.0}) + D_{qt1}\,(I_{q.a} + K_{dq} I_{q.0}),$$
$$I_{t.q.b} = -C_{qt1}(V_{q.b} + K_{cq} V_{q.0}) + D_{qt1}\,(I_{q.b} + K_{dq} I_{q.0}), \qquad (5.6)$$
$$I_{t.q.c} = -C_{qt1}(V_{q.c} + K_{cq} V_{q.0}) + D_{qt1}\,(I_{q.c} + K_{dq} I_{q.0});$$

and

$$I_{t.r.a} = -C_{rt1}(V_{r.a} + K_{cr} V_{r.0}) + D_{rt1}\,(I_{r.a} + K_{dr} I_{r.0}),$$
$$I_{t.r.b} = -C_{rt1}(V_{r.b} + K_{cr} V_{r.0}) + D_{rt1}(I_{r.b} + K_{dr} I_{r.0}), \qquad (5.7)$$
$$I_{t.r.c} = -C_{rt1}(V_{r.c} + K_{cr} V_{r.0}) + D_{rt1}\,(I_{r.c} + K_{dr} I_{r.0}).$$

5.1.3. Parallel Teed Transmission Lines

A PTTL can be modeled as either a fully transposed six-phase line or two parallel three-phase transposed lines. The voltages and currents at the junction T can be expressed in terms of terminal voltages and currents. These cases are examined here.

5.1.3.1. Two balanced three phase circuits

By this model, the two circuits are considered as two distinct, balanced three-phase circuit. Each line is equivalent to a three-mode system including two aerial modes and a ground mode. There is no coupling between the aerial mode currents but the ground mode currents in the two circuits are affected by the mutual couplings between the circuits. The following equations express the parameters for this case; [X] represents the line parameter matrices for the two circuits.

$$[X] = \begin{bmatrix} [X_1] & [X_3] \\ [X_3] & [X_2] \end{bmatrix},$$

where:

$$[X_1] = \begin{bmatrix} x_{l1} & x_{m1} & x_{m1} \\ x_{m1} & x_{l1} & x_{m1} \\ x_{m1} & x_{m1} & x_{l1} \end{bmatrix},$$

$$[X_2] = \begin{bmatrix} x_{l2} & x_{m2} & x_{m2} \\ x_{m2} & x_{l2} & x_{m2} \\ x_{m2} & x_{m2} & x_{l2} \end{bmatrix},$$

$$[X_3] = \begin{bmatrix} x_p & x_p & x_p \\ x_p & x_p & x_p \\ x_p & x_p & x_p \end{bmatrix},$$

x_{l1} and x_{l2} are the self impedances or capacitances of the phases of circuits 1 and 2 respectively,

x_{m1} and x_{m2} are the mutual impedances or capacitances between phases of each circuit and

x_p is the zero sequence mutual impedance between the two circuits.

By applying the procedure of Section 5.1.2 to Equations C.9, given in appendix C, Phase a current in circuit 1 can be expressed as

$$I_{t.x.a} = I_{t.x.1} + I_{t.x.2} + (I_{t.x.01} - I_{t.x.02})/2 =$$
$$- C_{xt.1}(V_{x.a} + K_{cx} V_{x.0}) + D_{xt.1}(I_{x.a} + K_{dx.1} I_{x.01} - K_{dx.2} I_{x.02}), \quad (5.8)$$

where:

x (= P, Q, R) denotes the terminal of the branch,

$I_{x.02}$ and $I_{x.02}$ are the ground mode currents in the two circuits,

$C_{xt.1}$, $D_{xt.1}$, $C_{xt.01}$, $C_{xt.02}$, $D_{xt.01}$ and $D_{xt.02}$ are ABCD parameters of the line from terminal X to T,

$$K_{cx} = \frac{C_{xt.01} - C_{xt.02} - 2C_{xt.1}}{2C_{xt.1}},$$

$$K_{dx.1} = \frac{D_{xt.01} - 2D_{xt.1}}{2D_{xt.1}}, \text{ and}$$

$$K_{dx.2} = \frac{D_{xt.02}}{2D_{xt.1}}.$$

Similar equations can be written for the other phases of the circuits.

5.1.3.2. Balanced six-phase model

In this situation, the procedure described in the previous section provides the following equation for the phase a current at the junction.

$$I_{t.x.a} = I_{t.x.1} + I_{t.x.2} + I_{t.x.3} + I_{t.x.4} + I_{t.x.5} + I_{t.x.0} =$$
$$= -C_{xt.1}(V_{x.a} + K_{cx} V_{x.0}) + D_{xt.1}(I_{x.a} + K_{dx} I_{x.0}), \quad (5.9)$$

where:

x denotes the terminal P, Q or R,

The subscript of 0 to 5 denote the six mode quantities respectively, and

$$K_{cx} = \frac{C_{xt.0} - C_{xt.1}}{C_{xt.1}},$$

$$K_{dx} = \frac{D_{xt.0} - D_{xt.1}}{D_{xt.1}}.$$

Currents in other phases can also be expressed in a form similar to Equation 5.9.

5.2. Compensated Differential Protection Algorithm

Based on the line equations derived in the previous section, a new compensated differential protection algorithm was developed as follows.

5.2.1. The Formation of Operating Current

At the tee junction, the following equations hold for each phase.

$$I_{t.p} + I_{t.q} + I_{t.r} = 0, \tag{5.10}$$
$$V_{t.p} = V_{t.q} = V_{t.r}. \tag{5.11}$$

Three combinations of currents that can be used as operating signals are

$$I_{op} = I_p + I_q + I_r, \tag{5.12.a}$$
$$I_{op} = I_{t.p} + I_{t.q} + I_{t.r}, \tag{5.12.b}$$
$$I_{op} = \Delta I_{t.p} + \Delta I_{t.q} + \Delta I_{t.r}, \tag{5.12.c}$$

In Equation 5.12.c, $\Delta I_{t.p}$, $\Delta I_{t.q}$ and $\Delta I_{t.r}$ are obtained by subtracting from the recently observed values the values of the currents observed one cycle earlier.

The impact of the use of the three types of operating currents is shown in Figure 5.2. The conventional operating current, described by Equation 5.12.a, is shown as a function of time as curve 1 in the figure. The compensated operating current, defined in Equation 5.12.b, is shown as curve 2 and the compensated delta-current is shown as curve 3. The compensated operating current is likely to perform the intended function better than the other two alternatives are likely to.

5.2.2. The Choice of Restraining Current

The operating current described by Equation 5.12.b is small when a PTTL is operating normally. In practice, however, the errors due to ct inaccuracies can be as high as 10%. Ct saturation, when experienced, further distorts current waveforms and

causes large spurious outputs during faults. The spurious operating currents must be adequately restrained so that the relay operates correctly. The use of a prespecified threshold usually requires a large setting. A restraining current that is proportional to the through current is, therefore, preferable.

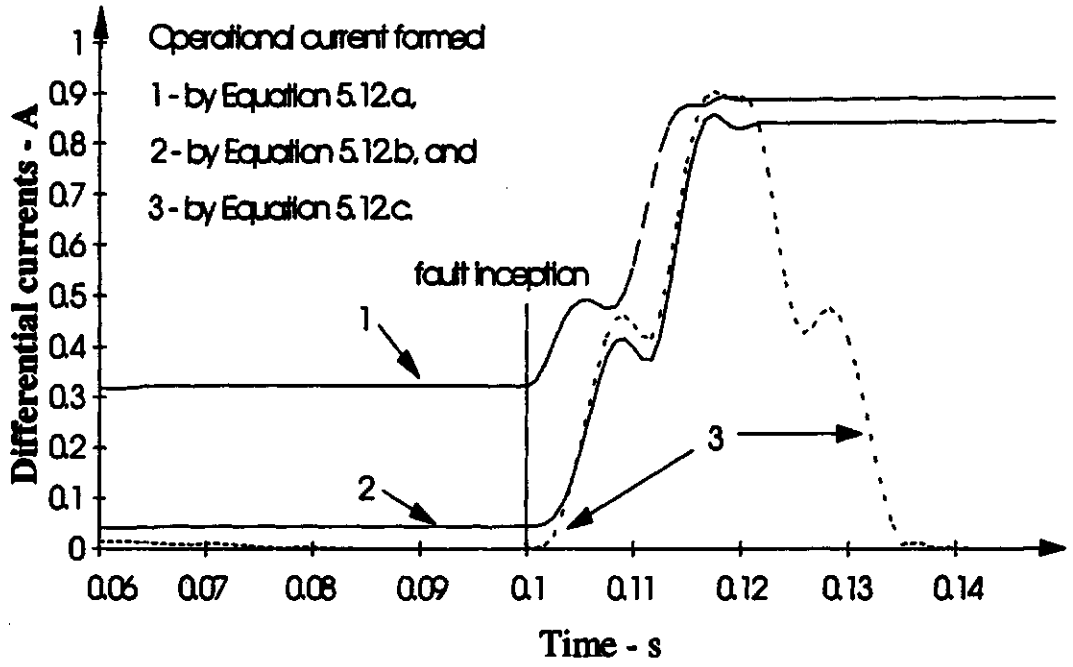

Figure 5.2. Comparison of different operational current.

Reference 20 proposed the use of a restraining current defined by

$$I_{res} = | I_p - I_q - I_r |, \tag{5.13}$$

where:

I_p, I_q and I_r are that phasors of the line currents observed at the buses P, Q and R respectively.

The fault currents are composed of the pre-fault currents and currents due to the fault. When the shunt capacitance effects are neglected, the prefault currents satisfy the condition

$$(I_q + I_r) = - I_p.$$

Substituting for ($I_q + I_r$) in Equation 5.13,

$$I_{res} = 2\, I_p.$$

The amplitude of this restraint, therefore, varies with the amplitude of the current at terminal P, and if I_p is zero, the relay has no restraint. The current at terminal P, in turn depends on the operating state of the system. The effectiveness of this form of restraint is, therefore, uncertain.

Another choice for the restraining current is

$$I_{res} = \text{Max} \{ |I_{t,p}|, |I_{t,q}|, |I_{t,r}| \}. \qquad (5.14)$$

This approach uses the maximum of the terminal currents as restraint irrespective of the nature of the systems connected to the three terminals. When the source is connected to one of the terminals only, the operating and restraining currents become the same. To ensure relay operation under this condition, the restraint setting of less than one must be used. The use of maximum current phasor can provide incorrect results for the first few samples after the inception of a fault. Based on these analyses, the following restraining current was selected.

$$I_{res} = k\, (|I_{t,p}| + |I_{t,q}| + |I_{t,r}|), \qquad (5.15)$$

where:

k is the restraint setting.

This choice avoids the problems experienced when the other options are used. The performance of the differential algorithm can now be expressed by

$$I_{op} > I_{res} \text{ and} \qquad (5.16)$$
$$I_{op} > k_s,$$

where:

k_s is a threshold setting.

5.3. Modification in One-Terminal-Open Condition

A section of a tapped system could some times be out-of-service. The teed line then becomes a conventional two-terminal-line except that it has a tapped open branch. The open branch may affect the behavior of the algorithm if substantial capacitance currents flow into it.

When vts are provided at each terminal on the line side of the controlling circuit breakers, equations derived in section 5.1 remain valid. However, if the vts are connected on the bus side at one of the terminals, the measured voltages should not be used in the equations and the algorithm should be modified as described in this section.

If terminals P and Q of the system shown in Figure 5.2 are connected to the sources, while the terminal R is not, the modal currents at R become

$$\begin{aligned} I_{r.0} &= C_{rt.0}V_{t.0} + D_{rt.0}I_{t.r.0} = 0, \\ I_{r.1} &= C_{rt.1}V_{t.1} + D_{rt.1}I_{t.r.1} = 0, \\ I_{r.2} &= C_{rt.2}V_{t.2} + D_{rt.2}I_{t.r.2} = 0. \end{aligned} \tag{5.17}$$

The current $I_{t.r.k}$ is now given by

$$I_{t.r.k} = -(C_{rt.k}/ D_{rt.k})\ V_{t.k},$$

where:

$V_{t.k}$ is the mode k voltage at the junction of the teed line.

$V_{t.k}$ can be estimated from the measurements taken at bus P (using Equation 5.1) as follows.

$$V_{t.k} = V_{t.p.k} = (A_{pt.k}\, V_{p.k} - B_{pt.k}\, I_{p.k}).$$

The current $I_{t.r.k}$ can be obtained by

$$\begin{aligned} I_{t.r.k} &= -(C_{rt.k}/ D_{rt.k})V_{t.k} = -(C_{rt.k}/ D_{rt.k})(A_{pt.k}\, V_{p.k} - B_{pt.k}\, I_{p.k}) \\ &= -C_{rp.k}V_{p.k} + D_{rp.k}I_{p.k}, \end{aligned} \tag{5.18}$$

where:

$C_{rp.k} = (C_{rt.k} / D_{rt.k}) A_{pt.k}$,

$D_{rp.k} = (C_{rt.k} / D_{rt.k}) B_{pt.k}$,

and $I_{t.r.a}$ can be obtained by

$$I_{t.r.a} = I_{t.r.1} + I_{t.r.2} + I_{t.r.0} = -C_{rp.1}(V_{p.1} + V_{p.2} + V_{p.0}) + D_{rp.1}(I_{p.1} + I_{p.2} + I_{p.0}) - (C_{rp.0} - C_{rp.1})V_{p.0} + (D_{rp.0} - D_{rp.1})I_{p.0}. \quad (5.19)$$

Combining Equation 5.19 with Equation 5.4.a,

$$I'_{t.p.a} = I_{t.r.a} + I_{t.p.a} = -C'_{pt.1}(V_{p.a} + K'_{cp}V_{p.0}) + D'_{pt.1}(I_{p.a} + K'_{dp}I_{p.0}), \quad (5.20)$$

where:

$C'_{pt.1} = C_{p.t1} + C_{rp.1}$,

$D'_{pt.1} = D_{pt.1} + D_{rp.1}$,

$K'_{cp} = K_{cp} + (C_{rp0} - C_{rp1})/C_{rp1}$,

$K'_{dp} = K_{dp} + (D_{rp0} - D_{rp1})/D_{rp1}$.

The equations for the operating currents of the other phases can be written in a similar form.

When the terminal R is open, the operating currents should be modified as

$$\begin{aligned} I'_{op.a} &= I'_{t.p.a} + I_{t.q.a}, \\ I'_{op.b} &= I'_{t.p.b} + I_{t.q.b}, \\ I'_{op.c} &= I'_{t.p.c} + I_{t.q.c}. \end{aligned} \quad (5.21)$$

A similar procedure can be used when side Q is open or when side Q and R are open.

5.4. Performance During Unbalanced Operation

Systems are occasionally unbalanced, for example, when at single phase has been tripped but the circuit breaker has not been reclosed. In this situation, shown in Figure 5.3, there is a considerable unbalance between currents in the circuit. The differential relay must operate correctly under such conditions.

For the two phases which are in operation, Equations 5.5 to 5.7 remain valid and the algorithm is able to detect internal faults. If the ccvts are connected on the line side, the equations are valid for the disconnected phase. If they are on the bus side, the equations can not be used because the voltages at the line terminals are not known. Since this phase is already open, relay of this phase can be disabled when its circuit breaker is open.

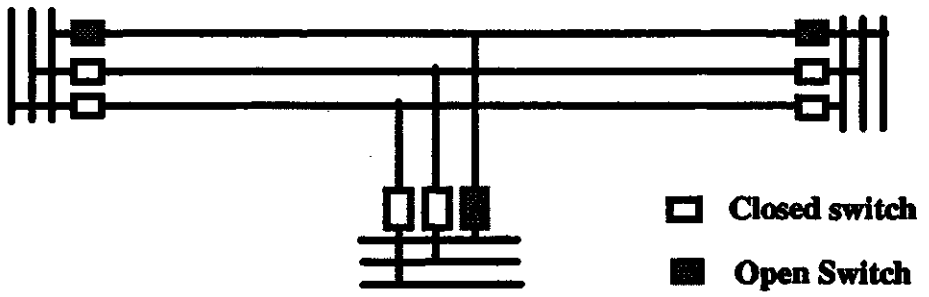

Figure 5.3. One-Phase-Open condition.

5.5. Summary

A compensated differential protection algorithm is developed in this chapter. Using the distributed parameter model of a transmission line, the algorithm takes into consideration the effect of line charging currents. This reduces the operating current during normal operation and during external faults. It also allows the sensitivity of the relay to be increased.

The validity of the algorithm, when the line is operated with one phase open, is examined. To improve the performance of the algorithm, when the line is disconnected at one of its terminals, on-line modification of the relay coefficients is suggested.

6. RELAY DESIGN

An algorithm for differential protection of teed parallel transmission lines is developed in Chapter 5. Some design aspects for using the algorithm in a protection system are discussed in this chapter. These include techniques for fault detection and data synchronization.

6.1. Protection System and Evaluation

A block diagram of a typical differential protection system is shown in Figure 6.1. The system consists of three microprocessor-based relays, one at each terminal. The phase voltages, and currents in each circuit are sampled by the local relay. Low-pass filters are used to attenuate high frequency components in the inputs. Digital I/O interfaces monitor the status of local and remote switches, exchange signals with other devices, scan relay settings and issue trip commands. Communication channels between the terminals of the line are used to send information concerning phasors of voltages and currents and transmit trip commands.

A master-slave protocol is assumed for estimating the communication requirements of the proposed system. The two slave relays monitor the local signals and estimate the voltage and current phasors at the tee point. They transmit the current phasors to the master station over the channels on receiving a request from it. Trip commands are sent from the master relay to the slave relays. The location of the master relay is not critical. In the example used to illustrate the working of the proposed system, it is assumed that the master relay is provided at terminal P.

6.1.1. Channel Throughput

It is assumed that the HDLC protocol [58], which is supported by a wide range of hardware devices, is used. This bit-oriented-protocol allows flexible length of data to be carried in one frame. The structure of the protocol is shown in Table 6.1.

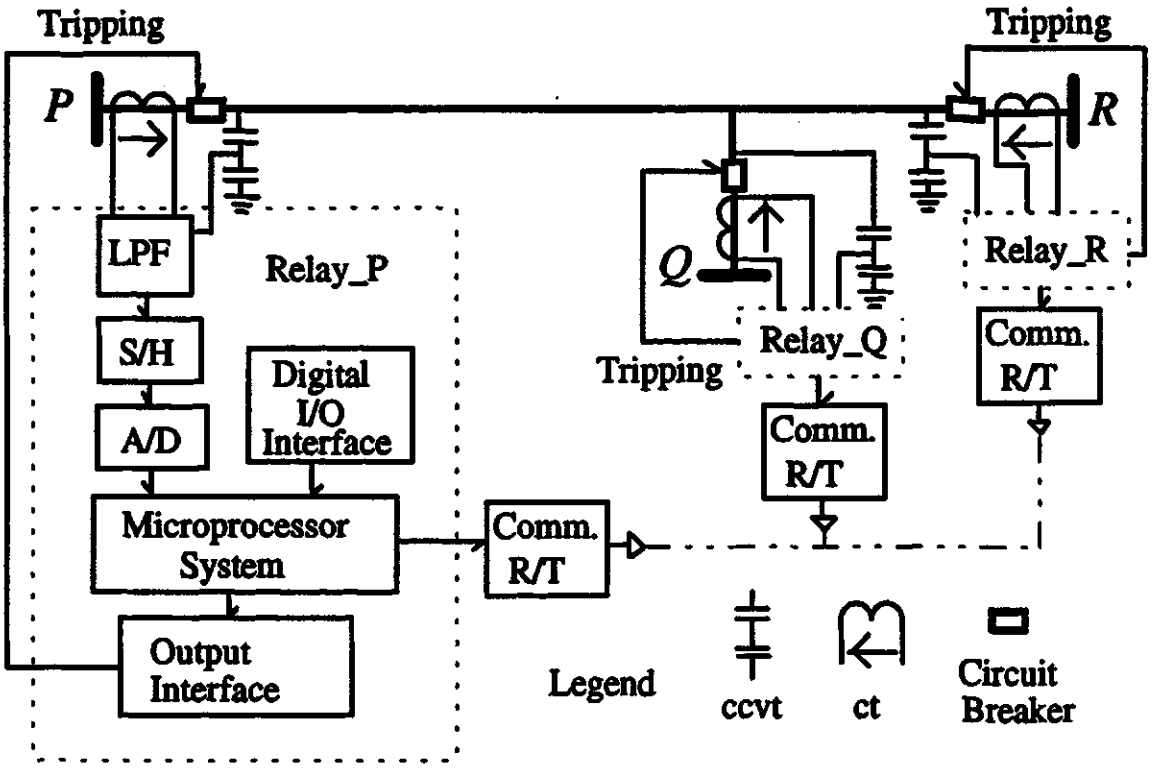

Figure 6.1. Block diagram of a differential protection system for a PTTL.

Table 6.1. Frame format for the HDLC protocol.

8 bits	8 bits	8 bits	any bits	16 bits	8 bits
Start flag	Address field	Control field	Information field	CRC check	Stop flag

Since the data to be transmitted, at each sampling instant, consists of four 16-bit words, (one word for each current phasor and, one word for status and other information), the communication requirement is four 16-bit words, or 64 bits. The start flag, address field, control field, CRC check field and stop flag take 48 bits and the total length of one HDLC frame is, therefore, 112 bits for each circuit.

6.1.2. Selecting Sampling Frequency

The sampling frequency of a microprocessor-based relay is limited by the clock-rate of the microprocessor and the capabilities of the communication facilities. The microprocessor must be able to finish its designated program within each sampling interval, and the required data must be transmitted to the destination terminals within the interval.

If dedicated relaying channels are not available, the protection system has to share channels with other users. CCITT (International Telegraph and Telephone Consultative Committee) Recommendation X.25 [59] suggests using a rate of 64 kbps for voice and data transmission. According to this rate, the maximum frequency for transmitting frames is given by

$$f_{t,max} = \frac{64{,}000}{\text{frame length}} \ Hz. \tag{6.1}$$

As described in chapter 3, relay output is considered valid only when the data window contains sufficient fault data. Data of several successive samples can be packed into one frame to increase the communication efficiency. The maximum sampling frequency, therefore, can be decided by multiplying $f_{t,max}$ with the number of samples included in a frame. A few examples are listed in Table 6.2.

Table 6.2. Frame length vs number of sampling sets included in one frame.

Number of sampling sets	1	2	3	4
Frame length	112 bit	160 bit	208 bit	256 bit
Transmitting frequency for frame	571 Hz	400 Hz	308 Hz	250 Hz
Maximum sampling frequency	571 Hz	800 Hz	923 Hz	1000 Hz
Recommended sampling rate	480 Hz	720 Hz	840 Hz	960 Hz

When dedicated fiber optic links are available, the transmission rate can be as high as 1.544 Mbps [60]. In such cases, the sampling rate of the relay is only limited by the processing speed of the microprocessor.

It is worth noticing that the calculations can be shared by the three relays, each performing only a part of the computations. For example, if a sampling frequency of 1200 Hz is selected, the interval between consecutive samples is 833 μs. The selected microprocessor should be able to execute the proposed algorithm within this interval.

6.2. Phasor calculation and Fault Detection

A simplified flow chart of the protection program is shown in Figure 6.2. The techniques that can be used for calculating the phasors are briefly outlined in the paragraphs that follow.

6.2.1. Fundamental Frequency Phasors

One-cycle Discrete Fourier Transform (DFT) algorithm, defined by Equation 6.2, was used to computer the 60 Hz phasors of voltages and currents.

$$X_{r.k} = \frac{\sqrt{2}}{N} \sum_{i=k-N+1}^{k} x_i \sin\left(\frac{2(i-k)\pi}{N}\right),$$
$$X_{j.k} = \frac{\sqrt{2}}{N} \sum_{i=k-N+1}^{k} x_i \cos\left(\frac{2(i-k)\pi}{N}\right), \qquad (6.2)$$

where:

$X_{r.k}$ and $X_{j.k}$	are the real and imaginary components of the phasors,
x_i	is the i^{th} sample of the signal and
N	is the number of samples in a cycle of the signal.

Non-recursive calculations are used for estimating phasors of voltages at the tee junction of the lines.

6.2.2. Transient Detector

The function of the transient detectors is to start the differential algorithm. The operating speed of the protection system will be, therefore, affected by the speed of fault detection. As described in Chapter 3, changes in terminal currents are traditionally used to start microprocessor-based relays, but fault detectors using this technique are

inherently slow. On the other hand, teed transmission lines are often characterized by wide variations of current distribution. A fast, reliable fault detector technique with stable sensitivity is, therefore, needed.

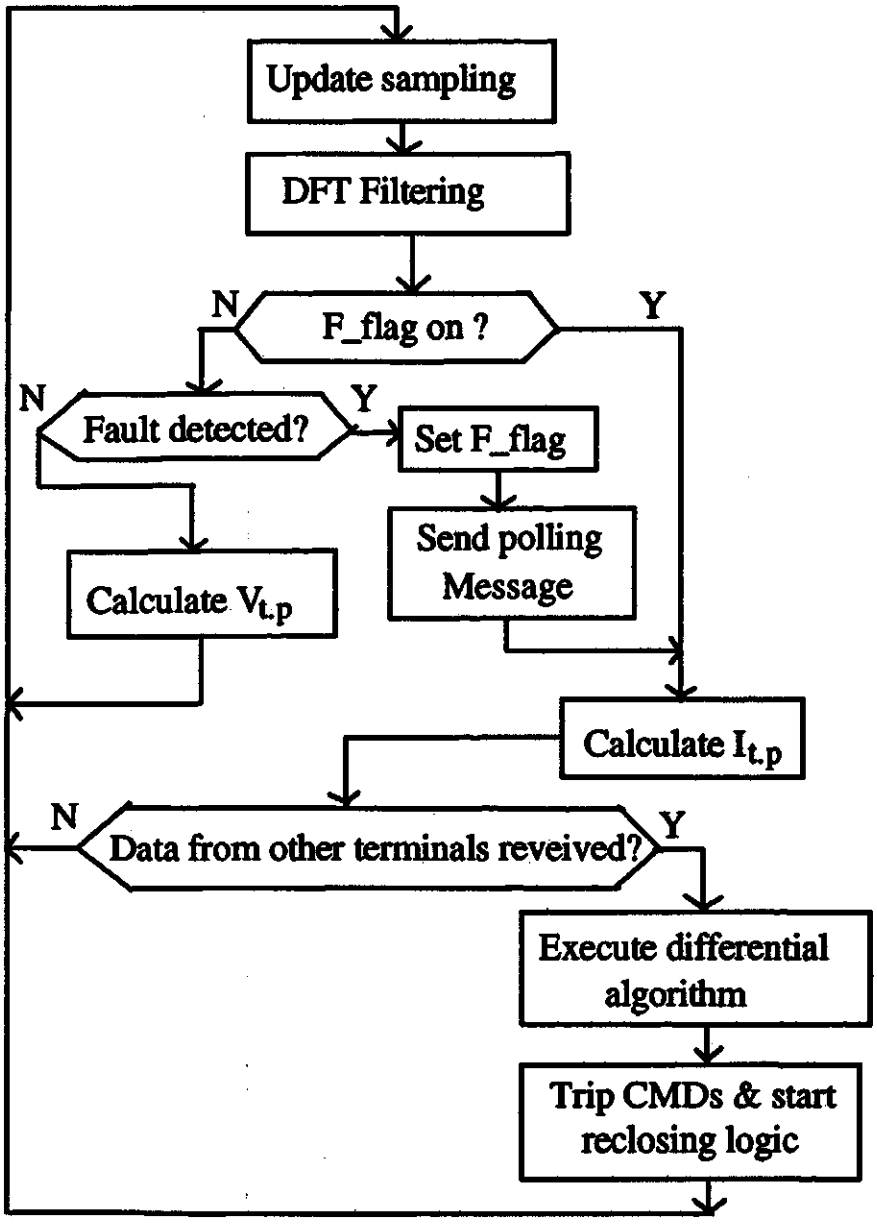

Figure 6.2. Flow chart of the differential program for the master relay.

A transient detector, based on the theory of transmission lines, is proposed. When a fault is experienced on a line, it initiates waves which start from the fault and propagate to the line terminals. The traveling waves observed at the line terminal are the earliest indications of a fault. At the relay location, two types of modal waves can be identified [48,49]; these are

$$W_f = \Delta v + \Delta i Z_0 \text{ and}$$
$$W_b = \Delta v - \Delta i Z_0, \tag{6.3}$$

where:

W_f is the forward traveling wave,
W_b is the backward traveling wave,
Z_0 is the surge impedance of the line for the relevant aerial mode and
Δv ,Δi are the incremental voltage and current respectively.

The criterion of the transient detector can be expressed as

$$F_d(k) = |\Delta v(k)| + |\Delta i(k)|\,|Z_0| \geq T_{hre}, \tag{6.4}$$

where:

k denotes the k^{th} samples and
T_{hre} is a threshold.

6.2.3. Compensated Voltages and Currents

The technique for estimating on-line currents and voltages at the tee junction from the observations at the line terminals are discussed in the previous chapter. The phase currents at the tee junction are estimated from the currents and voltages at the P terminal by

$$\begin{bmatrix} I_{t.p.a} \\ I_{t.p.b} \\ I_{t.p.c} \end{bmatrix} = -\begin{bmatrix} C_{pt.1} & 0 & 0 \\ 0 & C_{pt.1} & 0 \\ 0 & 0 & C_{pt.1} \end{bmatrix}\begin{bmatrix} V_{p.a} \\ V_{p.b} \\ V_{p.c} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}(C_{pt.1} - C_{pt.0})V_{p0} +$$
$$+\begin{bmatrix} D_{pt.1} & 0 & 0 \\ 0 & D_{pt.1} & 0 \\ 0 & 0 & D_{pt.1} \end{bmatrix}\begin{bmatrix} I_{p.a} \\ I_{p.b} \\ I_{p.c} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}(D_{pt.0} - D_{pt.1})I_{p0}, \tag{6.5}$$

Similar equations are used by the relays at terminals Q and R.

6.3. Data Synchronization

Based on the observations at the local terminal, each relay estimates a phasor of the aerial mode voltage at the tee junction of the line during normal operation. Following equation is used for this purpose.

$$V_{t.x} = (V_{t.a}-V_{t.b})_{.x} = A_{xt}(V_{a.x}-V_{b.x}) + B_{xt}(I_{a.x} - I_{b.x}), \qquad (6.6)$$

where:

A_{xt} and B_{xt}	are the aerial mode parameters of the line and
subscript x	represents p, q or r terminal respectively.

The discrepancy between the voltage phasors calculated from the observations taken at the three terminals during a normal operating state of the system is used to synchronize data.

The relay at each line terminal saves, in the memory of the microprocessor, the estimated modal voltage at the tee junction of the line using Equation 6.6. The relays at the master terminal monitor the system for transients. On the operation of the transient detector, the master relay sends to the remote relays a polling message which contains the angle of the modal voltage calculated just before the operation of the transient detector.

The slave relays implement the procedure shown in Figure 6.3. The angle contained in the polling message is used as a synchronous reference. Each slave relay searches the data in its memory banks for a sampling instant at which the difference between the angles of modal voltages estimated by the master and slave relays is minimum. The adjusting angles, defined by

$\Delta\angle V_q = \angle V_{t.p} - \angle V_{t.q}$ at station Q and
$\Delta\angle V_r = \angle V_{t.p} - \angle V_{t.r}$ at station R .

are then used to align the current phasors at the junction estimated by the slave relays as follow.

$$I_{t.q}(new) = I_{t.q}(old)\ \angle(\Delta\angle V_q + \theta_{qi}),$$
$$V_{t.r}(new) = I_{t.r}(old)\ \angle(\Delta\angle V_r + \theta_{ri}), \qquad (6.8)$$

where:

θ_{qi} and θ_{ri} are the phase angles of the phasors of the compensated currents and voltages,

$I_{t.r}(old)$ and $I_{t.q}(old)$ are the current phasors calculated by using Equations 5.5 and 5.7 and

$I_{t.q}(new)$ and $I_{t.r}(new)$ are the calculated synchronized current phasors.

The synchronized data are sent to the master relay where the differential algorithm is implemented.

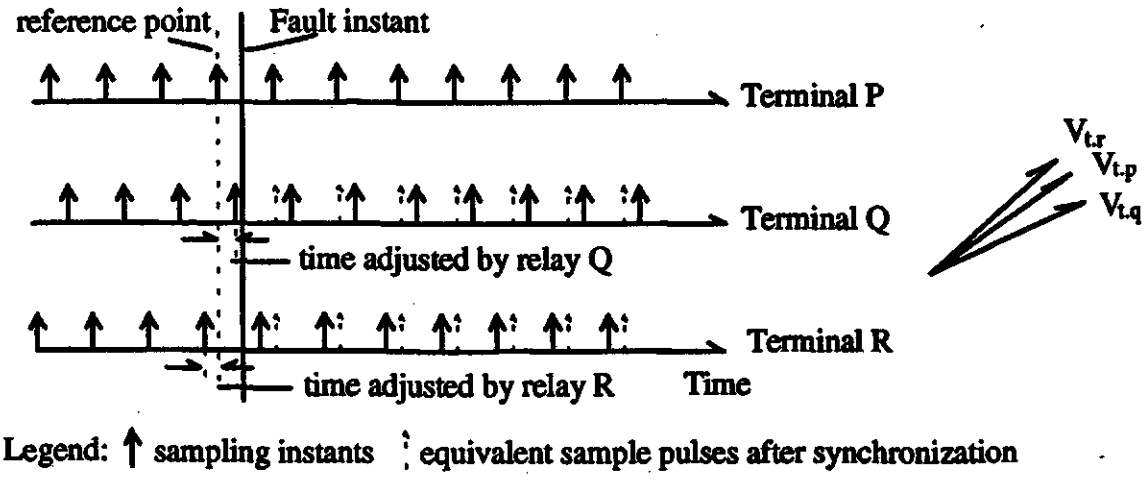

Figure 6.3. Synchronization procedure.

6.4. Summary

A protection system for teed transmission lines, based on the proposed differential algorithm is described in this chapter. The protection system is suitable for implementing in a microprocessor-based relay equipped with wideband communication channels. The transient detector technique and data synchronization method are developed in this chapter. The protection system, outlined in this chapter, was programmed and tested using digital simulations; the results are presented in the next chapter.

7. RELAY SIMULATION AND TESTS

The design of a protection system for implementing the proposed differential algorithm is presented in the previous chapter. The system was simulated using FORTRAN 77 for estimating its performance. Current and voltage waveforms of a test system were generated by using the simulation program, EMTDC [32]. The simulated system, its parameters and cases examined are summarized in this chapter. Results obtained from some of the tests are presented.

7.1. System Model

A single line diagram of the simulated power system is shown in Figure 7.1. Three systems, S_p, S_q and S_r, are represented by their equivalent Thevenin sources and are linked by two parallel teed lines, Circuit 1 and Circuit 2. The configuration of the transmission lines was changed by switching the circuit breakers at the line terminals. The lengths of the simulated transmission lines are shown in Figure 7.1. Other parameters of the simulated system are given in Appendix D. The prefault load flows were controlled by changing the phase angles of the source voltages.

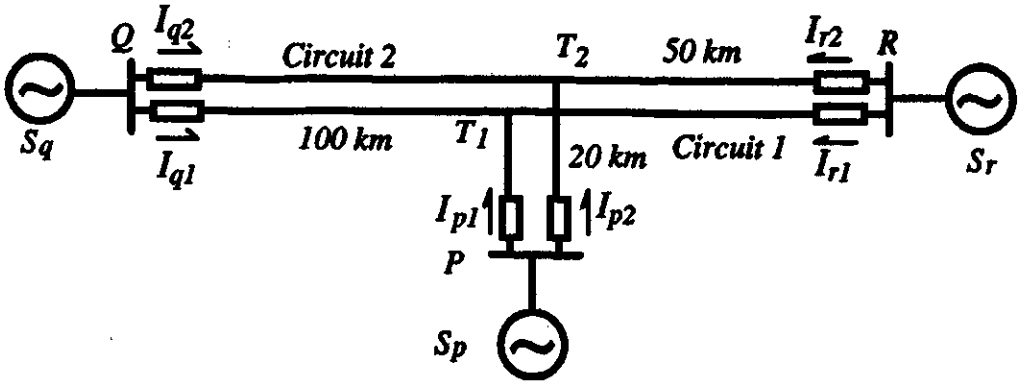

Figure 7.1. A single line diagram of the simulated system.

The lines were considered to be either 345 kV or 500 kV lines. To simulate the worst condition, the parallel lines were assumed to be configured such that there is considerable unbalance in currents during normal system operation.

7.2. Simulation Parameters

The EMTDC program was used to generate the waveforms of voltages and currents at the line terminals where protective relays were assumed to be installed. The time step chosen for the simulations was 16.667 μs, which allowed the signals to contain frequencies of up to 30 kHz.

The data representing the waveforms were preprocessed by a program which simulated 4th order Butterworth low pass filters designed with cut-off frequencies of 300 Hz. The transfer function of the filters can be expressed as

$$H(z) = \frac{a_4 Z^{-4} + a_3 Z^{-3} + a_2 Z^{-2} + a_1 Z^{-1} + a_0}{b_3 Z^{-3} + b_2 Z^{-2} + b_1 Z^{-1} + b_0}. \qquad (7.1)$$

where:

$(a_0, a_1, a_2, a_3, a_4)$ = (0.4e-3, 1.7e-3, 2.5e-3, 1.7e-3, 0.4e-3) and
(b_0, b_1, b_2, b_3) = (-3.1806, 3.8612, -2.1122, 0.4383).

A time delay of 1.3 ms was observed from viewing the input and output waveforms of the filter program, shown in Figure 7.2. The outputs of this program were resampled by the program that simulated the operation of the proposed relay.

It was observed that there are no significant differences in the performance of the proposed algorithm when applied to the 345 kV and 500 kV transmission systems. Results from the studies of the 345 kV system are presented in this chapter to facilitate discussions, and the results from the studies of the 500 kV system are included in Appendix E. Operating states and faults were selected with the objective of examining the influence of the unbalanced voltages and currents on the outputs of the relay algorithm. Based on preliminary studies, and assuming that cts of 1000:1 ratio are used at all terminals, the restraining coefficient (k in Equation 5.15) was set at 0.05, and the threshold (k_s in Equation 5.16) was set at 0.06 A. These settings ensured that the amplitude of the restraining currents remained 20% more than the largest spurious output of the differential current.

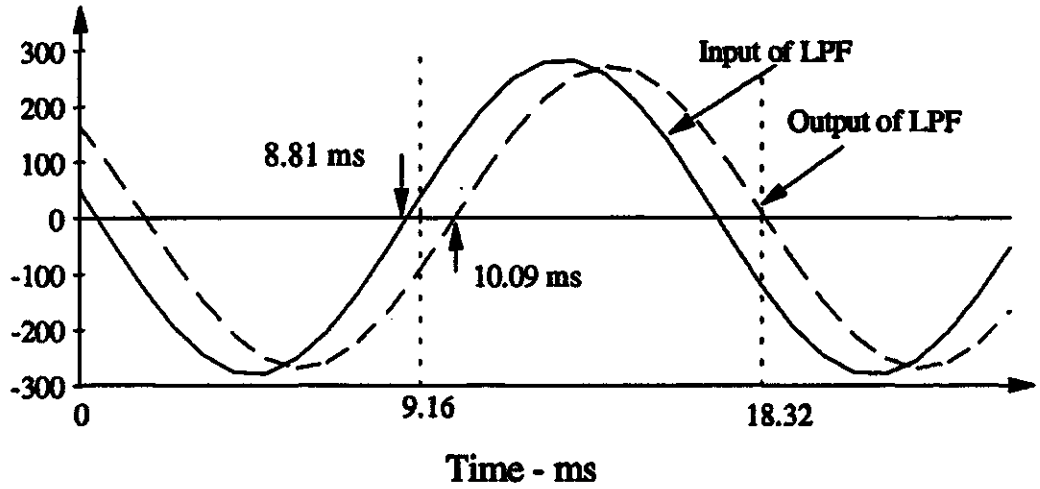

Figure 7.2. Signal delay of the anti-aliasing LPF.

7.3. Data Synchronization

The proposed data synchronization technique is discussed in the previous chapter. It was assumed that the three microprocessor-based relays, provided at the line terminals, sample voltages and currents at a selected frequency, but each relay generates its own train of sampling pulses. The sampling instants of the relays are usually different because they use independent clocks.

The proposed technique corrects the sampling difference by referring to the estimated voltage at the junction of the teed line as described before. To evaluate the effectiveness of the technique, a program was developed which simulated independent sampling at each terminal. The voltage phasors estimated at each terminal were compared with the sampling instant. Some typical results are listed in Tables 7.1 and 7.2.

Example in Table 7.1 lists the angles of the estimated phasors of the voltage at the tee junction calculated from samples taken by synchronized clocks. The results in the first part of Table 7.1 concern a model of a transposed transmission line, and the second part concerns a model of an un-transposed line. The results show that the differences in the angles of the voltage phasors calculated from the three terminals are small when the line is transposed. When the line is not transposed, the errors are somewhat lager but are not excessive.

Table 7.1. Compensated voltages calculated using synchronized sampling of signals.

Sampling instant -ms	Compensated voltages calculated from data sampled at					
	bus P		bus Q		bus R	
	phase angle	magni-tude -kV	phase angle	magni-tude -kV	phase angle	magni-tude -kV
Transposed line model						
78.26	86.44°	450.3	86.65°	449.5	86.56°	449.7
79.09	68.45°	450.4	68.65°	449.6	68.56°	449.8
79.92	50.46°	450.5	50.66°	449.7	50.58°	450.0
80.75	32.49°	450.6	32.68°	449.9	32.60°	450.1
81.58	14.52°	450.6	14.71°	450.0	14.63°	450.2
Untransposed line model						
78.26	86.54°	452.5	85.91°	444.3	86.26°	448.2
79.09	68.55°	452.6	67.91°	444.4	68.26°	448.3
79.92	50.57°	452.7	49.91°	444.6	50.27°	448.4
80.75	32.59°	452.8	31.93°	444.7	32.30°	448.5
81.58	14.63°	452.8	13.97°	444.9	14.33°	448.6

Table 7.2 lists the angles of the voltage phasors calculated from the data by separate clocks (not synchronized) at each terminal. The transmission line model used in this case was for an un-transposed line. The difference between the sampling instants t_q-t_r was kept the same as the difference between the sampling instants t_p-t_q.

Based on the fundamental frequency of the power system, the difference in sampling time Δt, can be interpreted as the difference in the phase angles. For example, $\Delta t = 83.3$ μs is equivalent to an angle of 1.8° of a 60 Hz phasor. The results presented in Table 7.2 show that the differences in the angles in the estimated voltage phasors are small. For the un-transposed line, the maximum difference in the calculated phase angles is less than 1°; this is equivalent to a synchronization error of 46 μs. This level of error is tolerable for the proposed differential algorithm and can be offset by selecting a suitable setting of the restraining coefficient.

Table 7.2. Samples of results for estimated voltage phasors vs. different sampling clocks.

Sampling instant -ms	Compensated voltages calculated from data sampled at					
	bus P		bus Q		bus R	
	phase angle	magni-tude -kV	phase angle	magni-tude -kV	phase angle	magni-tude -kV
Difference in sampling instants = 83 μs (Δθ =1.8°)						
78.26	86.54°	452.5	87.71°	444.3	89.86°	448.1
79.09	68.55°	452.6	69.71°	444.4	71.86°	448.2
79.92	50.57°	452.7	51.71°	444.6	53.87°	448.4
80.75	32.59°	452.8	33.73°	444.7	35.89°	448.5
81.58	14.63°	452.8	15.76°	444.9	17.92°	448.6
Difference in sampling instants = 166 μs (Δθ =3.6°)						
78.26	86.54°	452.5	89.51°	444.3	94.46°	448.1
79.09	68.55°	452.6	71.51°	444.4	75.46°	448.2
79.92	50.57°	452.7	53.51°	444.5	57.47°	448.3
80.75	32.59°	452.8	35.53°	444.7	39.49°	448.5
81.58	14.63°	452.8	17.56°	444.9	21.52°	448.6
Difference in sampling instants = 416 μs (Δθ =9°)						
78.26	86.54°	452.5	94.91°	444.3	104.26°	448.2
79.09	68.55°	452.6	76.91°	444.4	86.26°	448.2
79.92	50.57°	452.7	58.91°	444.5	68.26°	448.3
80.75	32.59°	452.8	40.92°	444.7	50.27°	448.4
81.58	14.63°	452.8	22.95°	444.8	32.30°	448.5
Difference in sampling instants = 833 μs (Δθ =18°)						
78.26	86.54°	452.5	-76.09°	444.3	-57.74°	448.2
79.09	68.55°	452.6	85.91°	444.3	-75.74°	448.2
79.92	50.57°	452.7	67.91°	444.4	86.26°	448.2
80.75	32.59°	452.8	49.91°	444.6	68.26°	448.3
81.58	14.63°	452.8	31.93°	444.7	50.27°	448.4

7.4. Fault Detection Technique

The selected fault detection technique is used to start the proposed differential algorithm. The sensitivity of the fault detection technique was tested by a program incorporated in the differential algorithm.

A logic diagram for implementing the selected fault detector technique is drawn in Figure 7.3. The changes in the instantaneous values of the voltage and current are calculated, their absolute values are added and compared with a threshold T_{her}. This output is latched until the relay is reset.

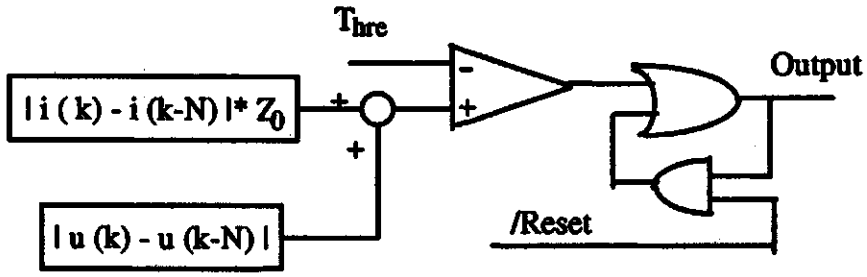

Figure 7.3. Logic diagram of the fault detector criterion.

Extensive tests showed that this technique detects the onset of faults at the first or second sampling instant after its inception. Typical results showing the operation of the fault detector during a phase a-to-g fault with a 800Ω fault resistance are presented in Figure 7.4. The effect of the point-on-wave was examined by starting faults with different initial angles in terms of the voltage of phase a at the tee junction.

7.5. Operating Speed

The differential algorithm starts executing at the master relay only when data from other terminals have been received. The total relay operating time should, therefore, include

(1) time required to obtain minimum data to reach a trip decision;

(2) transfer delay of selected channels and

(3) time required to execute the program.

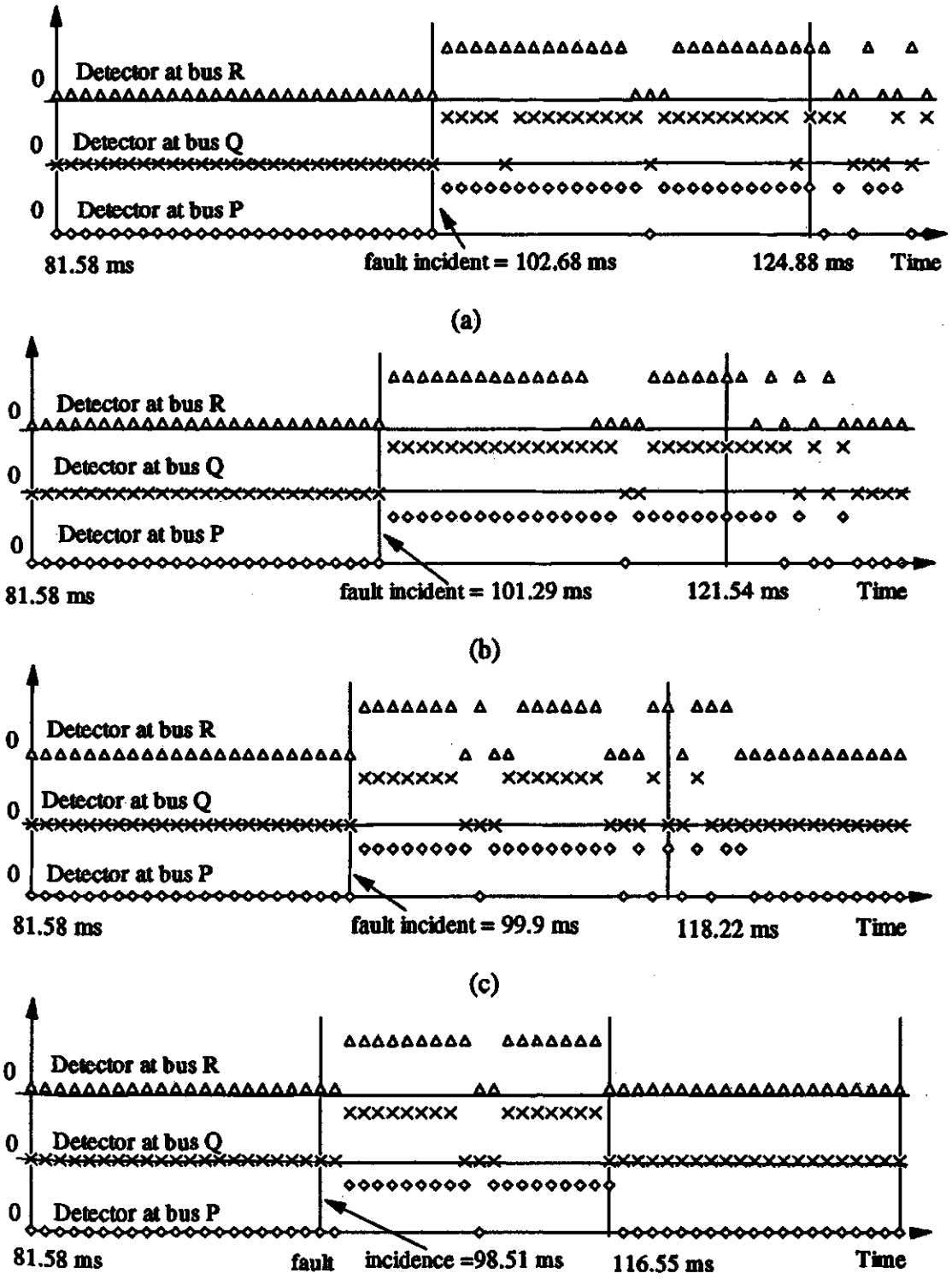

Figure 7.4. Operation of the fault detector for a phase a-to-g fault with R_f=800 Ω.
(a) fault incidence angle $\theta_0 = 90°$; (b) fault incidence angle$\theta_0 = 60°$;
(c) fault incidence angle $\theta_0 = 30°$; (d) fault incidence angle $\theta_0 = 0°$.

Because channel delay and execution times depend on selected facilities, the operating time discussed in this section only includes the time required to obtain minimum data, which is measured by the number of samples of data after the inception of a fault.

7.5.1. Operating Times vs. Fault Locations

The results, shown in Table 7.3, were obtained from tests simulating phase a to ground and phase b to phase c faults on the line at locations shown in Figure 7.5. In the prefault operating state, the voltage of the source S_p led the voltages of sources S_r and S_q by 35° and 30° respectively. The restraining currents were relatively larger in these cases compared to the restraining currents when the system was transmitting light load. Fault resistance of 0.2Ω was used (this is required by the EMTDC program). The operating time was measured from the time of the inception of the fault to the instant when the relay issued a trip command. The results show that there are no significant differences in the operating speed for faults at different locations.

Table 7.3. Impact of the fault location on the operating time of the relay.

Fault location	Relay operating time for	
	a-g faults (ms)	b-c faults (ms)
L_1	3.3	3.3
L_2	3.3	3.3
L_3	4.2	4.2
L_4	4.2	4.2
L_5	4.2	4.2
L_6	4.2	4.2
L_7	4.2	4.2
L_8	4.2	4.2
L_9	3.3	3.3

7.5.2. Operating Times vs. Point-on-Wave of Faults

To examine the influence of the point-on-wave incidence of fault on the operating speed of the algorithm, phase a-to-g and phase b-to-phase c faults at the junction point

were simulated. The switching times were controlled to specific phase angles of voltage phasor at the tee junction. The results are listed in Table 7.4.

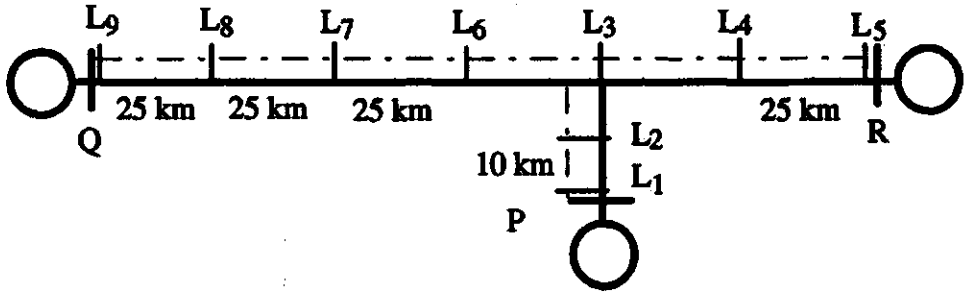

Figure 7.5. Location of faults used in the simulations.

Table 7.4. Impact of the point-on-wave inception of fault on the operating time of the relay.

Fault incidence angle of $V_{t\,a}$	Algorithm time for	
	a-g faults (ms)	b-c faults (ms)
30°	4.2	3.3
60°	3.3	4.2
90°	3.3	4.2
120°	3.3	4.2
150°	4.2	4.2
180°	4.2	3.3
210°	4.2	3.3

The results show that there were no significant differences between the operating times of the algorithm and the instant of fault inception. This can be partly attributed to the use of terminal voltages in calculating the compensated currents. Although the waveforms of currents and voltages are affected by the fault incident angle, their impacts are partly counterbalanced as is discussed in the section on fault detector.

7.5.3. Operating Times vs. Arc Resistance.

Ground faults were simulated to investigate the influence of arc resistance on the operating speed of the proposed algorithm. These studies were conducted by simulating

a phase a-to-g fault at the junction of the PTTL with fault resistances ranging from 10Ω to 800Ω. The results are shown in Figure 7.6.

These results show that the amplitude of the differential current decreases as the fault resistance increases. The operating speed is dictated by the amplitude of the differential current becoming larger than the restraining current. Assuming that the restraining current does not change as the arc resistance increases, the operating speed is expected to decrease as the fault resistance increases.

It can also be concluded from Figure 7.6 that, in order to enhance the sensitivity of the relay and to detect high resistance faults, the restraining current should be as small as possible.

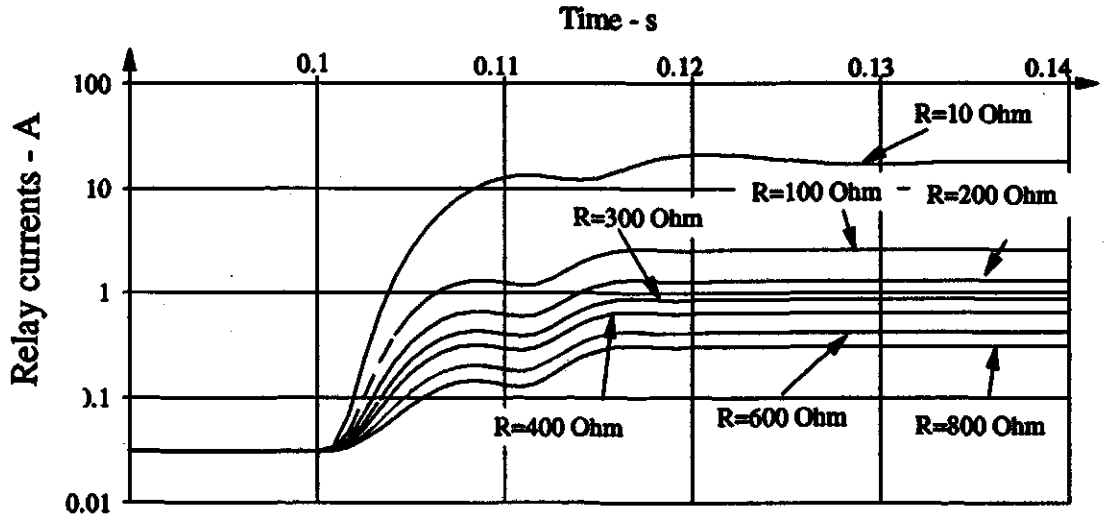

Figure 7.6. The influence of fault resistance on the operating current of the differential relay.

7.6. Transmission System Fault Studies

The performance of the proposed differential algorithm was also examined by applying it to a number of fault cases. Figure 7.7 shows the selected fault locations. The faults were initiated at t=0.1 s after the simulation was started unless otherwise stated in the presentation. For convenience, a 1200 Hz sampling frequency was selected. This corresponds to approximately 833 μs between consecutive samples. Only typical results are shown in this chapter, some additional results are included in Appendix E.

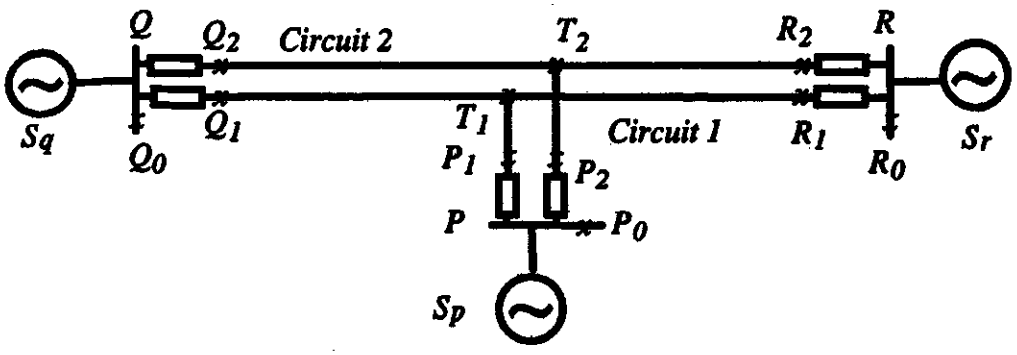

Figure 7.7. The locations selected for fault case studies.

7.6.1 Internal Faults

The proposed differential algorithm was examined by using it to detect internal faults. Table 7.5 lists the types and locations of the faults simulated for the studies. The PTTL was configured as shown in Figure 7.7, all switches were closed. Results from internal faults with special characteristics, such as cross-circuit faults, faults with outflow and faults with arc resistance, are presented later in this chapter. To simulate large current flows in the transmission circuits before the fault, the power angle differences between the voltages of S_p and S_q and between the voltages of S_p and S_r were set at 30° and 35° respectively. The operating current, I_{op}, and restraining current, I_{res}, in the relays protecting Circuits 1 and 2 were observed.

Results obtained from a phase b-to-phase c-to-g fault at T_1 are shown in Figures 7.8 to 7.11. The waveforms of the line currents in Circuit 1, shown in Figure 7.8, display a typical phenomena of phase b-to-phase c fault. The mutual coupling between the two parallel circuits and the traveling waves cause the high frequency currents in Circuit 2, as is shown in Figure 7.9.

The relay operating and restraining currents in the relays protecting the two circuits are shown in Figures 7.10 and 7.11. The results show that the algorithm correctly identified the faulted phases approximately 4 ms after the inception of the fault. The results also show that the operating currents in the phase a of Circuit 1 and all the three phases in Circuit 2 are less than the restraining currents during the fault.

Table 7.5. List of internal faults studies and their locations.

Location	Fault type
P_1	phase a-to-g
P_1	phase b-to-phase c
P_1	3-phases
Q_1	phase a-to-phase b-to-g
Q_1	phase b-to-g
Q_1	3-phases
T_1	phase a-to-g
T_1	phase b-to-phase c-to-g
T_1	3-phases
R_1	phase a-to-phase b-to-g
R_1	phase b-to-phase c
R_1	3-phases

7.6.2. Cross-circuit and Simultaneous Faults

Seven cross-circuit faults on the lines were simulated; the type and location of each fault are listed in Table 7.6. The purpose of these studies was to examine the ability of the proposed algorithm to correctly identify these difficult situations. The prefault load flow conditions were the same as were used for the internal faults reported in the previous section.

Results of the case in which phases a and b of Circuit 1 and phase c of Circuit 2 were short circuited near bus R are presented in Figures 7.12 to 7.15. The waveforms of line currents in both circuits, shown in Figures 7.12 and 7.13, are similar to the waveforms observed in the cases of 3-phase faults. Conventional protection systems, such as distance relays, will trip all three phases of both circuits and, thus, disrupt the transmission of power between the systems. The relay operating currents are shown in Figures 7.14 and 7.15. These figures show that the proposed algorithm correctly identified the circuits and the phases which were experiencing the fault.

Table 7.6. List of cross-circuit and simultaneous faults.

Location	Fault at Circuit 1	Fault at Circuit 2
R_1 / R_2	phase a-to-g	phase b-to-g
R_1 / R_2	phase a-to-phase b	phase c
R_1 / R_2	phase a-to-phase b	phase b-to-phase c
R_1 / R_2	phase c	phase b
T_1 / T_2	phase a-to-g	phase b-to-g
T_1 / T_2	phase b	phase c
T_1 / T_2	phase a-to-phase b-g	phase c-to-g

7.6.3. External Faults

Studies were also conducted to examine the performance of the algorithm during external faults listed in Table 7.7. In these cases, the systems were lightly loaded and the voltage of the source S_p led the voltage of sources S_q and S_r by 5° and 10° respectively. The restraining currents, which were proportional to the sum of the amplitudes of the line currents at the junction, were small; this indicates that the relay was vulnerable to external interference in these cases.

Table 7.7. List of external faults.

Location	Fault type
R_0	3-phases fault
R_0	phase b-to-phase c-to-g
P_0	3-phases fault
P_0	phase b-to-phase c-to-g
P_0	phase a-to-g
Q_0	3-phases fault
Q_0	phase b-to-phase c-to-g

Waveforms obtained from a phase b-to phase-c-to-g fault at Q_0 are shown in Figures 7.16 to 7.19. The waveforms of currents in the two circuits, shown in Figures 7.16 and 7.17, are identical because the currents were equally distributed in the two circuits. The

response of the algorithm to this fault is shown in Figures 7.18 and 7.19; no trip command was generated.

7.6.4. Faults that cause Outflow of Current

The conditions that cause outflow problems are discussed in Chapter 4. Cases of this type were simulated on a PTTL, shown in Figure 7.7, except that Circuit 2 was disconnected from bus P. Cases listed in Table 7.8 were simulated. The sources connected to the P, Q and R terminals were of 20, 5 and 1 GVA capacity; the source connected to terminal R is comparatively "weak".

Table 7.8. List of studies in which currents outflow at one terminal.

Location	Fault type
Q_1	3-phases fault
Q_1	phase b-to-phase c-to-g
Q_1	Phase a-to-g

Results shown in Figures 7.20 to 7.23 are for a 3-phases fault at Q_1. The currents, shown in Figures 7.20 and 7.21, clearly indicate the outflow of currents at bus R; they are 180° apart. The operating and restraining currents of the relaying systems are shown in Figures 7.22 and 7.23. These figures show that the proposed algorithm correctly identified the fault on Circuit 1. Figure 7.23 shows that the relaying system of Circuit 2 was restrained which is the desired response; there was no fault on Circuit 2.

7.6.5. High Resistance Faults

Faults were also simulated with high resistance between the faulted phases and between a phase to ground. A heavy load flow condition was simulated by setting the power angle of S_p 35° and 40° ahead of the power angles of S_q and S_r. A list of the simulation studies is given in Table 7.9.

Table 7.9. List of studies of faults with high resistance.

Locations	Fault resistance	Fault types
P_1	600 Ω	phase a-to-g
Q_1	2x200 Ω/400 Ω *	phase b-to-phase c-to-g
R_1	400 Ω	phase b-to-g
T_1	600 Ω	phase a-to-g
T_1	600 Ω	phase a-to-phase b-to-g

* fault resistance between phase to phase was 2x200 Ω and the ground resistance was 400 Ω.

Presented in Figure 7.24 to 7.27 are the results of a phase a-to-ground fault at T_1 with 600Ω fault resistance, which the conventional relaying techniques can not easily detect such faults. Figures 7.24 and 7.25 depict that the change in the currents were minimal. This is because the prefault load currents were large. The responses of the proposed algorithm are shown in Figures 7.26 and 7.27. The proposed algorithm recognized the fault four samples after its inception.. The algorithm processing the data from the two healthy phases, b and c, remained stable as the restraining currents remained in excess of the operating currents.

7.7 Summary

In this chapter, results from simulations are reported. A PTTL was simulated using EMTDC and the relaying algorithm was simulated by programs written in FORTRAN 77. The simulation of the relaying algorithm included the synchronization technique and the fault detectors. Faults on the PTTL were simulated and performance of the algorithm examined. Results show that the proposed algorithm works well; it detects faults in one quarter cycle of the nominal frequency and is quite stable.

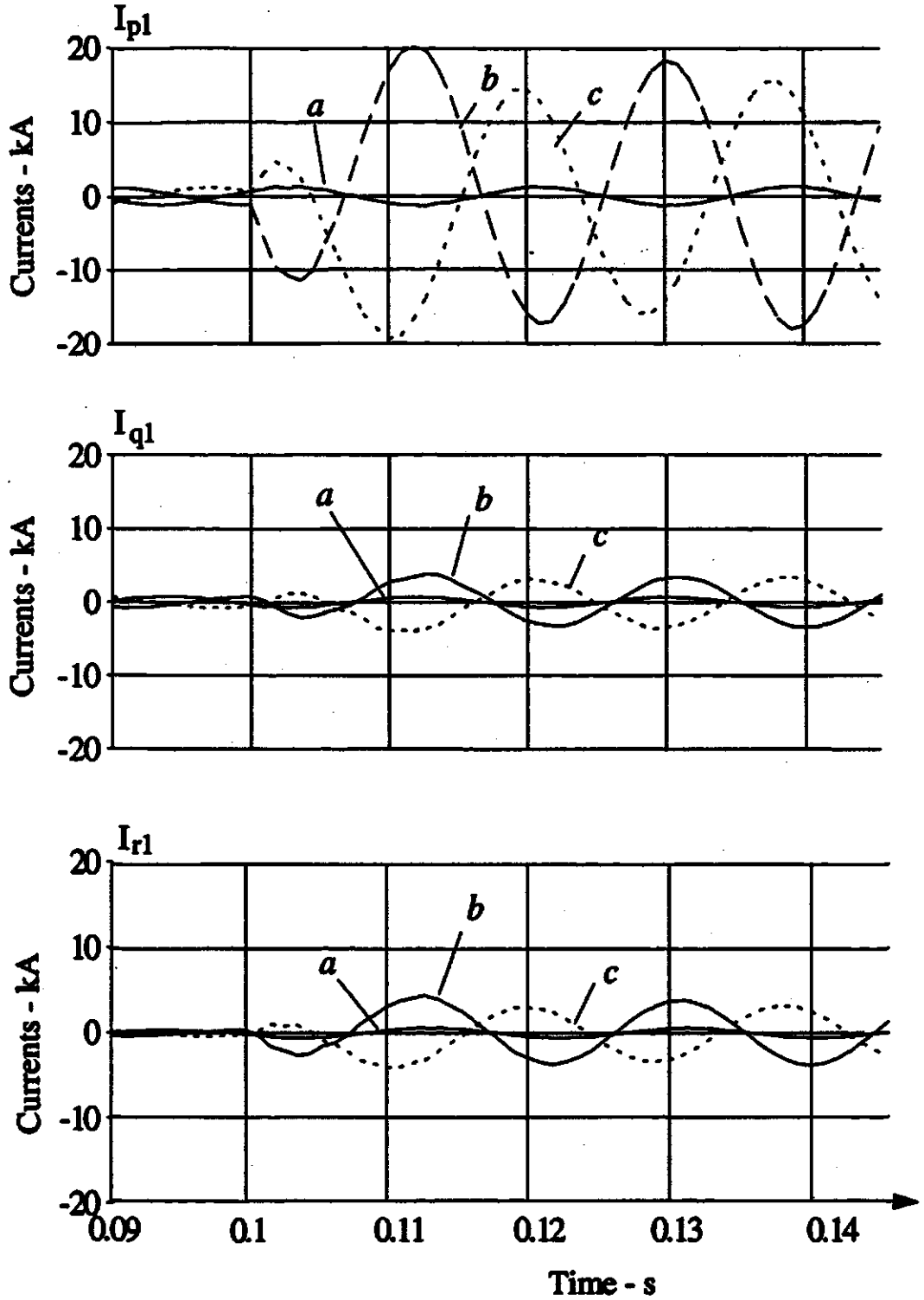

Figure 7.8. Waveforms of currents in Circuit 1 for a phase b-to-phase c-to-g fault at T_1.

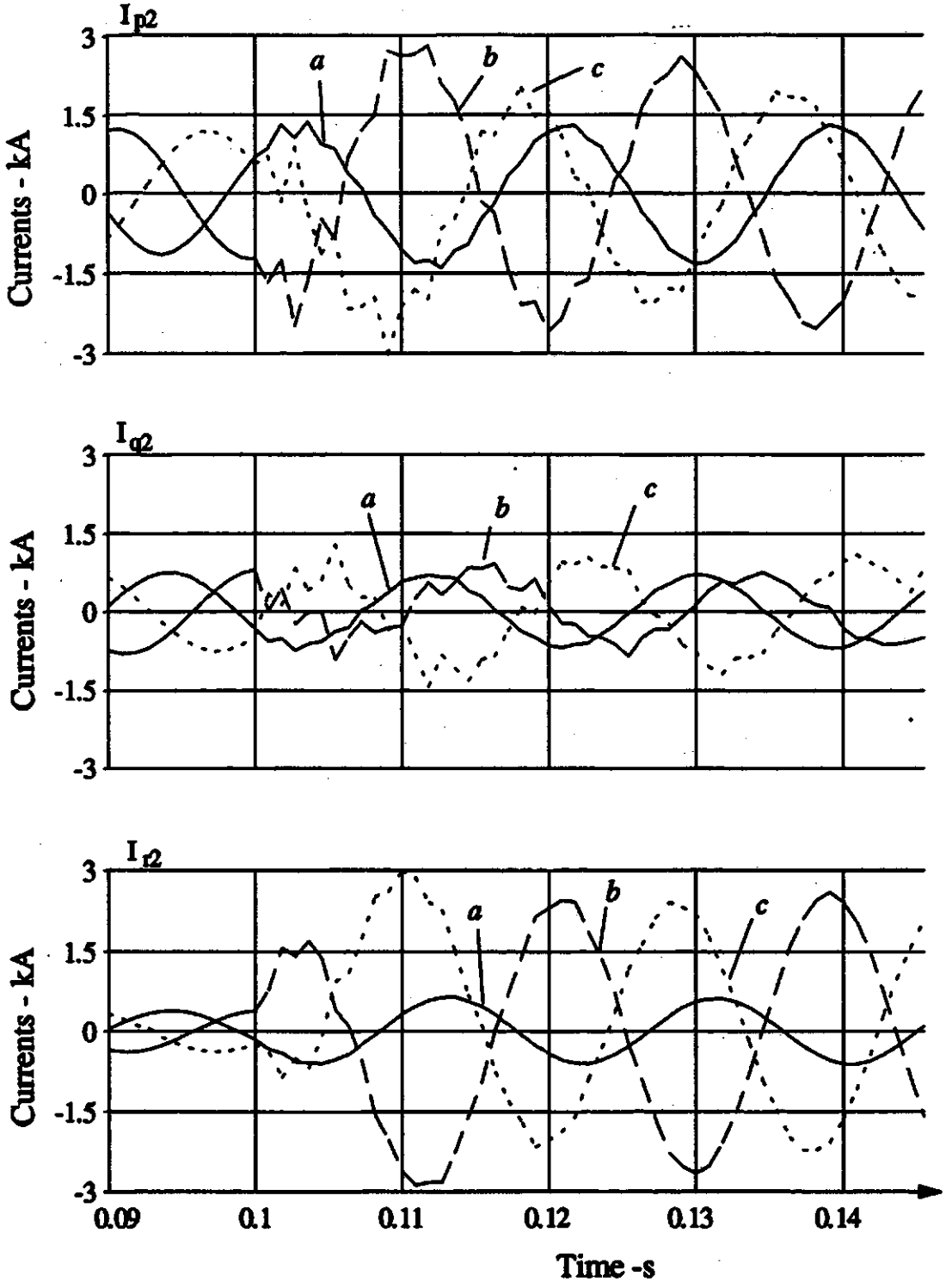

Figure 7.9. Waveforms of currents in Circuit 2 for a phase b-to-phase c-to-g fault at T_1.

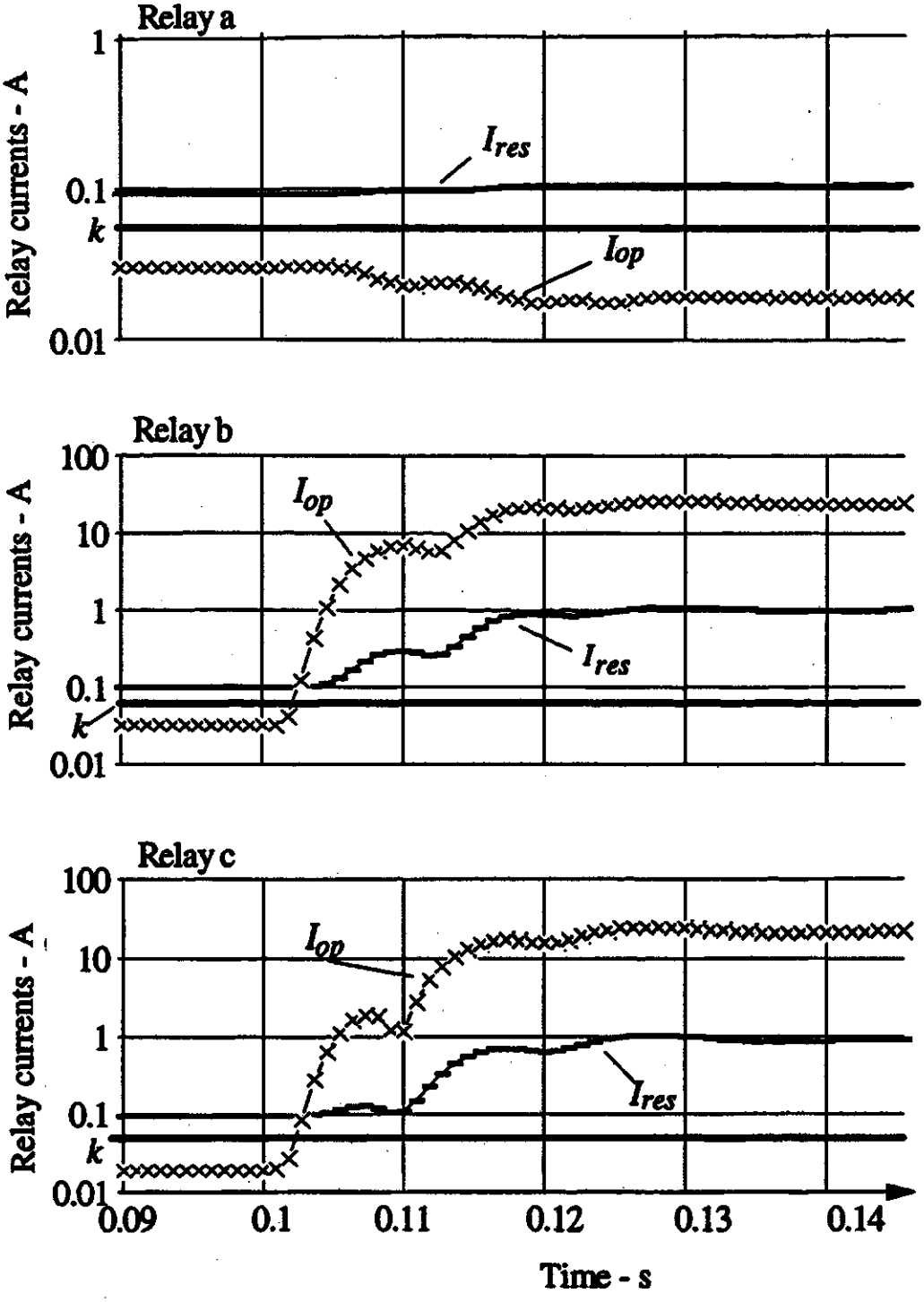

Figure 7.10. Operating and restraining currents in the master relay of Circuit 1 for a phase *b*-to-g fault at T_1.
I_{op} - Operating current,
I_{res} - Restraining current.

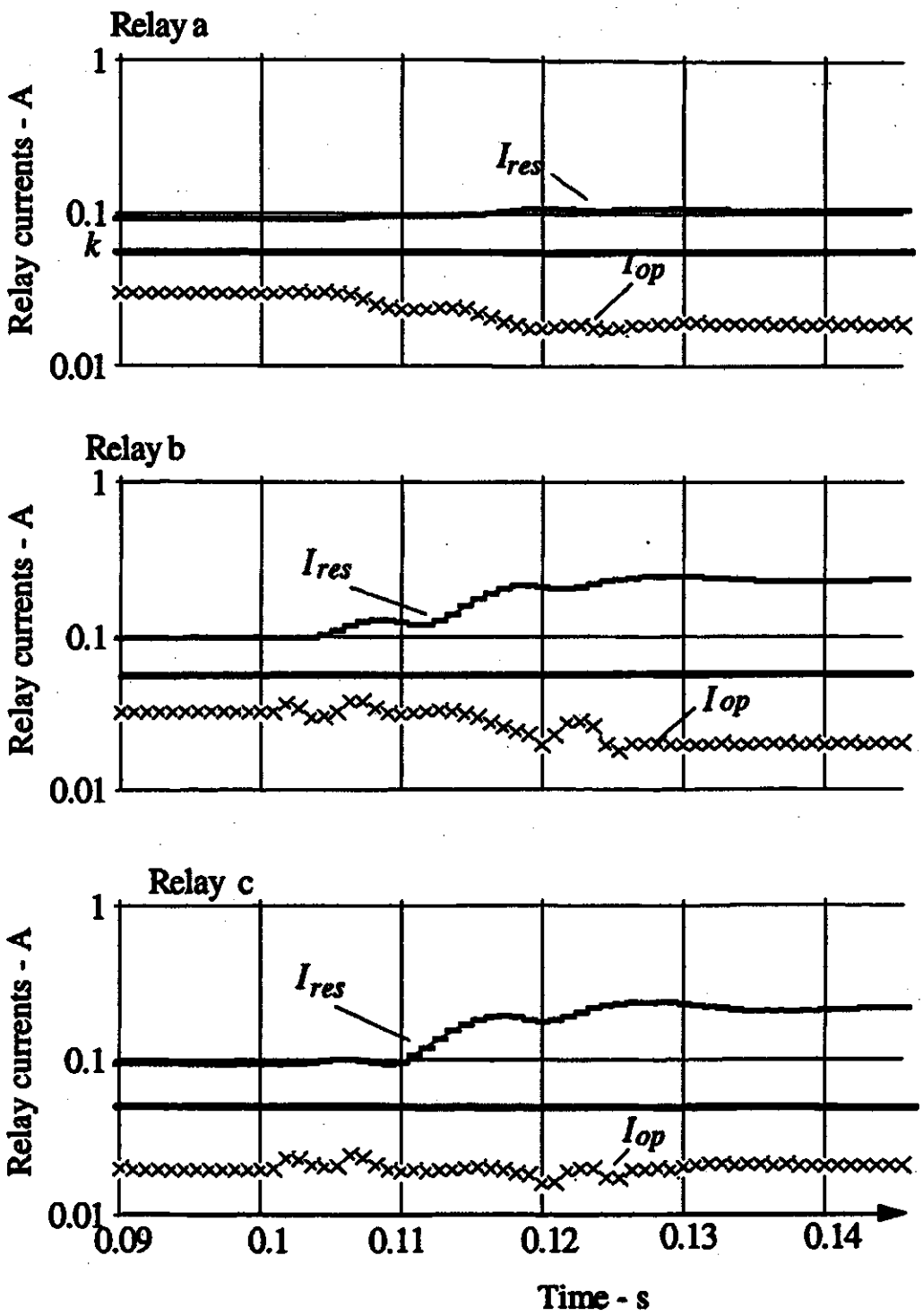

Figure 7.11. Operating and restraining currents in the master relay of Circuit 2 for a phase *b*-to-g fault at T_1.
I_{op} - Operating current,
I_{res} - Restraining current.

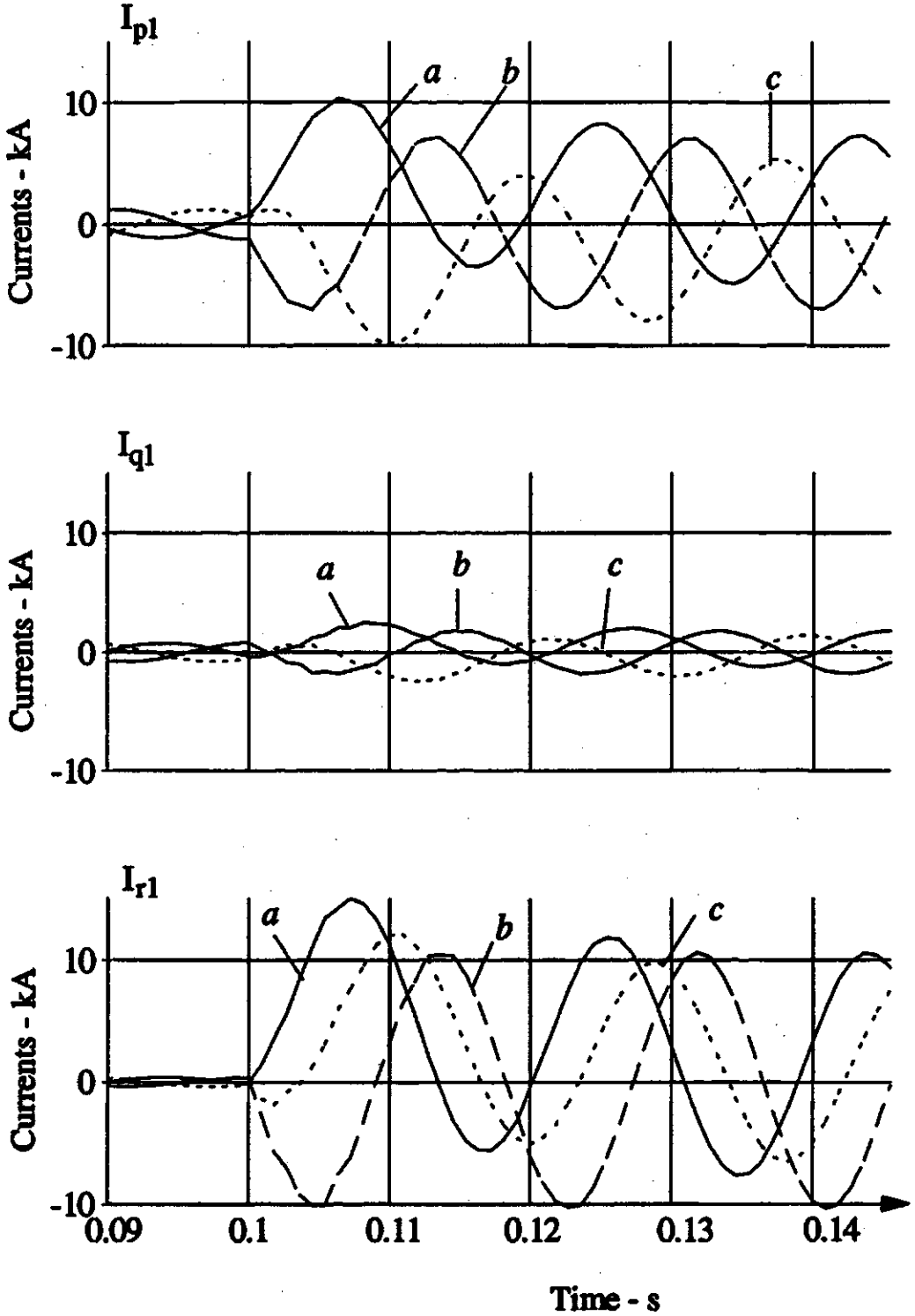

Figure 7.12. Waveforms of currents in Circuit 1 for a cross-circuit fault at R_1/R_2.

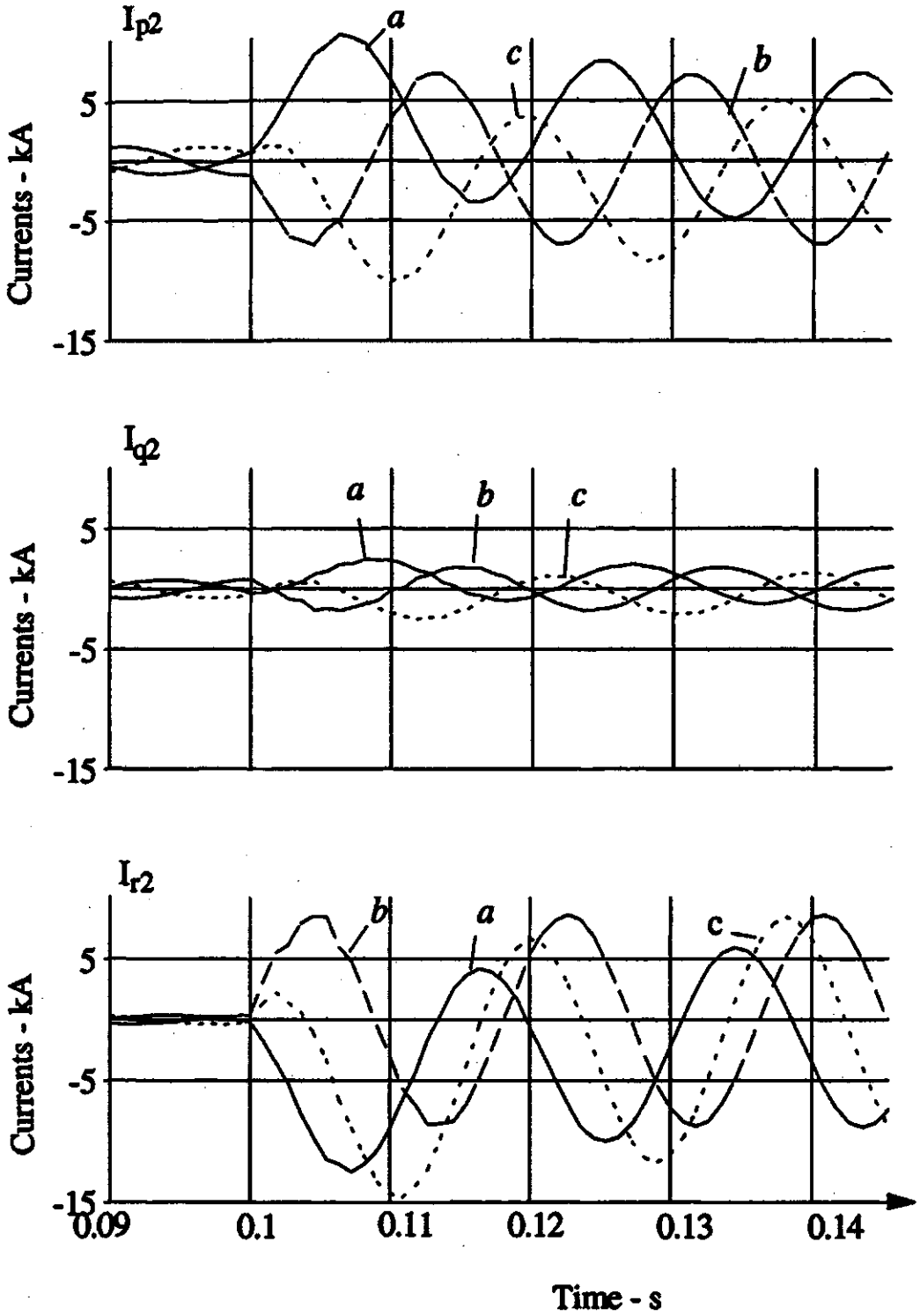

Figure 7.13. Waveforms of currents in Circuit 2 for a cross-circuit fault at R_1/R_2.

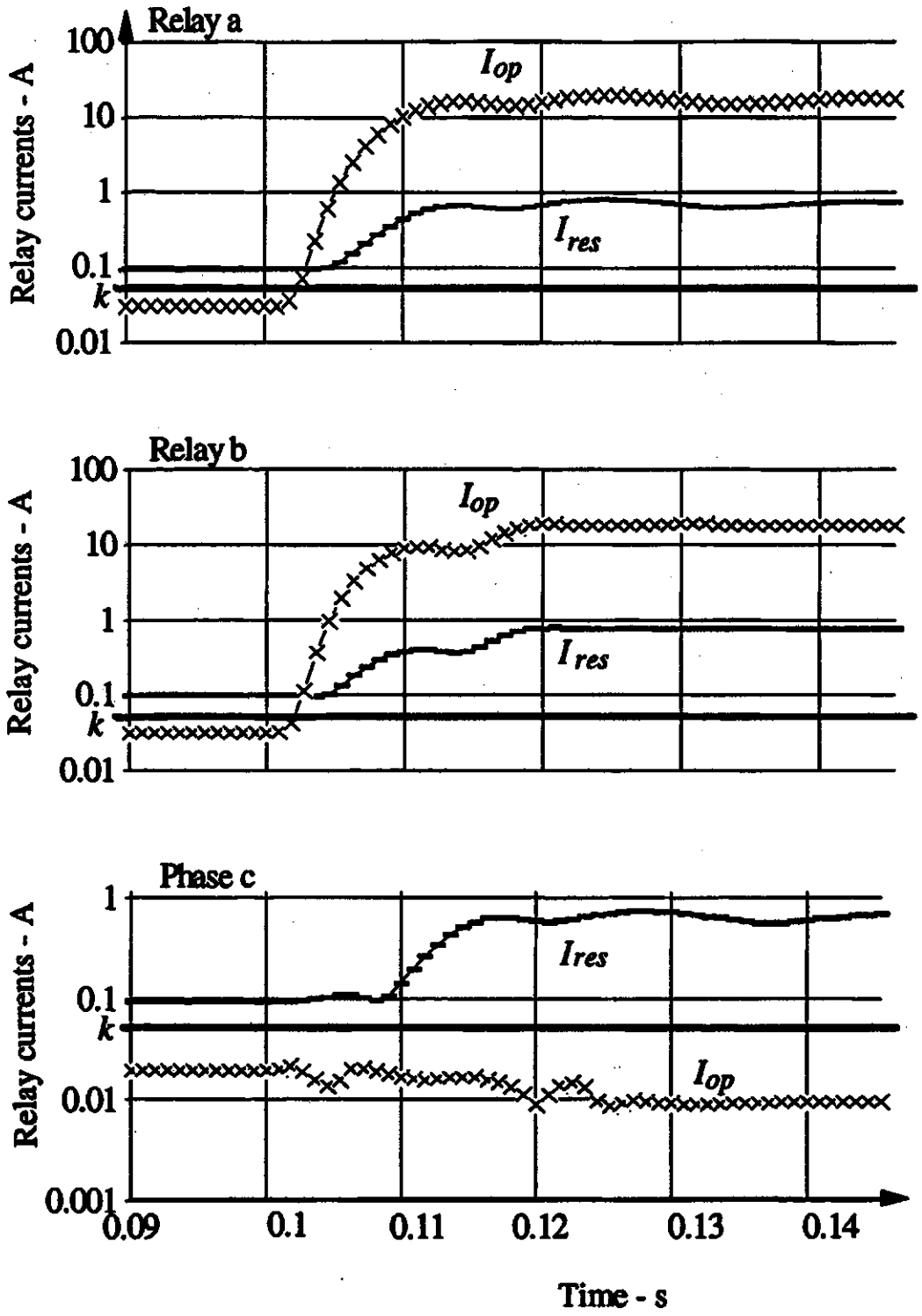

Figure 7.14. Operating and restraining currents in the master relay of Circuit 1 for a cross *circuit* fault at R_1/R_2.
I_{op} - Operating current,
I_{res} - Restraining current

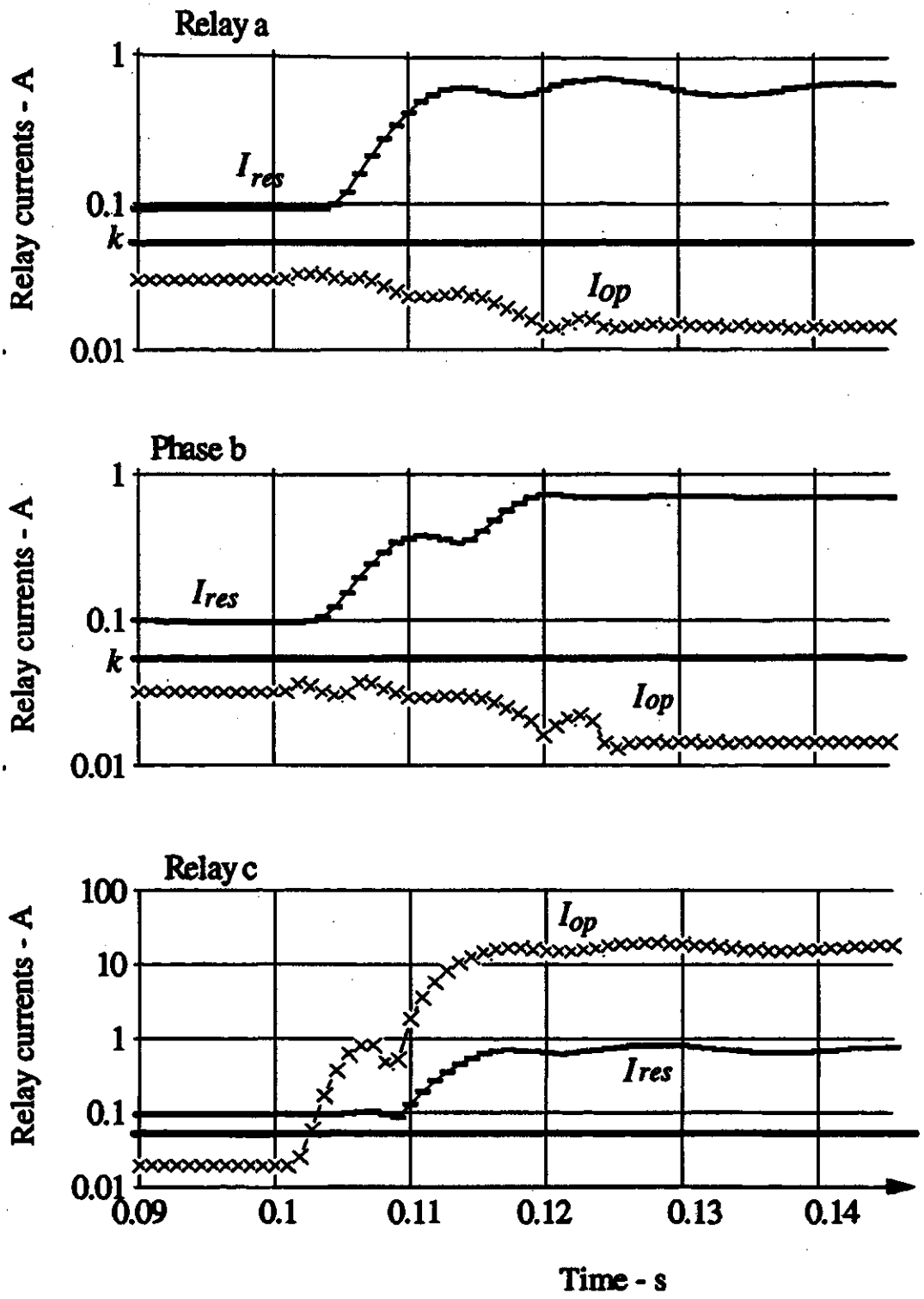

Figure 7.15. Operating and restraining currents in the master relay of Circuit 2 for a cross-circuit fault at R_1/R_2.
I_{op} - Operating current,
I_{res} - Restraining current

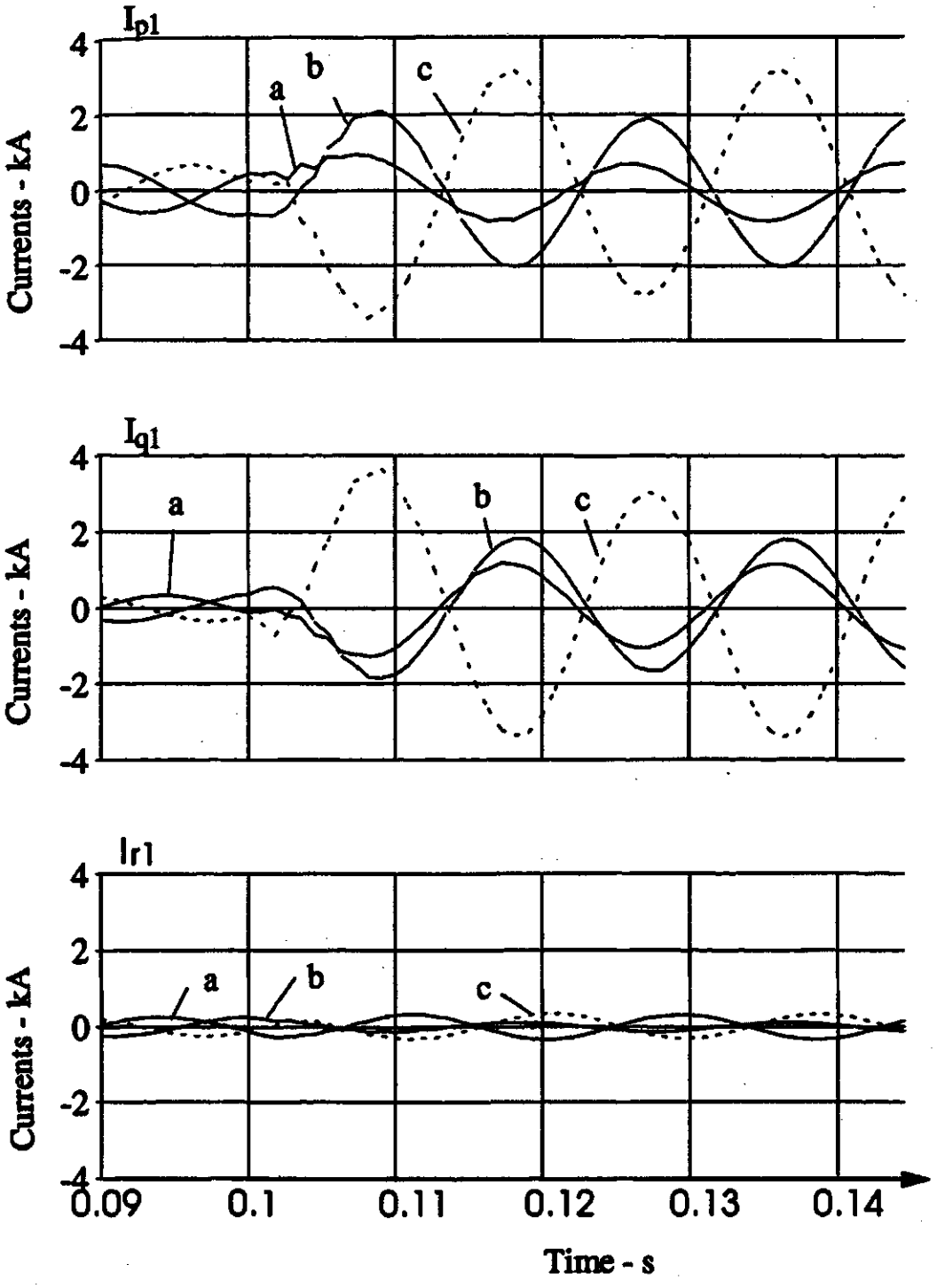

Figure 7.16. Waveforms of currents in Circuit 1 for a phase b-to-phase c-to-g fault at Q_0.

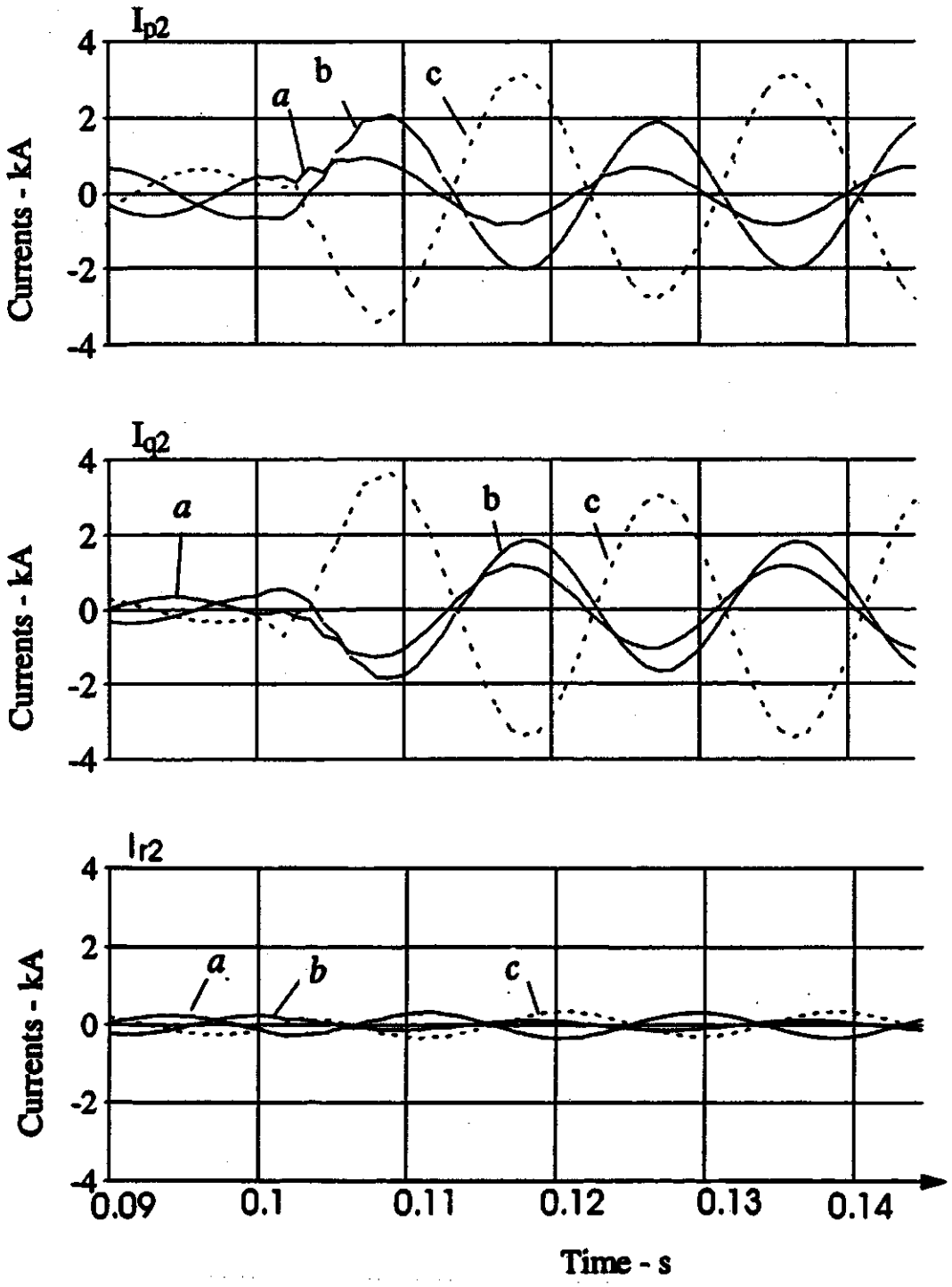

Figure 7.17. Waveforms of currents in Circuit 2 for a phase b-to-phase c-to-g fault at Q_0.

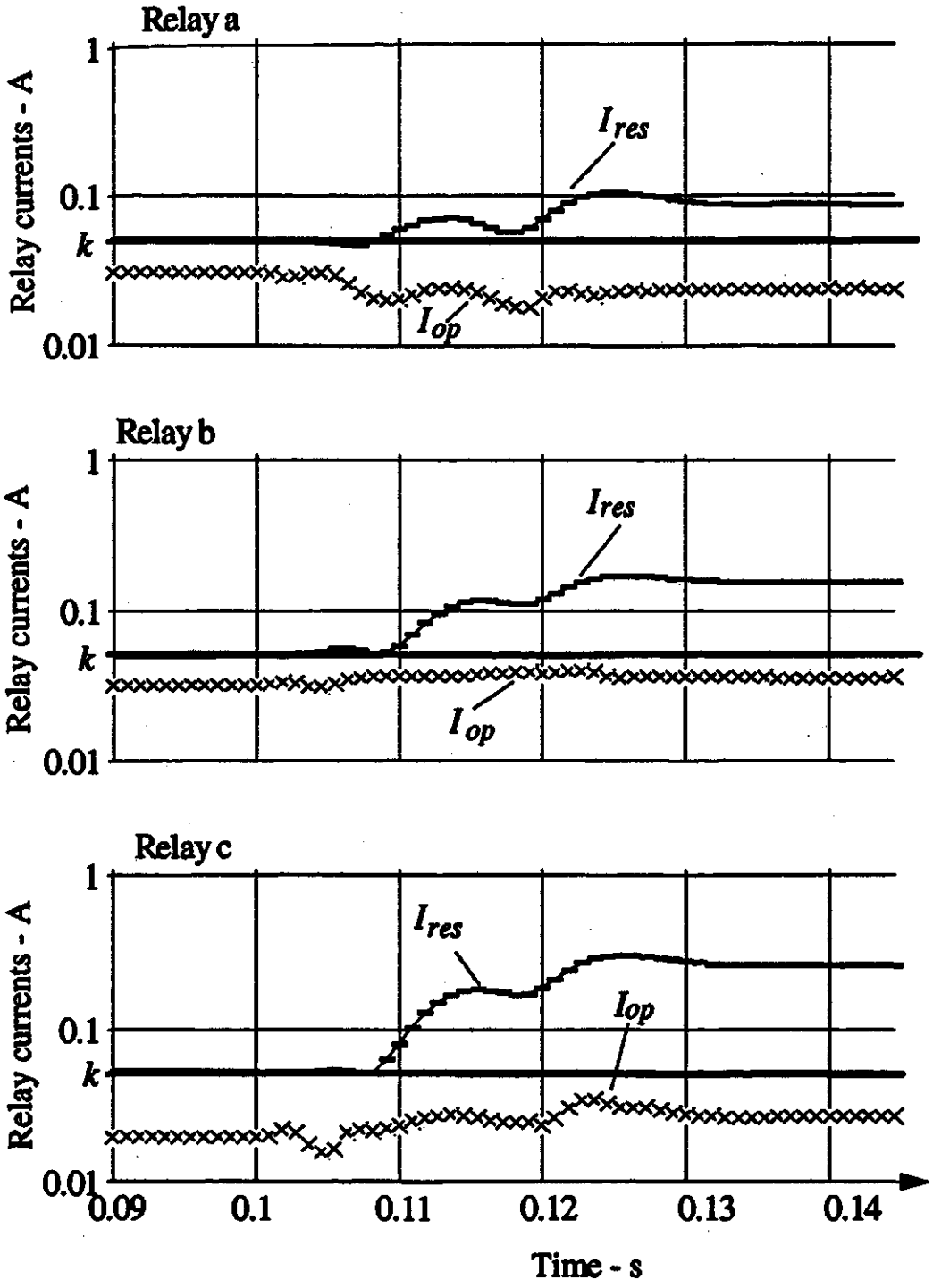

Figure 7.18. Operating and restraining currents in the master relay of Circuit 1 for a phase *b*-to-phase c-to-g fault at Q_0.
I_{op} - Operating current,
I_{res} - Restraining current.

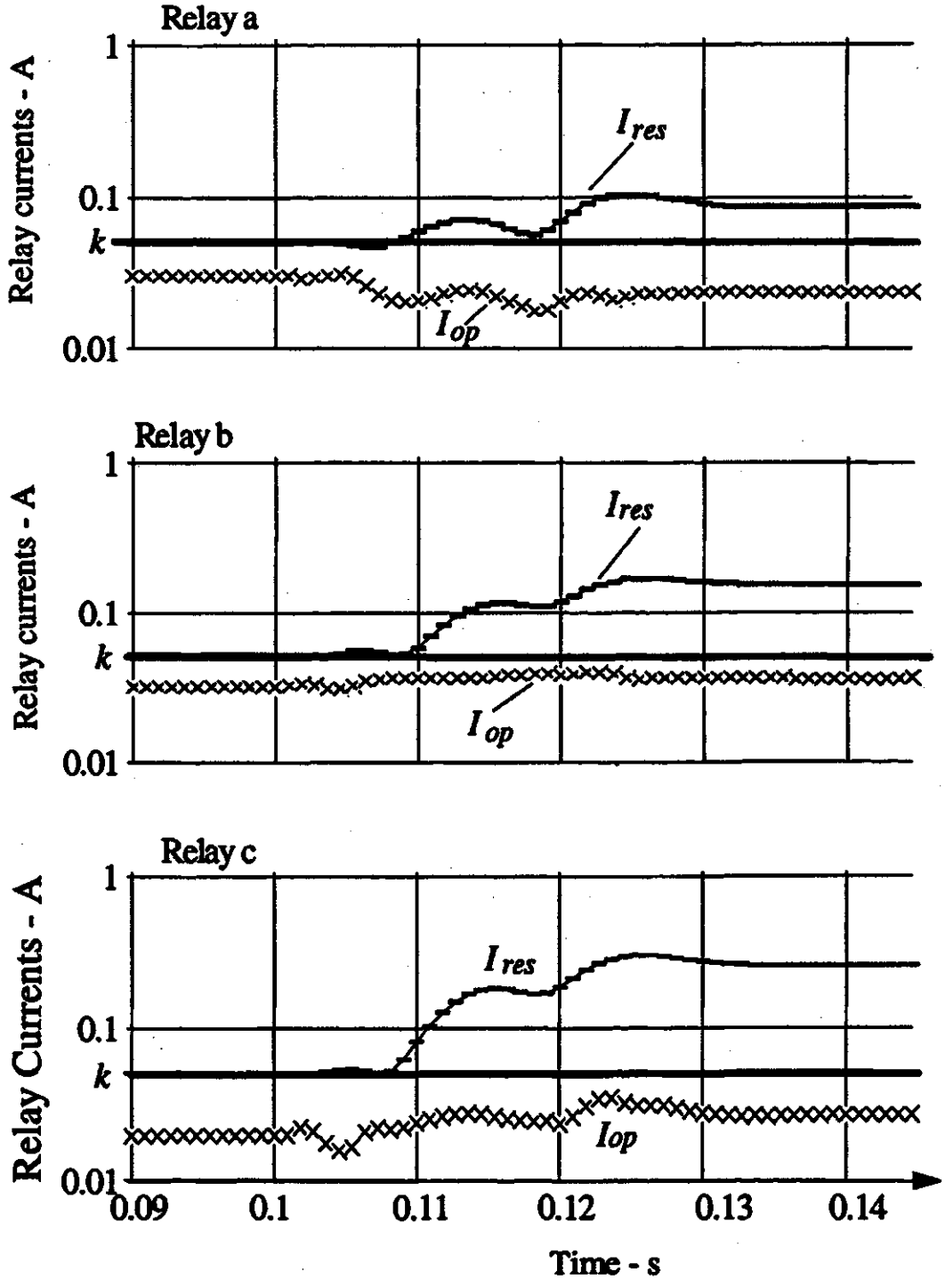

Figure 7.19. Operating and restraining currents in the master relay of Circuit 2 for a phase *b*-to-phase c-to-g fault at Q_0.
I_{op} - Operating current,
I_{res} - Restraining current.

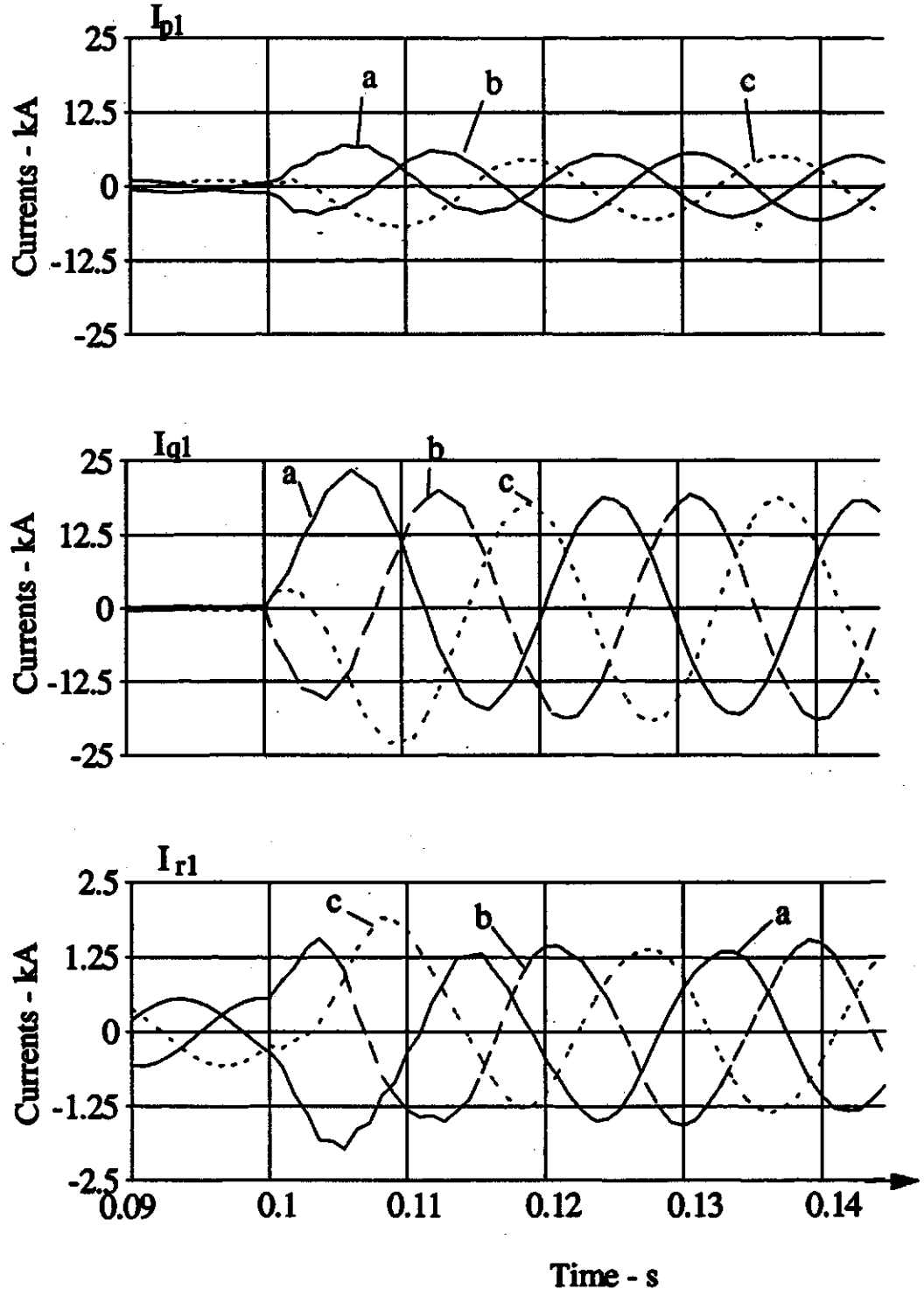

Figure 7.20. Waveforms of currents in Circuit 1 for a 3-phase fault at T_1 with currents outflow at terminal R.

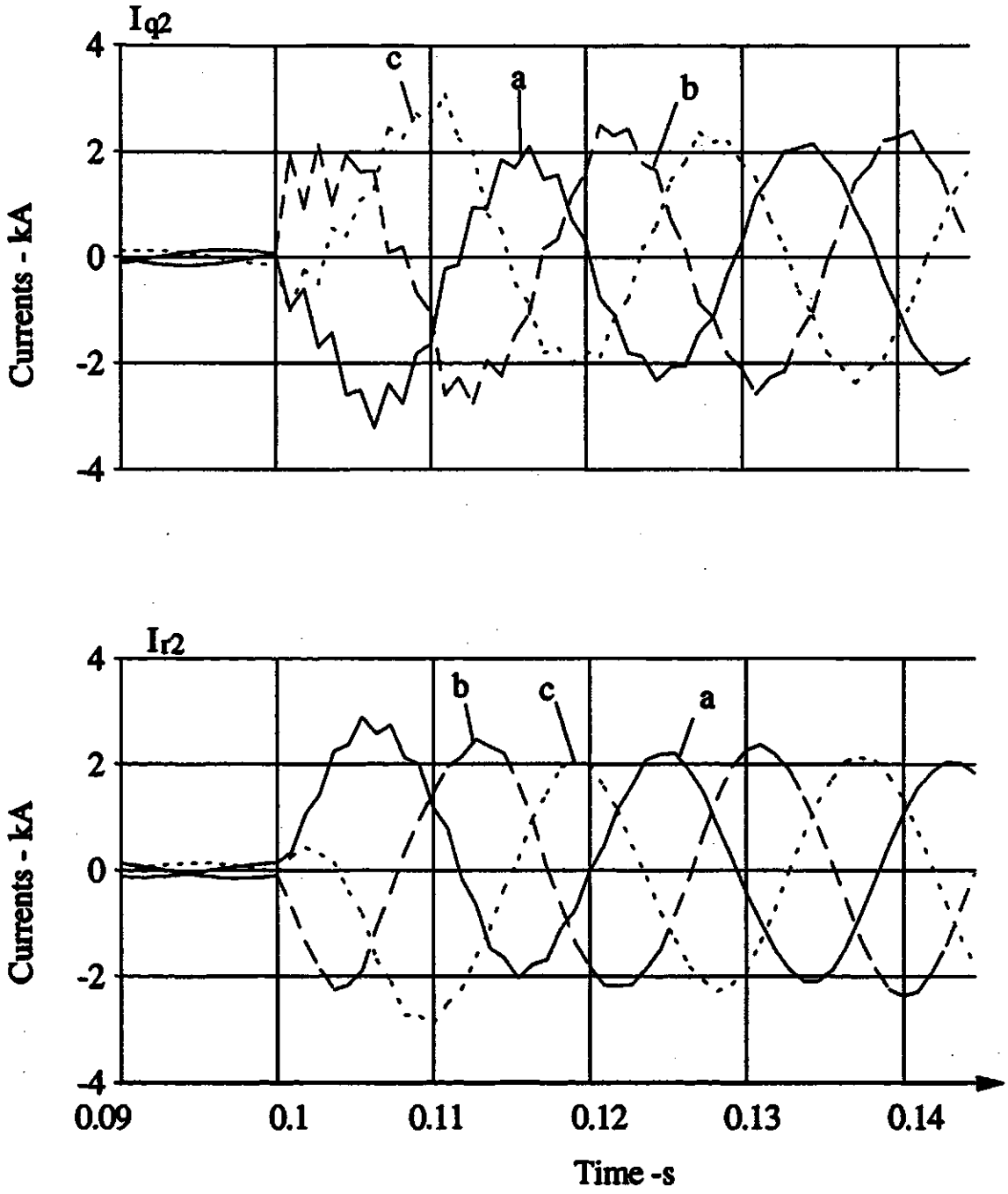

Figure 7.21. Waveforms of currents in Circuit 2 for a 3-phase fault at T_1 with currents outflow at terminal R.

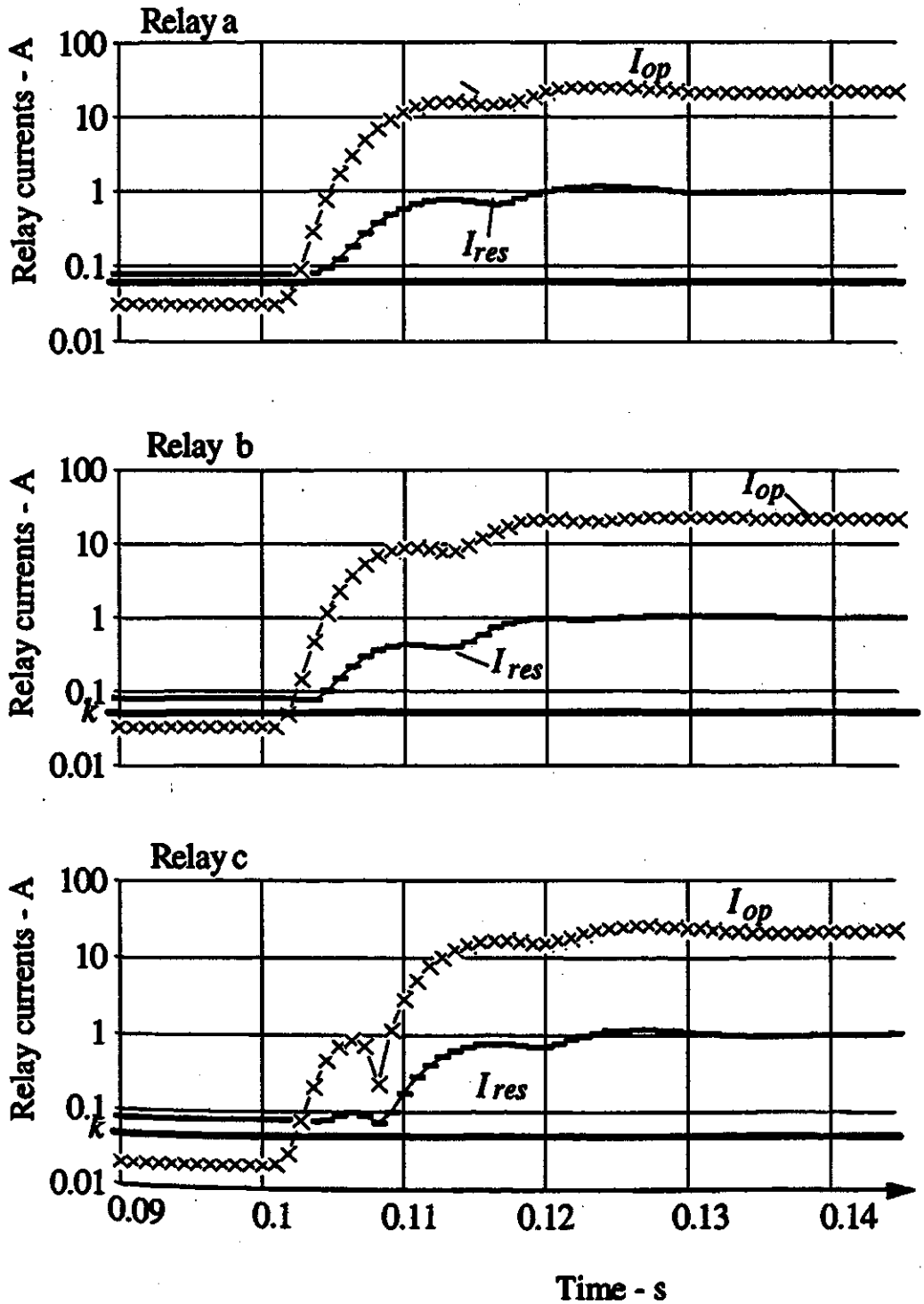

Figure 7.22. Operating and restraining currents in the master relay of Circuit 1 for a 3-phase fault at Q_1 with current outflow at terminal R.
I_{op} - Operating current,
I_{res} - Restraining current.

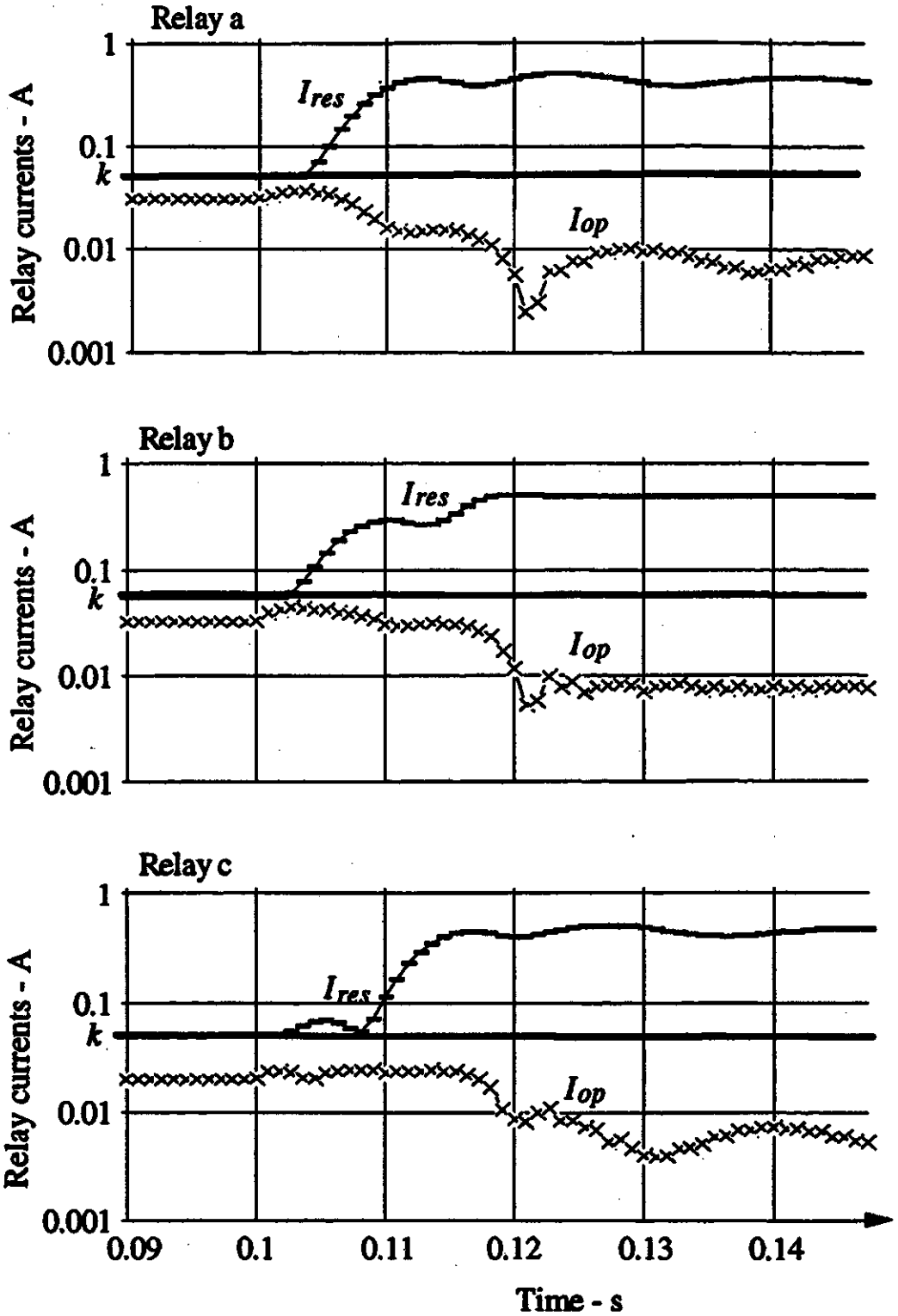

Figure 7.23. Operating and restraining currents in the master relay of Circuit 2 for a 3-phase fault at Q_1 with current outflow at terminal R.
I_{op} - Operating current,
I_{res} - Restraining current.

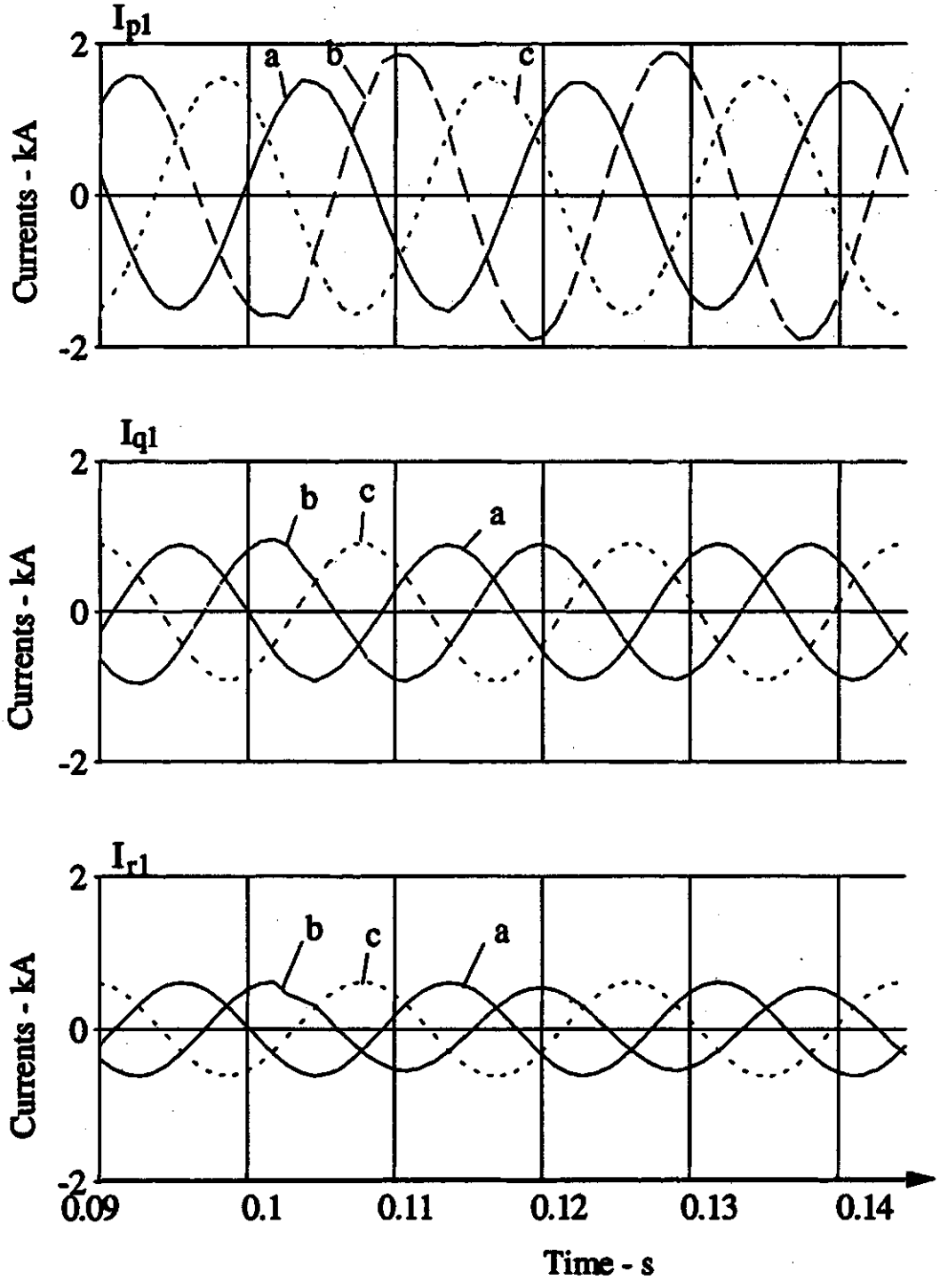

Figure 7.24. Waveforms of currents in Circuit 1 for a phase a-to-g fault at T_1 with 600 Ω fault resistance.

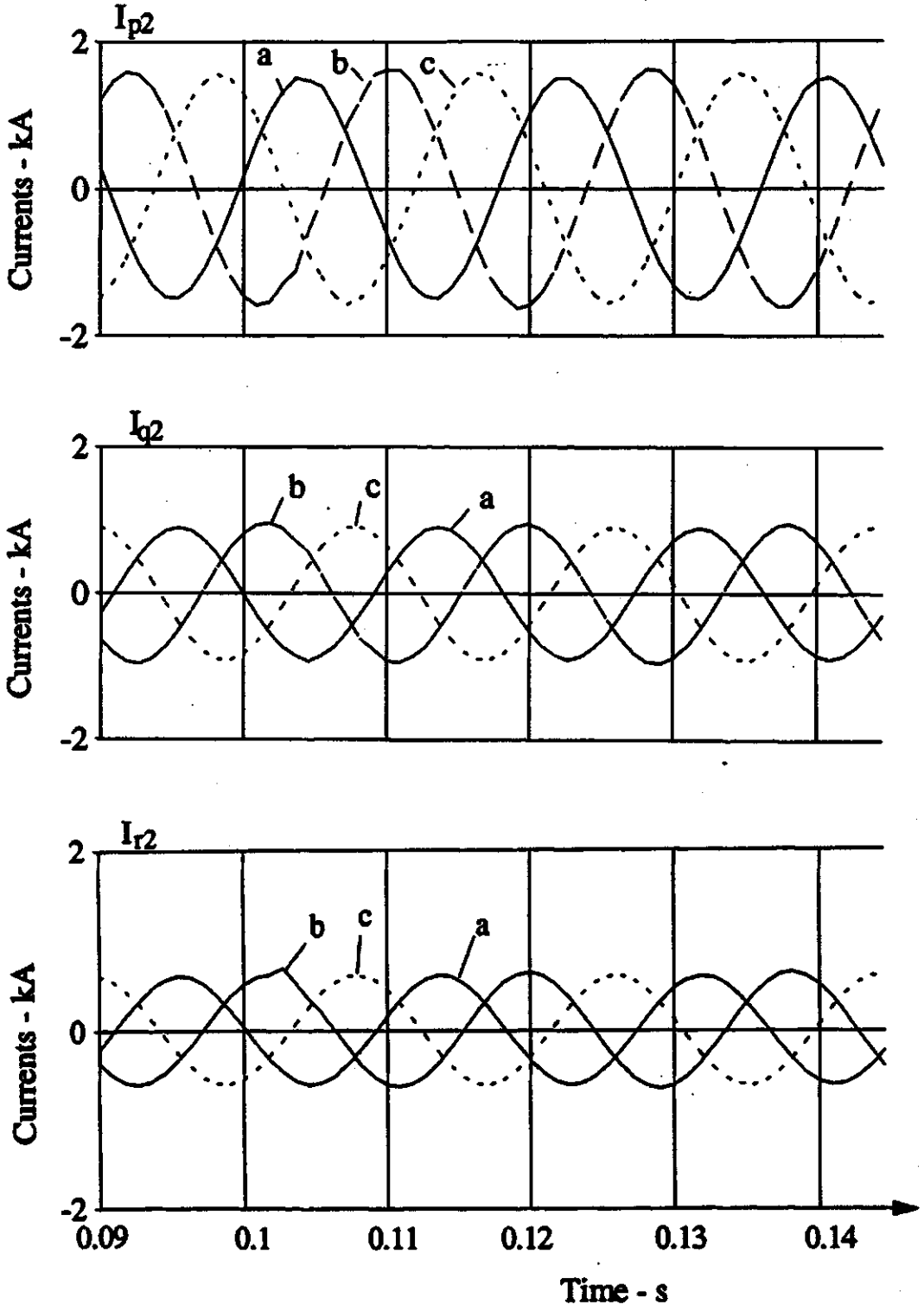

Figure 7.25. Waveforms of currents in Circuit 2 for a phase a-to-g fault at T_1 with 600 Ω fault resistance.

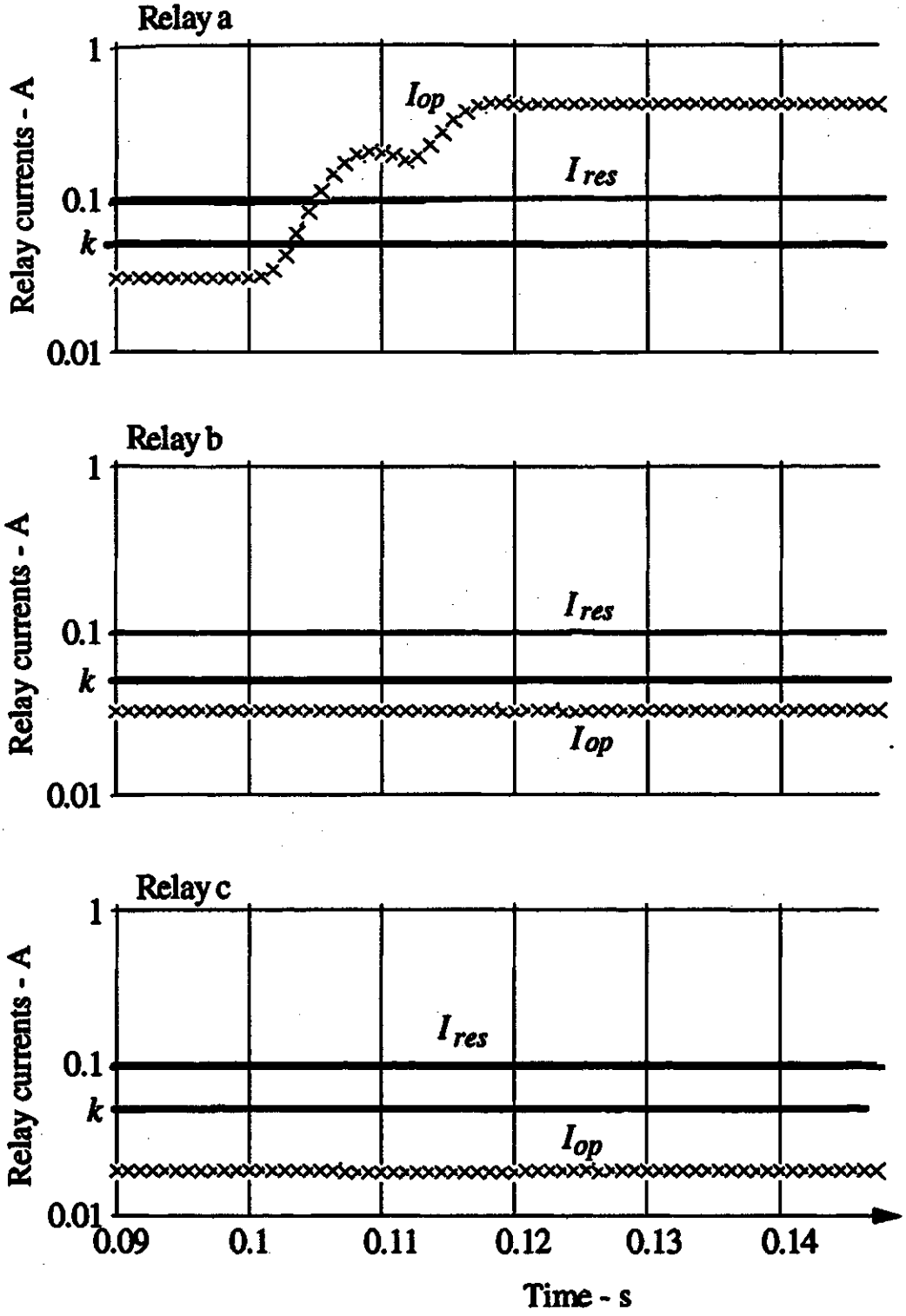

Figure 7.26. Operating and restraining currents in the master relay of Circuit 1 for a phase a-to-g fault at T_1 with 600 Ω fault resistance.
I_{op} - Operating current,
I_{res} - Restraining current.

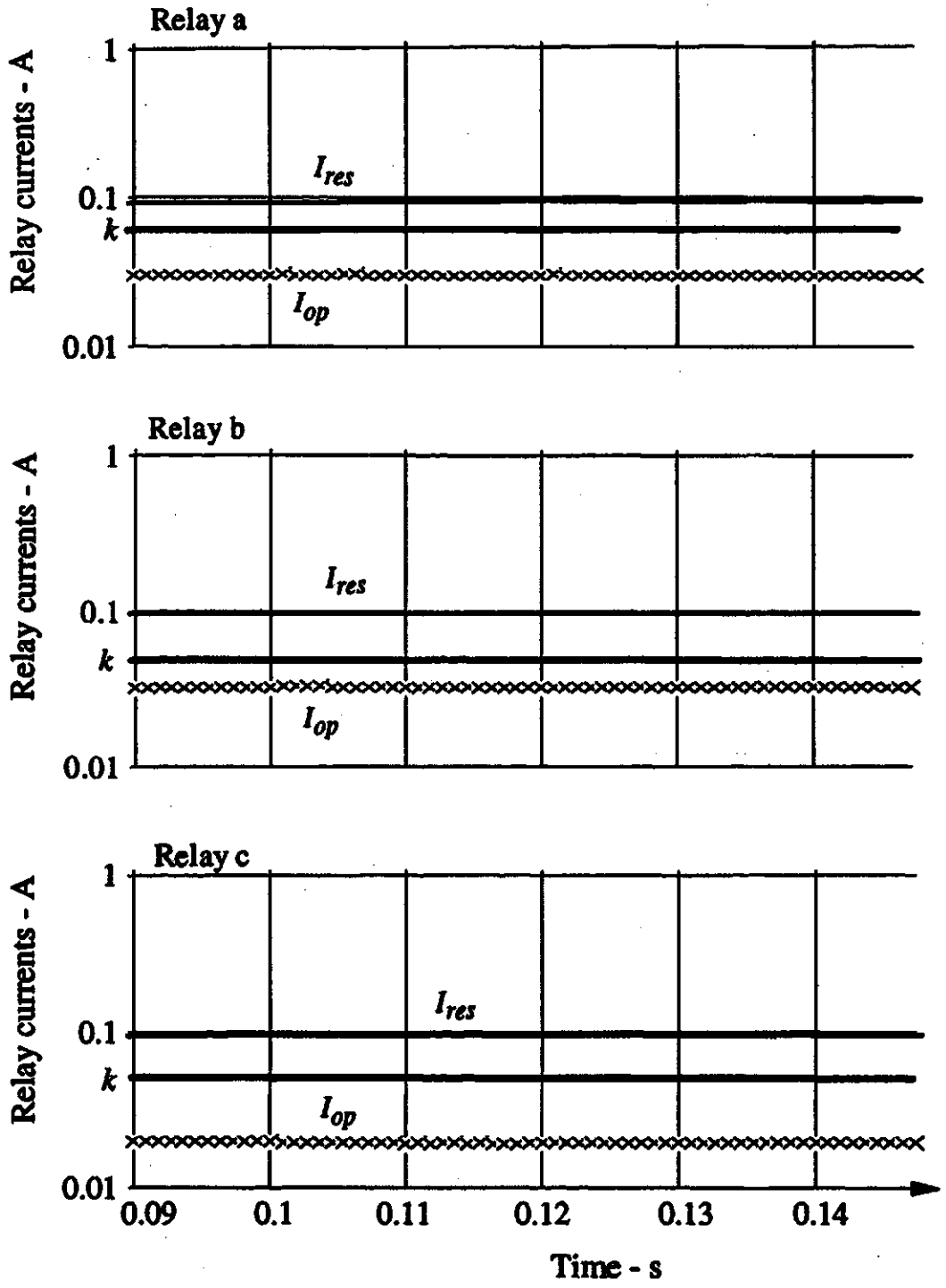

Figure 7.27. Operating and restraining currents in the master relay of Circuit 2 for a phase a-to-g fault at T_1 with 600 Ω fault resistance.
I_{op} - Operating current,
I_{res} - Restraining current.

8. SUMMARY AND CONCLUSIONS

8.1. Summary

Teed lines are used in high voltage electrical transmission networks for economic and environmental reasons. A parallel-teed line is a special case of a teed line in that there is mutual coupling between the parallel circuits and reclosure techniques, when applied, are more complex. These lines are heavily loaded for most of the time, therefore, system used to protect them are not very secure. Improper relaying operation can result in loss of transmission capacity which can result in system instability. For these reasons, relays with exceptionally good performance are required to provide reliable protection for the teed or parallel-teed lines. The objective of this research was to investigate the problem of protecting parallel-teed lines and develop a suitable algorithm for protecting these lines.

The protection techniques used in electrical transmission systems are reviewed in Chapter 2. These techniques are based on a comprehensive understanding of power system operation. With the acceptance of computer-based applications in electrical power systems, interest has increased in designing relays which will perform better than the conventional relays. Digital techniques have provided more opportunities for making innovations. Chapter 3 outlined the developments in digital relaying technology which have taken place during the last twenty years.

Chapter 4 discussed the application of conventional relaying techniques to the protection of parallel-teed lines. The discussions are split in two categories, the application of non-unit techniques and the application of unit techniques. The settings of relays, when conventional techniques are used, remain unaltered as the system operating state changes. In several operating states, their performance is unacceptable.

A new approach for detecting faults on parallel-teed lines has been presented in Chapter 5. Based on modal analysis and transmission line equations, this technique compensates for the impact of the change of current in the lines and takes into account the couplings between the parallel circuits. The proposed technique uses data collected

at the line terminals. The proposed algorithm was incorporated in a simulation of the relaying system. Some design features of the system are discussed in Chapter 6. To implement the differential algorithm, data sampled at the individual terminals must be synchronized before applying the relaying criterion. Based on the same theory as the differential algorithm, a simple synchronization technique is proposed. A technique for detecting the inception of faults is also developed.

An electromagnetic transient program, EMTDC, was used to generate fault data on a model electrical power system. The system operating and fault conditions, and the line configurations were altered to conduct several studies. The proposed protection system was simulated by an interface program; the parameters used in these simulations are discussed in Chapter 7. Test results obtained from the simulations indicate satisfactory relay performance. All the faults simulated for testing the relaying system were correctly detected. The algorithm proved to be sensitive, selective, stable and fast. Line faults were generally detected approximately four samples after their inception.

8.2. Conclusions

There are two main advantages of the proposed technique. Firstly, the proposed algorithm can be used to protect parallel-teed transmission lines. This is a major improvement because the conventional protection techniques cannot achieve this. Secondly, the spurious output of the relay operating signal is minimal during the normal operating conditions. This allows the relay engineers to use lower settings which increases the sensitivity of the relaying system. The simulations show that the relay is able to detect high resistance faults, arc resistance as high as 600 - 800 Ω. There are a few special opereating conditions in which the proposed algorithm can not protect the parallel-teed transmission lines. Backup relays based on other operating principles must be used to cover these situations.

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APPENDICES

Appendix A. The Distribution of Zero Sequence Current in A Teed Line

A typical parallel-teed transmission line, drawn in Fig. A.1, was used to study the distribution of zero sequence currents in a single-phase-to-ground fault condition. The selected fault locations are shown in the figure as F_1, F_2 and F_3 respectively.

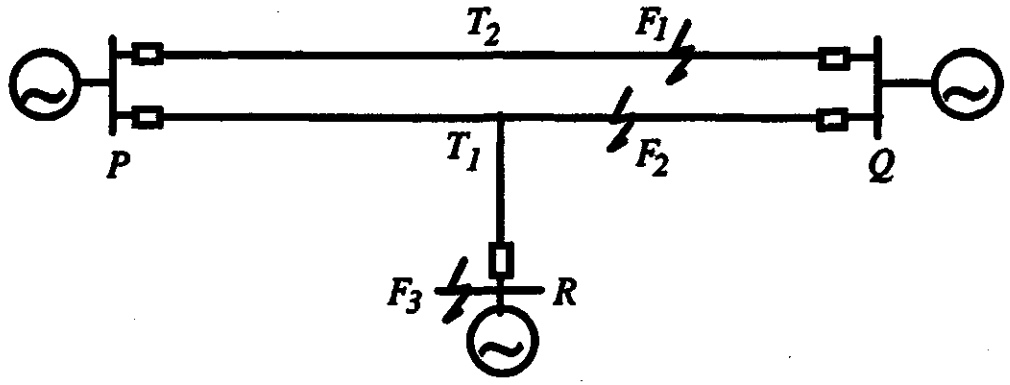

Figure. A.1. The Single line diagram of a PTTL

For a single phase to ground fault at F_1, the equivalent zero sequence network diagram [4] is drawn as Fig. A.2. By applying Kirchhoff voltage law, the voltage equations can be expressed for the loop of PQ,

$$\begin{bmatrix} Z_{ps}+(p+k'q)Z_l & -(Z_{qs}+(1-k')qZ_l \\ Z_{ps}+(p+k'q)Z_m & Z_{qs}+(p+k')qZ_m \end{bmatrix}\begin{bmatrix} I_{p1} \\ I_{q1} \end{bmatrix}=$$
$$=\begin{bmatrix} -(Z_{ps}+pZ_l) & -(Z_{qs}+pZ_m \\ -(Z_{ps}+pZ_m) & -(Z_{qs}+pZ_l \end{bmatrix}\begin{bmatrix} I_{p2} \\ I_{q2} \end{bmatrix}. \qquad (A.1)$$

Equation A.1 can be transformed by

$$\begin{bmatrix} I_{p1} \\ I_{q1} \end{bmatrix}=\frac{1}{\Delta}\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\begin{bmatrix} I_{p2} \\ I_{q2} \end{bmatrix}, \qquad (A.2)$$

where:

k'	is the length from T_1 to F_1 to the length of branch QT_1 and
p,q	are the ratio of the length of branch PT_1, QT_1 to the length of PQ respectively.

$\Delta=(p+k'q)Z_{qs}-(1-k')qZ_{ps}$, and

$$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} =$$

$$= \begin{bmatrix} pZ_{qs}+(1-k')q(Z_{ps}+p(Z_m+Z_l)), & -((qZ_{qs}+(1-k')q(Z_{qs}+q(Z_m+Z_l))) \\ Z_{ps}+(p-k'q)(Z_{ps}+p(Z_m+Z_l)), & -((qZ_{ps}+(p-k'q)(Z_{qs}+q(Z_m+Z_l))) \end{bmatrix},$$

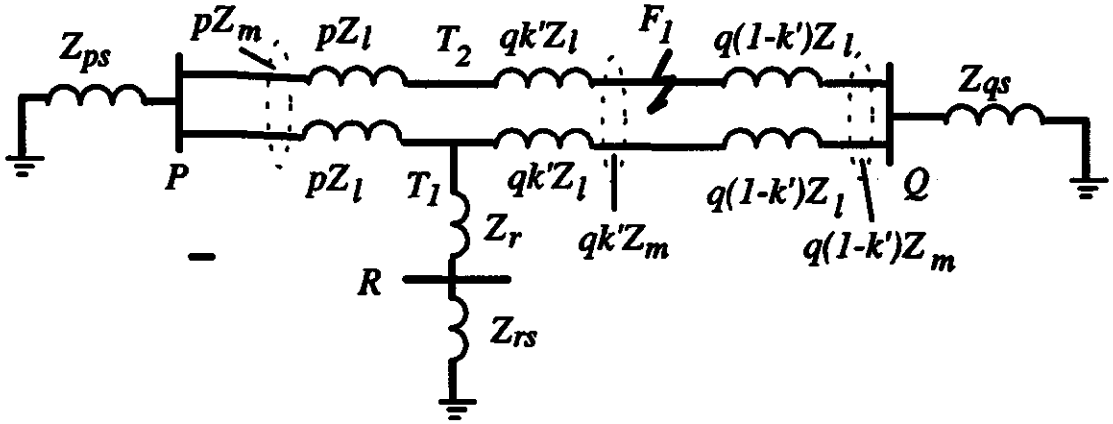

Figure A.2. Zero sequence circuit for calculating fault at F_1.

The current equation exists for the loop of PR.

$$I_{q2} = -(Z_{ps} + pZ_m)\, I_{p1} + (Z_{ps} + pZ_l + Z_r + Z_m) I_{p2} \;/(Z_r + Z_m) =$$
$$= b_{11}\, I_{p1} + b_{12} I_{p2}. \qquad \text{(A.3)}$$

Substitute Equation A.3 into A.2, the following result can be derived.

$$I_{p1} = \frac{1}{\Delta}(a_{11} I_{p2} + a_{12}(b_{11} I_{p1} + b_{12} I_{p2})), \qquad \text{(A.4)}$$

or

$$\frac{I_{p1}}{I_{p2}} = \frac{a_{11}+a_{12}b_{12}}{\Delta - a_{12}b_{11}} =$$

$$= \frac{pZ_{qs}+(1-k')q(Z_{qs}+p(Z_m+Z_l)+q(Z_{qs}+(1-k')(Z_{qs}+q(Z_m+Z_l)))(1+C_{rl})}{(p+k'q)Z_{qs}-(1-k')qZ_{ps}-q(Z_{qs}+q(Z_m+Z_l)))C_{rm}} =$$

$$= \frac{Z_{qs}+(1-k')q(Z_{ps}+Z_{qs}+Z_l+Z_m)+q(Z_{qs}+(1-k')(Z_{qs}+q(Z_m+Z_l)))C_{rl}}{Z_{qs}+(1-k')q(Z_{ps}+Z_{qs})-q(Z_{qs}+(1-k')q(Z_{qs}+q(Z_m+Z_l)))C_{rm}},$$

where:

$$C_{rl} = \frac{Z_{ps}+pZ_l}{Z_r+Z_m},$$

$$C_{rm} = \frac{Z_{ps} + pZ_m}{Z_r + Z_m} .$$

Similarly, for the currents at Side Q,

$$I_{q1}(Z_{qs}+(1-k')qZ_m) + I_{q2}(Z_{qs}+qZ_1+Z_r+Z_m) =$$
$$= I_{p1}(k'qZ_m+Z_r+Z_m) + I_{p2}(Z_r+Z_m) = (K_p(k'qZ_m+Z_r+Z_m)+Z_r+Z_m)I_{p2} ,$$

$$I_{p2} = \frac{(Z_{qs}+(1-k')qZ_m)I_{q1} + (Z_{qs}+qZ_1+Z_r+Z_m)}{K_p(k'qZ_m+Z_r+Z_m)+Z_r+Z_m} = c_{11}I_{q1} + c_{12}I_{q2} . \qquad (A.5)$$

Substitute A.5 into Equation A.1,

$$\frac{I_{q1}}{I_{q2}} = \frac{a_{21}c_{12}+a_{22}}{\Delta - a_{21}c_{11}} =$$

$$= \frac{(pZ_{ps}+(p+k'q)(Z_{ps}+p(Z_m+Z_1)))C_{r2}+(p-q)Z_{ps+}(p+k'q)(Z_{ps}-Z_{qs}+(p-q)(Z_m+Z_1))}{(p+k'q)Z_{qs}-(1-k')qZ_{ps}-c_{11}(pZ_m+(p+k'q)(Z_{ps}+p(Z_m+Z_1)))} .$$

If $Z_{rs} = \infty$, and k'=0, the equation becomes

$$\frac{I_{p1}}{I_{p2}} = \frac{Z_{qs}+q(Z_{ps}+Z_{qs}+Z_l+Z_m)}{Z_{qs}=q(Z_{ps}+Z_{qs})} . \qquad (A.7)$$

Further more, when q=0,

$I_{p1}/I_{p1} = 1$,

$I_{q1}/I_{q1} = -(1+(2Z_{qs}+Z_1+Z_m))/Z_{qs}$. (A.8)

The minus sign indicates that the currents in the two circuits at terminal Q are 180° out of phase.

When fault is at F_2 as is shown in Figure A.3, the equation is expressed by

$$\begin{bmatrix} Z_{ps}+(p+k''q)Z_1+C_{rm}k''qZ_m & -(Z_{qs}+(1-k'')qZ_1 \\ Z_{ps}+(p+k''q)Z_m+C_{rm}k''qZ_1 & -(Z_{qs}+(1-k'')qZ_m \end{bmatrix} \begin{bmatrix} I_{p1} \\ I_{q1} \end{bmatrix} =$$
$$\begin{bmatrix} -(Z_{ps}+pZ_m+(1-C_{r1})k''qZ_m) & Z_{qs}+(1-k'')qZ_m \\ -(Z_{ps}+pZ_1+(1-C_{r1})k''qZ_1) & Z_{qs}+(1-k'')qZ_1 \end{bmatrix} \begin{bmatrix} I_{p2} \\ I_{q2} \end{bmatrix} . \qquad (A.9)$$

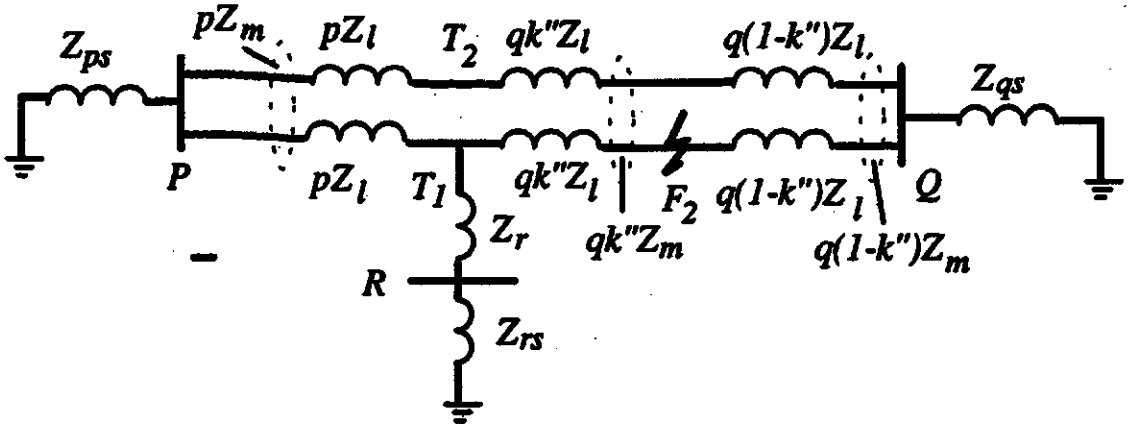

Figure A.3. Zero sequence circuit for calculating fault at F_2.

Equation A.9 is solved by

$$\begin{bmatrix} I_{p2} \\ I_{q2} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} a'_{11} & a'_{12} \\ a'_{21} & a'_{22} \end{bmatrix} \begin{bmatrix} I_{p1} \\ I_{q1} \end{bmatrix} .$$

where:

$a'_{11} = (p+k''q)[Z_{qs} + (1-k'')q(Z_l + Z_m) + q(1-k'')Z_{ps} - C_{rm} k''qZ_{qs}]$,

$a'_{12} = -[(1-k'')q(2Z_{qs} + (1-k'')q(Z_l + Z_m))]$,

$a'_{21} = pZ_{qs} + (p-k''q)(Z_{ps} + p(Z_l + Z_m)) + (1-C_{rl})k''q(Z_{ps} + (p + k''q)(Z_l + Z_m)]$,

$a'_{22} = -[p(Z_{ps} + (1-k'')q(Z_l + Z_m)) + (1-C_{rl})k''q(Z_l + Z_m + Z_{qs})]$,

$\Delta = (k''qC_{rm} + (p-k''q))Z_{qs} + (1-k'')qZ_{ps} + (1-k'')q^2k''C_{rm}$,

$$C_{rm} = \frac{Z_{ps} + pZ_m}{Z_r + Z_m} \quad \text{and}$$

$$C_{rl} = \frac{Z_{ps} + pZ_l}{Z_r + Z_m}.$$

The currents at the two terminals of Circuit 1 have $I_{p1} = -I_{q1}$, by substitution,

$$\frac{I_{p1}}{I_{p2}} = \frac{k''qC_{rm} + (p+k''q))Z_{qs} + (1-k'')qZ_{ps} + (1-k'')q^2k''C_{rm}}{(p+qk'')B_q + q(1-k'')Z_{ps} - qC_{rm}k''Z_{qs}] - [(1-k'')q(2Z_{qs} + (1-k'')q(Z_m + Z_l))]},$$

where:

$B_q = Z_{qs} + (1-k'')q(Z_l + Z_m)$,

Similarly, for a fault at F_3, the equivalent circuit is as shown in Figure A.4. The equations can be written by

$$\begin{bmatrix} Z_{ps}+pZ_l & -(Z_{ps}+qZ_l) \\ Z_{ps}+pZ_m & -(Z_{ps}+qZ_m) \end{bmatrix} \begin{bmatrix} I_{p1} \\ I_{q1} \end{bmatrix} = \begin{bmatrix} -(Z_{ps}+pZ_m) & Z_{qs}+qZ_m \\ -(Z_{ps}+pZ_l) & Z_{qs}+pZ_l \end{bmatrix} \begin{bmatrix} I_{p2} \\ I_{q2} \end{bmatrix}, \quad \text{(A.11)}$$

$$\begin{bmatrix} I_{p2} \\ I_{q2} \end{bmatrix} = \frac{1}{\Delta''} \begin{bmatrix} pZ_{qs}+qZ_{ps}+pq(Z_m+Z_l) & p(2Z_{ps}+p(Z_l+Z_m)) \\ -(pZ_{qs}+qZ_{ps}+pq(Z_m+Z_l)) & -p(2Z_{ps}+p(Z_l+Z_m)) \end{bmatrix} \begin{bmatrix} I_{p1} \\ I_{q1} \end{bmatrix}, \quad \text{(A.12)}$$

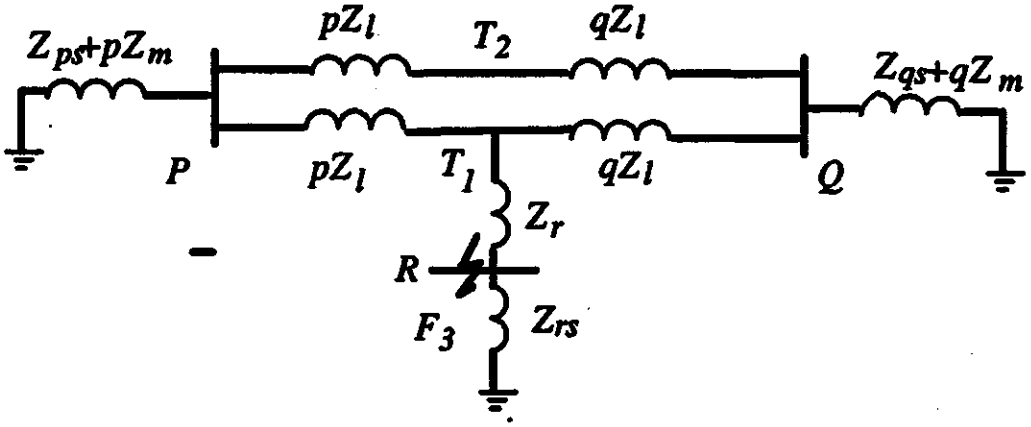

Figure A.4. Zero sequence circuit for calculating fault at F_3.

where:

$\Delta'' = pZ_{qs} - qZ_{ps}$.

By the relation $I_{p1} = -I_{q1}$, the following results can be derived.

$$\frac{I_{p1}}{I_{p2}} = \frac{pZ_{qs}-qZ_{ps}}{pZ_{qs}+qZ_{ps}+pq(Z_l+Z_m)-q(2Z_{qs}+q(Z_l+Z_m))} \quad \text{and}$$

$$\frac{I_{q1}}{I_{q2}} = \frac{qZ_{ps}-pZ_{qs}}{pZ_{qs}+qZ_{ps}+pq(Z_l+Z_m)-q(2Z_{qs}+q(Z_l+Z_m))}.$$

Appendix B. Modal Transformations for Three-phase Lines

The phasor relation of currents and voltages at any point along a three-phase transmission line can be expressed as

$$\frac{d}{dx}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = j\omega \begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{21} & l_{22} & l_{23} \\ l_{31} & l_{32} & l_{33} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}, \qquad \text{(B.1.a)}$$

$$\frac{d}{dx}\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = j\omega \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \qquad \text{(B.2.a)}$$

or short noted as

$$\frac{d}{dx}[V]_\varphi = j\omega[C][I]_\varphi \text{ and} \qquad \text{(B.1.b)}$$

$$\frac{d}{dx}[I]_\varphi = j\omega[L][V]_\varphi . \qquad \text{(B.2.b)}$$

The non-zero off-diagonal elements, l_{xy} and c_{xy} (x,y=1,2,3 and x≠y), in the matrices [*L*] and [*C*] reflect the mutual influence between phases. The mutual influence can be removed by modal analysis. Taking a particular phase as reference phase, the relations of quantities between a three-phase system and a modal system can be defined as

$[V]_\varphi = [S][V]_\varphi$,

$[I]_\varphi = [T][I]_\varphi$,

where:

[*S*] and [*T*] are 3x3 transformation matrices.

The transformation meet the relation

$[L]_m = [S][L]_\varphi[T]^{-1}$, and $[C]_m = [T][C]_\varphi[S]^{-1}$,

where:

$[L]_m$ and $[C]_m$ are diagonalized matrices,

the subscript *m* and φ denote modal and phase quantities respectively.

A ground mode, which is proportional to the sum of the three phase quantities, is usually denoted by a subscript '0', the other modes are called aerial modes.

When the three-phase line is geometrically balanced, the parameters of aerial modes are equal to each other [4]. Traditionally, transmission lines are simplified as balanced

line concerning relaying problems. In this case, the two transformation matrices, [S] and [T], are equal to each other. Some frequently used matrices for balanced lines are

1 Sequential transformation

The transformation matrices are defined as

$$[S]=[T]=\begin{bmatrix}1 & 1 & 1\\ 1 & e^{-120^\circ} & e^{120^\circ}\\ 1 & e^{120^\circ} & e^{-120^\circ}\end{bmatrix} \text{ and } [S]^{-1}=[T]^{-1}=\frac{1}{3}\begin{bmatrix}1 & 1 & 1\\ 1 & e^{120^\circ} & e^{-120^\circ}\\ 1 & e^{-120^\circ} & e^{120^\circ}\end{bmatrix}.$$

2. Karrenbauer's transformation

The transformation matrices are defined as

$$[S]=[T]=\begin{bmatrix}1 & 1 & 1\\ 1 & -2 & 1\\ 1 & 1 & -2\end{bmatrix} \text{ and } [S]^{-1}=[T]^{-1}=\frac{1}{3}\begin{bmatrix}1 & 1 & 1\\ 1 & -1 & 0\\ 1 & 0 & -1\end{bmatrix}.$$

3. Clarke's transformation

The transformation matrices is as follows.

$$[S]=[T]=\begin{bmatrix}1 & 1 & 1\\ 1 & -1/2 & -\sqrt{3}/2\\ 1 & -1/2 & \sqrt{3}/2\end{bmatrix} \text{ and } [S]^{-1}=[T]^{-1}=\begin{bmatrix}1 & 1 & 1\\ 2 & -1 & -1\\ 0 & -\sqrt{3} & \sqrt{3}\end{bmatrix}.$$

Appendix C. A parallel Line Modeled as Two balanced Three-phase Lines

Parallel circuits installed on horizontally or triangularly constructed towers can be approached by two balanced three-phase lines that only the ground modes quantities are mutually linked.

The parameter matrices of the two lines can be expressed by

$$[L]=\begin{bmatrix} l_1 & m_1 & m_1 & m_p & m_p & m_p \\ m_1 & l_1 & m_1 & m_p & m_p & m_p \\ m_1 & m_1 & l_1 & m_p & m_p & m_p \\ m_p & m_p & m_p & l_2 & m_2 & m_2 \\ m_p & m_p & m_p & m_2 & l_2 & m_2 \\ m_p & m_p & m_p & m_2 & m_2 & l_2 \end{bmatrix}, \quad \text{(C.1)}$$

$$[C]=\begin{bmatrix} c_1 & d_1 & d_1 & d_p & d_p & d_p \\ d_1 & c_1 & d_1 & d_p & d_p & d_p \\ d_1 & d_1 & c_1 & d_p & d_p & d_p \\ d_p & d_p & d_p & c_2 & d_2 & d_2 \\ d_p & d_p & d_p & d_2 & c_2 & d_2 \\ d_p & d_p & d_p & d_2 & d_2 & c_2 \end{bmatrix}. \quad \text{(C.2)}$$

The modal transformation can be carried by two steps. Firstly, use a matrix as

$$[H_1]=\begin{bmatrix} [H_t] & 0 \\ 0 & [H_t] \end{bmatrix},$$

where:

$[H_t]$ is a transformation matrix for a three-phase balanced line.

The [L] and[C] matrices are transformed by this matrix as

$$[L']=[H_1][L][H_1]^{-1}=\begin{bmatrix} \begin{bmatrix} l_{10} & 0 & 0 \\ 0 & l_{11} & 0 \\ 0 & 0 & l_{11} \end{bmatrix} & \begin{bmatrix} 3l_p & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 3l_p & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} & \begin{bmatrix} l_{20} & 0 & 0 \\ 0 & l_{21} & 0 \\ 0 & 0 & l_{21} \end{bmatrix} \end{bmatrix}, \quad \text{(C.3)}$$

$$[C']=[H_1][C][H_1]^{-1}=\begin{bmatrix} \begin{bmatrix} c_{10} & 0 & 0 \\ 0 & c_{11} & 0 \\ 0 & 0 & c_{11} \end{bmatrix} & \begin{bmatrix} 3c_p & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 3c_p & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} & \begin{bmatrix} c_{20} & 0 & 0 \\ 0 & c_{21} & 0 \\ 0 & 0 & c_{21} \end{bmatrix} \end{bmatrix}, \quad \text{(C.4)}$$

Secondly, a eigenvector matrix of [L'] and [C'] is identified as

$$[H_2]=\begin{bmatrix} [I] & [J_2] \\ [J_1] & [I] \end{bmatrix}, \quad \text{(C.5)}$$

where:

$$[J_x]=\begin{bmatrix} k_x & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

$x = 1, 2,$ and

$[I]$ is a order 3 unit matrix.

$$k_1 = \frac{1}{3x_p}\left(\frac{X_{01}-X_{02}}{2}+\sqrt{(3x_p)^2+\left(\frac{X_{01}-X_{02}}{2}\right)^2}\right),$$

$$k_2 = \frac{1}{3x_p}\left(\frac{X_{01}-X_{02}}{2}-\sqrt{(3x_p)^2+\left(\frac{X_{01}-X_{02}}{2}\right)^2}\right).$$

When the two circuits are identical,

$k_1 = -k_2 = 1$

The relationship of the modal quantities of the "six-phase" lines and the two "three-phase balanced lines" can be expressed by

$$\begin{bmatrix} I_0 \\ I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} I_{10}+K_1 I_{20} \\ I_{11} \\ I_{12} \\ K_2 I_{10}+I_{20} \\ I_{21} \\ I_{22} \end{bmatrix} \text{ and } \begin{bmatrix} V_0 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = \begin{bmatrix} V_{10}+K_1 V_{20} \\ V_{11} \\ V_{12} \\ K_2 V_{10}+V_{20} \\ V_{21} \\ V_{22} \end{bmatrix}. \qquad \text{(C.6)}$$

where:

I_0 - I_5 and V_0 - V_5 are the modal quantities of the "six-phase" lines and

I_{10} - I_{12}, V_{10} - V_{12} and I_{20} - I_{22} and V_{20} - V_{22} are the modal quantities in the two "three-phase" lines 1 and 2.

Using Karrenbauer's transformation as $[H_t]$ in Equation C.2, the [T] is as follows.

$$[T]=[H_1][H_2]=\frac{1}{3}\begin{bmatrix} \begin{bmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 0 & -1 \end{bmatrix} & \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} -1 & -1 & -1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} & \begin{bmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 0 & -1 \end{bmatrix} \end{bmatrix}, \qquad \text{(C.7)}$$

$$[T]^{-1} = [H_2]^{-1}[H_1]^{-1} = \frac{1}{3}\begin{bmatrix}\begin{bmatrix}1/2 & 1 & 1\\ 1/2 & -2 & 1\\ 1/2 & 1 & -2\end{bmatrix} & \begin{bmatrix}-1/2 & 0 & 0\\ -1/2 & 0 & 0\\ -1/2 & 0 & 0\end{bmatrix}\\ \begin{bmatrix}1/2 & 0 & 0\\ 1/2 & 0 & 0\\ 1/2 & 0 & 0\end{bmatrix} & \begin{bmatrix}1/2 & 1 & 1\\ 1/2 & -2 & 1\\ 1/2 & 1 & -2\end{bmatrix}\end{bmatrix}. \quad \text{(C.8)}$$

By these relations, the phase a quantities can be expressed by the "three-phase" modal quantities by

$$I_a = I_{11} + I_{12} + (I_{10} - I_{20})/2\,, \quad \text{(C.9)}$$

$$V_a = V_{11} + V_{12} + (V_{10} - V_{20})/2\,. \quad \text{(C.10)}$$

Appendix D. Simulated System Data

A single line diagram of the simulated system is drawn in Figure D.1. Three systems, S_p, S_q and S_r, were connected by a PTTL. The lengths of these lines from the junction to the three terminals are 100, 50 and 20 km respectively, as is shown in the diagram.

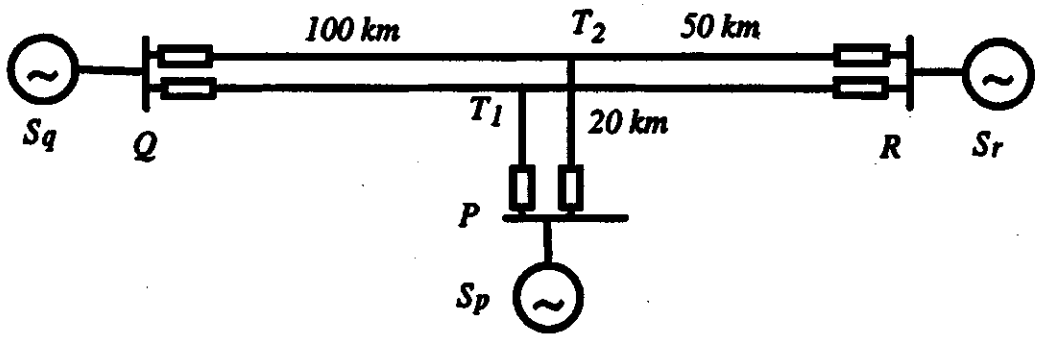

Figure D.1. Single line diagram of the simulated system.

D.1. Simulated Source Conditions

The connected systems were represented by their equivalent Thevenin voltage sources. Source P has a 20 GVA in capacity, and Source R and source Q have 1 GVA and 5 GVA in capacities respectively. The parameters of these simulated systems are listed in Tables D.1.

Table D.1. Parameters of the simulated sources.

System	Capacity (GVA)	X/R ratio	Z0/Z1 ratio
S_n	20	30	0.5
S_a	5	35	0.5
S_r	1	30	0.5

D.2. Parameters of the Simulated Transmission Lines

The parameters of the simulated lines were selected by referring the data in Reference [5]. The detail of these parameters are listed in Table D.2.

Table D.2. Line conductors.

Voltage (kV)	Name of ACSR	Strand of wire	# of bundles	Spacing (m)	Diam (cm)	R (dc) Ω/mi	R(60Hz) Ω/mi	GMR (cm)	Span (cm)	Sag (cm)
345	Drake	26/7	2	0.4572	2.81	0.112	0.114	1.137	305	6.7
500	Bluebird	84/19	2	0.4572	4.476	0.042	0.046	1.792	457	14

D.3. Tower Constructions

It was assumed that parallel 500 kV lines are installed side by side on horizontal constructed towers. The dimensions of the simulated construction of a pair of parallel 500 kV towers are shown in Figure D.2. The phasing pattern used in the simulation is also shown in the figure.

Parallel 345 kV lines were assumed to be installed on a vertical or triangular structured tower as shown in Figure D.3. Both structures were used in the simulation tests. The phasing pattern used for the simulation is shown in Figure D.3, which is the most unfavorable circular current around the parallel lines.

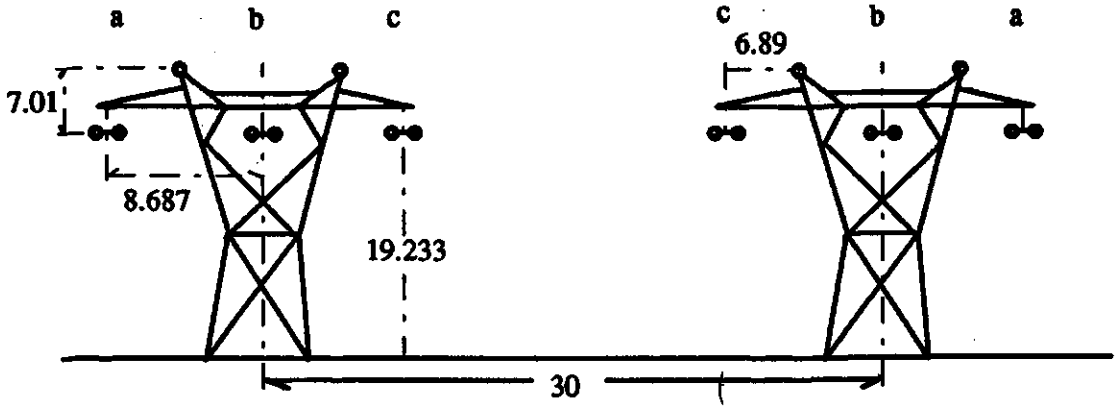

Figure D.2. 500 kV horizontal configuration and phasing pattern.
(Unit in meter).

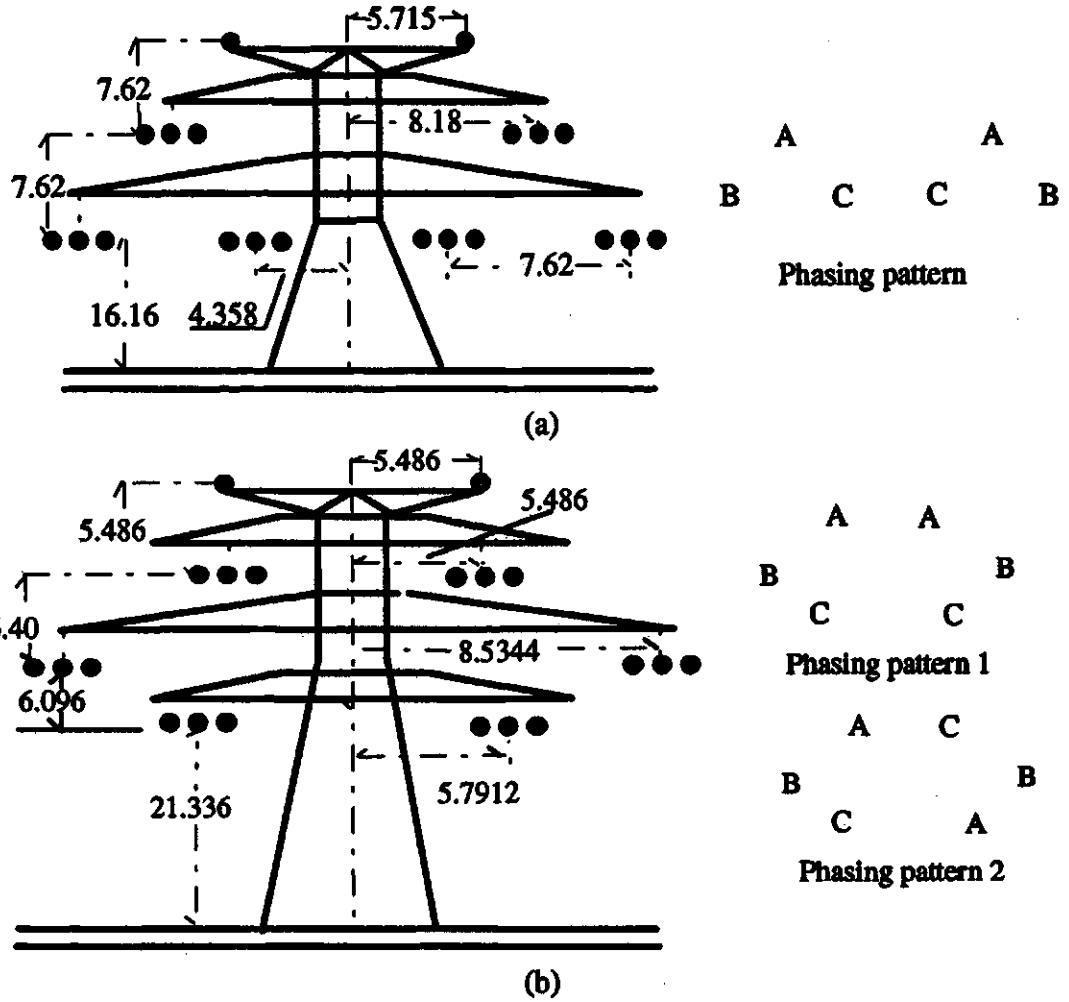

Figure D.3. 345 kV line triangular tower configuration and phasing patterns
(a) Triangular tower; (b) Vertical tower. (Unit in meter)

Appendix E. Results of Fault Case Studies for a 500 kV line

The parameters of the simulated 500 kV parallel teed transmission line are given in Appendix D. The included results are selected from simulation studies of internal faults on this 500 kV line at three locations. The system configuration is shown in Figure E.1. The fault condition and their waveforms are listed in Table E.1 correspondingly.

Table E.1. Lists of fault case studies on a 500 kV line

Waveforms	Fault type	Fault location
Figures E.2 - 5	b-c-g	R_1
Figures E.6 - 9	b-g	Q_1
Figures E.10 - 13	3-phases	T_1

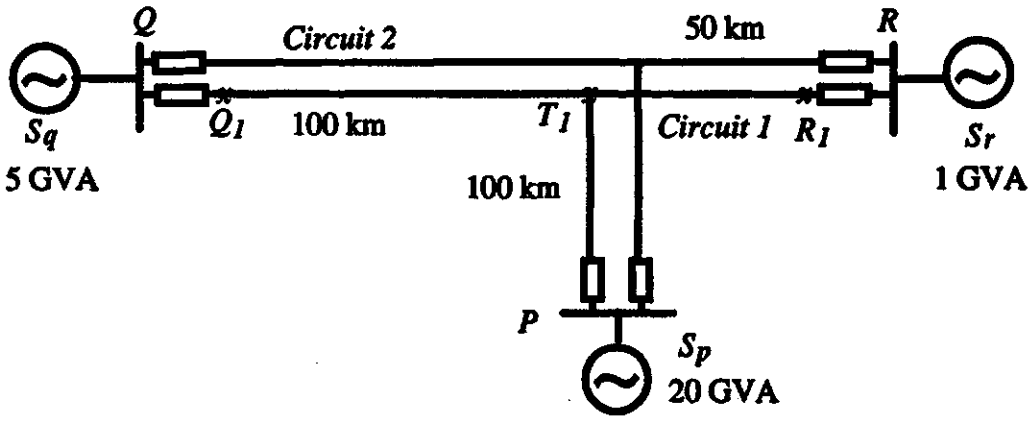

Figure E.1. The simulated 500 kV parallel teed transmission system.

The load flows in the transmission lines before the fault were arranged in such a way that the phase difference between the voltage phasors of the source S_p and S_q and between the voltage phasors of the S_p and S_r were set as 30° and 35° respectively.

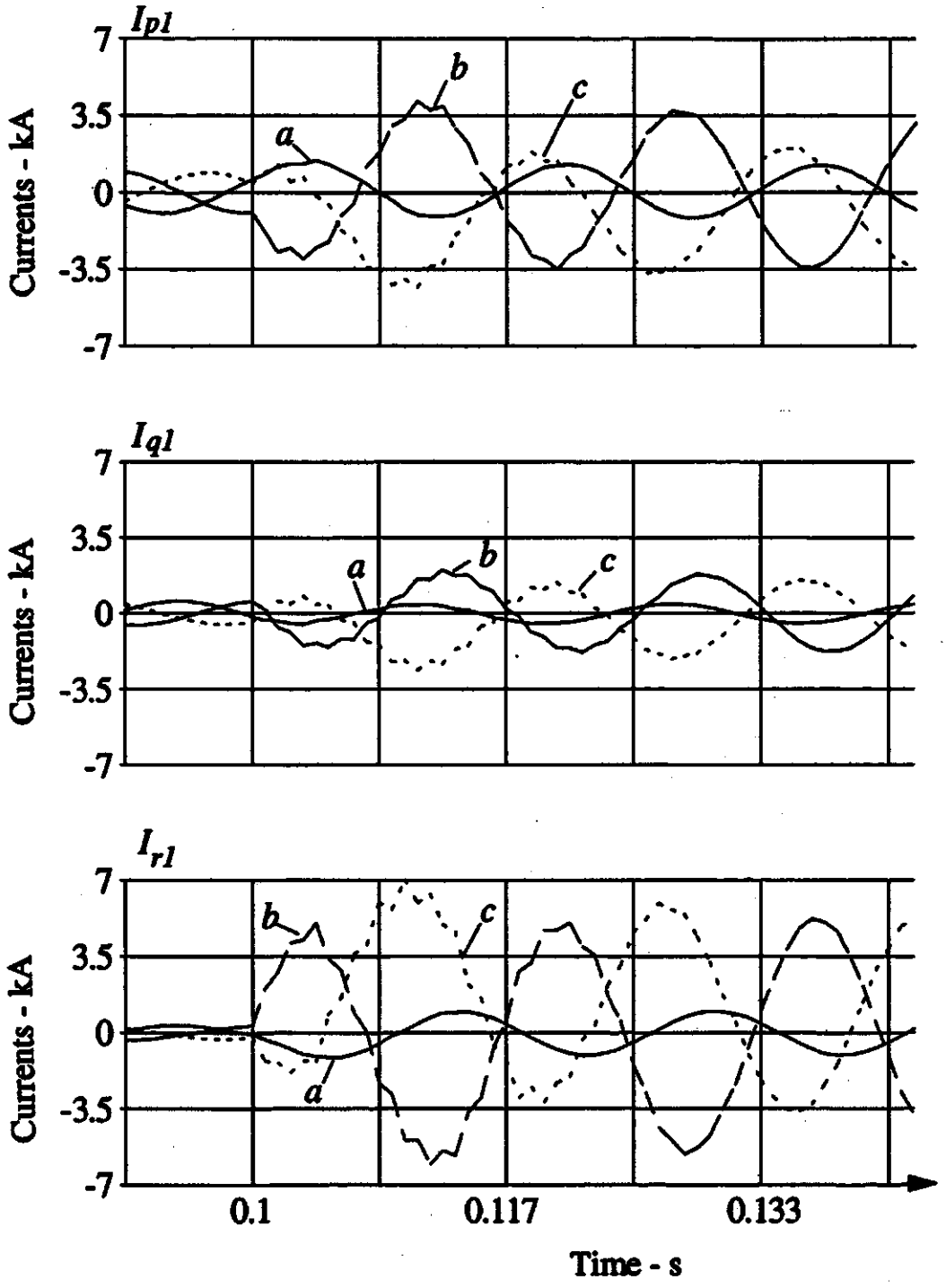

Figure E.2. Waveforms of currents in Circuit 1 for a b-c-g fault at R_1.

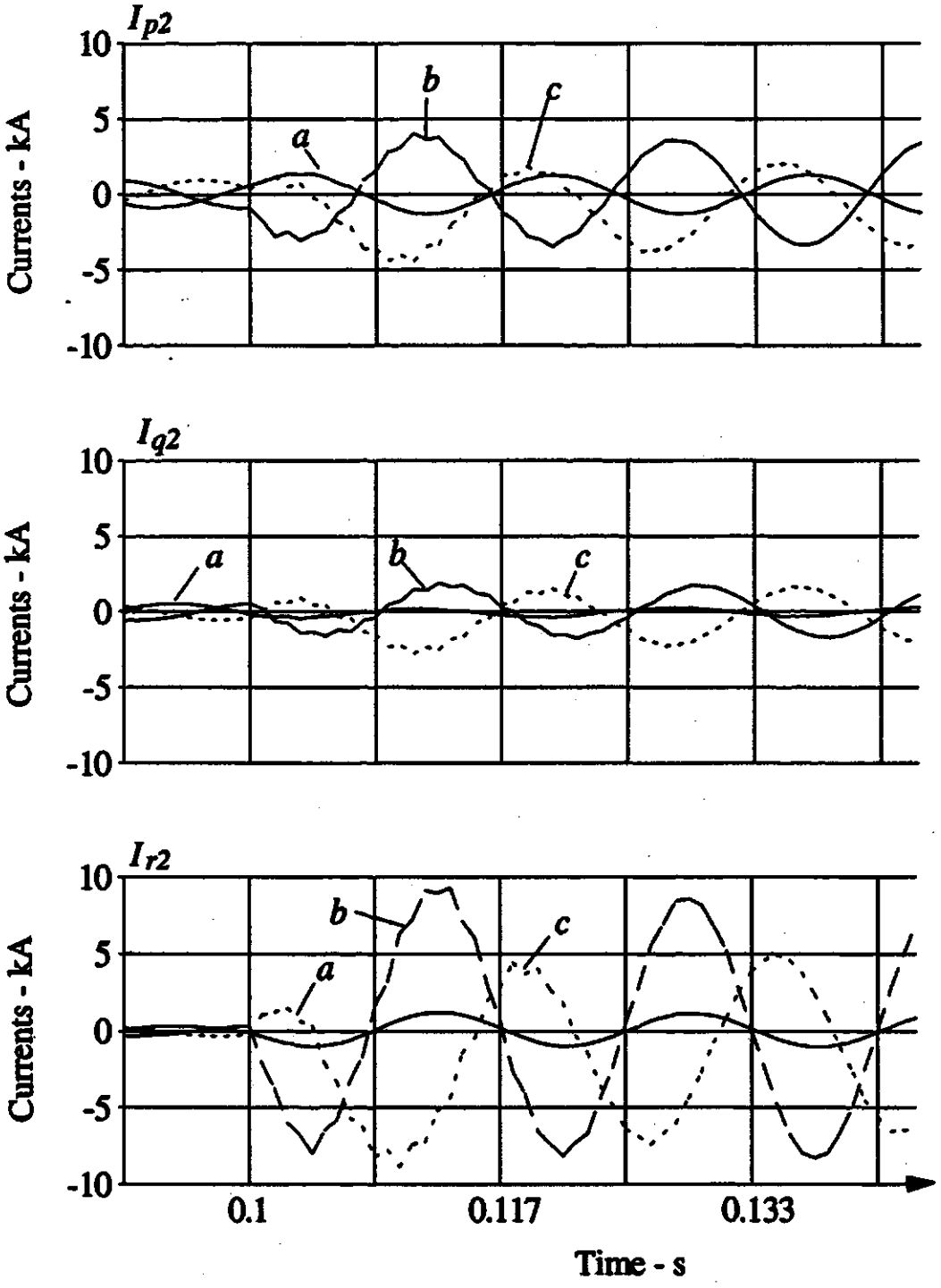

Figure E.3. Waveforms of currents in Circuit 1 for a b-c-g fault at R_1.

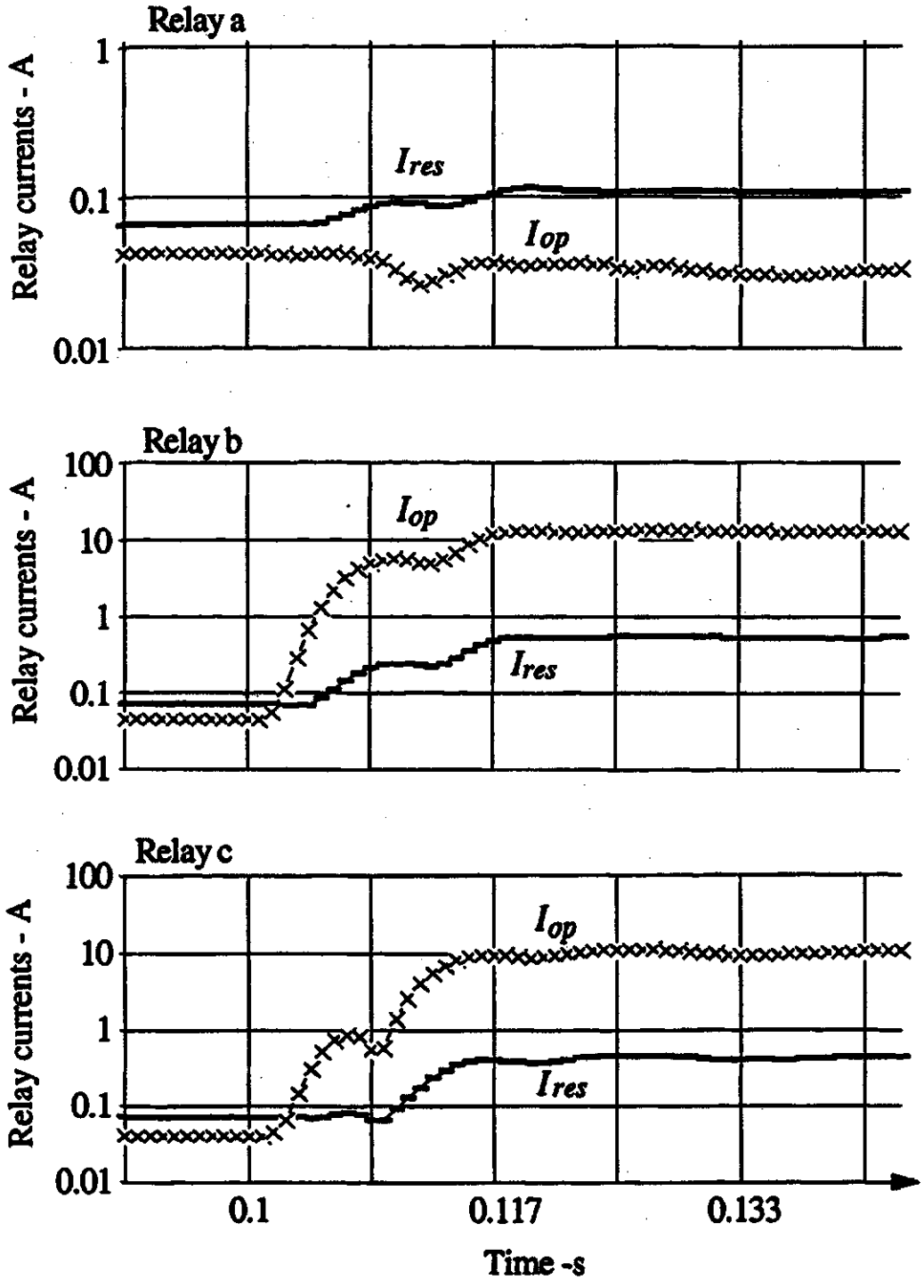

Figure E.4. Operating and restraining currents in the master relay of Circuit 1 for a b-c-g fault at R_1.
I_{op} - Operating current,
I_{res} - Restraining current.

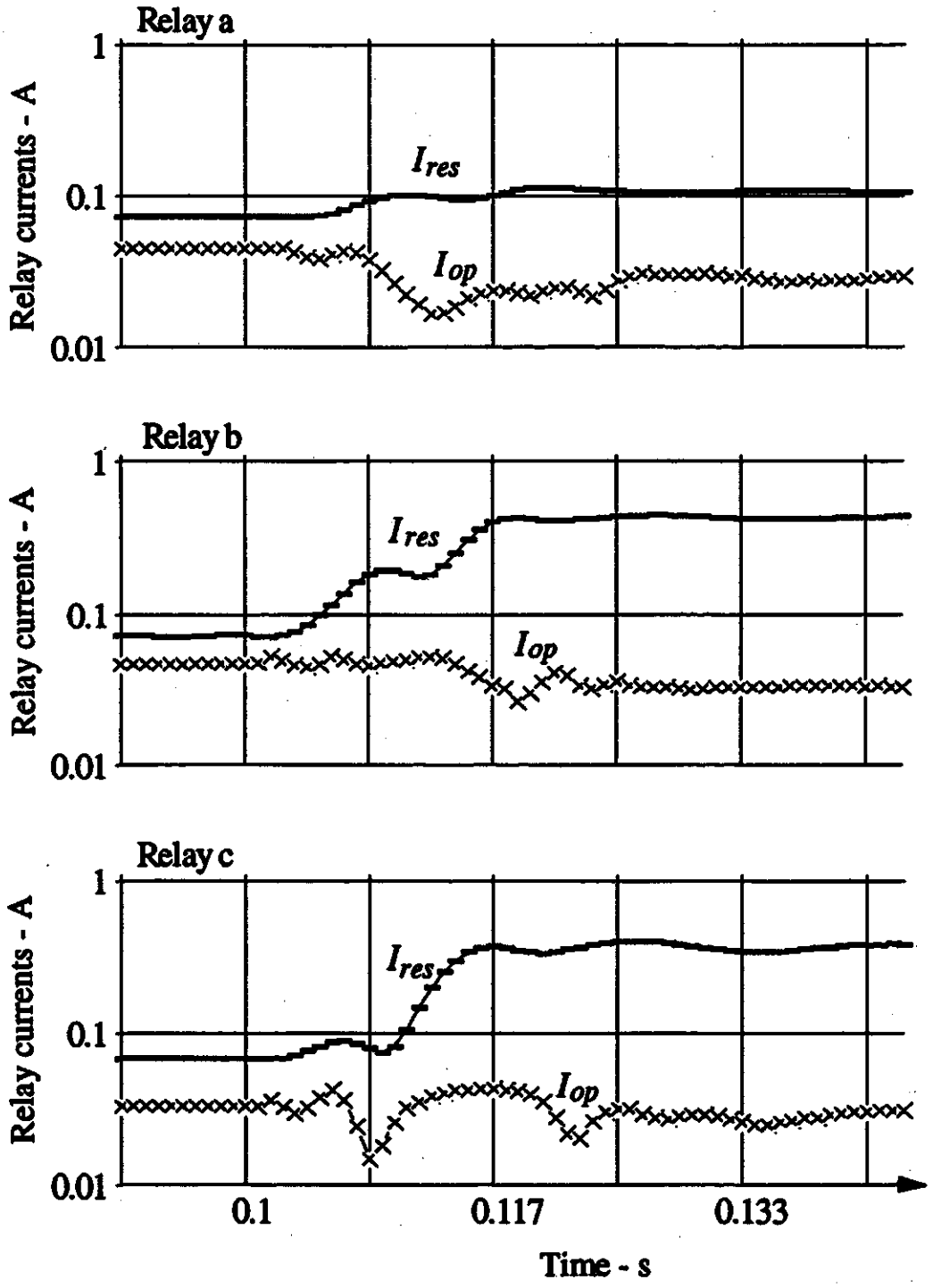

Figure E.5. Operating and restraining currents in the master relay of Circuit 2 for a b-c-g fault at R_1.
I_{op} - Operating current,
I_{res} - Restraining current.

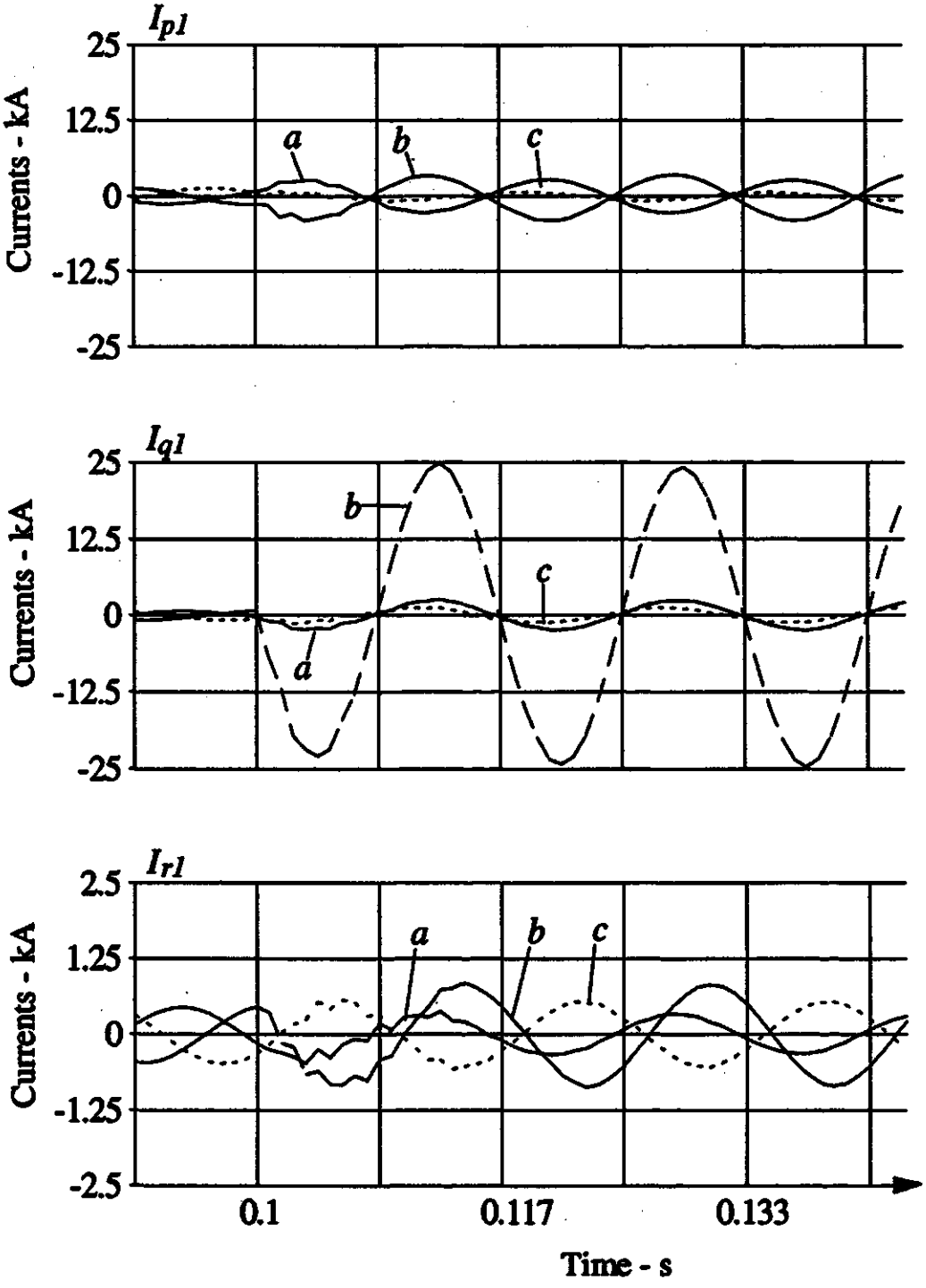

Figure E.6. Waveforms of currents in Circuit 1 for a b-g fault at Q_1.

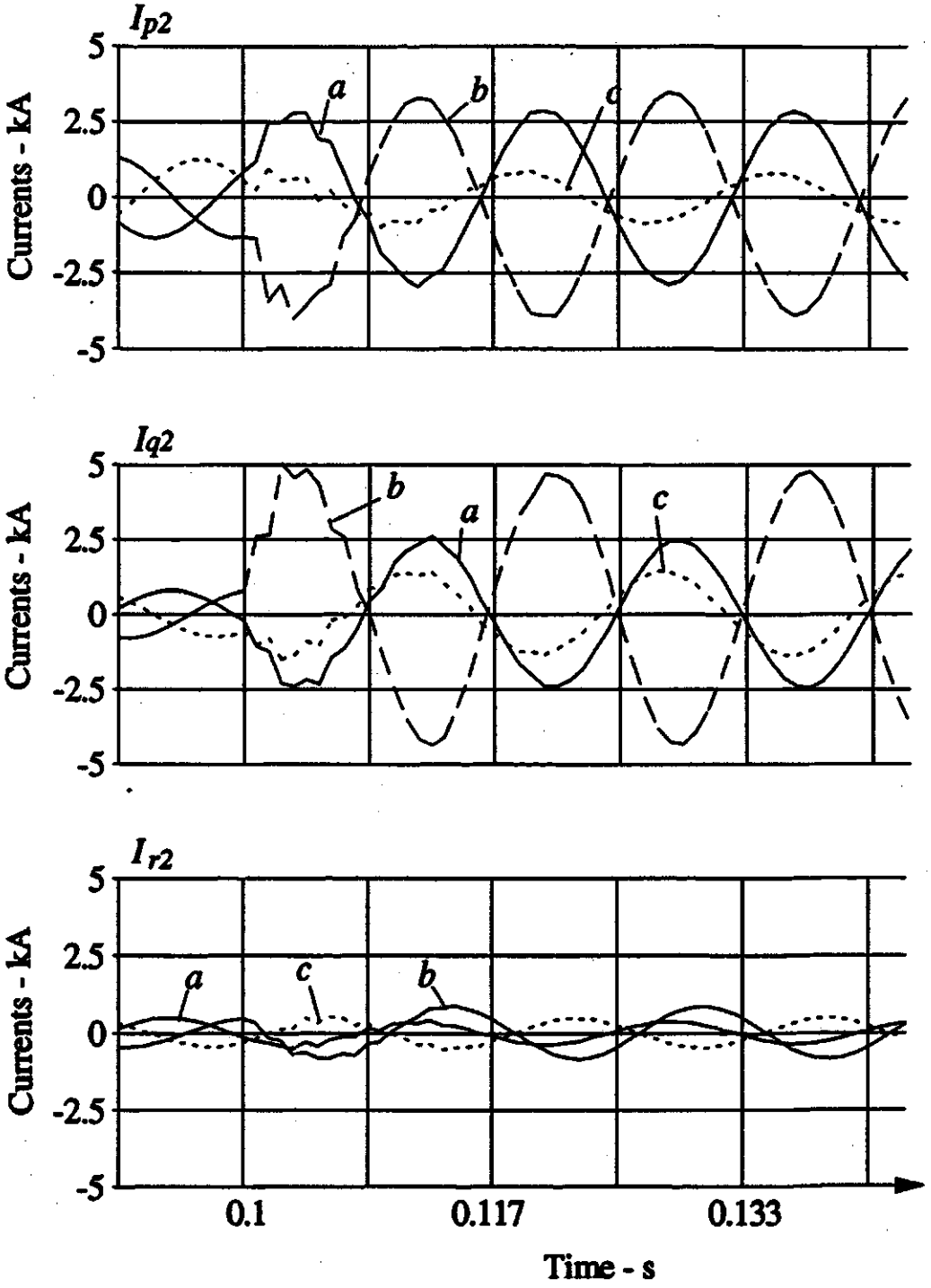

Figure E.7. Waveforms of currents in Circuit 2 for a b-g fault at Q_1.

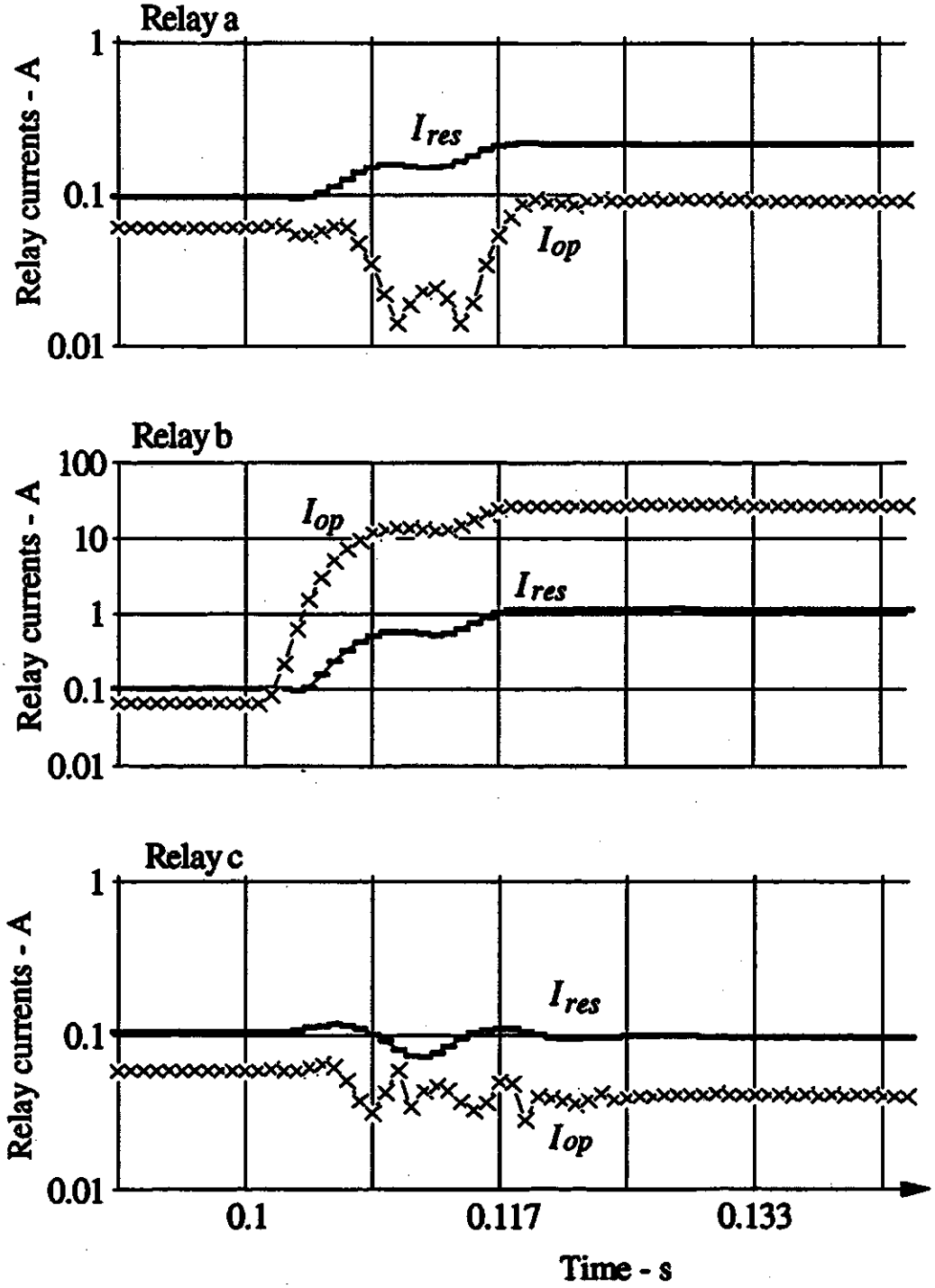

Figure E.8. Operating and restraining currents in the master relay of Circuit 1 for a b-g fault at Q_1.
I_{op} - Operating current,
I_{res} - Restraining current.

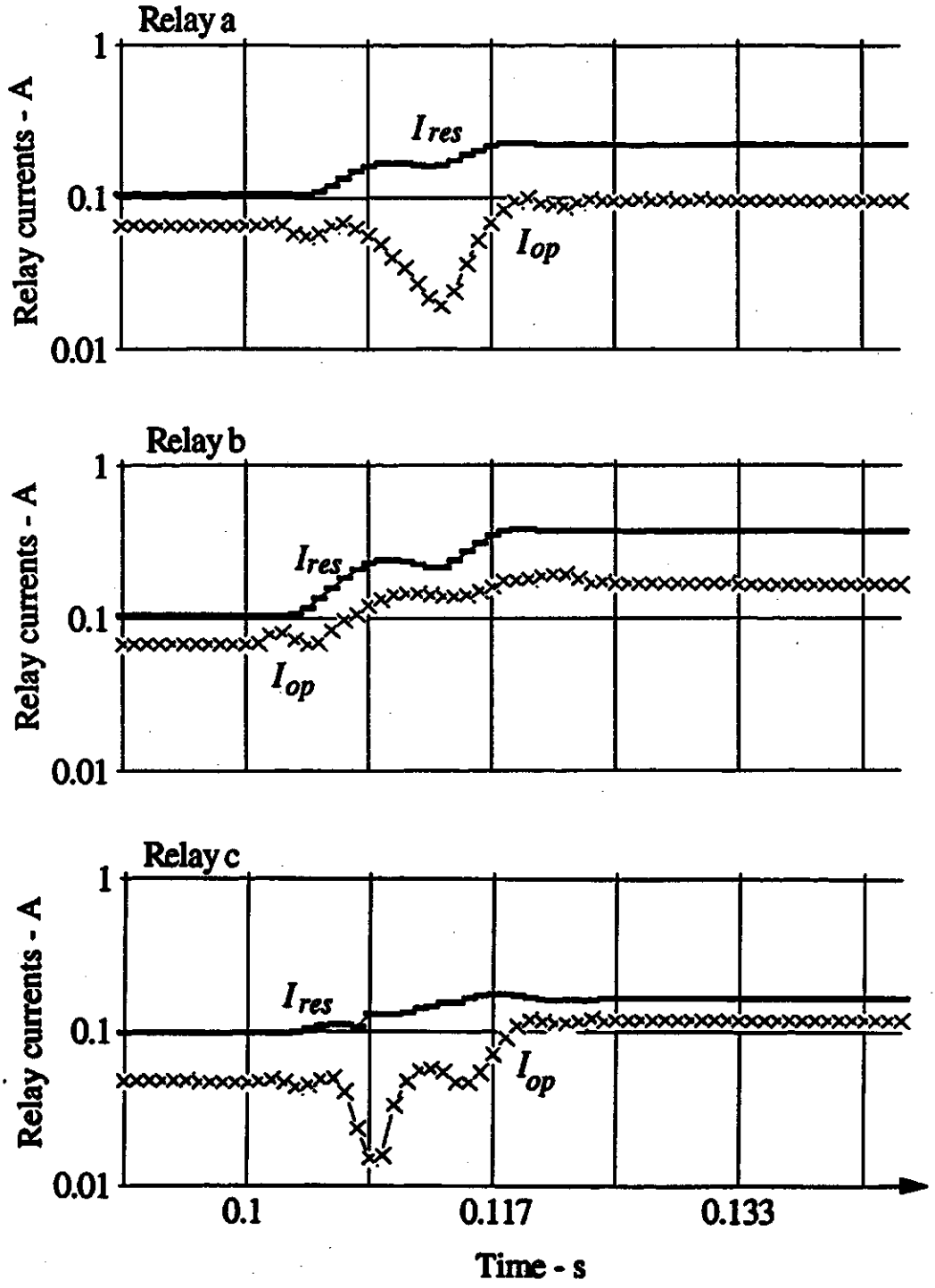

Figure E.9. Operating and restraining currents in the master relay of Circuit 2 for a b-g fault at Q_1.
I_{op} - Operating current,
I_{res} - Restraining current.

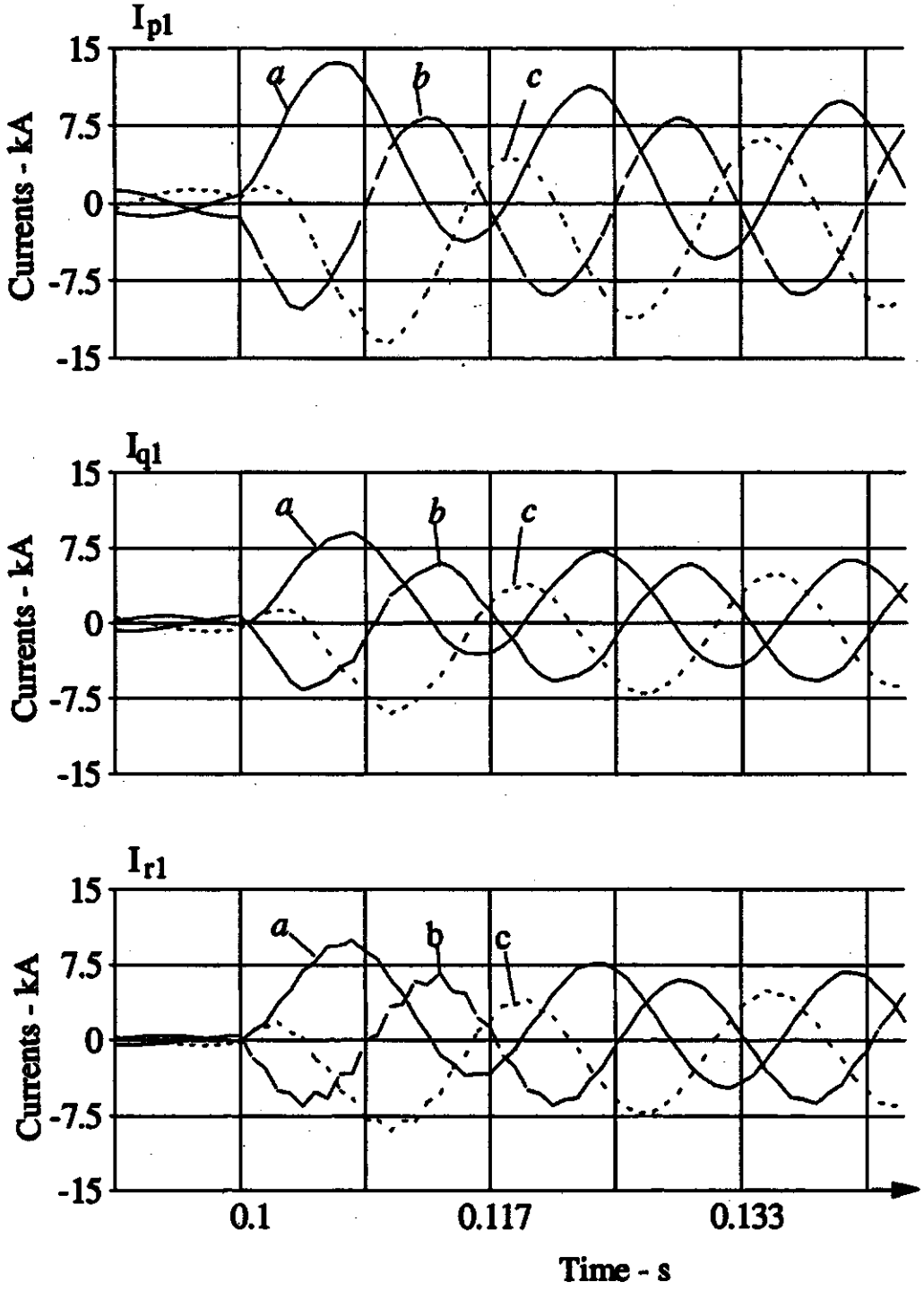

Figure E.10. Waveforms of currents in Circuit 1 for a 3-phase fault at T_1.

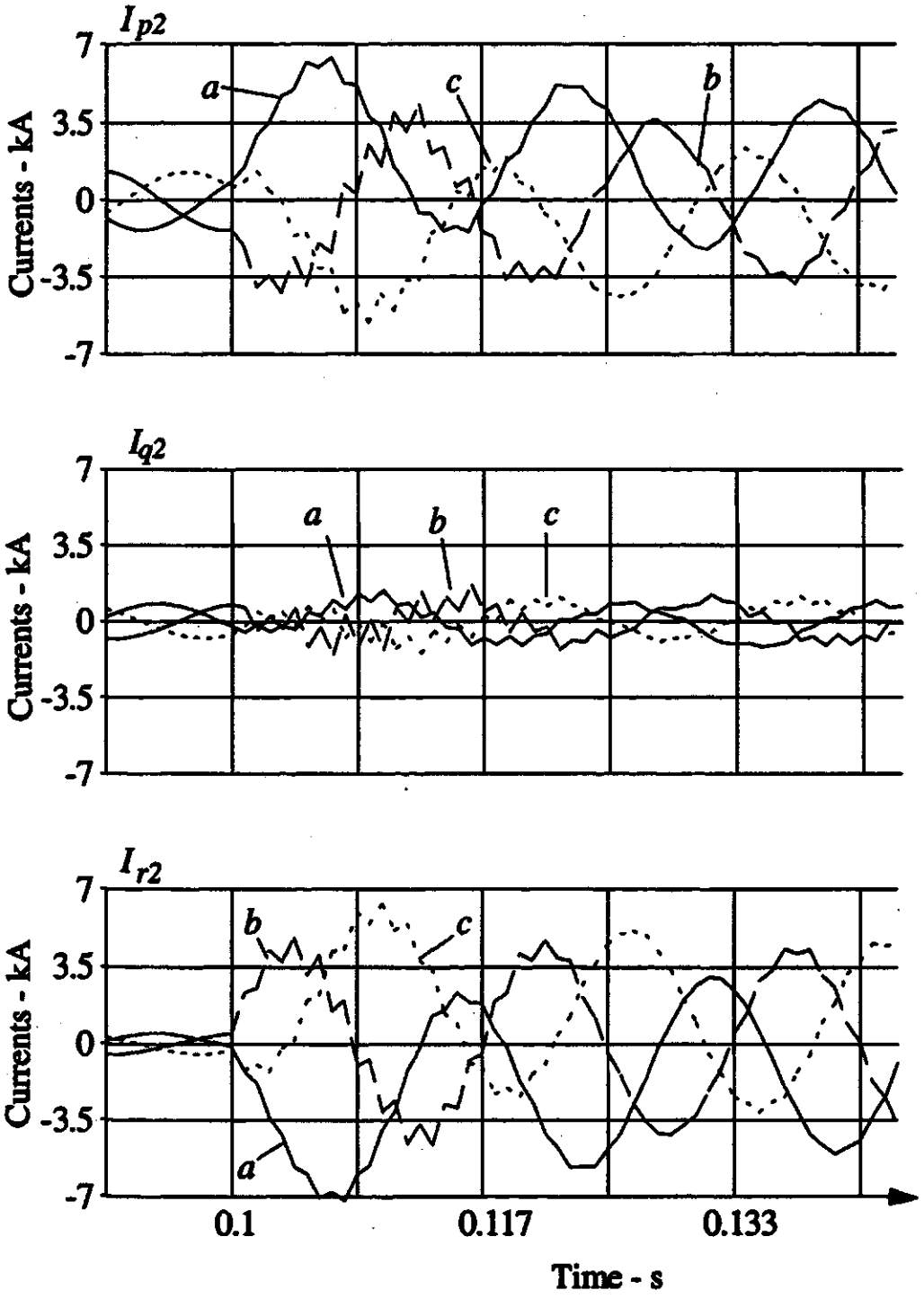

Figure E.11. Waveforms of currents in Circuit 2 for a 3-phase fault at T_1.

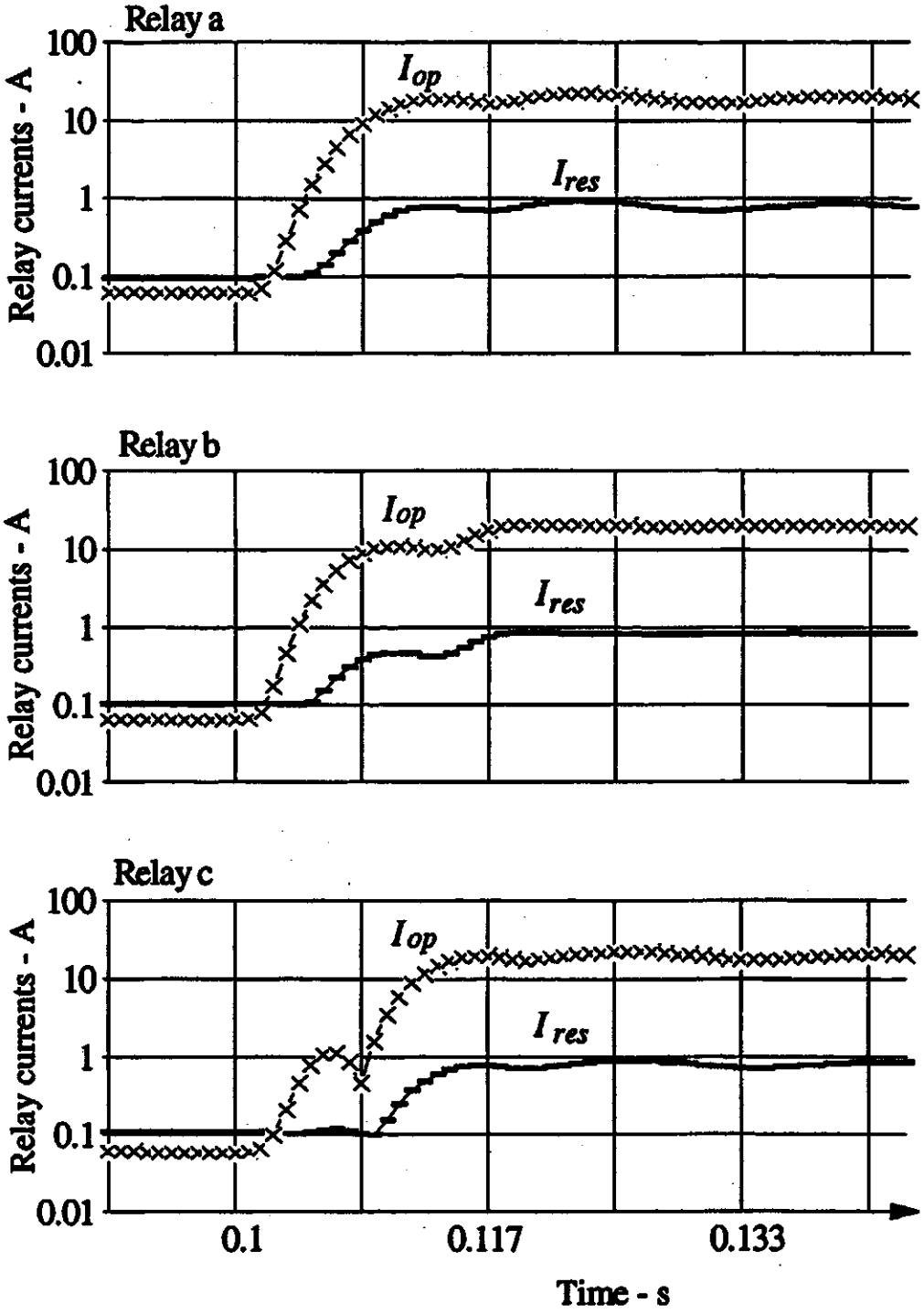

Figure E.12. Operating and restraining currents in the master relay of Circuit 1 for a 3-phase fault at T_1.
I_{op} - Operating current,
I_{res} - Restraining current.

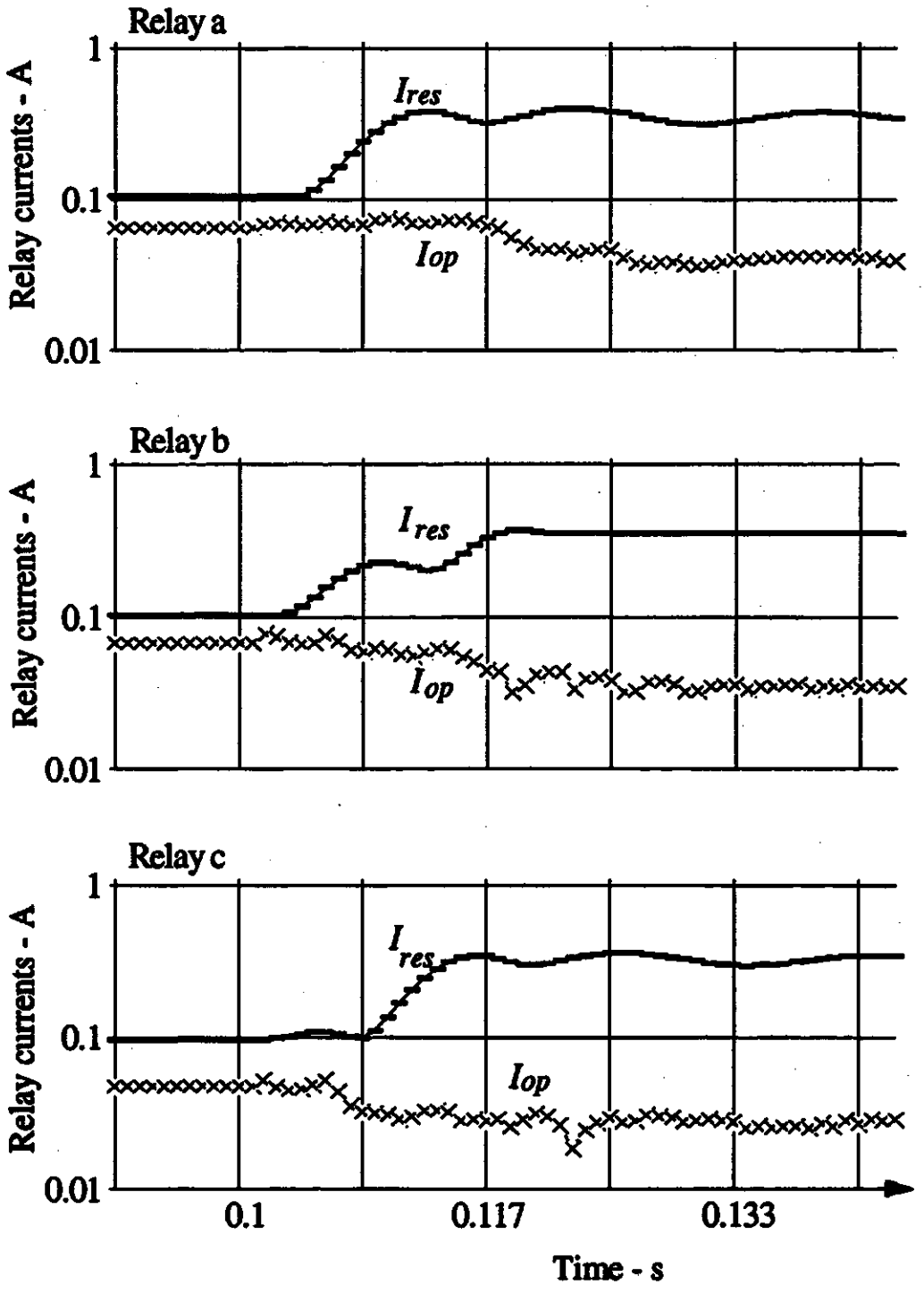

Figure E.13. Operating and restraining currents in the master relay of Circuit 2 for a 3-phase fault at T_1.
I_{op} - Operating current,
I_{res} - Restraining current.

Appendix F. Additional Results of Fault Case Studies for 345 kV Lines

The results included in this section are selected from the simulation studies on 345 kV PTTLs. Table F.1 lists the fault conditions and the corresponding waveforms. The system configurations for these case studies were based on the system shown in Figure 7.7; but the switch states in this system were changed in each cases to create special system conditions in order to examine the performance of the algorithm. These changes are defined in Table F.2. The connections of fault resistance of the two high resistance faults, shown in Figures F.17 to F.20 and Figures F.21 to F.24, are shown in Figures F.25(a) and F.25(b) respectively.

Table F.1. Lists of figures and corresponding fault case studies.

Number of Figures	Fault type and location	Line connection
Figures F.1 - 4	A cross-circuit Fault of a_1-b_1-b_2-c_2 at T_1/T_2.	Configuration 3
Figures F.5 - 8	A cross-circuit Fault of c_1-b_2 at R_1/R_2.	Configuration 4
Figures F.9 - 12	An a-c fault at Q_1 with current outflow at R.	Configuration 5
Figures F.13 - 16	An a-g fault at P_0.	Configuration 6
Figures F.17 - 20	An a-c-g fault with at Q_1 with high resistance	Configuration 2
Figures F.21 - 24	A b-g fault at R1 with high resistance.	Configuration 1

Table F.2. Specification of system configuration.

Configuration	Lengths of lines PT:QT:RT (km)	Specification referring to Figure 7.7
Configuration 1	20:100:50	All switches closed.
Configuration 2	20:50:50	All switches closed.
Configuration 3	100:100:50	All switches closed.
Configuration 4	20:50:5	All switches closed.
Configuration 5	20:100:50	Switch at terminal P of Circuit 2 opened.
Configuration 6	20:50:5	Switch at terminal Q of Circuit 2 opened.

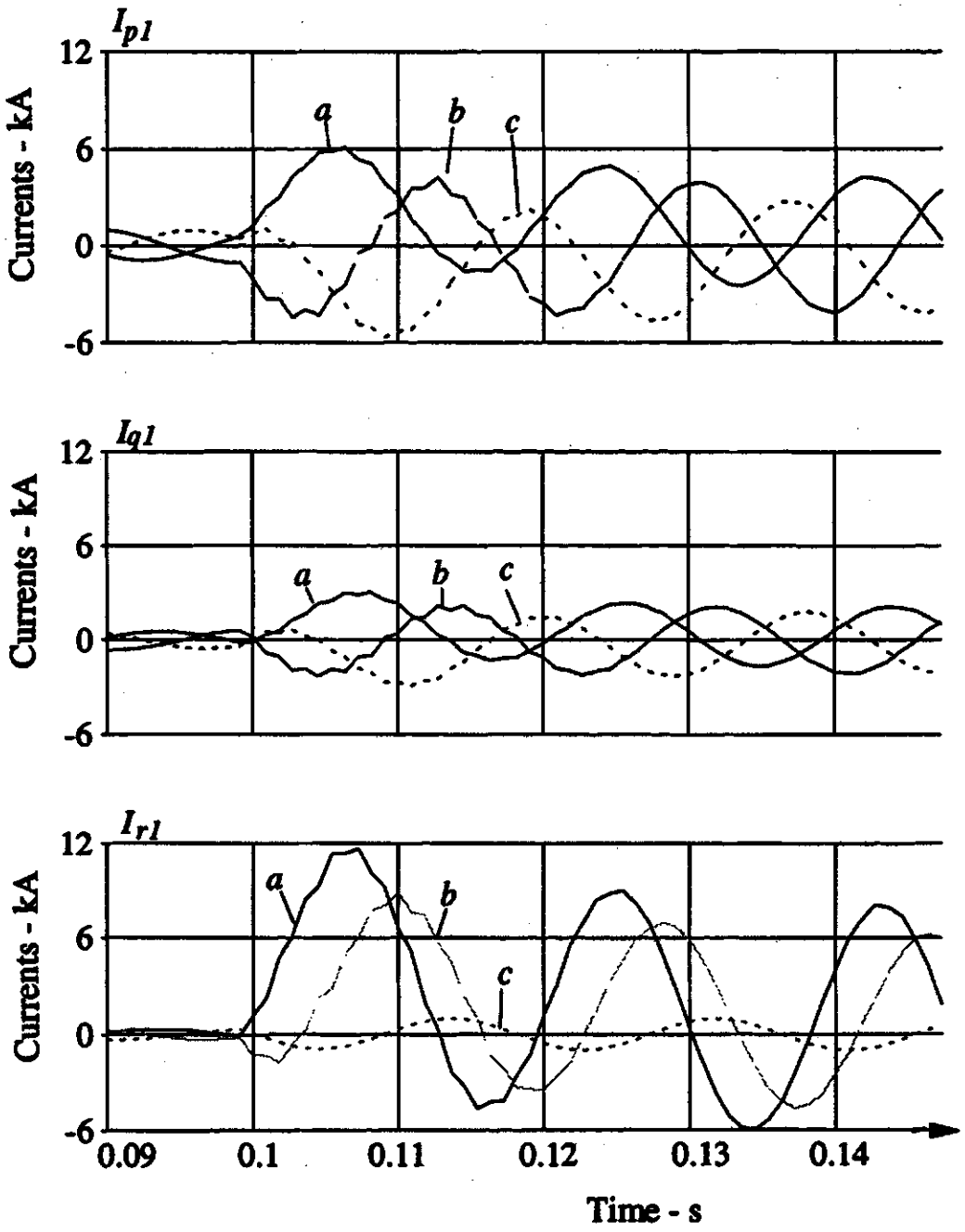

Figure F.1. Waveforms of currents in Circuit 1 for a cross circuit fault of a_1-b_1-b_2-c_2 at T_1/T_2).

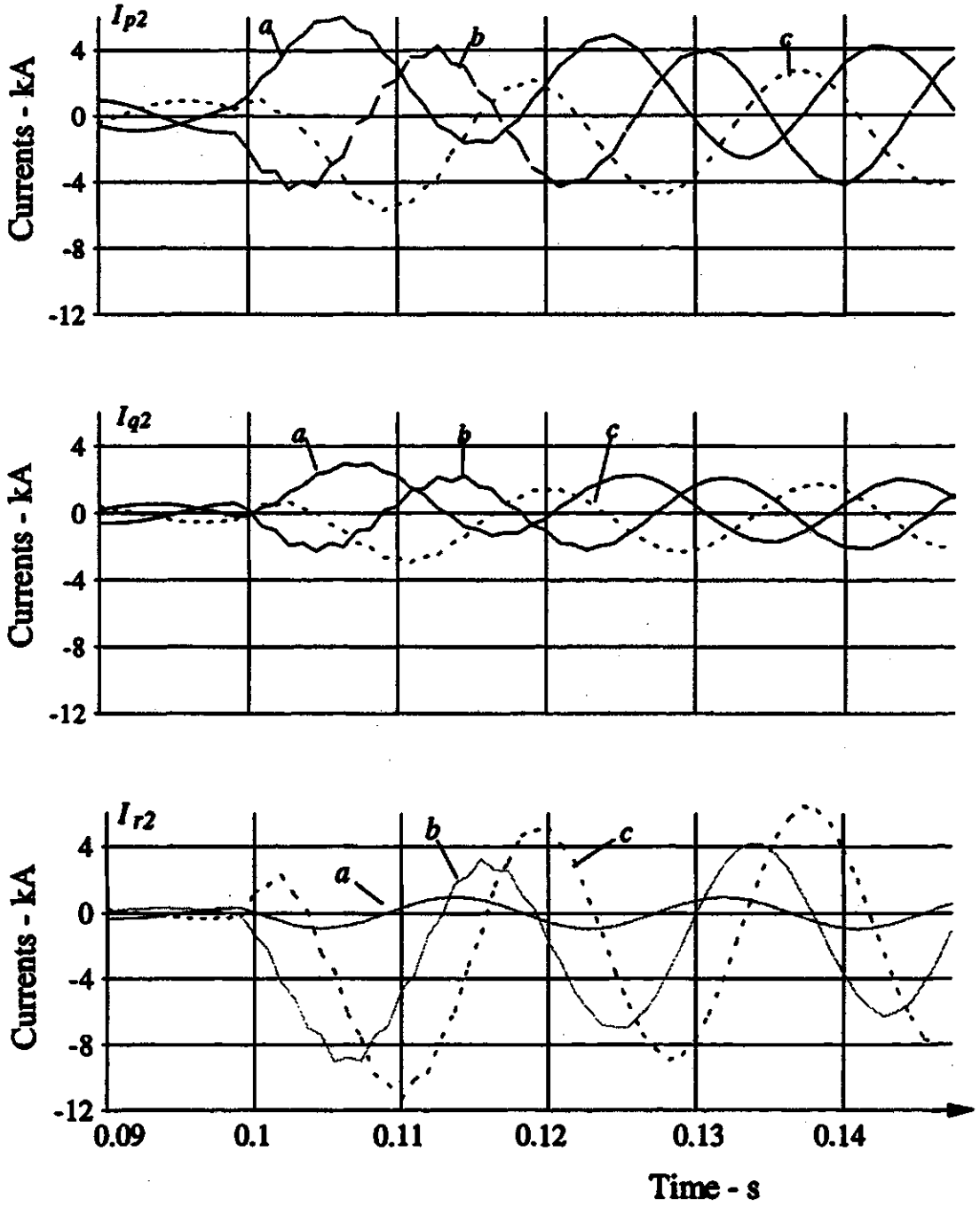

Figure F.2. Waveforms of currents in Circuit 2 for a cross circuit fault of a_1-b_1-b_2-c_2 at T_1/T_2).

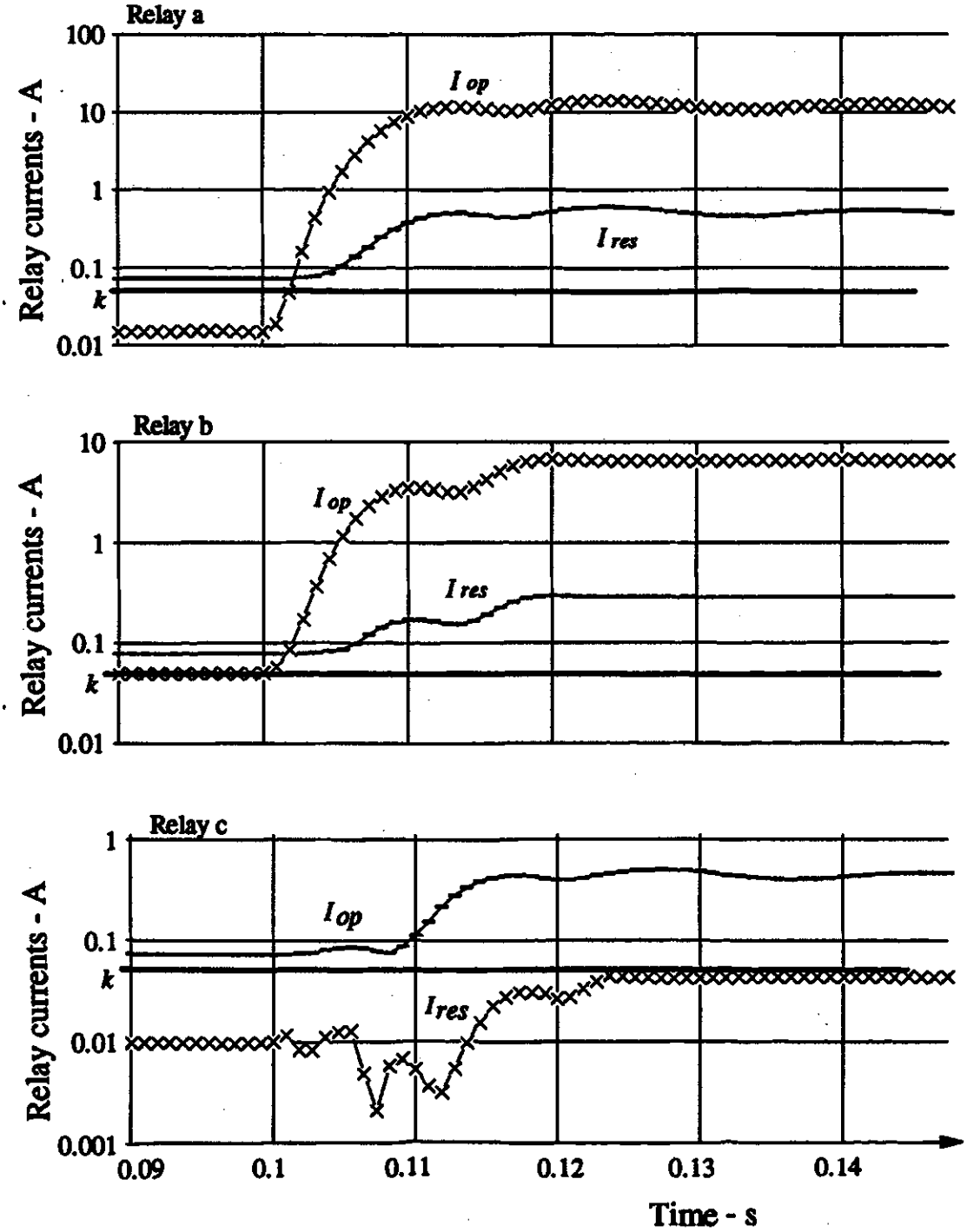

Figure F.3 Operating and restraining currents in the master relay of Circuit 1 for a cross circuit fault of a_1-b_1-b_2-c_2 at T_1/T_2.

I_{op}: operating current.

I_{res}: restraining current.

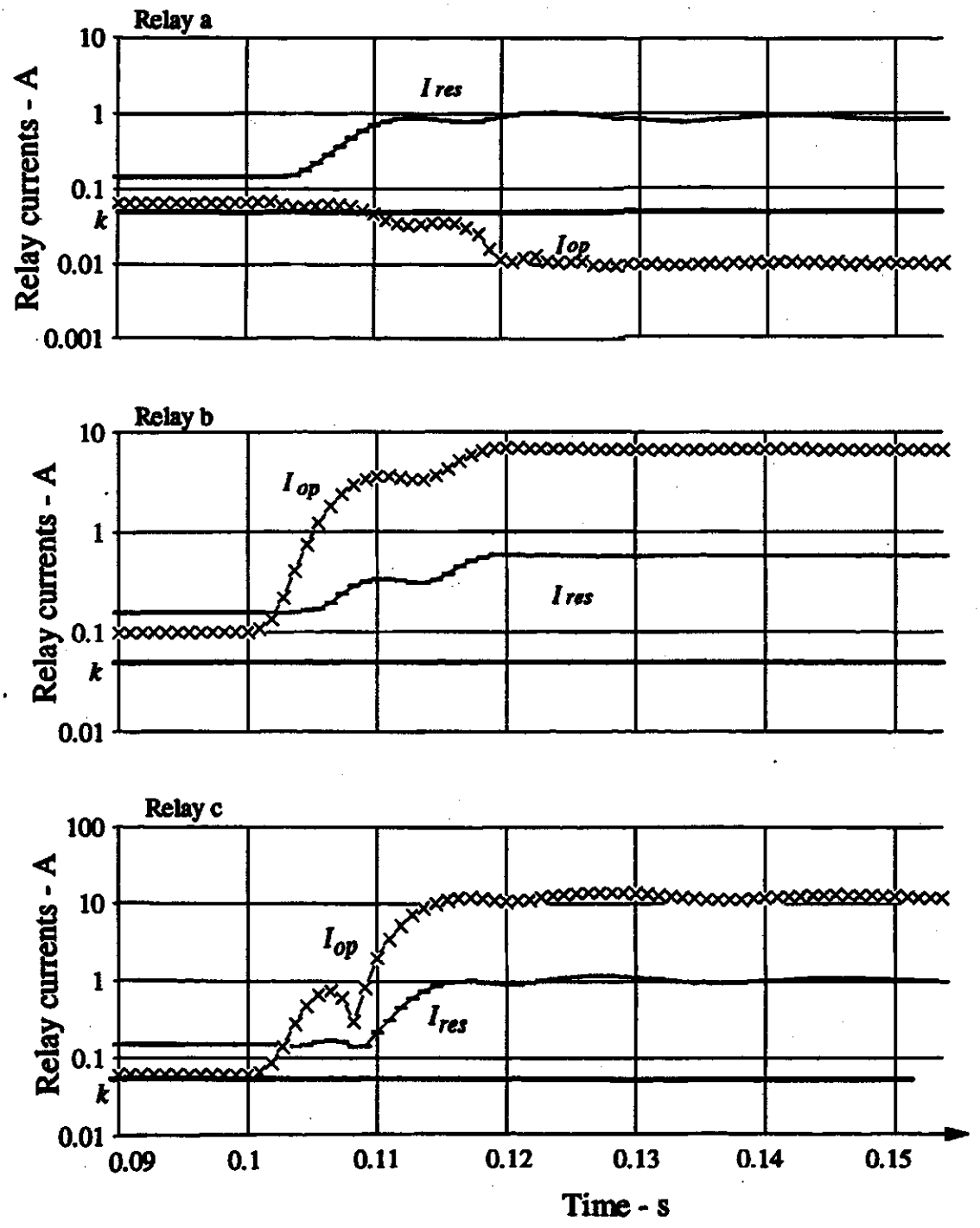

Figure F.4. Operating and restraining currents in the master relay of Circuit 2 for a cross circuit fault of a_1-b_1-b_2-c_2 at T_1/T_2.

I_{op}: operating current

I_{res}: restraining current.

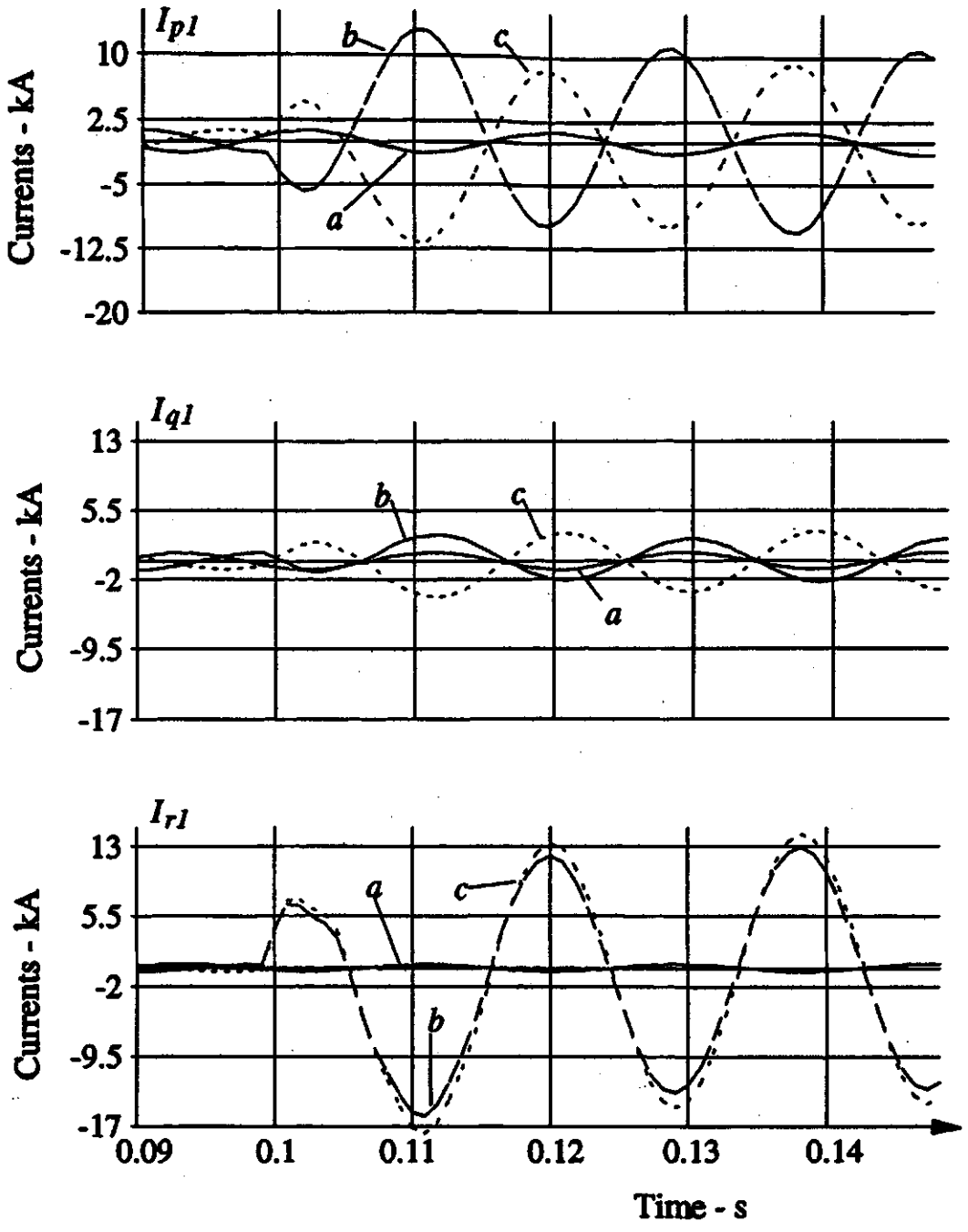

Figure F.5. Waveforms of Currents in Circuit 1 for a cross-circuit fault of c_1-b_2 at R_1/R_2.

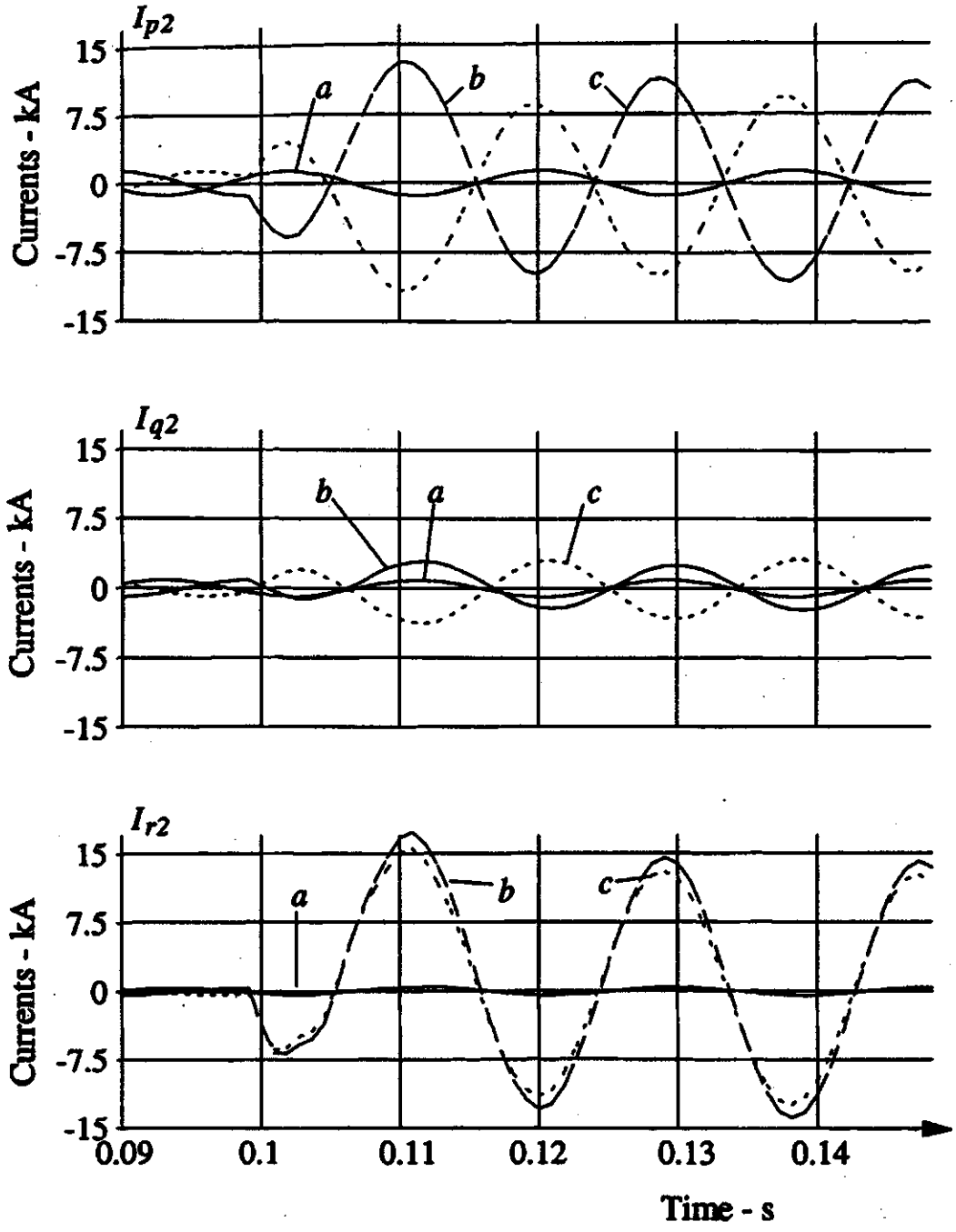

Figure F.6 Waveforms of currents in Circuit 2 for a cross-circuit fault of c_1-b_2 at R_1/R_2.

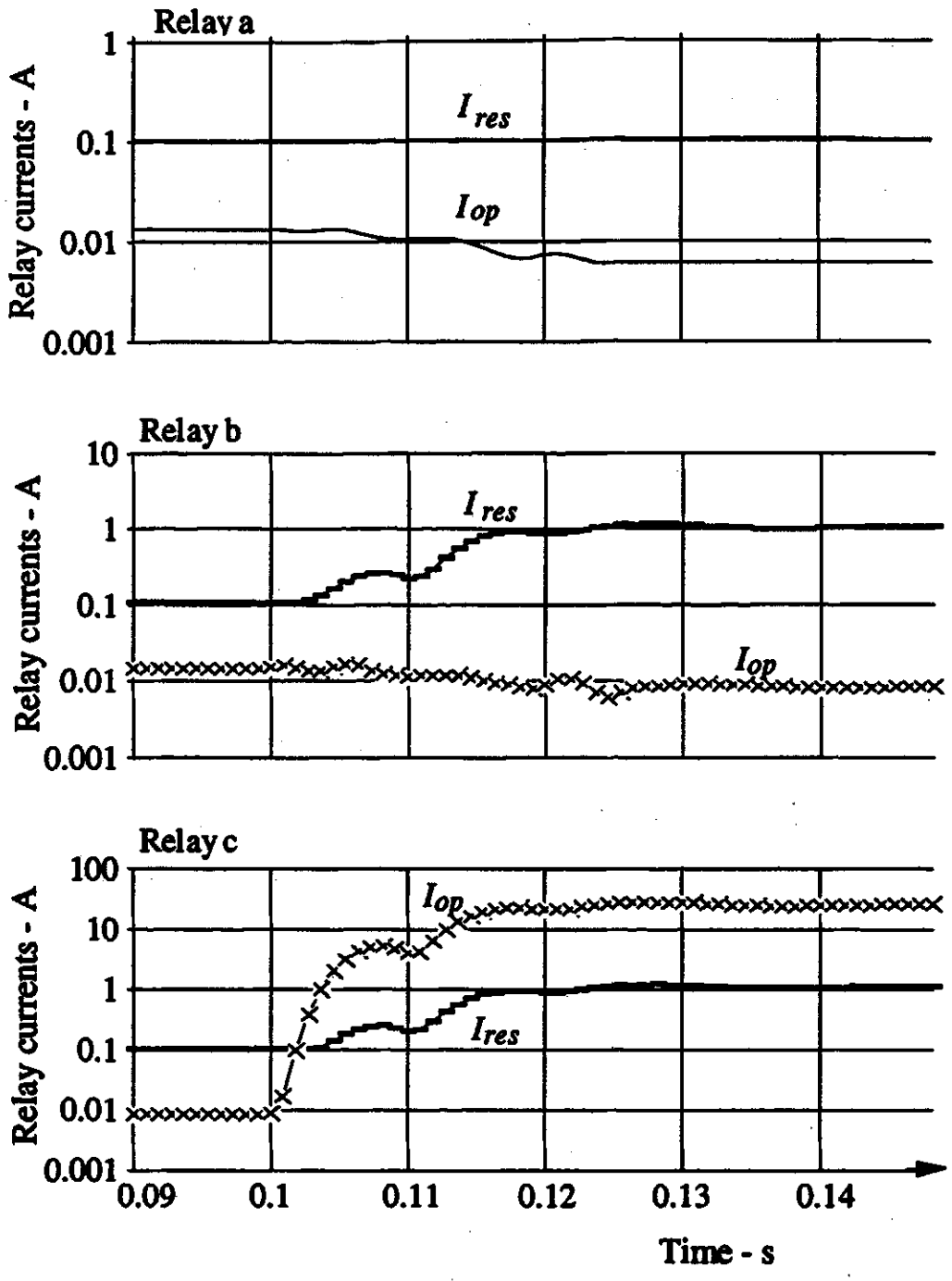

Figure F.7 Operating and restraining currents in the master relay of Circuit 1 for a cross-circuit fault of c_1-b_2 at R_1/R_2.
I_{op}: operating current
I_{res}: restraining current.

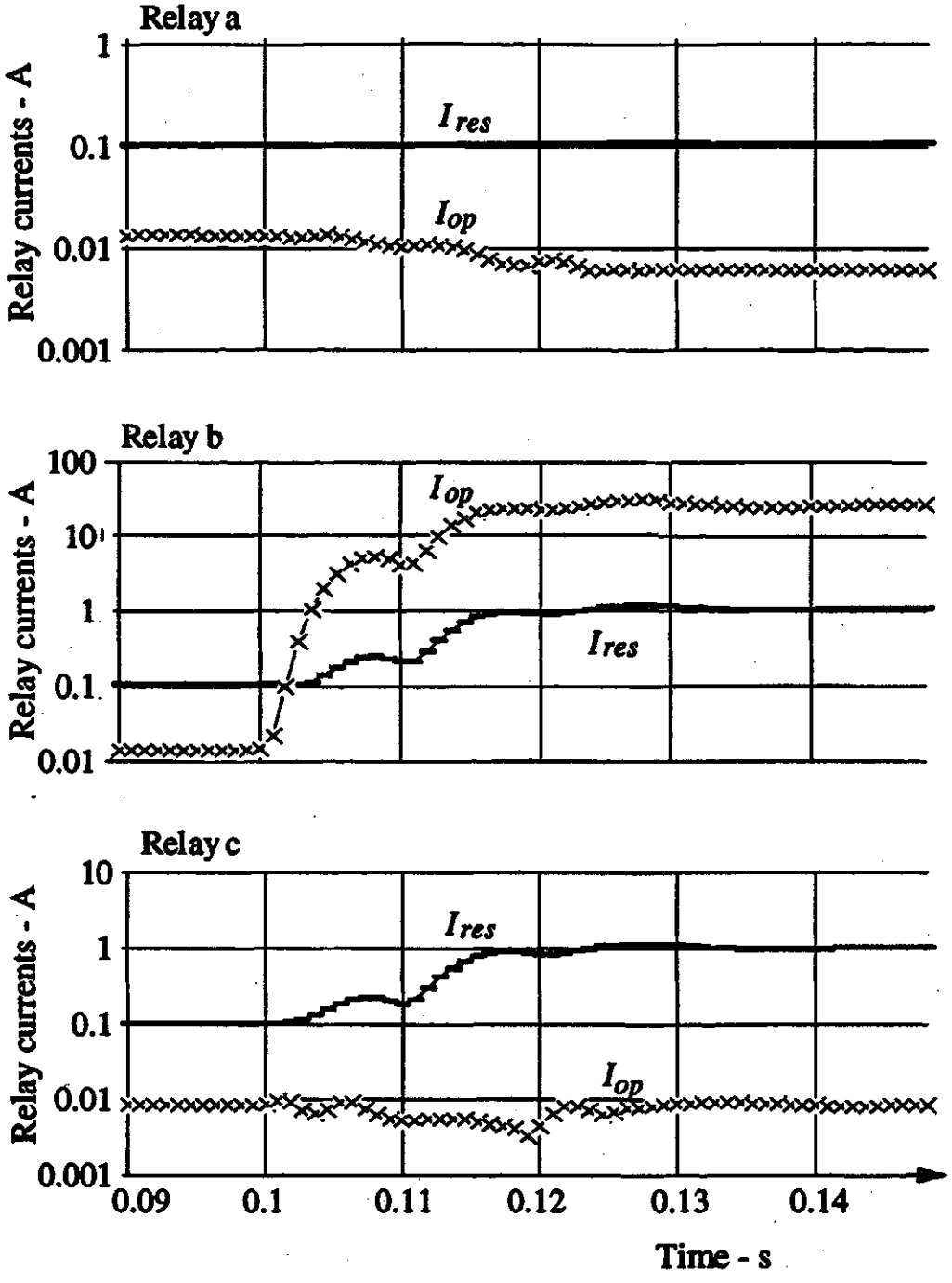

Figure F.8 Operating and restraining currents in the master relay of Circuit 2 for a cross-circuit fault of c_1-b_2.

I_{op}: operating current

I_{res}: restraining current.

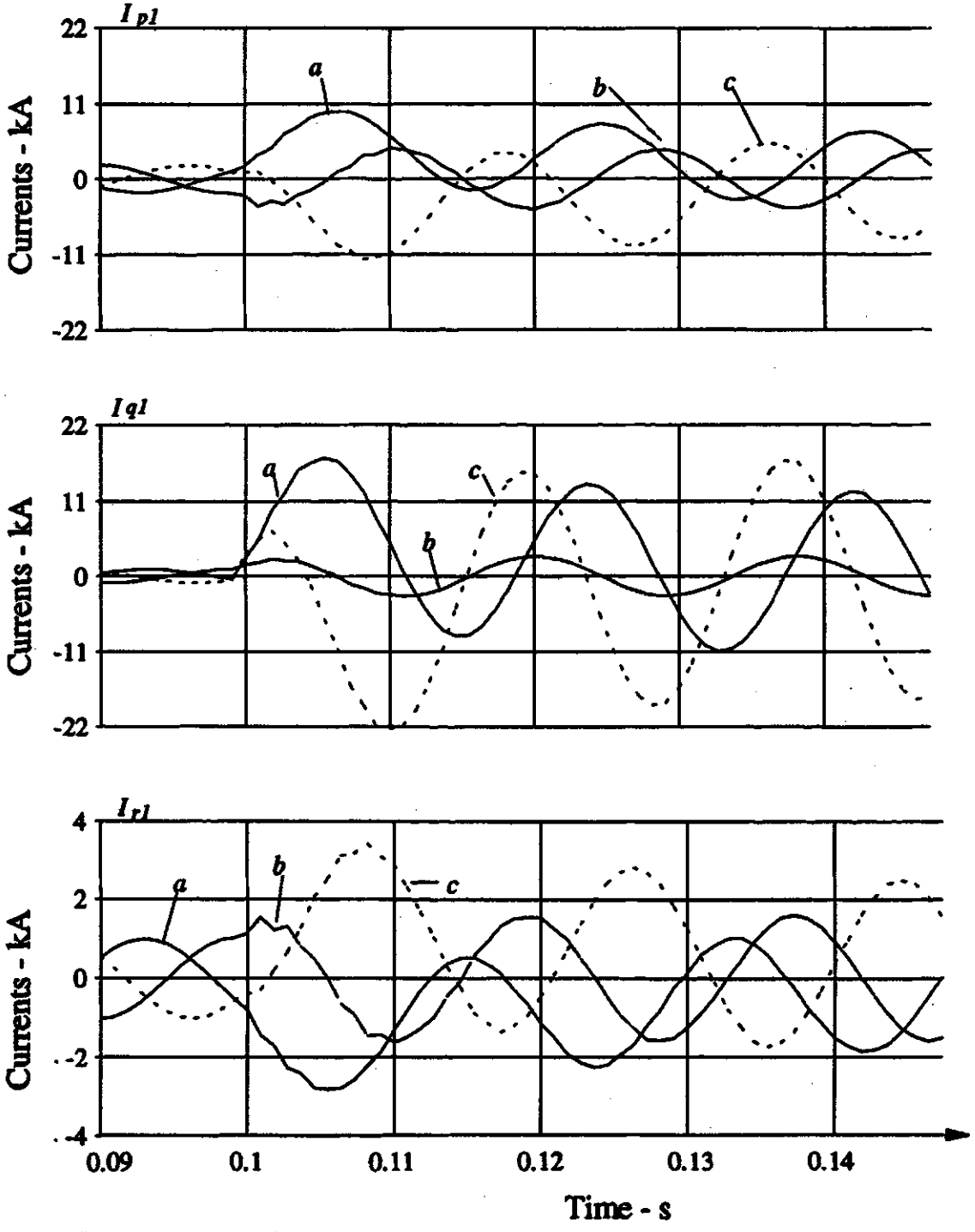

Figure F.9. Waveforms of currents in Circuit 1 for an a-c fault at Q_1 with outflow at Terminal R.

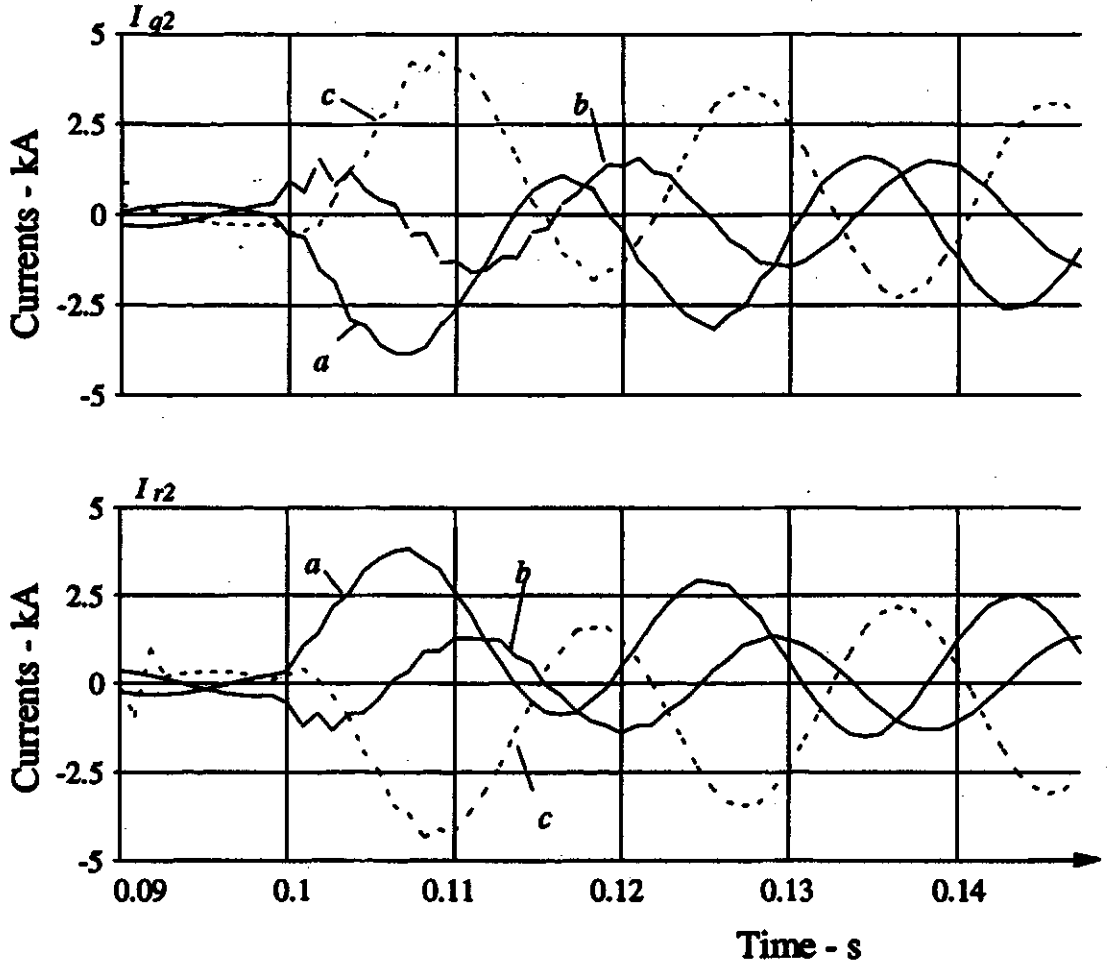

Figure F.10. Waveforms of currents in Circuit 2 for an a-c fault with outflow at Terminal R.

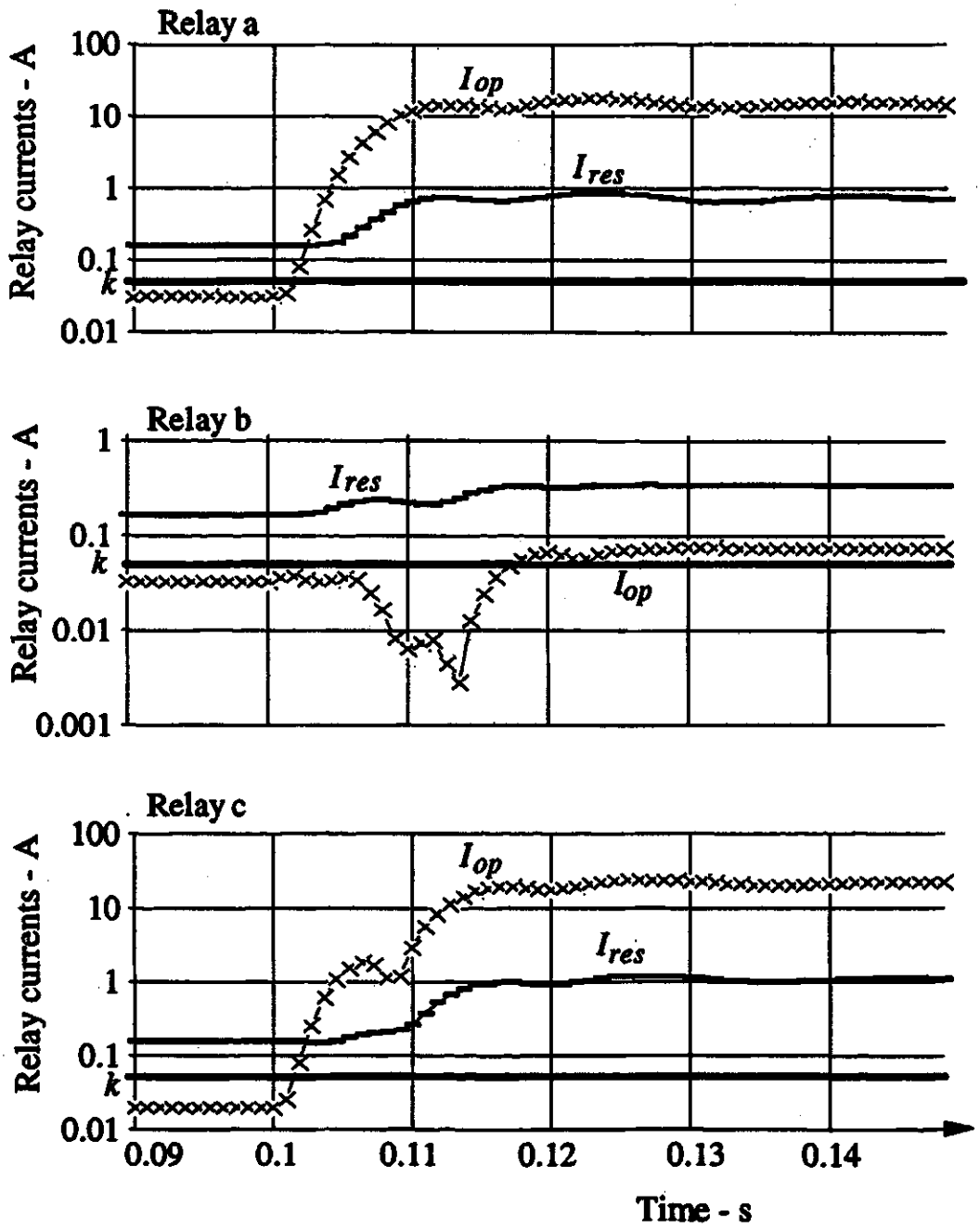

Figure F.11. Operating and restraining currents of the master relay in Circuit 1 for an a-c fault with outflow at Terminal R.

I_{op}: operating current

I_{res}: restraining current.

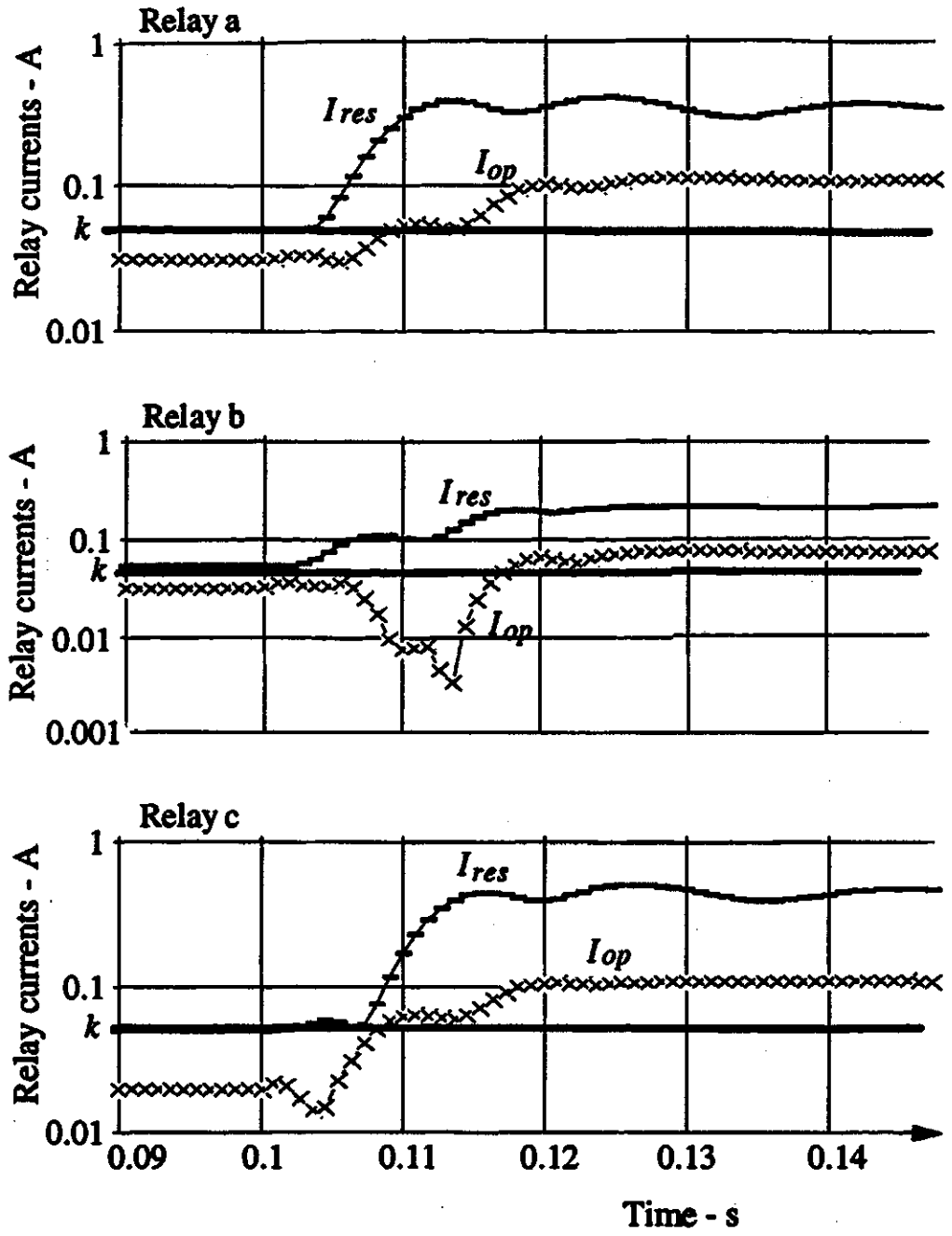

Figure F.12. Operating and restraining currents of the master relay in Circuit 2 for an a-c fault with outflow at Terminal R.

I_{op}: operating current

I_{res}: restraining current.

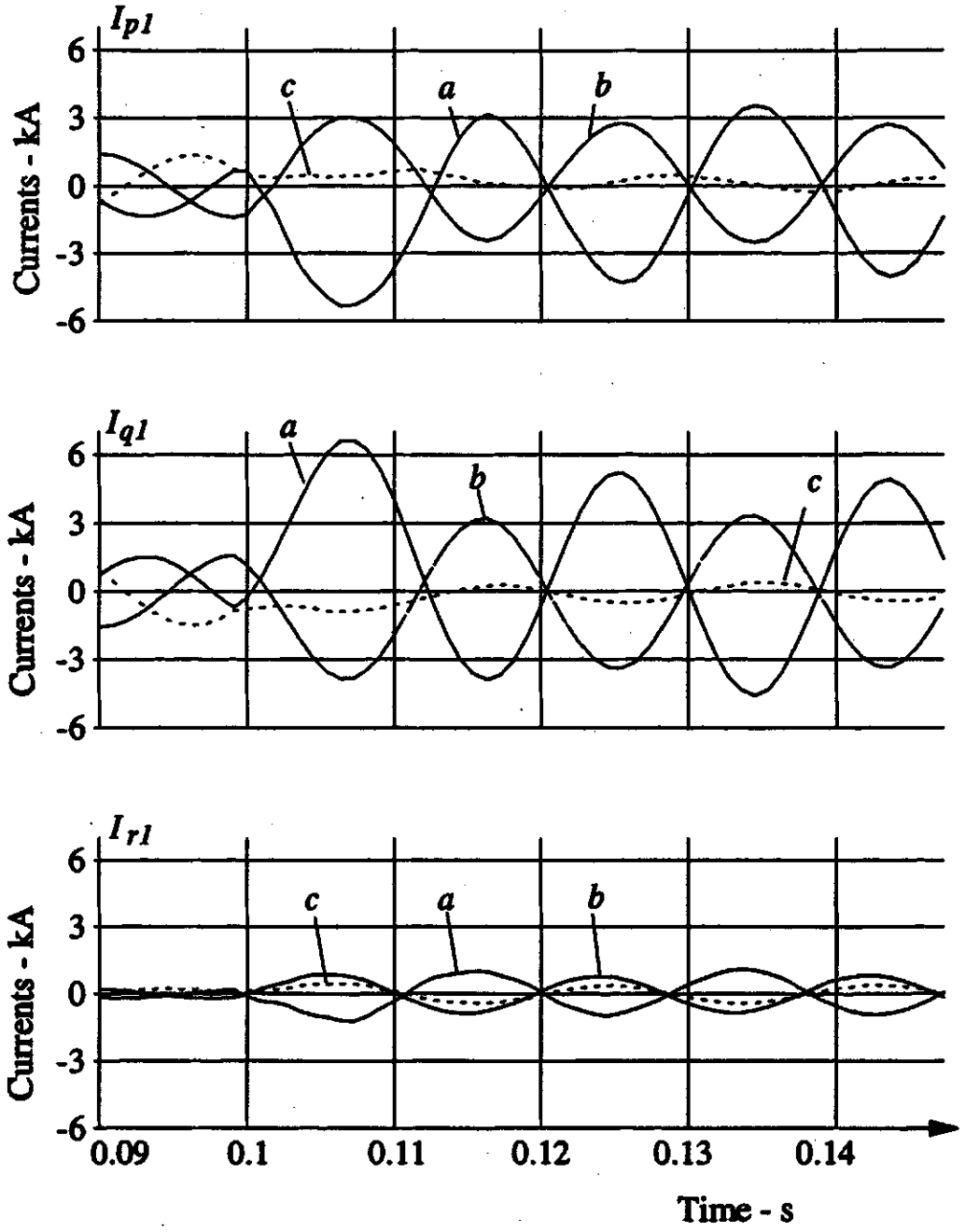

Figure F.13. Waveforms of current in Circuit 1 for an a-g fault at P_0.

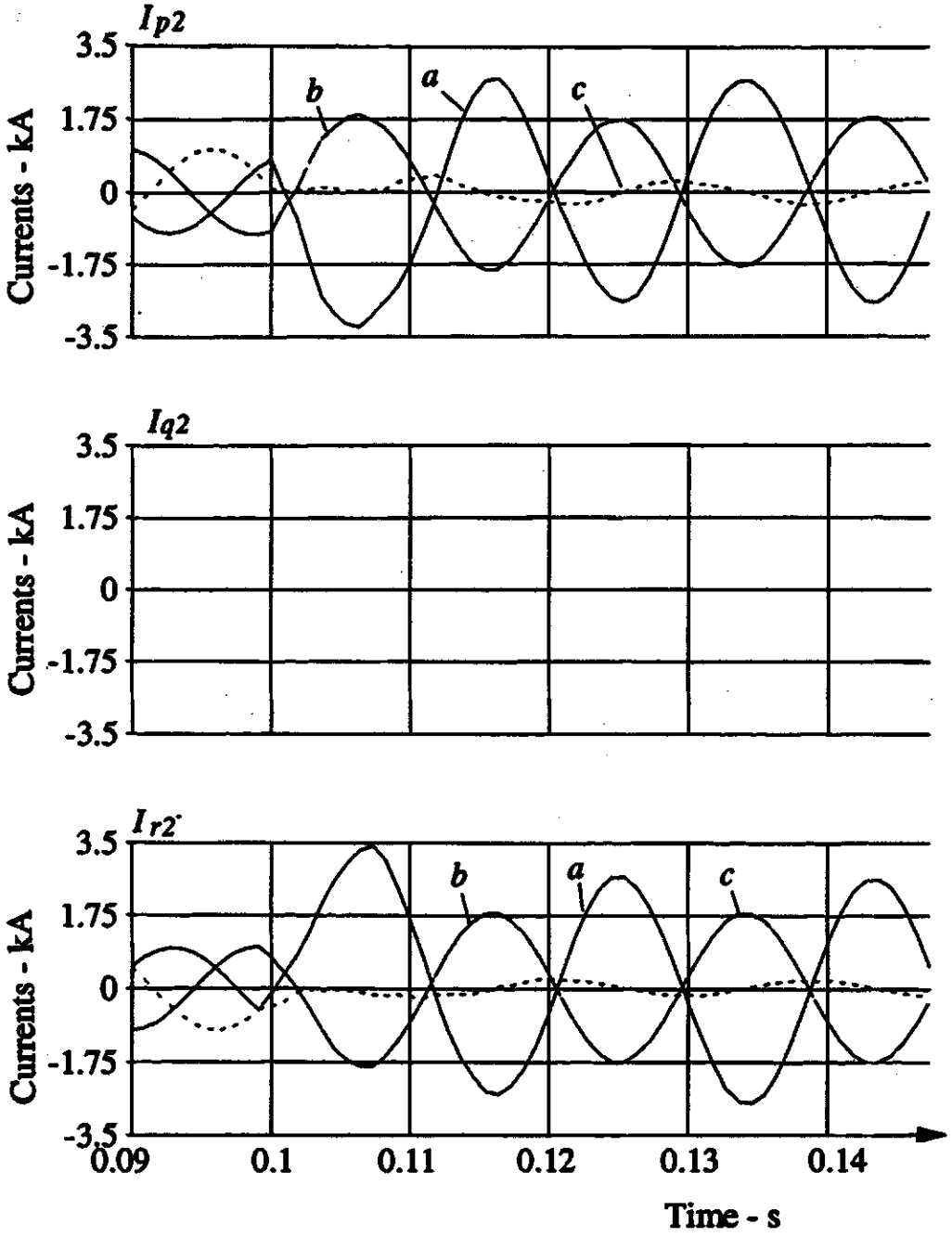

Figure F.14. Waveforms of current in Circuit 2 for an a-g fault at P_0.

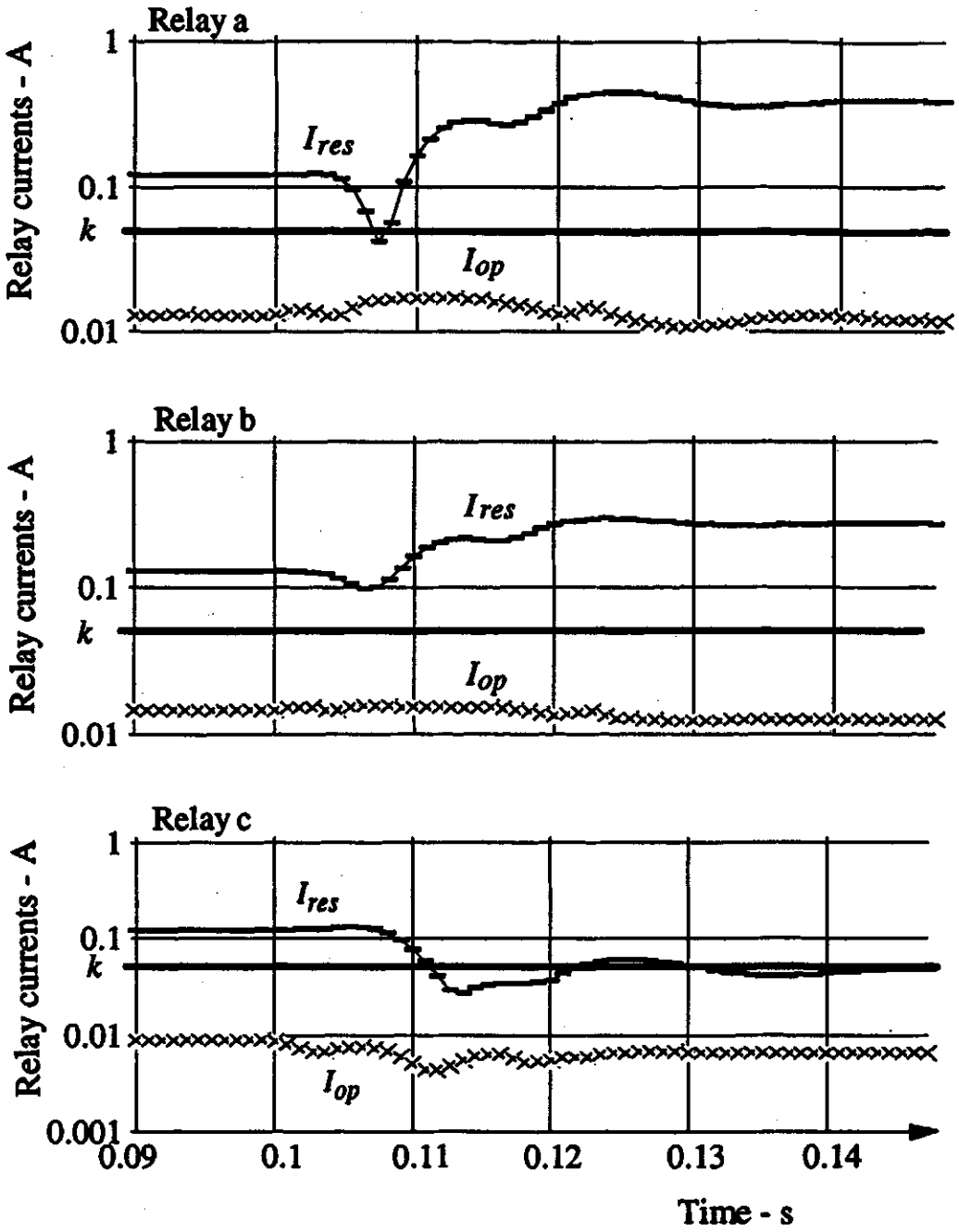

Figure F.15. Operating and restraining currents in the master relay of Circuit 1 for an a-g fault at P_0.

I_{op}: Operating current,

I_{res}: Restraining current.

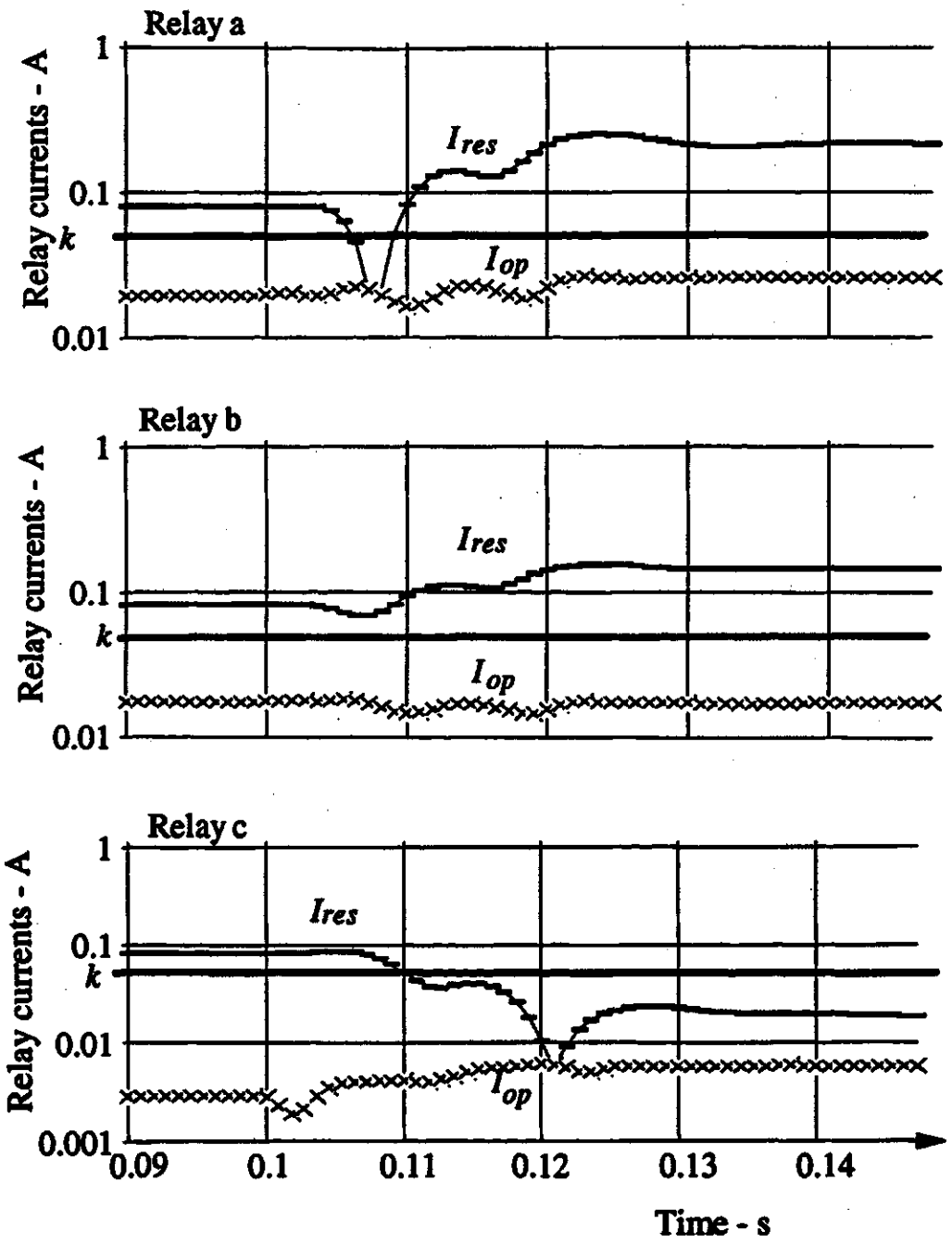

Figure F.16. Operating and restraining currents in the master relay of Circuit 2 for an a-g fault at P_0.

I_{op}: Operating current,

I_{res}: Restraining current.

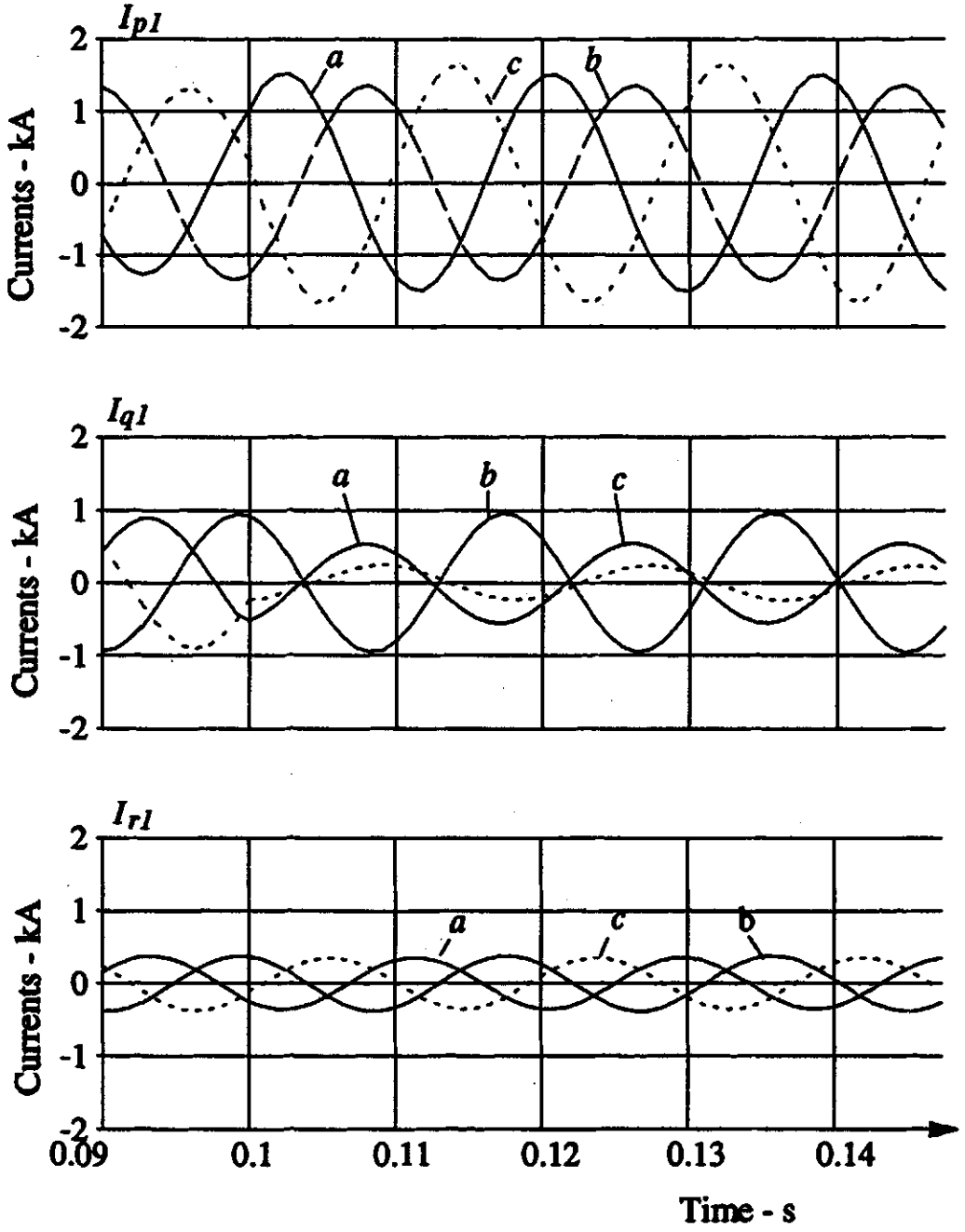

Figure F.17. Waveforms of current in Circuit 1 for an a-c-g fault at Q_1 with arc resistance.
(Ra-c = 2 x 200Ω, Rg = 600 Ω).

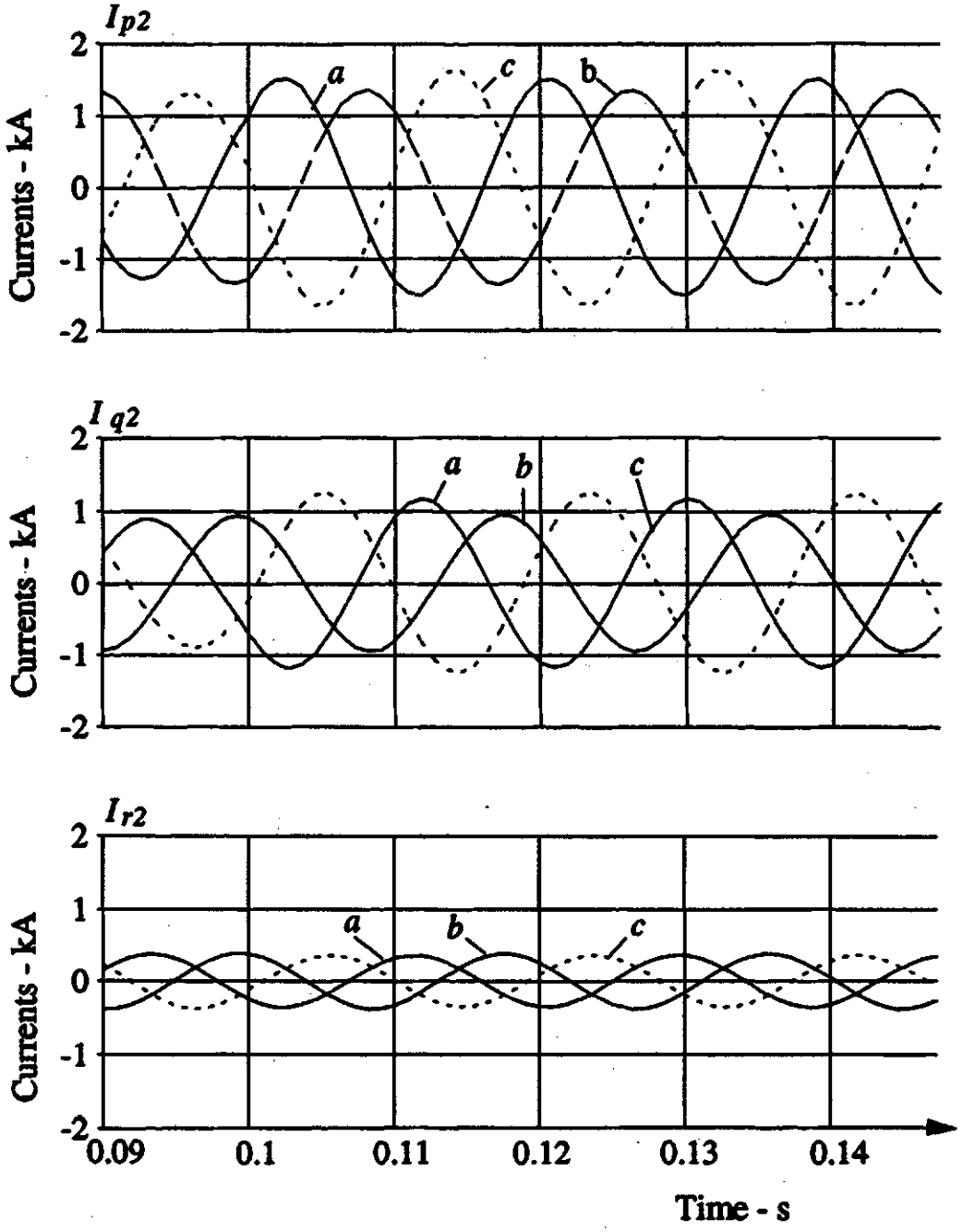

Figure F.18. Waveforms of current in Circuit 2 for an a-c-g fault at Q_1 with arc resistance.
(Ra-c = 2 x 200Ω, Rg = 600 Ω).

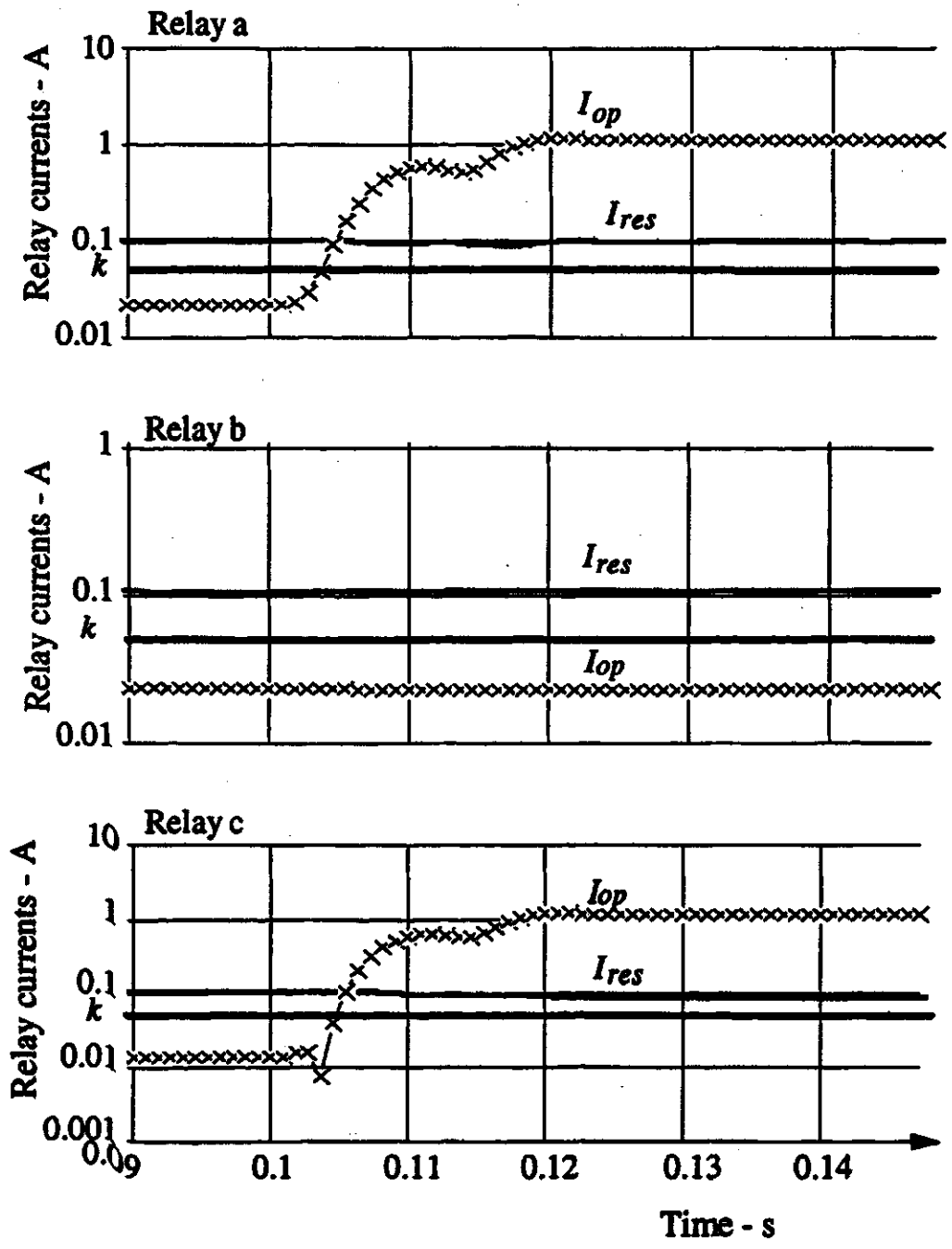

Figure F.19. Operating and restraining currents in the master relay of Circuit 1 for an a-c-g fault at Q_1 with arc resistance.
I_{op} - Operating current,
I_{res} - Restraining current.

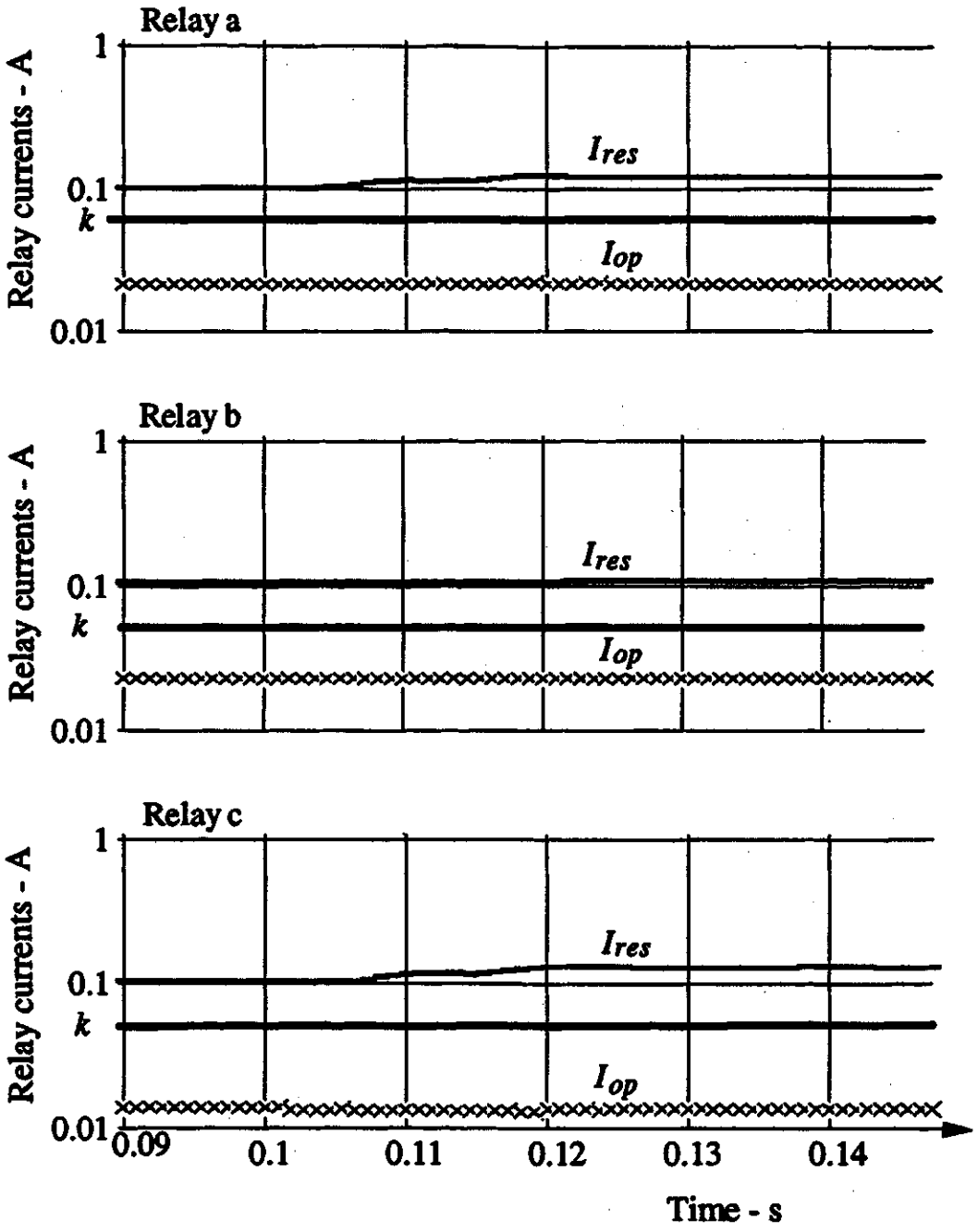

Figure F.20. Operating and restraining currents in the master relay of Circuit 2 for an a-c-g fault at Q_1 with arc resistance.
I_{op} - Operating current,
I_{res} - Restraining current.

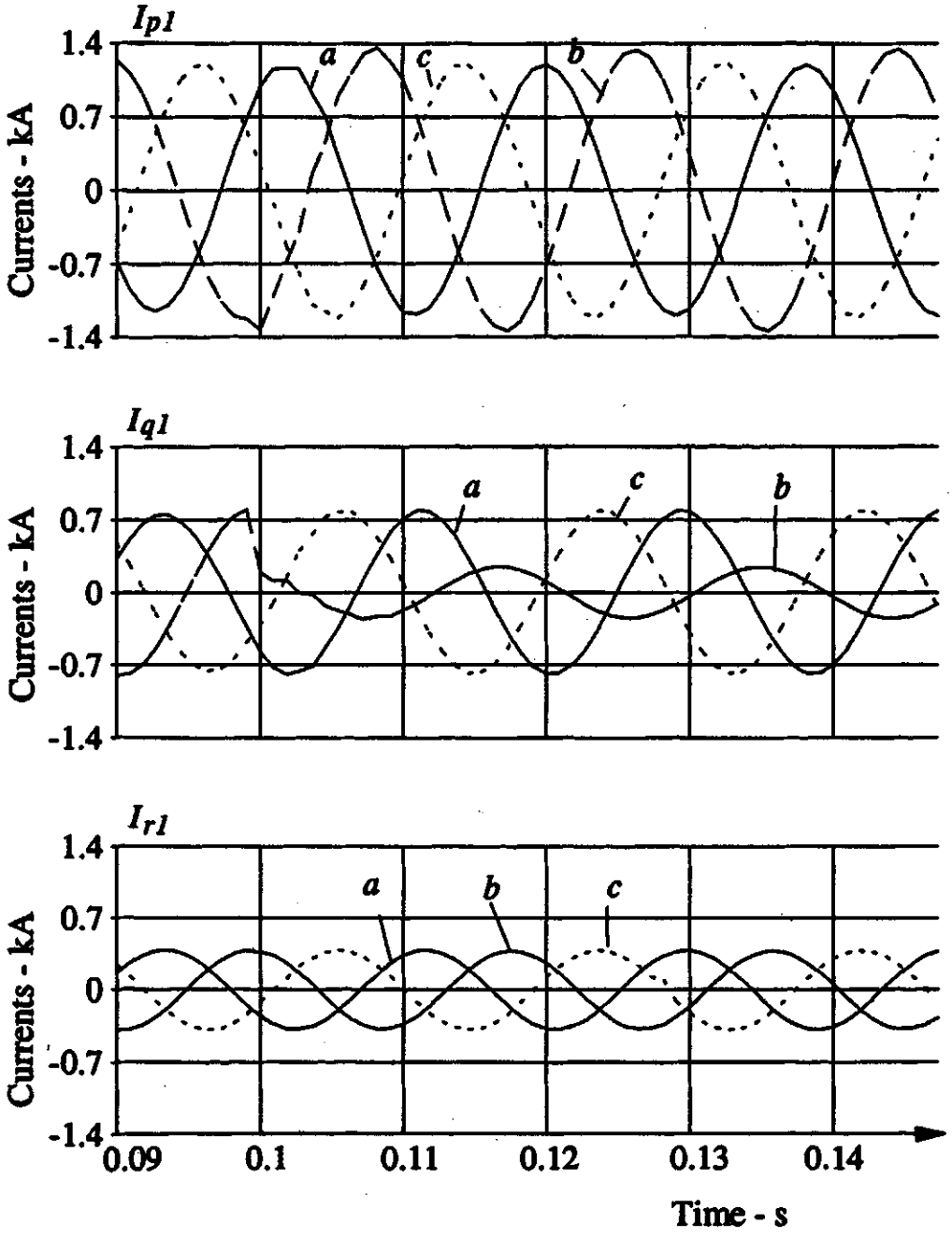

Figure F.21. Waveforms of current in Circuit 1 for a b-g fault at R_1 with 400Ω fault resistance.

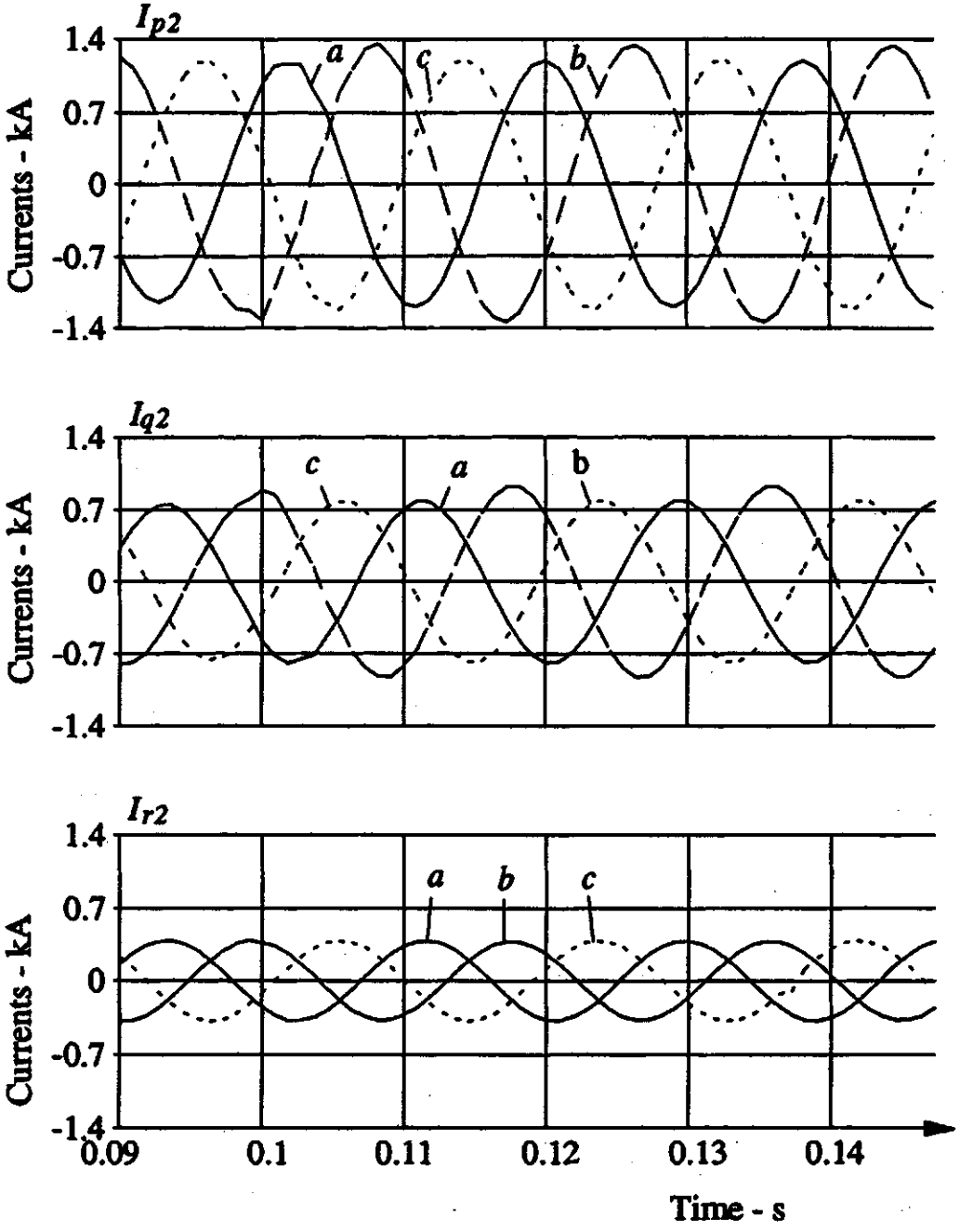

Figure F.22. Waveforms of current in Circuit 2 for a b-g fault at R_1 with 400Ω fault resistance.

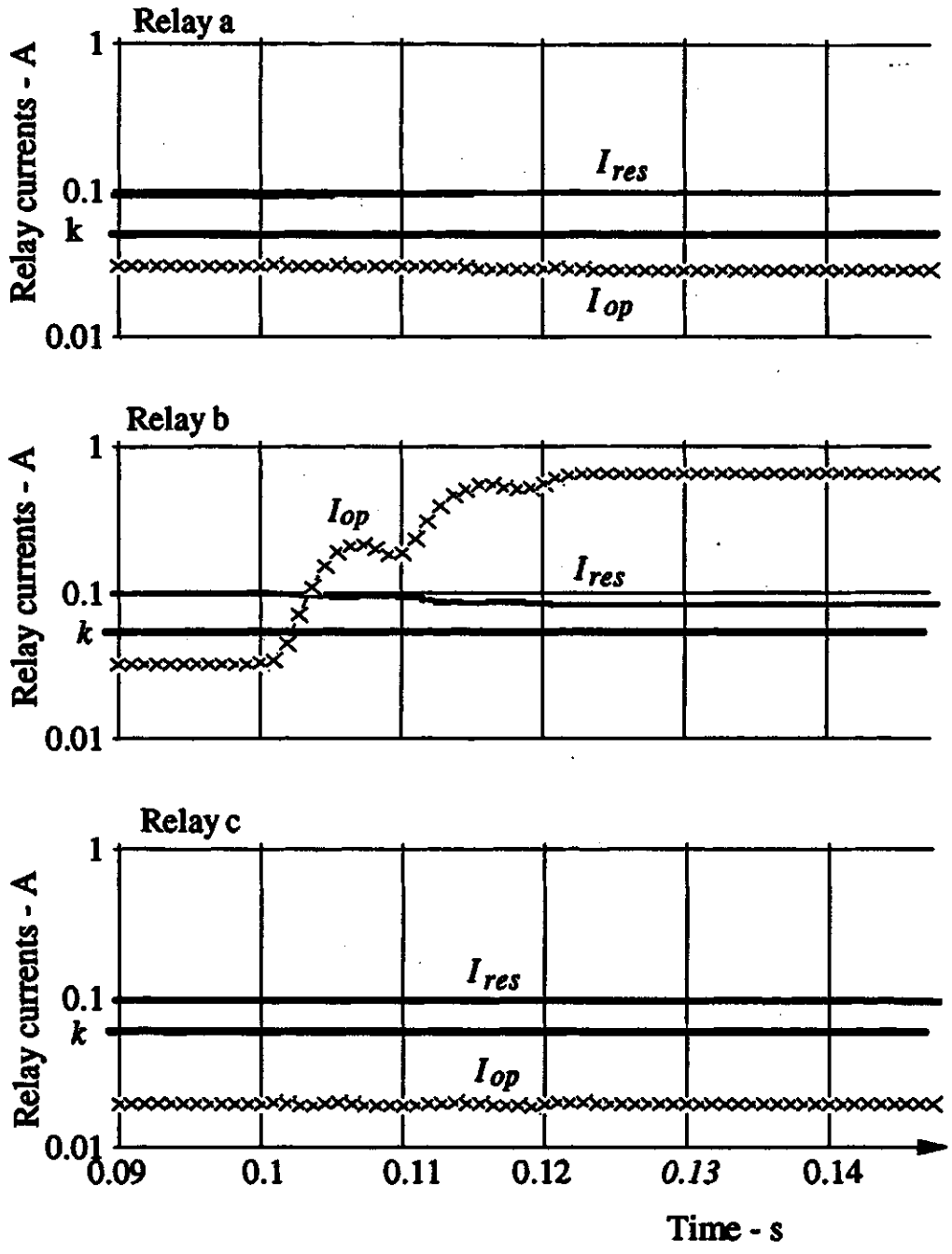

Figure F.23. Operating and restraining currents in the master relay of Circuit 1 for a b--g fault at R_1 with arc resistance of 400 Ω.

I_{op} - Operating current,

I_{res} - Restraining current.

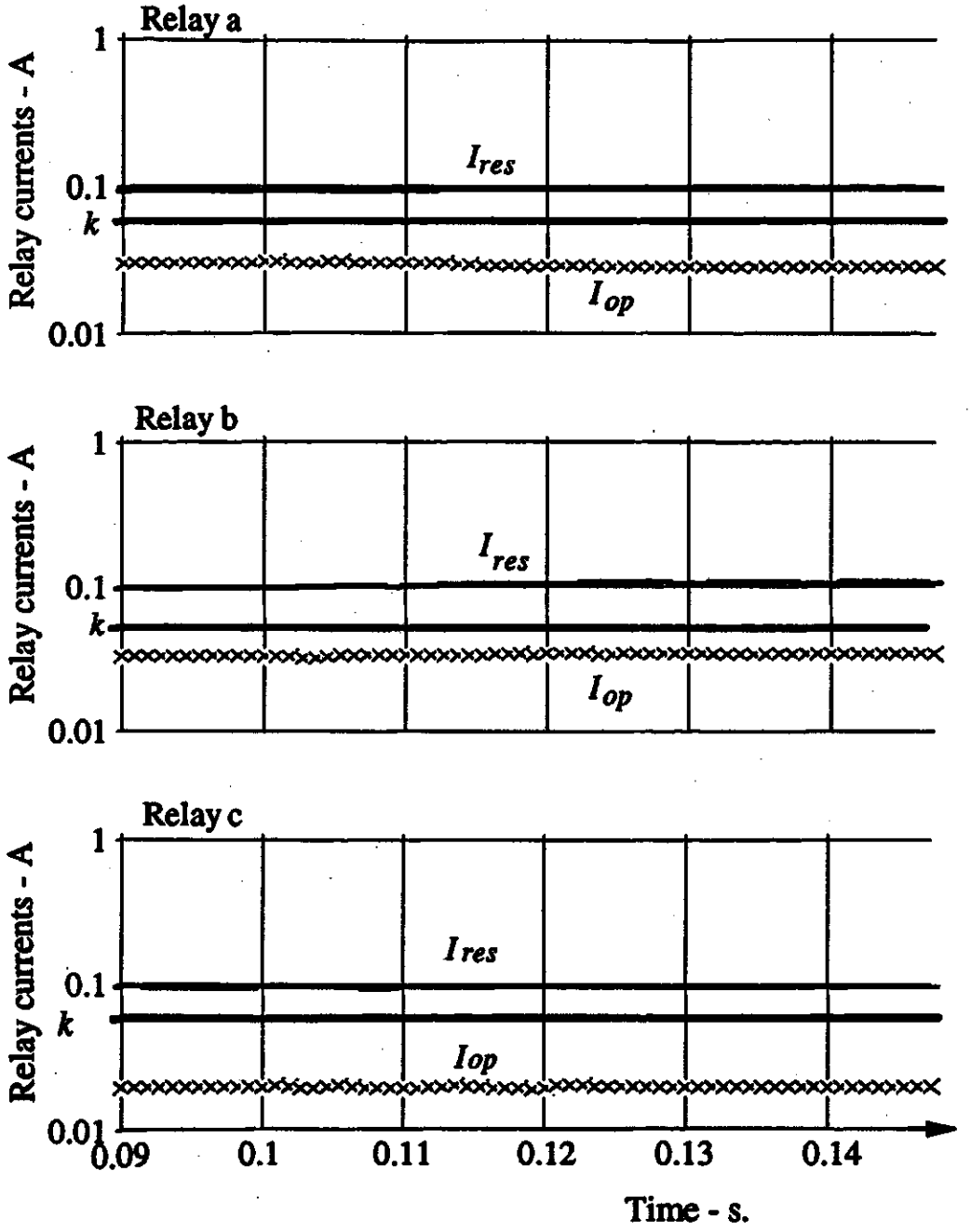

Figure F.24. Operating and restraining currents in the master relay of Circuit 2 for a b--g fault at R_1 with arc resistance of 400 Ω.

I_{op}: Operating current,

I_{res}: Restraining current.

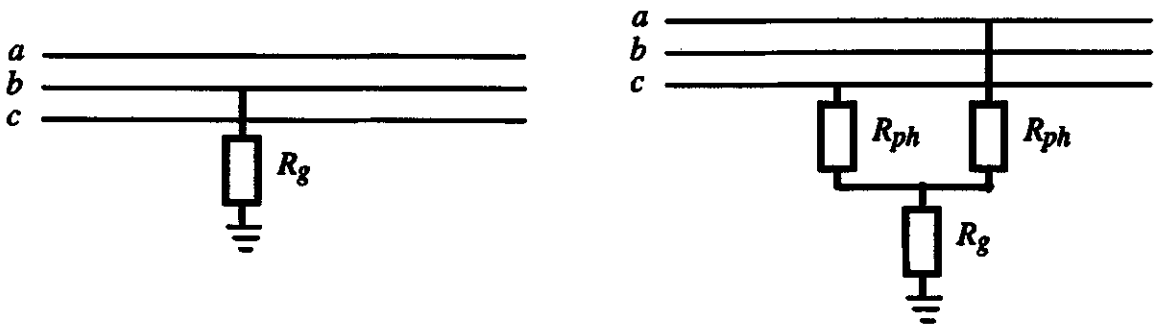

Figure F.25. Connections of fault resistance in the fault case studies.