High Speed Distance Relaying Using Least Error Squares Method

A Thesis Submitted
to the College of Graduate and Postdoctoral Studies
in Partial Fulfillment of the Requirements
for the Degree of Master of Science
in the Department of Electrical and Computer Engineering
University of Saskatchewan

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Abstract

Due to the increasing scale and complexity of modern power grids, the demand for high-speed protection is growing. Distance relays are the most commonly used type for transmission line protection. Fast sub-cycle numerical distance elements are useful, especially for EHV/UHV transmission systems (400 kV and above). A primary advantage of the LES method is that the length of the window for phasor estimation can be varied and therefore it can be used as a sub-cycle algorithm. And a mho characteristic is adopted to achieve a trip decision.

The proposed LES technique is tested on a two generator power system configuration. The method is tested using three-phase voltage and current data generated from a PSCAD/EMTDC simulation model. The relay module developed has three functional components: fault detection, phasor estimation, and protective elements. The code for the relay module is developed in MATLAB. Next, different scenarios are considered taking into account the various fault types and locations. Some of the essential practical considerations such as coupled capacitor voltage transformer (CCVT) and current transformer (CT) saturation are also taken into account for the modelled 375 kV (EHV) test system.

In this MSc work, a preliminary prototype is developed with the necessary interfaces for the LES-based distance relay. With the interface, the operating data are imported into FPGA in Comtrade99 format, and then the voltage and current instantaneous values are transformed into single-precision floating type variables.

The thesis work shows that the proposed LES scheme is a straightforward and reliable technique, can run faster than some other sub-cycle techniques, and can be applied to any power system configuration. The main contribution of this research is the application of the LES technique for distance relaying with a faster trip time. The other contributions are developing an FPGA interface for simulation and testing of the proposed relay and addressing some of the hardware implementation issues.

Acknowledgments

Above all, I wish to first thank my supervisor, Prof. Ramakrishna Gokaraju. His instruction, knowledge, and patience helped me throughout my entire M.Sc. program. I am grateful for the opportunity he provided to conduct research in the Real-Time Power Systems Simulation Lab of the University of Saskatchewan, and for the financial support he provided through his NSERC Grant(2014). I also wish to thank the University of Saskatchewan for the financial support provided through a fellowship award (2015).

My gratitude goes to all of the faculty in the Department of Electrical and Computer Engineering at the University of Saskatchewan for their support. Thanks to Prof. Li Chen for his valuable experimental equipment and continuous guidance, and Mr. Su Wang (Graduate Student) for explaining some of the mathematical details.

To Xingxing Jin (Ph.D. Student), I am thankful for the meaningful thoughts and mentoring. To Dr. Kalpesh Joshi (Postdoctoral Researcher) and Jason Pannell (Ph.D. Student), I am thankful for the valuable suggestions and corrections during thesis writing. I thank all of the graduate students in our lab for their support.

I am grateful to my family and friends, especially my beautiful parents, father Mr. Xinsheng Liu and mother Mrs. Xuanfang Zhou, to whom I owe all of my success. I am grateful for your immense love, endless encouragement, and continuous support. Thank you.

Dedicated to my

Dear Parents,

Supportive Family,

and Lovely Yiting Yang.

Table of Contents

List of Tables

List of Figures

List of Abbreviations

ALM	Adaptive Logic Module
CCVT	Coupled Capacitor Voltage Transformer
CT	Current Transformer
DFT	Discrete Fourier transform
DSP	Digital Signal Processing
EHV	Extra high voltage
FCDFT	Full Cycle Discrete Fourier transform
FPAA	Field-Programmable Analog Array
FPGA	Field Programmable Gate Array
HCDFT	Half Cycle Discrete Fourier transform
HDL	Hardware Description Language
I/O	Input/Output
IP	Intellectual Property
LAB	Logic Array Block
LES	Least Error Squares
LUT	Look-up Table
RAM	Random Access Memory
ROM	Read-Only Memory
RTL	Register Transfer Level
TW	Travelling Wave
UHV	Ultra high voltage
VHDL	VHSIC Hardware Description Language
VLSI	Very-Large-Scale Integration
WT	Wavelet Transform

Chapter 1

Introduction

Electrical power system infrastructure consists of generation, transmission, and distribution elements. In modern power systems, electrical energy is stored to complement intermittent power from renewable energy sources. Faults tend to happen on the system, and can permanently damage multi-million-dollar equipment if not removed quickly. Faults can also cause stability issues in the power system and bring down a large portion of the system in a matter of a few seconds ("blackout") if not isolated quickly enough. Therefore, in essence, protecting the power system from faults and abnormal events is critical for its reliable and secure operation.

1.1 Background

A protective relay is a vital device in power systems to alert or isolate faults by detecting abnormal conditions and sending a trip command to the corresponding circuit breaker. Relays make tripping decisions based on power system quantities such as current, voltage, frequency, power, etc. Once a fault occurs, the relay senses the fault and issues the trip signal, which must be quick and reliable. The security requirement means the relay should be able to identify and respond to real faults, but should not respond to normal events such as sudden load changes or system transients during the normal operation. The dependability requirement means the relay should not miss any faults. The security and dependability

together make up reliability. Regarding speed, primary relaying systems typically operate in one to one-and-a-half cycles. Some of the latest research shows that a one-millisecond reduction in tripping time can increase the power transfer by 15 MW [1], which is equivalent to saving one new distribution feeder.

If we look at the long history of protective relay developments, they have evolved through three main generations: electromechanical relays, solid-state relays, and digital relays. Electromechanical relays consist of an electromagnet and a moving solenoid. When abnormal changes in current or voltage occur, the electromagnet generates a mechanical torque, which is applied on the solenoid, that then finally closes a contact to energize the trip coil. Solid-state relays are the static versions of electromechanical relays, where moving elements are replaced by analog electronic devices such as transistors, diodes, and other electronic components. The two types of relays share the same functions and characteristics. In general, solid-state relays have improved size, speed, and reliability compared to electromechanical relays. They do not have moving parts, which means less maintenance is needed. Currently, most of the relays in the industry are digital numerical relays based on microprocessor technology. This type of relay was introduced to the market with advancements in VLSI (Very-Large-Scale Integration) technology and fast digital signal process (DSP) microprocessors. Analog inputs such as voltages and currents from the power systems are filtered and transformed into digital form by an analog-to-digital converter in the first step. Then the DSP algorithm processes the sampled data to produce a digital output, which is utilized by a relaying logic element to generate a trip signal. The most obvious benefit of digital relays is their flexibility in terms of programming, so this means numerical relay functions can be easily updated for prevailing system conditions at a low cost.

In summary, the following technological improvements are evident when considering the evolution of protective relays: speed, security, and reliability provided by the tripping logic, and the flexibility in relay logic design provided by new hardware.

1.2 Literature Review

Fast algorithms for detecting a fault and identifying the type of fault has been one of the hottest topics for research in the power system protection area for the past several decades. As discussed above, the primary reason is that fast fault clearing helps to improve the power system stability margin. Faster fault clearing also means improved power quality and enhanced public and utility personnel safety.

1.2.1 Phasor-based methods

A fault signal normally contains three components: a fundamental frequency component, an integer harmonic component, and a decaying DC component. Most of the protection principles are based on the estimation of fundamental frequency components of voltages and currents. The classical full cycle discrete Fourier transform (FCDFT) algorithm cannot effectively remove the DC decaying component due to its nonperiodic property. In [2], an improved FCDFT is proposed, and it takes one cycle plus two samples to obtain an accurate estimation of the fundamental when the DC component is present. Besides FCDFT, several other modified sub-cycle methods have been proposed in [3]-[13]. In [3], [4], a half-cycle discrete Fourier transform (HCDFT) is developed where only samples from half-a-cycle are utilized to estimate the phasors; this significantly reduces the calculation time compared to the classical type FCDFT. However, HCDFT loses the ability to reject even harmonics and remove the decaying DC component. In [5], [6], three off-line look-up-tables are formed to estimate the decaying DC parameters. The look-up-table approach can find the time constant of the decaying DC component using anti-aliasing filters with a specific cut-off frequency. If the system parameters change, the decaying DC parameters would also change, and the filter parameters would have to be found again. Otherwise, some errors would be introduced in estimating the decaying DC parameters, which means errors in phasor estimation. In addition, some of the system transients that could arise due to CT saturation and CCVT transient errors are not considered, yet these may affect the estimation accuracy and speed. Another linear estimation method found to be reliable in the literature is the Kalman filtering technique [7]. The method is stable in the presence of noise and harmonics but takes almost

one cycle to obtain a stable result. Also, a large number of computations are needed in each time step due to the use of a state transition matrix and a driving function matrix.

Wavelet transform (WT) techniques have also been introduced in digital distance protection. Using WT multi-resolution analysis (MRA), [8], the fundamental frequency phasor can be extracted faster than by using FCDFT. Even though the response is fast, the algorithm may become insecure as the impedance trajectories swing in and out of the protection zone before settling. To overcome this challenge, we need to reset the data window once a disturbance is detected to deliver a more stable response. Moreover, a pre-band pass filter is added to remove the DC component, but a time delay is introduced.

References [9] and [10] describe a phaselet scheme and testing for transmission line distance protection. Phaselets are pieces of phasor obtained using partial integral with increasing data windows. They become more and more accurate when the window length becomes one full cycle. The focus of the phaselet method is to balance the speed and accuracy with a variable-length window.

Research on high-speed relaying in the Real-Time Power System Simulations Laboratory began in May 2014 with Shane Jin (Ph.D. student) and the author of this MSc thesis (Shenyi Liu) researching different types of algorithms. Jin researched phaselet-based and incremental-phasor methodologies [11, 12] on a Virtex 7 FPGA board and conducted testing with a real-time simulation tool RTDS$^{\text{TM}}$. This MSc thesis work focuses on developing a least error squares methodology for high-speed relaying.

Recently, transient components in the time-domain have also been researched for high speed relaying. The primary advantage of transients-based relays is that they are less dependent on the source behaviour and more dependent on the network they are protecting. This feature is potentially useful in applications with inverter-based sources, such as wind and solar, that do not have the same voltage and current behaviour as a conventional synchronous generator. Two types of time-domain methods have appeared in the literature: incremental quantity-based, and travelling wave-based methods [1], which will be explained in the following subsections.

1.2.2 Incremental quantity-based methods

An incremental quantity signal will appear when a fault happens. In this kind of post-fault analysis, the network is simplified by removing all of the power sources and leaving the fault point as the only "source" in the equivalent network.

Figure 1.1 illustrates the incremental quantity-based approach. Assume a fault happens between two terminals of the transmission line. The Thévenins theorem together with the principle of superposition is used to solve the faulted network. The final solution (voltages and currents at any point in the faulted network) is the sum of the pre-fault and fault-generated components. The pre-fault (load) components of the voltages and currents are obtained from the pre-fault network, and the fault-generated components are obtained from the fault network. The pre-fault network is in the steady state, while the fault network has only one source (the Thévenin source) at the fault location. The Thévenin source voltage equals the negative of the voltage at the fault point in the pre-fault network.

The fault network produces incremental quantities like voltages and currents. Before the fault happens, this equivalent network is not energized, and all of its quantities are zero. After the fault, this network goes through a transient state and eventually settles into the fault steady state. Fault-generated components are not influenced by the load or generators but are driven by the Thévenin source in the fault network located at the fault point. Therefore, these quantities only depend on the network parameters. Sources and load flow indirectly establish the initial conditions for the superposition (the Thévenin) source.

Because the fault values are sums of the pre-fault values and the fault-generated values (see Fig. 1.1), the fault-generated values are going to be the difference between the fault values and the pre-fault values. Relays measure the fault quantities as the instantaneous values of voltages and currents at the relay terminals. Relays also measure the pre-fault quantities, which can be extrapolated forward for a short interval in time. This extrapolation is only applicable for a few tens of milliseconds because the power system only remains predictable for a short period. Therefore, one simple method to derive the incremental quantities is:

$$\Delta N_{(t)} = N_{(t)} - M(N_{(t-kT)}, kT) \tag{1.1}$$

where ΔN is the instantaneous incremental quantity,

N is the measured instantaneous value at a certain moment,

T is the period of the measured quantity,

k is an arbitrary number of periods, and

M is the extrapolation function.

Using equation (1.1), we obtain an incremental quantity that lasts for k power cycles, after which this quantity expires because the historical values we subtract slide into the fault period. We select the value of k depending on the intended usage of the incremental quantity. For example, if we intend to use incremental quantities during two power cycles, we can select $k = 2$.

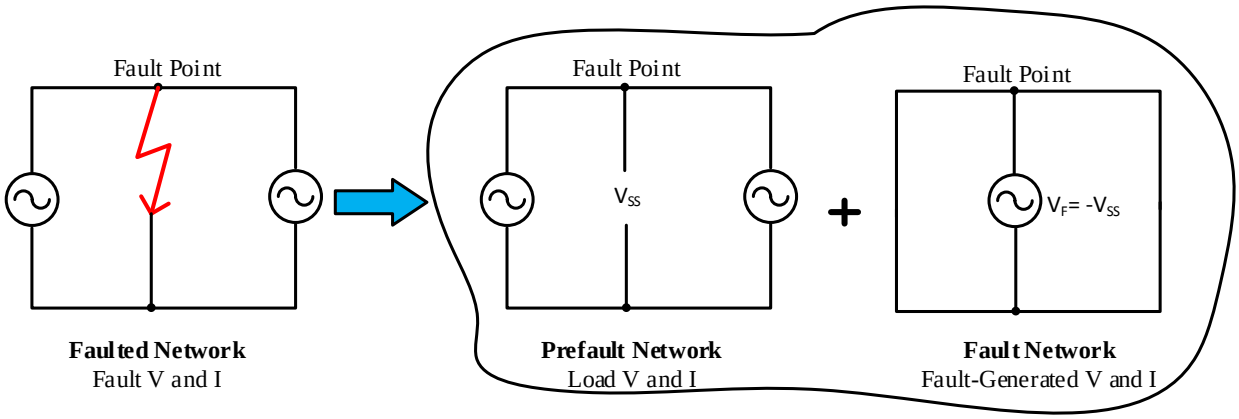

Figure 1.1 Incremental quantity-based analysis of the faulted network

In the time domain, consider the single-phase RL network of Figure 1.2 with a fault on the line between Terminal S and Terminal R. The fault network of Figure 1.3 contains incremental voltages and currents that will be used for explaining the time domain protection principles.

At the relay location S, the incremental voltage and current are related by a voltage drop

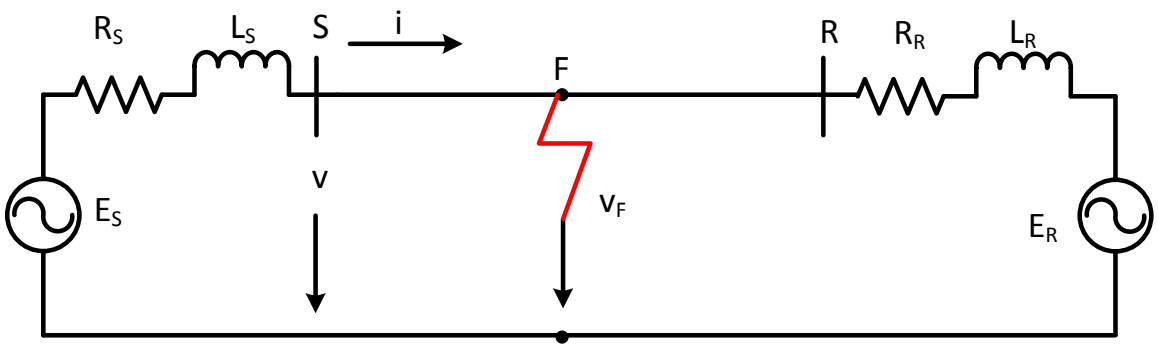

Figure 1.2 Simple two-machine single-phase system with a fault at F

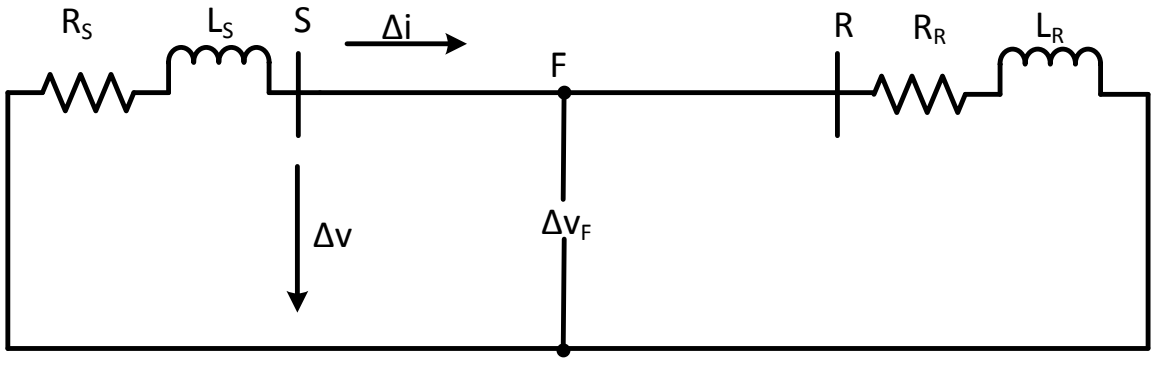

Figure 1.3 Fault network of the system in Figure 1.2 for analysis of incremental quantities

equation across the Source S resistance and inductance:

$$\Delta v = -(R_S \cdot \Delta i + L_S \cdot \frac{d}{dt}\Delta i) \tag{1.2}$$

Equation (1.2) includes a current term that is a combination of the instantaneous incremental current and its derivative. This new current signal is referred to as a "replica current" and labelled as follows:

$$\Delta i_Z = \frac{R_S}{|Z_S|} \cdot \Delta i + \frac{L_S}{|Z_S|} \cdot \frac{d}{dt}\Delta i \tag{1.3}$$

By selecting the R_S, L_S, and $|Z_S|$, we obtain a unity gain between the measured incremental current Δi and the replica current Δi_Z at the system fundamental frequency.

A simple voltage-current equation can now be written for the incremental quantities measured at Terminal S:

$$\Delta v = -|Z_S| \cdot \Delta i_Z \tag{1.4}$$

Then we notice that Equation (1.4) has the same format as the voltage-current expression for phasors:

$$\Delta V = -Z_S \cdot \Delta I \tag{1.5}$$

Therefore, we can use phasor-based analysis principles to analyze the incremental quantities-based methods.

If reverse faults occur in the network of Figure 1.3, they can be represented by placing the Δv_F source behind Terminal S. In this case, the following equation represents the relations between the incremental voltage and the incremental replica current:

$$\Delta v = |Z_R| \cdot \Delta i_Z \tag{1.6}$$

From Equations (1.4) and (1.6), it can be concluded that the incremental voltage and the incremental replica current have similar waveforms, their relative polarities indicate the fault direction, and their amplitude relationship depends on the system impedances.

Next, Δv and Δi_Z would be measured and calculated as operating quantities, then compared with pre-defined threshold values plus a certain secure margin, to implement distance and directional protective functions.

In terms of performance, for the test case described in [13], the distance relaying function is consistently fast with an average operating time below 4 ms, while the directional relaying function operates consistently in about 2 ms. The limitation of this method is that it will not detect faults that create a small change in the fault point voltage, such as high-resistance faults. Also, the operating time may be slower than a quarter of a cycle for faults that occur close to the voltage zero crossing.

1.2.3 Travelling Wave-based Methods

Faults launch travelling waves (TWs) that travel close to the speed of light and get reflected at buses or other discontinuities. At the very initial stage of the fault, the power system behaves as a distributed parameter network. The TWs are well described by the line characteristic impedance. TWs can be used to provide ultra-high-speed protection, with possible operating times that are below 1 millisecond. TWs from a fault anywhere on a 160 km line reach both ends within 600 microseconds. After a few roundtrip reflections, TWs recombine into stationary waves, and the power system starts to look like a lumped parameter RLC network in a transient state.

1.2.3.1 Travelling Wave Principles

A fault on a transmission line generates TWs that propagate from the fault location to the line terminals with a propagation velocity that depends on the distributed inductance and capacitance of the line. Figure 1.4 shows the equivalent circuit of a segment with length Δx of a two-conductor transmission line. The circuit includes resistance R, inductance L, conductance G, and capacitance C in per unit of the total line length.

Equations (1.7) and (1.8) determine the voltage and current as a function of wave position (x) and time (t) for a two-conductor lossless transmission line in the time domain as the length of segment Δx approaches zero. The negative sign indicates that the amplitudes of the waves decrease as x increases.

$$\frac{\partial v(x,t)}{\partial x} = -L\frac{\partial i(x,t)}{\partial t} \tag{1.7}$$

$$\frac{\partial i(x,t)}{\partial x} = -C\frac{\partial v(x,t)}{\partial t} \tag{1.8}$$

Differentiating equations (1.7) and (1.8) with respect to time and position is conducted to obtain the wave equations (1.9) and (1.10).

$$\frac{\partial^2 v(x,t)}{\partial x^2} = LC\frac{\partial^2 v(x,t)}{\partial t^2} \tag{1.9}$$

$$\frac{\partial^2 i(x,t)}{\partial x^2} = LC\frac{\partial^2 i(x,t)}{\partial t^2} \tag{1.10}$$

Equations (1.11) and (1.12) are the corresponding general solutions for the second-order

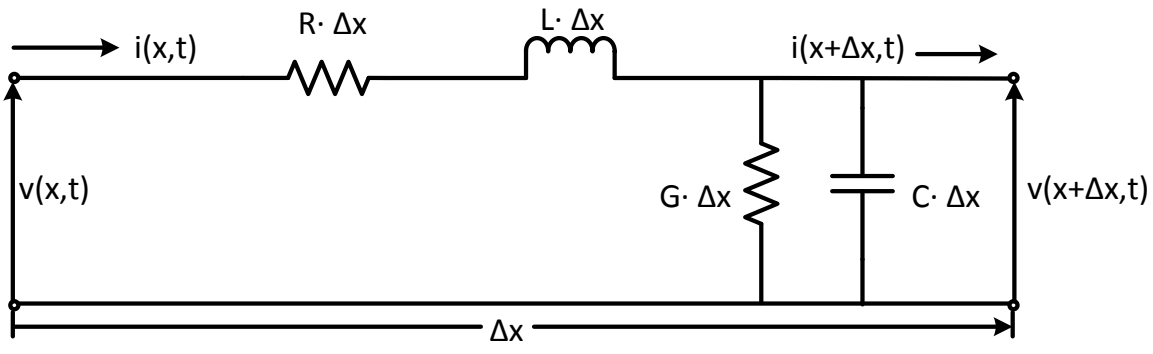

Figure 1.4 Equivalent circuit of a segment of a two-conductor transmission line

partial differential equations (1.9) and (1.10) in the time domain. The $F(x-u\cdot t)$ represents forward waves and $f(x+u\cdot t)$ represents backward waves:

$$v(x,t) = F(x-u\cdot t) + f(x+u\cdot t) \tag{1.11}$$

$$i(x,t) = \frac{1}{Z_0}\cdot[F(x-u\cdot t) - f(x+u\cdot t)] \tag{1.12}$$

where $Z_0 = \sqrt{\frac{L}{C}}$ is the characteristic impedance of the line and $u = \frac{1}{\sqrt{LC}}$ is the propagation velocity.

The forward wave can be obtained by multiplying equation (1.12) by Z_0 and adding it to equation (1.11). This wave depends on the line characteristic impedance Z_0 but is independent of the termination impedance.

$$v(x,t) + Z_0\cdot i(x,t) = 2\cdot F(x-u\cdot t) \tag{1.13}$$

Similarly, by using equation (1.14), the backward wave can be extracted from the measured terminal quantities.

$$v(x,t) - Z_0\cdot i(x,t) = 2\cdot f(x+u\cdot t) \tag{1.14}$$

In the faulted circuit in Figure 1.5, the fault current wave i_{FS} and the fault voltage wave v_{FS} travel toward Terminal S, and the fault current wave i_{FR} and the fault voltage wave v_{FR} travel toward Terminal R. The incident wave that is travelling from the fault to Terminal S can be calculated using equation (1.15):

$$v_S(x,t+\tau_S) - Z_0\cdot i_S(x,t+\tau_S) = v_{FS}(x,t) + Z_0\cdot i_{FS}(x,t) \tag{1.15}$$

where τ_S is the travel time of the wave from the fault to Terminal S and currents flowing into the line are considered to be positive.

1.2.3.2 Travelling Wave Scheme Based on the Incident Wave Amplitudes

Assume that the prefault voltage at the fault point is $V_P \cdot \sin(\omega \cdot t + \theta)$, where ω is the system frequency and θ is the fault incidence angle. Then, the voltage at the fault point is $v_F(t) = -V_P \cdot \sin(\omega \cdot t + \theta)$. The incident wave at Terminal S is calculated using equation (1.14) and is given in equation (1.16).

$$v_S(t + \tau_S) - Z_0 \cdot i_S(t + \tau_S) = -2 \cdot V_P \cdot \sin(\omega \cdot t + \theta) \tag{1.16}$$

The wave given in equation (1.16) is termination-independent, but depends on the fault incidence angle. To make it independent of the fault incidence angle, Dommel introduced a discrimination factor D based on equations (1.17) through (1.20) [14]. First, take the time derivative of equation (1.16) to get:

$$\frac{1}{\omega}\frac{d}{dt}[v_S(t + \tau_S) - Z_0 \cdot i_S(t + \tau_S)] = -2 \cdot V_P \cdot \cos(\omega \cdot t + \theta) \tag{1.17}$$

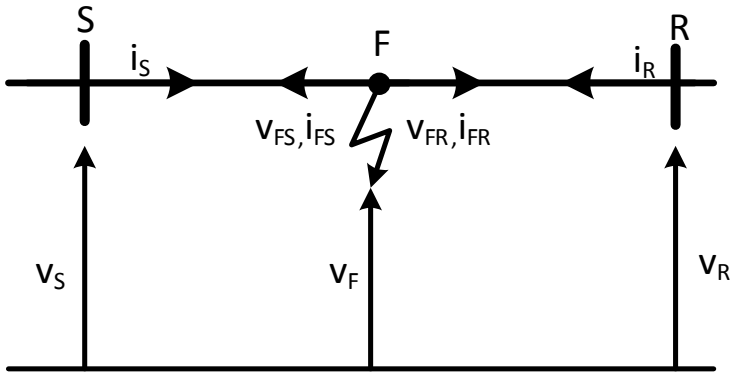

Figure 1.5 Faulted line showing waves travelling from the fault toward the line terminals

Then square equation (1.16) and (1.17) to obtain:

$$[v_S(t+\tau_S) - Z_0 \cdot i_S(t+\tau_S)]^2 = 4 \cdot V_P^2 \cdot \sin^2(\omega \cdot t + \theta) \tag{1.18}$$

$$\{\frac{1}{\omega}\frac{d}{dt}[v_S(t+\tau_S) - Z_0 \cdot i_S(t+\tau_S)]\}^2 = 4 \cdot V_P^2 \cdot \cos^2(\omega \cdot t + \theta) \tag{1.19}$$

By adding equation (1.18) and (1.19), discriminant D can be defined as a value independent from the fault incidence angle:

$$D = 4 \cdot V_P^2 = [v_S(t+\tau_S) - Z_0 \cdot i_S(t+\tau_S)]^2 + \frac{1}{\omega^2}[\frac{dv_S(t+\tau_S)}{dt} - Z_0 \cdot \frac{di_S(t+\tau_S)}{dt}]^2 \tag{1.20}$$

Because the D factor is comprised of incident waves, the D values are large for forward faults and near zero for reverse faults. A communications-based comparison scheme is used to locate the fault according to D values obtained from different line terminals, and then send the corresponding trip signal. The described method works with a traditional low-bandwidth communications channel, but it needs high-fidelity voltage signals, that generally cannot be provided by CCVTs.

1.2.3.3 Directional Comparison Scheme Based on Incident and Reflected Travelling waves

The incident and reflected TWs can be compared to make directional tripping decisions. The algorithm described in this part calculates the incident (forward) and reflected (backward) TWs using equations (1.21) and (1.22), respectively.

$$s_F = v(t) - Z_0 i(t) \tag{1.21}$$

$$s_B = v(t) + Z_0 i(t) \tag{1.22}$$

The sequence in which the incident and reflected waves exceed a predefined threshold determines the fault direction. For a forward fault, the incident wave appears before the reflected wave, assuming that it takes some time for the wave to reach a discontinuity and travel back toward the line terminal. For a reverse fault, the reverse direction wave from the fault appears long before the wave reflected from the remote terminal returns to the relay location as a forward wave. A directional comparison scheme using this TW directional element is applied to trip the line.

The method was originally proposed by Johns in [15] and is a straightforward application of wave separation theory. The wave separation method uses a traditional low-bandwidth communications channel, but requires high-fidelity voltage measurements.

1.2.3.4 Distance to Fault Element Based on Travelling Waves

As shown in Figure 1.6, the TW launched by the fault is reflected at the relay location (the bus S) and the fault point several times. Therefore, we can design an underreaching TW distance element by measuring the time difference Δt between the arrival of the first TW from the fault and the arrival of the TW reflected at the fault point. The element calculates the fault distance using Δt and the wave propagation velocity, and issues a trip if the distance is shorter than the set reach.

The following steps summarize the distance-to-fault calculation:

• Upon arrival of the first TW to the line terminal, determine the fault direction using a directional element similar to the one in previous subsection proposed by [15].

• For faults in the forward direction, estimate t between the two TWs, as shown in Figure 1.6. The method can use cross-correlation to verify the similarity of the wave reflected from the fault and the prior wave travelling toward the fault.

• Calculate the distance to the fault using $d = \frac{\Delta t}{2} \cdot u$.

• Trip if d is less than a reach setting.

The distance measurement method was initially proposed by Crossley [16].

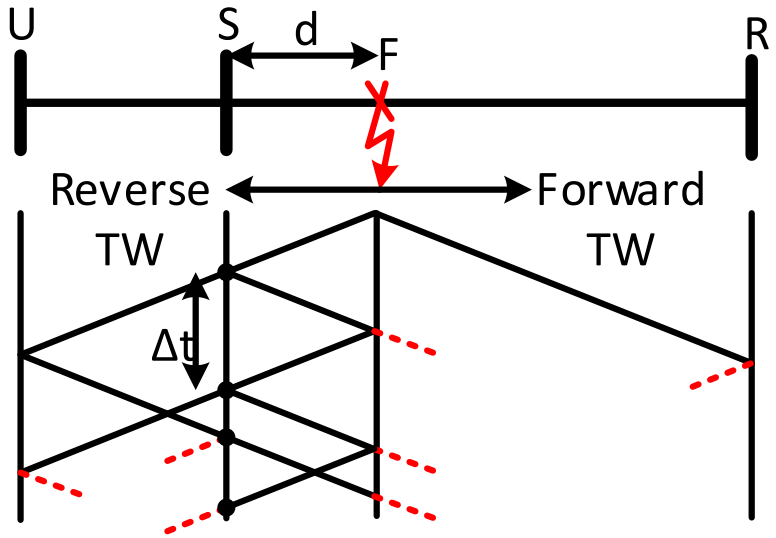

Figure 1.6 Using multiple reflections to calculate the distance to the fault

1.2.3.5 Advantages and Limitations

Reference [13] claims the operating times for the TW-based line protection elements are less than 1 ms plus the channel time. However, these methods require high-fidelity voltages and currents. CTs allow measurement of current TWs, but CCVTs are not adequate for TW voltage measurements. The need for high-fidelity voltage information calls for high-bandwidth voltage sensors and creates an obstacle in the application of TW-based protection methods that use high-fidelity voltage information. A novel TW current-only differential element presented in [1] eliminates the high-fidelity voltage requirement. It uses high-speed communications, which are easier to achieve today with the widespread availability of fiber-optic channels as compared to installing new high-voltage measuring devices. Another solution is presented in [17], in which the correlation coefficient of the incremental quantities of fault-generated TWs within a specific window are used for directional protection. This method does not add any additional requirement to the network and the operating time is less than 7 ms.

Another challenge for ultra-high-speed line protection comes from speeds that are possibly too fast. The TW-based method has a chance to see events other than short circuits, such as the normal operation of in-line surge arresters, overvoltages caused by switching events or external faults, opening or closing the bypass breaker on in-line series capacitors, and lightning strikes to ground wires and towers that induce TWs on power conductors. Today's protection schemes are too slow or insensitive to respond to these events. As a result, ultra-high-speed line protection must be designed to distinguish between a short circuit that requires tripping and normal arrester conduction. Reference [1] proposed two groups of solutions that are based on measurement of air insulation energy and surge arrester voltage, respectively.

1.3 Motivation for this Work

The growing complexity and size of modern power systems demand faster and more secure protective relays. High-speed protection is especially desirable for extra high voltage

(EHV) transmission lines (400 kV and above). Additionally, the traditional notion of power systems is mutating into the smart grid concept with the widespread use of distributed generation and smart loads, which pose significant challenges for power system protection and security [18], [19]. There is a need for a high-capacity, high-bandwidth protective relay that can cope with the demand for signal processing, intelligence, and communication functions.

Aside from the algorithms reviewed in the last subsection, Dr. Sachdev and Mr. Baribeau proposed a least error square-based technique in [20]. This method is phasor-based like the DFT method, but needs to build the signal components using Taylor expansion beforehand; this is unlike DFT method that can directly extract fundamental component of interest. Therefore, the critical drawback of the technique is that the resource demand for computation is several times (at least two times if only fundamental and DC components are taken into account) more than the DFT method. Another factor is the sampling rate, which was 12 samples/cycle in the year when that paper was published but now may be as high as hundreds or even thousands of samples per cycle; as such, the calculation requirements are exponentially greater. This situation was not resolved until recent years when the digital-signal-process-based integrated circuit (IC) technology become sufficiently fast and cheap to meet the requirements.

Among all computing platforms, field programmability (FP) is a competitive feature to have in a protective relay. In the past, distance relays were designed on FPAAs (field programmable analog arrays) [21]. Since then, FPGAs (field programmable gate arrays) are making significant inroads in many applications in industrial and commercial systems [22]. Considerable research is currently being undertaken in the protective relays area; for example, reference [23] designed an FPGA-based protective relay, [24] proposed a protection scheme for HVDC lines using FPGA, [25] implemented a DFT-based protective relay on FPGA, and [26] implemented a phaselet-based protective relay on FPGA. The characteristics of the FPGA that are pertinent for its use in protection relay applications are:

• inherent parallel hard-wired architecture allowing for an ultra-low latency realization of complex algorithms;

• huge capacity devices comprised of millions of logic building blocks to provide substantial hardware resources for even the most resource-intensive models and algorithms;

• mature design and development tools for customized prototyping, and integration with mathematical software packages such as MATLAB/Simulink, allowing users the choices of written textual (VHDL or Verilog) or schematic design entry methods; and

• fast clock speeds and high-speed transceivers to communicate with external devices.

The FPGA device uses the inherent parallelism of the hardware to increase execution speed compared to sequential software architecture-based microprocessor technology.

1.4 Objectives

The main objectives of this thesis consist of verifying the performance and reliability of an LES algorithm for distance protective relaying, and developing some necessary modules for hardware simulation and testing on the FPGA. The research work is divided into the following parts:

• Each functional module of the protective relay needs to be specified and implemented. For instance, the modules within the protective relay contain fault detection, LES estimation, and several other sub-modules to fulfill its function.

• Model the test power system in simulation software PSCAD/EMTDC® and collect fault data to validate the functions of the proposed protective relay. After several types of faults are simulated in the software, faulted voltage and current data are generated. The proposed relay will take in the fault data, process the corresponding calculations and issue the trip signal to a circuit breaker.

• Take practical aspects into consideration, such as CT saturation and CCVT transients, to confirm the robustness of the LES algorithm.

• The hardware emulation of the distance relay starts from building a data interfacing module on the FPGA. To achieve high performance, these individual hardware modules apply both the paralleled and pipelined computational schemes.

1.5 Thesis Outline

The remaining chapters of this thesis are outlined as follows:

• Chapter two presents general information about three kinds of phasor-based estimation technologies, comparison of different algorithms, and the design flow used for emulation of the high-speed protective relay .

• Chapter three illustrates the design details of the various modules of the distance relay (LES, fault detection, trip delay routine, etc.), and presents a discussion of the simulation results.

• Chapter four describes the impact of some practical factors on the distance relay designed in the previous chapter, such as CT saturation and CCVT transient error, and the preliminary stages of implementation on the FPGA platform.

• Chapter five gives the conclusions of the thesis and suggestions for the future work.

Chapter 2

Digital/Numerical Phasor-based Methodology

2.1 Introduction

In Chapter 1, three kinds of methods for implementing the high-speed relaying were discussed, including phasor-based method, incremental quantities-based method, and travelling wave-based method. The last two techniques are inherently sensitive and are nowadays talked about as the next generation of ultra-high-speed relays. However, the ultra-high-speed comes with a significant cost – the electrical networks have to be upgraded with the new high frequency and fidelity measurement and communication equipment, which would need significant investment. This thesis work focuses on the classical phasor-based approaches but with the aim of making the relay high-speed. In this Chapter 2, the basic concept of a phasor-based method for fault detection is discussed, and the most efficient and reliable technique is chosen for further research with high-speed relaying purposes.

Digital/numerical relays are the ones in which the measured AC quantities are sequentially sampled and converted into digital data form. Mathematical operations on the digitized data can be implemented on a digital signal processing (DSP) hardware. Different types of estimation algorithms can be implemented on the DSP to obtain the magnitude and phase angle of the voltage and current for numerical relay design. Logic operations then can be

performed using the obtained phasors to make relay trip decisions.

2.2 Phasor-based Algorithms

There are essentially three types of phasor-based algorithms, which are used for various protective relaying functions. The classifications of these algorithms are given as below:

(1) **Non-Recursive Type**

• Short window algorithms

From the 1950s to 70s of last century, several short window algorithms using three or more samples were introduced as follows: Mann and Morrison [27], Rockefeller and Udren [28], Gilbert and Shovlin [29], and the least error squares (LES) algorithms [20]. The computational power of the relay hardware was minimal during this time, and the short window algorithms were first implemented in the early days using this technology.

• Long window algorithms

The long window algorithms are about one cycle (1/60≈16ms), such as classical Fourier Transform techniques, optimized Fourier Transform techniques and least squares techniques. Note that the least squares algorithm can be designed with both a short window and a long window.

(2) **Recursive Type**

In this method, the parameter value $\theta(t)$ at moment t is estimated using the parameter values at time t-1, $\theta(t-1)$, and the input and output values $u(t)$, and $y(t)$ measured at time t. Similarly the new parameter value $\theta(t+1)$ is found until a satisfactory parameter value is obtained.

The typical recursive algorithm includes recursive least squares, and Kalman filtering [30]. The recursive type algorithms take fewer calculation resources than the non-recursive type at every time step but take more time to converge to a stable value.

(3) **Modern Digital Filtering Techniques**: Pattern recognition using Wavelets, Neural Networks etc [30] [31].

All the algorithms are based on the extraction of information about the waveforms from the current and voltage samples. The type of phasor estimation technique used and the system conditions (composition of harmonics, the time constant of decaying dc component) influence the fault detection time and accuracy of the relay. In this chapter, three methods -Mann and Morrison, DFT and LES -will be discussed.

2.3 Mann and Morrison Technique

The Mann and Morrison technique [27], one of the first numerical type techniques used for protective relay applications was proposed in the 1970s. It uses three samples to estimate each point of the waveform. The waveform of the signal is assumed sinusoid of the nominal frequency, and the frequency of the signal is assumed invariant.

The method with the equations are explained below briefly,

Consider a situation as shown in Figure 2.1. Notice that the time is zero at the middle of the window.

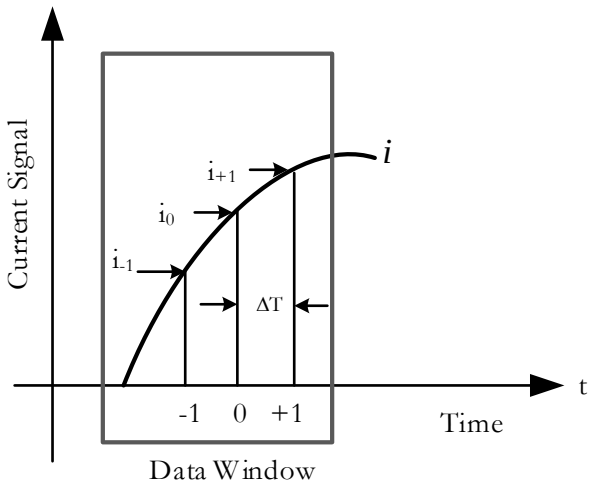

Figure 2.1 Mann and Morrison Technique with 3 data samples (window is full)

At time t = 0, the instantaneous value and change rate of current can be measured as belows,

$$i = i_0 \tag{2.1}$$

$$i' \approx \frac{i_{+1} - i_{-1}}{2\Delta T} \tag{2.2}$$

Meanwhile, a current signal at time t can be represented as:

$$i = I_p sin(\omega t + \theta) \tag{2.3}$$

$$i' = \omega I_p cos(\omega t + \theta) \tag{2.4}$$

Then, the peak value (magnitude) and the phase angle of the voltage can be estimated using the following two equations,

$$I_p^2 = i^2 + \left(\frac{i'}{\omega}\right)^2 \tag{2.5}$$

$$tan(\omega t + \theta) = \frac{\omega i}{i'} \tag{2.6}$$

Advantages of the Mann and Morrison Technique are:
Have a rapid response to transients.
Can be implemented with a few computations only.

Disadvantages of the Mann and Morrison Technique are:
The results are adversely affected by the decaying DC components in the inputs.
The results are adversely affected by the harmonics in the inputs.
The results are adversely affected by the presence of noise; noise is amplified.

2.4 Discrete Fourier Transform (DFT) Filtering Technique

For implementing this technique, the waveform should be first analyzed to determine the components of frequencies present, then two orthogonal functions of those frequencies are described.

The orthogonal functions extract the components of the frequency of interest. Two sets of functions commonly used are the sine and cosine functions. The Fourier Transform (FT) technique equations for estimating the magnitude and phase angle in the continuous domain are:

$$I_p cos(\theta) = \frac{1}{\pi} \int_0^{2\pi} I_p sin(\omega t + \theta)[sin(\omega t)] d\omega t \tag{2.7}$$

$$I_p sin(\theta) = \frac{1}{\pi} \int_0^{2\pi} I_p sin(\omega t + \theta)[cos(\omega t)] d\omega t \tag{2.8}$$

The above equations can be represented in the discrete form by replacing integration to summation. The DFT equations are shown below.

The real component of the phasor can be estimated using the following equation:

$$I_p cos(\theta) = \frac{2}{N} \sum_{k=m-N}^{k=m-1} i_k sin[(k + N - m)\omega \Delta T] \tag{2.9}$$

The imaginary component of the phasor can be estimated using the following equation:

$$I_p sin(\theta) = \frac{2}{N} \sum_{k=m-N}^{k=m-1} i_k cos[(k + N - m)\omega \Delta T] \tag{2.10}$$

In equations (3) and (4), N is the number of samples in a data window. m is the present sample number. i_k is the instantaneous value of the current.

Advantages of the DFT Technique are
Attenuates noise effectively,
Attenuates all of the harmonic components effectively,
Rejects the non-decaying part of the DC component.

Disadvantages of the DFT Technique are
Transient response is slower compared to the transient response of the Mann and Morrison Algorithm. And at least one cycle of samples are needed to obtain a stable estimation; this is one of the primary reasons why most of the numerical relays take more than a cycle to

detect faults,

Decaying part of the DC component affects accuracy,

More computations are required compared to the computations required by the Mann and Morrison algorithm.

2.5 Least Error Squares Method

To obtain the fundamental AC phasor and to remove the decaying DC component from fault current inputs, Sachdev and Baribeau [20] proposed an algorithm based on the least error squares for numerical relaying at 1979.

2.5.1 Fundamental Mechanism

The basic equation for parameter estimation in matrix form could be represented as follows,

$$[A]\,[x] - [m] = [e] \tag{2.11}$$

where, A is an independent variable polynomial,

x is the parameter to be estimated,

m are the measurements and

e is the error.

Thus, $[e]^T\,[e]$ is the sum of error squares. To make the sum minimum, its derivative is equated to zero, therefore we have,

$$[x] = \left[[A]^T\,[A]\right]^{-1}\,[A]^T\,[m] = [A]^{-1}_{left}\,[m] \tag{2.12}$$

where, $[A]^{-1}_{left}$ is left inverse matrix of $[A]$.

2.5.2 Waveform Expression

Now let us analyze the output of a CT or current transformer during a fault. The waveform mostly consists of a fundamental frequency, harmonic components (2nd, 3rd harmonic and some higher order frequency), and a decaying DC component depending on the instant of the fault. An anti-aliasing or low-pass filters before the numerical relaying blocks the higher order harmonics above the fifth harmonic frequencies.

For the purpose of explaining briefly the basic least error square equations, a waveform to be analyzed is expressed below as mostly consisting of fundamental frequency term and a decaying DC term:

$$i = I_p sin\left(\omega t + \theta\right) + I_0 e^{-t/\tau} \tag{2.13}$$

It is reasonable to expand $e^{-t/\tau}$ by using a Taylor series and ignoring the terms equal or higher than the 2nd order considering t or sampling interval is small enough,

$$i = I_p sin\left(\omega t + \theta\right) + I_0 - I_0 \frac{t}{\tau}$$

$$= I_p cos\left(\theta\right) sin\left(\omega t\right) + I_p sin\left(\theta\right) cos\left(\omega t\right) + I_0 - I_0 \frac{t}{\tau} \tag{2.14}$$

where, I_p is the peak value of the fundamental frequency component,
θ is the phase angle of the fundamental frequency component,
I_0 is the magnitude of the DC offset at t = 0,
τ is the time constant of the decaying DC offset and
w is 2π times the frequency of the power system.

Since t is a constant and known in advance when the sampling rate is decided, it can be replaced by a series of $n\Delta t$. i is the current measurement, which is also known. Now there are four parameters that need to be estimated, which are I_p, θ, I_0 and τ. Comparing equation (2.12) and (2.14), we can develop the current phasor calculation equation as follows,

$$\begin{bmatrix} I_p cos\left(\theta\right) \\ I_p sin\left(\theta\right) \\ I_0 \\ -I_0/\tau F \end{bmatrix} = \left[\left[A\right]^T \left[A\right]\right]^{-1} \left[A\right]^T \left[i\right] \tag{2.15}$$

where, $[A]=\begin{bmatrix} sin\left(-n\omega\Delta t\right) & cos\left(-n\omega\Delta t\right) & 1 & -n \\ sin\left(-\left(n-1\right)\omega\Delta t\right) & cos\left(-\left(n-1\right)\omega\Delta t\right) & 1 & -\left(n-1\right) \\ ... & ... & ... & ... \\ sin\left(0\right) & cos\left(0\right) & 1 & 0 \\ ... & ... & ... & ... \\ sin\left(\left(n-1\right)\omega\Delta t\right) & cos\left(\left(n-1\right)\omega\Delta t\right) & 1 & \left(n-1\right) \\ sin\left(n\omega\Delta t\right) & cos\left(n\omega\Delta t\right) & 1 & n \end{bmatrix}$,

F is sampling rate, and $F = \frac{1}{\Delta t}$.

2.5.3 Window Length

The number of rows from matrix A is the same as sampling window length of i. Since the number of unknowns is four, the minimum requirement for window length is four. With a varying data window, the speed and accuracy become a trade-off. Obviously when the data window length is more, the accuracy would be more, i.e. the method will be able to attenuate noise or other higher harmonic components more effectively. However, it will take more time for the longer window method to detect a fault condition. On the other hand, when the window length is less than half a cycle, the fault detection would be faster but the accuracy could be also compromised.

One major advantage of the Least Squares algorithm is the freedom of choosing a window size. In this research, the objective is to obtain the stable estimation of a phasor as soon as possible (less than one cycle). Considering the sampling rate is 64 samples/cycle or 3,840 samples/s, so the window length is chosen to be 32, which is a half cycle. The effectiveness

of half-cycle-window can be proven in the following section.

2.6 An Example to Demonstrate the Phasor-based Methods

To demonstrate the advantages and disadvantages of the three algorithms for phasor estimation mentioned above, we will present a case study in this section.

Suppose a current signal consists of a 60 Hz AC component and a decaying DC component. The fundamental frequency is 60 Hz. The signal is sampled at 720 Hz. The quantized values of its samples are listed in Table 2.1.

Table 2.1 Quantized Value of the Current Signal

Sample No	**Quantized Value**	**Sample No**	**Quantized Value**	**Sample No**	**Quantized Value**
1	0	17	1370	33	998
2	0	18	1706	34	480
3	0	19	1811	35	-36
4	0	20	1649	36	-418
5	0	21	1256	37	-567
6	0	22	730	38	-448
7	0	23	205	39	-96
8	0	24	-185	40	390
9	0	25	-342	41	876
10	0	26	-231	42	1229
11	0	27	113	43	1351
12	0	28	592	44	1205
13	0	29	1072	45	827
14	100	30	1418	46	316
15	433	31	1538	47	-195
16	901	32	1381	48	-571

From Figure 2.2, it can be seen that the current measurement signal consists of a sinusoid

component and a decaying DC component.

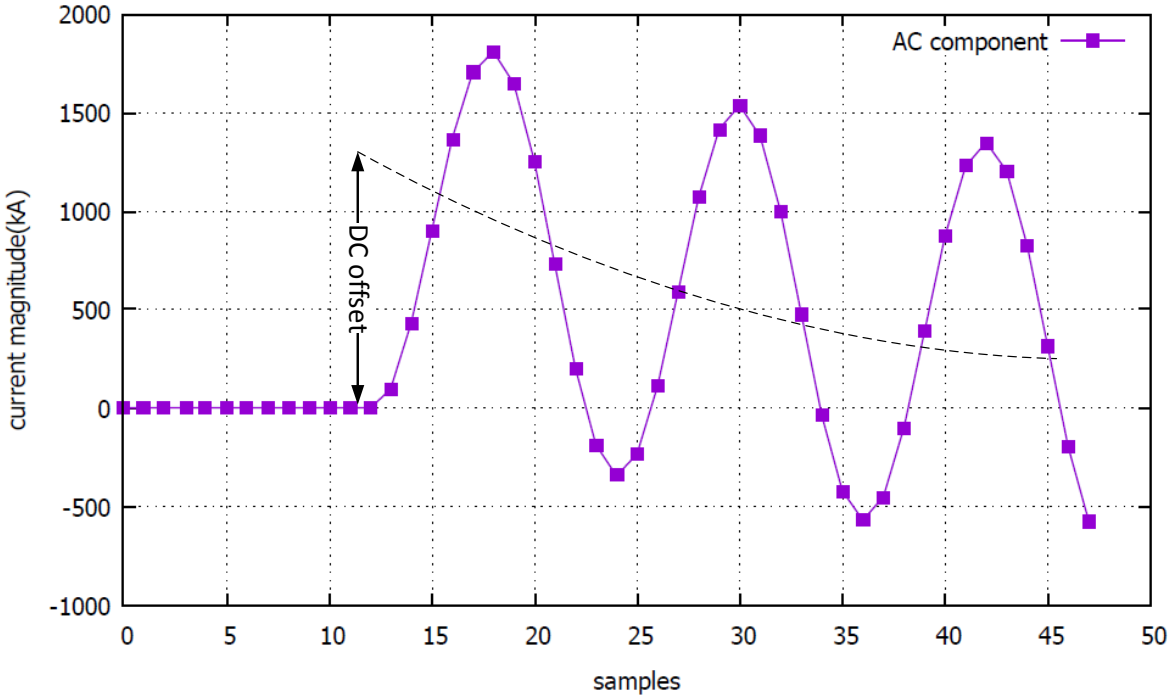

Figure 2.2 Current Measurement Signal

(1) **Mann and Morrison Algorithm**

The AC component phasor obtained by Mann and Morrison method is shown in Figure 2.3, it is quite evident that the results are affected by the decaying DC components so much that the estimated magnitude cannot converge to expected value even after two and a half cycles.

(2) **DFT Algorithm**

The AC component phasor acquired by DFT method is shown as Figure 2.4, notice that the decaying DC component causes oscillation in the range of ten percent during the second cycle, and in the range of seven percent during the third cycle. Therefore, the presence of DC component deteriorates the performance of DFT algorithm so that classical DFT cannot be used for a high-speed relaying. In 2000, J.C. Gu and S.L. Yu [2] proposed an improved DFT algorithm, which can make the convergence period shorter into one cycle and two samples

by adding a few amounts of calculation.

(3) **LES Algorithm**

Since the sampling rate is 12 samples/cycle, the $\omega\Delta t$ is equal to 30 degrees. To demonstrate the effect of filter window length on the estimation result, we would choose the length to be as five and seven, because they are both greater than four and hovering around the half cycle length which is six. Therefore, using equation (2.15) and select n equal to two and three, the matrix A for both cases look like as follows,

When windows length is five, $[A]=\begin{bmatrix} -0.866 & 0.5 & 1 & -2 \\ -0.5 & 0.866 & 1 & -1 \\ 0 & 1 & 1 & 0 \\ 0.5 & 0.866 & 1 & 1 \\ 0.866 & 0.5 & 1 & 2 \end{bmatrix}$

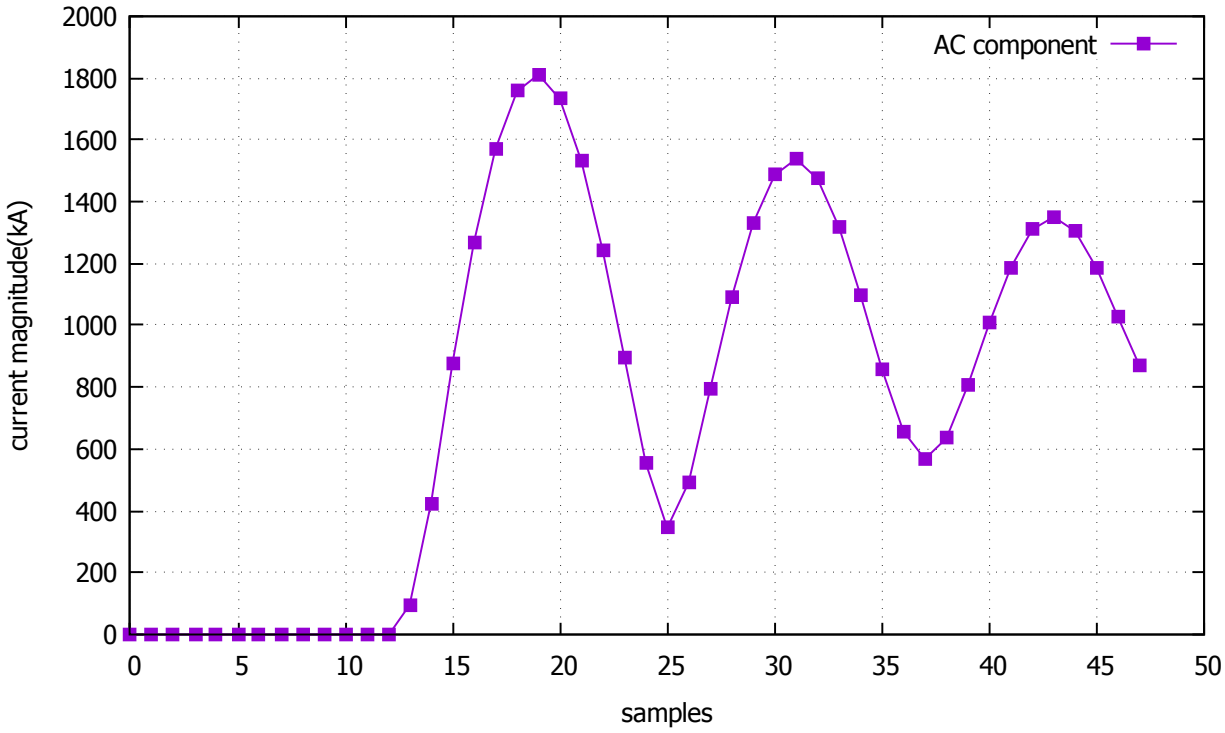

Figure 2.3 Phasor estimation using Mann and Morrison method

When windows length is seven, $[A]=$

$$\begin{bmatrix} -1 & 0 & 1 & -3 \\ -0.866 & 0.5 & 1 & -2 \\ -0.5 & 0.866 & 1 & -1 \\ 0 & 1 & 1 & 0 \\ 0.5 & 0.866 & 1 & 1 \\ 0.866 & 0.5 & 1 & 2 \\ 1 & 0 & 1 & 3 \end{bmatrix}$$

The AC component phasor is shown in Figure 2.5 and 2.6,

Comparing the two figures, five-sample-window converges at the 17th sample, and seven-sample-window converges at the 19th sample. Considering the first non-zero measurement occurs at the 14th sample, and the sampling rate is 12 samples/cycle, so it takes four samples for a five-sample-window algorithm to converge, and six samples for a seven-sample-window

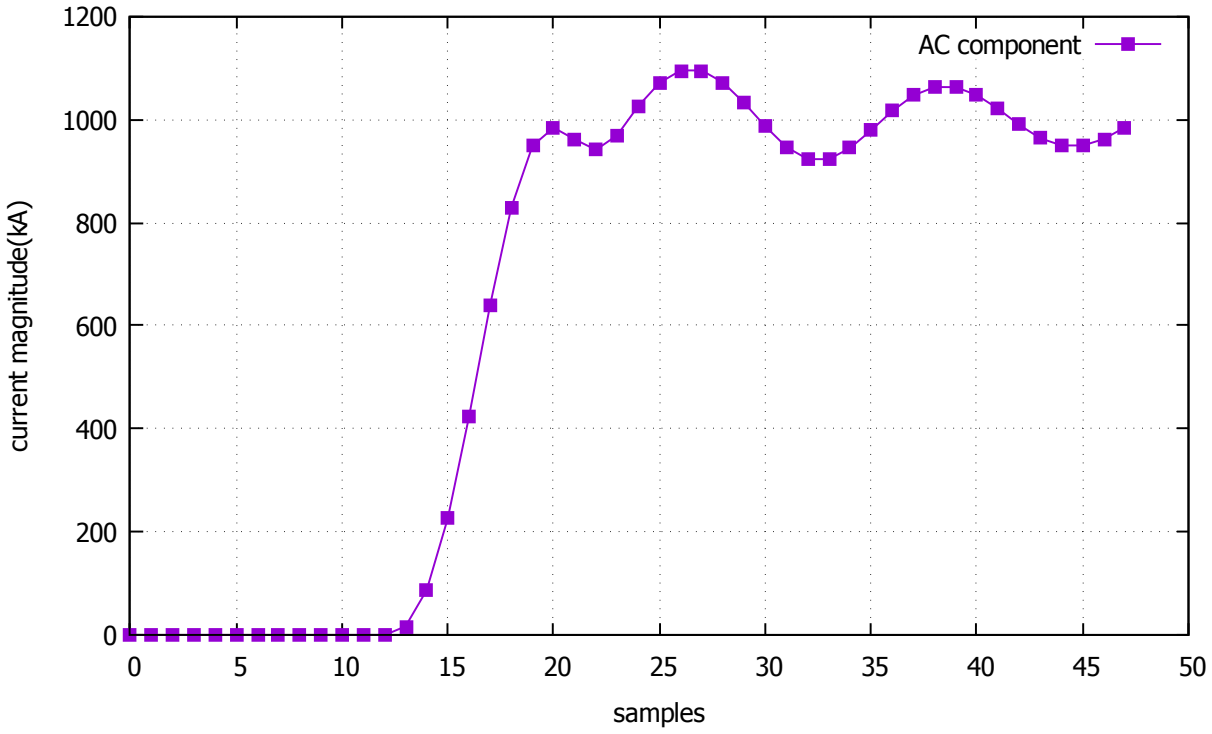

Figure 2.4 Phasor estimation using DFT method

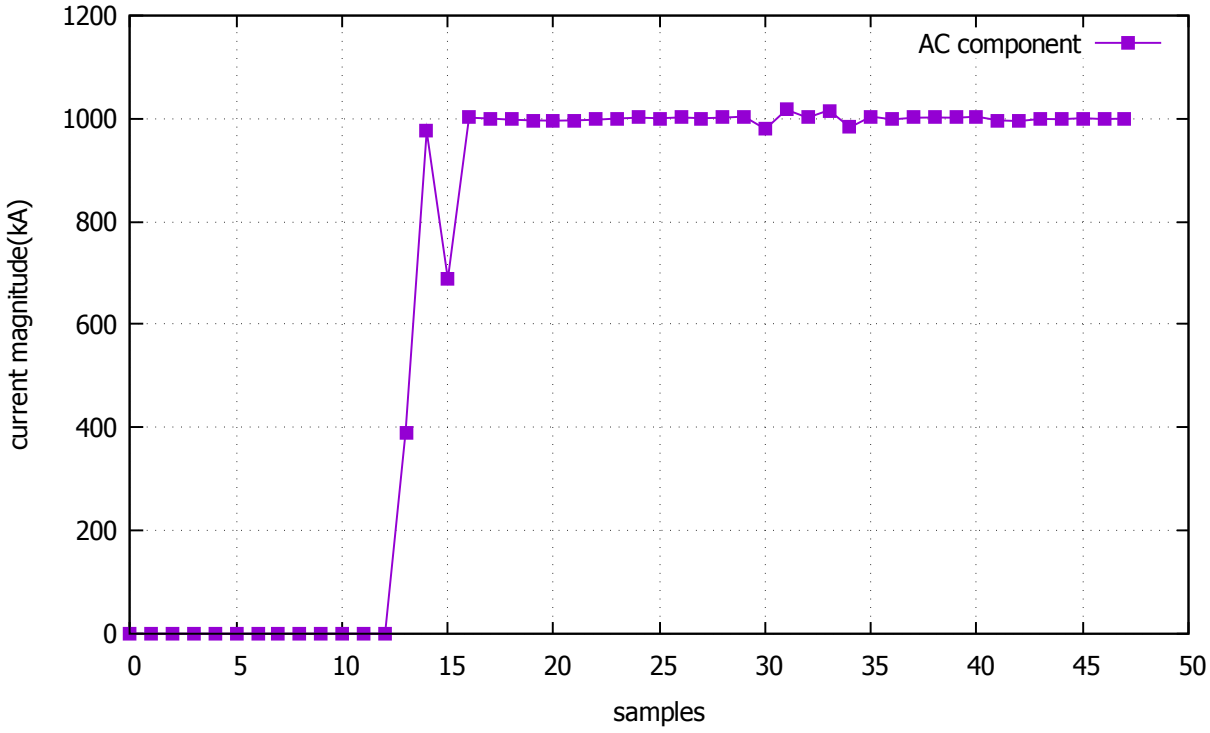

Figure 2.5 Phasor estimation using LES method(window size=5)

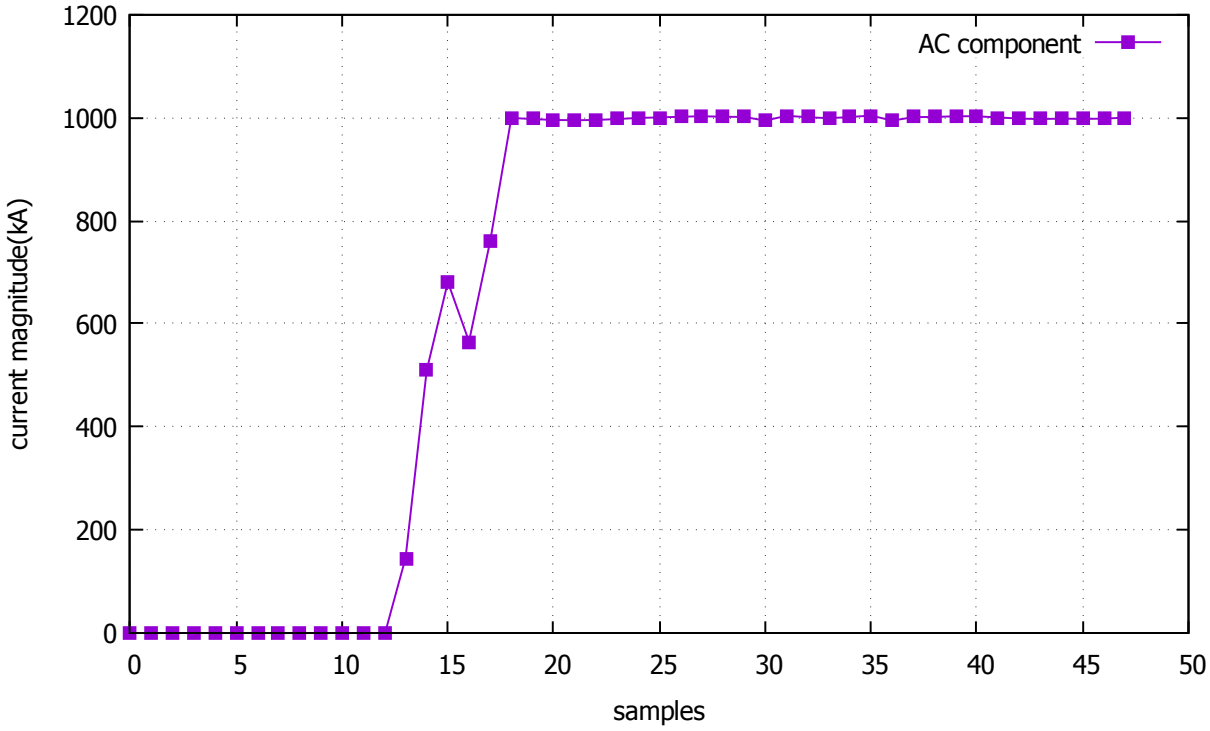

Figure 2.6 Phasor estimation using LES method(window size=7)

to converge. Thus, these two methods both meet the half cycle convergence time, which means the steady state value is reached before the 20th sample. However, the seven-sample-window has a better filtering performance, which avoids the oscillation to occur from 31st to 36th sample in the five-sample-window method.

2.7 Distance Relay Operating Characteristics

2.7.1 Concept of Distance Relay

Distance relays are used to protect transmission lines. They issue trip commands responding to the impedance between relay location and fault location. The reach of a distance relay can be divided into three zones, which are Zone 1, Zone 2, and Zone 3. The three zones are progressively increasing in the distance, which is shown in Figure 2.7. Typically, Zone 1 protects 80% length of the line; Zone 2 can protect 120% of the whole length of the line, while zone 3 protects the whole line plus 120% of the longest adjoining line. Generally, Zone 1 is primary protection for the local transmission line, so it operates at the fastest speed, while Zone 2 and Zone 3 are back-ups for Zone 1 to increase protection reliability. Since the objective of this research is to speed up the trip operation, the performance and characteristics of Zone 1 are discussed.

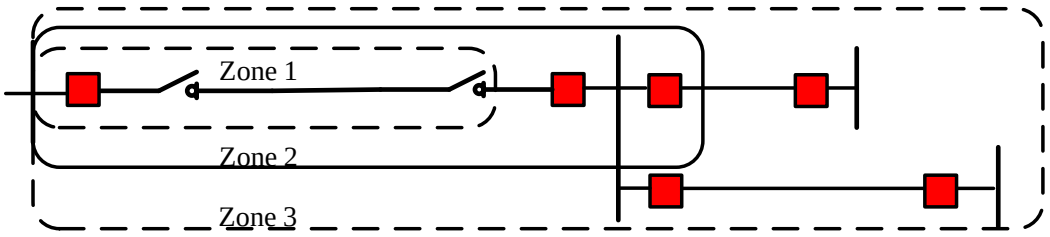

Figure 2.7 Three protective zones of distance relay

2.7.2 Distance Relays Types

According to the operational mode and attributes of the protected transmission lines, there are four general distance relay types which are recognized from the shapes of their operating zone. The diagram used to show the characteristic of a relay is so-called "impedance diagram"or "R-X diagram", which is shown in Figure 2.8. Regarding their characteristics, the impedance relays are basic distance relays type, the mho relays are impedance relays plus directional element, and the reactance/quadrilateral relays are more preferred when protecting short lines as they have better resistive coverage.

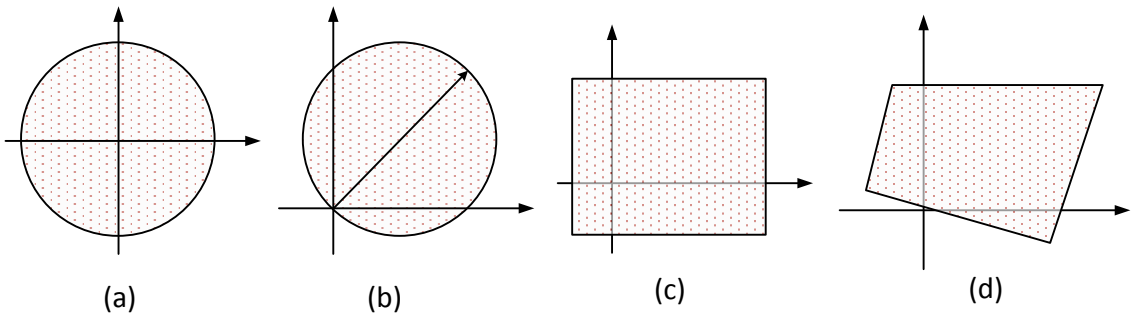

Figure 2.8 Types of distance relay:(a) impedance relays, (b) admittance or mho relays, (c) reactance relays, and (d) quadrilateral relays

2.8 Emulation Methodology

The main work in this research consists of two parts, verification of the LES algorithm on MATLAB and implementation of hardware on FPGA board. The design philosophy and procedure of first part is presented in this section, and the second part will be presented in Chapter 4.

2.8.1 Matlab Design Flow

Before prototyping the LES-based distance relay on FPGA platform, the validation and optimization of LES algorithm with MATLAB are first completed. The simulation of a transmission line and generation of the fault data is also involved in this part. The design

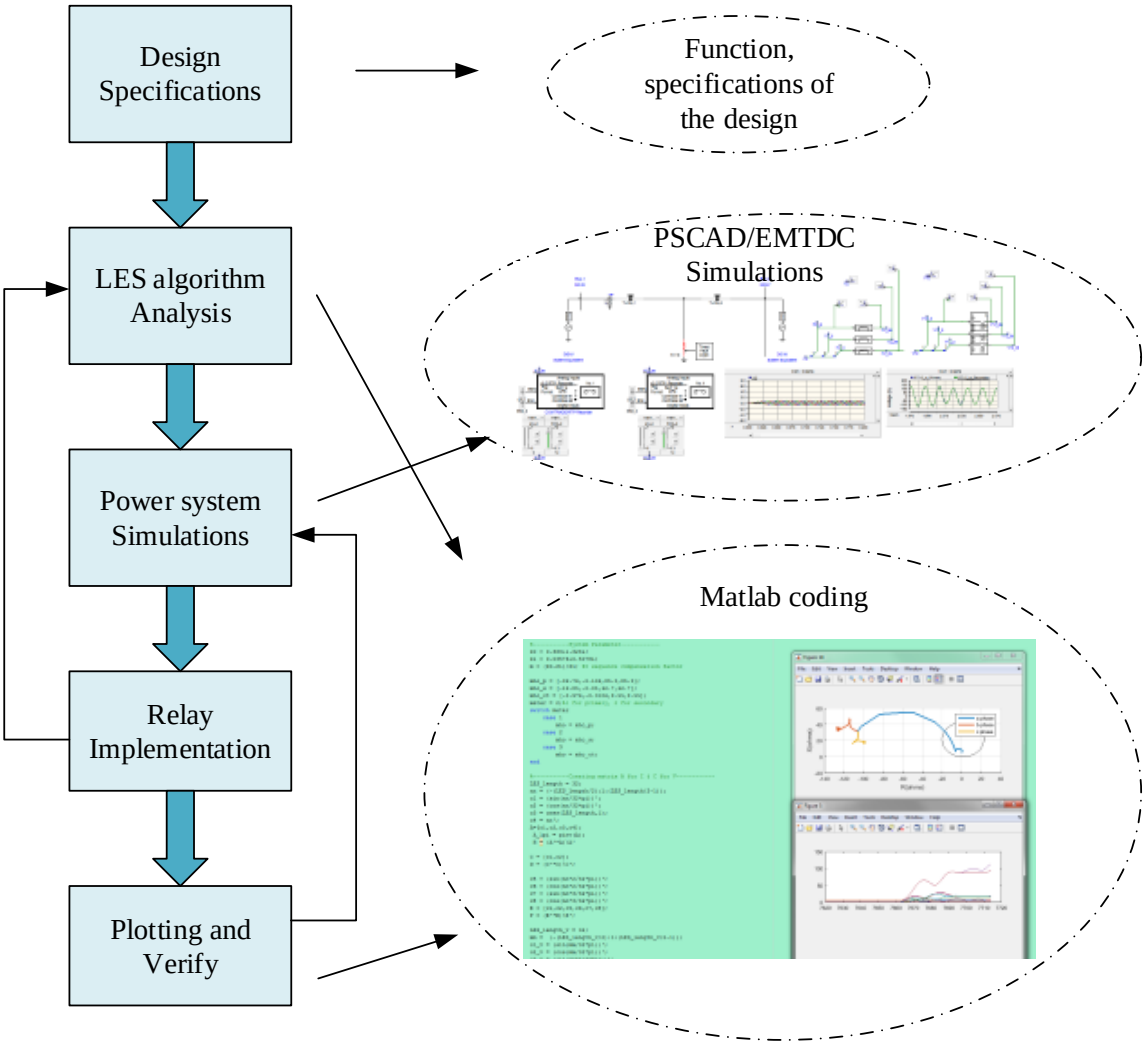

Figure 2.9 Flow chart of design on Matlab

flow is shown in Figure 2.9, and the main five steps are explained as follows,

• **Design Specification**: The first step to undertake is understanding the requirement and standards of the design, then choose the development platform and associated tools. Since MATLAB is a mature and comprehensive platform, this part is relatively easier than the FPGA part. The main work is to break down several modules according to the relaying function, determine the description about each module's architecture, data flow, and the control signals.

• **LES algorithm analysis**: Based on the performance and reliability analysis of the results, modify and configure different parameters such as the windows size and convergence threshold.

• **Power system Simulation**: Create a two-bus transmission line system in PSCAD/EMTDC®, collect fault data for different scenarios and record the data into COMTRADE format files.

• **Relay Implementation**: Follow the mho characteristic of distance relay, calculate the phase-to-phase, and phase-to-ground protection elements with the estimation results from LES module, track the loci of impedance in R-X diagram and then make a trip decision.

• **Plotting and Verifying**: Output the results to graphs such as voltage/current phasor diagram, R-X diagram to compare the performance with the other algorithms or techniques.

2.9 Summary

In this chapter, several algorithms are compared with an example, and further analysis regarding LES methods will be discussed in Chapter 3. Since two perspectives are used for speeding up the distance relaying in this thesis, which are algorithm-based and hardware-based. In Chapter 4, the hardware interface will be discussed with more details.

Chapter 3

High-Speed Distance Protective Relay Emulation in Matlab

3.1 Introduction

Within the transmission line protection area, distance protection is the most widely used protective function. The mechanism is based on the evaluation of the fault impedance, which is proportional to the distance between the fault location and the relay.

The main relaying function designed in this research is high-speed distance protective relaying. The LES methodology discussed in Chapter 2, is enhanced for high-speed relaying and at the same to achieve higher reliability. The relaying unit consists of several necessary modules including LES, fault detection, mho elements, and a trip delay routine to accomplish the distance relaying function.

The complete architecture of the LES-based distance relay is illustrated in Figure 3.1. The general operation process is as follows: after obtaining the fault voltage and current signal from off-line simulation data, the LES module estimates the fundamental magnitude and phase angle of the signals. The fault detection module uses the LES results of the current to detect the initiation of a fault, while the mho element module calculates the line impedance and makes a comparison with the reference impedance. If the calculated impedance value

falls into the zone configuration, the trip delay routine module is activated and monitors a couple of steady values to issue a final trip command, which makes the circuit breaker isolate the fault. In this chapter, each module is discussed, with design details presented in the following sections.

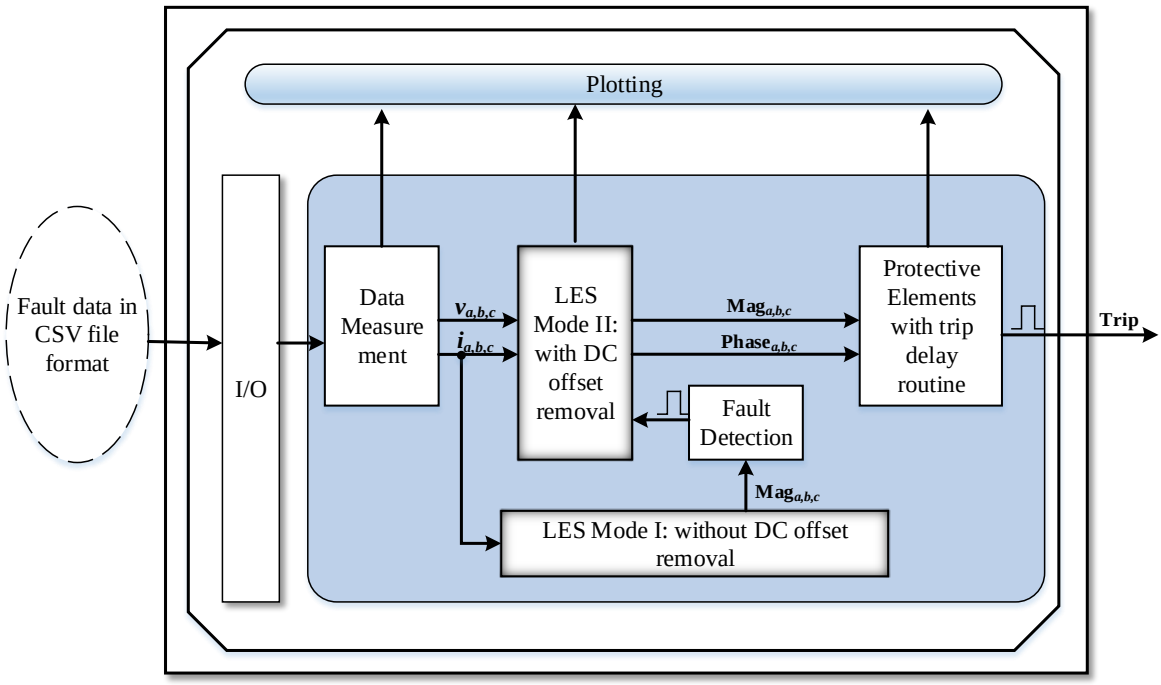

Figure 3.1 The overall architecture of the LES-based distance relay to show (1)the three main modules:fault detection, LES with/without DC offset removal, and protective elements with trip delay routine, and (2) inputs/outputs

3.2 LES Module with DC Offset Removal

3.2.1 Waveforms Measurement

A three-phase power system can have ten distinct types of possible faults: a three-phase fault, three phase-to-phase faults, three phase-to-ground faults, and three double-phase-to-ground faults. To determine the fault type and make different trip decisions, we separately measured three-phase voltage and three-phase current. Generally speaking, two kinds of

sampling rate are used, a lower sampling rate of 64 samples/cycle and a higher sampling rate of 320 samples/cycle; these are respectively 3,840 and 19,200 samples per second in a 60-Hz power system. Due to the high calculation complexity of the matrix-based LES algorithm, a lower sampling rate is utilized in this research. Figure 3.2 shows the current measurement during the pre-fault and post-fault time range. Because it is a three-phase-to-ground fault, there are considerable magnitude surges on all of the three-phase currents.

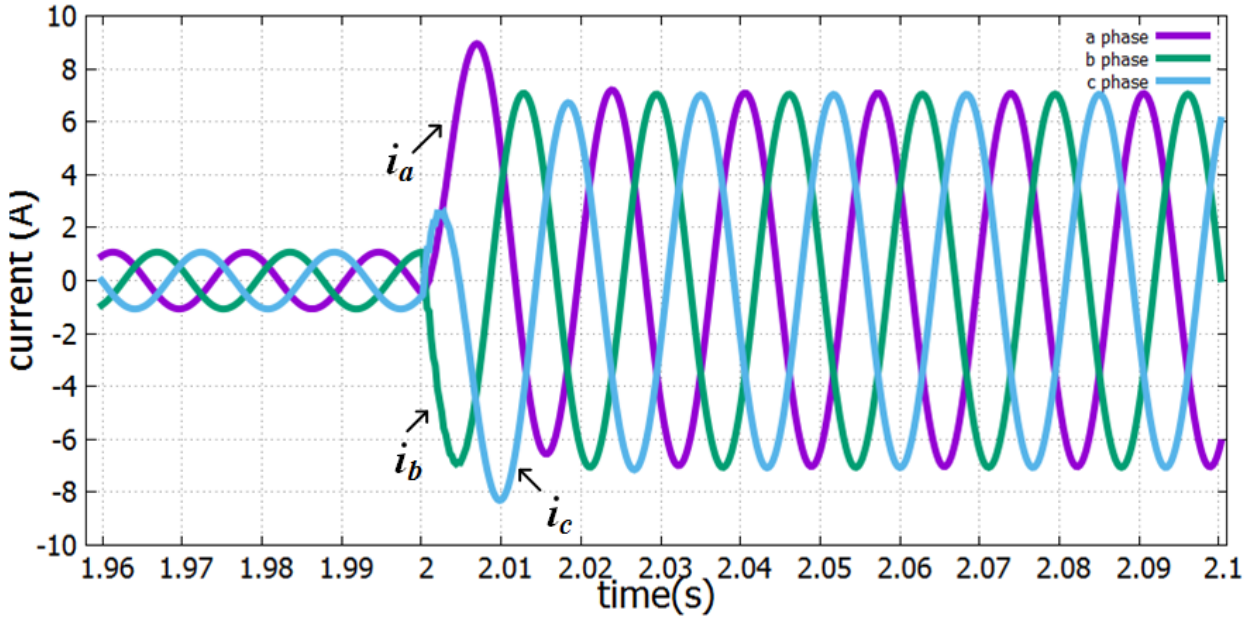

Figure 3.2 Fault data generation

3.2.2 LES Estimation

Implementing the calculation of fault impedance requires the fundamental frequency components of fault voltages and currents, and the moment of initiating the calculation depends on the fault detection results, which are based on the incremental changes in current magnitude. Thus, LES estimation is a continuously running function and needs to operate in two modes: pre-fault and post-fault. In the pre-fault stage, LES estimation is utilized to obtain the current magnitude and the DC offset removal function is turned off, which can reduce the calculation burden and the resource requirements for implementation on FPGA hardware. After the fault detection signal is sent out (details will be presented in the next subsection about how fault detection is done), the LES estimation will be running for both

current and voltage signals. In particular, DC offset removal is activated for fault current data.

The analysis in Chapter 2 shows that an LES window length of less than half of the samples per cycle results in some unsteady variation in the phasor estimation result. On the other hand, shorter window lengths result in better sensitivity for detecting the fault. Therefore, the window length will be 32 samples for a sampling rate of 64 samples/cycle.

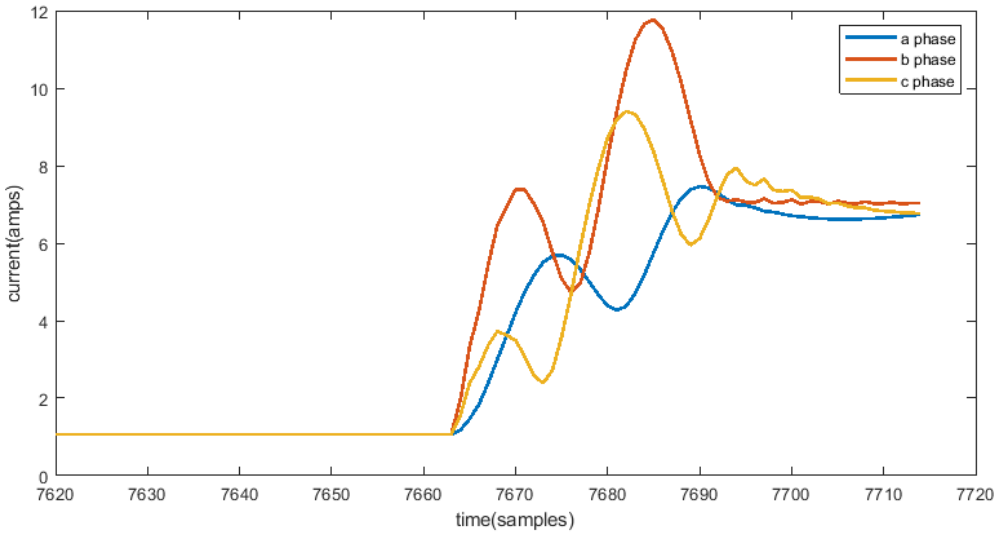

Figure 3.3 LES current phasor for abc-to-ground fault

Figure 3.3 shows the LES estimation procedure for a three-phase-to-ground fault. The system operates normally until a fault occurs at the 7664th sample, the LES estimation then converges at the 7710th sample, so it takes 46 samples (0.72 cycles) to obtain a stable estimation.

3.2.3 Fault Detection

In general, the parameters used to detect the initiation of faults include the magnitude of the current phasor, phase angles of the current and voltage, active and reactive power, frequency of power system, and so on. In this case, the current magnitude is being monitored and tracked to detect the fault and trigger the protection process. This method is based

on the over-current principle. The inputs of the fault detector are the present sequence currents and the corresponding measurements from two cycles earlier, as shown in Figure 3.4. The magnitude of the changes in these currents are evaluated against two times the cut-off threshold, which is set at 2% [32] of the steady-state value. If the change in any sequence current exceeds the limit, this demonstrates the transmission line is exposed to an irregular situation and a fault detection signal is issued.

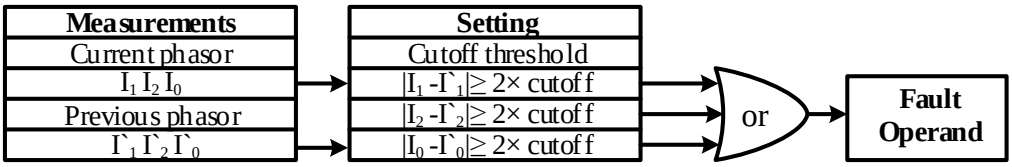

Figure 3.4 Logic implementation of fault detection. $|I_1|'$,$|I_2|'$, and $|I_0|'$ are previous phasor magnitudes from two cycles earlier.

3.2.4 Protective Elements

The relay in this research is designed to protect a transmission line with six impedance protection elements: three phase-to-ground elements and three phase-to-phase elements. Table 3.1 shows the apparent impedance calculation equations for different fault types. The factor m_0 is known as a compensation factor, which compensates the phase current for the mutual coupling between the faulted phase(s) and the other two (one) normal phases. All six of these elements are calculated after the fault detection signal is received. When a certain type of fault occurs, one or more of these elements will be activated to swing with a trajectory in an impedance diagram, the details of which are discussed in the next subsection.

3.2.5 Mho Trajectory

The protective elements that would be activated for a fault can be analyzed by looking at the impedance trajectory of the impedance value of the three phases and the moment when it encroaches into the mho characteristic figure (discussed in Section 2.6.2). By utilizing only

Table 3.1 Impedance equations based on different fault types

Relay elements	Impedance formula
a-g	$V_A/(I_A + 3m_0 * I_0)$
b-g	$V_B/(I_B + 3m_0 * I_0)$
c-g	$V_C/(I_C + 3m_0 * I_0)$
a-b	$(V_A - V_B)/(I_A - I_B)$
b-c	$(V_B - V_C)/(I_B - I_C)$
c-a	$(V_C - V_A)/(I_C - I_A)$

I_0 is zero sequence current calculated from $(I_A + I_B + I_C)/3$; $m_0 = (Z_0 - Z_1)/3Z_1$; Z_0 and Z_1 are the zero and positive sequence line impedance from the relay location to the protection zone, respectively.

two quantities, R and X (or Z and θ), the confusion introduced using the three quantities E, I, and θ is avoided. A mho relay is selected because the transmission line is long and EHV type (reactance value is much greater than the resistance).

In general, there are three protection zones from zone 1 to zone 3 covering overlapped and extensive reach in one distance relay; moreover, they need to be set and coordinated to operate together to make sure the transmission line is protected with back up. Because this research is focussed on the high-speed feature of relays, only zone 1 is involved.

The impedance setting of the relay can be determined according to the following principle: if Z_L is the positive impedance of the transmission line, and zone 1 protects 80% of the length of the line, n_i and n_e are the current transformer (CT) and voltage transformer (VT) turns ratios, then relay setting Z_r equals $0.8 \times Z_L \frac{n_i}{n_e}$. The final mho characteristic is a circle passing through the origin with a diameter equal to $|Z_r|$.

After a fault occurs, the fault impedance Z_f will be calculated according to LES estimation of the voltage and current in every sampling step, so the Z_f is visualized as a trajectory moving in the R-X diagram. If the trajectory hits and settles into the mho characteristic circle, then it means that the fault happens in the zone 1 protection reach. For example,

Figure 3.5 shows the mho trajectory for a three-phase-to-ground fault. Note that every time interval between two marks on the loci is a sampling step equal to 260 μs.

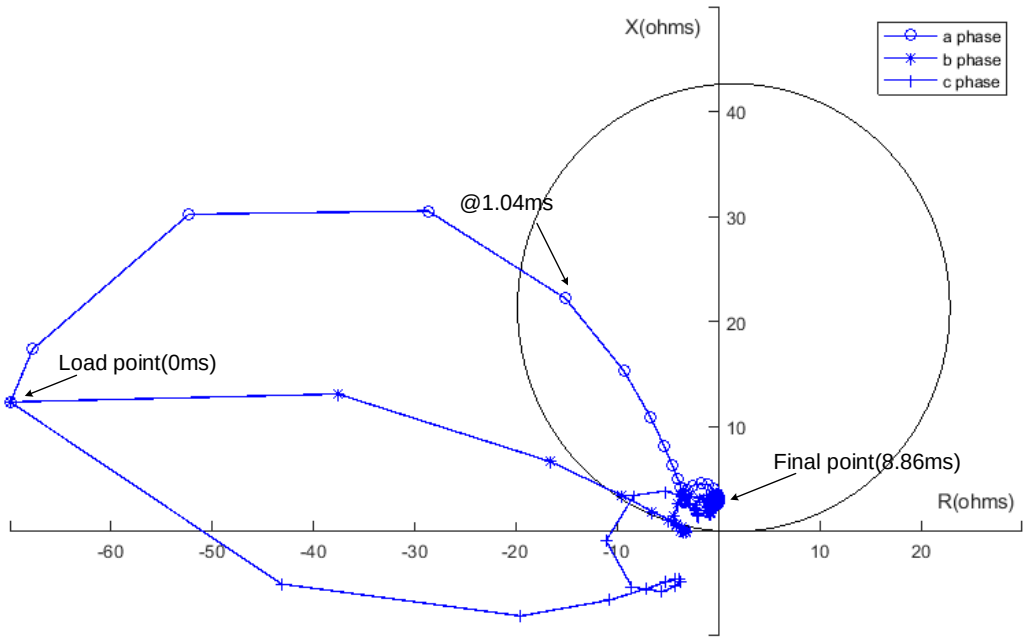

Figure 3.5 Mho trajectory for phase abc-to-ground fault

For the impedance comparison logic on a computer, the software calculates the angle between fault vector Z_f and operating vector $Z_o = Z_f - Z_r$. As can be seen from Figure 3.6, if the angle is greater than or equal to 90° then the fault impedance Z_f is within or on the mho circle, meaning the calculated impedance is under-reaching the zone. In this case, the relay will issue a trip decision (with a trip delay routine) to the circuit breaker to isolate the fault. For example, with two vectors ready, $Z_o = a + jb$ and $Z_f = c + jd$, the angle between them can be derived from $cos\theta = \dfrac{Z_o \cdot Z_f}{|Z_o||Z_f|}$, where $Z_o \cdot Z_f$ is the inner product of the two vectors in a Cartesian coordinate system. As the cosine value of 90° is zero, the sign of the cosine value, determined from the $Z_o \cdot Z_f$ part that is $ac + bd$, can be an ideal indicator to determine whether the fault impedance is inside the mho circle zone.

3.2.6 Trip Delay Routine

This feature is activated when the impedance trajectory enters into the mho circle at any time. It then waits for a subsequent few sample calculations and evaluates two conditions: (i) if the magnitude of change in impedance is small enough and (ii) if the following consecutive impedances are also located inside the mho circle. If both of the conditions are met, a trip decision will be issued; otherwise, the trip delay routine is reset to wait for the next activation.

3.3 Case Study and Results

To verify the effectiveness of the proposed distance relay design, we simulated several typical types of faults on a test power system, and used PSCAD/EMTDC ® to generate the fault data. These off-line data are then fed into the target relay for testing and verification. The validated system consists of two synchronous generators and one transmission line, which is 210 km long. The system is shown in Figure 3.7 with parameters given below.

V_{base} = 345 kV, S_{base} = 100 MVA, fault impedance = 0.001 Ω.

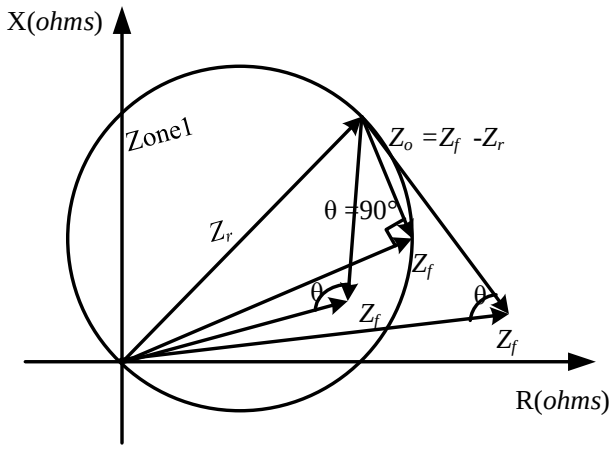

Figure 3.6 Impedance comparison method

Source parameters: Z_s = 9+j37.7 Ω, E_{s1} = 345∠ 0°, E_{s2} = 345∠ 30°.

Transmision line length: 210 km.

Transmision line sequence impedance (Ω/km): Z_0 = 0.363+j1.323, Z_1 = 0.0358+j0.5078, Z_2 = 0.0358+j0.5078.

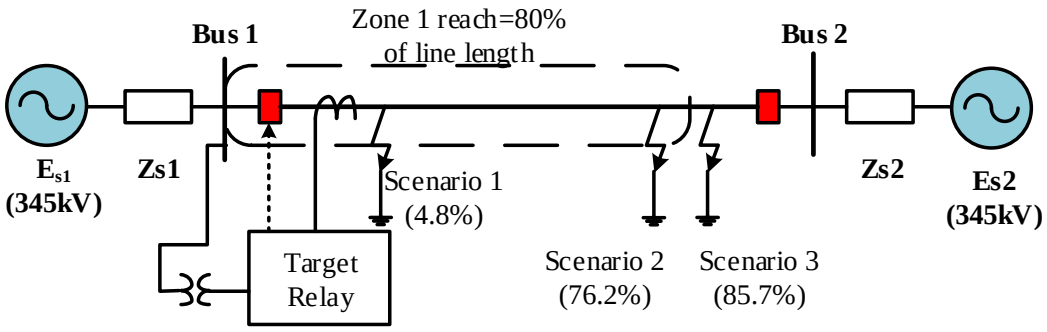

Figure 3.7 Test project of transmission line in PSCAD

The proposed distance relay is tested for three scenarios of different fault locations, and each scenario consists of four fault types; therefore, there are twelve test case combinations. Figure 3.7 shows the configurations of three locations. For example, the first test case is a single-phase-to-ground fault which occurs at 10 km away from the relay location. The oscilloscope traces simulation data of fault during the transient state, which are given in Figure 3.8 and 3.9 with the time range from t=1.85 s to t=2.2 s. When the phase-a-to-ground fault happens at t_f =2 s, the consecutive increase in i_a with its DC offset, and decrease in v_a can be observed.

The results with the LES for the fault current magnitude are shown in Figure 3.10. The current magnitude in Segment I stays constant under normal operating steady-state until at t=7664 sample when a ground fault happens. In Segment II, the i_a magnitude starts to increase after a noticeable oscillation. It takes 36 samples or 9.38 ms in Segment II, which is from 7,664th to 7,700th sample, for LES module to obtain a stable current magnitude value. The smoothness in Segment III indicates that DC offset is effectively removed from the fault

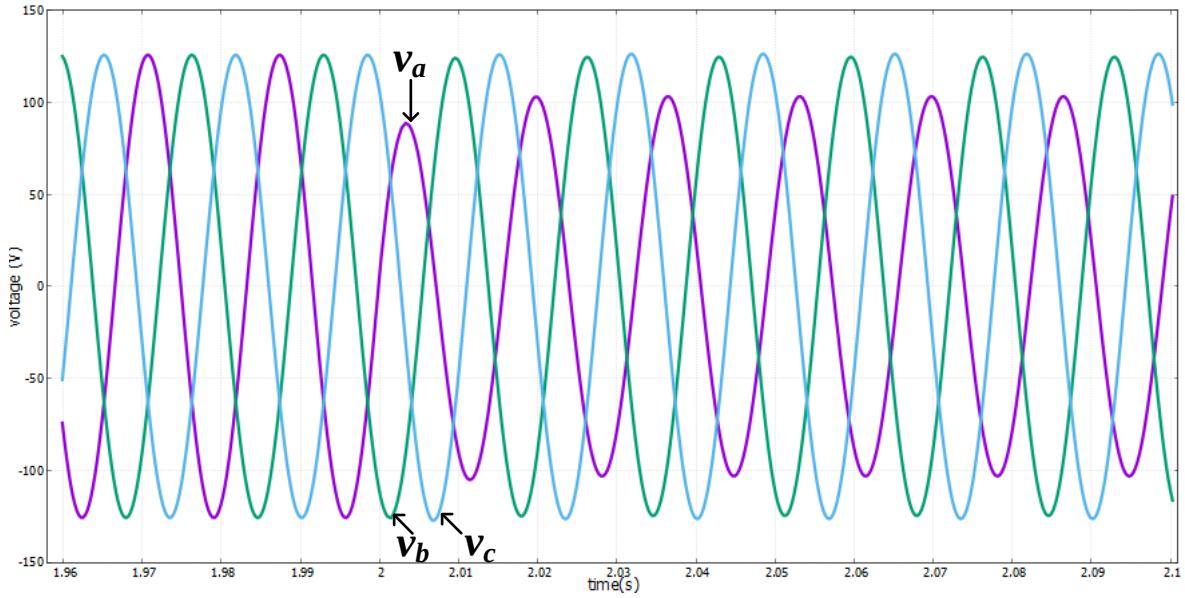

Figure 3.8 Real-time voltage waveform for a single-phase-to-ground fault

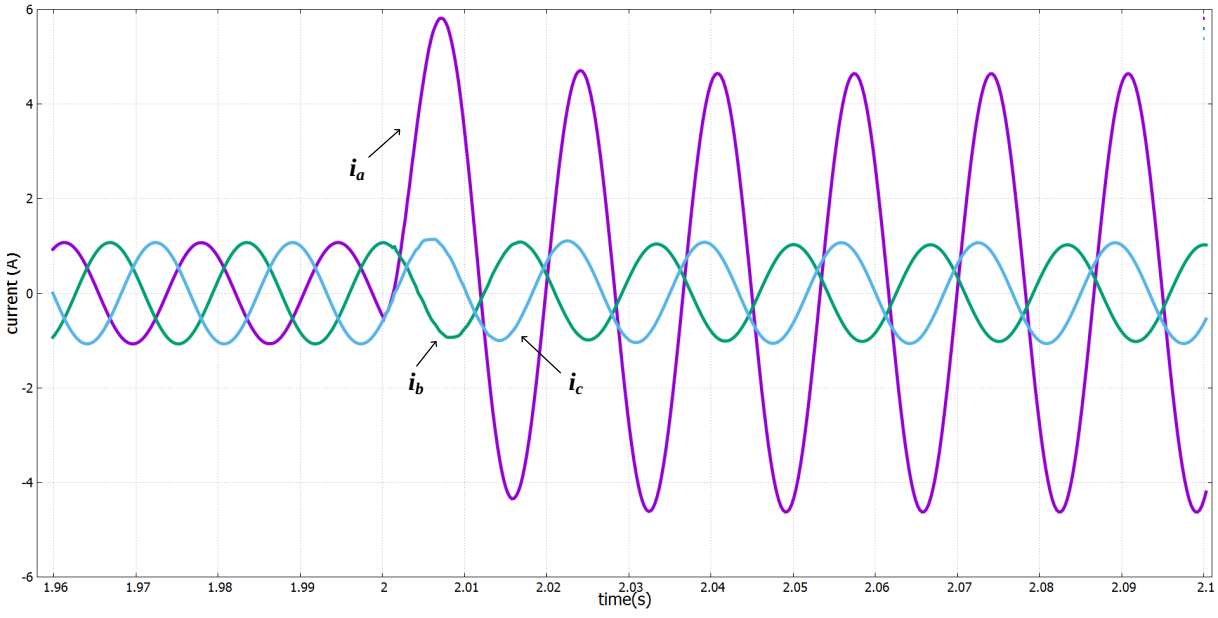

Figure 3.9 Real-time current waveform for a single-phase-to-ground fault

current during the faulted state. The fault detection module is activated when the increase on three sequence current magnitudes meet the 2% criteria discussed in Section 3.2.3.

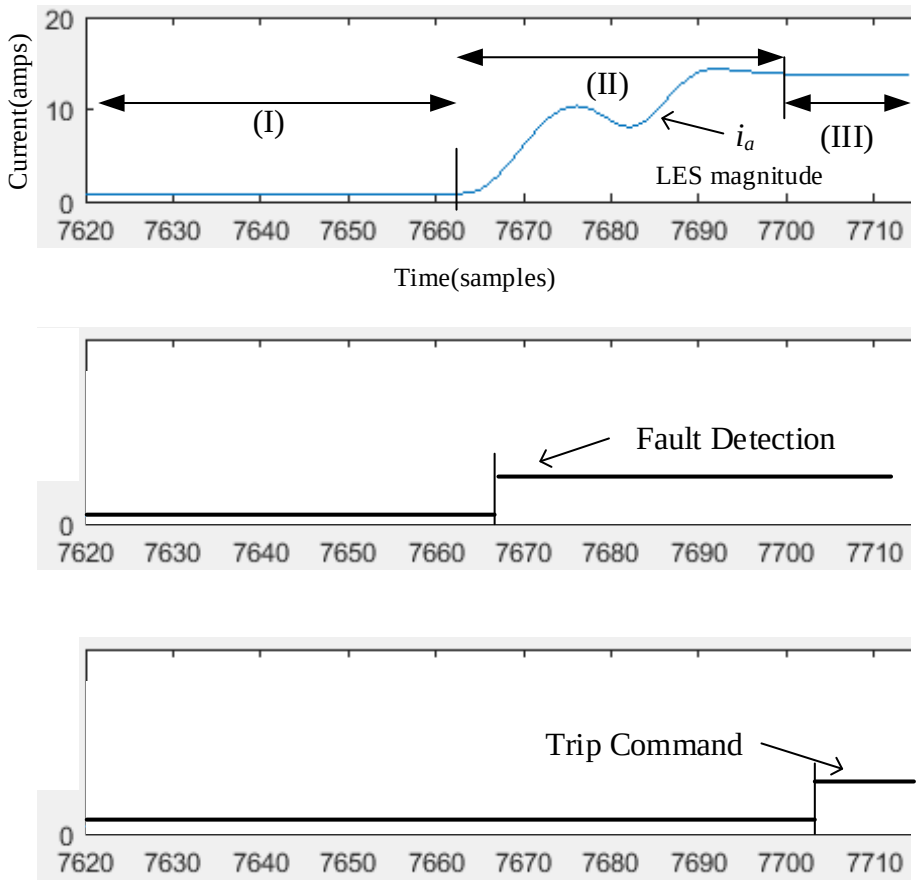

Figure 3.10 LES results, fault detection and trip signal for a single-phase-to-ground fault

Figure 3.11 to 3.22 show the trajectory of the apparent impedance observed by the relay during the fault for the three scenarios, which are (1)close to the relay, barely (2)within and (3)beyond the relay zone setting reach. The zone reach is 80% of the line length, which means Z_r is equal to 3.004+j42.7 Ω.

(1) **Scenario 1** (Fault occurs at 10 km, which is 4.8% of transmission line)
Before the fault occurs, the steady state impedance -66.7+j12.8 Ω is outside the mho characteristic circle. After a phase-a-to-ground fault is initiated, the phase-a impedance trajectory enters into the circle and converges to its final new steady state of -1.2+j4.8 Ω. When the trip delay routine check succeeds, which means the magnitude change of impedance is less than 1% and the operating point is staying within the zone circle for five samples, then the relay will issue a final trip signal at 30th sample, or tripping duration equals to 7.81 *ms*. Furthermore, for the phase-a-to-ground fault, only the impedance of phase-a moves into the circle, while the other two phase impedance loci stay at the original area during the pre-fault and post-fault period.

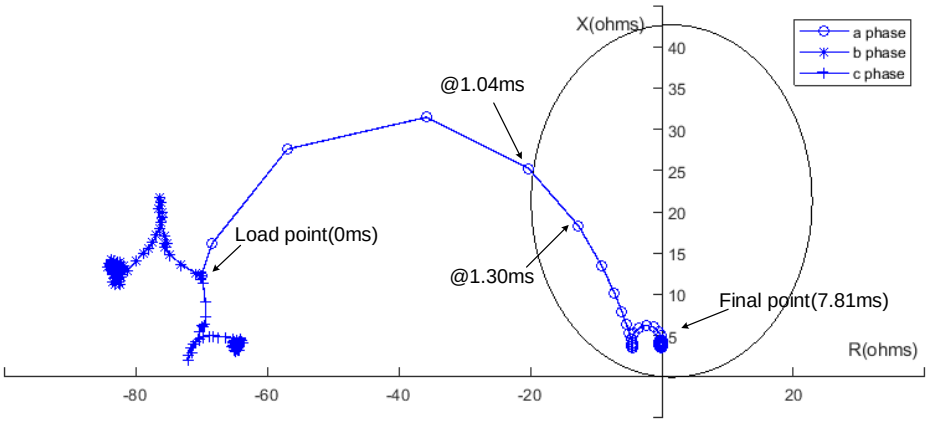

Figure 3.11 Impedance trajectory of a-to-ground fault

A similar situation also fit the three-phase-to-ground fault and two-phase-to-ground fault. Figure 3.12 and 3.13 show that the corresponding impedances enter into the circle when specific faults occur.

For the phase-to-phase fault, the impedance calculated should be phase-to-phase instead of the phase-to-ground element. Figure 3.14 shows the result. The tripping time of the four types of fault are shown in Table 3.2, and all of them meet the sub-cycle requirement.

(2) **Scenario 2** (Fault occurs at 160 km, which is 76.2% of transmission line)

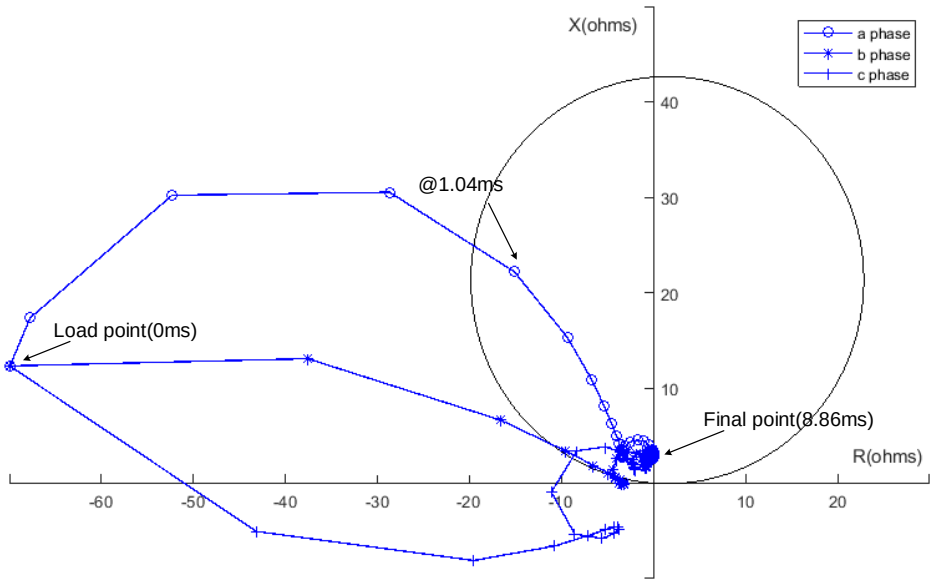

Figure 3.12 Impedance trajectory of three phase fault

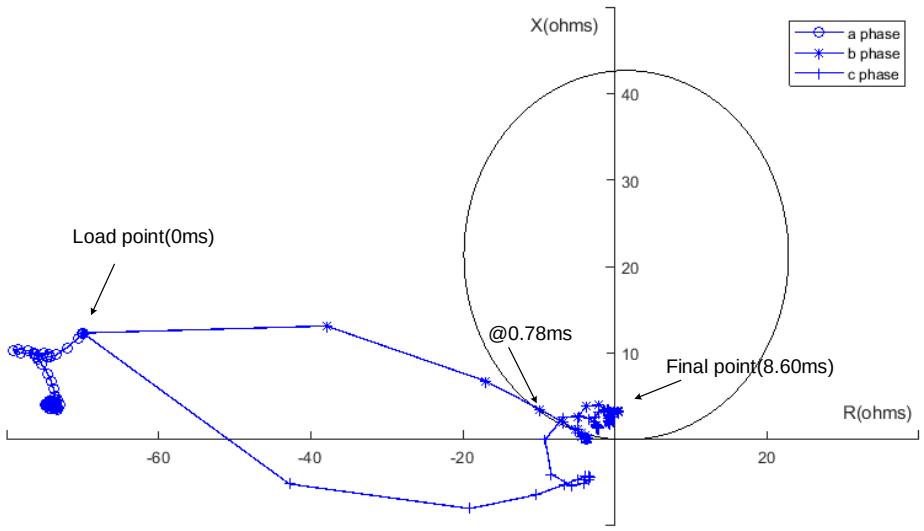

Figure 3.13 Impedance trajectory of bc-to-ground fault

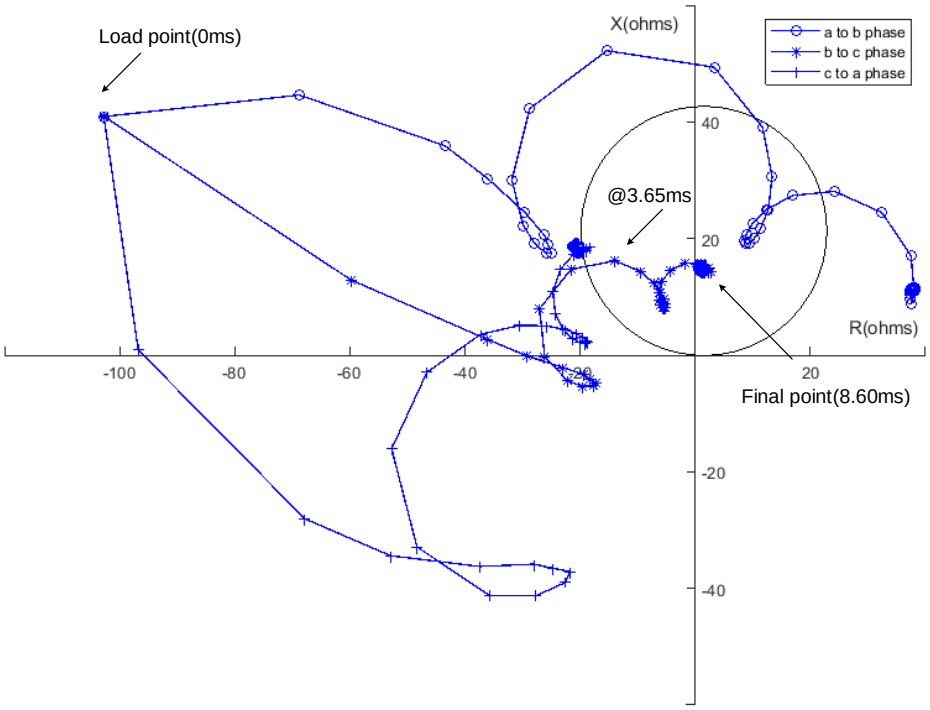

Figure 3.14 Impedance trajectory of b-to-c fault

Table 3.2 Tripping time of scenario 1

Fault Type	**First Tripping Delay Activated**	**Second Tripping Delay Activated**	**Tripping issued at**	**Time in ms**	**Time in cycles**
3 phase-g	4	no	34	8.86	0.53
a-ground	5	no	30	7.81	0.49
bc-ground	3	13	33	8.60	0.52
b-c	12	no	33	8.60	0.52

The impedance trajectories are shown in Figure 3.15 to 3.18. In this case, since the fault occurs near the relay reach of the transmission line, the impedance trajectory enters the circle but keeps close to the edge of the circle. The tripping time of the four types are shown in Table 3.3, and all of them meet the sub-cycle requirement.

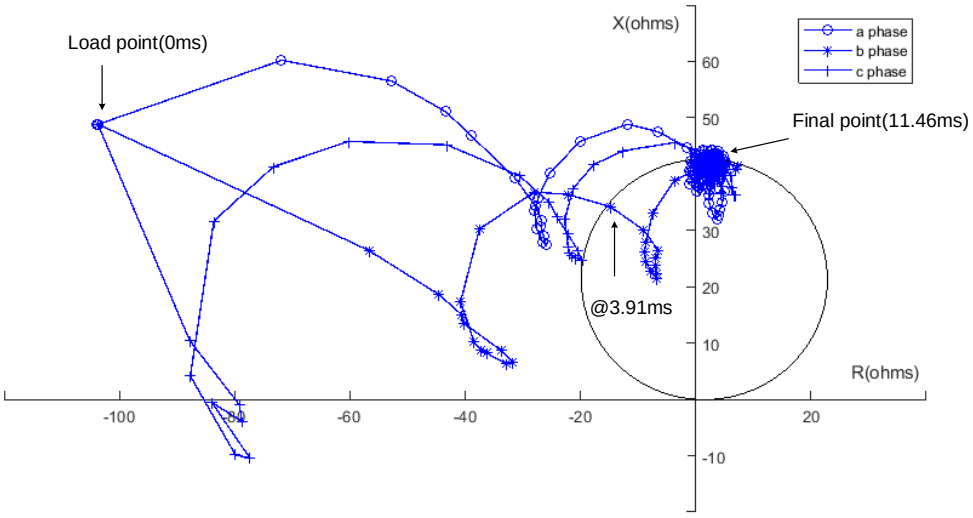

Figure 3.15 Impedance trajectory of three phase fault

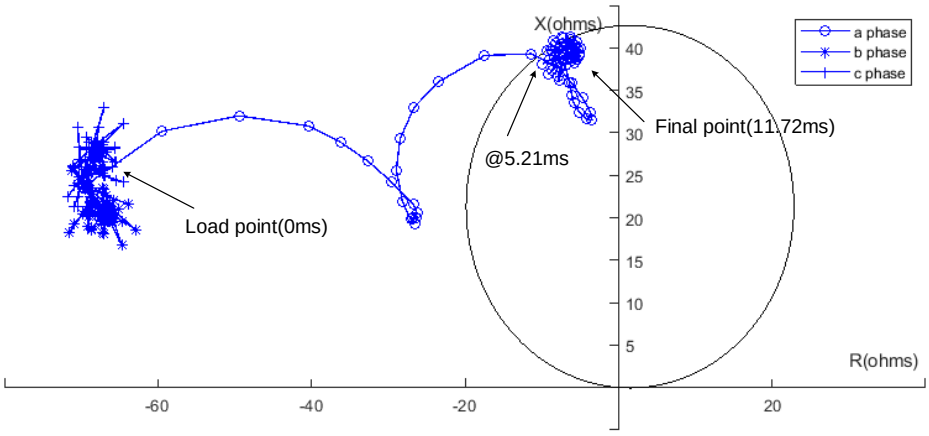

Figure 3.16 Impedance trajectory of a-to-ground fault

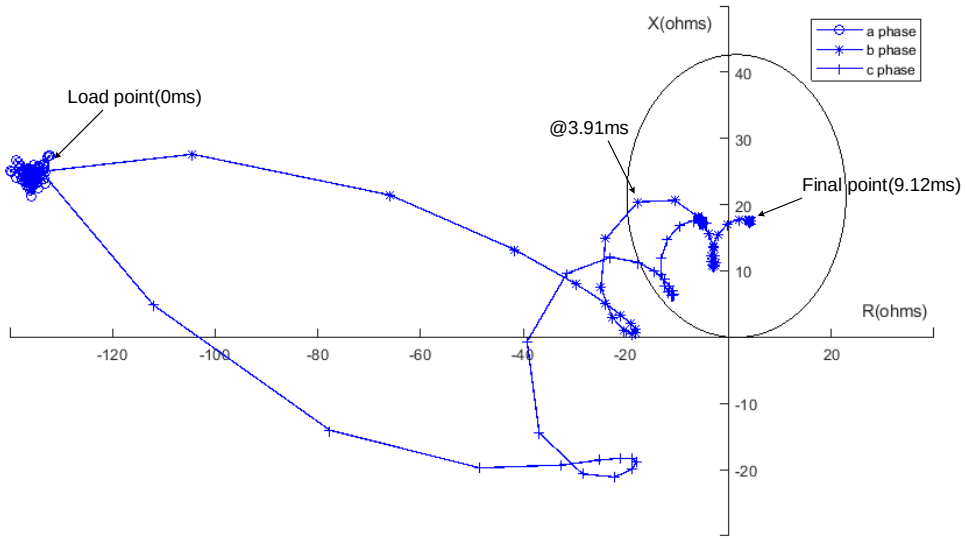

Figure 3.17 Impedance trajectory of bc-to-ground fault

Table 3.3 Tripping time of scenario 2

Fault Type	**First Tripping Delay Activated**	**Second Tripping Delay Activated**	**Tripping issued at**	**Time in ms**	**Time in cycles**
3 phase-g	13	no	44	11.46	0.69
a-ground	18	no	45	11.72	0.70
bc-ground	15	no	35	9.12	0.55
b-c	16	no	35	9.12	0.55

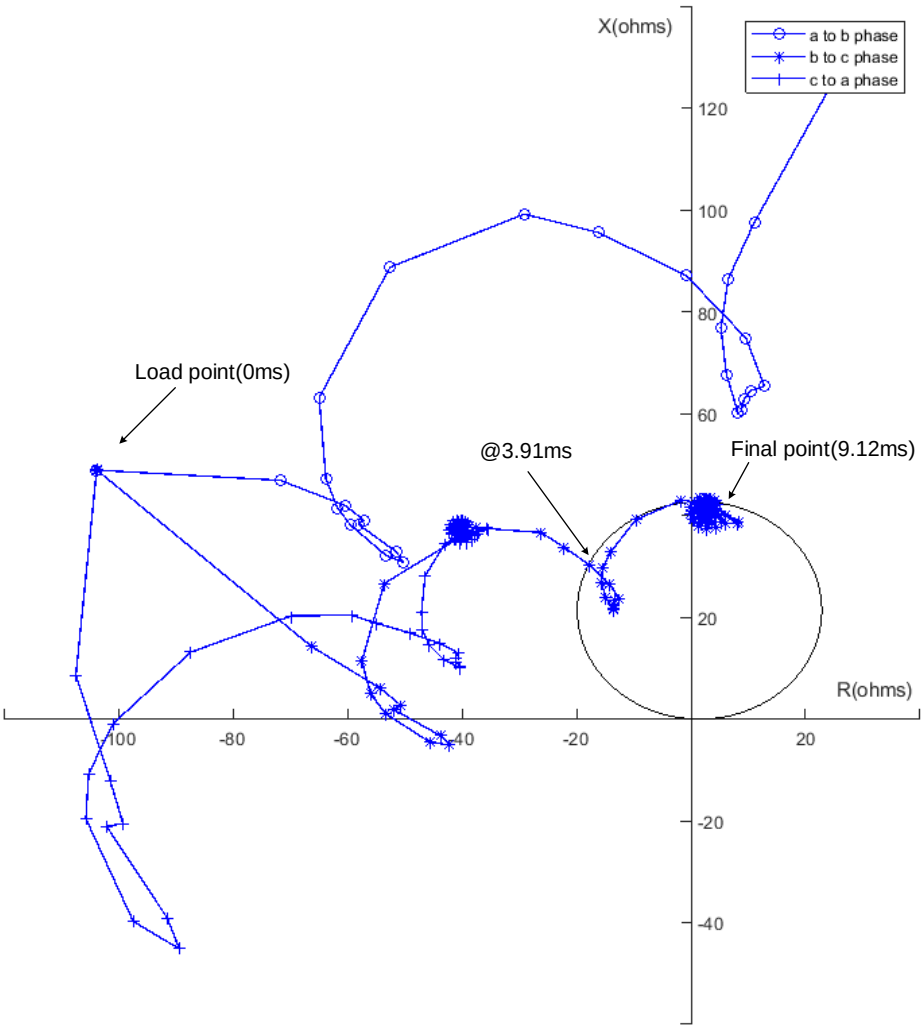

Figure 3.18 Impedance trajectory of b-to-c fault

(3) **Scenario 3** (Fault occurs at 180 km, which is 85.7% of transmission line)

The impedance trajectories are shown in Figure 3.19 to 3.22. In this case, since the fault occurs out of the relay reach of the transmission line, the impedance trajectory does not enter the circle, which means the relay does not trip in this scenario.

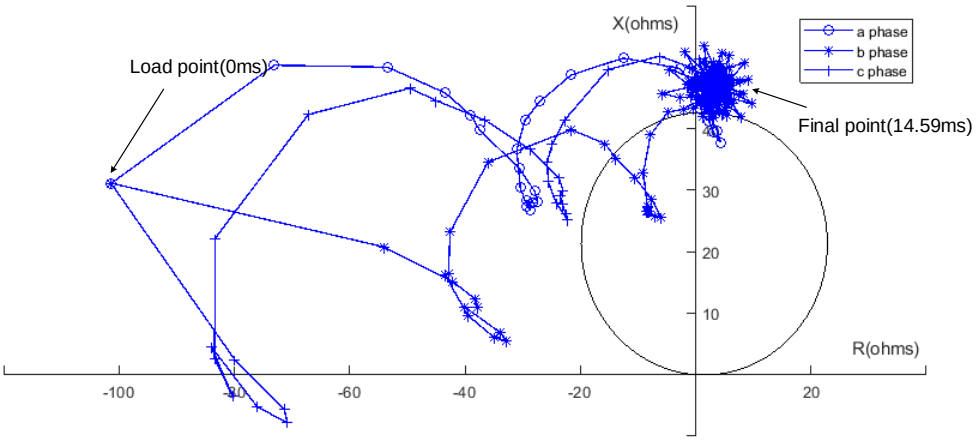

Figure 3.19 Impedance trajectory of three phase fault

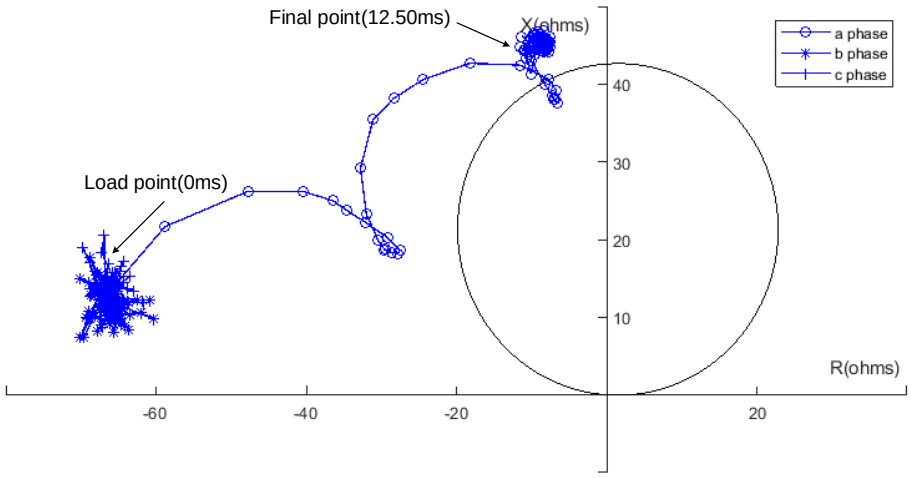

Figure 3.20 Impedance trajectory of a-to-ground fault

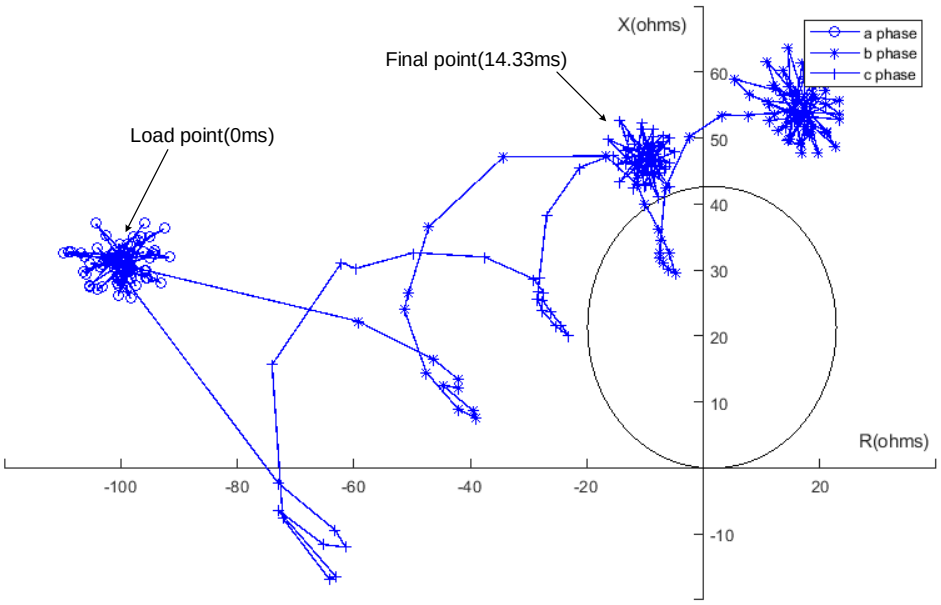

Figure 3.21 Impedance trajectory of bc-to-ground fault

Table 3.4 Tripping time of scenario 3

Fault Type	**First Tripping Delay Activated**	**Second Tripping Delay Activated**	**Tripping issued at**	**Time in ms**	**Time in cycles**
3 phase-g	17	no	no trip	14.59	0.88
a-ground	22	no	no trip	12.50	0.75
bc-ground	17	no	no trip	14.33	0.86
b-c	19	no	no trip	13.02	0.78

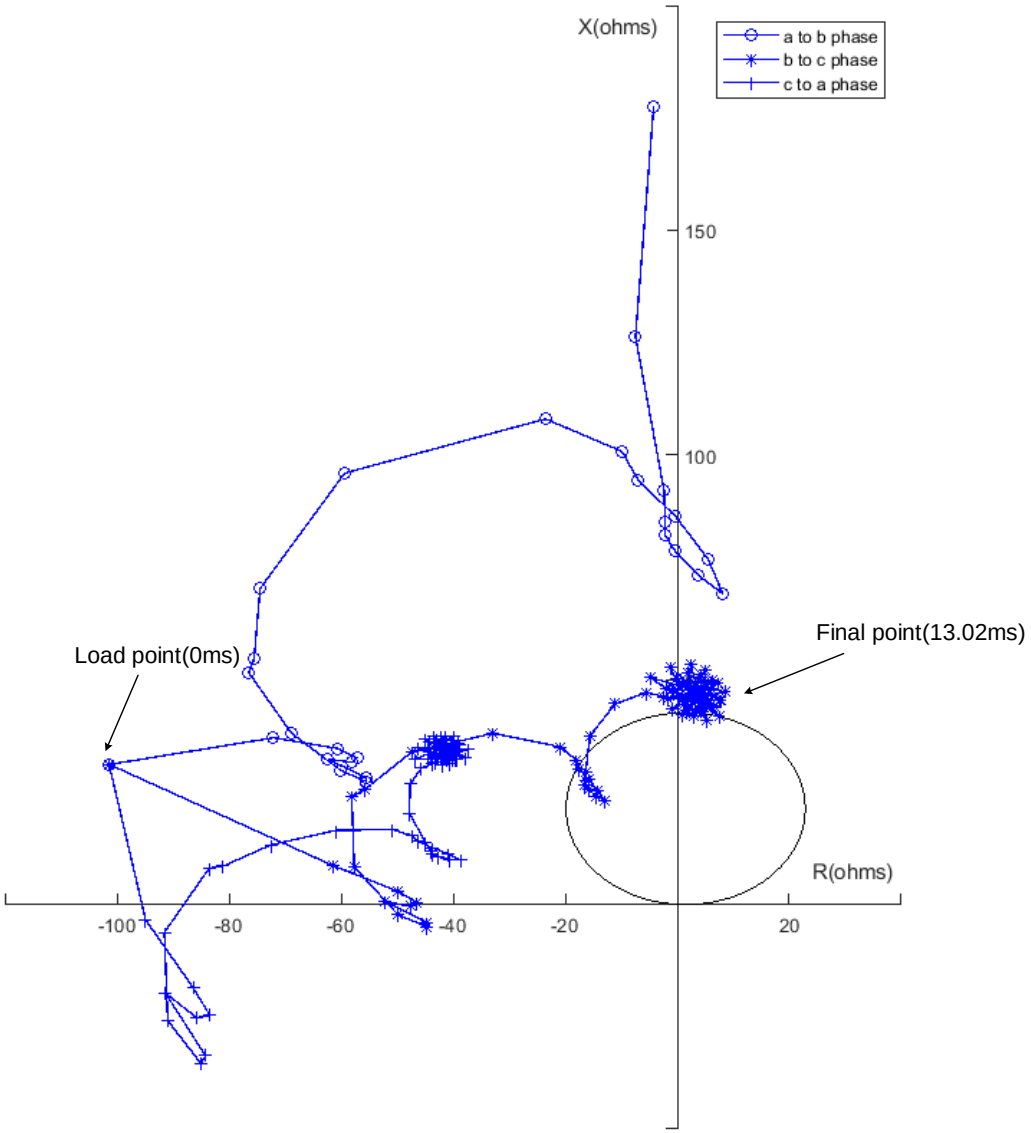

Figure 3.22 Impedance trajectory of b-to-c fault

Table 3.5 Operating time improvement

Fault Type	**Proposed sub-cycle LES (ms)**	**GE D90plus sub-cycle mode (ms)**	**SEL 421 high-speed mode (ms)**	**FC-DFT (ms)**
3 phase-g	11.46	17.50	14.17	22.14
a-g	11.72	17.50	14.17	25.12
b-c	9.12	16.84	13.17	22.89

3.4 Summary

The case studies discussed above show that the LES-based relay has the following features in terms of its performance and reliability:

(1) **Performance**

The most important finding is that, for different fault types and fault locations, the LES method operates within one cycle. For scenario 1 where fault location is at the near end of the relay reach setting, the trip signals are sent out the fastest, at around 0.49 to 0.53 cycles. For scenario 2 where fault location is at the far end of the relay reach setting, the trip signals are sent out at 0.55 to 0.70 cycles. These results are close to the operating time of 0.6 cycles presented in [5], which also uses an LES method and the same sampling rate. In addition, take scenario 2 for example, the proposed LES method is compared with other methods and equipment such as FC-DFT [25], GE D90plus [33] (time-domain short-window orthogonal filters), and SEL-421 [34] (HC-DFT). Table 3.5 shows that the proposed LES method is considerably faster.

(2)**Reliability**

The LES technology correctly responds to different fault types and fault locations. When a specific kind of fault occurs, the corresponding impedance element(s) enter and settle in the mho circle, while the other impedance element(s) stay out of the mho circle. Furthermore, the impedance loci move into the circle when faults occur within the relay reach setting, while the impedance loci stay out of the circle when faults are initiated beyond the relay reach setting.

Therefore, the LES method demonstrates the capability to be applied in high-speed distance protection with respect to both performance and reliability.

Chapter 4

High Speed Distance Protective Relay Implementation

4.1 Introduction

In the previous chapter, the LES-based distance relaying was tested. To use it with the relay hardware, we need to consider some important operational aspects. Besides that, a preliminary distance relaying module is developed on an FPGA board.

4.2 Practical Considerations

4.2.1 CT Saturation

CT saturation is discussed first. Abnormally high primary fault currents, primary fault currents with a DC offset, residual flux, high secondary burden (CT secondary load), or a combination of these factors results in the creation of high flux density in the CT magnetic core. When the density reaches or exceeds the design limits of the core, saturation occurs. At this point, the accuracy of the CT becomes poor, and the output waveform may be distorted. Saturation results in the production of a secondary current that is lower in magnitude than could be indicated by the CT ratio.

Consider a CT ratio is 800:5, and a phase-a-to-ground fault happens at 10% of the relay

reach setting. In this case, CT saturation has an observable impact compared to primary end faults. Figure 4.1 shows that CT saturation barely introduces any waveform distortion within the first one-and-a-quarter cycle after fault initiation. After that period, the distortion is noticeable. Figure 4.2 shows the impedance trajectory of the scenario. Then, we can see that the phase-a trajectory settles within the mho circle at 8.60 ms, just like it does in Scenario 1. However, after one-and-a-half cycles, it will start to swing out of the circle, and it takes five samples for it to swing into the circle again and settle around the original spot. In summary, because CT saturation does not occur instantly, the LES-based relay can operate quickly enough before severe distortion occurs.

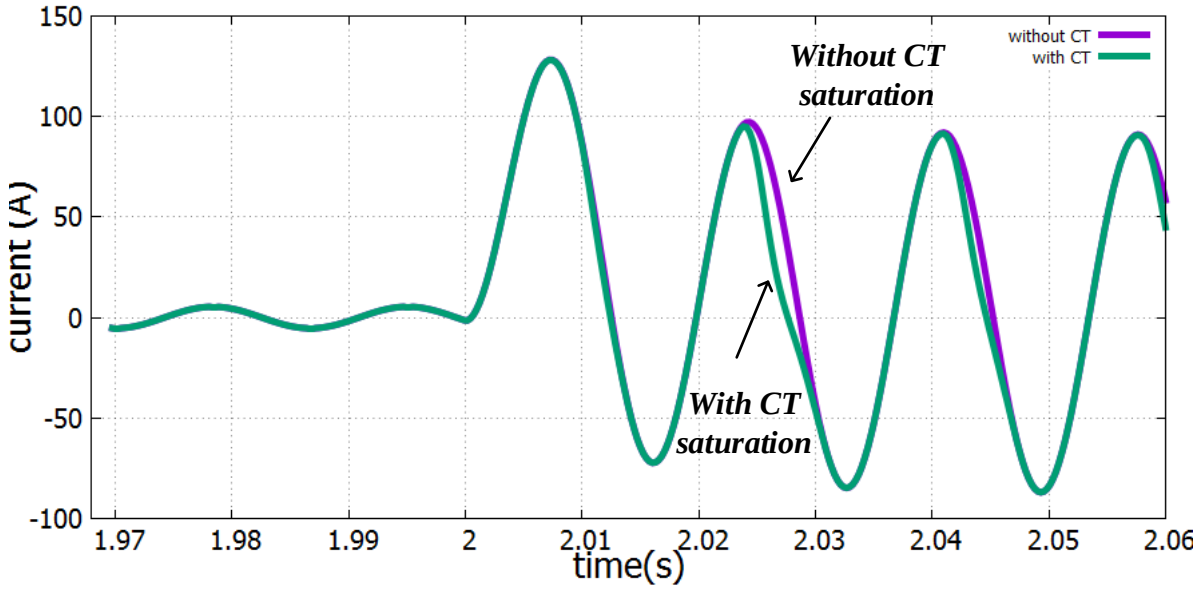

Figure 4.1 Current with and without saturation

4.2.2 CCVT Transient

One of the most common voltage measurements for relaying, particularly at higher voltages, is the CCVT, Coupling Capacitor Voltage Transformers. A capacitor stack is used as a potential divider between the high-voltage apparatus and ground. A typical Lucas model of CCVT is shown in Figure 4.3. Due to the tuned circuit used for compensation of the phase shift between the primary and secondary voltages, the secondary voltages may be significantly different from the primary voltages in waveform during transient conditions.

Furthermore, CCVT output under faulted conditions become lower, so even a small transient component may cause problems for relaying applications. Figure 4.4 shows a single-line-to-ground fault is applied when instantaneous current is at the zero point, the transient waveforms are distorted just after the moment fault occurs. Whereas Figure 4.5 shows the fault is applied when instantaneous current is at the peak point. These two scenarios are the boundaries for all of the possible situations.

In practice, the Source Impedance Ratio (SIR) is a key factor causing voltage to collapse when faults occur. IEEE C37.113, IEEE Guide for Protective Relay Applications to Transmission Lines [35] classifies line length based on SIR as follows,

•Long line (SIR <0.5)

•Medium line (0.5 <SIR <4)

•Short line (SIR >4)

In this case study, three scenarios where SIR = 0.5, 4, and 10 are selected to analyze the

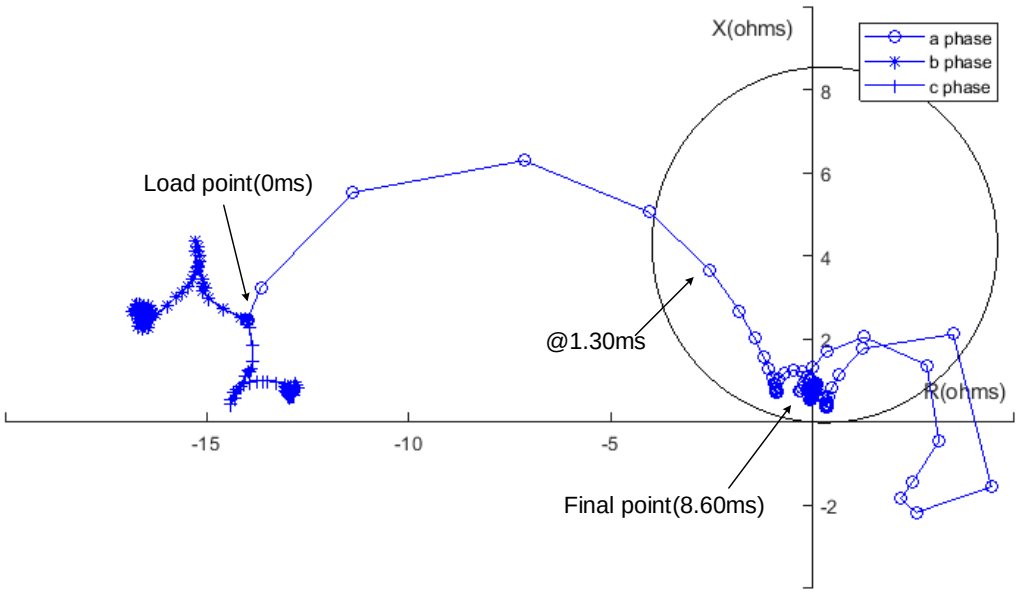

Figure 4.2 Mho trajectory of a-to-ground fault under CT saturation

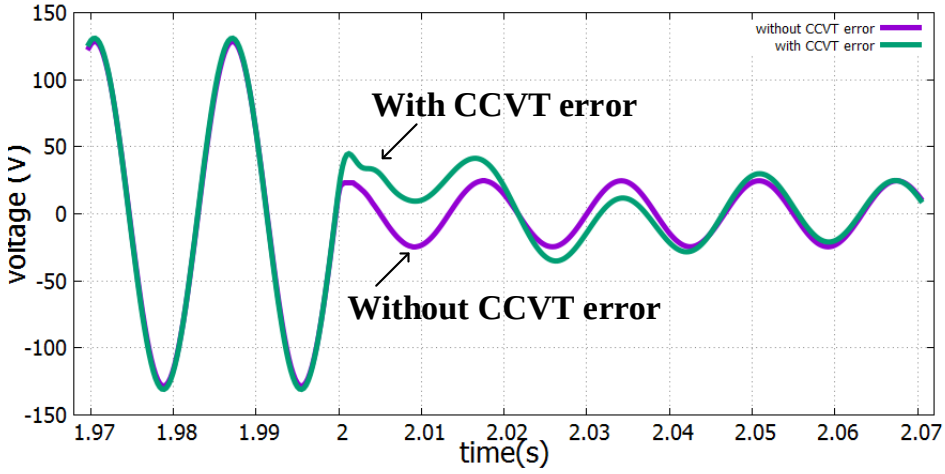

Figure 4.3 Secondary voltage for zero-point-fault

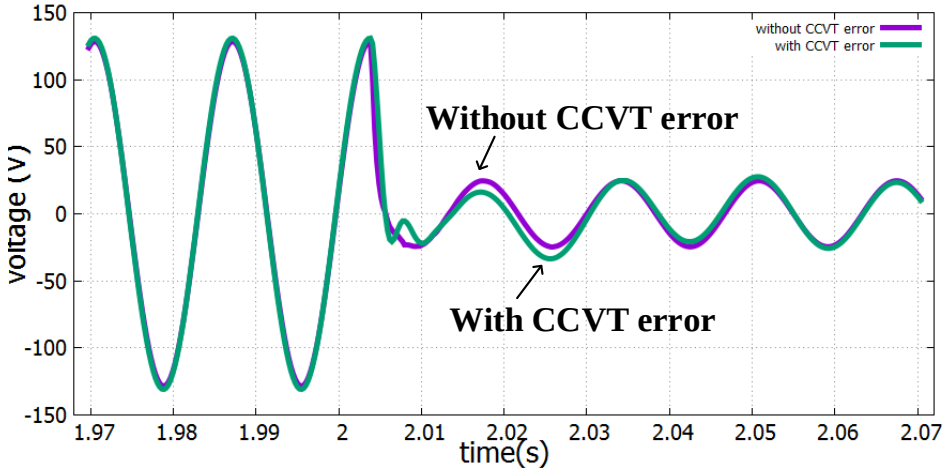

Figure 4.4 Secondary voltage for peak-point-fault

relationship between SIR and relaying performance.

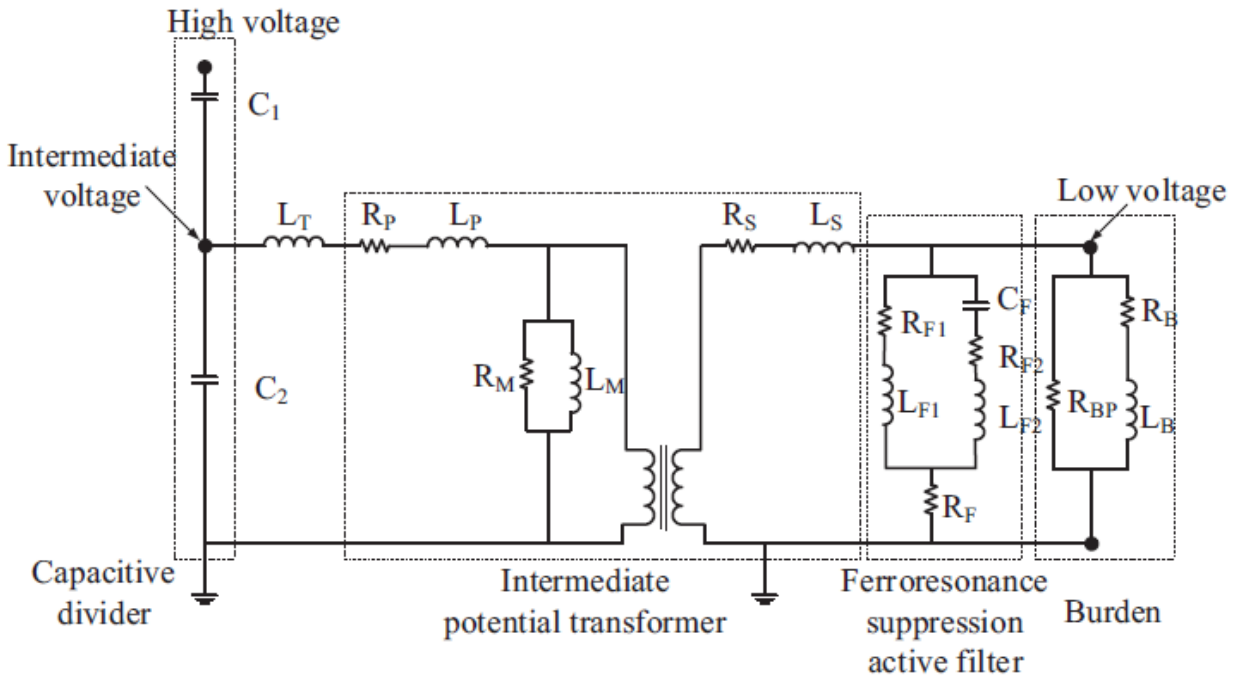

Figure 4.5 CCVT model for simulation

(1) **Scenario 1** (SIR = 0.5, Fault angle= 0 degree)

Figure 4.6 and 4.7 show the impedance trajectories in this scenario, where CCVT is a presence or not respectively. It can be noticed that the loci start from the same point, it takes more 2.35 ms for the loci with CCVT to swing into the circle and more 0.78 ms to settle into a stable value.

(2) **Scenario 2** (SIR = 4, Fault angle= 0 degree)

Figure 4.8 and 4.9 show the impedance trajectories in this scenario. Comparing these two loci, it takes more 1.82 ms for the loci with CCVT to settle into a stable value. Moreover, as the SIR becomes greater, the loci in Figure 4.9 has one more curve than it in Figure 4.7 of Scenario 1, which causes the convergence time to be longer.

(3) **Scenario 3** (SIR = 10, Fault angle= 0 degree)

Figure 4.10 and 4.11 show the impedance trajectories in this scenario. In this case, the addition curve in Figure 4.11 becomes much bigger than in Figure 4.9 so that the impedance

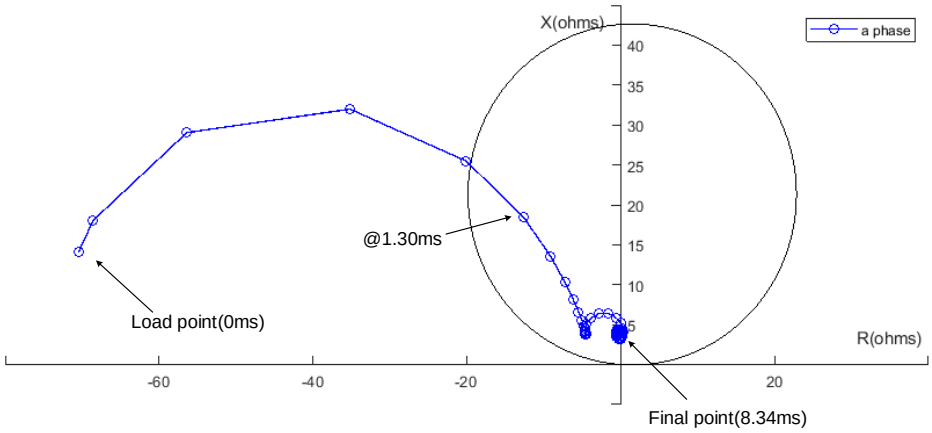

Figure 4.6 Mho trajectory of zero-point fault in transmission line which SIR = 0.5, no CCVT

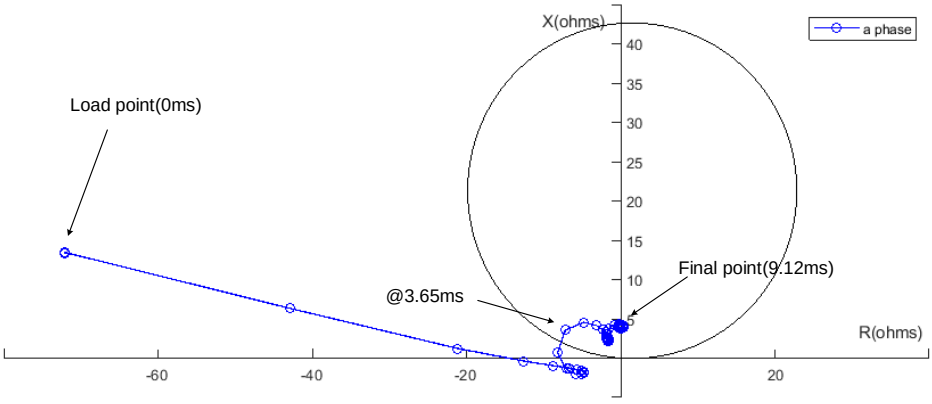

Figure 4.7 Mho trajectory of zero-point fault in transmission line which SIR = 0.5, with CCVT

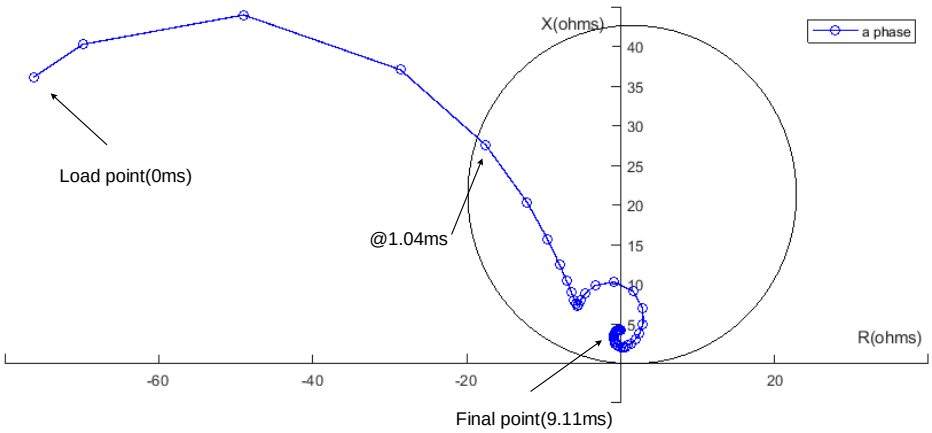

Figure 4.8 Mho trajectory of zero-point fault in transmission line which SIR = 4, no CCVT

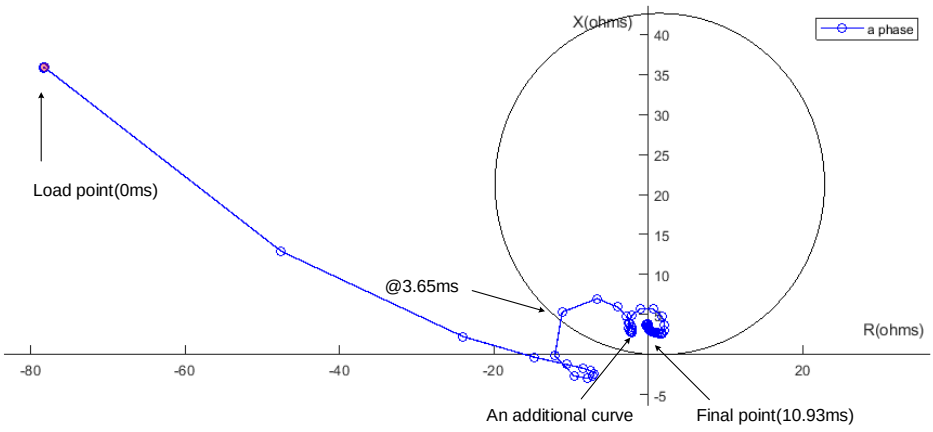

Figure 4.9 mho trajectory of zero-point fault in transmission line which SIR = 4, with CCVT

locus swings out of the mho circle at 9.17 ms, and settles into the mho circle again at 19.50 ms with a slow convergence speed, which makes the trip signal to happen 0.65 cycles later compared to the 8.60 ms when the CCVT is not present. Considering the SIR equaling to 10 is a quite extreme condition, a 0.8 cycles trip delay margin is needed to obtain the secure trip command.

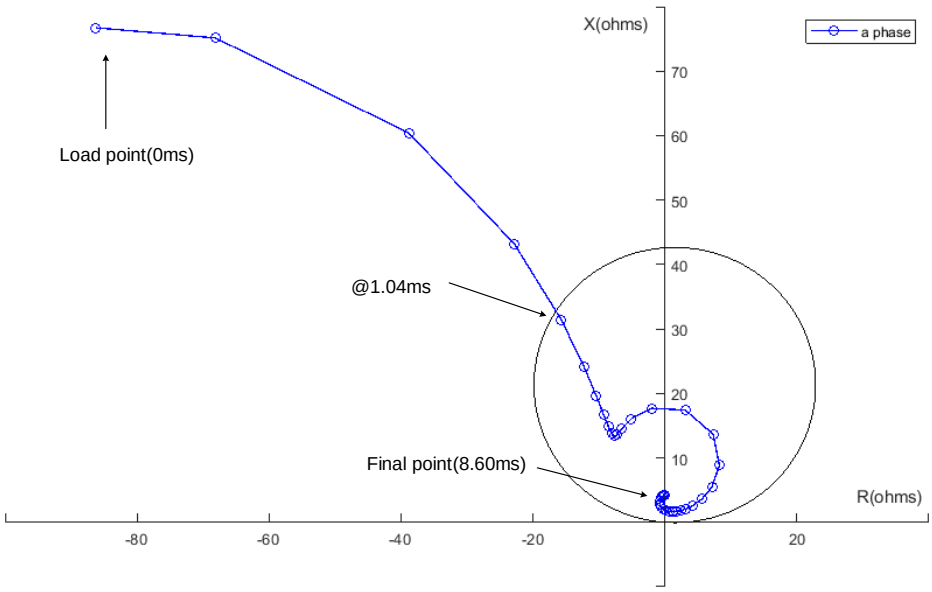

Figure 4.10 mho trajectory of zero-point fault in transmission line which SIR = 10, no CCVT

(4) **Scenario 4** (SIR = 10, Fault angle= 90 degree)

The impact of fault angle is shown in Figure 4.12. For the peak-point fault, the impedance locus converges into the mho circle at 9.84 ms, so the CCVT transient error does not have a noticeable impact on the tripping process.

4.3 Hardware Implementation on FPGA

In this section, a data interface module for distance relaying simulation is implemented on an Altera^{TM}FPGA board. Through this module, the fault file can be transported from RAM

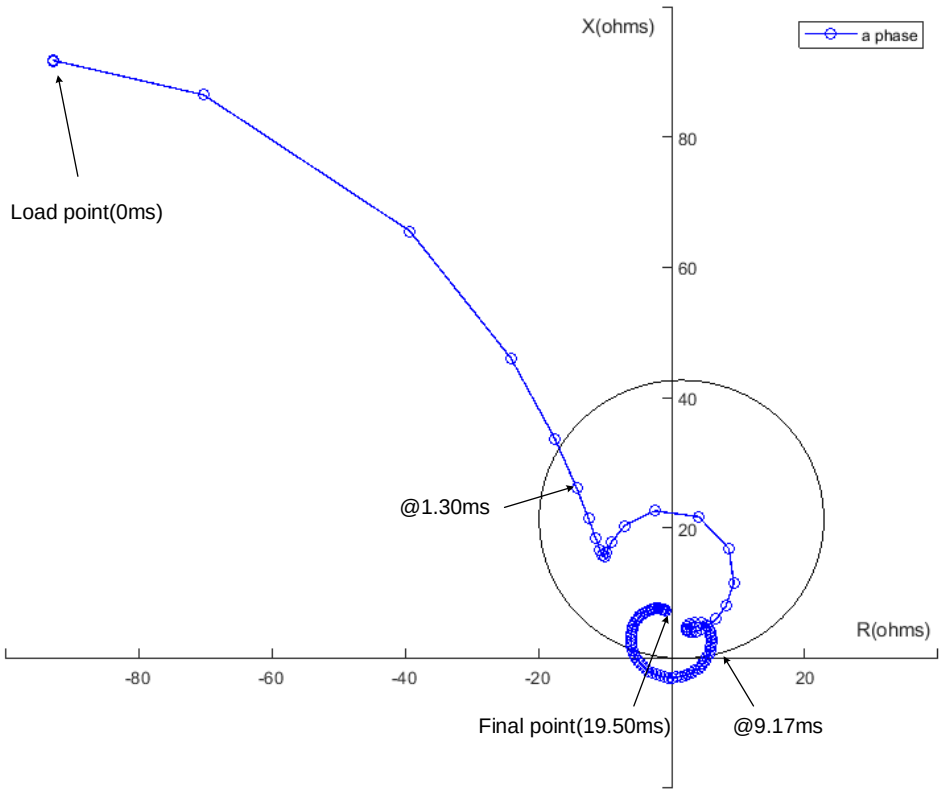

Figure 4.11 mho trajectory of zero-point fault in transmission line which SIR = 10, with CCVT

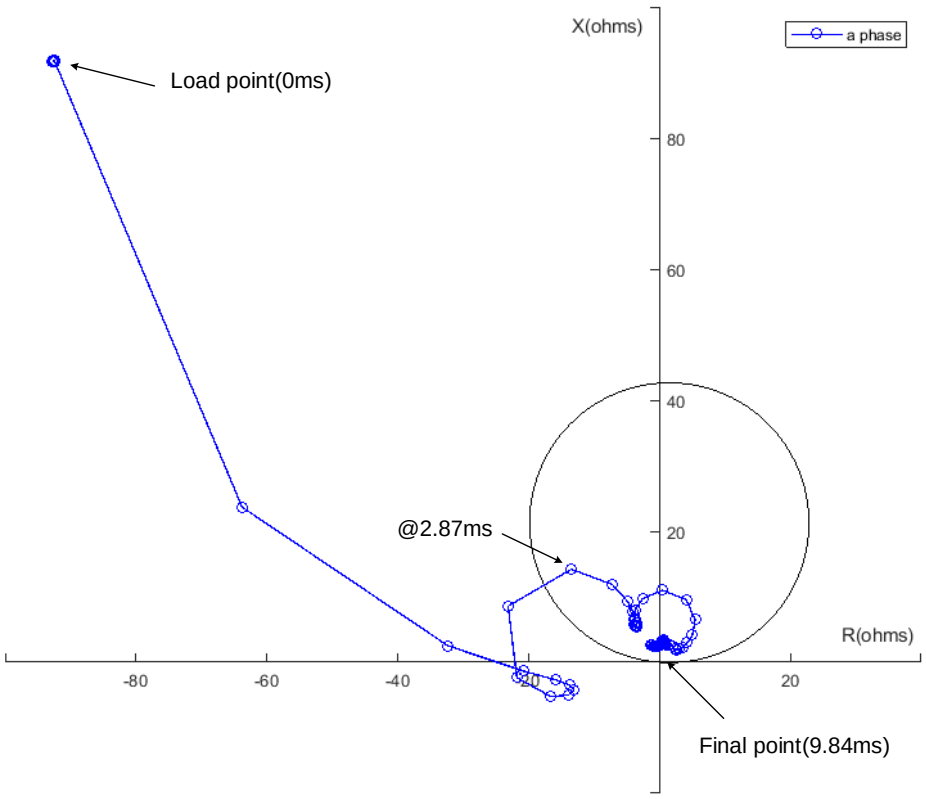

Figure 4.12 mho trajectory of peak-point fault in transmission line which SIR = 10, with CCVT

to registers on the FPGA, and the fault data in COMTRADE 99 format are transformed to a single-floating format that follows the IEEE 754 standard. In the next subsections, FPGA architecture, the design flow, and a case study will be presented.

4.3.1 The Generic FPGA Architecture

The FPGA is essentially a high-density array of unfixed logic cells, which can be built to modular hardware with specific function by partitioning and routing the infrastructure in the field. The main advantage of FPGAs is the highly efficient parallel computing structure and short time-to-market due to abundant IP (Intellectual Property) cores and peripheral I/Os (Input/Output). Furthermore, FPGA devices are able to handle sophisticated, high-speed control and data processing requirements by using a hardware description language (HDL) such as VHDL or Verilog.

Nowadays, FPGA technology is widely used in various areas: industrial control, defense applications, customer applications such as network servers, routers, smart terminals, etc. FPGAs have also been used for real-time modeling and simulation for power system and electronic equipment in recent years [21, 22, 23]. The major FPGA vendors in the market are Xilinx®and Altera ®.

The FPGA is generally composed of three types of programmable logic components: Logic Fabric, configurable I/O blocks, and configurable interconnections. A typical architecture of FPGA is shown in Figure 4.13. The I/O blocks are located around the periphery of the chip, providing programmable I/O connections. All the user-defined functional elements are achieved by Logic Fabric that is composed of several basic logic building blocks, for example, Logic Elements, DSP and Embedded Memory. These blocks are connected to programmable switch matrix and can implement sequential as well as combinational circuits.

The following subsections will introduce the Altera Stratix-IV FPGA [36] which is utilized in this research for distance relay design.

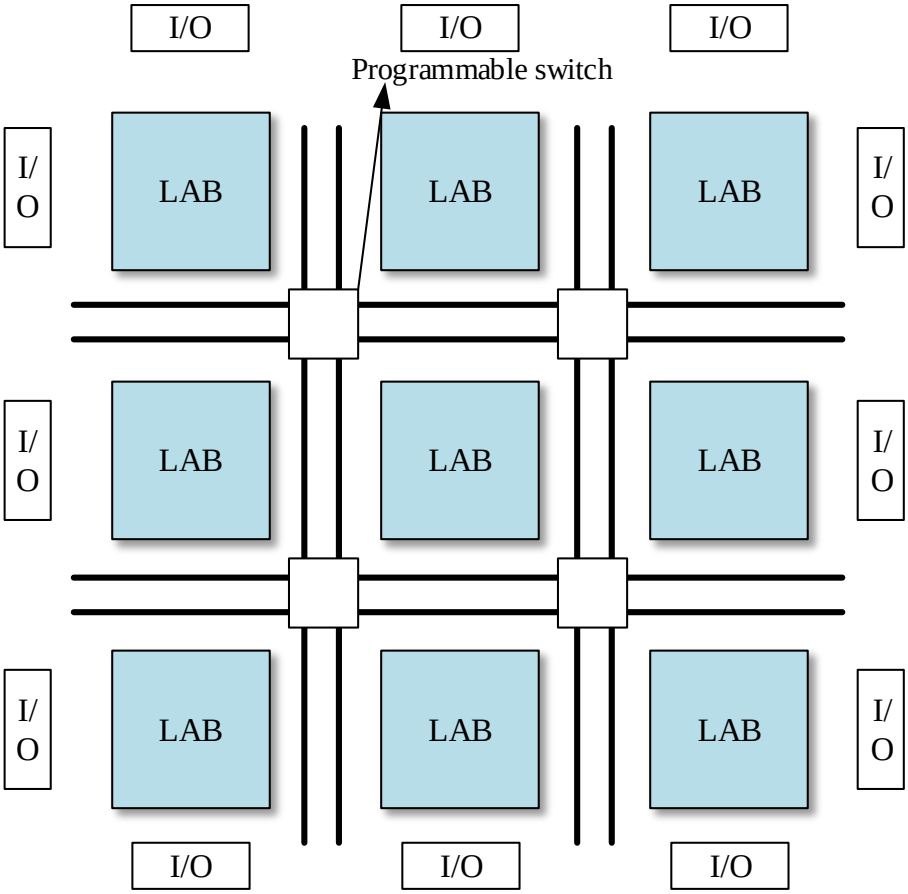

Figure 4.13 Generic FPGA architecture and components

4.3.2 The Altera Stratix-IV FPGA

The Stratix-IV FPGA significantly improved system performance and capacity compared to previous generations, which makes it suitable for the proposed design due to the high-density fabric, I/O bandwidth and up to 50% lower power consumption than other high-end FPGAs in the market. The primary logic components for implementing the design are presented as follows.

(1) **LABs**

One Logic Array Block(LAB) contains ten Adaptive Logic Modules (ALM) that are composed of two 6-input look-up table (LUT), two dedicated full adders, two programmable registers such as the flip-flop (FF) and latch, and a carry chain as shown in Figure 4.14. With up to eight inputs for the two combinational LUTs, one ALM can implement various combinations of two functions, and it can also execute any function with up to six inputs and specific seven-input functions. Further down the logical hierarchy of ALM, these basic logic elements such as adders and registers provide functions including logic and arithmetic operations. The LABs are main logic resources for implementing logic circuits with a connection to the programmable switch matrix, and half of the LABs can be configured as Memory LAB which supports a maximum of 640 bits of simple dual-port static random access memory (SRAM). It is worth to mention that FPGA device capacity is often measured in terms of logic cells, which are the logical equivalent of a classic four-input LUT. The ratio between the number of logic cells (four-input LUT)and 6-input LUTs is 1.6:1.

(2) **Memory Blocks**

The embedded memory blocks in Stratix IV devices provide three different sizes of embedded SRAM to address the needs of FPGA designs efficiently: 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks, which are used for data storage, FIFO(First In First Out) buffering, large shift registers, large look-up tables, or ROMs (Read Only Memory). When used for data storage, these block RAM can be configured in single-port or dual-port mode as shown in Figure 4.15. The single-port RAM has the data, data address, write enable and clock inputs. The simple dual-port block RAM has one

read-only port and one write-only port with independent clocks. The true dual-port block RAM has two utterly independent access ports, i.e. A and B. Data can be written to or read from either or both ports. Under the true dual-port mode, it can double the throughput of original RAMs.

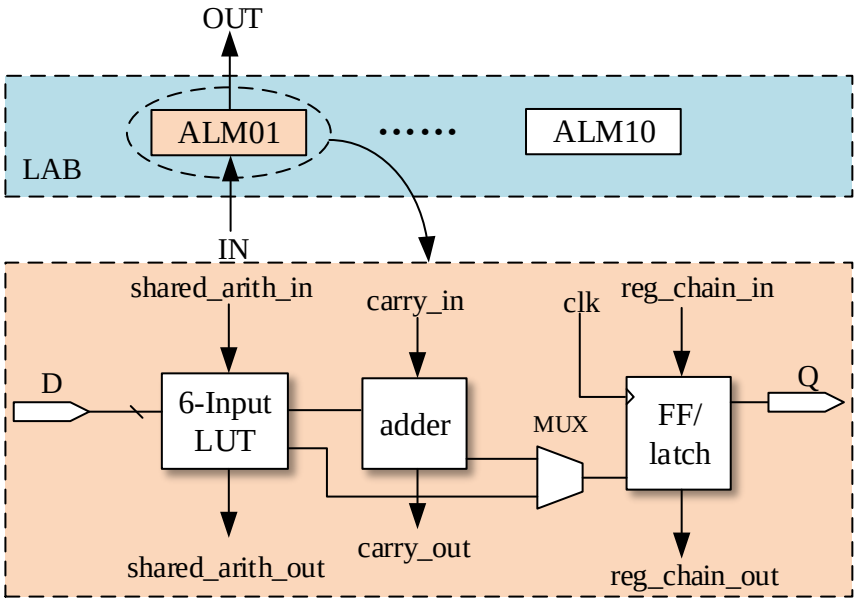

Figure 4.14 LAB unit in FPGA

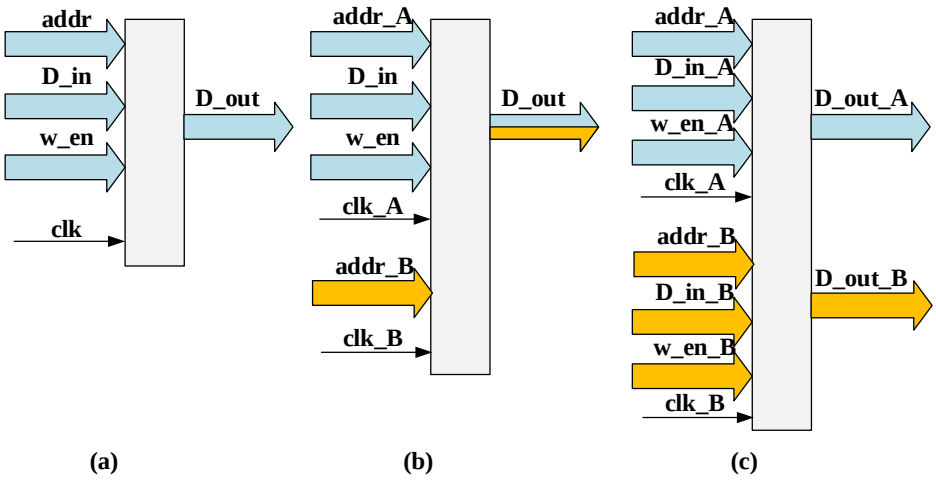

Figure 4.15 memory block unit in FPGA

(3) **DSP**

Modern FPGAs not only provide a large capacity of configurable logic gates but also integrate embedded IP (Intellectual Property) cores, for example, DSP blocks, to facilitate the implementation of the design. The DSP block consists of two identical halves (the top half and bottom half). Each half has four 18 × 18 multipliers. There are also registers, accumulators and many other logic units within the block can help implement high data throughput and computationally intensive applications such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and encoders. The DSP blocks have features like chain cascade mode, automatic optimization mode, and full-custom mode. Figure 4.16 shows the basic functionality of the DSP block.

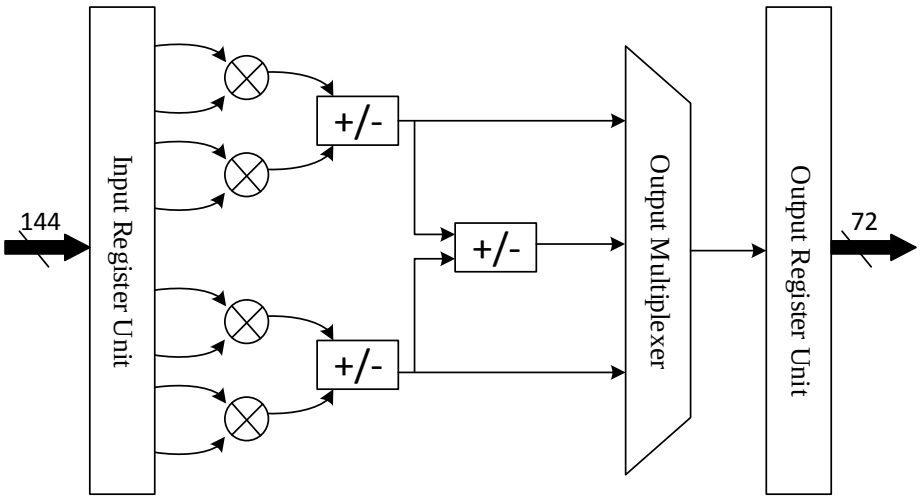

Figure 4.16 DSP unit in FPGA

4.3.3 FPGA Design Flow

Various design tools are available to accomplish synthesis and compilation, from design in hardware languages such as Verilog or VHDL all the way down to a bit-stream file that can be downloaded to FPGA chips. The two mainstream software tools are Quartus II for Altera FPGA and ISE for Xilinx FPGA. Here, Quartus II software suite is used for the protective relay hardware emulation because the Altera FPGA is utilized. The applications include module design, verification, debugging, and implementation. A typical FPGA design

flow is shown in Figure 4.17. It mainly consists of seven steps: design specification, HDL coding, behavioral simulations, synthesis, implementation, timing analysis, and verification of a device.

• **Design Specification**: The first step to undertake is understanding the standards of the design. According to the overall functional and resource requirements of the project, the most suitable FPGA platform can be determined. After the whole model is broken down into several functional modules, the description of each module's architecture, data flows, and the control signals interface between modules should be considered, e.g., the maximum operating frequency of the design, the I/O bandwidths, etc. Therefore, the output of this step is generally a graph describing the system architecture and functions, interconnections of functional modules, and design constraints.

•**HDL Coding**: When the design specifications are done, register transfer level (RTL) codes can be written to realize the design functions. The programming languages are usually Verilog HDL or VHDL. There are two kinds of programming styles: behavior-oriented and structure-oriented. The former is easier to understand and good at handling large and intricate designs, while the latter has better operating efficiency by manipulating the abstractions of components.

•**Behavioral Simulation**: With the coded HDL design, the next step is to do a behavioral simulation to see if the function of each module is valid. Generally, the simulation starts with the lowest level submodules, after which a higher level module can be simulated. The behavioral simulation is very fundamental because if the simulation does not generate correct outputs, the next several steps will not work either. Moreover, debugging an error in this step costs less time than in the rest of the design. In Altera Quartus II software, the ModelSim can be used to do the simulations.

• **Synthesis**: This step is to transform the high-level language code (Verilog or VHDL) into the device netlist. The netlist is essentially a standard schematic with logic elements, such as flip-flops, gates, phase lock loop (PLL), etc. Synthesis tools in the software suite will check code syntax for compatibility and analyze the architecture of the design for resource

optimization.

• **Implementation**: This step contains four procedures: compilation, mapping, pins distribution, and place-and-route. All of the logic elements are mapped to the FPGAs and are routed to realize the designed functions. Recent software tools provide some options in this step, such as size priority or performance priority. When the implementation is done, a binary stream configuration file that contains the whole design can be produced.

• **Timing Analysis**: Specific tools check if the design meets the timing constraints because it is necessary for all modules to be synchronously operating so that parallel operation is realized. The output of this step is the maximum clock frequency at which the design can be running and the slack time for all of the working paths. If the clock frequency is not satisfied with the specifications, the critical working path can be found and optimized to reach the desired frequency.

• **Download and Verify**: After the previous work has been done, the design is ready to be verified on FPGA devices. The binary stream file then can be transferred into the FPGA device. The function and outputs of the design are verified to ensure it is operating correctly. Programmers may use software like Signaltap or digital oscilloscopes to check the outputs.

4.3.4 Case Study

The two major features that allow an FPGA to improve speed and throughput are parallel processing and pipelining techniques. For parallel processing, FPGAs are simply arrays of programmable gates and so they can be combined into many individual hardware units with arbitrary size. Different operations can be processed at the same moment and do not need to compete for the same resources. For pipelining, operations can be inserted in data flip-flops (DFF) between steps to preserve the output of the last step for next step operation. Then, a critical path is assembled by wiring the inputs and outputs of each step into a line, so different steps in the critical path can operate at the same time. Although the latency of a single step is increased due to the delay of the DFFs, the total latency for a big batch of work can be reduced. Assuming there are three steps of operations, each with a latency of

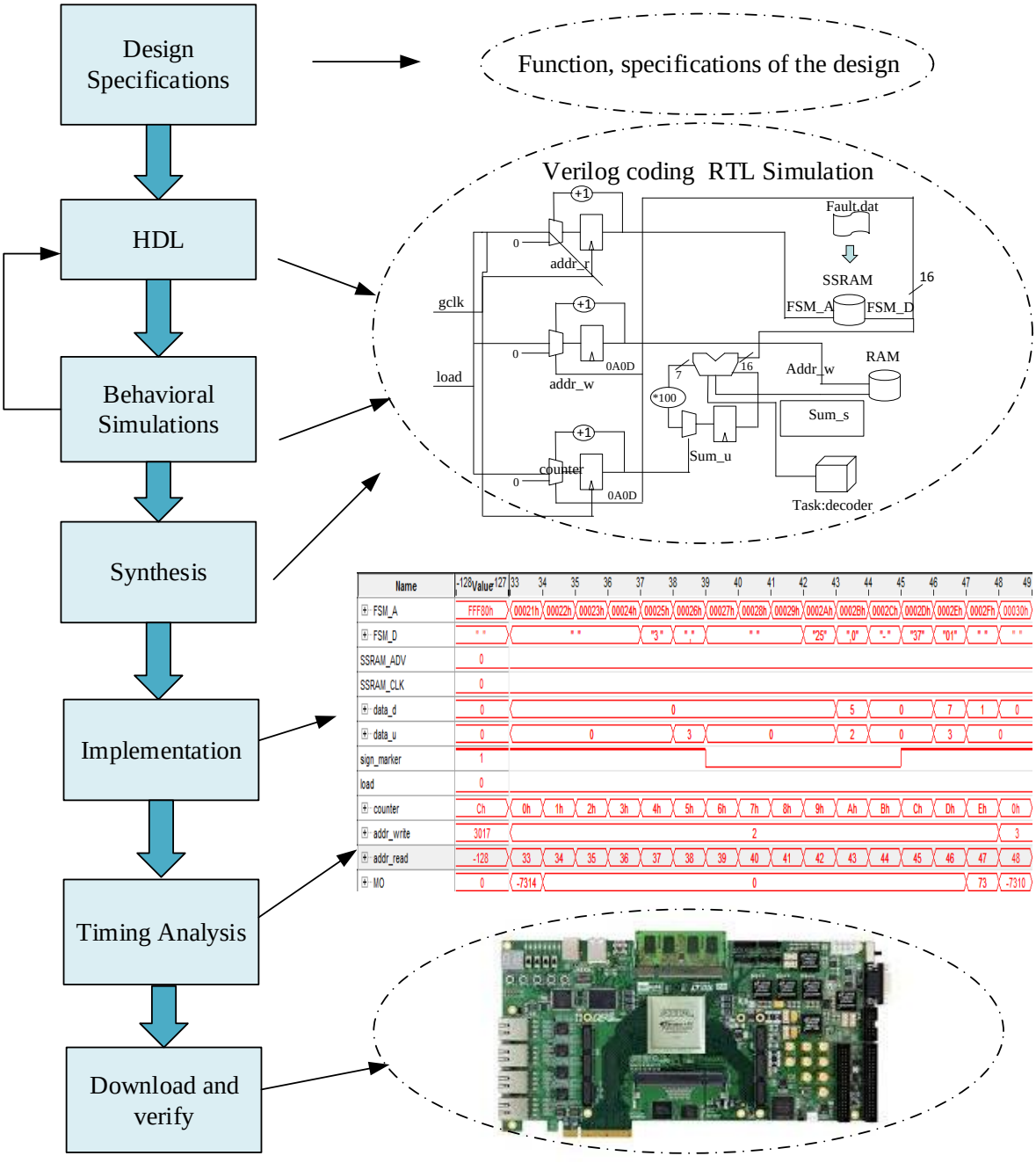

Figure 4.17 Flow chart FPGA design

N clock cycles, then the latency for the critical path is $3N$ clock cycles. If inputs are given a new value continuously, then only the first calculation output takes an initial $3N$ clock cycles to generate; however, there will be a new output in N clock cycles.

To fulfill a functional module on FPGA, we need to perform three fundamental developing steps: logic design, RTL design, and Verilog coding. In this subsection, they will be presented with a design case of a data interface module. There are two parts in this module: uploading fault signals in a COMTRADE 99 file from RAM to registers, and transforming the COMTRADE 99 format data into IEEE 754 standard floating-point binary data. In this thesis, the first part is used to show RTL design step and the second part is used to show logic design step.

(a) **Logic Design**

The goal of the logic design is to break down the functional module into combinational logic components or a sequential logic flow. The combinational logic is made of several or/and/not digital logic gates and used for building a logical judgment branch, while sequential logic is used for the general operation process, which is synchronized with clocks generated by crystal chips on FPGA. First, when a power system is simulated in PSCAD, there are two types of files generated simultaneously in the COMTRADE 99 protocol: Setting file and Data file. When extracting fault data from the COMTRADE 99 files, the sample values y are calculated using the equation $y = Mx + N$, where x is quantized records stored in data files, which range from -32678 to 32677, and M and N are constants saved in setting files. Next, to transform one certain x to y taking advantage of parallel processing, the calculation could be divided into three parallel paths: the sign and highest digit, two middle digits, and two lowest digits. Figure 4.18 shows the design diagram. Then, for the most time-consuming critical path, there are four steps of operations to be done sequentially: two adders and two multipliers. Since an adder costs two more clocks than a multiplier, a two-clock-delay DFF needs to be inserted between an adder and a multiplier to fulfill the pipelining feature. Therefore, in terms of one x, it takes 28 clock cycles to obtain the calculation result y. However, as the input x is given a new value, there will be a new result every seven clock cycles until all of the x in the COMTRADE file are transformed.

(b) **RTL Design**

The role of RTL design is to act as the bridge connecting high-level logic design and low-level Verilog coding. In addition to the data flow in logic design, control signals such as *enable* and *clock* signals also need to be specified in this stage to make sure the components work correctly. State machines and counters are utilized to synchronize all of the first-level components such as registers, RAM/ROM, and adder/multiplier to cooperate under the same global clock. Figure 4.19 illustrates the RTL design for the data uploading part.

(c) **Verilog coding**

After the RTL design is done, the diagram is translated into Verilog code. In this case, the data uploading part is broken down into three components: reader, decoder, and assembler. A typical COMTRADE 99 data file is shown in Figure 4.20. The second column is the timestamp, which is in μm units and the interval is 260, which means that a sample value would be generated every 260 μm according to a sampling rate of 3840 samples/s. The third

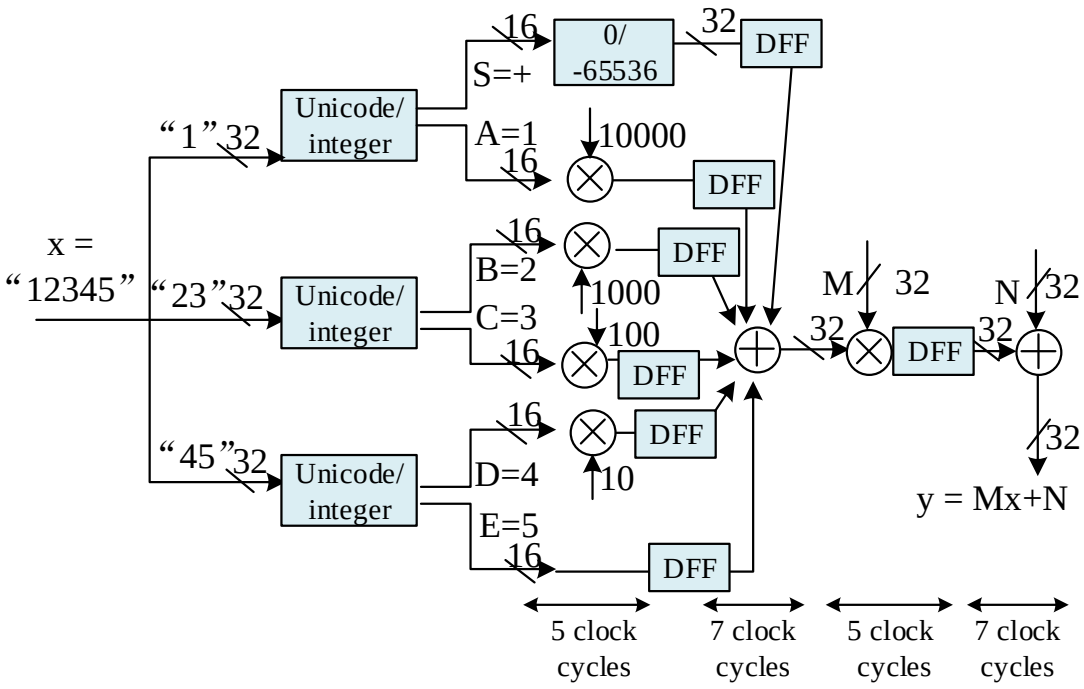

Figure 4.18 Logic design diagram for data transformation

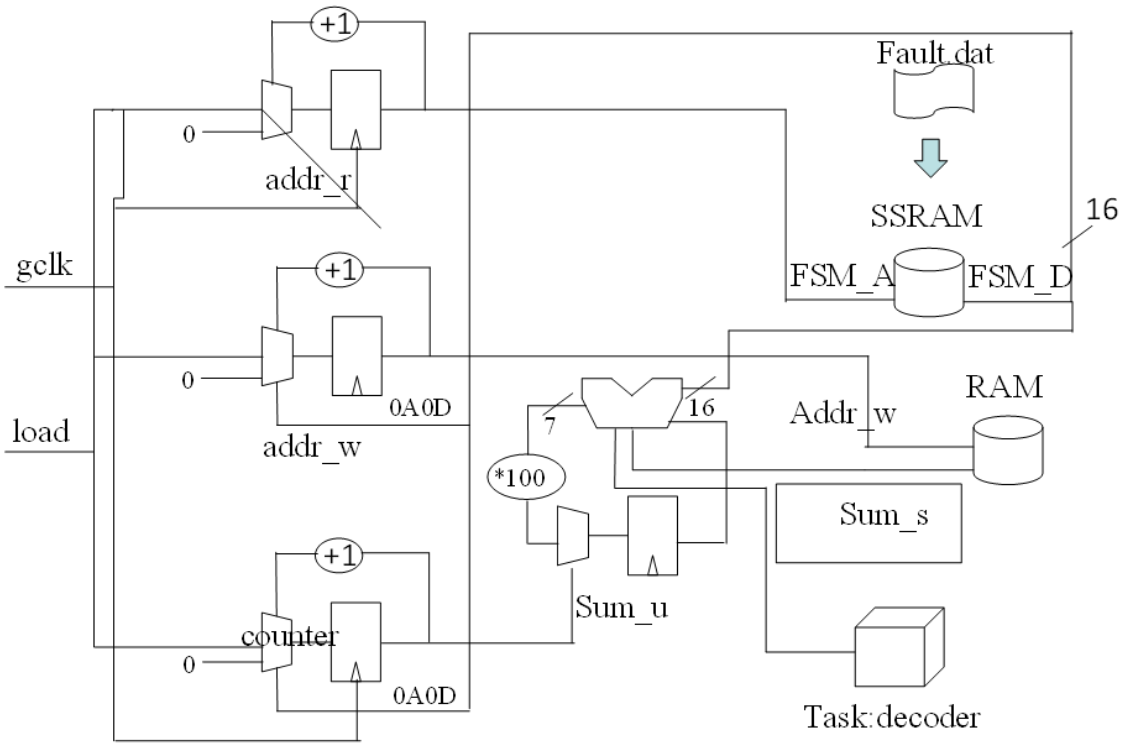

Figure 4.19 RTL design diagram for data uploading

column is the sample values, which range from -32678 to 32677. Noticed that all of the values in this table are strictly aligned, which is convenient for a machine to recognize them. Taking the third sample value of -7310 for instance, the data uploading process result can be shown in the timing diagram in Figure 4.21 step by step, as follows.

(1) First, the data are read from RAM and stored into registers through the I/O interface. Because the bandwidth of the interface for the FPGA bus is 32-bit and the data are coded in 16-bit ASCII format, two digits of data can be transferred from RAM into registers every single clock.

(2) Second, the data pair is divided into two digits, which are $data\_d$ and $data\_u$, and they are transformed individually from ASCII format into two'complement binary format with a decoder.

(3) Next, every three pairs of data are assembled into the final output, which is stored in a register called MO. For every 15 clocks, a sample value uploaded in this fashion. Because there are six groups of data -three phase voltages and three phase currents- need to be uploaded, then the total time of 90 clocks needs to be smaller than 260 μs to fulfill a real-time interface. On the other hand, FPGA can work at a 100 MHz clock rate (up to 156.25 MHz for this board [36]), so one clock takes 0.01 μs. Because the uploading time for one sample of $90 \times 0.01 = 0.9$ μs is much smaller than 260 μs, the designed interface module can handle the data sampling in a real-time fashion.

4.4 Summary

In this chapter, the case study shows that CT saturation does not have a substantial impact on LES-based relaying because the saturation generally occurs 1.1∼1.25 cycles post-fault, which is after the time required for the LES relay to obtain a secure estimation result. For the CCVT transient, as the SIR increases there is an incremental delay in the operating time of the proposed relaying. However, the performance does not obviously deteriorate until the SIR increases above 10. Last, in this chapter, an FPGA design procedure is proposed with a data interface module by which the fault signals in COMTRADE file are uploaded

1, 0, -7315
2, 260, -7314
3, 520, -7310
4, 780, -7303
5, 1040, -7312
6, 1300, -7323
7, 1560, -7337
8, 1820, -7347
9, 2080, -7352
10, 2340, -7359

Figure 4.20 Fault data in COMTRADE 99 file

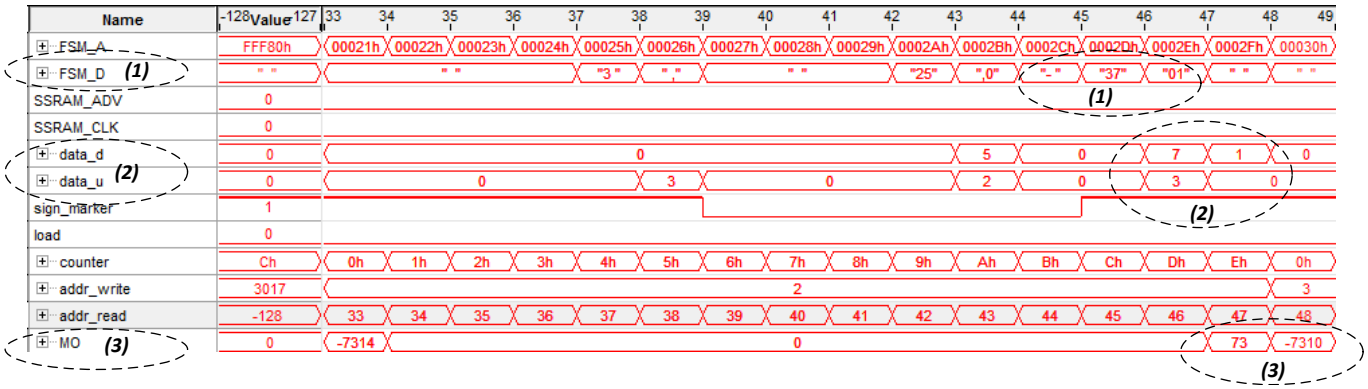

Figure 4.21 Transformed data of single-floating format displayed in Quartus Signal-Tap simulation tool

from RAM into registers and transformed into single-floating data.

Chapter 5

Conclusion

In this research work, an LES-based distance relaying algorithm is first proposed using a higher sample rate and shorter window length than in the existing literature. By testing other operational aspects such as CT saturation and CCVT transient error, a practical distance protection system has been created. The case studies show the operational effectiveness of the designed relay. Additionally, the data interfacing module is implemented on an FPGA board, and the resource usage and latency for the function is estimated with simulation results.

All of the relay submodules are developed in MATLAB and Verilog, which can be easily transplanted to different development environments. Taking advantage of the inherent flexibility and expandability of the LES method, the proposed distance relay can fit various scenarios. For the hardware implementation part, parallel architecture and pipelined workflow, the two critical features of FPGA, are taken into account to achieve high efficiency and low latency. The advantages of the LES-based protection design and future work are discussed in the following sections.

5.1 Advantages of the LES-based Relay

• The LES-based distance relaying is verified using the window lengths of seven and five. The proposed sub-cycle method is tested using off-line simulation data generated by

a PSCAD/EMTDC system to achieve better performance compared to current sub-cycle methods in the literature. The experimental test results show that the proposed relay can make a secure trip decision in 0.49∼0.70 cycles.

• The proposed relay has good reliability when responding to different faults with respect to both types and locations.

• The proposed relay shows robustness under a practical scenario where CT saturation and CCVT transients are present.

• The scheme is implemented on an FPGA board, which achieves data interface supporting real-time simulation up to a sampling rate of 1 MHz.

5.2 Future Work

The research in this thesis can be extended in the following ways.

Besides the data interface module on FPGA, other modules such as phasor estimation and trip logic can be developed to construct a complete hardware distance relay.

Also, the communication function could be enhanced on the existing system. Some new features such as Gigabit Ethernet and IEC 61850 could be supported to make the relay handle the data in a more efficient real-time manner.

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Appendix

System Parameters

Table 1 CT Parameters

CT ratio	800:5
Burden resistance R_b	1.2 Ω
Burden reactance X_b	0.189Ω
Secondary resistance R_s	0.1 Ω
Secondary reacance X_s	0.189Ω

Table 2 CCVT Parameters

C_1	2.92E-3μf	R_{F1}	5.5Ω
C_2	1.35E-1μf	L_{F1}	0.01H
L_C	42.0H	C_F	8.0μf
$VTRatio$	1600:1	R_{F2}	3.9Ω
R_P	0.05Ω	L_{F2}	0.394H
L_P	0.47E-3H	R_F	40.0Ω
R_S	0.18Ω	R_B	301.0Ω
L_S	0.47E-3H	L_B	2.4H
		R_{BP}	785.0Ω